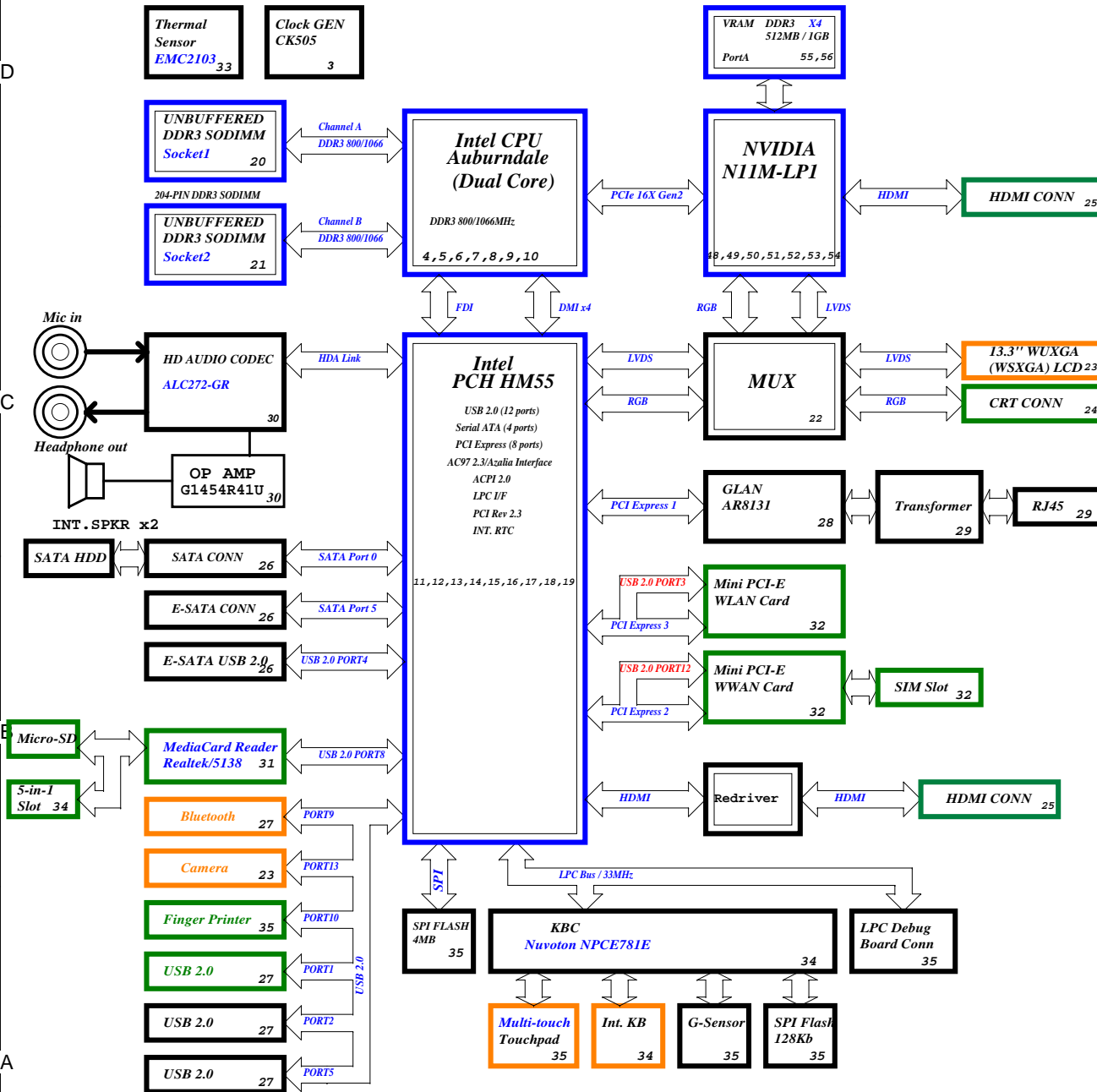


# LA36 Switchable Graphics System Schematics

Project Code: 91.4JG01.001  
PCB(Raw Card): 09939-1

## PCB LAYER

L1: Top  
L2: VCC/GND  
L3: Signal  
L4: Signal  
L5: GND  
L6: Boot



Finger Printer BD

BT BD

AV BD

CPU DC/DC  
ISL62882

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC  
RT8223BGQW

INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC  
RT8209E

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

SYSTEM DC/DC  
RT8209E

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC  
RT8209E

INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

LDO  
RT9025

INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

LDO  
RT9026

INPUTS	OUTPUTS
1D5V_S3	0D75_S0 DDR_VREF_S3

SYSTEM DC/DC  
ISL62881

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

SYSTEM DC/DC  
RT8208A

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0

CHARGER  
BQ24745

INPUTS	OUTPUTS
DCBATOUT	BT+

<Variant Name>

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Title	Block Diagram	Rev
Size	Document Number	LA36 MB
Customer		
Date	Monday, March 22, 2010	Sheet 1 of 58

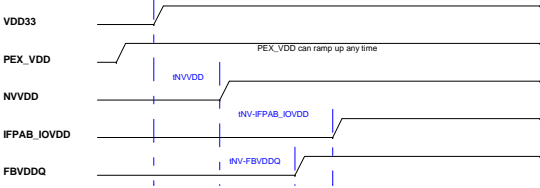
Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor <b>Note:</b> Only temporary for early CFD samples (rPCK/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

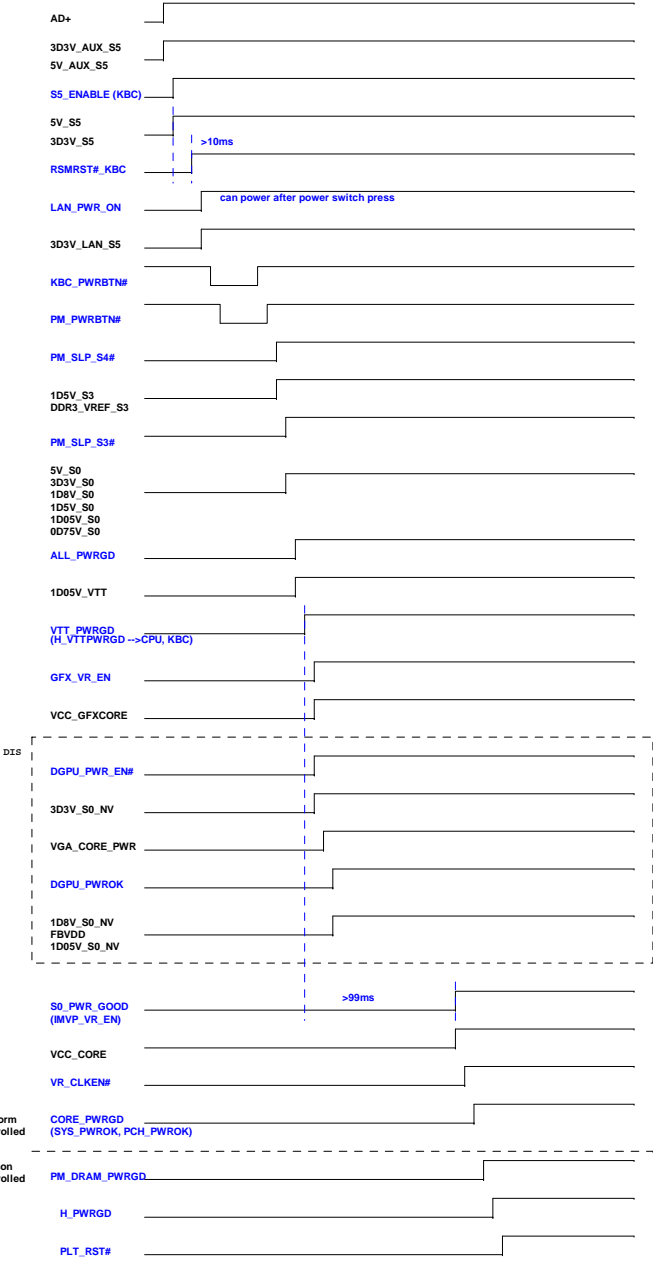
PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up <b>Default Mode:</b> Internal weak Pull-down. <b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	<b>Default Mode:</b> Internal pull-up. <b>Low (0) = Top Block Swap Mode</b> (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	<b>High (1) = Integrated VRM is enabled</b> <b>Low (0) = Integrated VRM is disabled</b>
GNT0#, GNT1#	<b>Default (SPI):</b> Left both GNT0# and GNT1# floating. No pull up required. <b>Boot from PCI:</b> Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. <b>Boot from LPC:</b> Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	<b>Default - Internal pull-up.</b> <b>Low (0)=</b> Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	<b>Default:</b> Do not pull low. <b>Disable ME in Manufacturing Mode:</b> Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	<b>Enable iTPM:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor <b>Disable iTPM:</b> Left floating, no pull-down required.
NV_ALE	<b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. <b>Disable Danbury:</b> Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	<b>Low (0):</b> Flash Descriptor Security will be overridden. <b>High (1) :</b> Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	<b>Default = Do not connect (floating)</b> High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

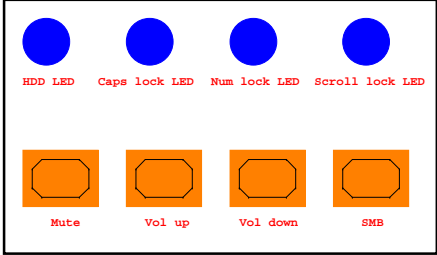
N11M-GE Power Sequence



Sequence AC

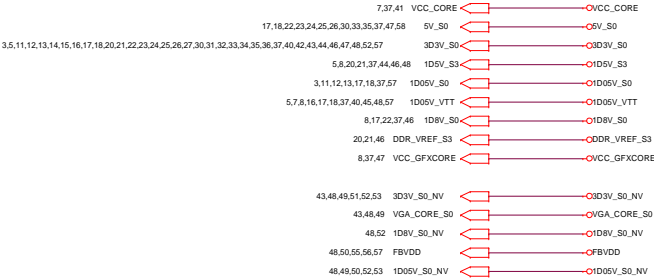


AV PANEL



PLANAR\_ID[1..0]

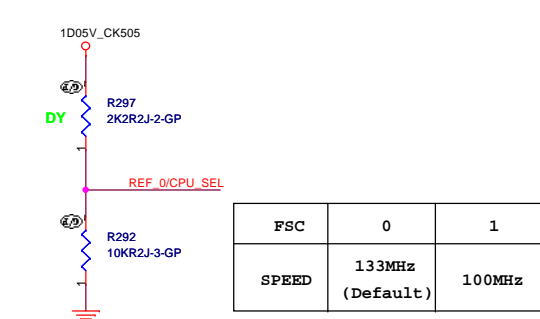
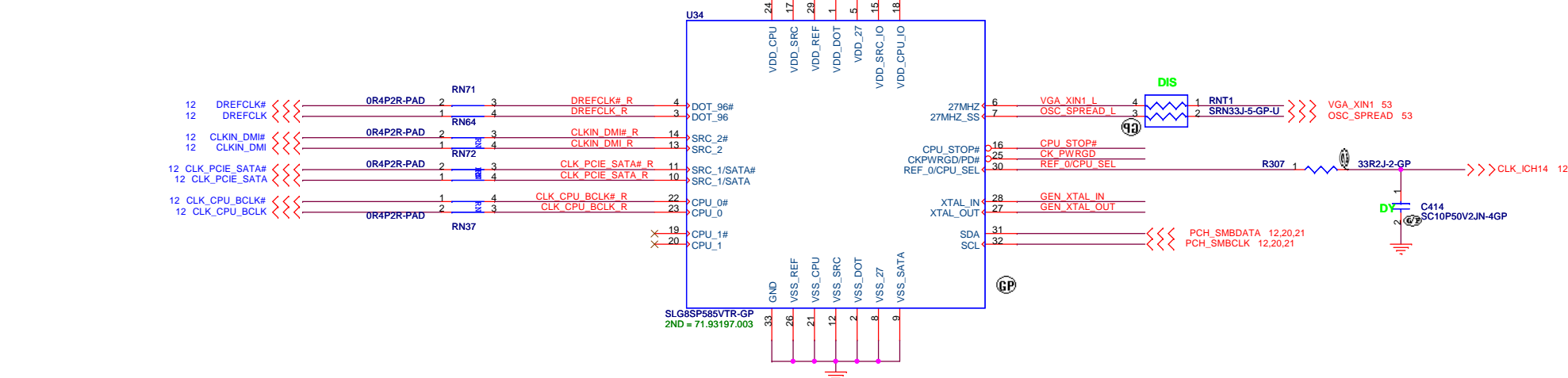
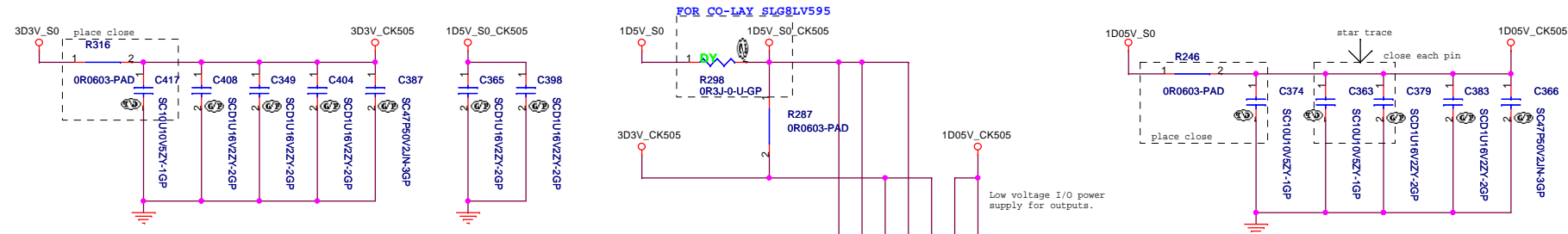
KBC GPin	31	23	Planar ID Version	Planar PCB Version
PLANAR_IDn	1	0		
	0	0	LA36 - SA	SA
	0	1		SB
	1	0		SC
	1	1		-1



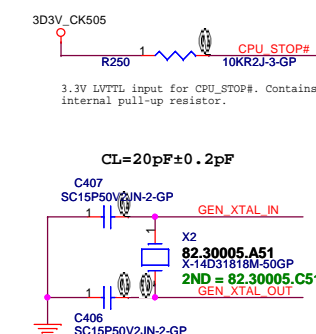
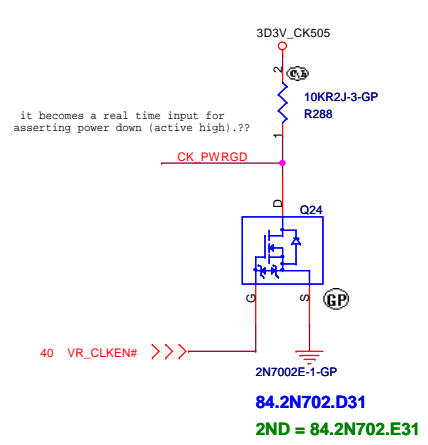
<Variant Name>

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Reference			
Size A2	Document Number	LA36 MB DIS	
Date: Monday, March 22, 2010	Sheet	2	of 58

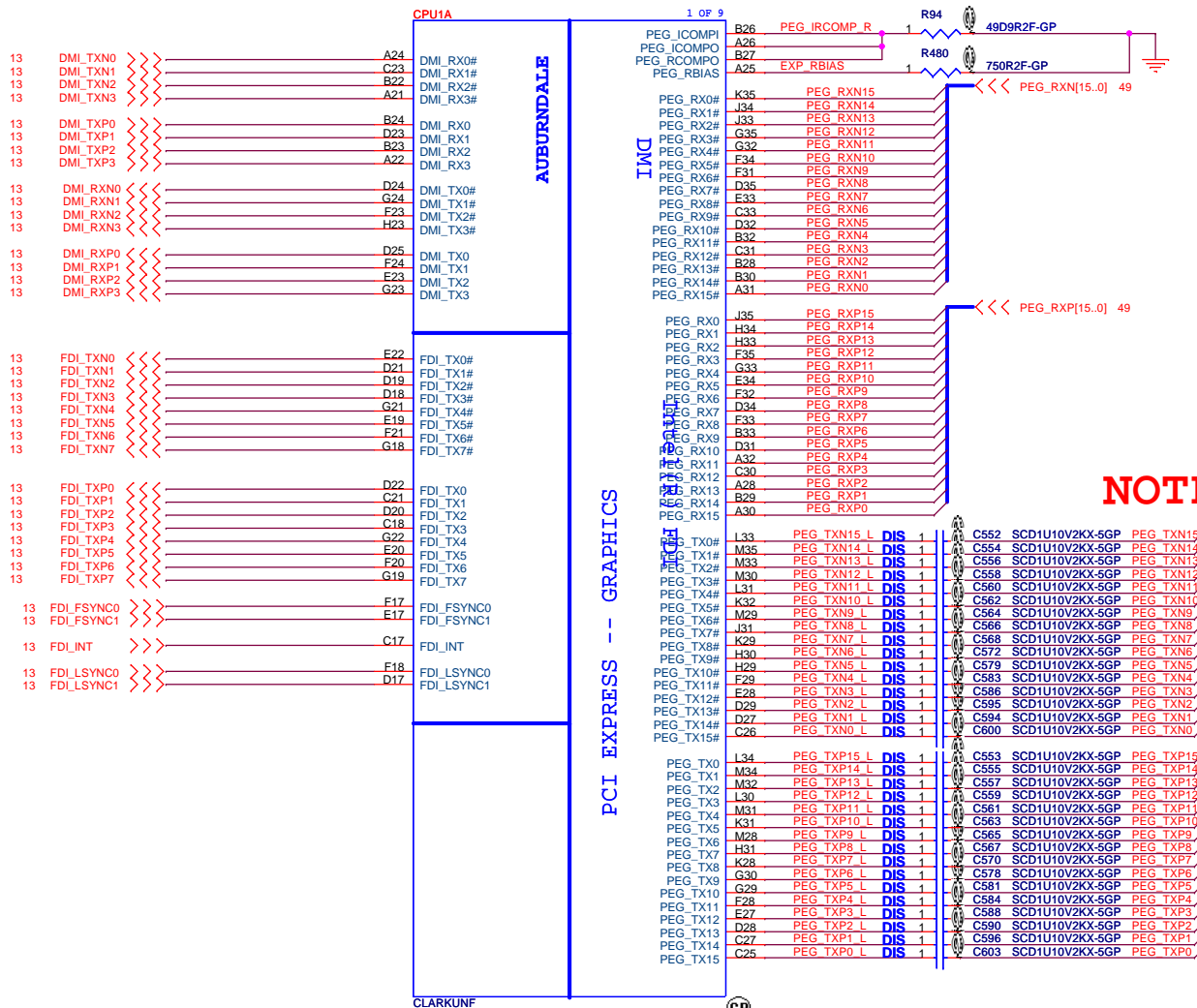


FSC	0	1
SPEED	133MHz (Default)	100MHz



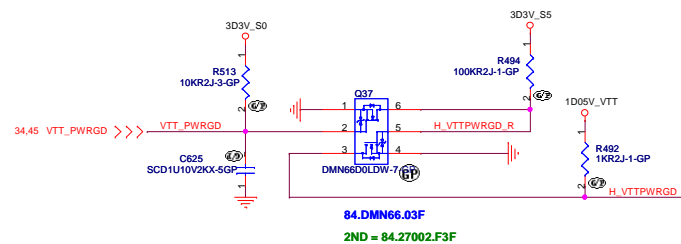
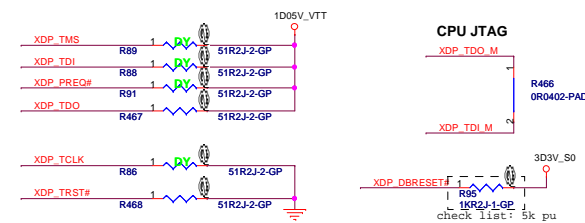
**Layout Notes:**

Make sure that the stubs to the test points(CK\_PWRGD, CLK\_EN#, GEN\_XTAL\_OUT) in the layout are as short as possible on the high speed signals.



NOTE SWAP TX0~15

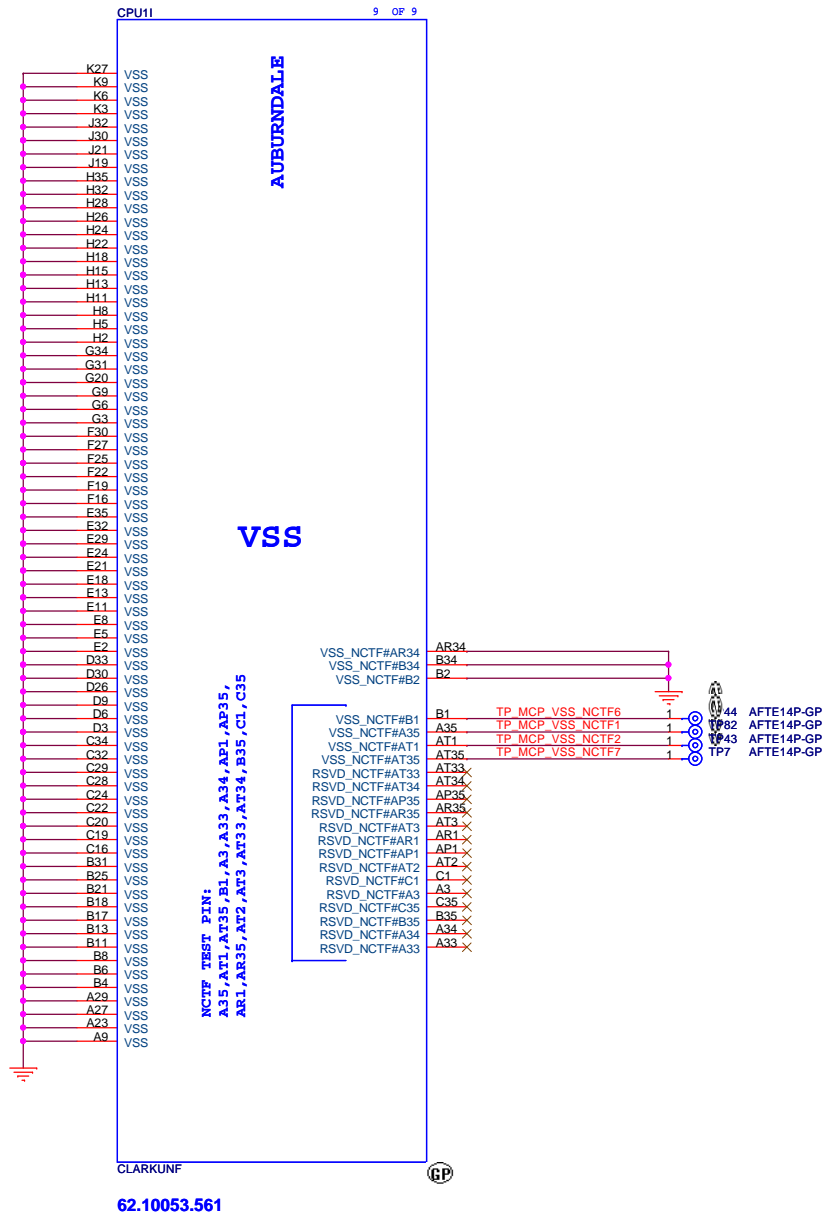
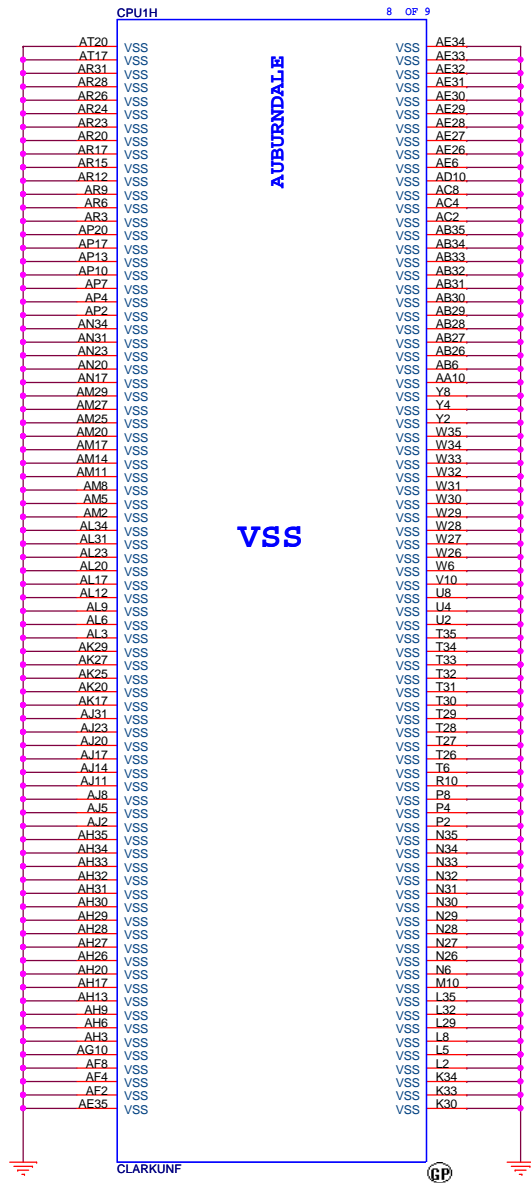
62.10053.561  
2ND = 62.10055.321





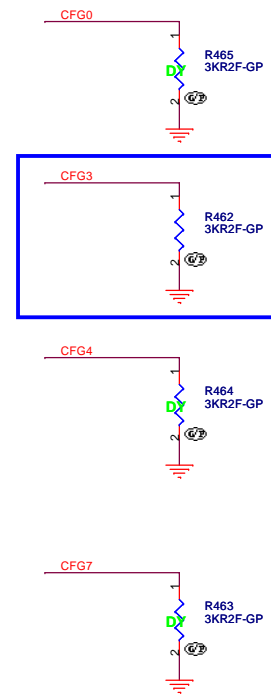






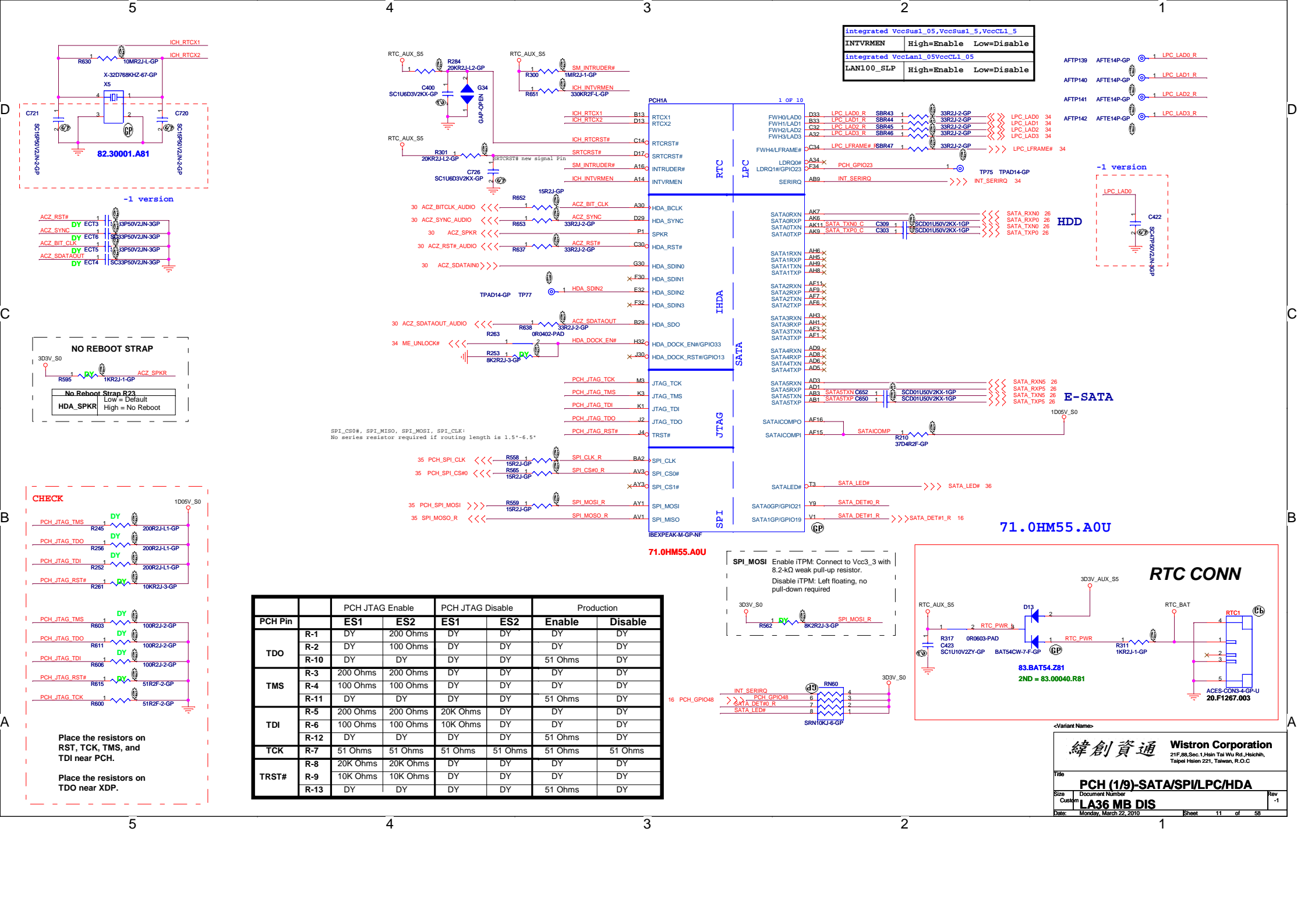
<Variant Name>

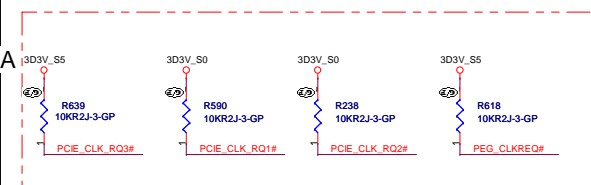
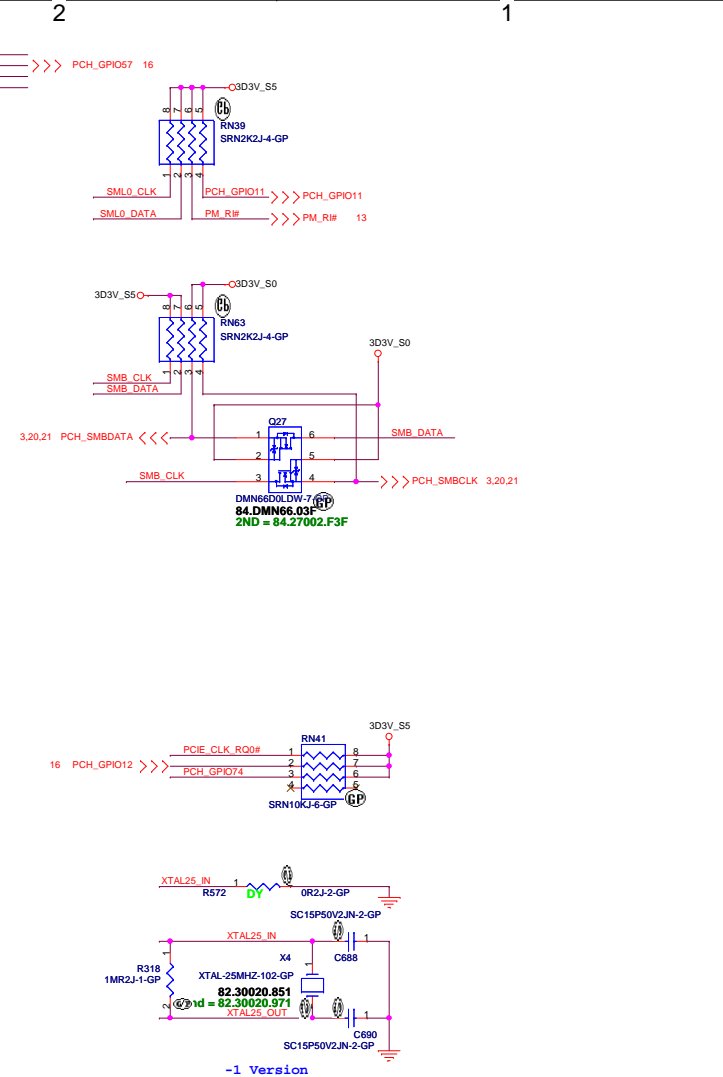
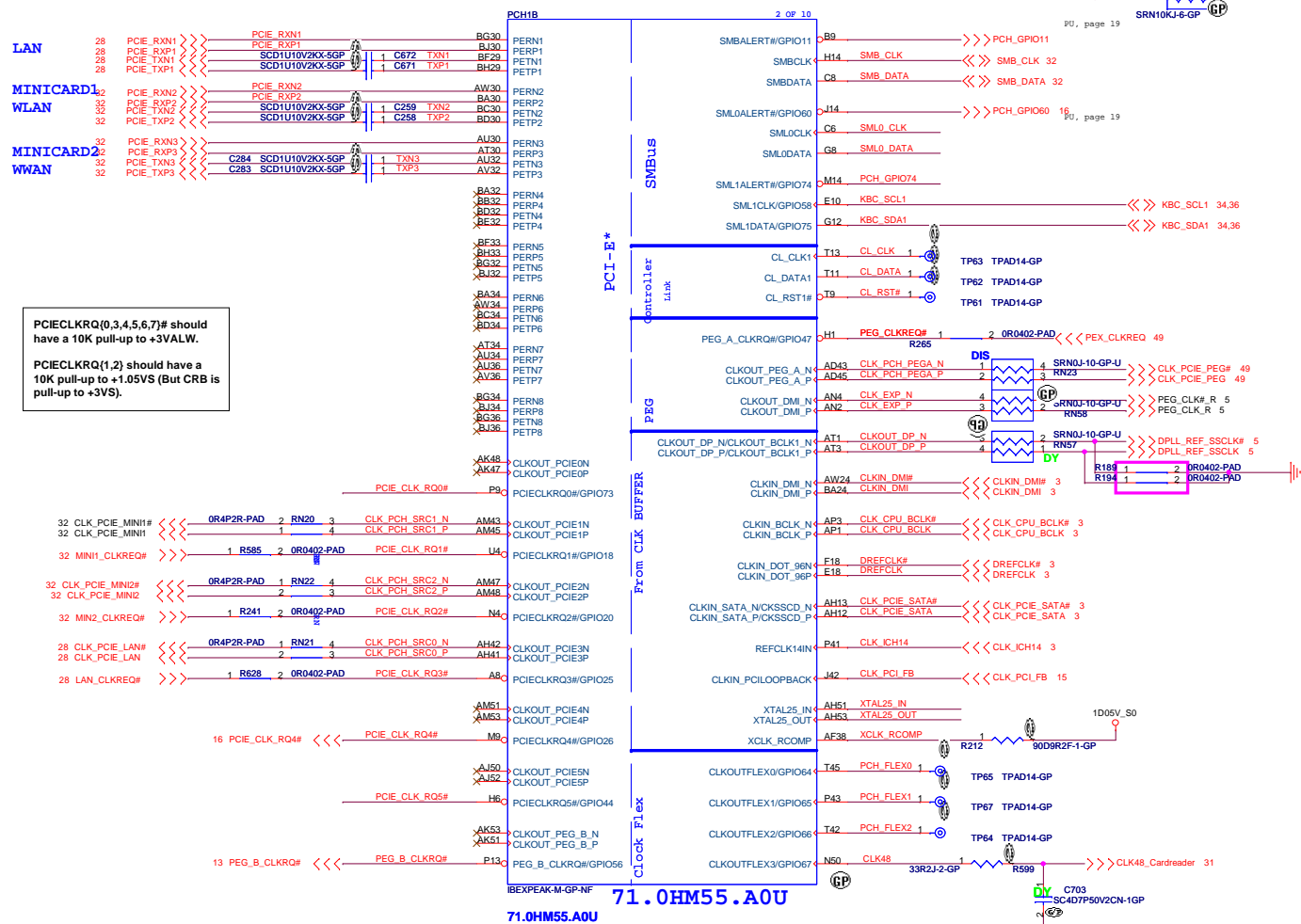
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File	
CPU (6/7)-VSS	
Size A3	Document Number
LA36 MB DIS	
Date: Monday, March 22, 2010	Sheet 9 of 58
Rev -1	

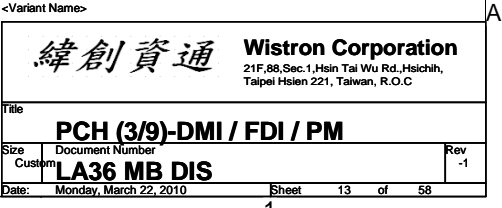


CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	<p>Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.</p> <p>Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.</p>

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

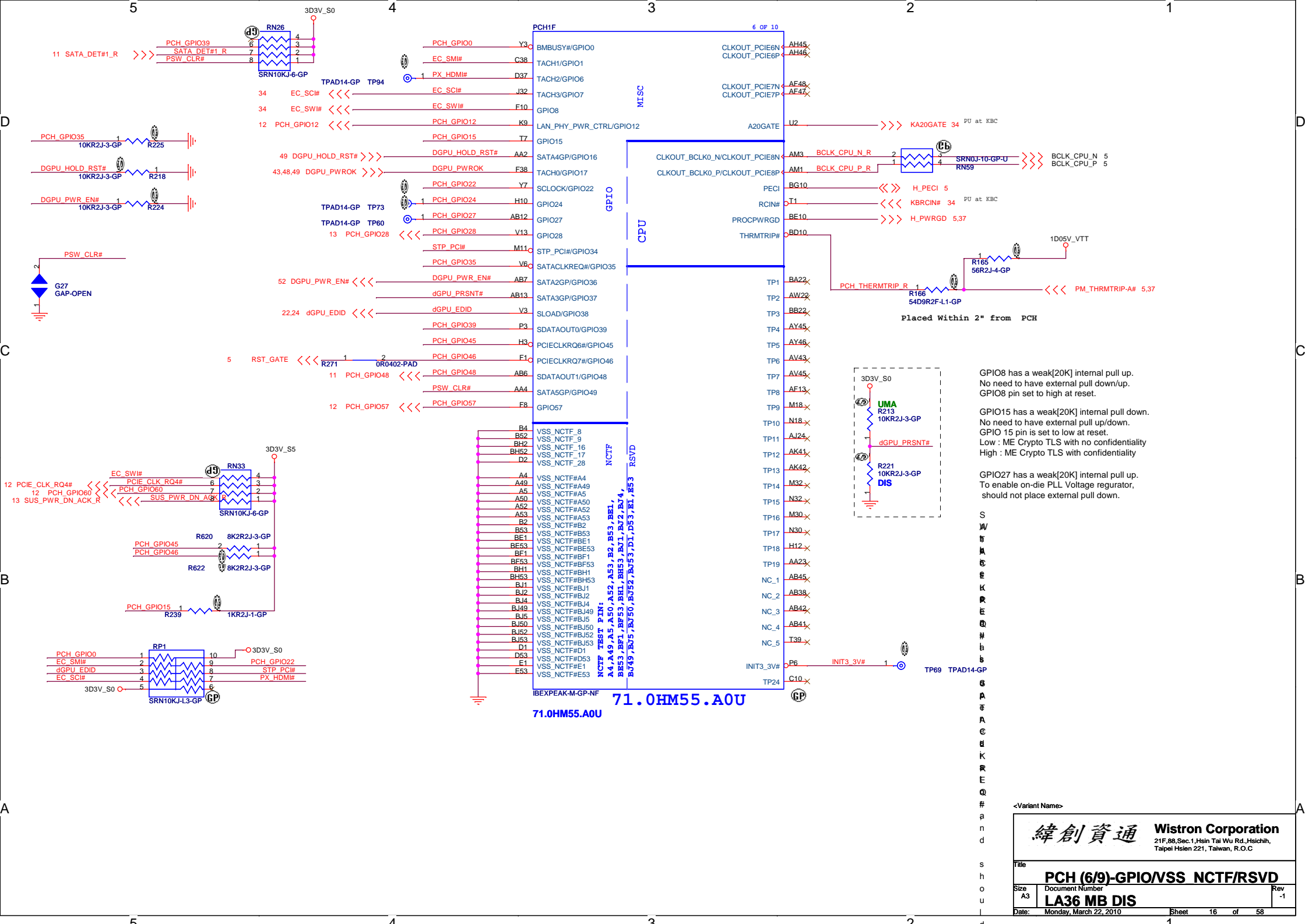
















PCH11 9 OF 10

AY7	VSS	H49
B11	VSS	H5
B15	VSS	J24
B19	VSS	K11
B23	VSS	K43
B31	VSS	K47
B35	VSS	K7
B39	VSS	L14
B43	VSS	L18
B47	VSS	L2
B7	VSS	L22
BG12	VSS	L32
BB12	VSS	L36
BB16	VSS	L40
BB20	VSS	L52
BB24	VSS	M12
BB30	VSS	M16
BB34	VSS	M20
BB38	VSS	N38
BB42	VSS	M34
BB49	VSS	M38
BB5	VSS	M42
BC10	VSS	M46
BC14	VSS	M49
BC18	VSS	M5
BC2	VSS	M8
BC22	VSS	N24
BC32	VSS	P11
BC36	VSS	AD15
BC40	VSS	P22
BC44	VSS	P30
BC52	VSS	P32
BH9	VSS	P34
BD48	VSS	P42
BD49	VSS	P45
BD5	VSS	P47
BE12	VSS	R2
BE16	VSS	R52
BE20	VSS	T12
BE24	VSS	T41
BE30	VSS	T46
BE34	VSS	T49
BE38	VSS	T5
BE42	VSS	T8
BE46	VSS	U30
BE48	VSS	U31
BE50	VSS	U32
BE6	VSS	U34
BE8	VSS	P38
BF3	VSS	V11
BF49	VSS	P16
BF51	VSS	V19
BG18	VSS	V20
BG24	VSS	V22
BG4	VSS	V30
BG50	VSS	V31
BP42	VSS	V32
BP46	VSS	V32
BH11	VSS	V34
BH15	VSS	V34
BH19	VSS	V35
BH23	VSS	V38
BH31	VSS	V43
BH35	VSS	V45
BH39	VSS	V46
BH43	VSS	V47
BH47	VSS	V49
BH7	VSS	V5
C12	VSS	V7
C50	VSS	V8
D51	VSS	W2
E12	VSS	W52
E16	VSS	Y11
E20	VSS	Y12
E24	VSS	Y15
E30	VSS	Y19
E34	VSS	Y23
E38	VSS	Y28
E42	VSS	Y30
E46	VSS	Y31
E48	VSS	Y32
E49	VSS	Y38
E6	VSS	Y43
E8	VSS	Y46
F49	VSS	P49
F5	VSS	Y5
G10	VSS	Y6
G14	VSS	Y8
G18	VSS	P24
G2	VSS	T43
G22	VSS	AD51
G32	VSS	AT9
G36	VSS	AD47
G40	VSS	Y47
G44	VSS	AT12
G52	VSS	AM6
AF39	VSS	AT13
H16	VSS	AM5
H20	VSS	AK45
H30	VSS	AK38
H34	VSS	AV14
H38	VSS	
H42	VSS	

IBEXPEAK-M-GP-NF 71.0HM55.A0U

PCH1H 8 OF 10

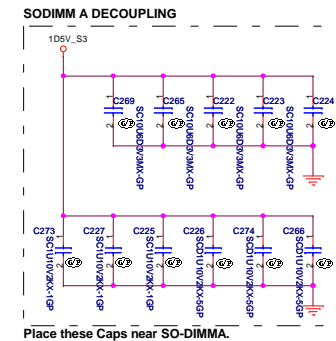
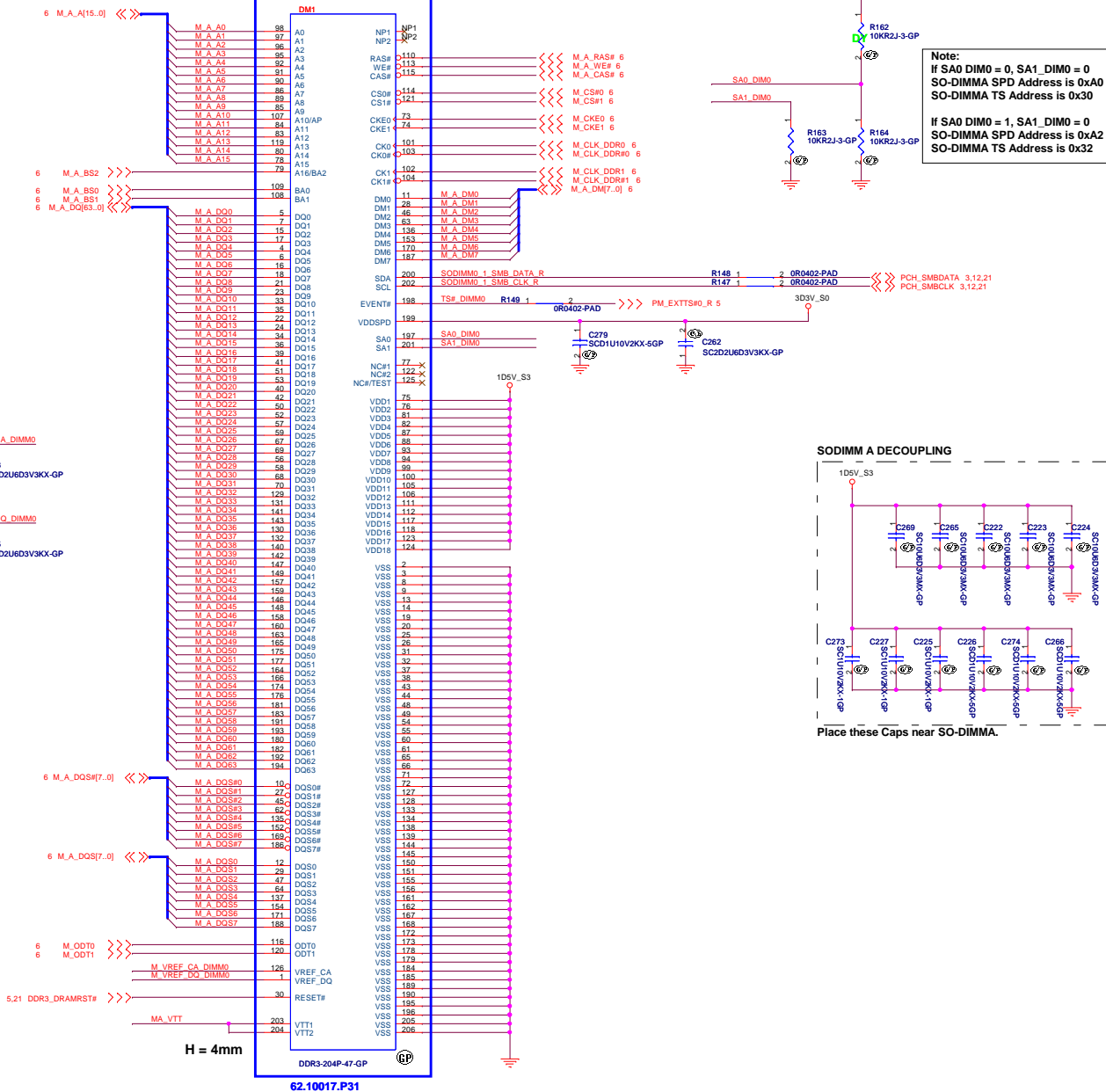
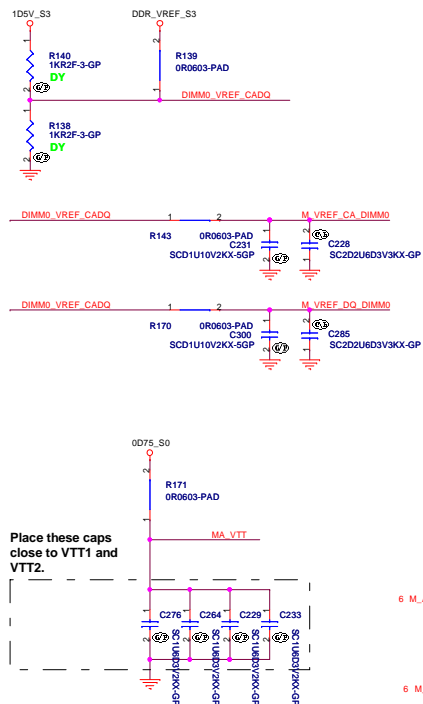
AB16	VSS	AK30
AA19	VSS	AK31
AA20	VSS	AK32
AA22	VSS	AK34
AM19	VSS	AK35
AA24	VSS	AK38
AA26	VSS	AK43
AA28	VSS	BB5
AA30	VSS	AK49
AA31	VSS	AK5
AA32	VSS	AK8
AB11	VSS	AL2
AB15	VSS	AL52
AB23	VSS	AM11
AB30	VSS	BB44
AB31	VSS	AD24
AB32	VSS	AD20
AB39	VSS	AM22
AB43	VSS	AM24
AB47	VSS	AM26
AB5	VSS	AM28
AB8	VSS	BA42
AC2	VSS	AM30
AC52	VSS	AM31
AD11	VSS	AM32
AD12	VSS	AM34
AD16	VSS	AM35
AD23	VSS	AM38
AD30	VSS	AM39
AD31	VSS	AM42
AD32	VSS	AU20
AD34	VSS	AM46
AU22	VSS	AV22
AD42	VSS	AM49
AD46	VSS	AM7
AD49	VSS	AA50
AD7	VSS	BB10
AE2	VSS	AN32
AE4	VSS	AN50
AF12	VSS	AN52
Y13	VSS	AP12
AH49	VSS	AP42
AU4	VSS	AP46
AF35	VSS	AP49
AP13	VSS	AP49
AN34	VSS	AP5
AF46	VSS	BH23
AF49	VSS	BH31
AF5	VSS	BH35
AF8	VSS	BH39
AG2	VSS	BH43
AG52	VSS	BH47
AH11	VSS	BH7
AH15	VSS	C12
AH16	VSS	AT41
AH24	VSS	AT47
AH32	VSS	AT7
AV18	VSS	AV12
AH43	VSS	AV16
AH47	VSS	AV20
AH7	VSS	AV24
AJ19	VSS	AV30
AJ2	VSS	AV34
AJ20	VSS	AV38
AJ22	VSS	AV42
AJ23	VSS	E46
AJ26	VSS	AV46
AJ28	VSS	AV49
AJ32	VSS	E6
AJ34	VSS	AV5
AT5	VSS	AV8
AJ4	VSS	AW14
AK12	VSS	AW18
AM41	VSS	AW2
AN19	VSS	AW2
AK26	VSS	BF9
AK22	VSS	AW32
AK23	VSS	AW36
AK28	VSS	AW40
	VSS	AW52
	VSS	AY11
	VSS	G44
	VSS	AY47

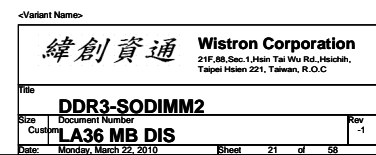
IBEXPEAK-M-GP-NF 71.0HM55.A0U

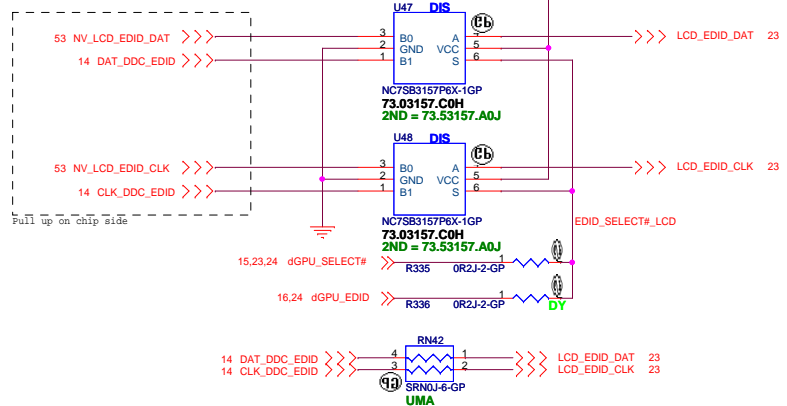
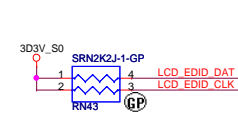
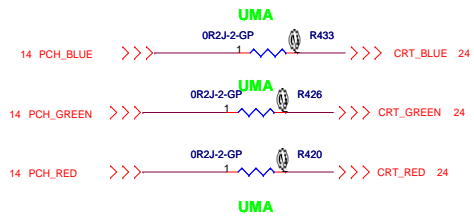
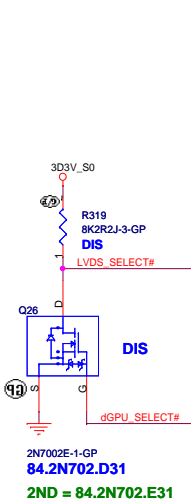
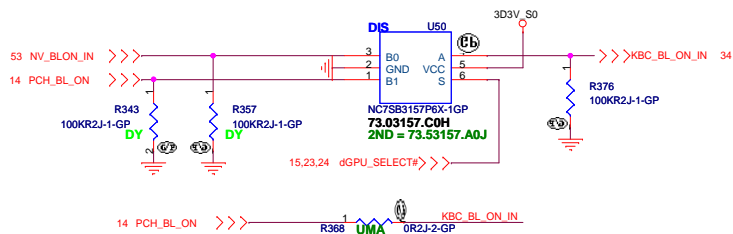
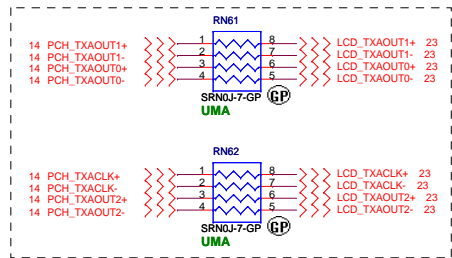
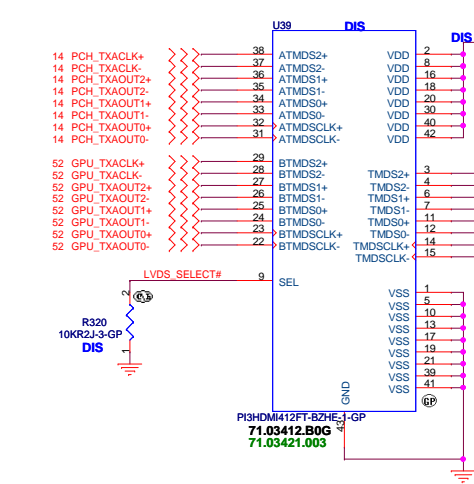
<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C

Title		PCH (9/9)-VSS	
Size	Document Number	LA36 MB DIS	Rev -1
Custom			
Date:	Monday, March 22, 2010	Sheet	19 of 58



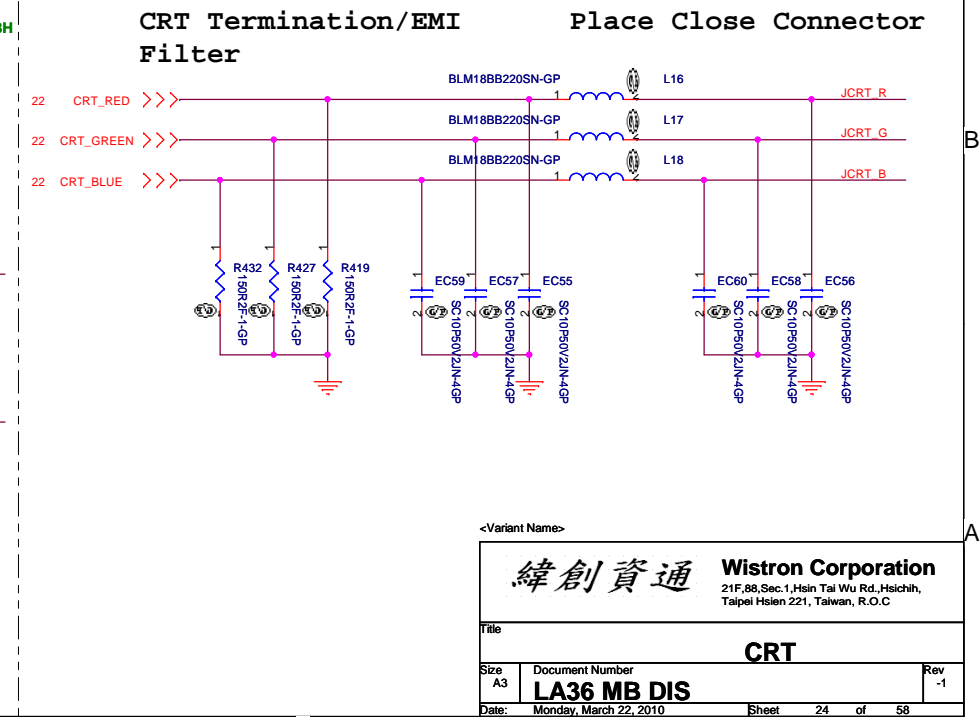
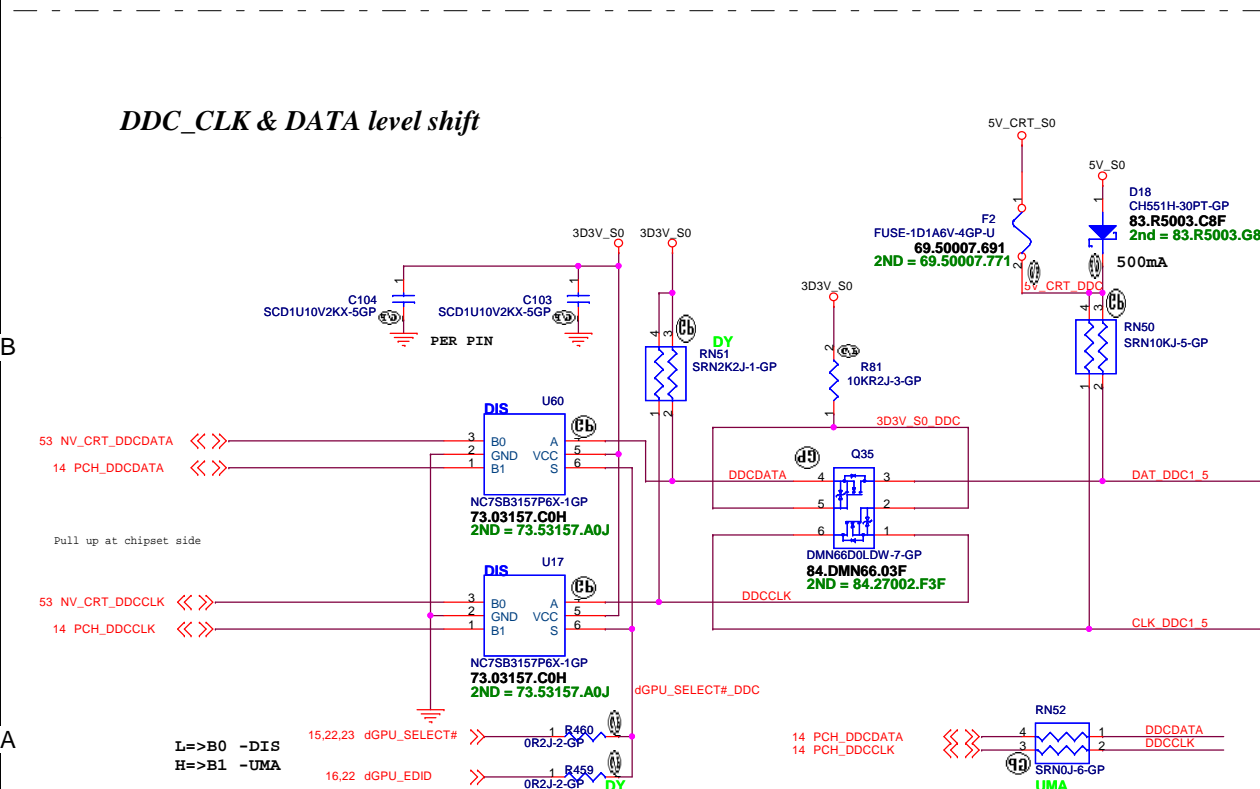
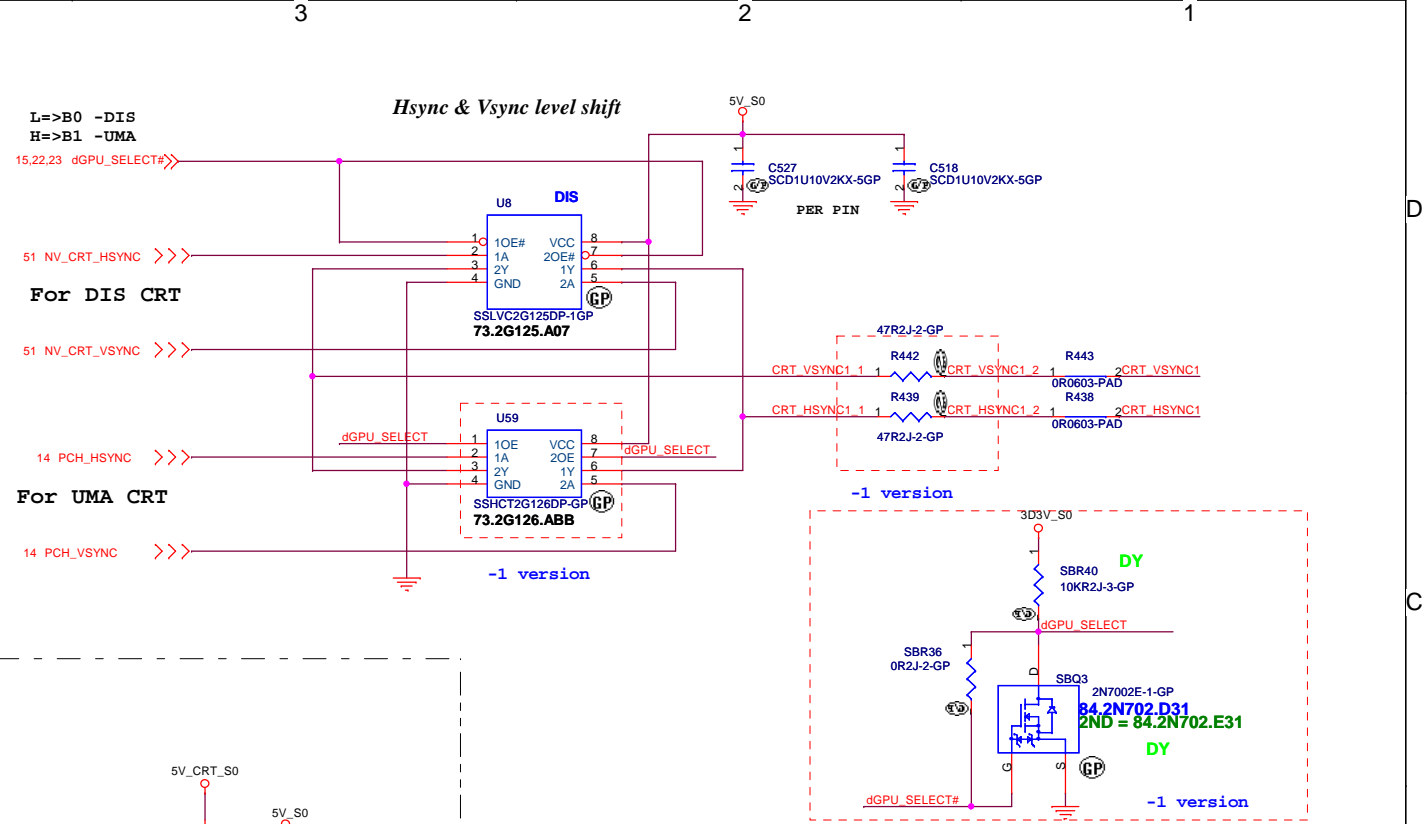
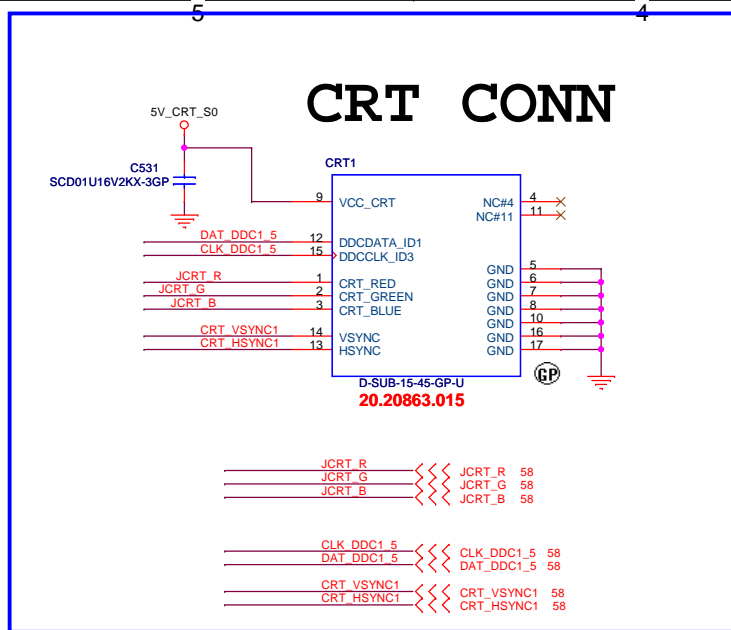


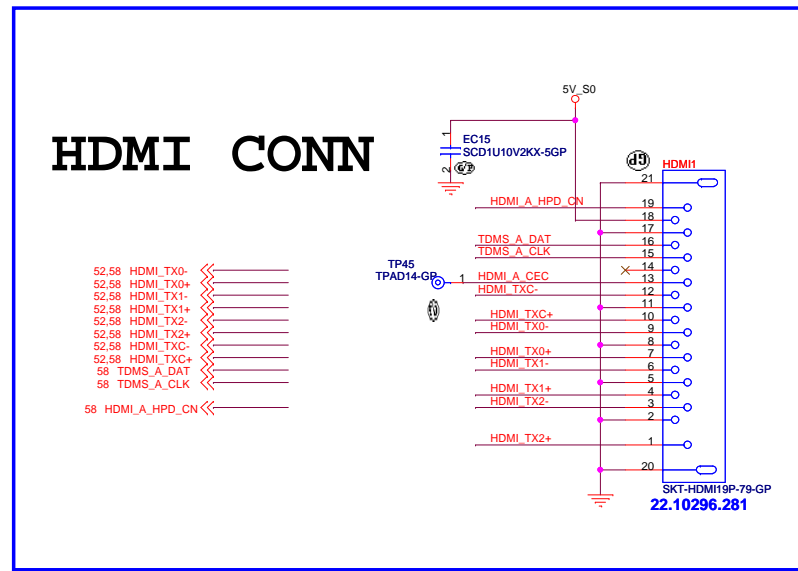
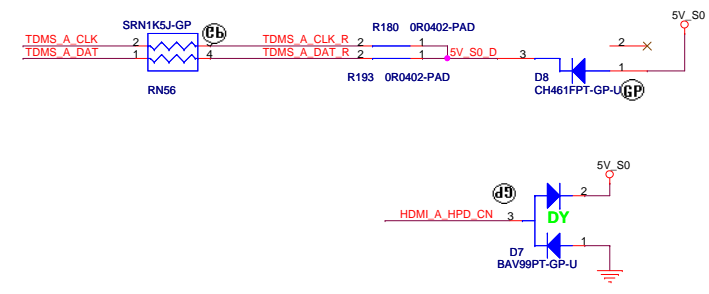
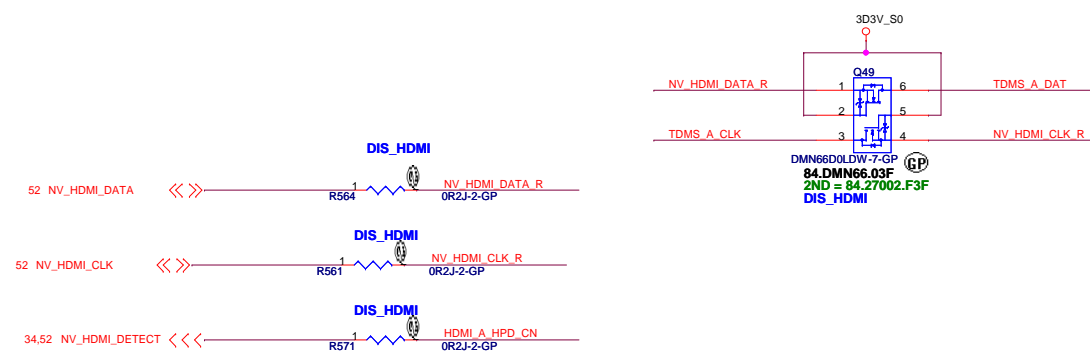
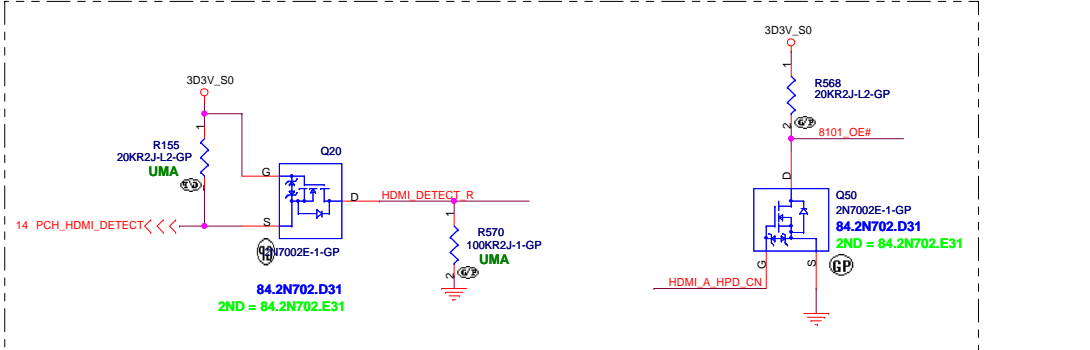
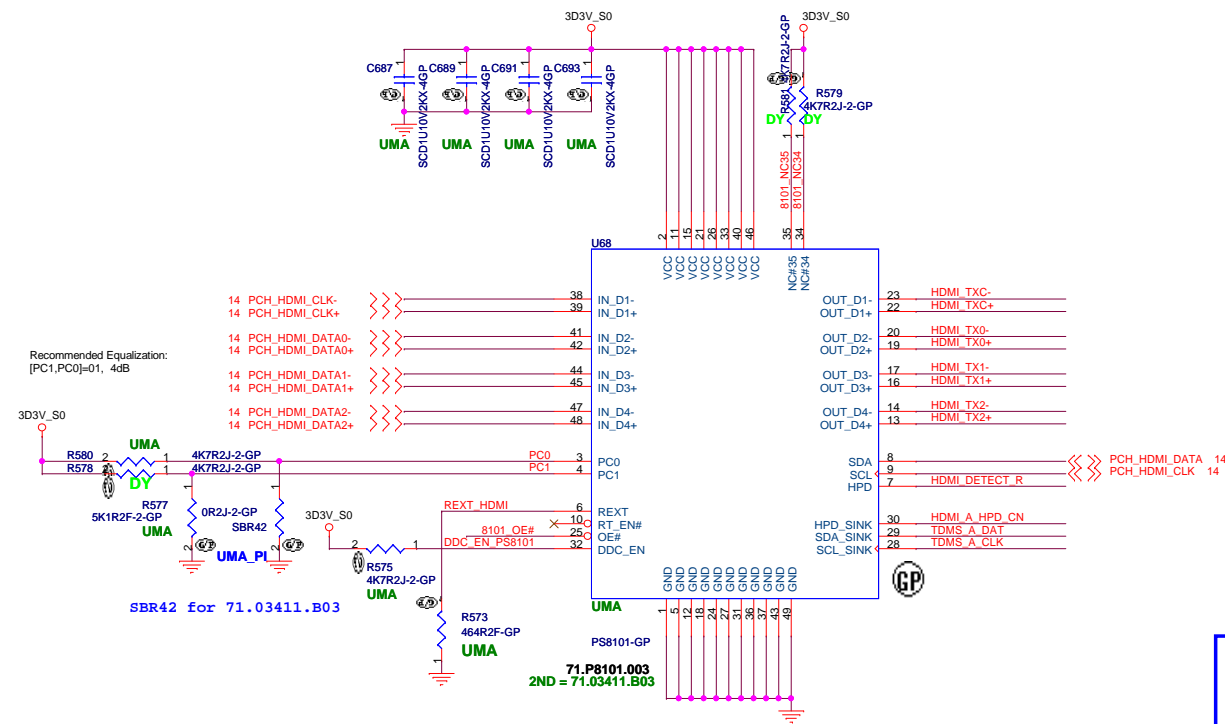


FUNCTION TABLE		
SEL	FUNCTION	OUTPUT
L	TMD�n+ = ATMD�n+ TMD�n- = ATMD�n- TMD�CLK+ = ATMD�CLK+ TMD�CLK- = ATMD�CLK- BTMD�n+ = High Impedance BTMD�n- = High Impedance BTMD�CLK+ = High Impedance BTMD�CLK- = High Impedance	TMD�n+ TMD�n- TMD�CLK+ TMD�CLK-
H	TMD�n+ = BTMD�n+ TMD�n- = BTMD�n- TMD�CLK+ = BTMD�CLK+ TMD�CLK- = BTMD�CLK- ATMD�n+ = High Impedance ATMD�n- = High Impedance ATMD�CLK+ = High Impedance ATMD�CLK- = High Impedance	TMD�n+ TMD�n- TMD�CLK+ TMD�CLK-

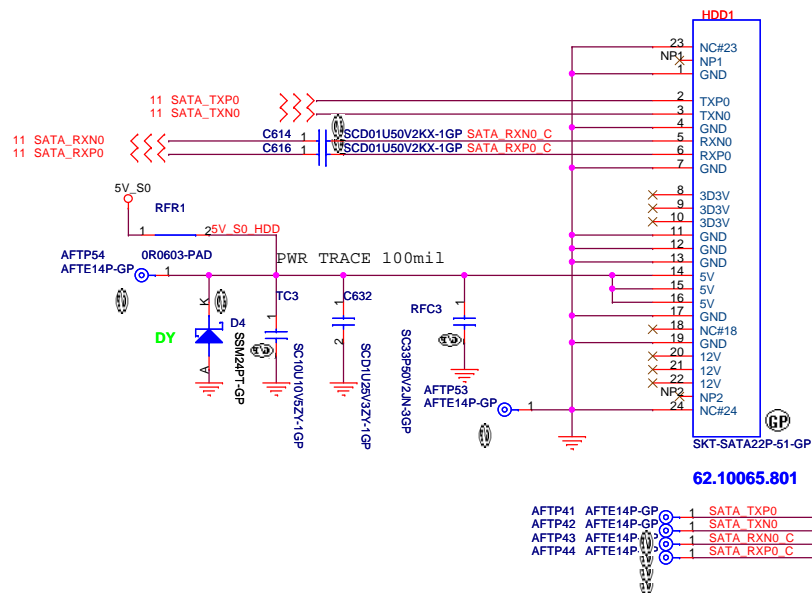
$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1



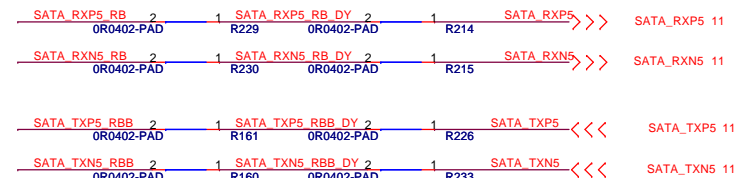
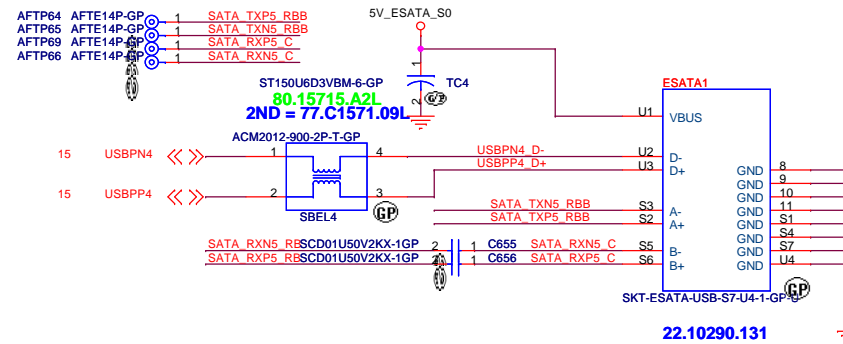




# SATA Connector

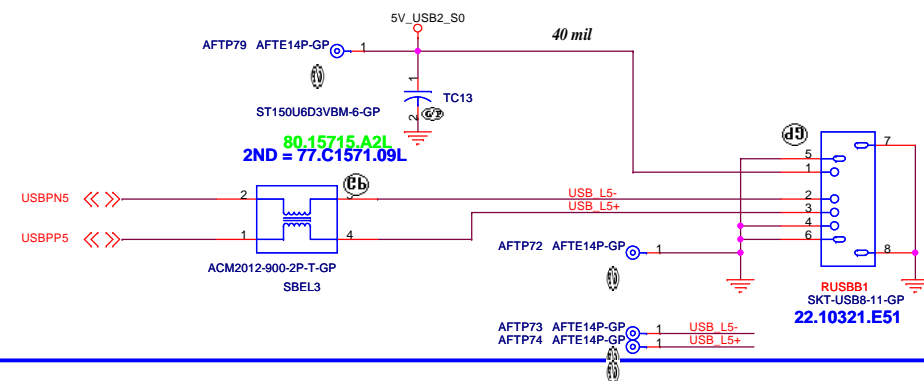


# E-SATA Connector

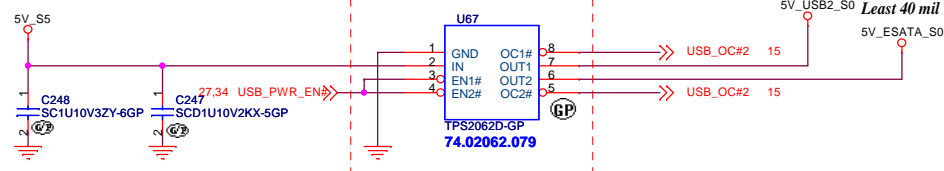


-1 Version

# USB2



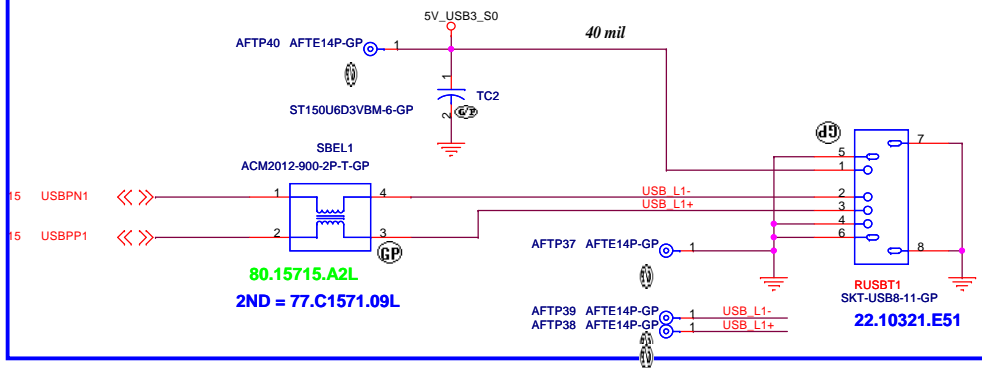
-1 version



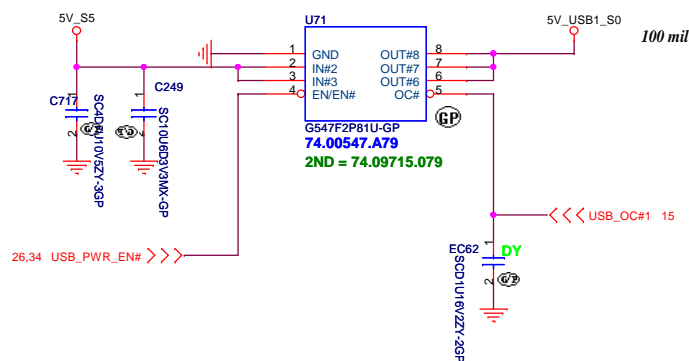
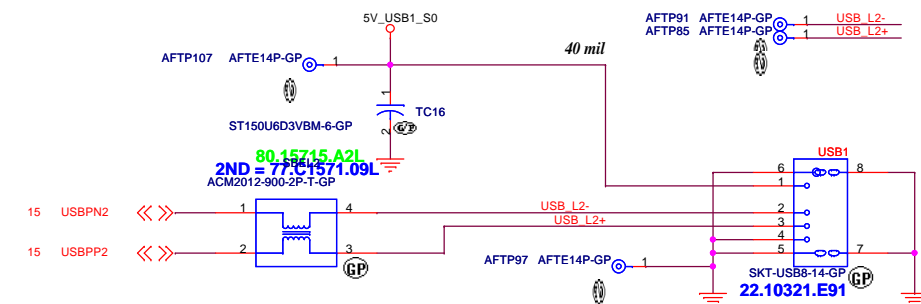
<Variant Name>

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C		
<b>Title</b> HDD & E-SATA&USB2		
<b>Size</b> A3	<b>Document Number</b> LA36 MB DIS	<b>Rev</b> -1
<b>Date:</b> Monday, March 22, 2010 <b>Sheet</b> 26 <b>of</b> 58		

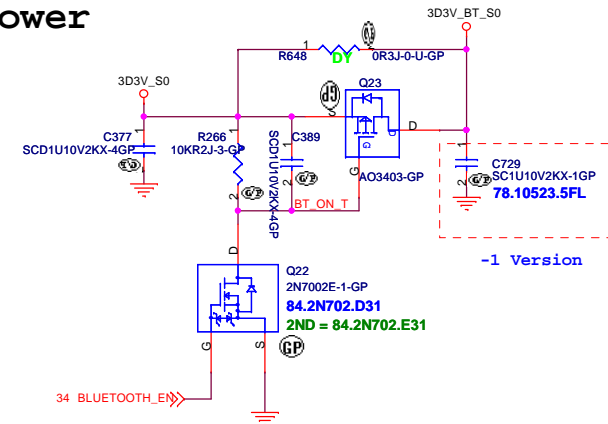
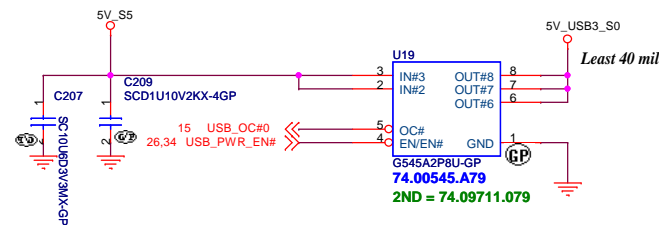
## USB3



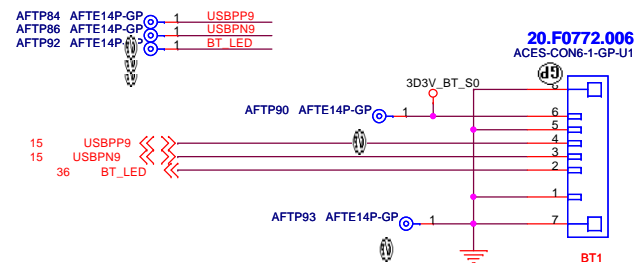
## USB1



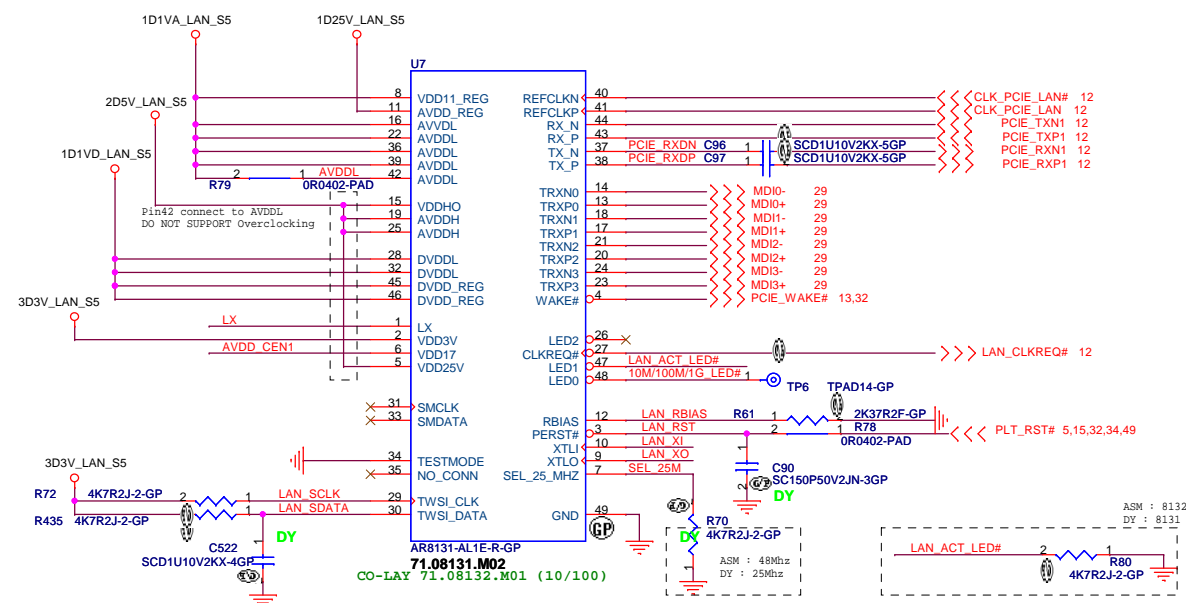
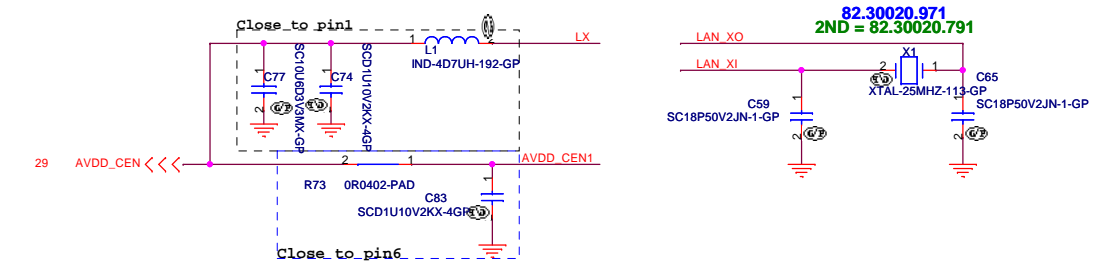
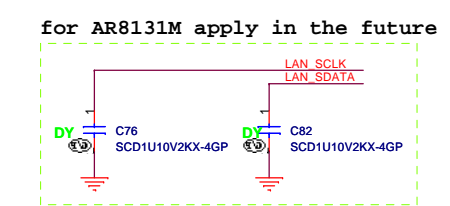
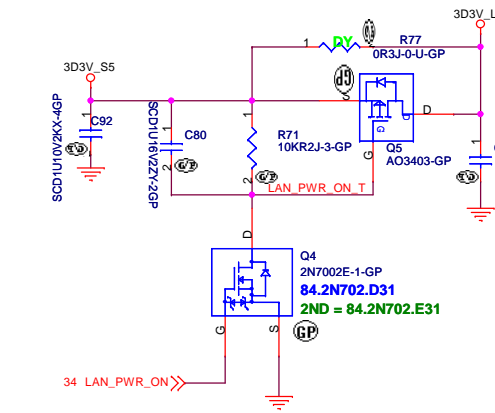
## Bluetooth Power



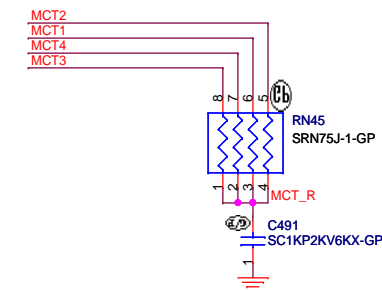
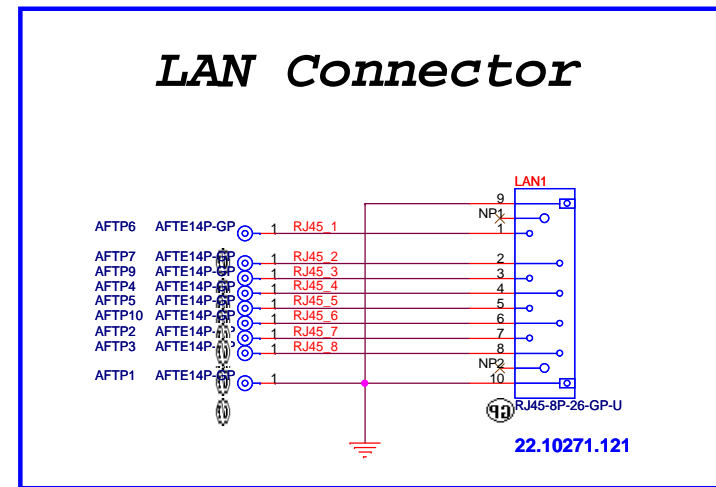
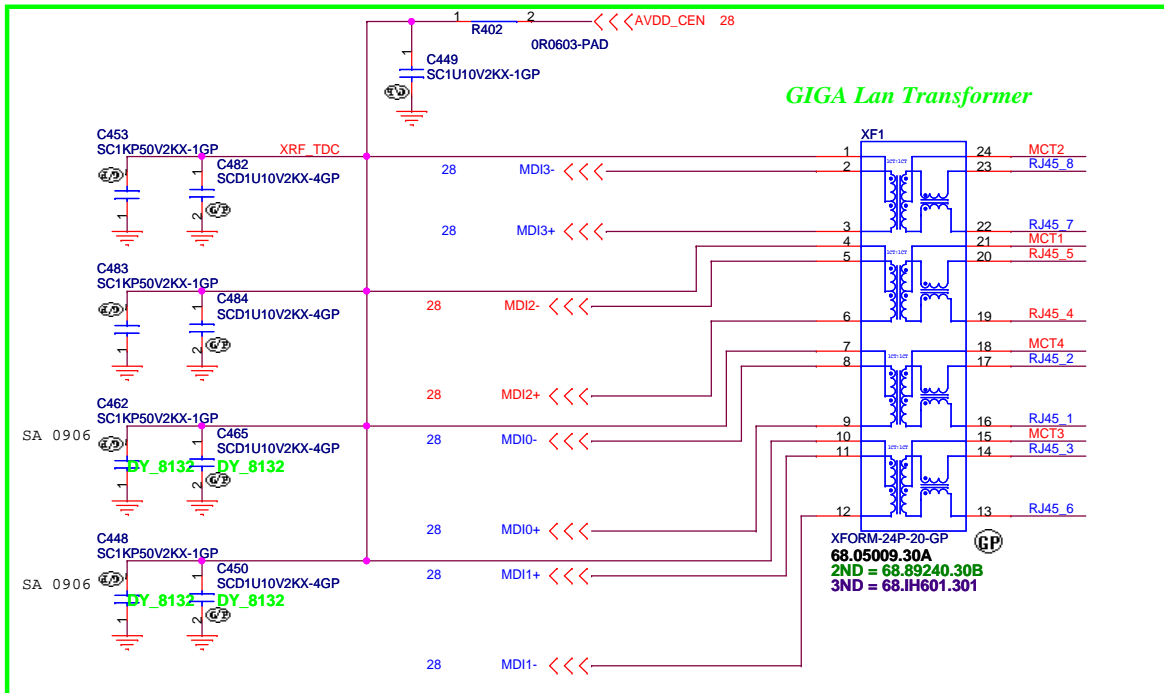
## BT CONN

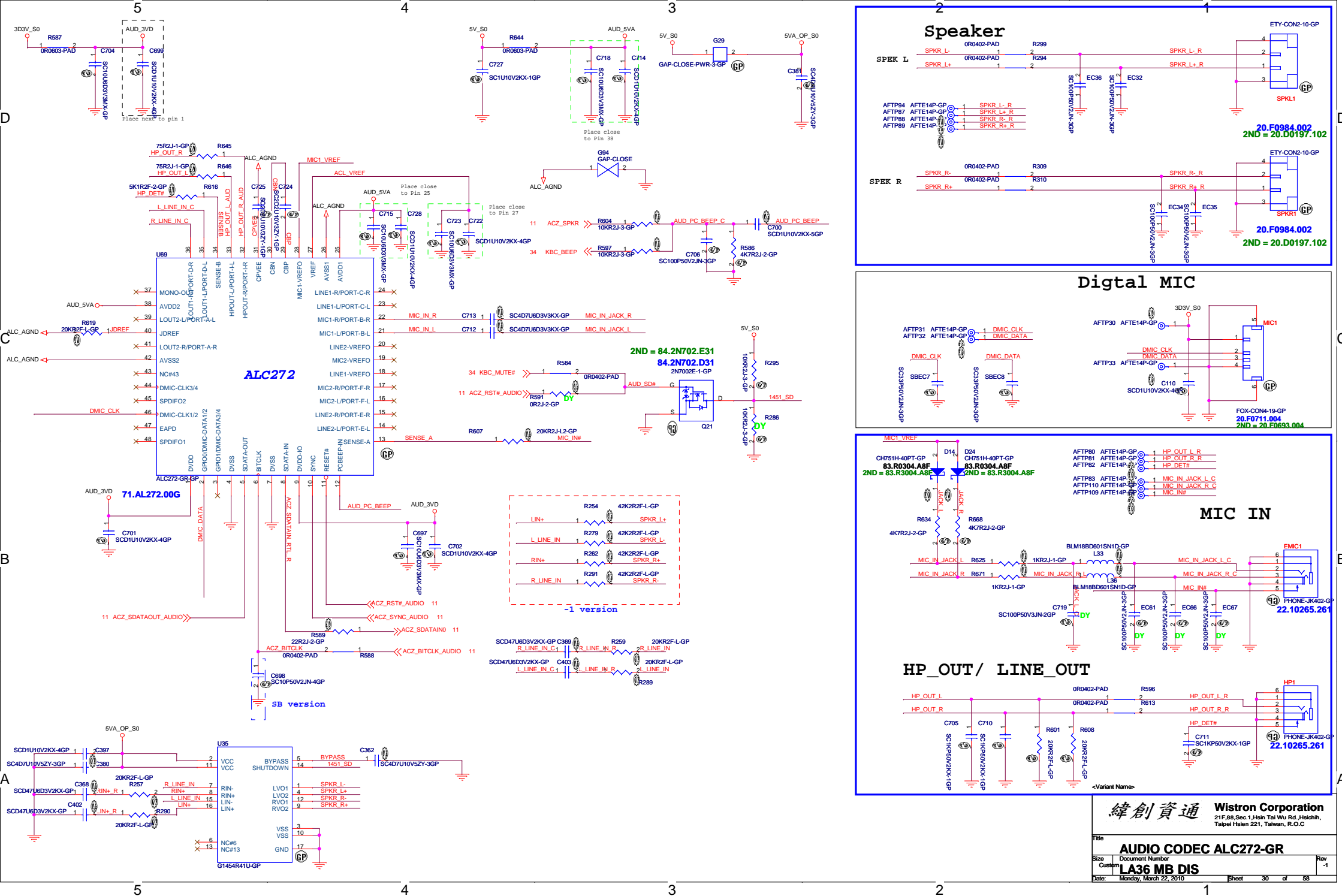


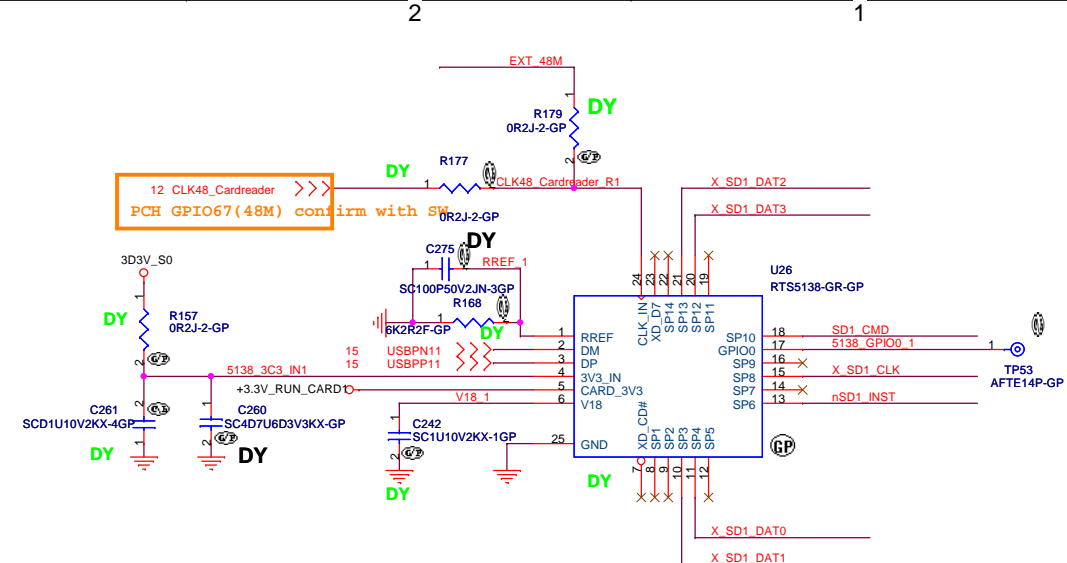
<Variant Name>



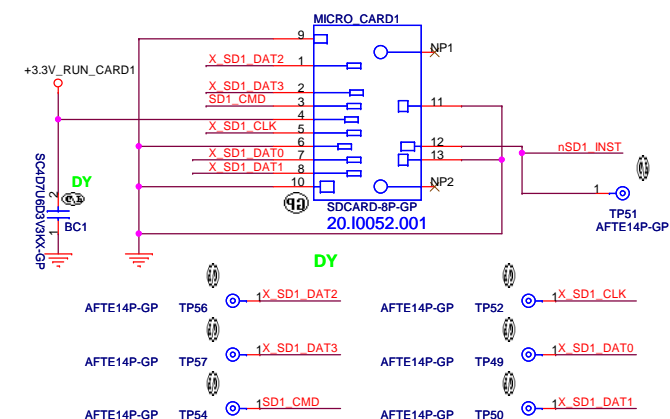
- 1.route on bottom as differential pairs.  
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.  
3.No vias, No 90 degree bends.  
4.pairs must be equal lengths.  
5.6mil trace width, 12mil separation.  
6.36mil between pairs and any other trace.  
7.Must not cross ground moat,except RJ-45 moat.





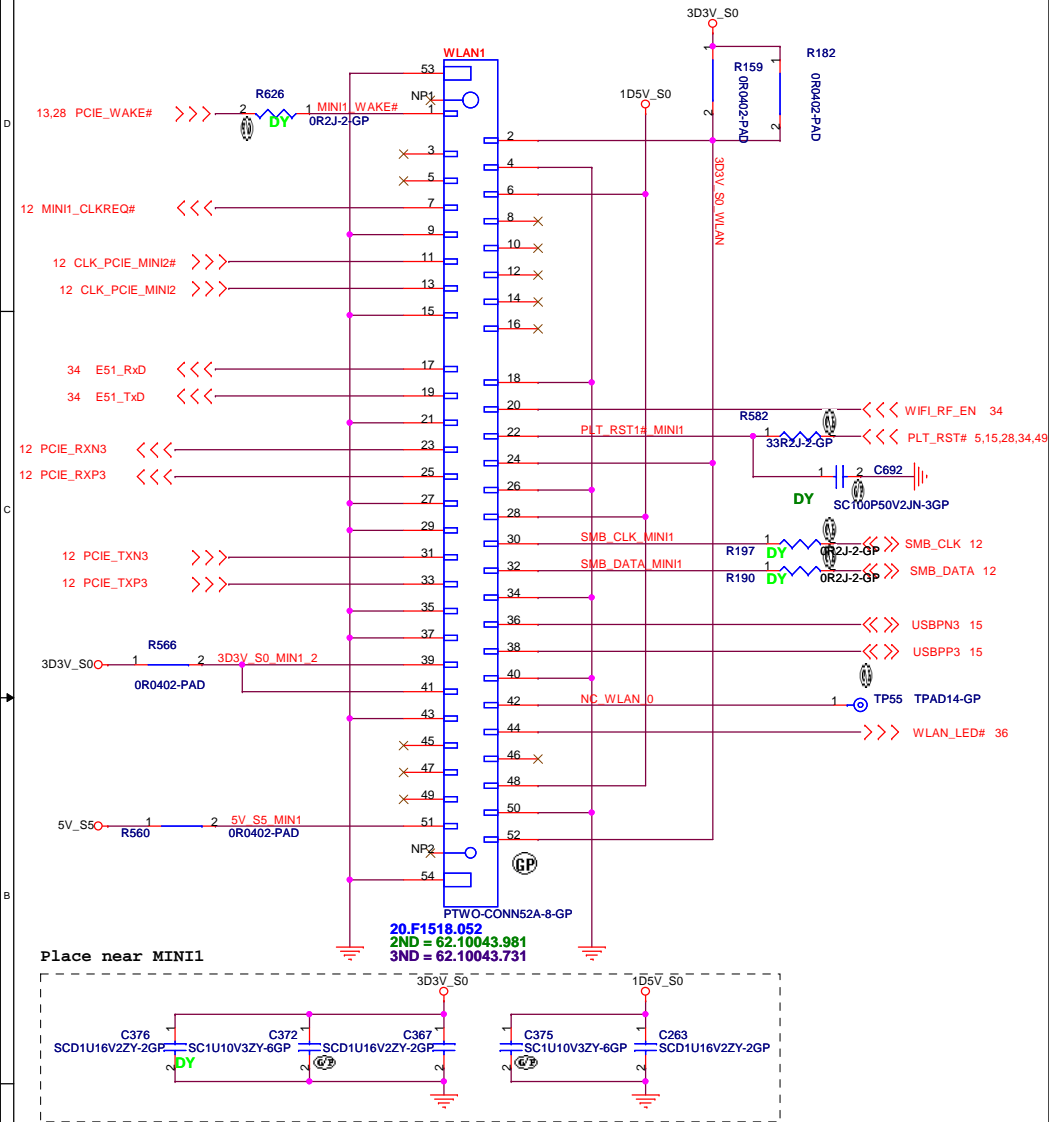


## 4 IN 1 CONN

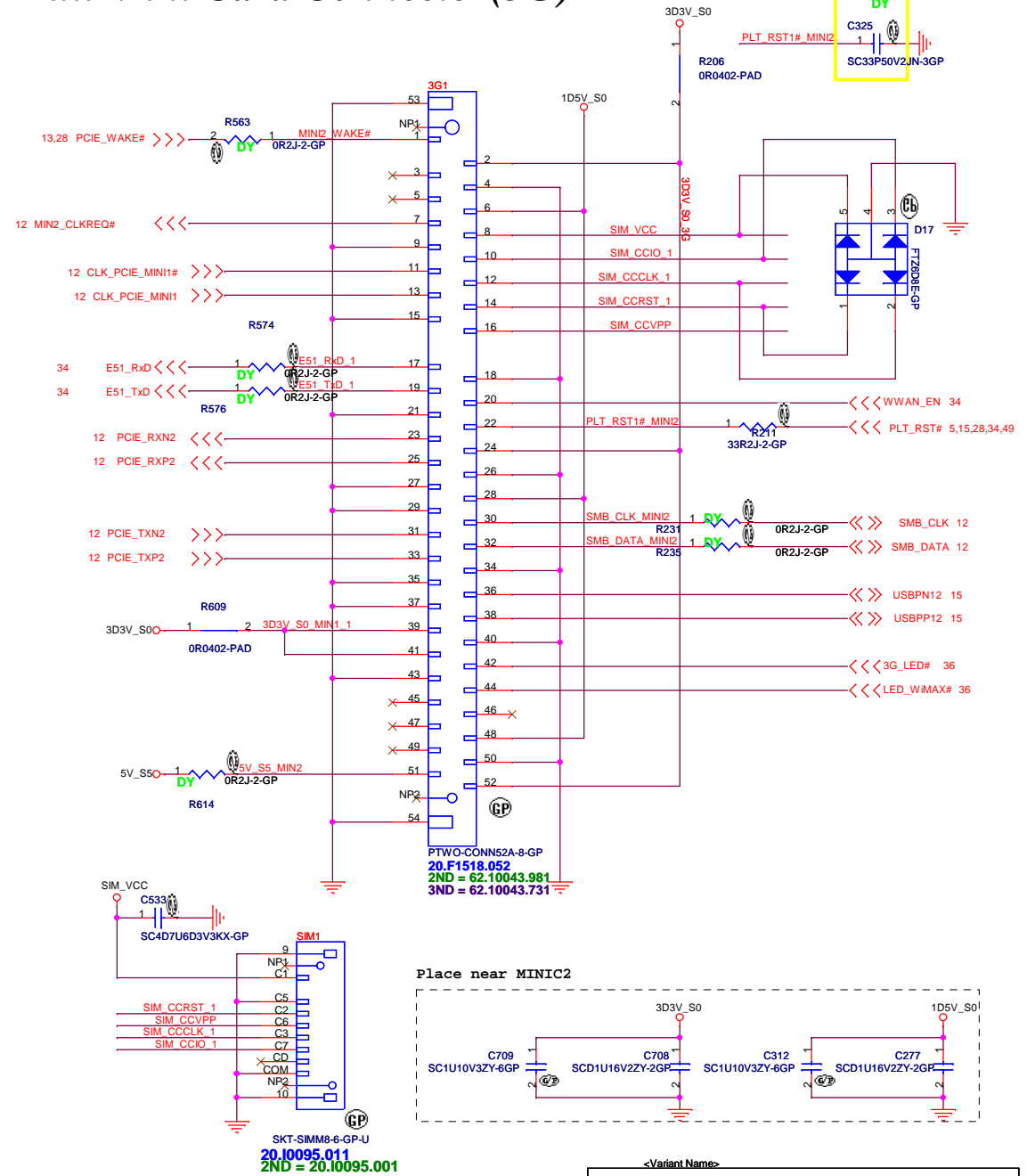


Title			
<b>Cardreader RTS5138</b>			
Size A3	Document Number <b>LA36 MB DIS</b>	Rev -1	
Date:	Monday, March 22, 2010	Sheet	31 of 58

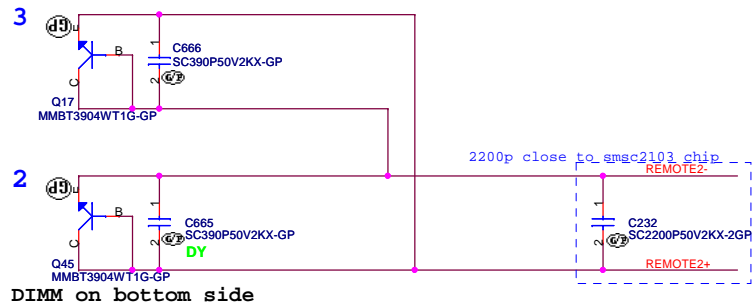
# Half Mini Card Connector(WLAN)



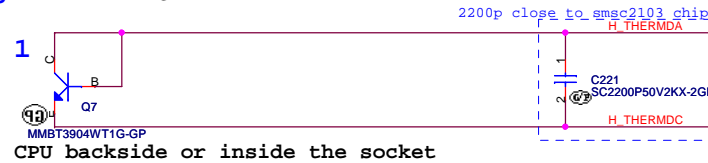
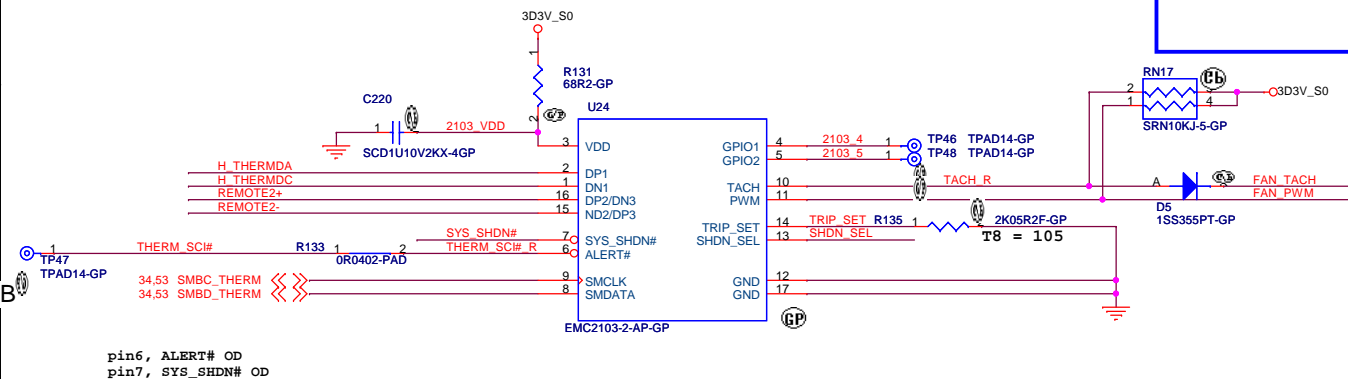
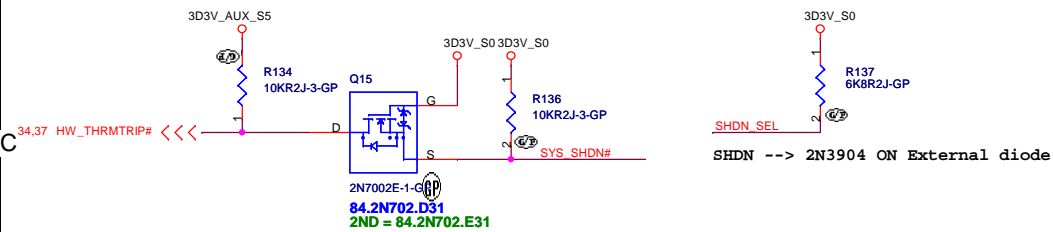
# Full Mini Card Connector(3G)



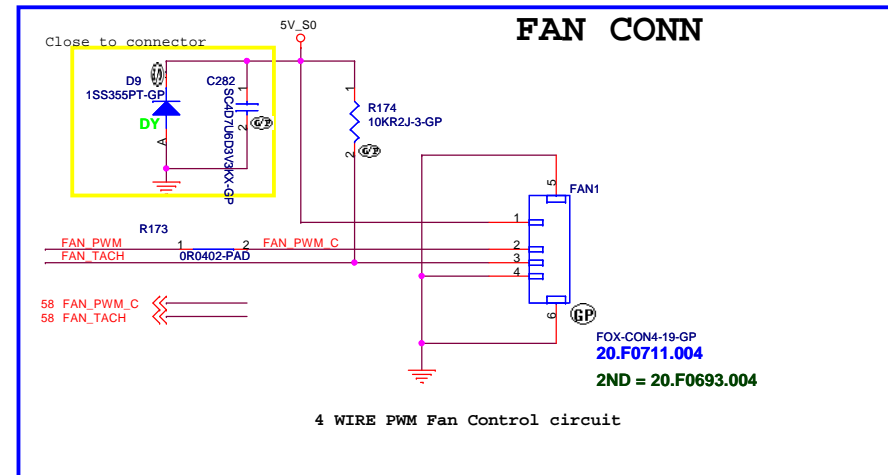
Close to PCH on top side.



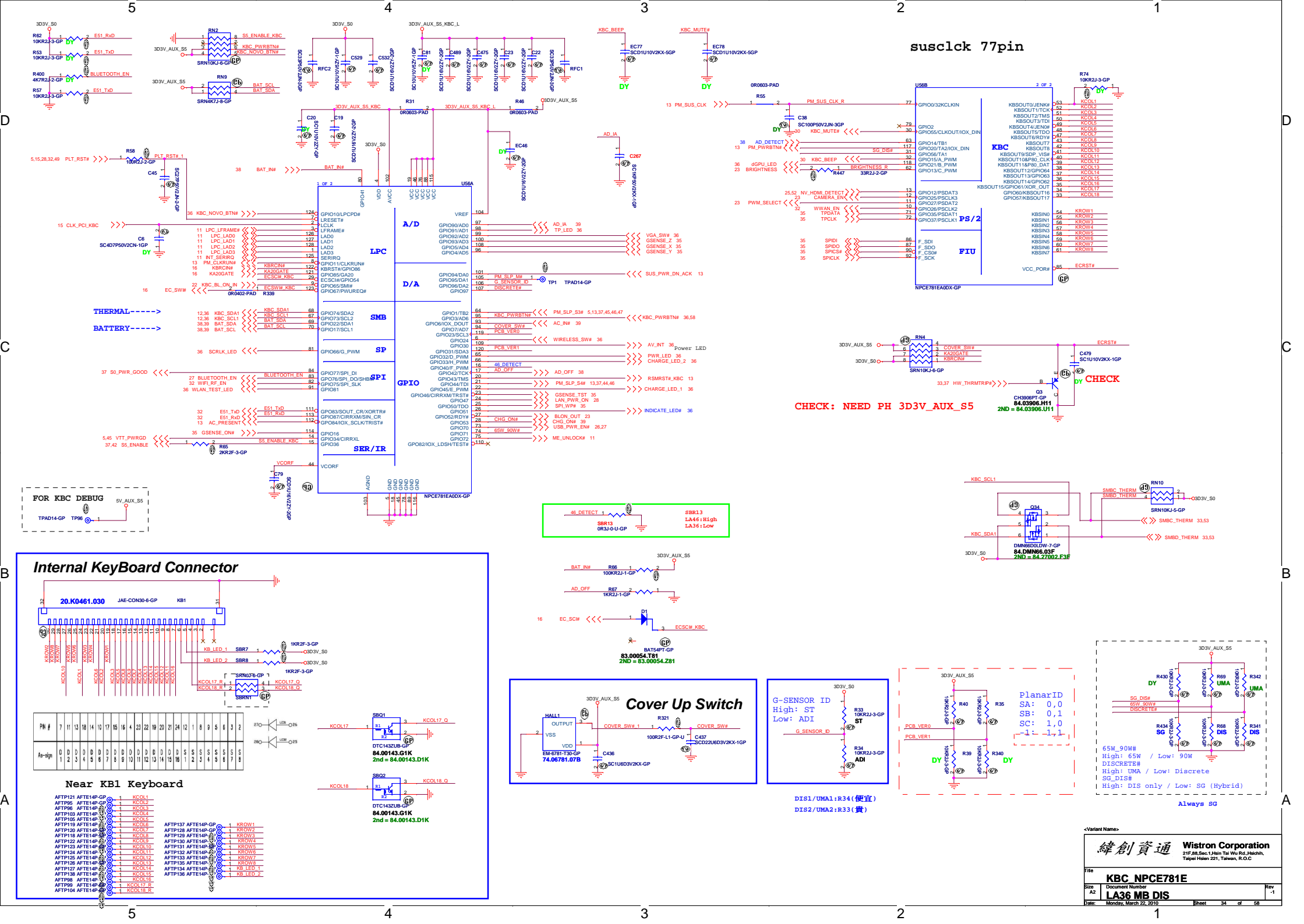
DIMM on bottom side



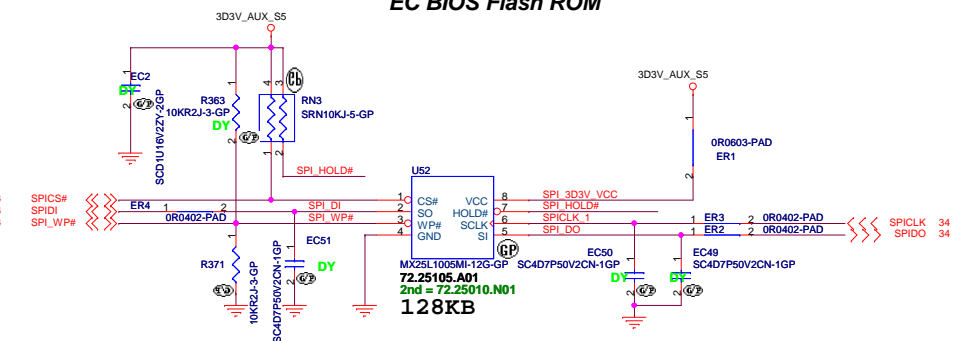
CPU TEMP:  
H\_THERMDA and H\_THERMDC routing 10mil trace width  
and spacing. Locate Capacity near Thermal diode.



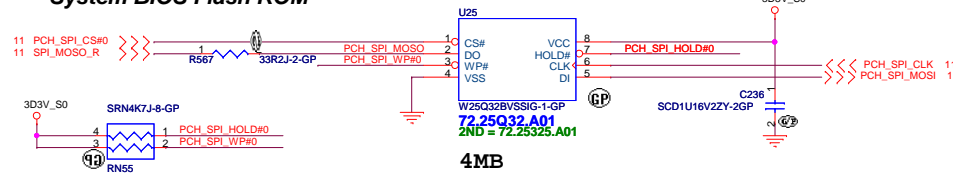
<Variant Name>



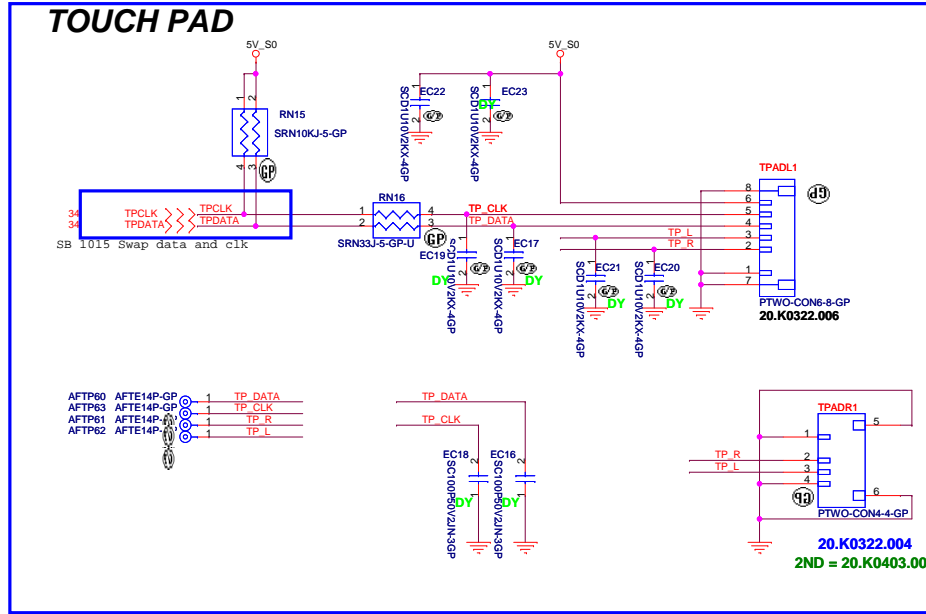
## EC BIOS Flash ROM



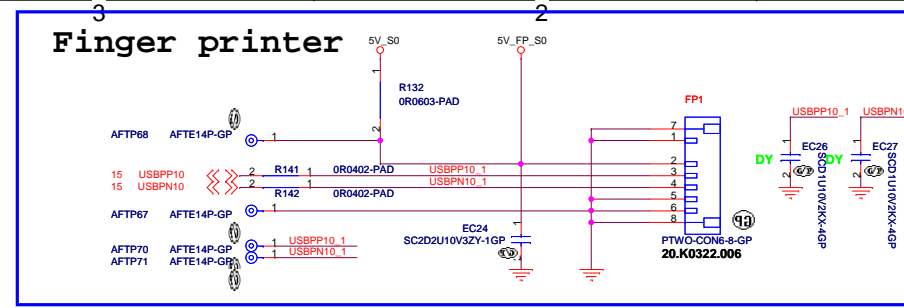
## System BIOS Flash ROM



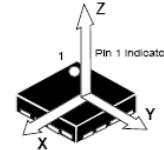
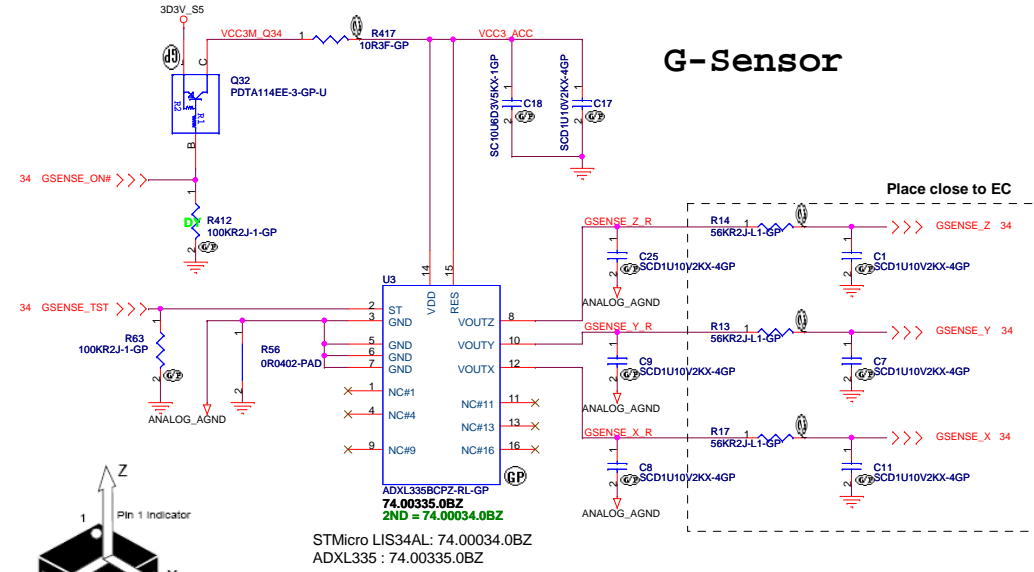
## TOUCH PAD



## Finger printer



## G-Sensor

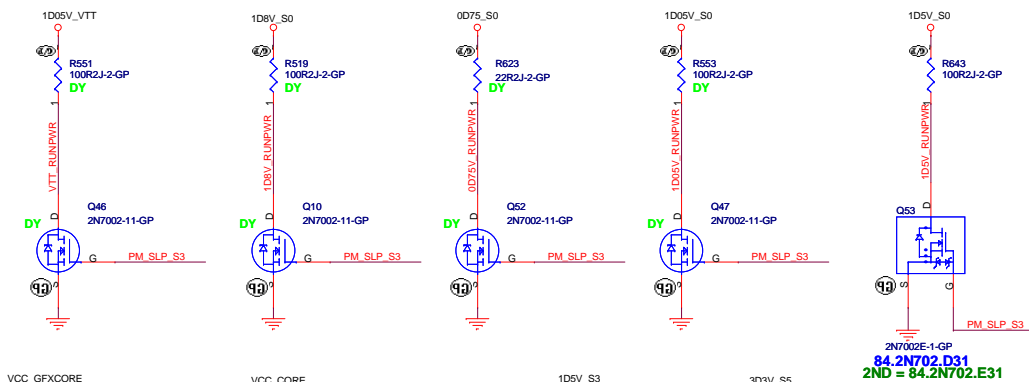
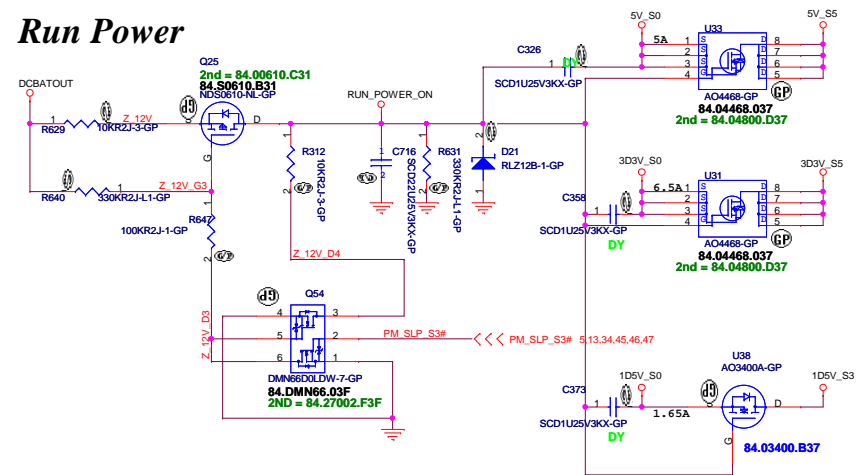
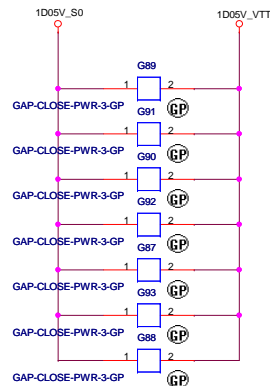
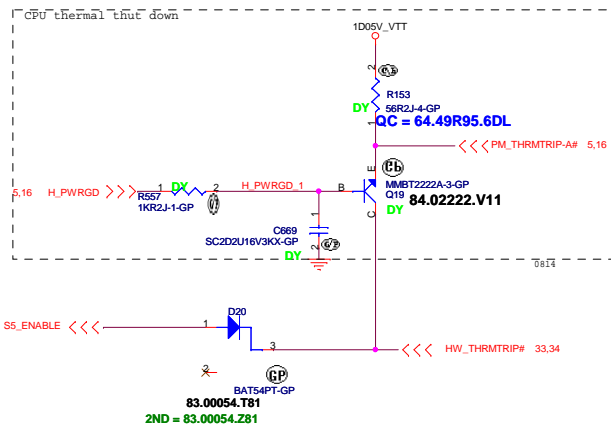


<Variant Name>

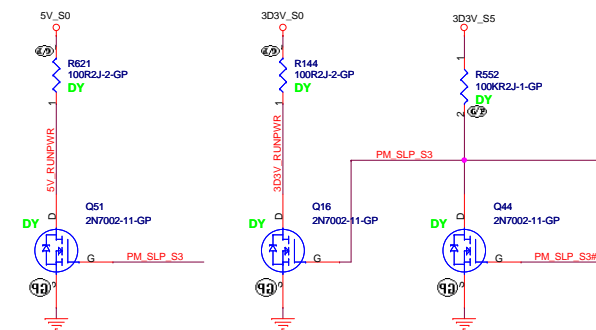
緯創資通 Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taiwan 300, Taiwan, R.O.C.

Title BIOS & TP & G-Sensor & FP  
Size Customer Document Number LA36 MB DIS  
Date: Monday, March 22, 2010 Sheet 35 of 58

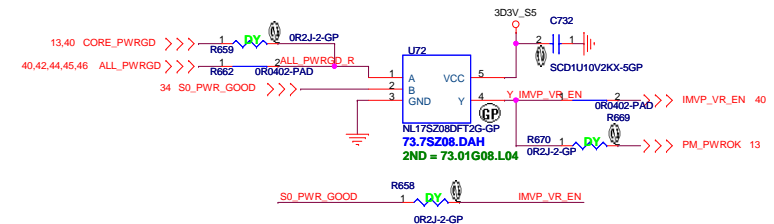
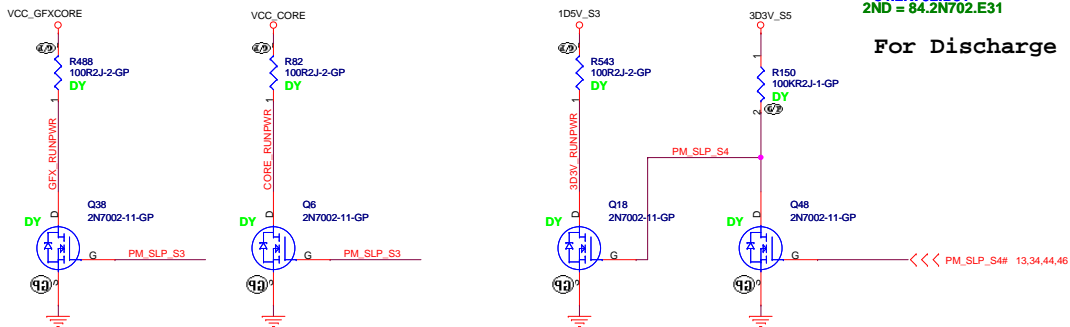


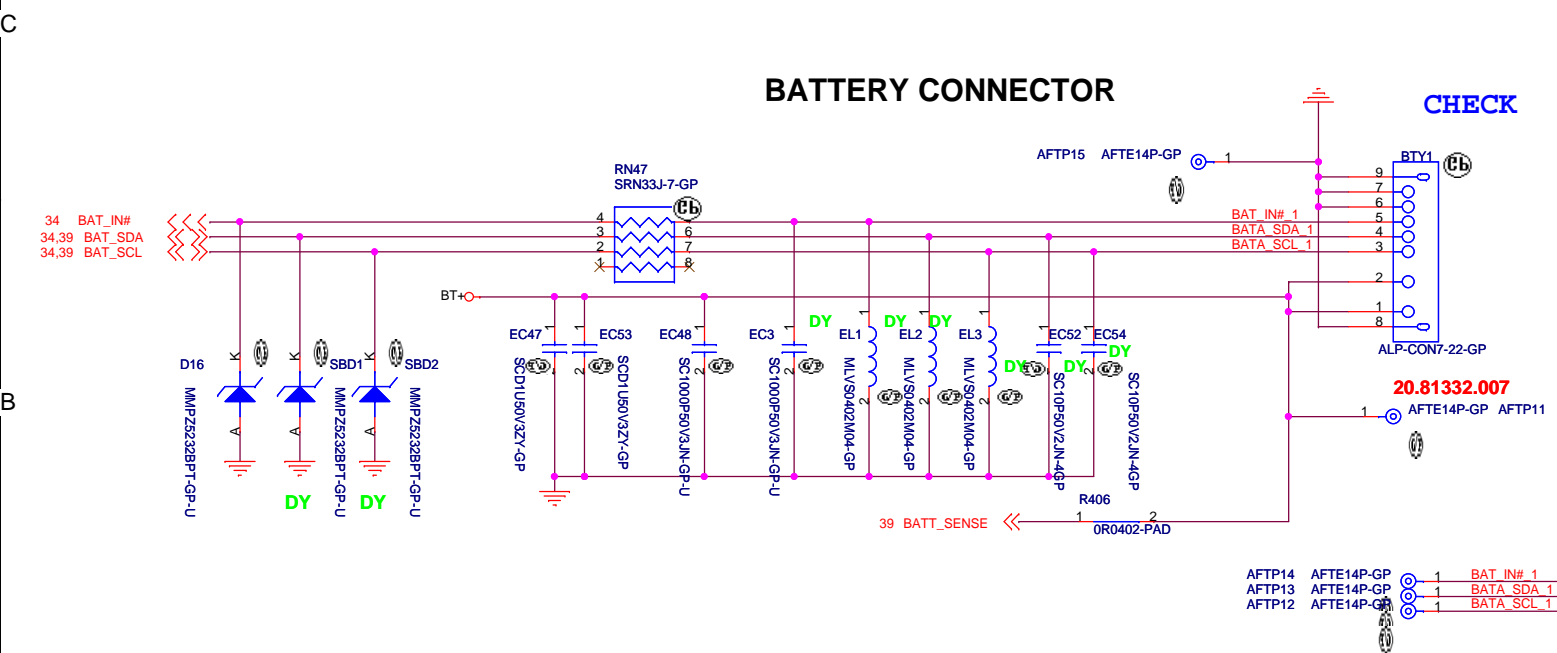
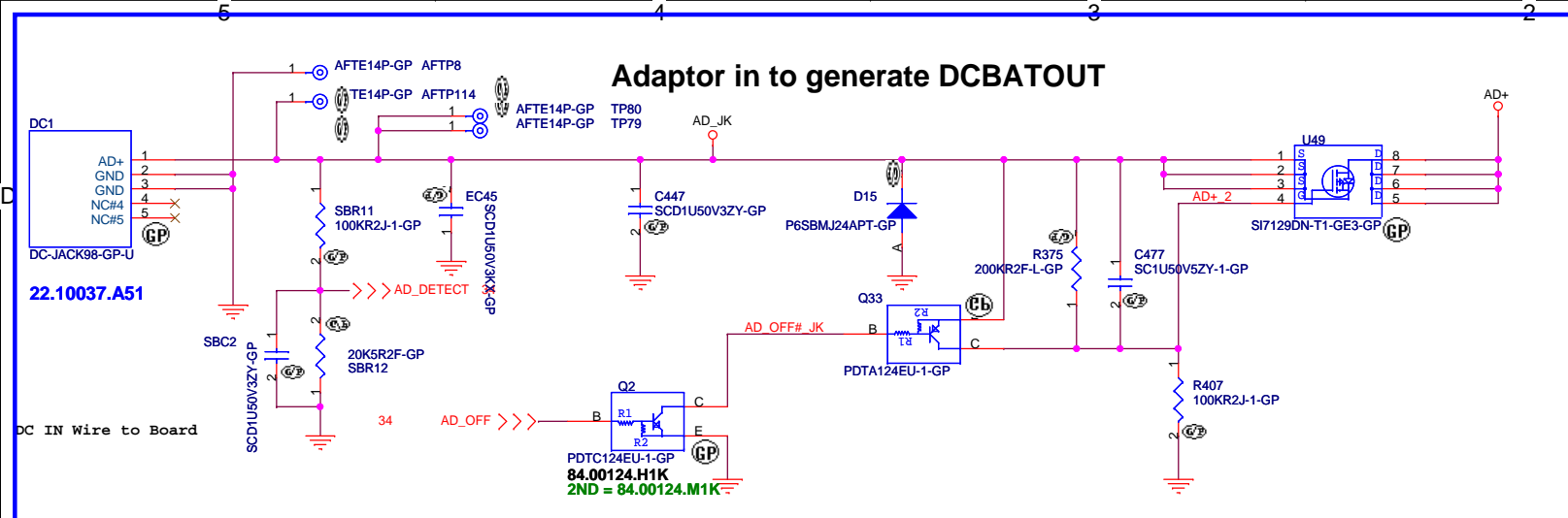


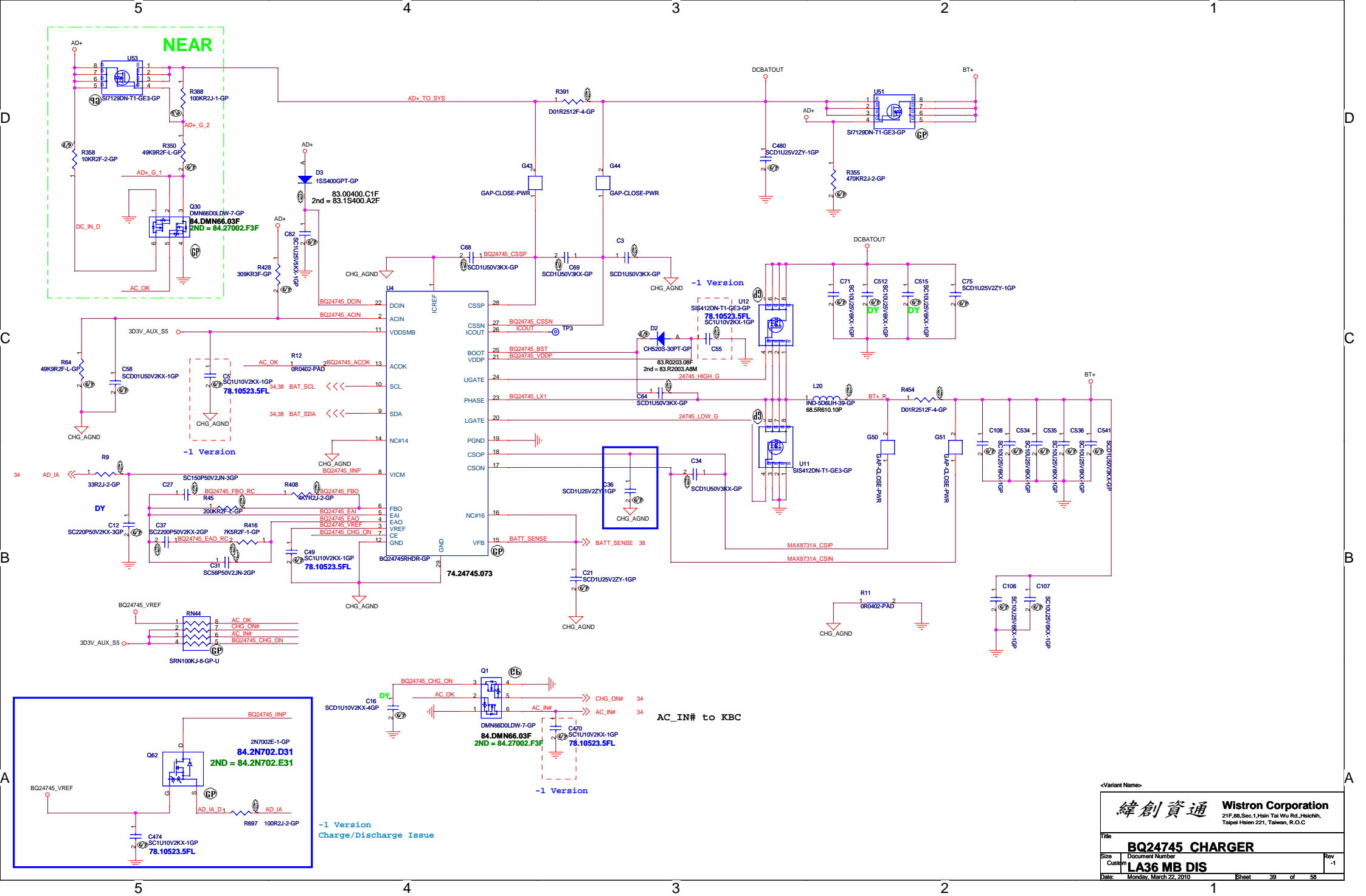
For Discharge

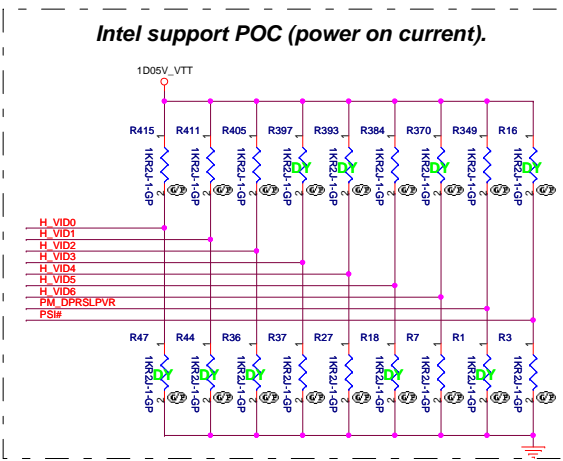
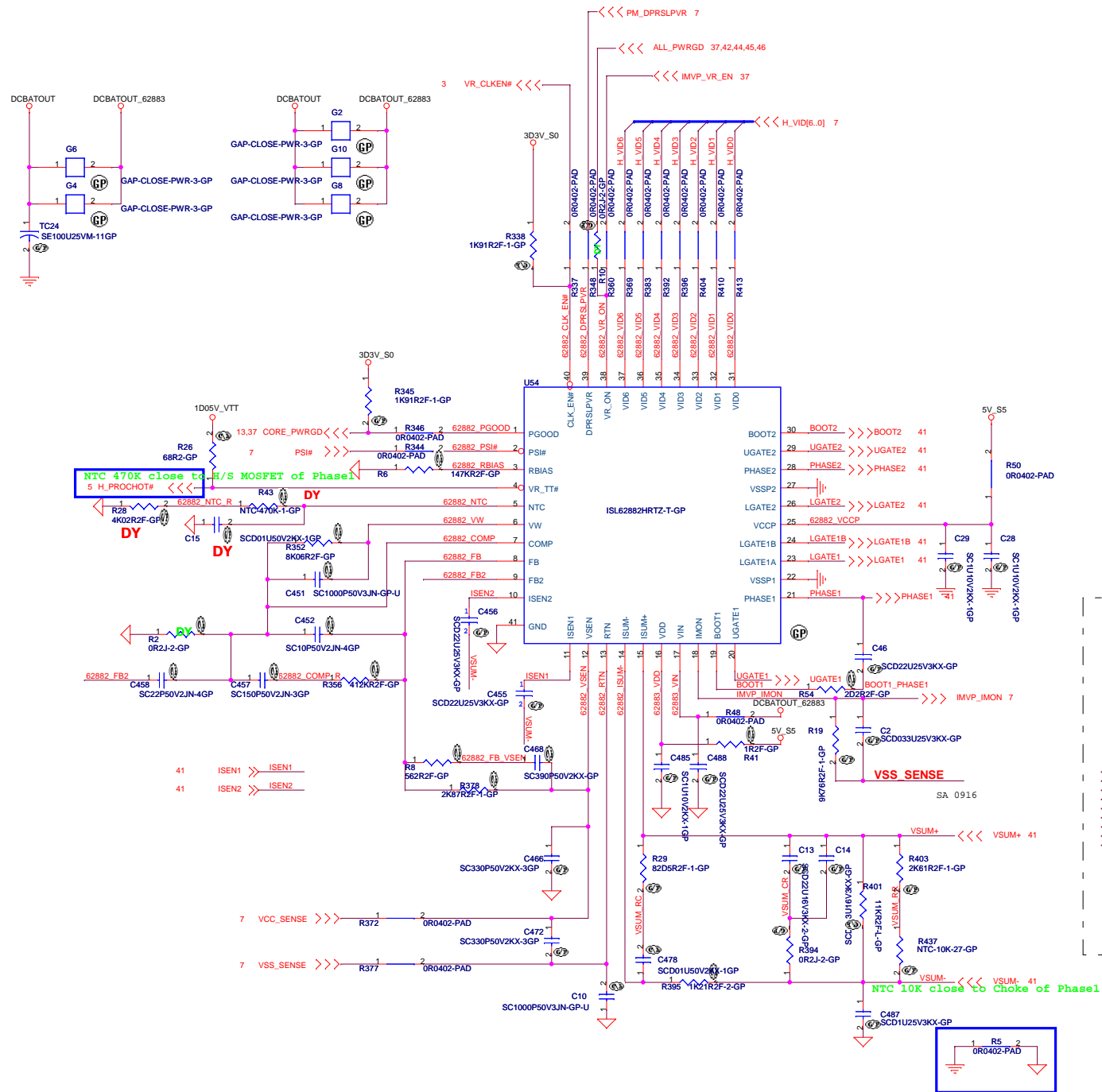


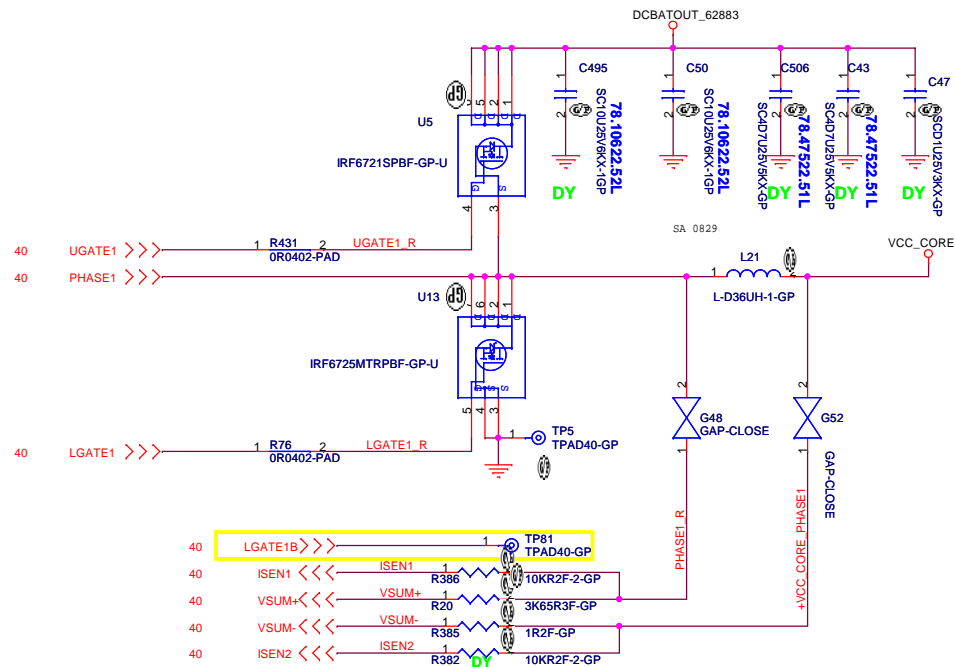
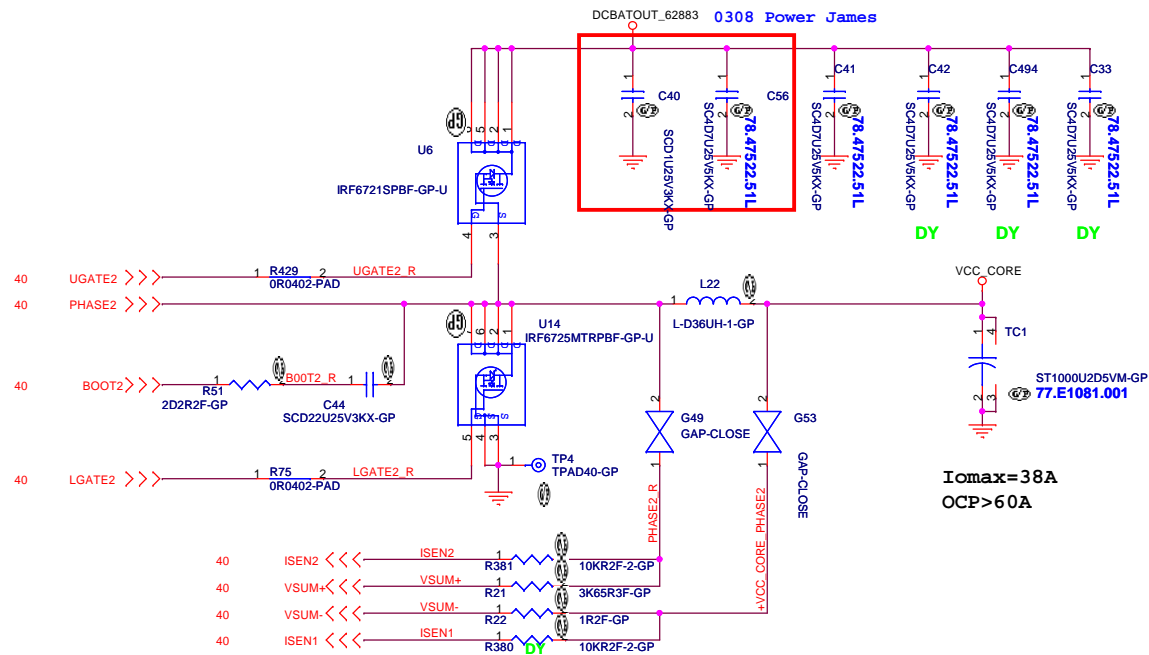
For Discharge





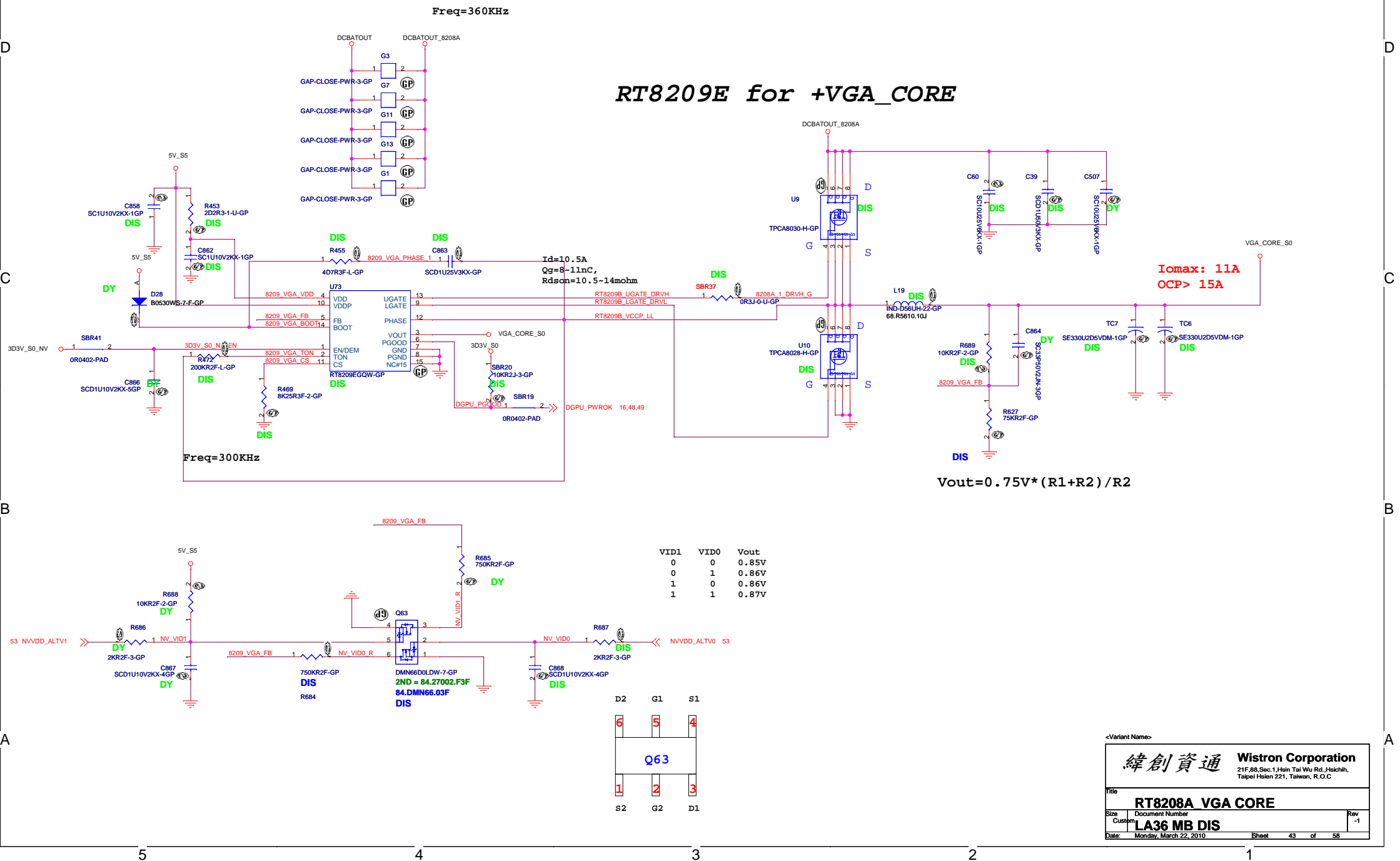




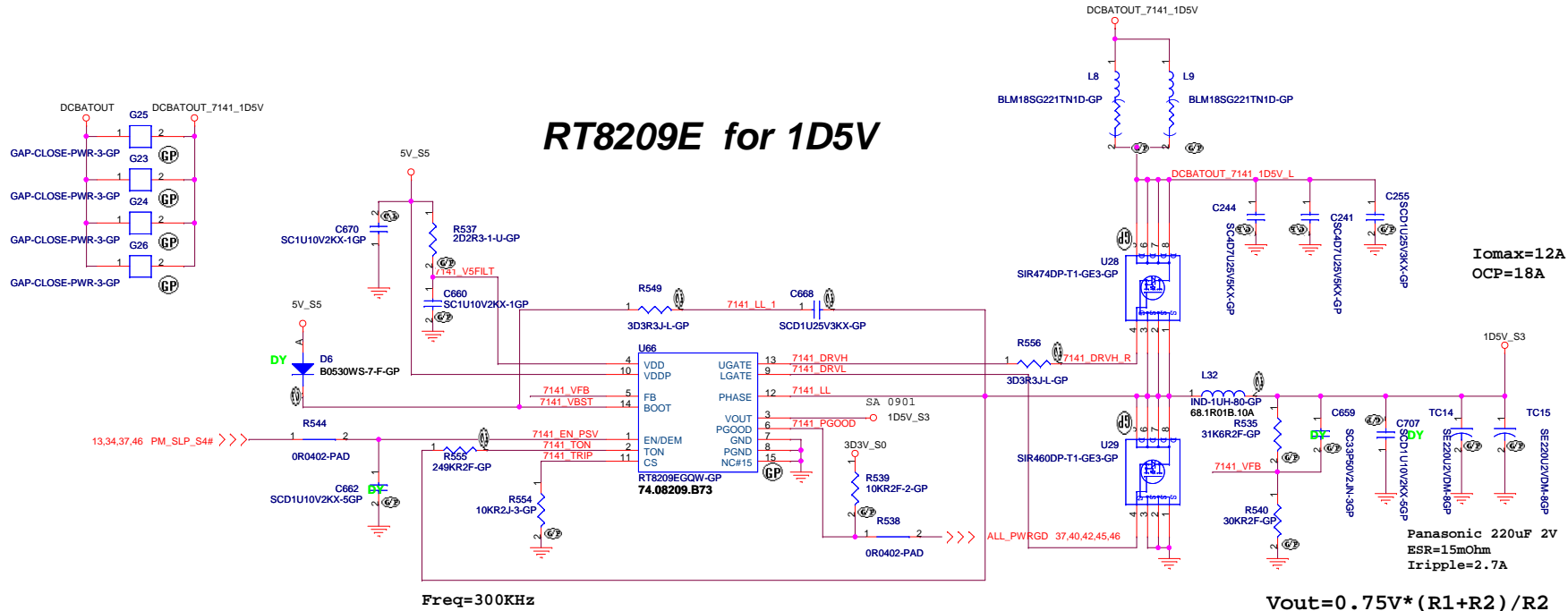


<Variant Name>

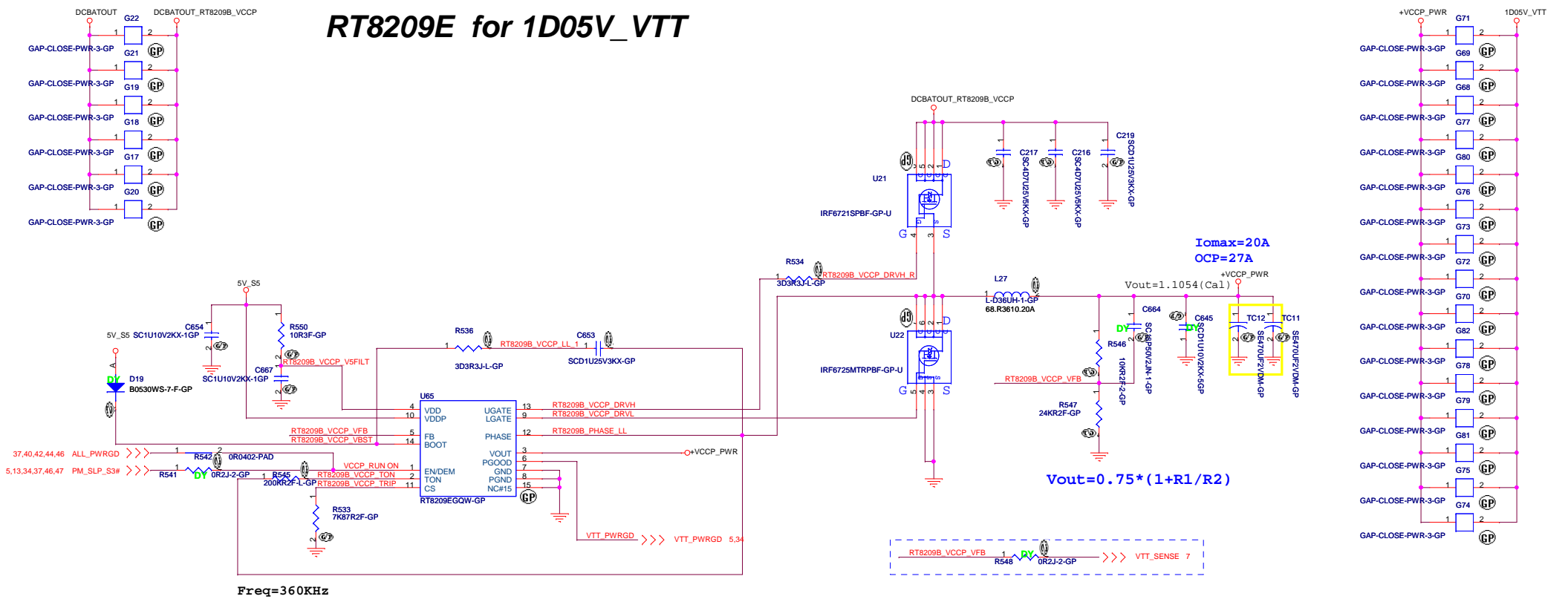


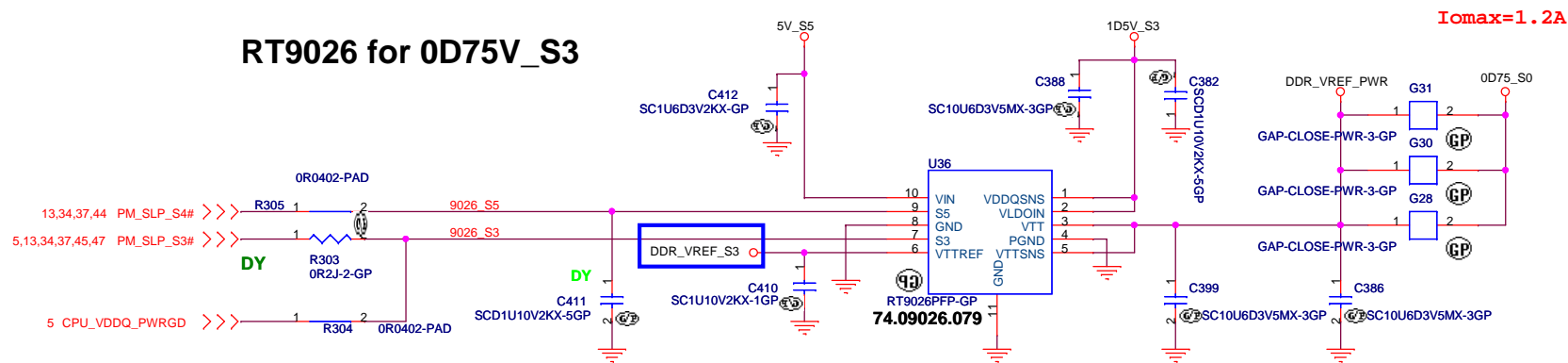
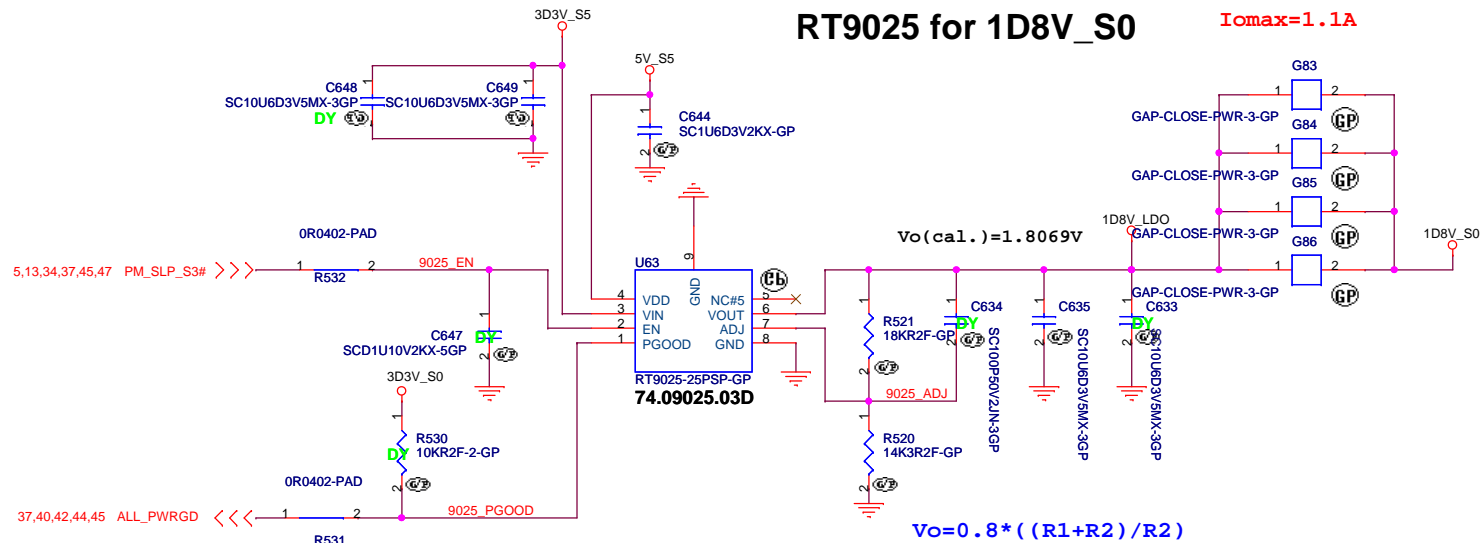


# RT8209E for 1D5V



RT8209E for 1D05V\_VTT





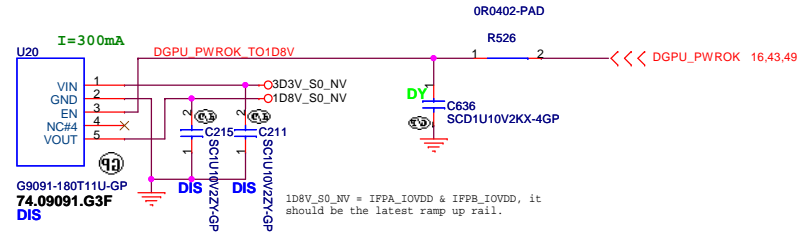
<Variant Name>

**緯創資通** **Wistron Corporation**  
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C

Title		
<b>RT9025 1D8V/ RT9026 0D75</b>		
Size	Document Number	Rev
Custom	<b>LA36 MB DIS</b>	-1
Date:	Monday, March 22, 2010	Sheet 46 of 58

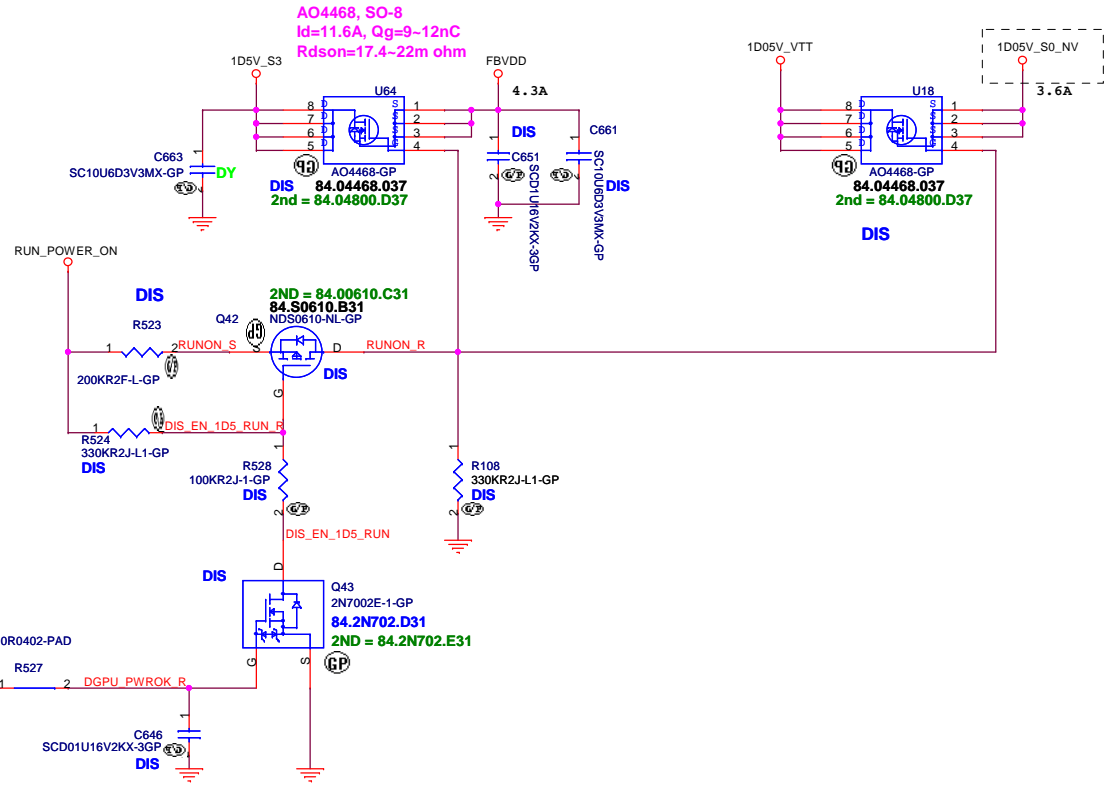


## +3VS to 1.8V Transfer



## +1.5V to FBVDD Transfer

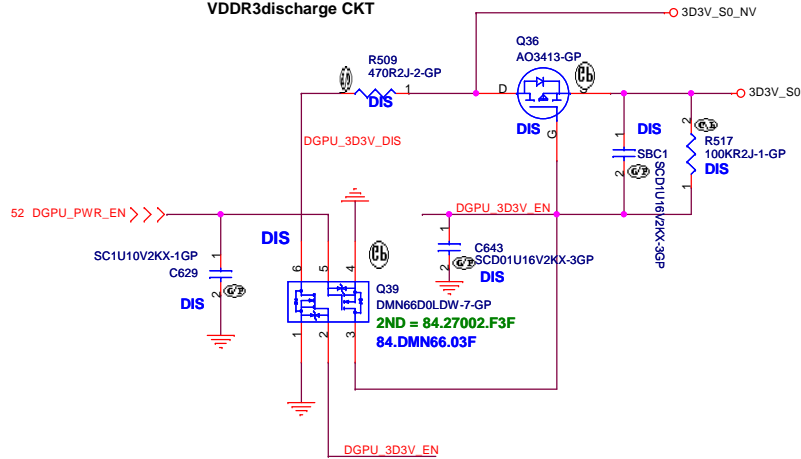
## +1.05V to +1.05V\_NV Transfer



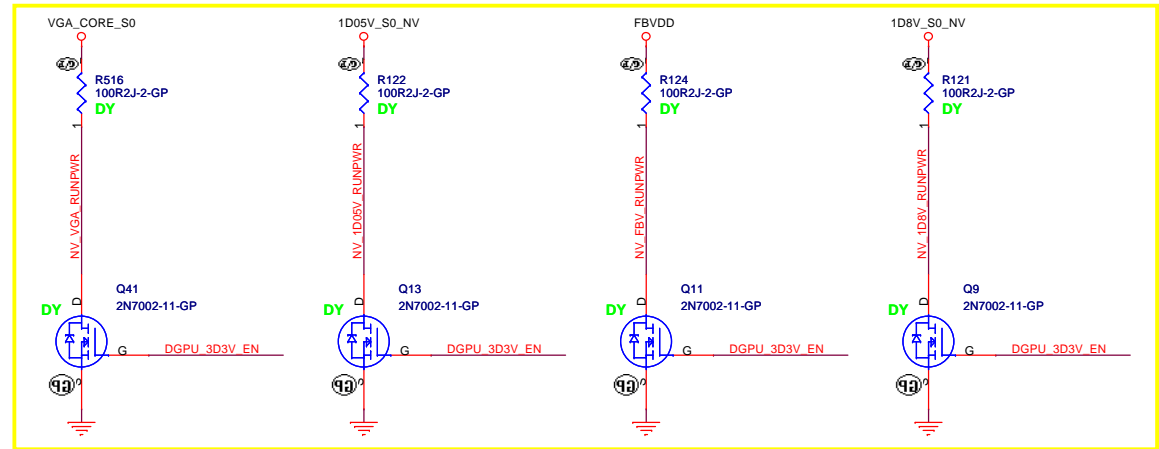
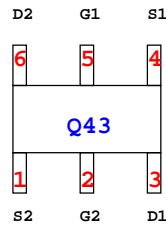
## +3VS to 3.3V\_DELAY Transfer

3.3v (580mA)

VDDR3discharge CKT



system turn on 3D3V\_S0\_NV --> VGA\_CORE\_S0  
DGPU\_PWROK --> FBVDD, 1D05V\_S0\_NV, 1D8V\_S0\_NV



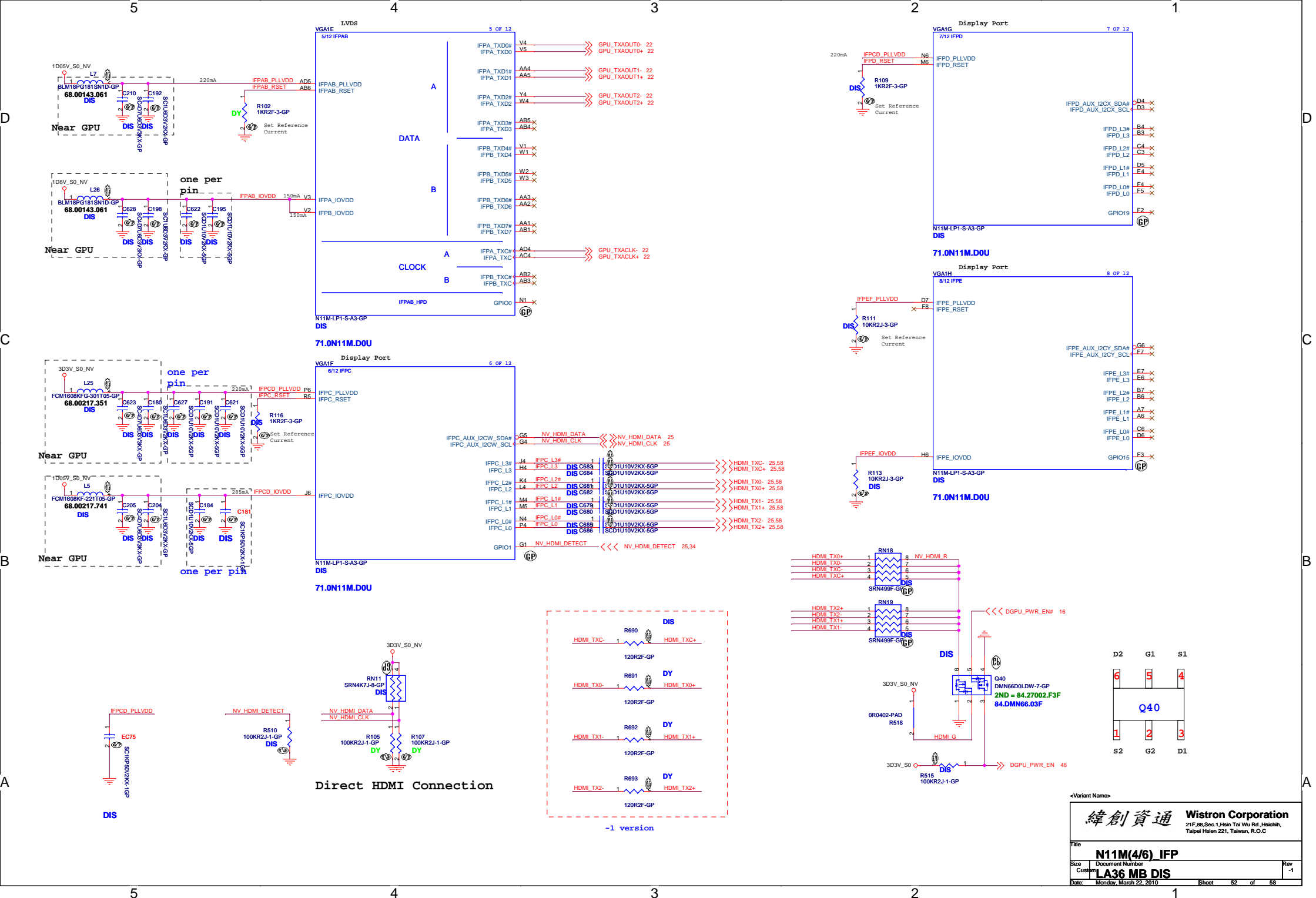
<Variant Name>

緯創資通 Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C	
File	
NV power	
Document Number	
LA36 MB DIS	
Size A3	Rev -1
Date: Monday, March 22, 2010	Sheet 48 of 58

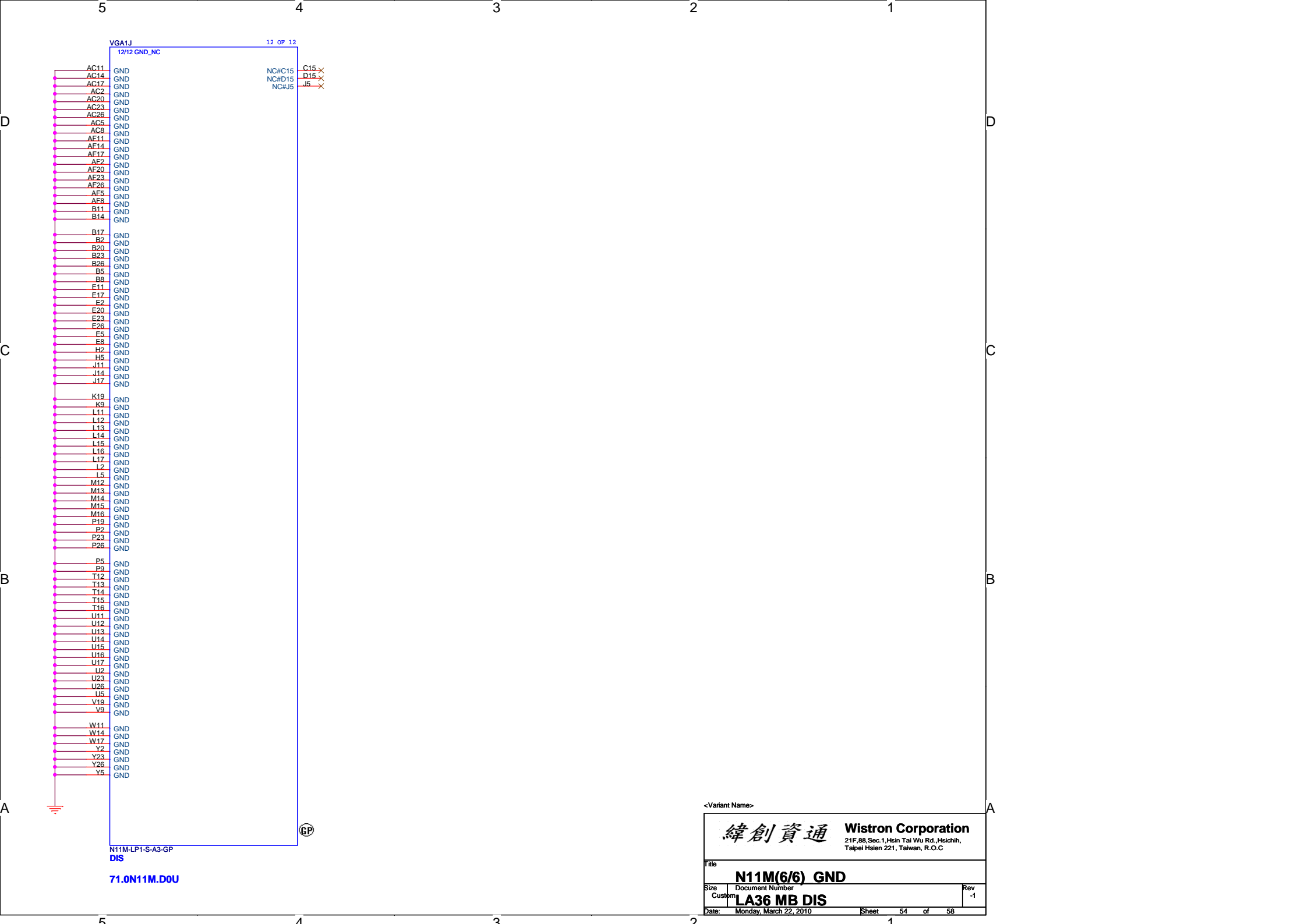












VGA1J 12 OF 12

12/12 GND\_NC

AC11 GND  
AC14 GND  
AC17 GND  
AC2 GND  
AC20 GND  
AC23 GND  
AC26 GND  
AC5 GND  
AC8 GND  
AF11 GND  
AF14 GND  
AF17 GND  
AF2 GND  
AF20 GND  
AF23 GND  
AF26 GND  
AF5 GND  
AF8 GND  
B11 GND  
B14 GND  
  
B17 GND  
B2 GND  
B20 GND  
B23 GND  
B26 GND  
B5 GND  
B8 GND  
E11 GND  
E17 GND  
E2 GND  
E20 GND  
E23 GND  
E26 GND  
E5 GND  
E8 GND  
H2 GND  
H6 GND  
J11 GND  
J14 GND  
J17 GND  
  
K19 GND  
K9 GND  
L11 GND  
L12 GND  
L13 GND  
L14 GND  
L15 GND  
L16 GND  
L17 GND  
L2 GND  
L5 GND  
M12 GND  
M13 GND  
M14 GND  
M15 GND  
M16 GND  
P19 GND  
P2 GND  
P23 GND  
P26 GND  
  
P5 GND  
P9 GND  
T12 GND  
T13 GND  
T14 GND  
T15 GND  
T16 GND  
U11 GND  
U12 GND  
U13 GND  
U14 GND  
U15 GND  
U16 GND  
U17 GND  
U2 GND  
U23 GND  
U26 GND  
U5 GND  
V19 GND  
V9 GND  
  
W11 GND  
W14 GND  
W17 GND  
Y2 GND  
Y23 GND  
Y26 GND  
Y5 GND

NC#C15  
NC#D15  
NC#J5

C15  
D15  
J5

N11M-LP1-S-A3-GP  
DIS

71.0N11M.D0U

<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec. 1, Heil Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C			
File			
<b>N11M(6/6) GND</b>			
Size	Document Number	Rev	-1
Custom	<b>LA36 MB DIS</b>		
Date:	Monday, March 22, 2010	Sheet	54 of 58

D

C

B

<Variant Name>

緯創資通

**Wistron Corporation**

21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C

	<b>Title</b>
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## VRAM(1/2)

Size	Document Number
Custom	<b>LA36 MB DIS</b>

Rev  
-1

Date: Monday, March 22, 2010

Sheet 55 of 58

