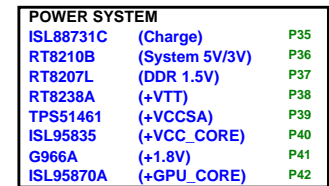


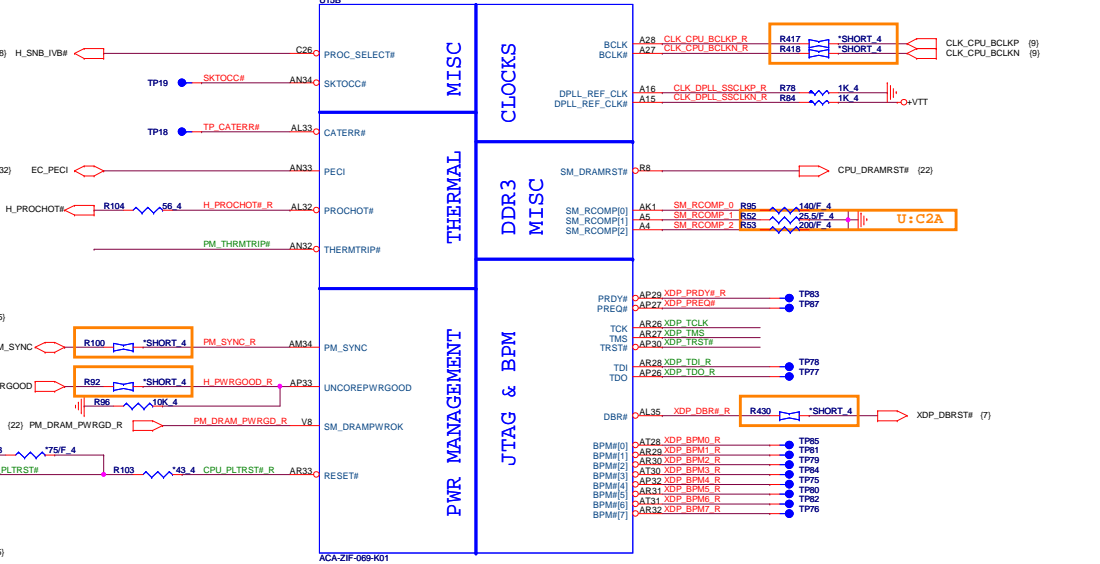
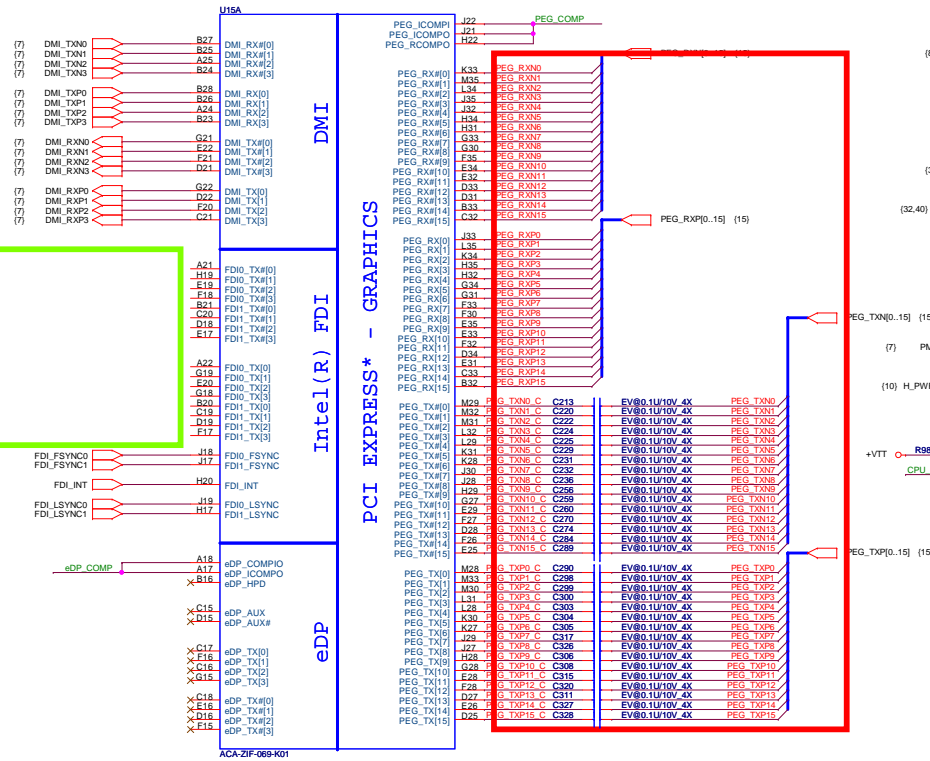
01



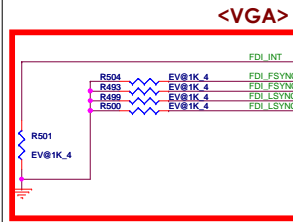
Sandy Bridge Processor (DMI,PEG,FDI) <CPU,VGA>

Sandy Bridge Processor (CLK,MISC,JTAG)<CPU>

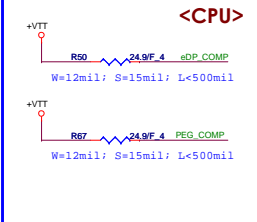
03



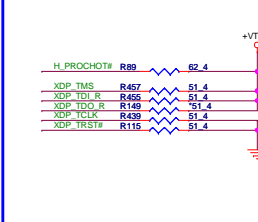
FDI Disabling (Discrete Only)



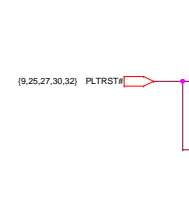
DP & PEG Compensation



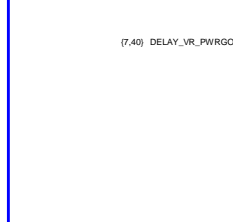
Processor pull-up <CPU>



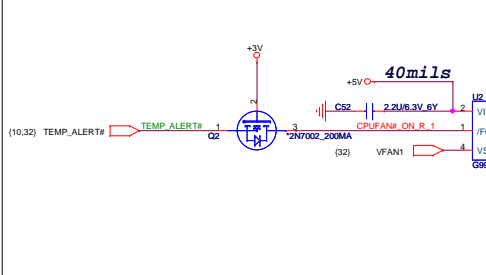
Level Shift <CPU>



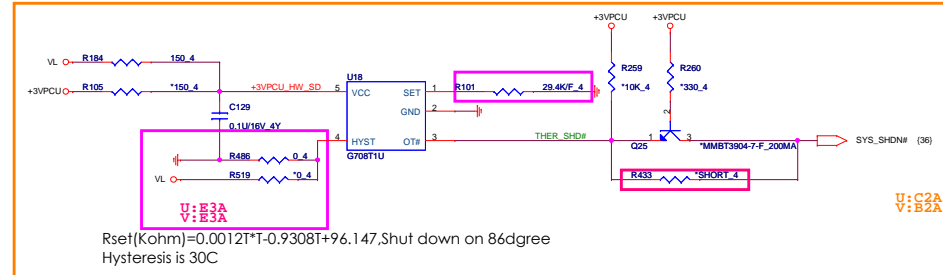
Thermal Trip <CPU>



FAN Control-->For one FAN solution <THC/THV>

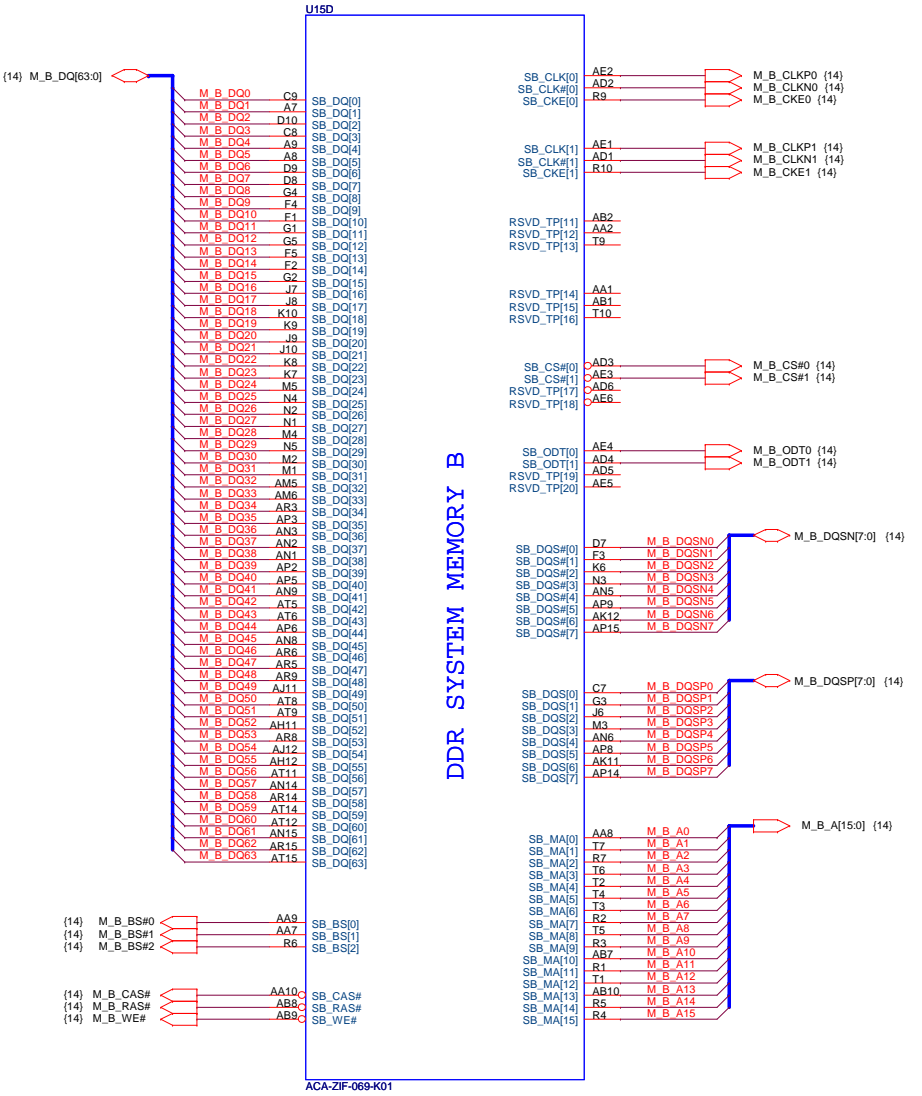
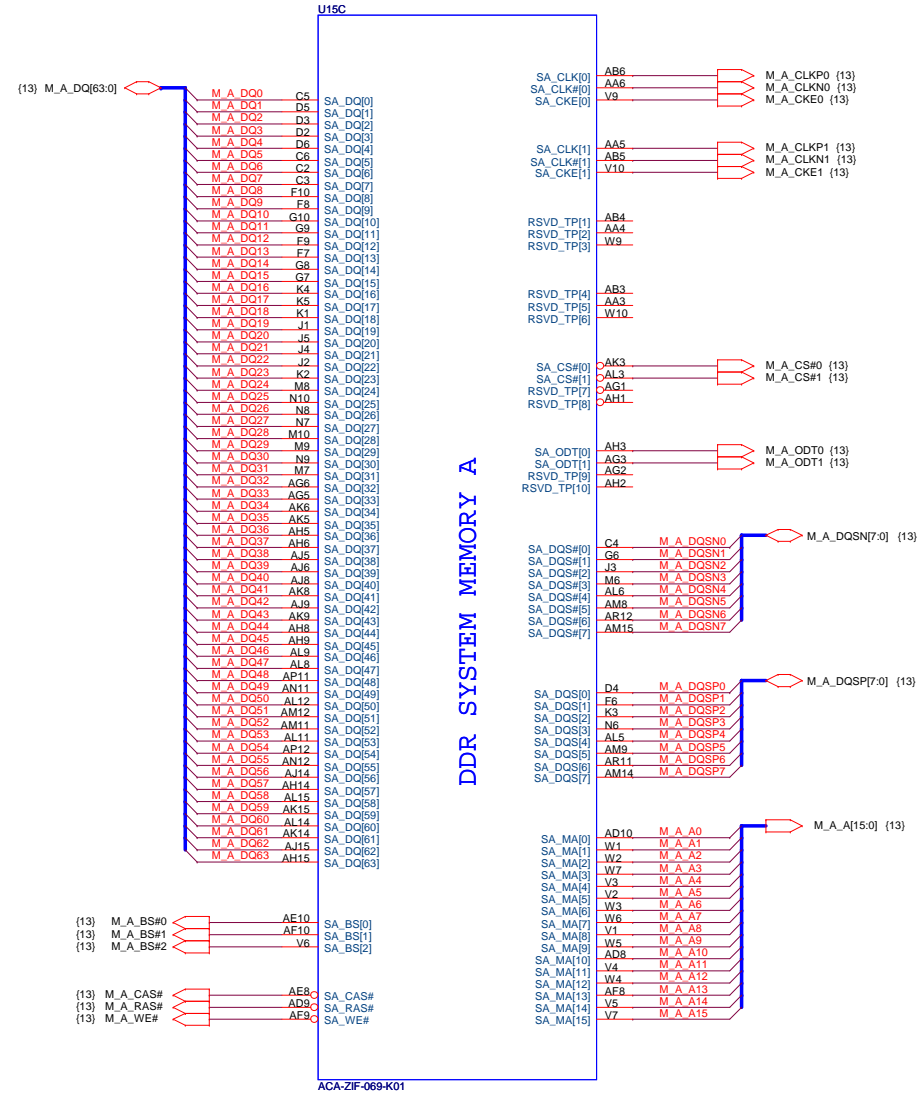


CPU Thermal sensor / MB Local TEMP <THC>



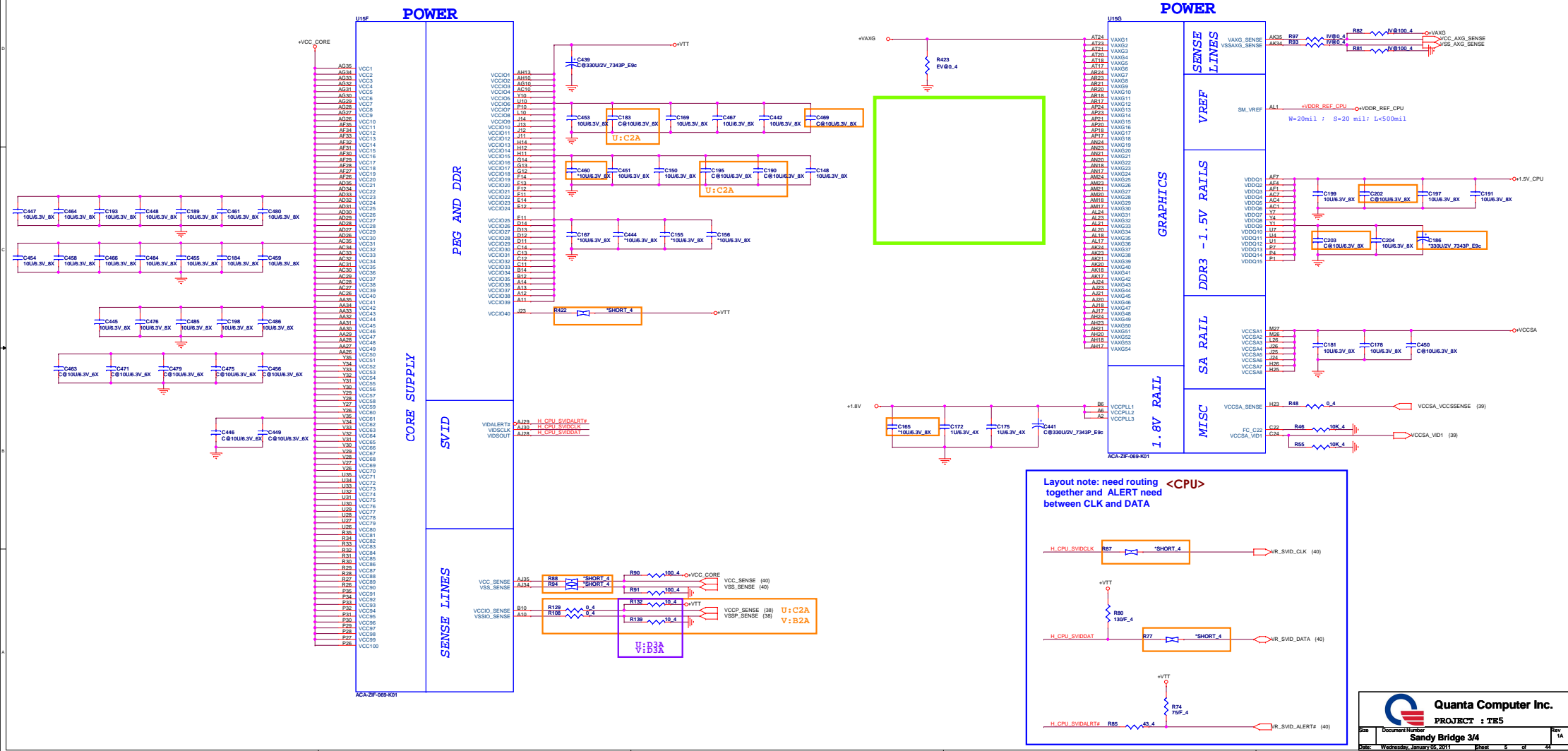
Sandy Bridge Processor (DDR3)

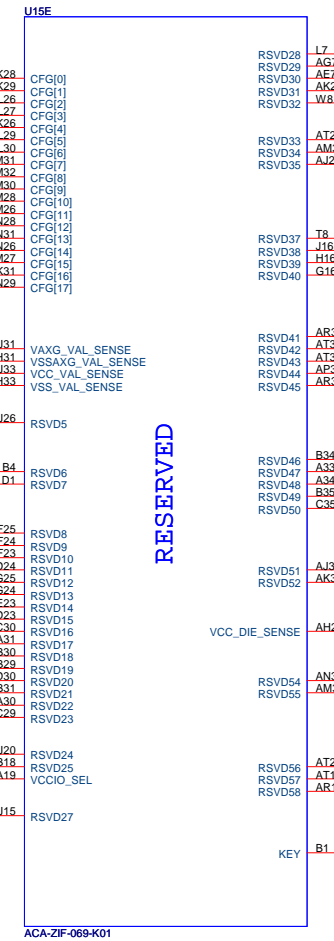
04



Sandy Bridge Processor (POWER)<CPU>

Sandy Bridge Processor (GRAPHIC POWER)<CPU,UGA>





```
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```

CFG2 R136 EV@1K_4

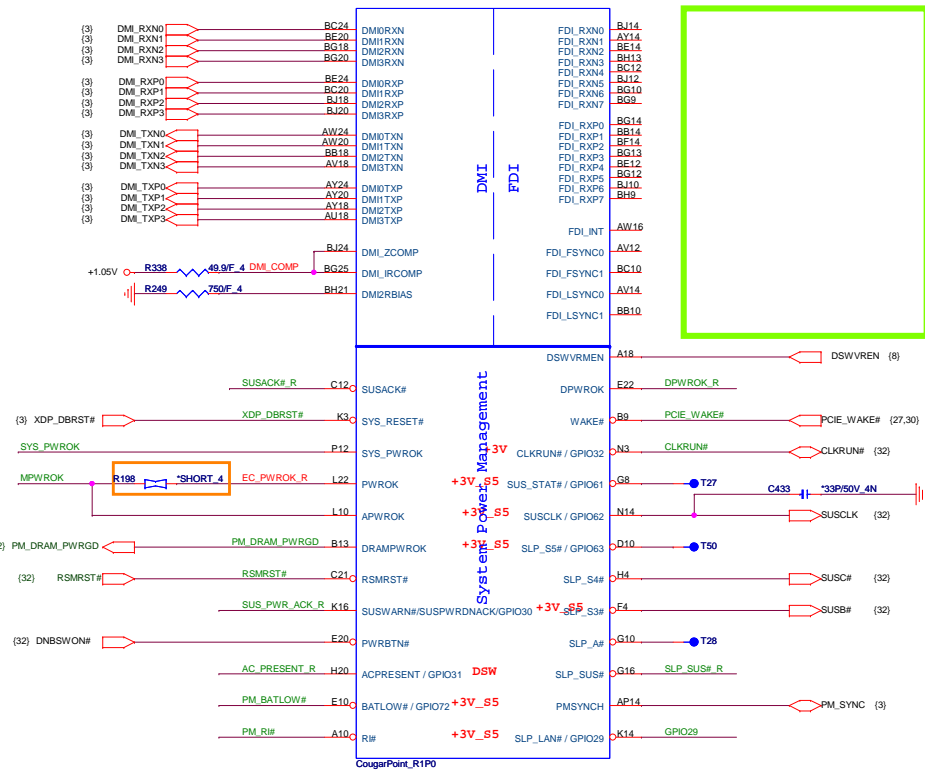
CFG4 R79 *1K_4

CFG7 R109 *1K_4



Cougar Point (DMI,FDI,PM)<CLG>

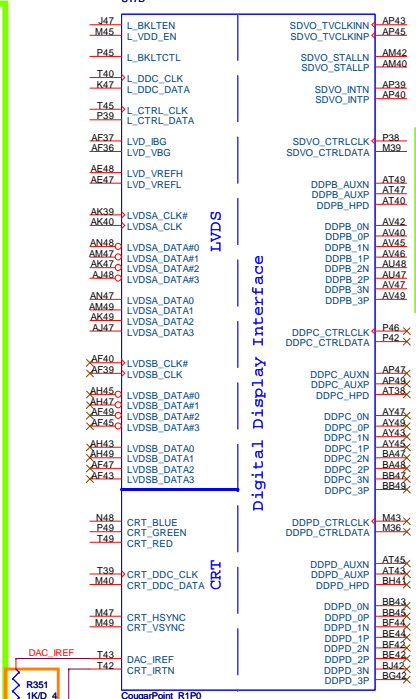
U17C



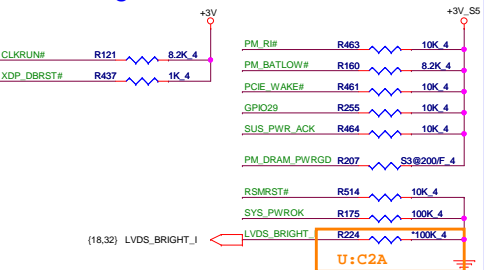
Cougar Point (LVDS,DDI)<CLG/UGA/HMG>

U17D

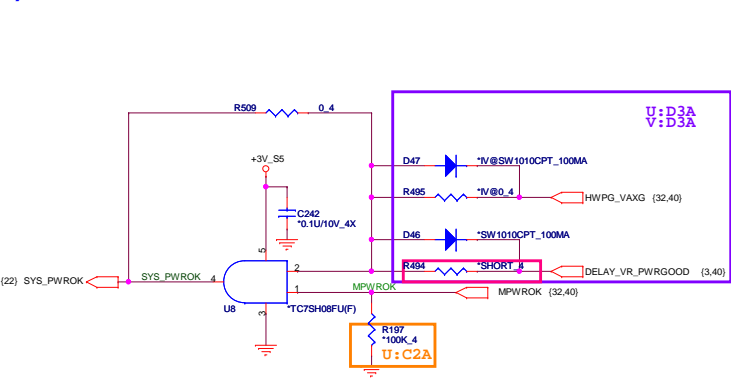
<CLG,UGA,HMG>



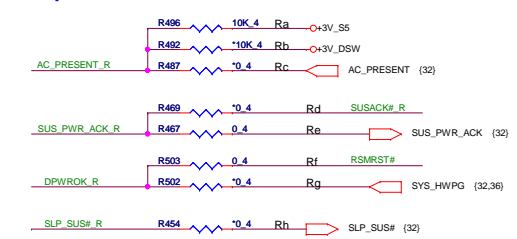
PCH Pull-high/low<CLG>



System PWR_OK <CLG>

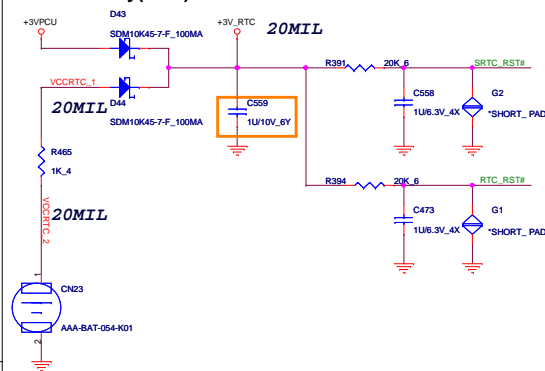


Deep Sx <CLG>

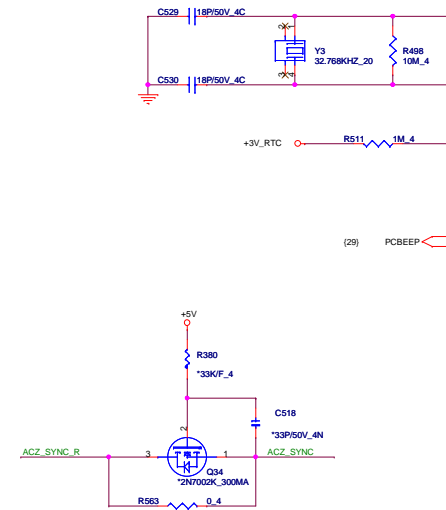


Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

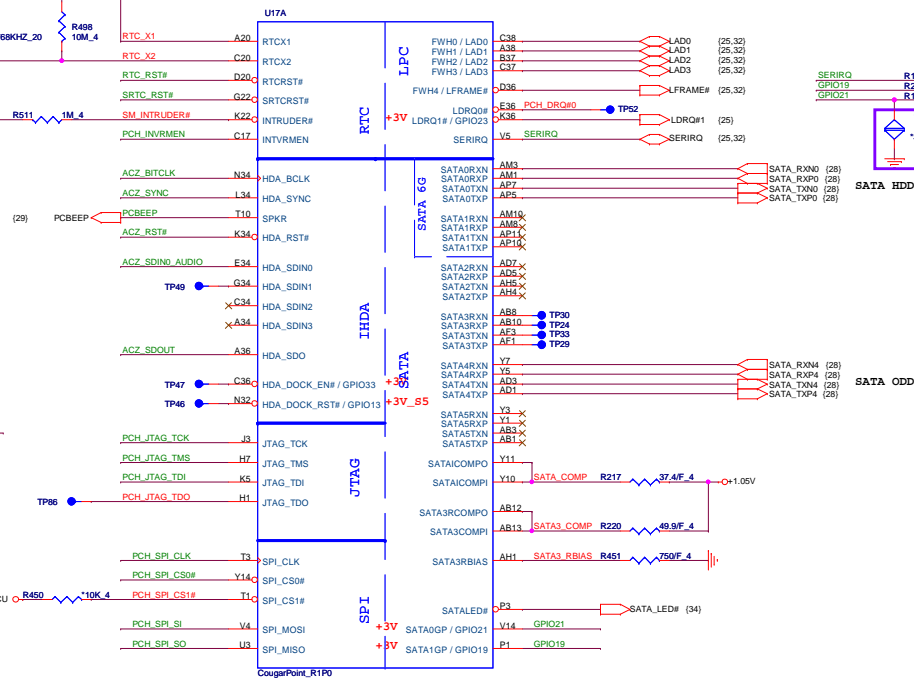
RTC Circuitry(RTC)



PCH2 (CLG)



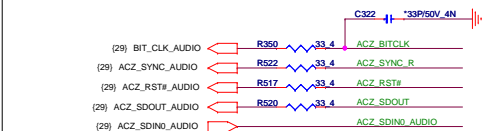
Cougar Point (HDA,JTAG,SATA)



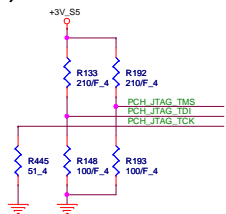
SATA HDD/SSD

SATA ODD

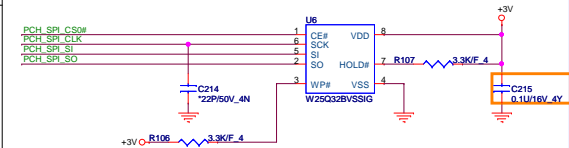
HDA Bus(CLG)



PCH JTAG Debug (CLG)



PCH Dual SPI (CLG)

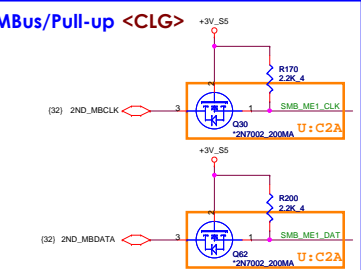
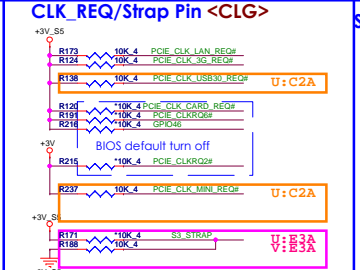
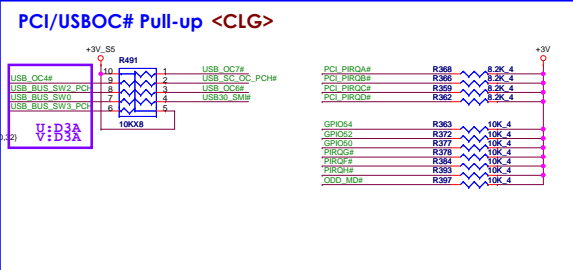
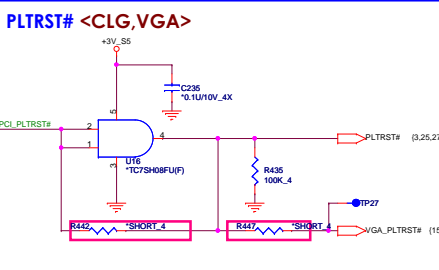
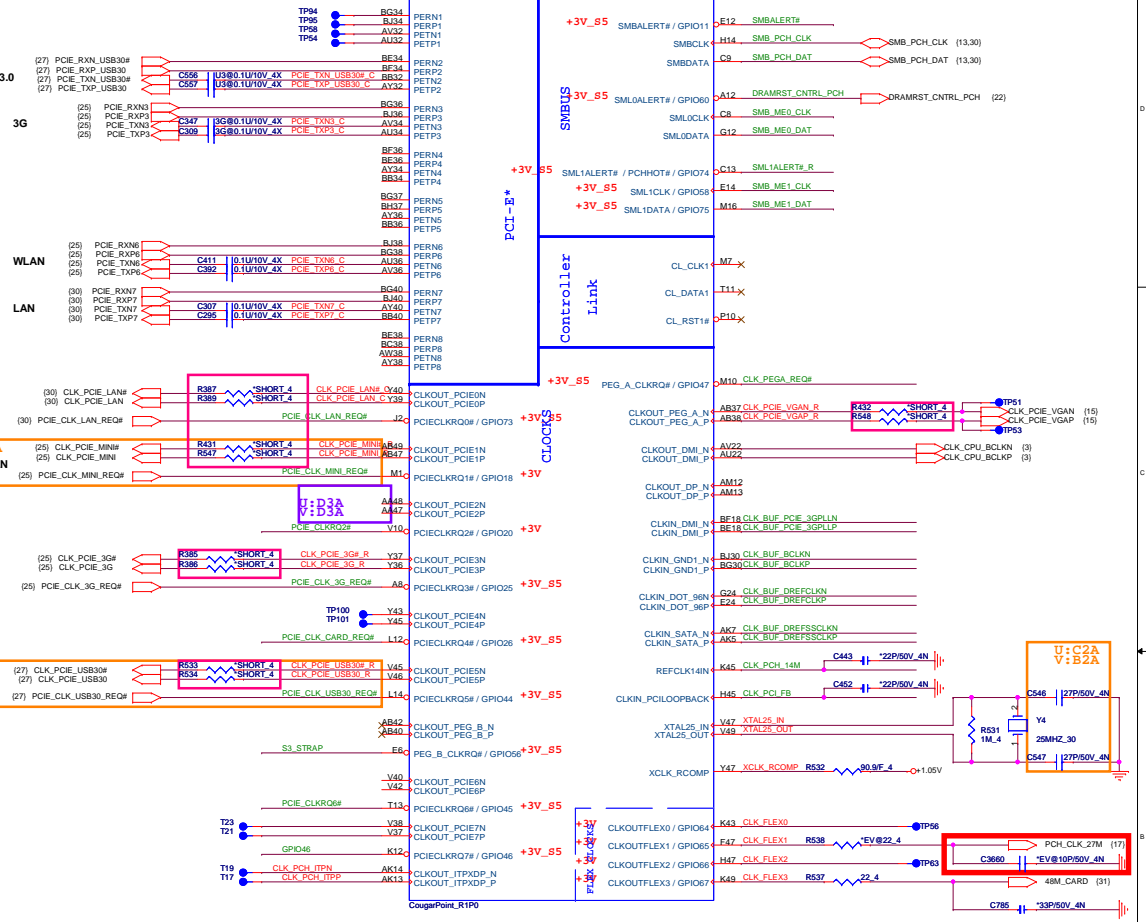
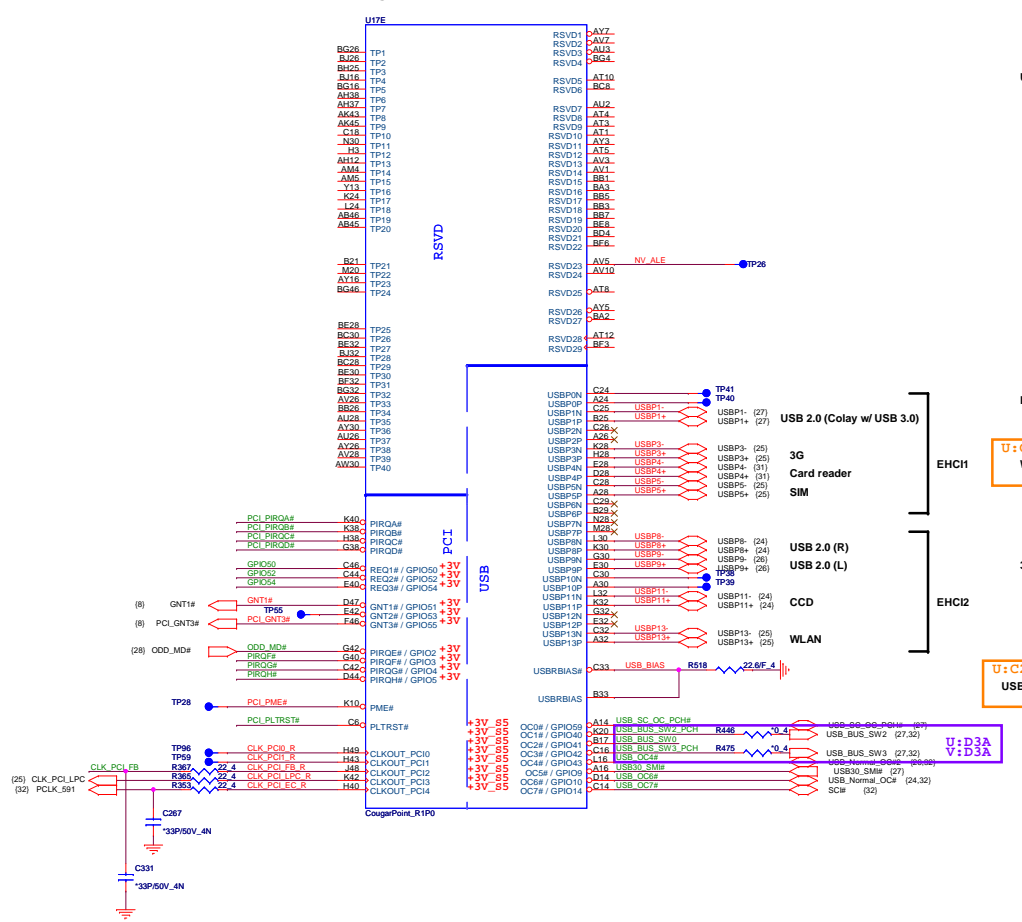


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V ₀ R116 1K 4 PCBEEP									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R530 1K 4 PCL_GNT3# (9)									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R497 330K 4 PCH_INVRMEN									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><th>GNT1#</th><th>GPIO19</th><th>Boot Location</th></tr><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	GNT1#	GPIO19	Boot Location	1	1	SPI *	0	0	LPC	R539 1K 4 GNT1# (9) R449 1K 4 GPIO19
GNT1#	GPIO19	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V ₀ R521 1K 4 ACZ_SDOUT ACZ_SDOUT									
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R453 2.2K 4 +0.18V DF_TVS (10) R452 1K 4 H_SNB_IVB#									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	+3V_S5 R208 10K 4 PLL_ODVR_EN (10) R195 1K 4									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R525 1K 4 ACZ_SYNC									
INIT3_3V#	Reserved	PWROK	1 = Default (weak pull-up 20K)	Should not pull low. leave as No Connect									
GNT2# / GPIO53	ESI Strap (Server Only)	PWROK	1 = Default. Should not be pulled low for desktop and mobile	Should not pull low for desktop and mobile									
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS No Confidentiality 1 = TLS Confidentiality	+3V_S5 R313 1K 4 GPIO15 (10)									
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1 = PU to 3V									
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1 = PU to 3V									
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC									
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC									
SATA3GP / GPIO37	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled									
SATA2GP / GPIO36	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled									
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	+3V_RTC R489 330K 4 DSWVREN (7) R490 330K 4									

Cougar Point-M (PCI,USB,NVRAM) <CLG>

Cougar Point-M (PCI-E,SMBUS,CLK) <CLG,U3B,VGA,MNG>



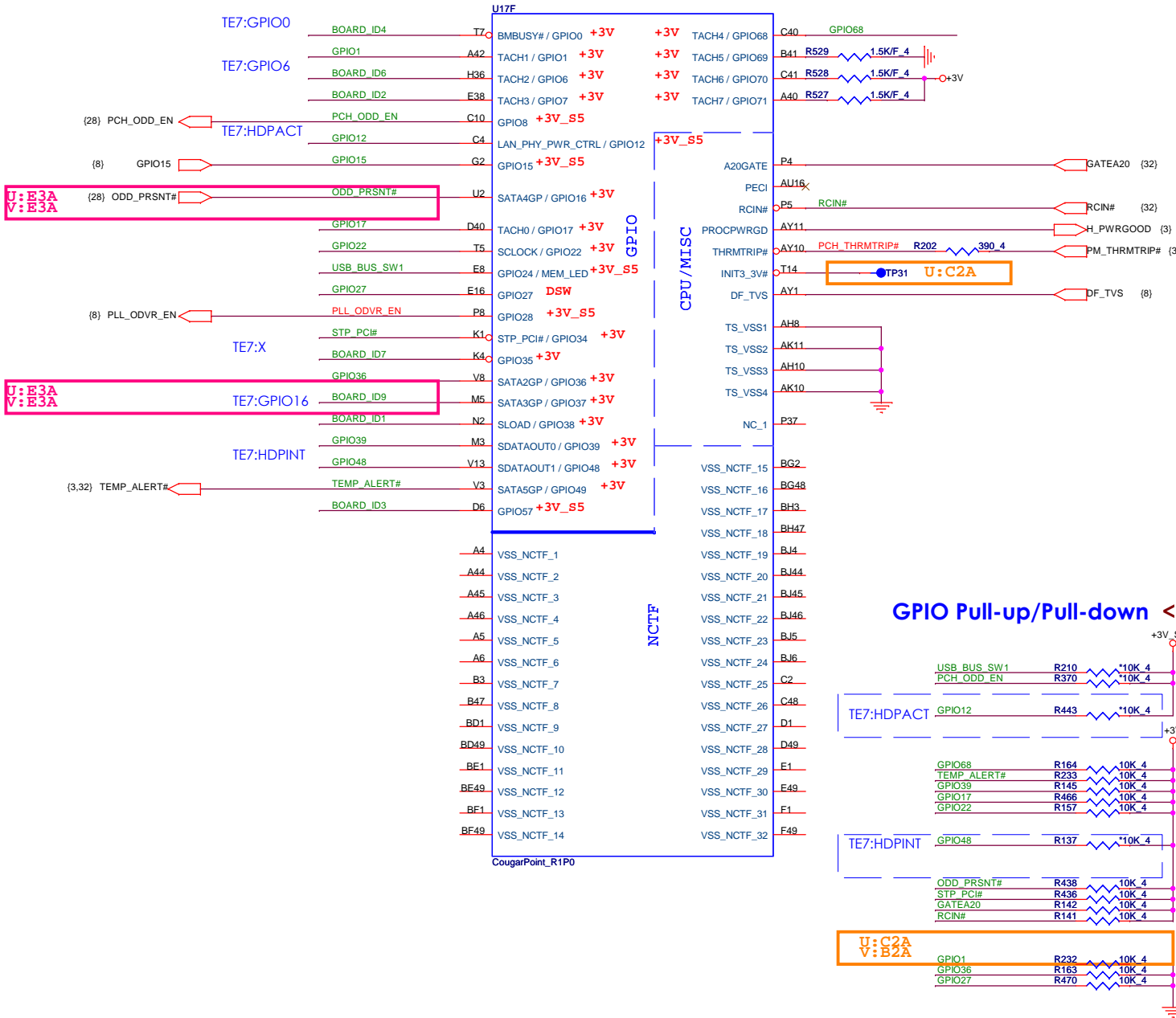
	33MHz	27MHz	18/24MHz	14.318MHz	25MHz
CLK_FLEX0					
CLK_FLEX1					
CLK_FLEX2					
CLK_FLEX3					

Cougar Point (GPIO,VSS_NCTF,RSVD) <CLG>

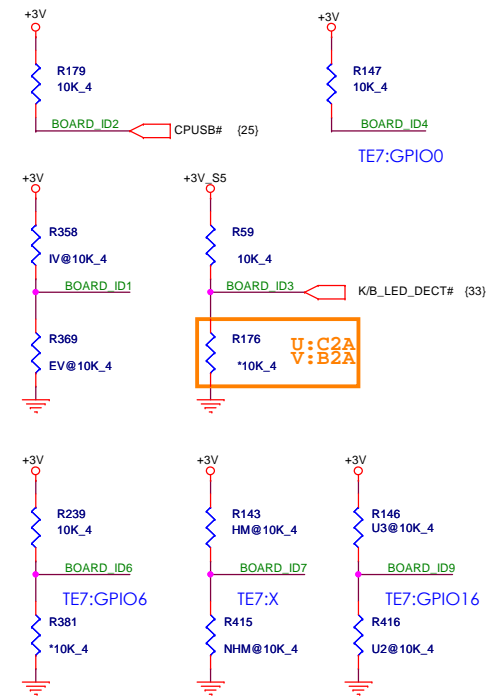
BOARD ID SETTING <CLG>

10

Board ID	ID1	ID2	ID3	ID4	ID6	ID7	ID9	GPIO1
UMA SKU VGA SKU	H L							
W/O 3G W/ 3G		H L						
W/O LED KB W/ LED KB			H L					
14" 15"				H L				
W/ MDC W/O MDC					H L			
W/ HDMI W/O HDMI						H L		
USB3.0 USB2.0							H L	
W/ G-sensor W/O G-sensor								H L



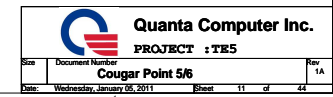
U:C2A



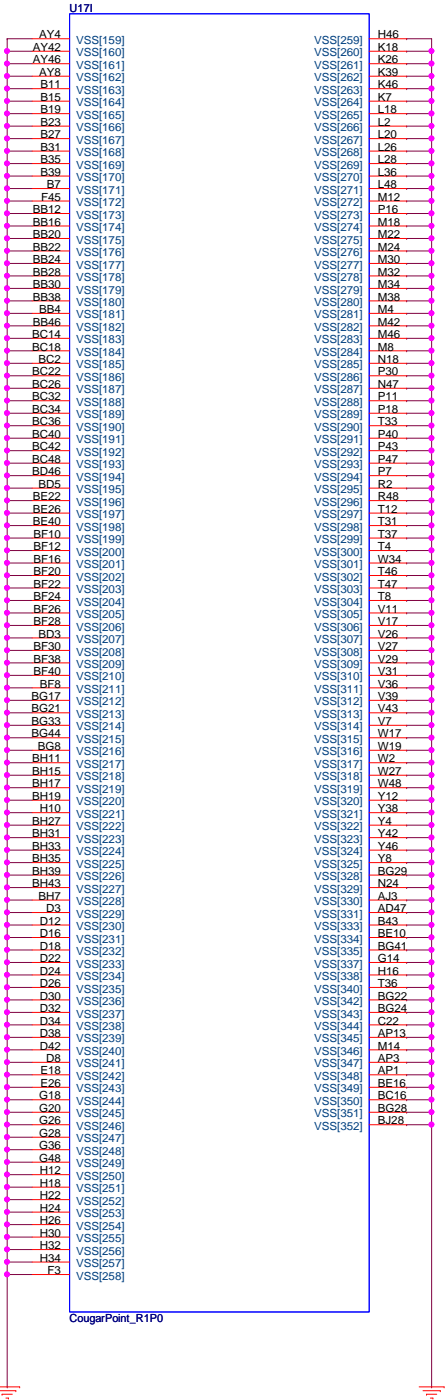
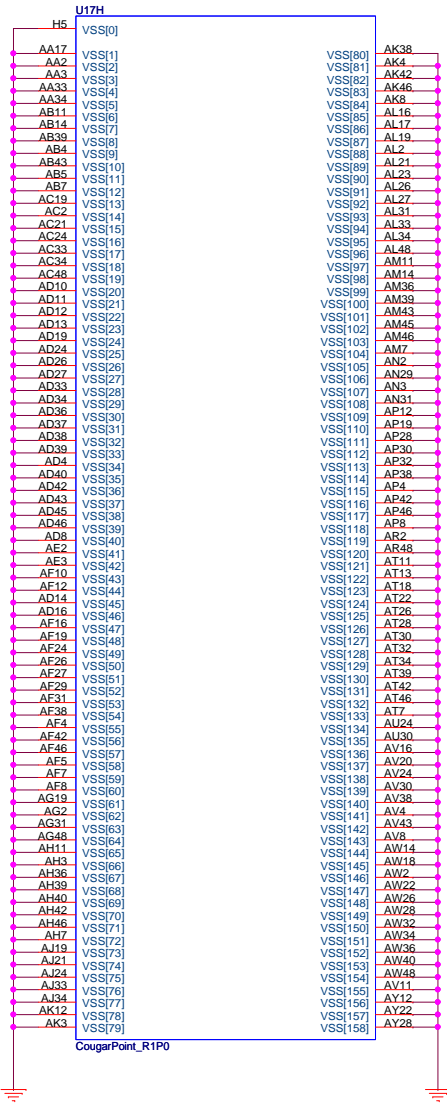
Quanta Computer Inc.
PROJECT : TE5

Size	Document Number	Rev
	Cougar Point 4/6	1A
Date:	Wednesday, January 05, 2011	Sheet 10 of 44

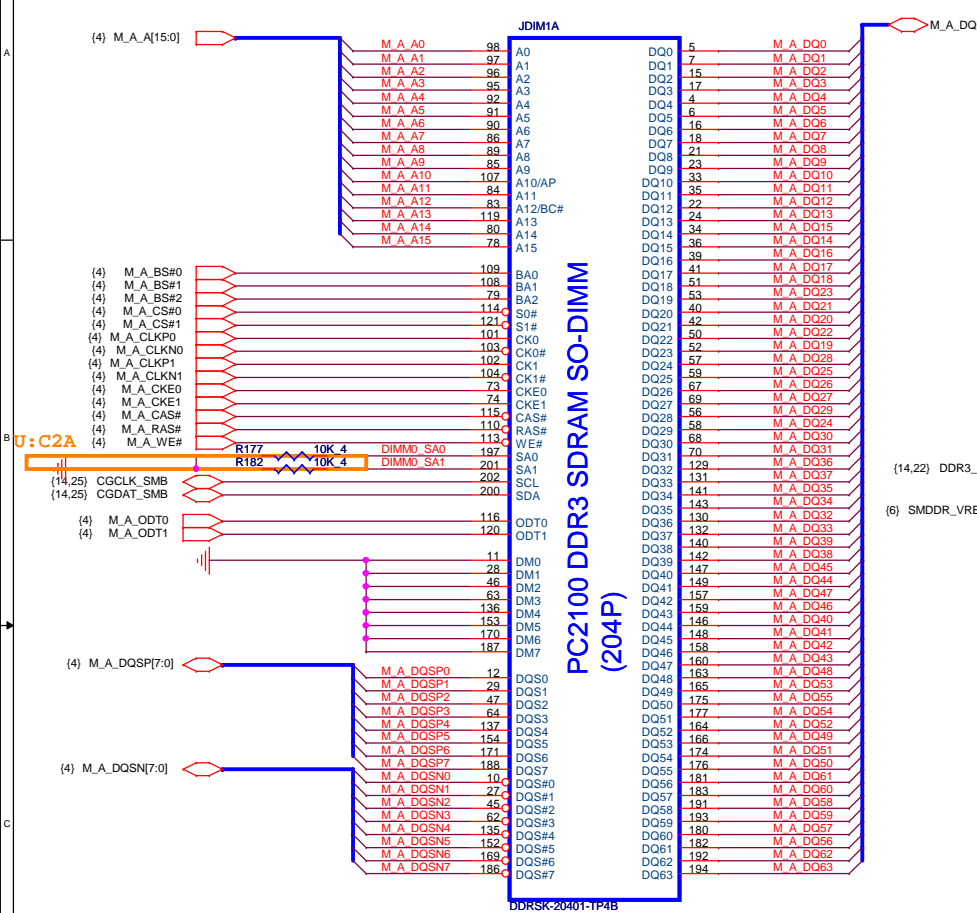
Cougar Point-M (POWER)



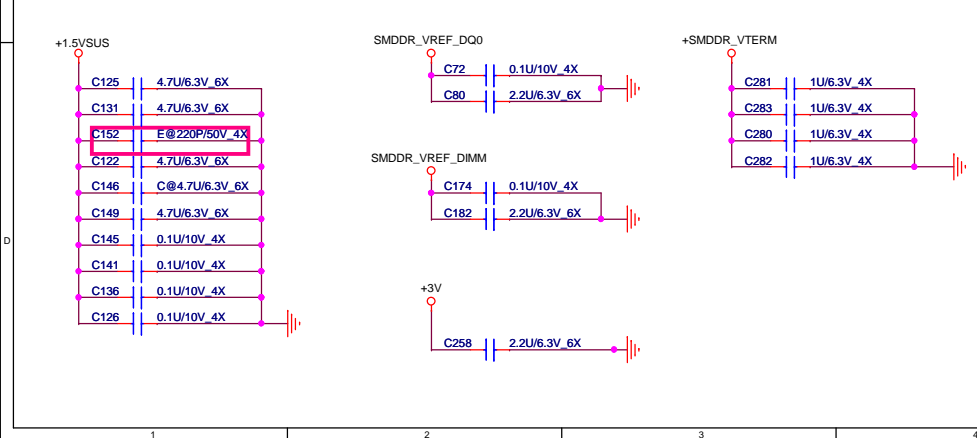
IBEX PEAK-M (GND)



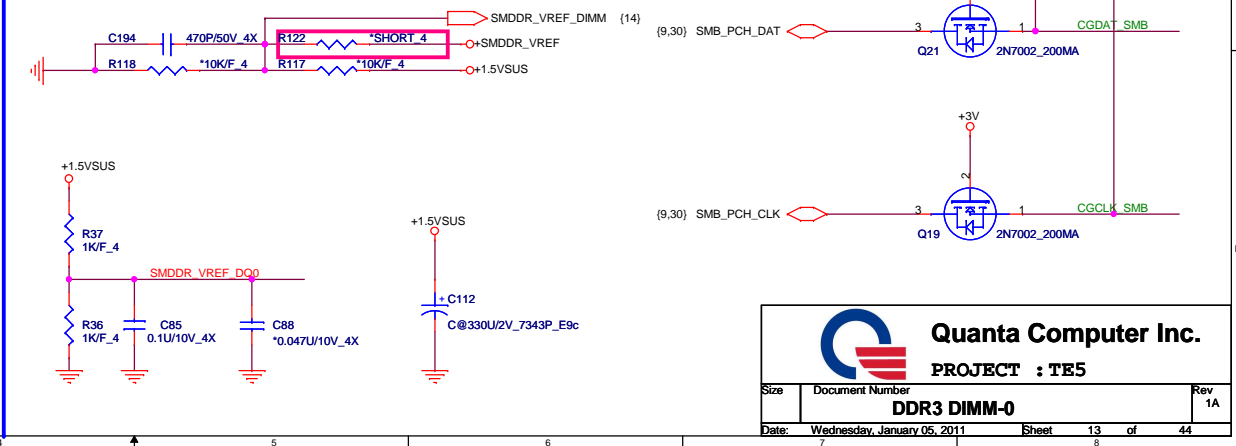
<DDR>



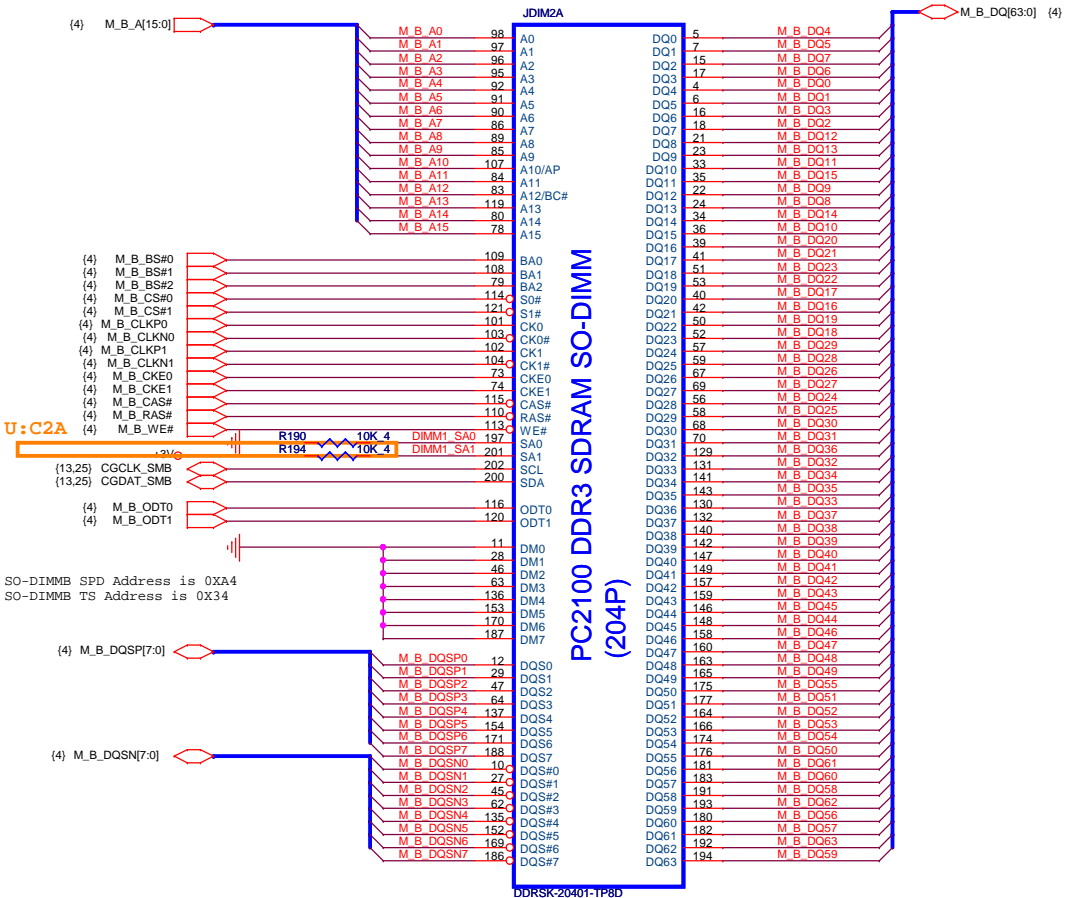
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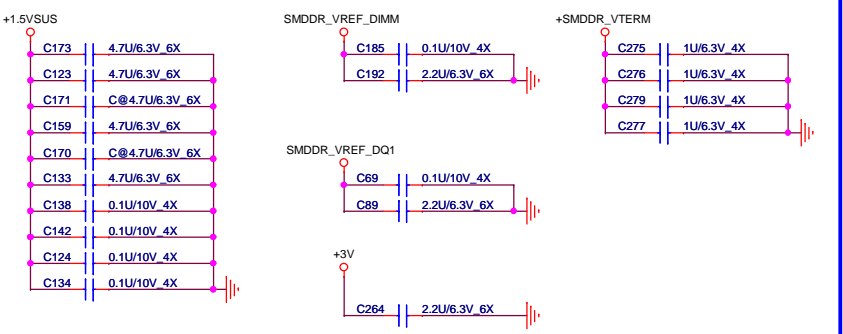
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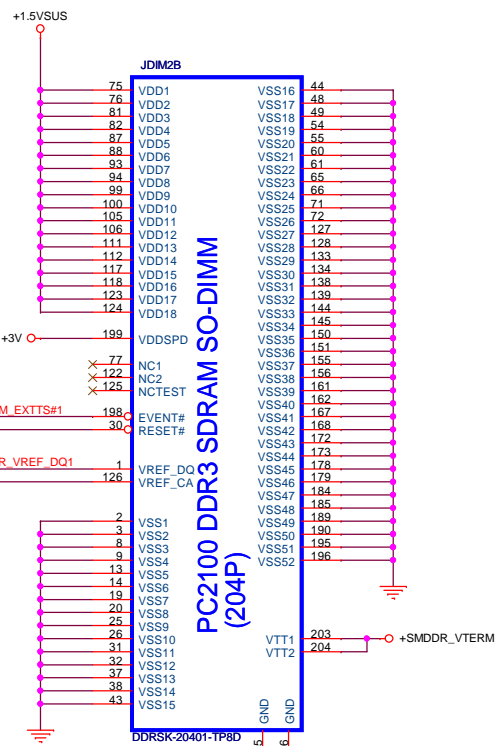
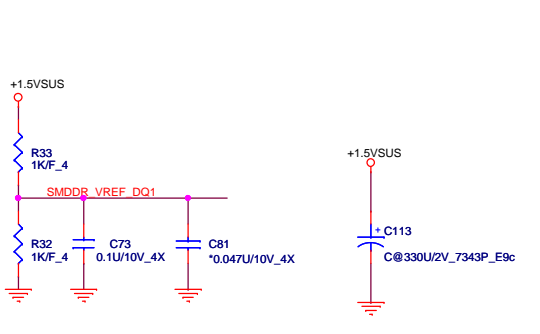
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<DDR>

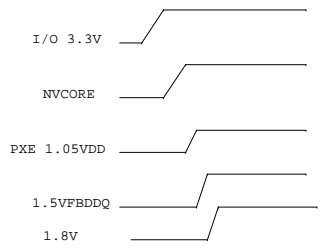


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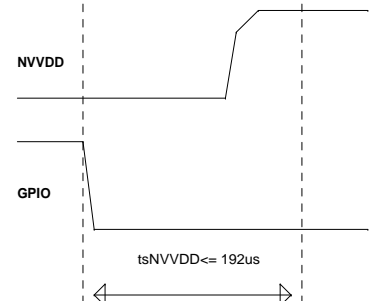


15-V

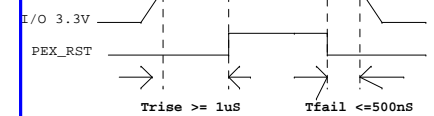
power up sequence



NB9M: VGACORE +0.90V (Normal) , +1.09V
NVVDD Maximum Settling Time



PEX_RST timing



PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

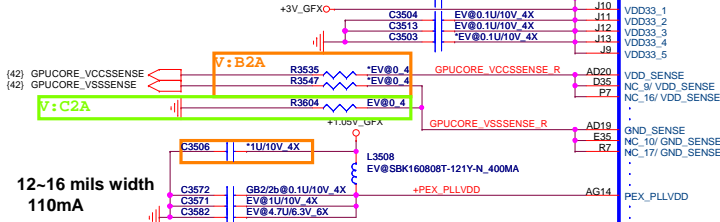
~ 500mA

+1.05V_GFX

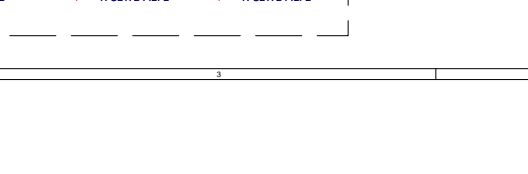
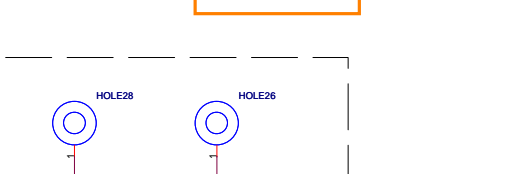
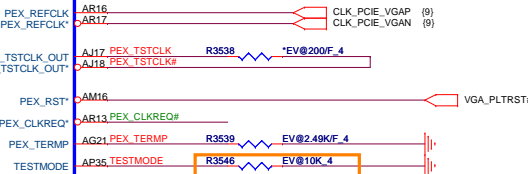
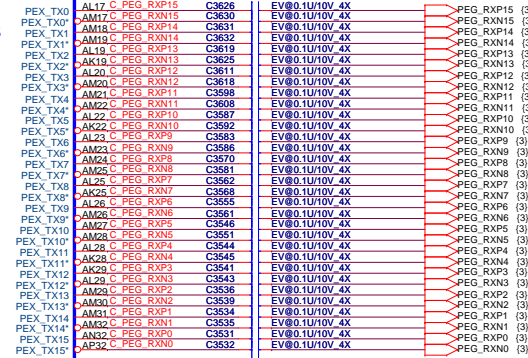
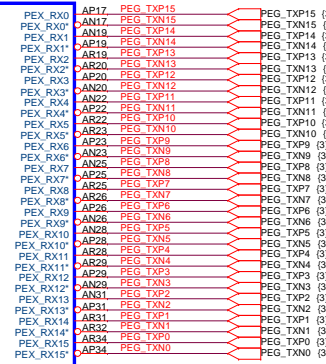
1600mA

+1.05V_GFX

+1.05V_GFX



PCI EXPRESS



VGA HOLE HOLE27 HOLE28 HOLE26

*H-C217D142P2

GPU3500B

16qg075.midea11p-as-a1

COMMON

(20) FBA_CMD0	Y32	FBA_CMD0	FBA_D00	L32	VMA_D00
(20) FBA_CMD1	W31	FBA_CMD1	FBA_D01	L33	VMA_D01
(20) FBA_CMD2	Y32	FBA_CMD2	FBA_D02	L33	VMA_D02
(20) FBA_CMD3	Y32	FBA_CMD3	FBA_D03	N34	VMA_D03
(20) FBA_CMD4	AB35	FBA_CMD4	FBA_D04	N35	VMA_D04
(20) FBA_CMD5	AB34	FBA_CMD5	FBA_D05	P33	VMA_D05
(20) FBA_CMD6	W33	FBA_CMD6	FBA_D06	P34	VMA_D06
(20) FBA_CMD7	W33	FBA_CMD7	FBA_D07	P34	VMA_D07
(20) FBA_CMD8	W30	FBA_CMD8	FBA_D08	K35	VMA_D08
(20) FBA_CMD9	T34	FBA_CMD9	FBA_D09	K34	VMA_D09
(20) FBA_CMD10	T35	FBA_CMD10	FBA_D10	H33	VMA_D10
(20) FBA_CMD11	AB31	FBA_CMD11	FBA_D11	H33	VMA_D11
(20) FBA_CMD12	Y30	FBA_CMD12	FBA_D12	G33	VMA_D12
(20) FBA_CMD13	W32	FBA_CMD13	FBA_D13	G33	VMA_D13
(20) FBA_CMD14	W32	FBA_CMD14	FBA_D14	E34	VMA_D14
(20) FBA_CMD15	AA30	FBA_CMD15	FBA_D15	E33	VMA_D15
(20) FBA_CMD16	AA32	FBA_CMD16	FBA_D16	G31	VMA_D16
(20) FBA_CMD17	U32	FBA_CMD17	FBA_D17	F30	VMA_D17
(20) FBA_CMD18	Y31	FBA_CMD18	FBA_D18	G30	VMA_D18
(20) FBA_CMD19	U34	FBA_CMD19	FBA_D19	G32	VMA_D19
(20) FBA_CMD20	Y35	FBA_CMD20	FBA_D20	K30	VMA_D20
(20) FBA_CMD21	W34	FBA_CMD21	FBA_D21	K32	VMA_D21
(20) FBA_CMD22	Y30	FBA_CMD22	FBA_D22	H30	VMA_D22
(20) FBA_CMD23	U30	FBA_CMD23	FBA_D23	K31	VMA_D23
(20) FBA_CMD24	U30	FBA_CMD24	FBA_D24	L31	VMA_D24
(20) FBA_CMD25	U33	FBA_CMD25	FBA_D25	L30	VMA_D25
(20) FBA_CMD26	AB30	FBA_CMD26	FBA_D26	M32	VMA_D26
(20) FBA_CMD27	AB33	FBA_CMD27	FBA_D27	N30	VMA_D27
(20) FBA_CMD28	T33	FBA_CMD28	FBA_D28	M30	VMA_D28
(20) FBA_CMD29	W29	FBA_CMD29	FBA_D29	P31	VMA_D29
(20) FBA_CMD30	W29	FBA_CMD30	FBA_D30	R32	VMA_D30

VMA_DM0	P32	FBA_DQM0
VMA_DM1	H34	FBA_DQM1
VMA_DM2	J30	FBA_DQM2
VMA_DM3	F30	FBA_DQM3
VMA_DM4	AF32	FBA_DQM4
VMA_DM5	AL32	FBA_DQM5
VMA_DM6	AL34	FBA_DQM6
VMA_DM7	AF35	FBA_DQM7

VMA_WDS0	L34	FBA_DQS_WP0
VMA_WDS1	H35	FBA_DQS_WP1
VMA_WDS2	J32	FBA_DQS_WP2
VMA_WDS3	N31	FBA_DQS_WP3
VMA_WDS4	AF31	FBA_DQS_WP4
VMA_WDS5	AL34	FBA_DQS_WP5
VMA_WDS6	AJ34	FBA_DQS_WP6
VMA_WDS7	AC33	FBA_DQS_WP7

VMA_RDQS0	L35	FBA_DQS_RN0
VMA_RDQS1	G35	FBA_DQS_RN1
VMA_RDQS2	H31	FBA_DQS_RN2
VMA_RDQS3	N32	FBA_DQS_RN3
VMA_RDQS4	AD32	FBA_DQS_RN4
VMA_RDQS5	AJ31	FBA_DQS_RN5
VMA_RDQS6	AJ35	FBA_DQS_RN6
VMA_RDQS7	AC34	FBA_DQS_RN7

P29	FBA_WCK0
R29C	FBA_WCK0_N
L29	FBA_WCK1
M29C	FBA_WCK1_N
AG29	FBA_WCK2
AD29	FBA_WCK2_N
AE29C	FBA_WCK3
AE29C	FBA_WCK3_N

AA27	FBVDDQ_1
AA29	FBVDDQ_2
AA31	FBVDDQ_3
AB27	FBVDDQ_4
AB29	FBVDDQ_5
AC27	FBVDDQ_6
AE27	FBVDDQ_7
AJ28	FBVDDQ_8
B18	FBVDDQ_9
E21	FBVDDQ_10
G17	FBVDDQ_11
G18	FBVDDQ_12
G22	FBVDDQ_13
G8	FBVDDQ_14
G9	FBVDDQ_15
H29	FBVDDQ_16
J14	FBVDDQ_17
J15	FBVDDQ_18
J16	FBVDDQ_19
J17	FBVDDQ_20
J20	FBVDDQ_21
J21	FBVDDQ_22
J23	FBVDDQ_23
J24	FBVDDQ_24
J25	FBVDDQ_25
J26	FBVDDQ_26
J27	FBVDDQ_27

MEMORY I/F A

FB_VREF

FBA_CMD31(Fermi)

FBA_DEBUG1(Fermi)

FBA_DEBUG

FB_DLLAVDD0

FB_PLLAVDD0

15mils width

Y29

T29

T30

AG27

AF27

15mils width

Y29

T29

T30

AG27

AF27

15mils width

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AG27

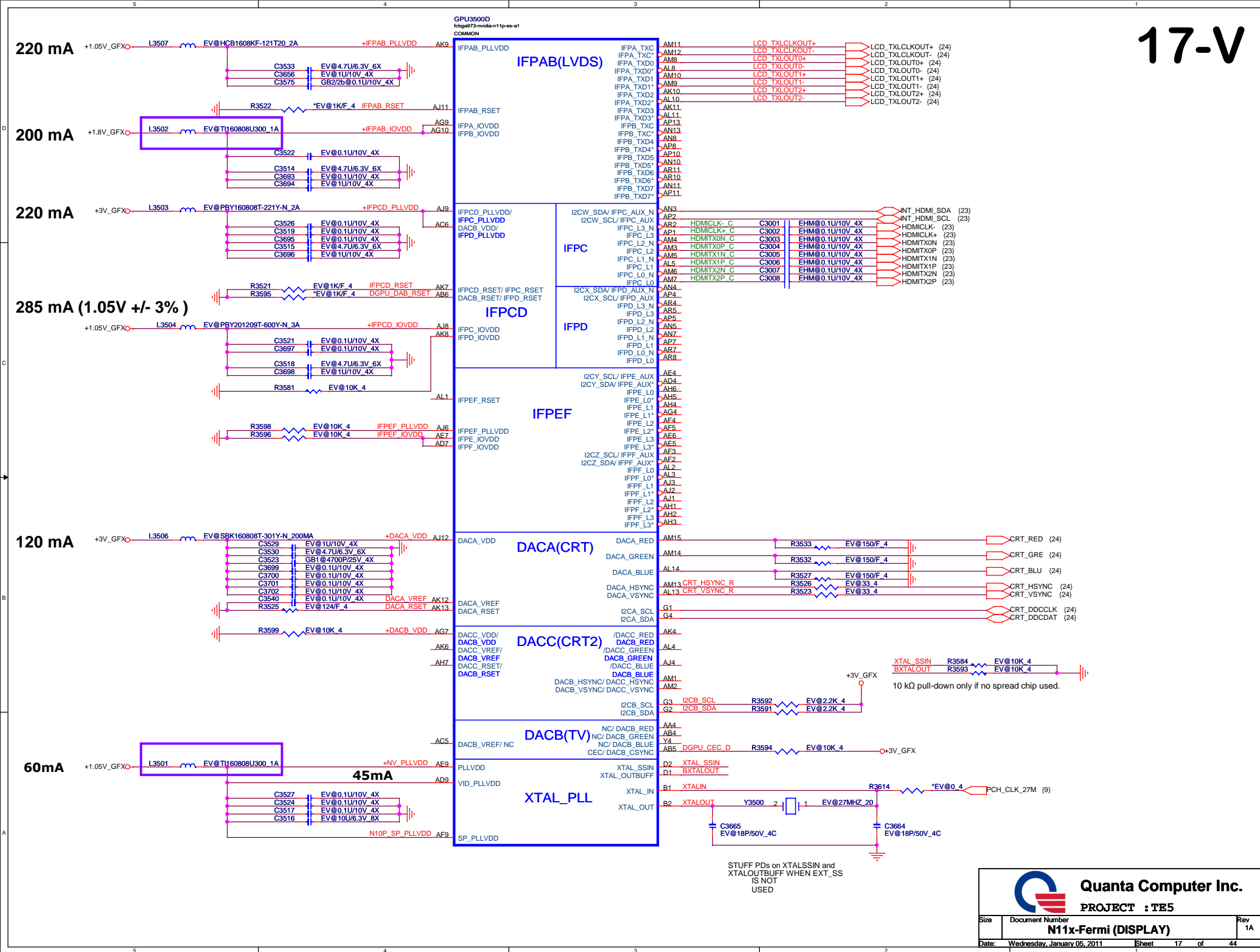
AF27

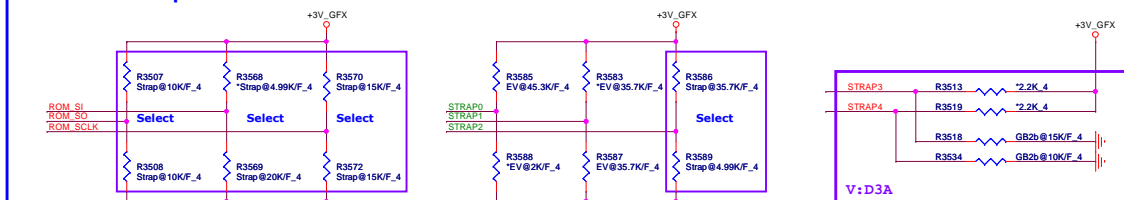
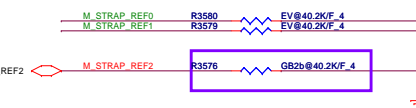
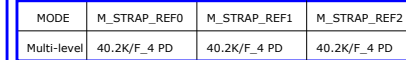
15mils width

Y29

T29

17-V





	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	N12M-GE	N12P-GV	N12P-LP	
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG[5]	PEX_PLL_EN_TERM	1010(15KPU)	1001(10KPU)	0010(15KPD)	
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	RAMCFG 7	RAMCFG 7	RAMCFG 7	
ROM_SO	GB1/2	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VMA_DEVICE	0001(10KPD)	0001(10KPD)	
	GB2B	FB[1]	FB[0]			1001(10KPU)		Need to Update
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111(45KPU)	1111(45KPU)	1111(45KPU)	
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110(35KPD)	0110(35KPD)	0110(35KPD)	Need to Update
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1010(15KPU)	0000(5KPD)	1100(25KPU)	
STRAP3(Only GB2B)	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED		0010(15KPD)		
STRAP4(Only GB2B)	Reserve	Reserve	PCIE_MAX_SPEED	DP_PLL_VDD33V		0001(10KPD)		Need to Update

VRAM Configuration Table

RAMCF3 (3-D)	DESCRIPTION	Vendor	Vendor P/N	ROM_S1	
D20 0000					
D21 0001					
D22 0010	DDR3 64Mx16x8, 128bit, 1GB	Hynix	H5TQ1G63D3FR-12C(800MHz) / H5TQ1G63D3FR-11C(900MHz)		PD 15K
D23 0011	DDR3 64Mx16x8, 128bit, 1GB	Samsung	K4W1G1646E-HC12(800MHz) / K4W1G1646E-HC11(900MHz)		PD 20K
D24 0101					
D25 0110					
D26 0111	DDR3 128Mx16x8, 128bit, 2GB	Hynix	H5TQ2G63BFR-12C(800MHz) / H5TQ2G63BFR-11C(900MHz)		PD 35K
D27 0111	DDR3 128Mx16x8, 128bit, 2GB	Samsung	K4W2G1646C-HC11(800MHz)2 / K4W2G1646C-HC11(900MHz)		PD 45K

N12M-GE(QS)
Device Id=0x0A7A
STRAP2 =15K PU
ROM_SCLK=15K PU

N12P-GV(QS)
Device Id=-x1050
STRAP2 =5K PD
ROM_SCLK=10K PU

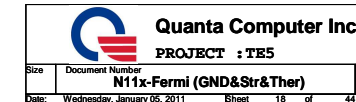
N12P-LP(QS)
Device Id=0x0DEC
STRAP2=25K PU
ROM SCLK=15K PD

GPIO ASSIGNMENTS

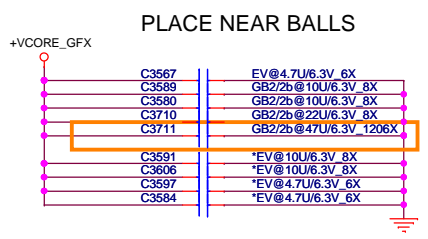
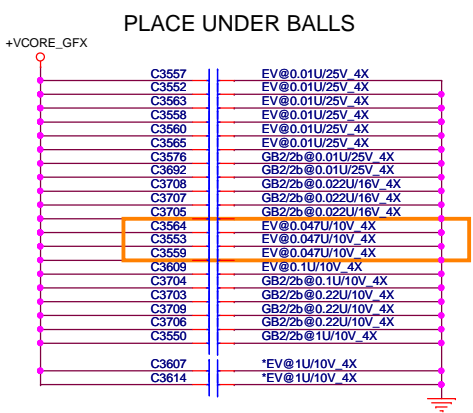
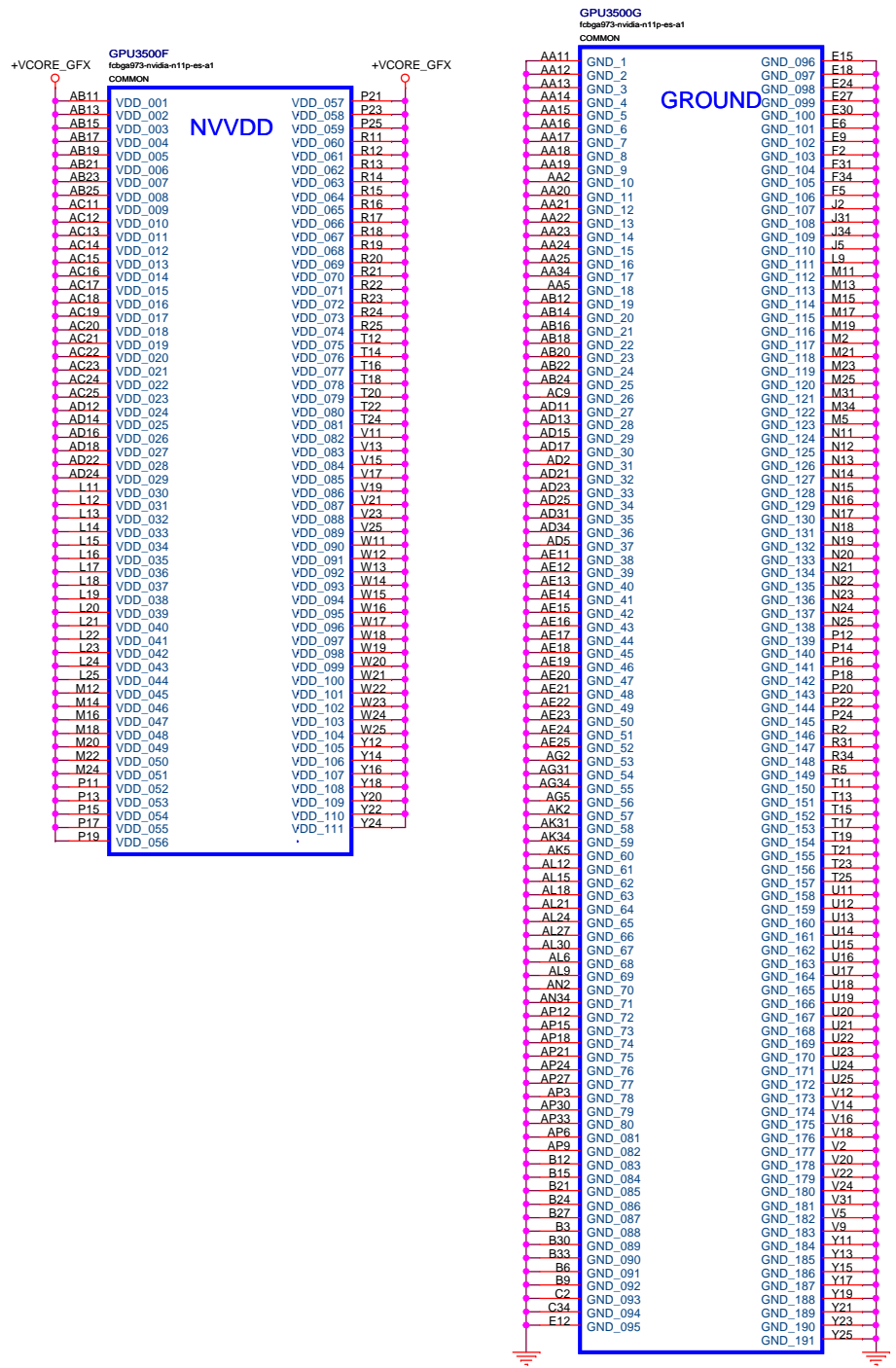
GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

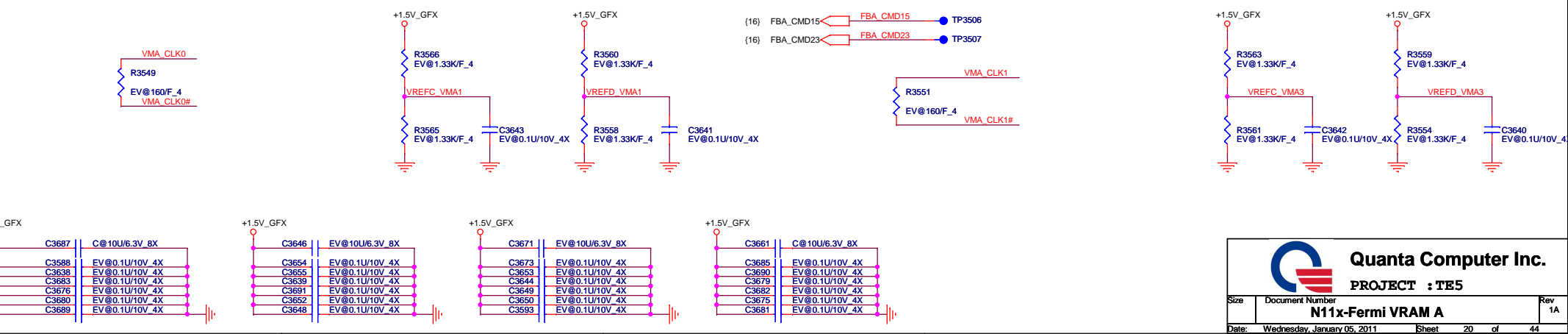
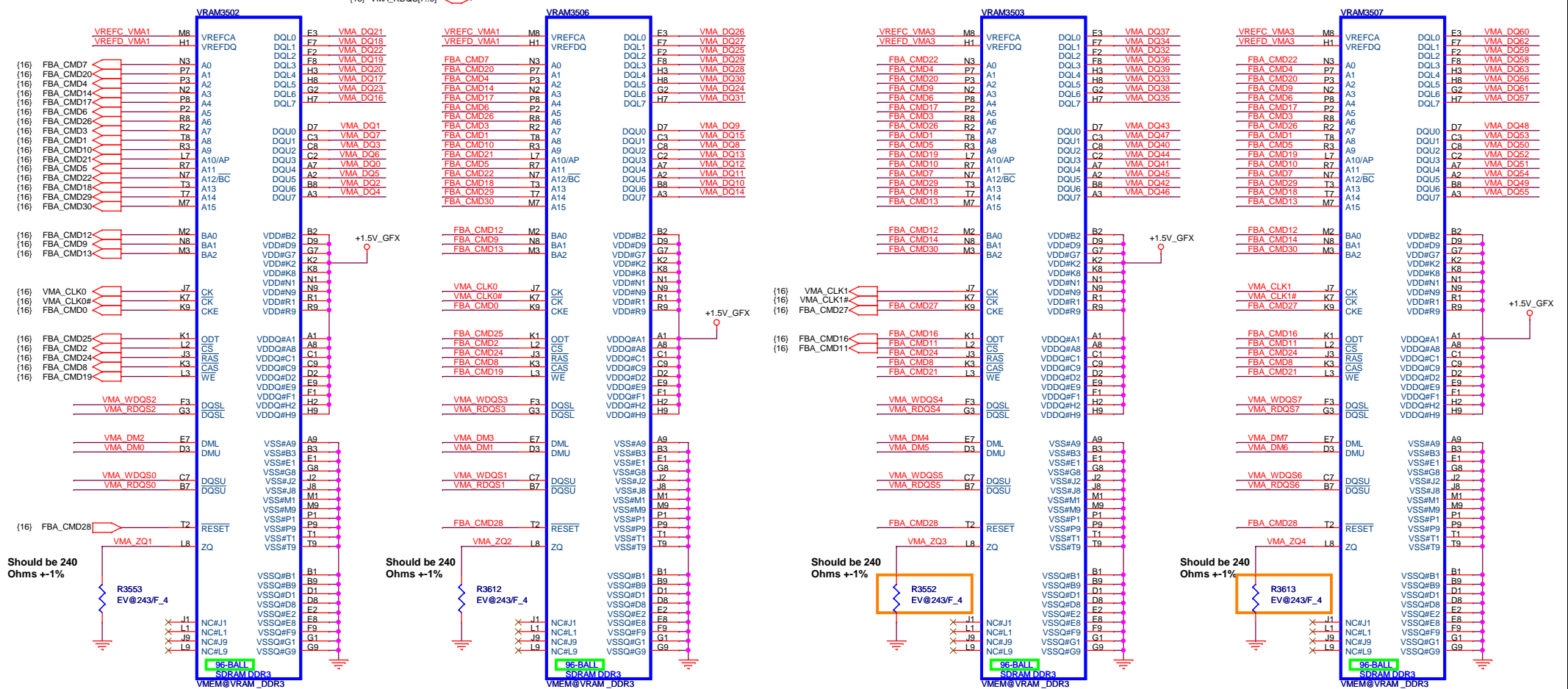


19-V



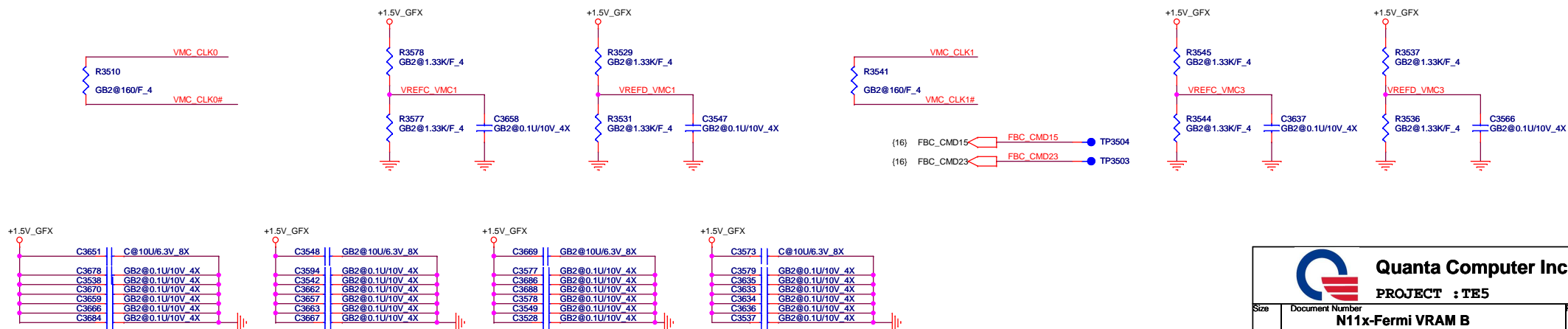
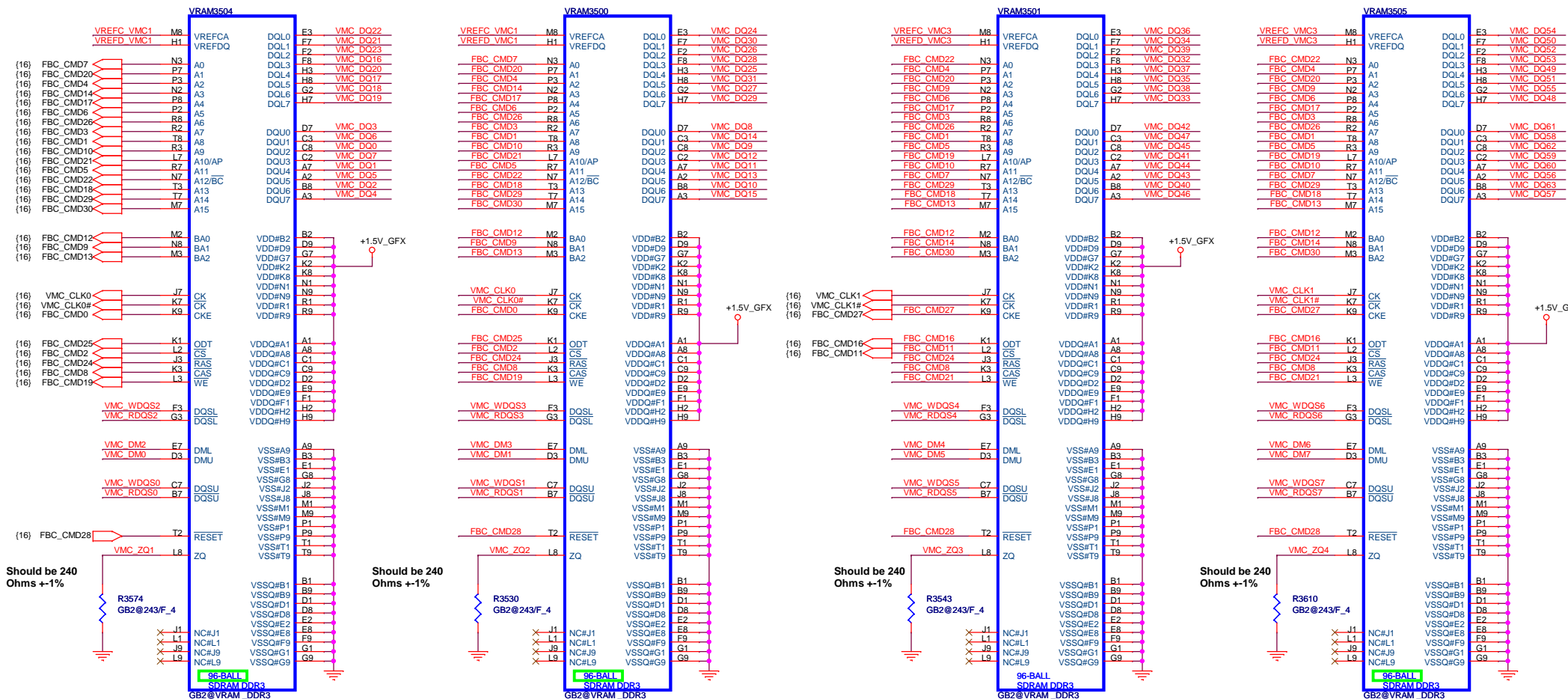
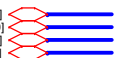
CHANNEL A: 256MB/512MB DDR3

(16) VMA_DQ[63..0]
(16) VMA_DM[7..0]
(16) VMA_WDQS[7..0]
(16) VMA_RDQS[7..0]

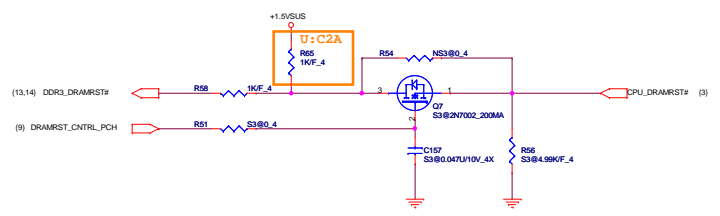


CHANNEL B: 256MB/512MB DDR3

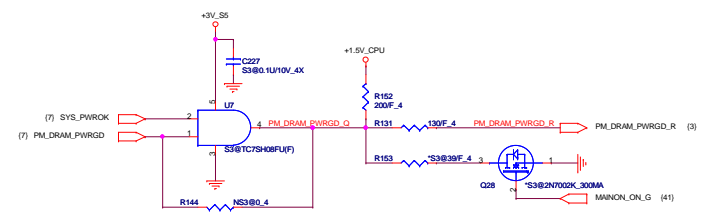
```
{16} VMC_DQ[63..0]
{16} VMC_DM[7..0]
{16} VMC_WDQS[7..0]
{16} VMC_RDQS[7..0]
```



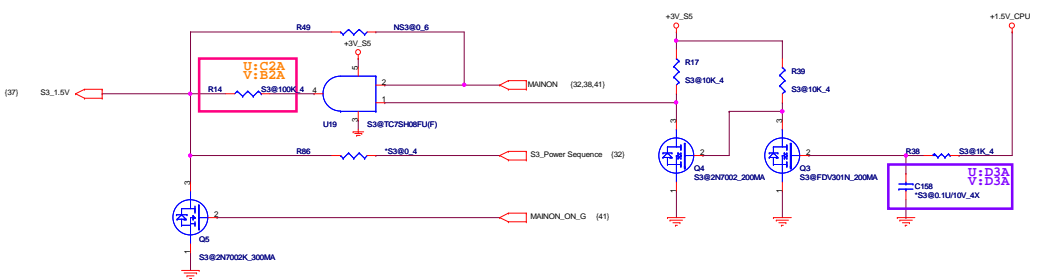
S3 power Reduction (SM_DRAMRST#) <S3P> <4>



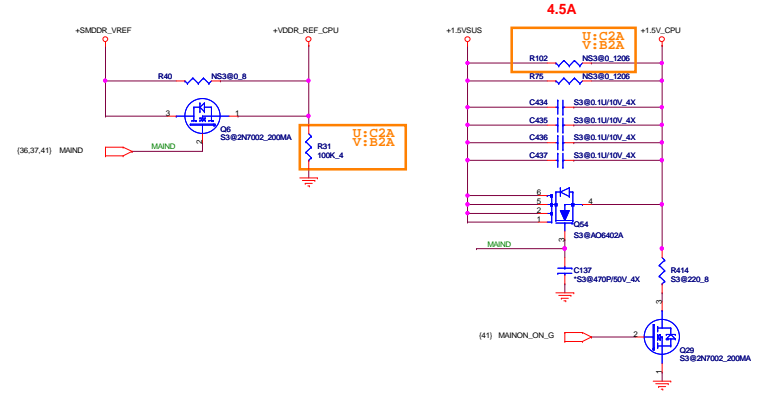
S3 power Reduction (SM_DRAMPWRK) <S3P> <3>



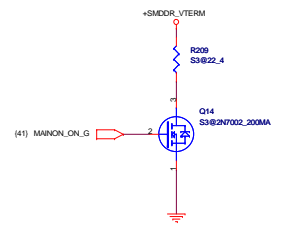
For S3 power Reduction Sequence <S3P> <3>



S3 power Reduction (CPU Power) <S3P> <5>

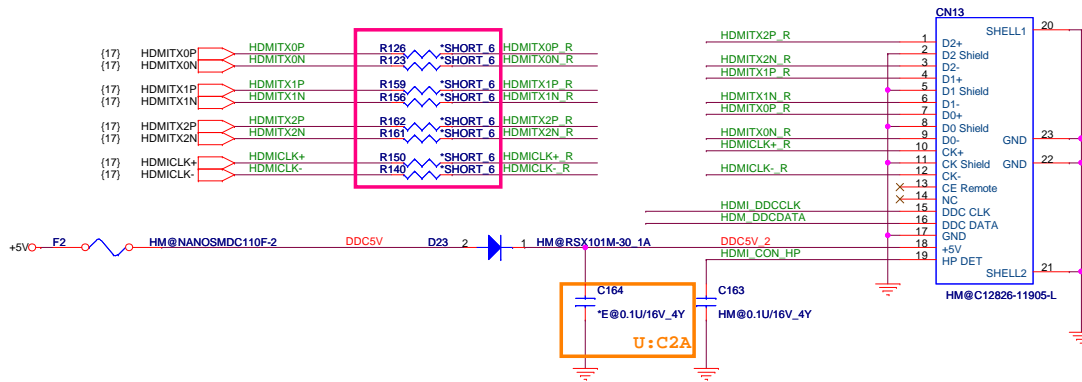


For S3 power Reduction VTT discharge <S3P> <13>

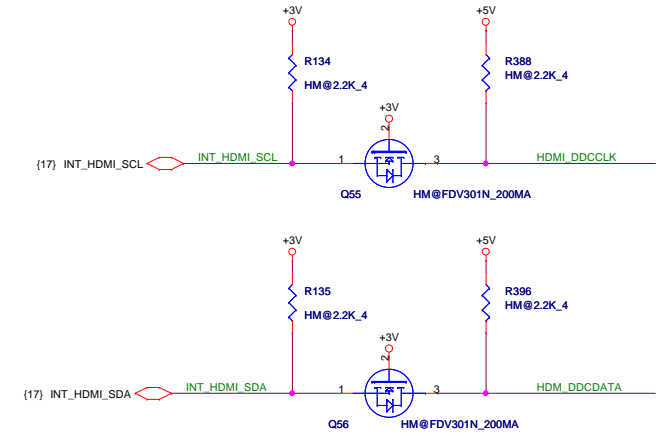


HDMI Conn [HDM]

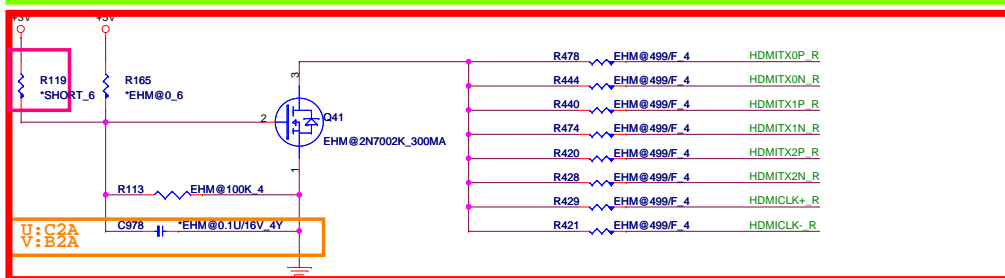
HDMI-CONN <HDM>



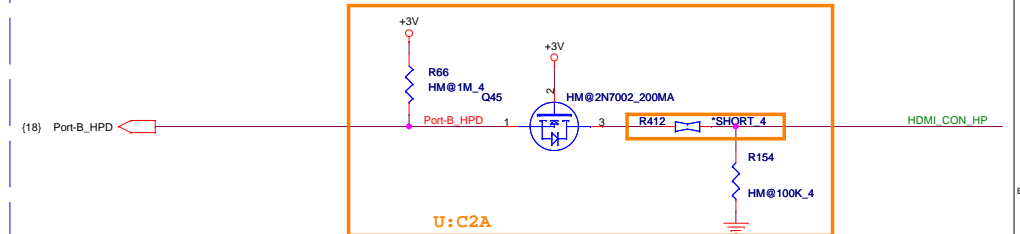
HDMI-SMBus <HDM>

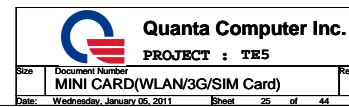


HDMI-passive level shift <HMP/HMG>

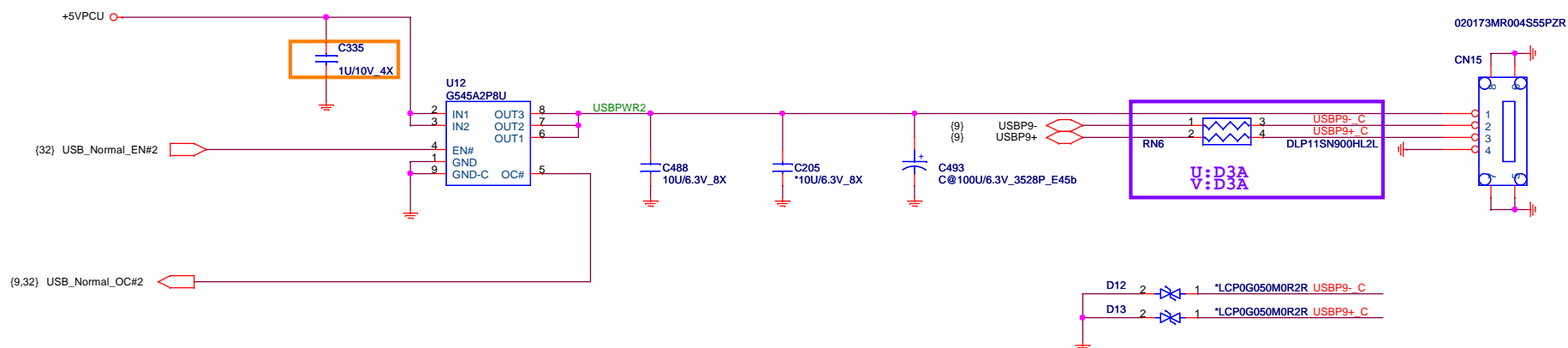


HDMI-HPD <HMP/HMG>

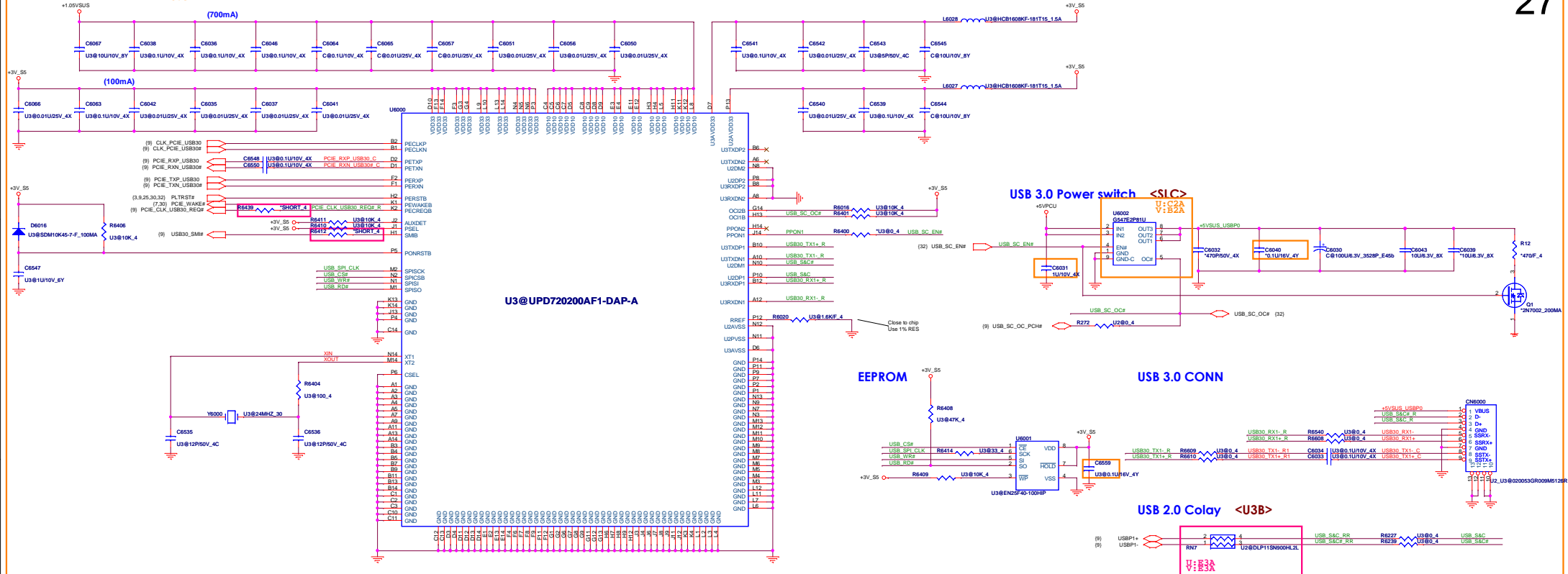




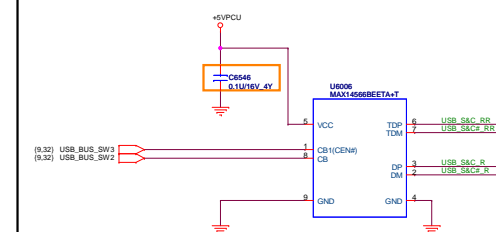
USB2.0 MB SIDE (Left) <USB>



U:C2A



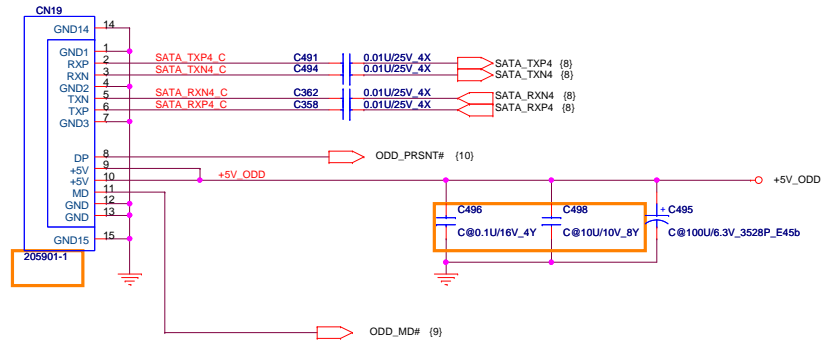
USB w S&C MAXIM solution <SLC>



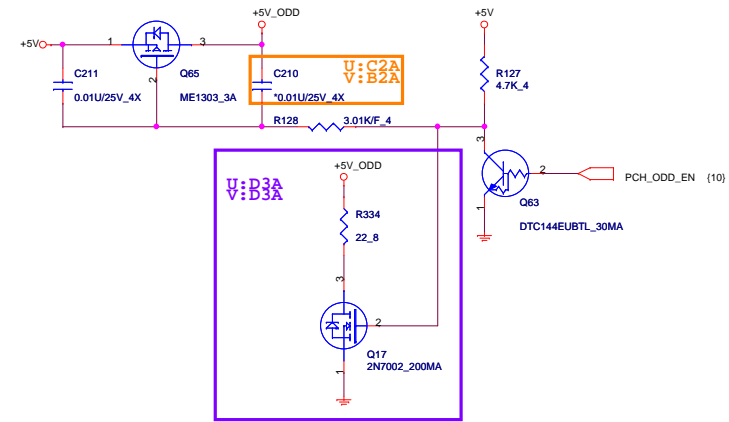
CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

SATA ODD

[ODD]



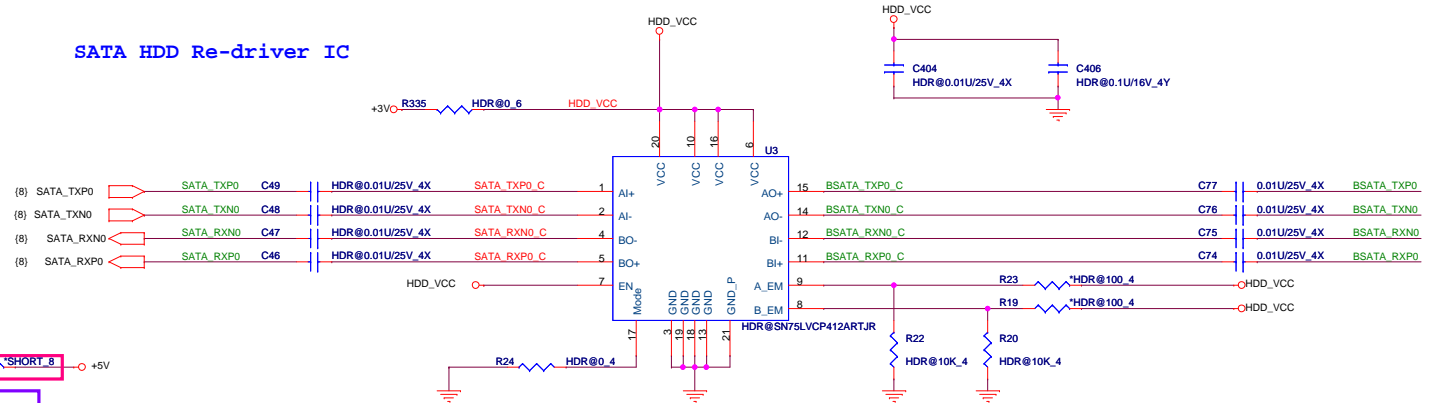
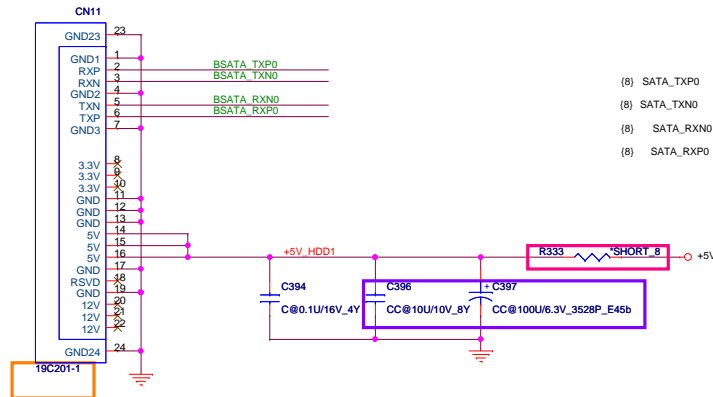
ODD Zero power . (Only for Intel) <OZP>



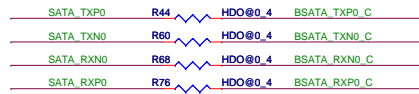
SATA HDD

[HDD]

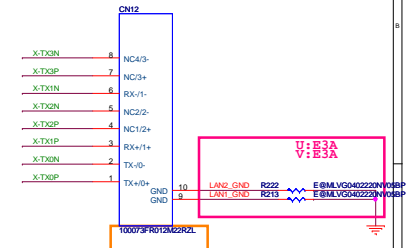
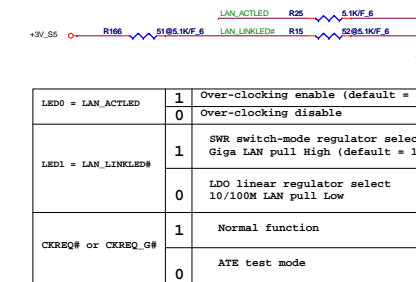
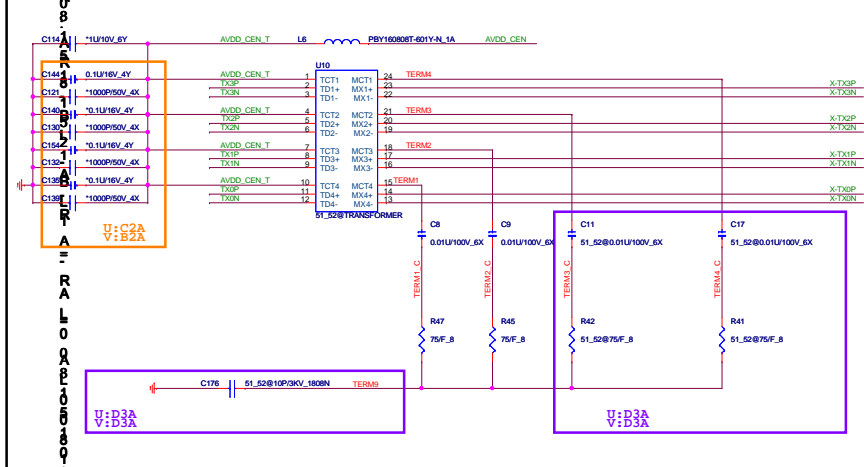
SATA HDD Re-driver IC



Colay with Redriver IC

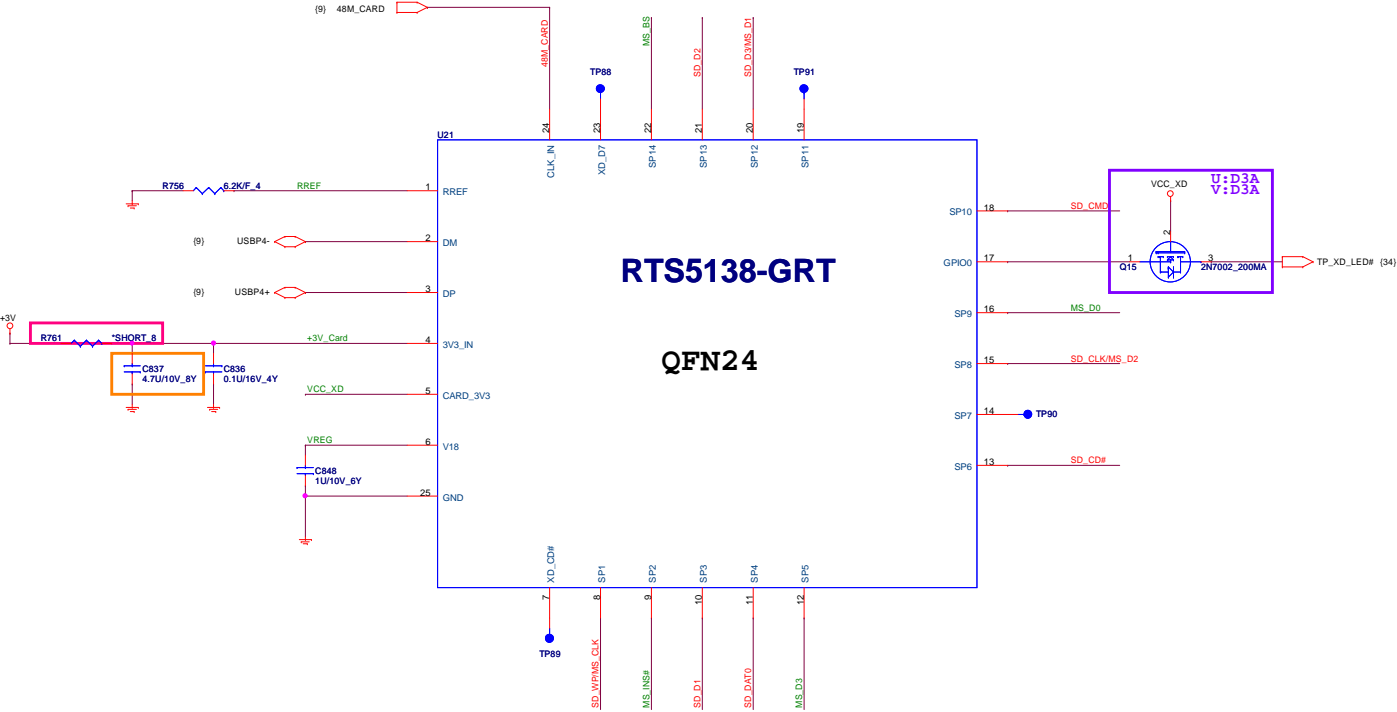


SATA Re-driver Bypass



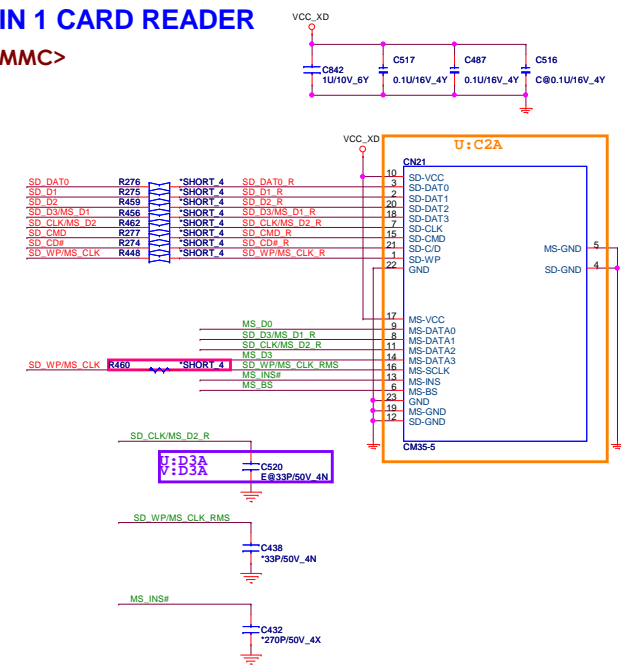
3 IN 1 CARD READER

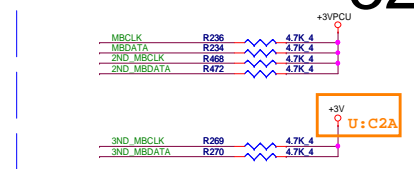
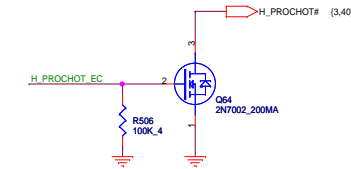
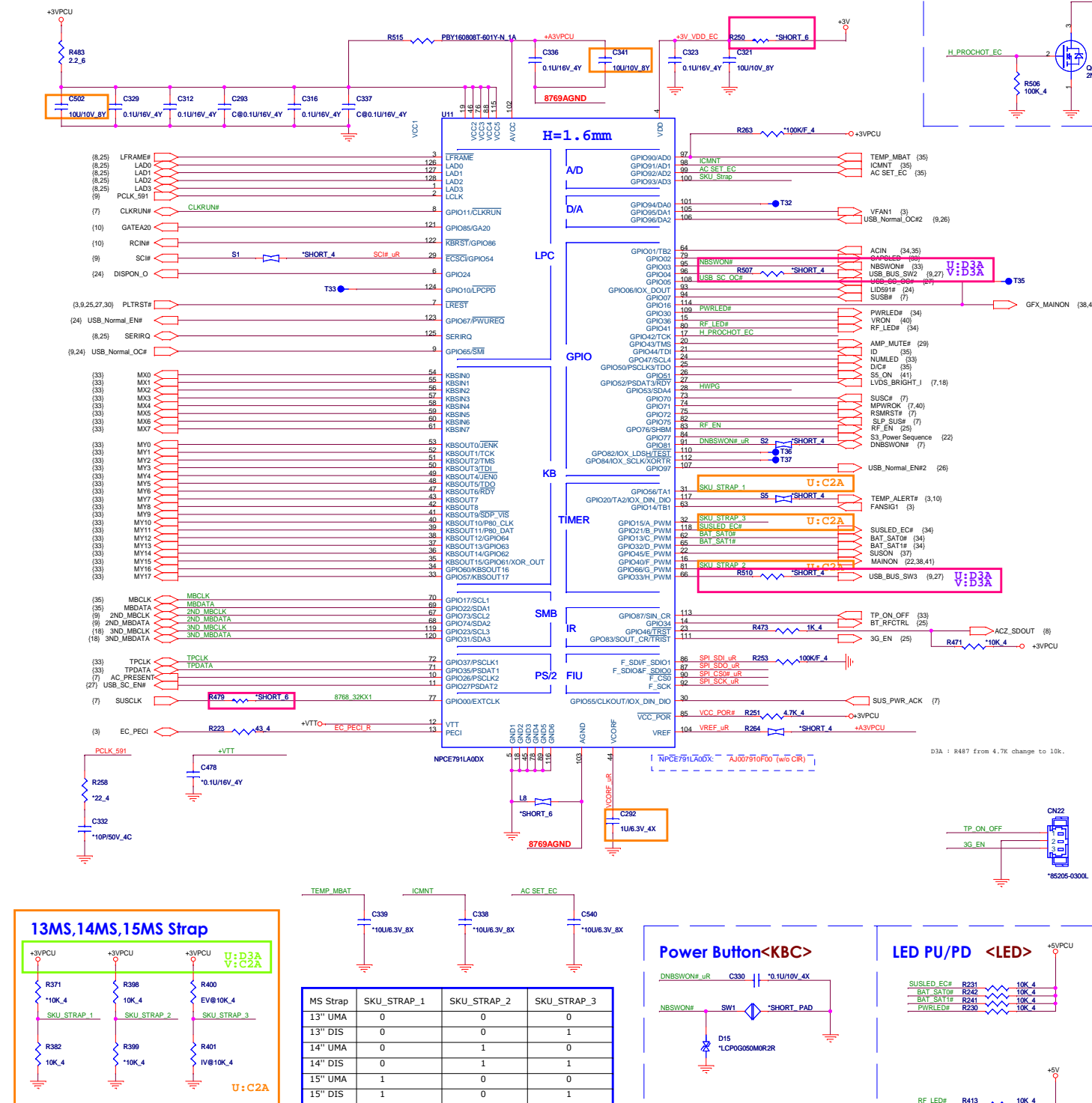
Card reader controller <MMC>



3 IN 1 CARD READER

<MMC>





3Cell Battery protect & K/B LED Control <KBC>

TP <KBC>

Strap <KBC>

ID EEPROM <KBC>

SPI FLASH <KBC>

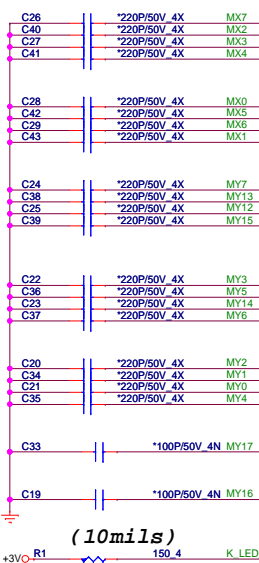
INTERNAL KEYBOARD STRIP SET <KBC>

HWPG circuit <KBC>

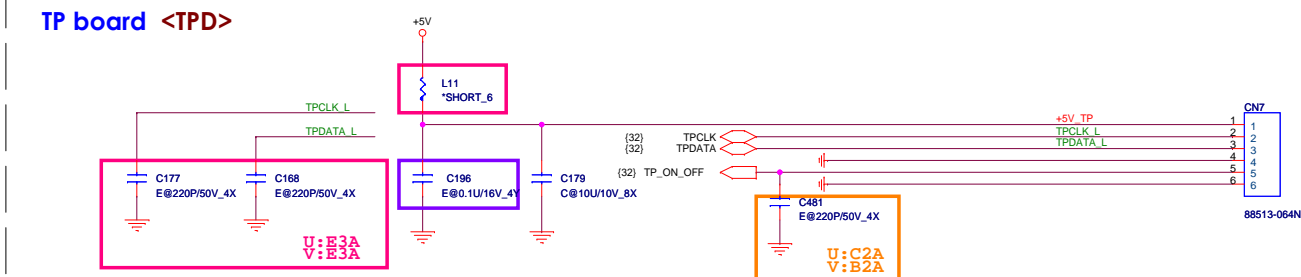
Power Button <KBC>

LED PU/PD <LED>

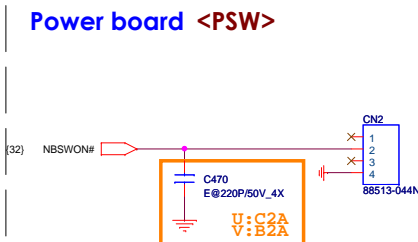
INT KeyBoard <KBC>



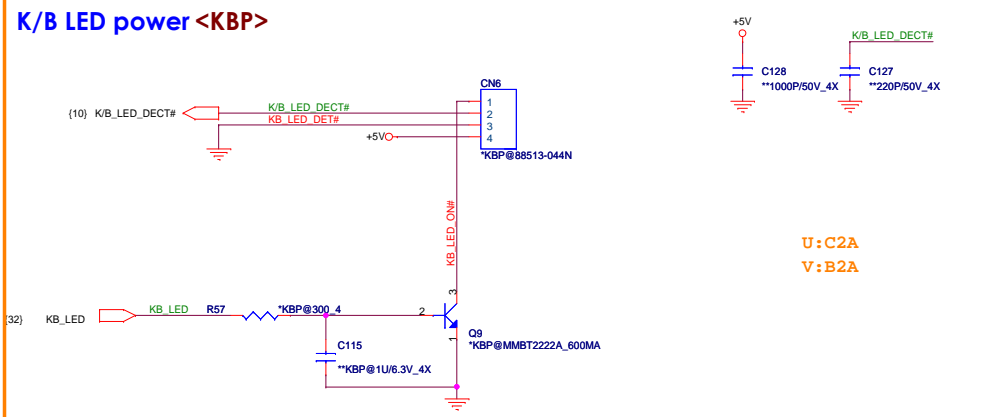
TP board <TPD>



Power board <PSW>

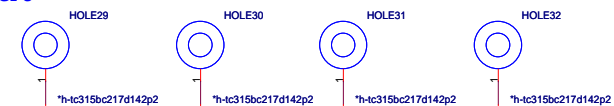


K/B LED power <KBP>



HOLE

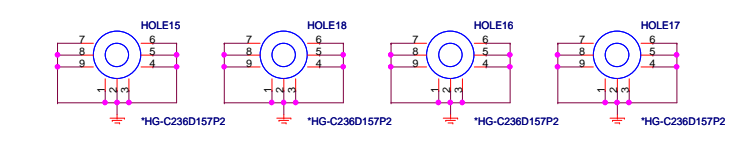
CPU



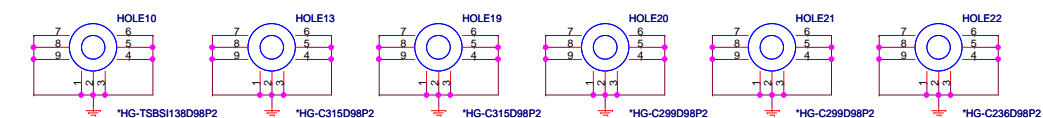
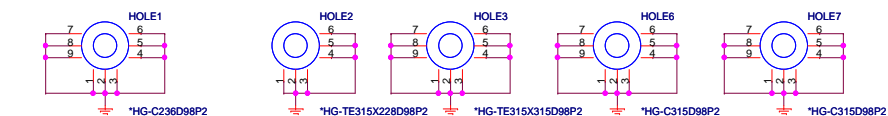
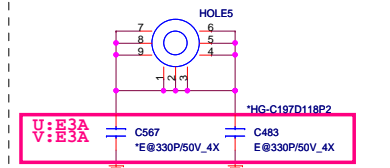
HDD&ODD



MINI CARD

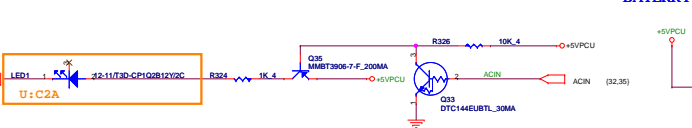


MDC

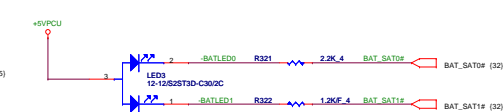


LED <LED>

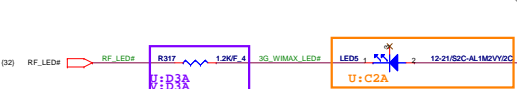
AC-IN



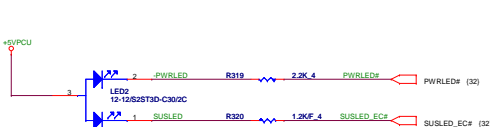
BATTERY



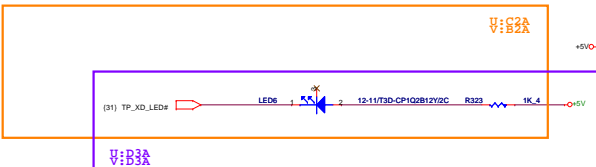
RF LED



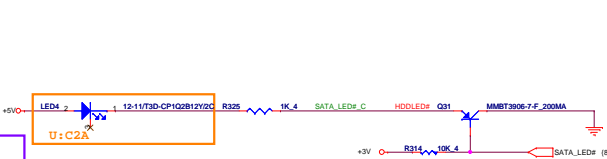
POWER



CARDREADER



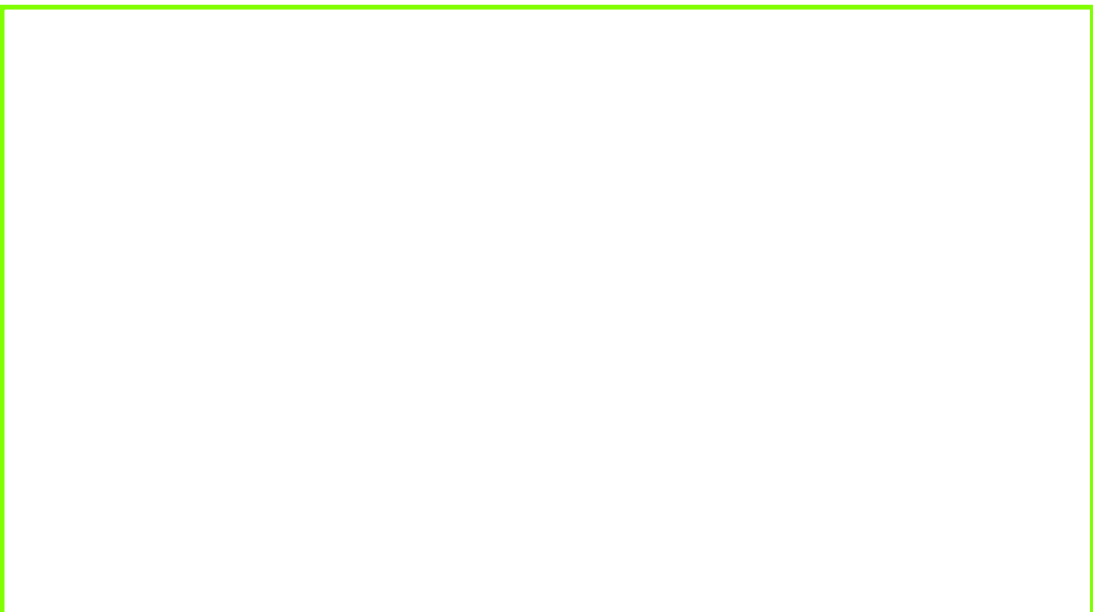
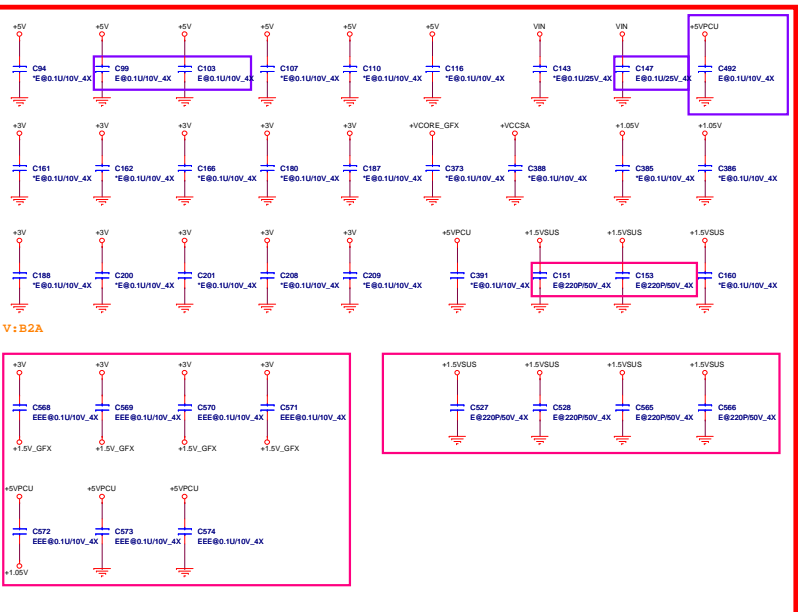
HDD/ODD



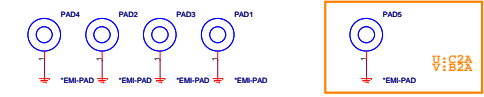
ESD Protect



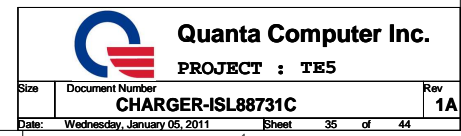
EMI

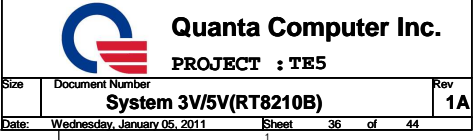


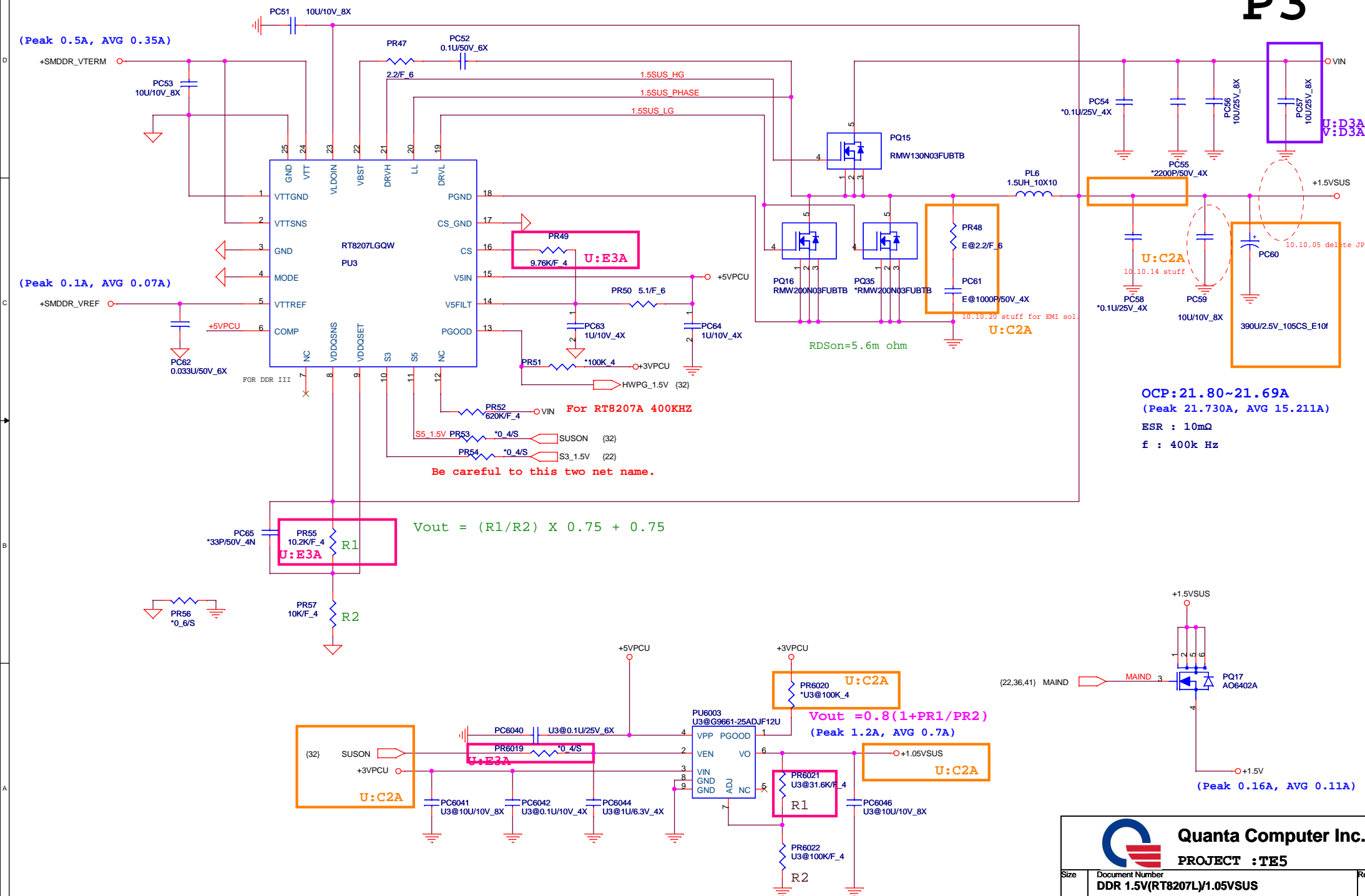
EMI PAD



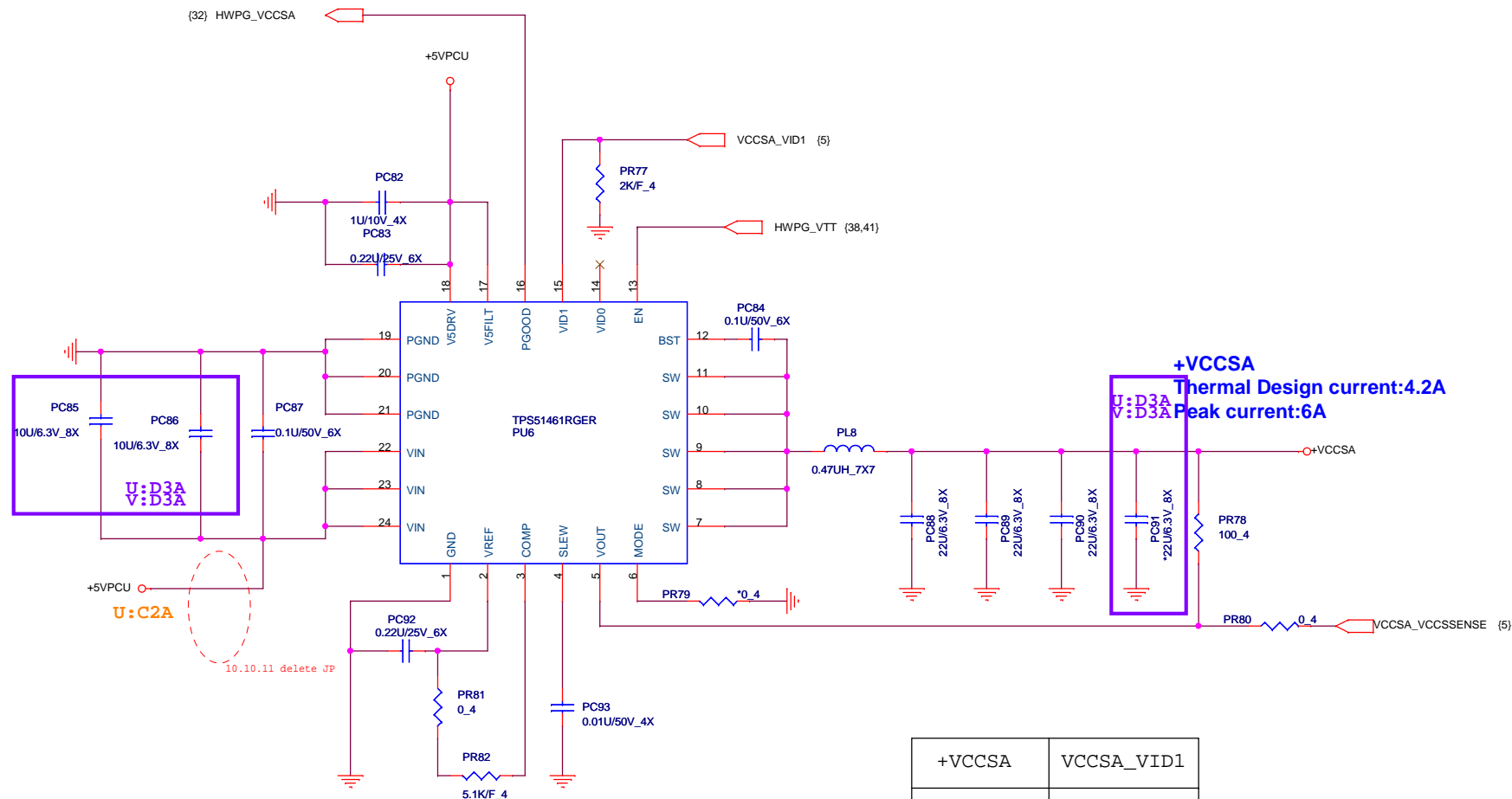
1.



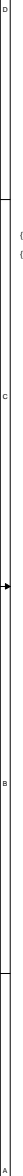


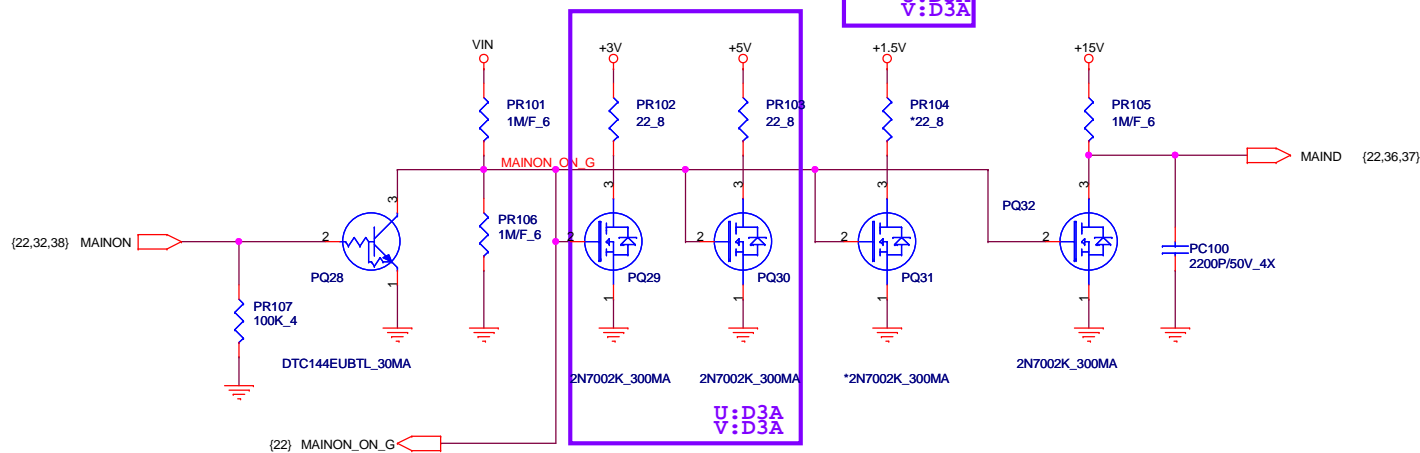
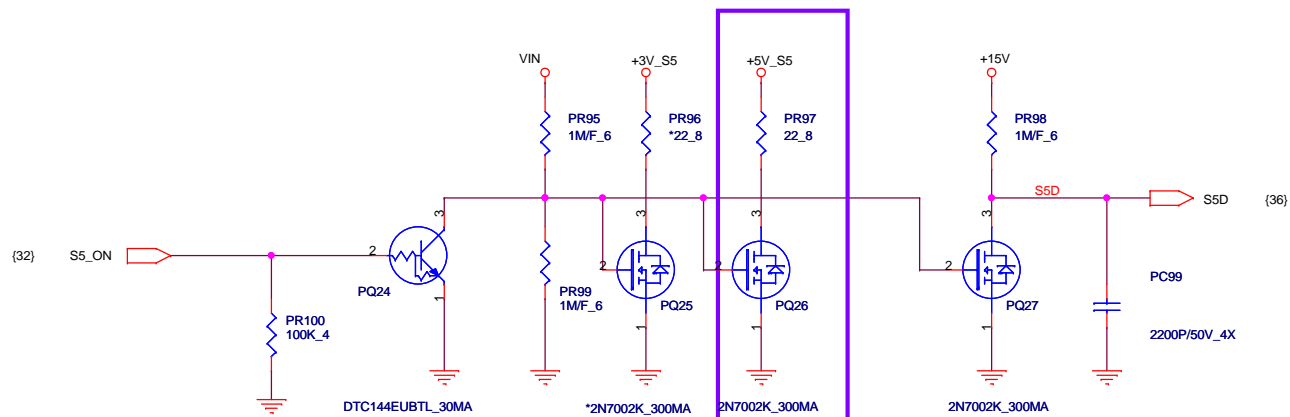
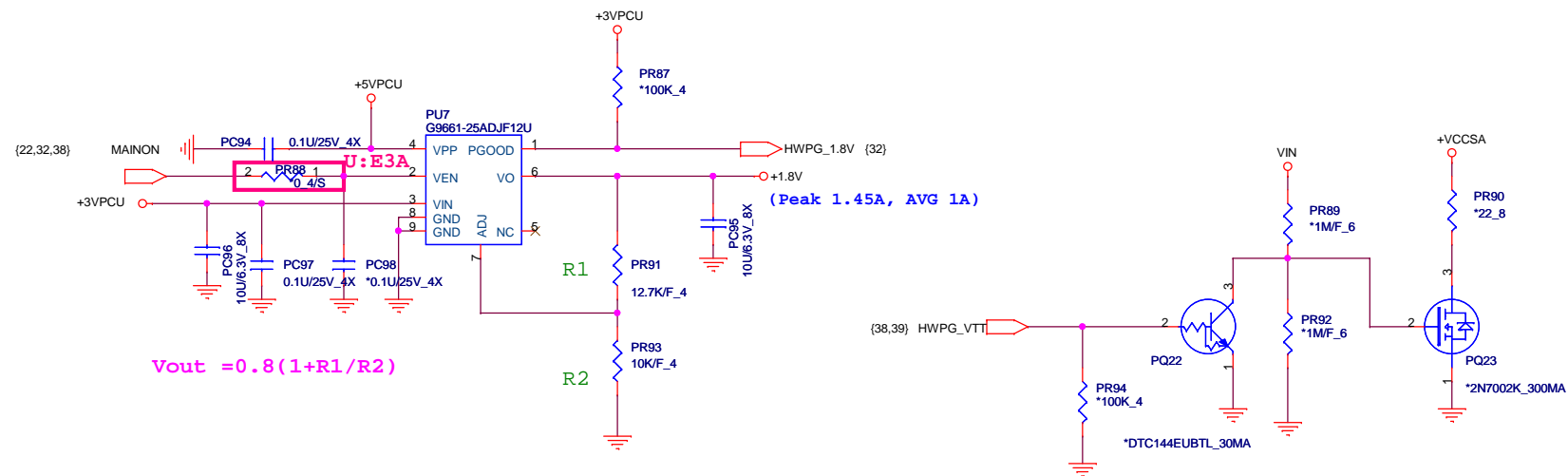






+VCCSA	VCCSA_VID1
0.8V	High
0.9V	Low





OCP: 25A
(Peak 21A)
Total capacitor: 660 uF
ESR: 4.5mΩ
f: 300K Hz

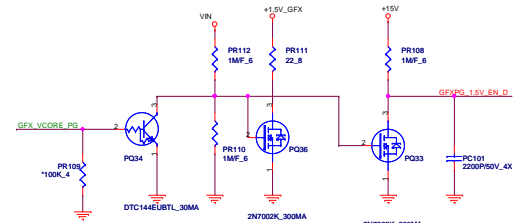
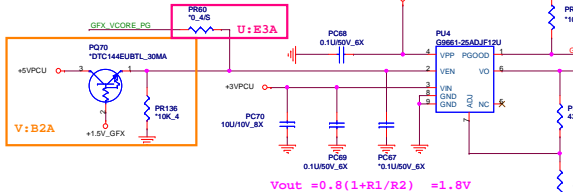
Need to consider DOS mode

Default	N12M-GE	N12P-LP	N12P-GV
PR131 R5 NC	10K CS31002JB28	10K CS31002JB28	NC
PR113 R6 10K CS31002JB28	NC	NC	NC
PR121 R7 10K CS31002JB28	NC	10K CS31002JB28	NC
PR134 R8 NC	10K CS31002JB28	NC	NC

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	N12M-GE	N12P-LP	N12P-GV
LOW	LOW	1.0V	0.925V	1.025V
LOW	HIGH	1.0V	0.90V Default	1.0V
HIGH	LOW	1.0V Default	0.9V	1.0V
HIGH	HIGH	0.85V	0.825V	0.85V Default

	N12M-GE	N12P-LP	N12P-GV
R1 PR117	47.5K/F_4 CS34752PB14	22.6K/F_4 CS32262PB15	34.8K/F_4 CS33482PB22
R2 PR124	0.4 CS00002JB38	0.4 CS00002JB38	0.4 CS00002JB38
R3 PR119	270K/F_4 CS42702JB10	243K/F_4 CS42432PB02	200K/F_4 CS42002PB12
R4 PR114	1M/F_4 CS51002PB11	750K/F_4 CS47502PB14	1M/F_4 CS51002PB11
R5 PR118,PR123	2.32K/F_4 CS22322PB01	2.10K/F_4 CS22102PB12	2.32K/F_4 CS22322PB01
R6 PR128,PR129	3.3K/F_4 CS23302PB12	3.24K/F_4 CS23242PB17	3.3K/F_4 CS23302PB12

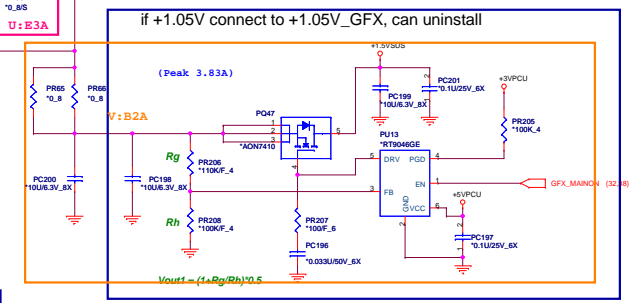
VEN need more than 1.6V



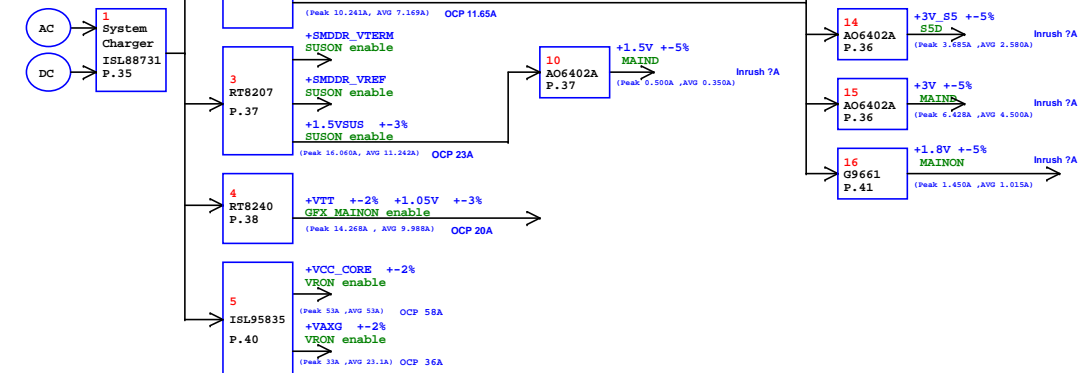
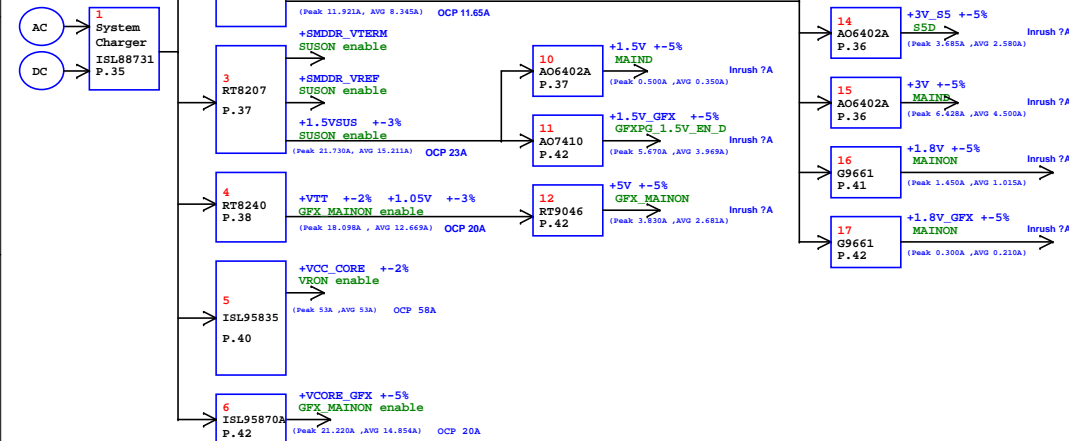
+3VPCU change to +3V
+5VPCU change to +5V


- Power On Sequence
- +3V_GFX connect +3V
 - +1.05V_GFX connect +1.05V
 - GFX_Mainon Enable +VCORE_GFX
 - GFX_VCORE_PG Enable(Delay) +1.5V_GFX
 - +1.5V_GFX Enable +1.8V_GFX
 - GFX_V18_PG connect GFX_PG

Power Off Sequence
compare +VCC3_GFX with +V1.8_GFX



if +1.05V connect to +1.05V_GFX, can uninstall

[illegible]

Model	REV	CHANGE LIST	MODEL			TE5		
			PAGE	FROM	To			
TE5 MB	1A	PAGE 3: (UMA)--R52 change to 25.5/F_4	1	1A				
		PAGE 5: (UMA)--C183,C190,C195 change to 10U/6.3V_8X	2	1A				
		PAGE 7: (UMA)--R224,R197 change to NC	3	1A				
		PAGE 9: (UMA)--PCIE_CLK_USB30_REQ#, R138 pull up to +3V_S5	4	1A				
		PAGE 9: (UMA)--PCIE_CLK_MINI_REQ#, R237 pull up to +3V	5	1A				
		PAGE 9: (UMA)--R199 NC	6	1A				
		PAGE 9: (UMA)--Q30, Q62 NC	7	1A				
		PAGE 10: (UMA)--add TP31	8	1A				
		PAGE 10: (UMA)--change Board ID9 strap Function name	9	1A				
		PAGE 11: (UMA)--C252 change to 10U/6.3V_8X	10	1A				
		PAGE 11: (UMA)--Net +1.05V change to +VTT	11	1A				
		PAGE 11: (UMA)--R117,R182,R114 change to 10K_4	12	1A				
		PAGE 12: (UMA)--R190,R194,R110 change to 10K_4	13	1A				
		PAGE 23: (UMA)--C978 NC	14	1A				
		PAGE 23: (UMA)--R66,R412,R154,Q45 change Function code to HM@ and delete discrete HDMI-HPD reference	15	1A				
		PAGE 24: (UMA)--add D7	16	1A				
		PAGE 25: (UMA)--add R201,R7,Q10	17	1A				
		PAGE 27: (UMA)--USB3.0 change to NEC solution	18	1A				
		PAGE 30: (UMA)--C97,C92,C106 change to 1U/10V_6Y	19	1A				
		PAGE 31: (UMA)--CN21 Foot-print change to 3in1-cm35-5-21p	20	1A				
		PAGE 32: (UMA)--3ND_MBCLK,3ND_MBDATA R269,R270 pull up to +3V	21	1A				
		PAGE 32: (UMA)--add 13MS,14MS,15MS Strap pin SKU_STRAP_1,SKU_STRAP_2,SKU_STRAP_3	22	1A				
		PAGE 33: (UMA)--add PR1	23	1A				
		PAGE 34: (UMA)--LED1,LED4,LED5,LED6 change symbol and Foot-print	24	1A				
		PAGE 16: (VGA)--add R3712	25	1A				
		PAGE 19: (VGA)--R3711 change to 47U/6.3V_1206X	26	1A				
		PAGE 25: (ALL)--Net name PCIE_CLK_3G_REQ# change to PCIE_CLK_3G_REQ#_C	27	1A				
		PAGE 22: (ALL)--add R65	28	1A				
		PAGE 37: (ALL)--PC60 change to CC7390JM202	29	1A				
		PAGE 18: (VGA)--add R3601, R3575	30	1A				
	PAGE 24: (UMA)--CN4 Value change to 87213-2000G							
	PAGE 22: (ALL)--add R102							
	PAGE 33: (ALL)--Remove K/B LED power circuit							
2A	PAGE 15: (VGA)--delete R3535,R3547							
	PAGE 22: (ALL)--add R31							
	PAGE 22: (ALL)--add R102							
	PAGE 40: (ALL)--add PC168							
	PAGE 32: (ALL)--13MS,14MS,15MS Strap pull up voltage change to +3VPCU							
	PAGE 34: (ALL)--add R213							
	PAGE 42: (VGA)--add PQ49							
DOC NO. 204		PROJECT MODEL :	TE5	APPROVED BY:	Andy Wang	DATE:	2010/10/01	 Quanta Computer Inc. PROJECT : TE5 Change list Date: Wednesday, January 05, 2011 Sheet 31 of 35
		PART NUMBER:		DRAWING BY:	Andy Wang	REVISION:	1A	

Model		REV	CHANGE LIST				MODEL			TE5	
							PAGE	FROM	To		
TE5 MB	1A	PAGE 35: (COM)--add PC76 and PC77 for EMI Sol. (101005)					1	1A			
		PAGE 35-42: (COM)--delete PJP1 , PJP2 , PJP3 , PJP14 , PJP6 , PJP9 (101005)					2	1A			
		PAGE 38: (COM)--PC212 change to 0.1U/25V_6X (101005)					3	1A			
		PAGE 38: (COM)--PC216 change to 1.74K/F_4 (101005)					4	1A			
		PAGE 40: (COM)--PC153 and PC154 change to 330U/2V_7343P_E9C (101005)					5	1A			
		PAGE 36: (COM)--add PD12 , PR142 , PR139 (101011)					6	1A			
		PAGE 38: (COM)--Change VTT/1.05V solution (101011)					7	1A			
		PAGE 37: (COM)--PC59 stuff (101014)					8	1A			
		PAGE 38: (COM)--Change PQ18 and PQ19 Value (101014)					9	1A			
		PAGE 40: (COM)--Change PR184 Value ; PC151 stuff (101014)					10	1A			
		PAGE 42: (COM)--PC113 no stuff (101014)					11	1A			
		PAGE 35 , 37 , 38 , 40: (COM)--PR14 , PC19 , PR48 , PC61 , PR70 , PC80 , PR159 , PC157 , PR177 , PC171 , PR200 , PC195 stuff (101020)					12	1A			
		PAGE 36: (COM)--PU2 , PL4 , PL5 change Value (101020)					13	1A			
							14	1A			
							15	1A			
							16	1A			
							17	1A			
							18	1A			
							19	1A			
							20	1A			
							21	1A			
							22	1A			
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							24	1A			
							25	1A			
							26	1A			
							27	1A			
							28	1A			
							29	1A			
							30	1A			
DOC NO. 204		PROJECT MODEL :	TE5	APPROVED BY:	Andy Wang	DATE:	2010/10/01	<div><div><div></div></div><div>Quanta Computer Inc.</div><div>PROJECT : TE5</div><div>Change list</div><div>Date: Wednesday, January 05, 2011Sheet 31 of 35</div></div>			
		PART NUMBER:		DRAWING BY:	Andy Wang	REVISION:	1A				