

# Strike

AX01 Build

MS14  
2010.10.06

**INVENTEC**

TITLE  
**Strike**

SIZE Custom	CODE CS	DOC NUMBER CS-131	REV X01
SHEET 1		of 58	

CHANGE by IEC	DATE Thursday, October 07, 2010
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# 1. Schematic Page Description :

## MS14 Schematic Ver : X01

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12. PWR_5VA/SCREW/IO CNN	27. PCH_LVDS,CRT,HDMI	42. I/O CNN	57. PWR_SW CNN
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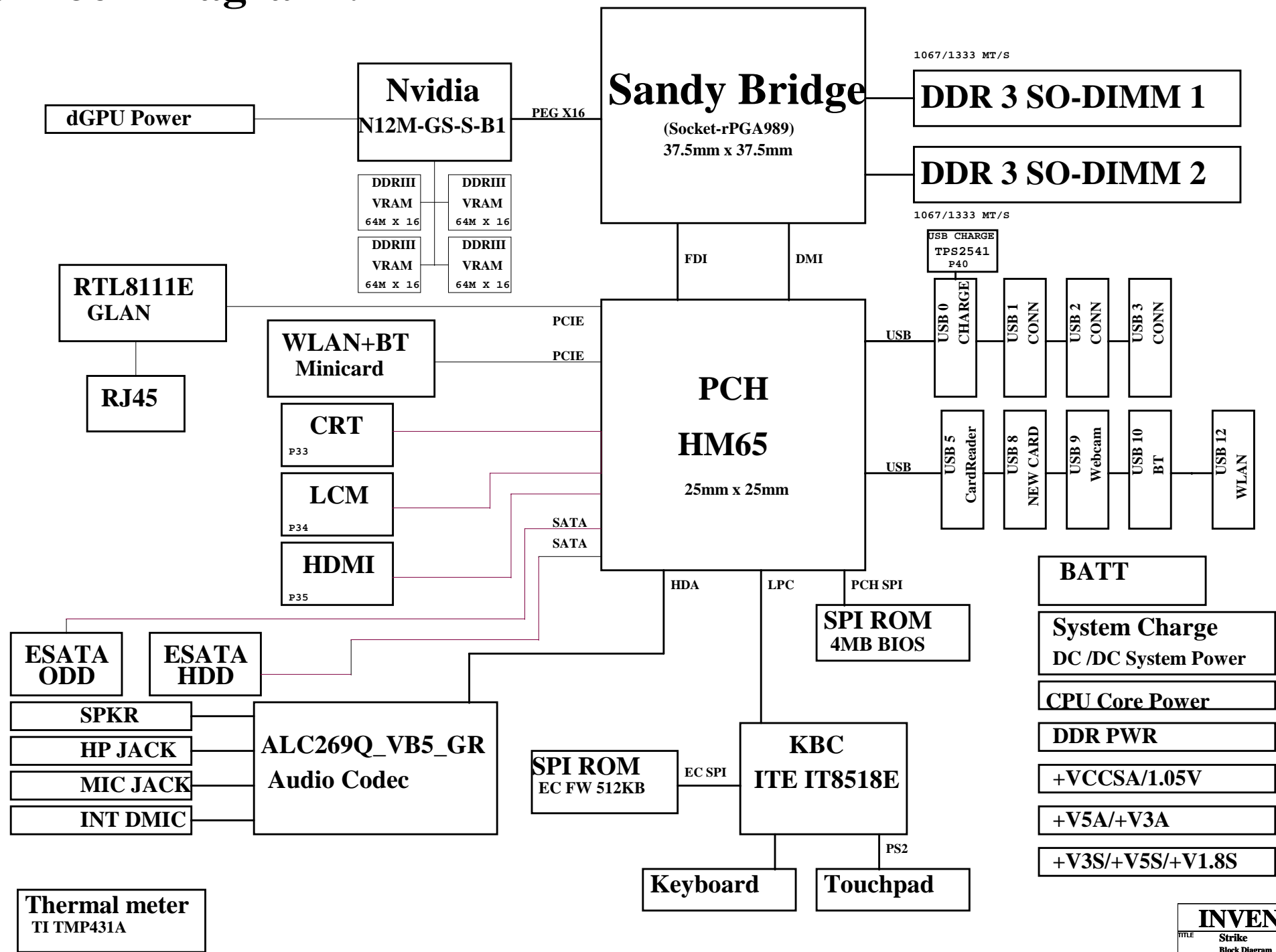
# 2. PCI & IRQ & DMA Description :

IDSEL	CHIP	PCIINT	CHIP	Interface	REQ	CHIP
None		None			None	

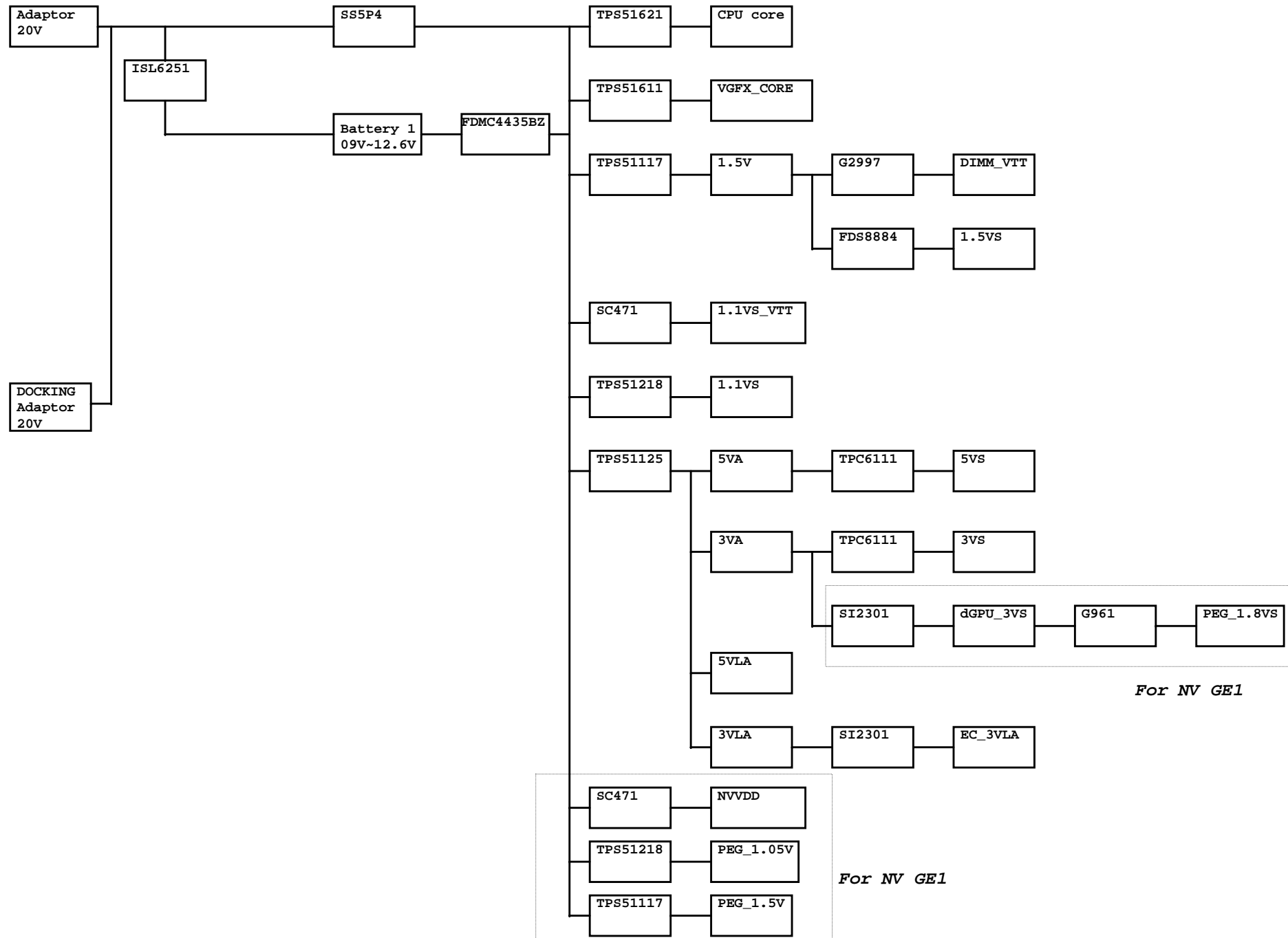
# 3. USB & PCI-Express & SATA Description :

USB Port	DEVICE	USB Port	DEVICE	PCI-E	DEVICE	SATA	DEVICE
Port 0	System (ESATA)	Port 7	Bluetooth	Port 1	New Card	Port 1	HDD
Port 1	System	Port 8		Port 2	Docking	Port 2	E-SATA
Port 2	System	Port 9	Web Cam	Port 3	Mini Card(WLAN)	Port 4	BAY
Port 3	System	Port 10		Port 4	Mini Card(3G)	Port 5	None
Port 4	CardReader	Port 11	FingerPrint	Port 5	Mini Card(ROBSON)		
Port 5		Port 12		Port 6	Giga-LAN		
Port 6		Port 13	3G				

### 3. Block Diagram :



### Power Block Diagram :



# 4. Net name Description :

## Voltage Rails

DCIN	Primary DC system power supply
3VLA	3.3V always on power rail by DCIN
5VLA	5.0V always on power rail by DCIN
EC_3VLA	3.3V always on power rail by 5VAUXON
3VA	3.3V always on power rail by LATCH_ON
5VA	5.0V always on power rail by LATCH_ON
3VM	3.3V power rail by SUSM#
1.05VM	1.05V switched power rail by SUSM#
1.5V	1.5V switched power rail by SUSC#
1.8V	1.8V power rail by SUSC#
3VS	3.3V power rail by SUSB#
5VS	5.0V power rail by SUSB#
1.5VS	1.5V power rail by SUSB#
1.05VS	1.05V power rail by SUSB#
PWR_DIMM_VTT	0.75V DDR Termination Voltage by SUSB#
VGFX_CORE	1.05V power rail for UMA by SUSB#
PEG_1.8VS	1.8V switched power rail for NB9x by SUSB#
PEG_PEX_1.1VS	1.1V switched power rail for NB9x by SUSB#
PEG_NVDD	Variable switched power rail for NB9x by SUSB#

Vcore\_CPU Core switched power rail for CPU

## Part Naming Conventions

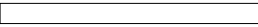







C = Capacitor	Q = Transistor
CN = Connector	R = Resistor
D = Diode	RP = Resistor Pack
F = Fuse	U = Arbitrary Logic Device
L = Inductor	Y = Crystal and Osc

## Name Suffix

# = Active Low signal
NU = No Stuff

# 5. Board Stack up Description

## PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Stripline Layer
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side, Microstrip signal Layer

	Differential Impedance for Microstrip(5-mils)	Differential Impedance for Stripline(4-mils)
Host Clock	95 ohm +/- 20%	100 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	100 ohm +/- 20%
DDR2 CLK	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	85 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	100 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	100 ohm +/- 20%
SDVO	95 ohm +/- 20%	100 ohm +/- 20%
SATA	95 ohm +/- 20%	100 ohm +/- 20%
USB	90 ohm +/- 20%	95 ohm +/- 20%
LVDS		100 ohm +/- 20%
Lan	95 ohm +/- 20%	100 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn HFM: LFM:	1.3319V-1.4375V-1.4591V 0.9221V-0.9625V-0.9739V	36A
1.05VS	Penryn: AGTL+ termination Cantiga GM: Core Cantiga GM: PCIE Cantiga GM:Core+IMEL+HSIO Cantiga GM:VCC_GMCH Cantiga GM:VCCA_SM_CK and NCTF Cantiga GM:VCC_DMI Cantiga GM:VCCA_SM Cantiga GM:VTT ICH9M:VCC1_05 ICH9M:DMI ICH9M:CPU_IO	1V-1.05V-1.10V 0.997V-1.05V-1.102V 0.9975V-1.05V-1.1025V 0.9975V-1.05V-1.1025V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V	4.5A 8.7A 1.78A 2.898A 10.154A 37.95mA 456mA 747.5mA 852mA 1.634A 48mA 2mA
1.5VS	Penryn PLL Cantiga GM: QDAC Cantiga GM: LVDS Cantiga GM: TVDAC Cantiga GM: Various PLLS analog supply Cantiga GM: VCC_SM_CK Cantiga GM: VCC_SM ICH9M:PCIE_ICH ICH9M:SATA_ICH ICH9M:VCC_GLAN Mini Card: Express Card:	1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.71V-1.8V-1.89V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V	130mA 0.5mA 60.31mA 35mA 485mA 149.5mA 3.1625A 646mA 1.342A 80mA 650mA
1.5V	Cantiga GM: DDRIII System Memory	1.425V-1.5V-1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIIIDDRIII Terminator:		0.7125V-0.75V-0.7875V	1.0A
3VS	Cantiga GM: HV CMOS Cantiga GM: VCCS_TV DAC ICH9M:VCC3_3 ICH9M:VCCGLAN3_3 Thermal Sensor: Mini Card: UMTS Express Card: CLK Generator: ICS9LPRS397BKLFT Mini Card: WirelessLan Bluetooth: Super I/O: IT8305E Azalia Codec: ALC262 Azalia MDC:	3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V	105.3mA 78mA 308mA 1mA 5mA 1.3A 500mA
1.8VS	DVI	3.0V-3.3V-3.6V	120mA
3VA	ICH9M: RTC ICH9M:VCCSUS3_3 ICH9M:VCCCL3_3 ICH9M:VCCLAN3_3 LCD: Lan:82567LM Azalia MDC: Flash ROM: BIOS	2V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 1.0V and 1.8V 3.0V-3.3V-3.6V	6uA 212mA 73mA 78mA 2A Each 1A
5VS	Cardreader: GL827 Azalia Codec: ALC262 HDD: SATA ODD: SATA Audio AMP: G1432 Inverter: WebCam	3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA Max: 1.5A ; R/W: 900mA ; STDBY: 45mA
5VA	USB: x 2 ports USB and ESATA	5VA 5VA	1.5A 2A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V-3.3V-3.6V	300mA

INVENTEC

FILE

Strike Annotations

SIZE Custom

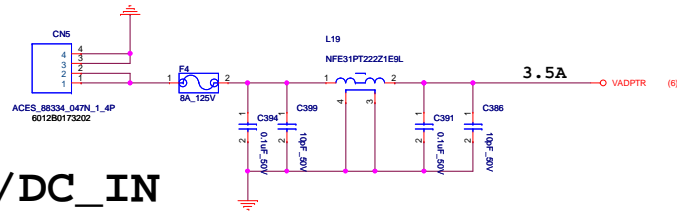
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DOC NUMBER CS-131

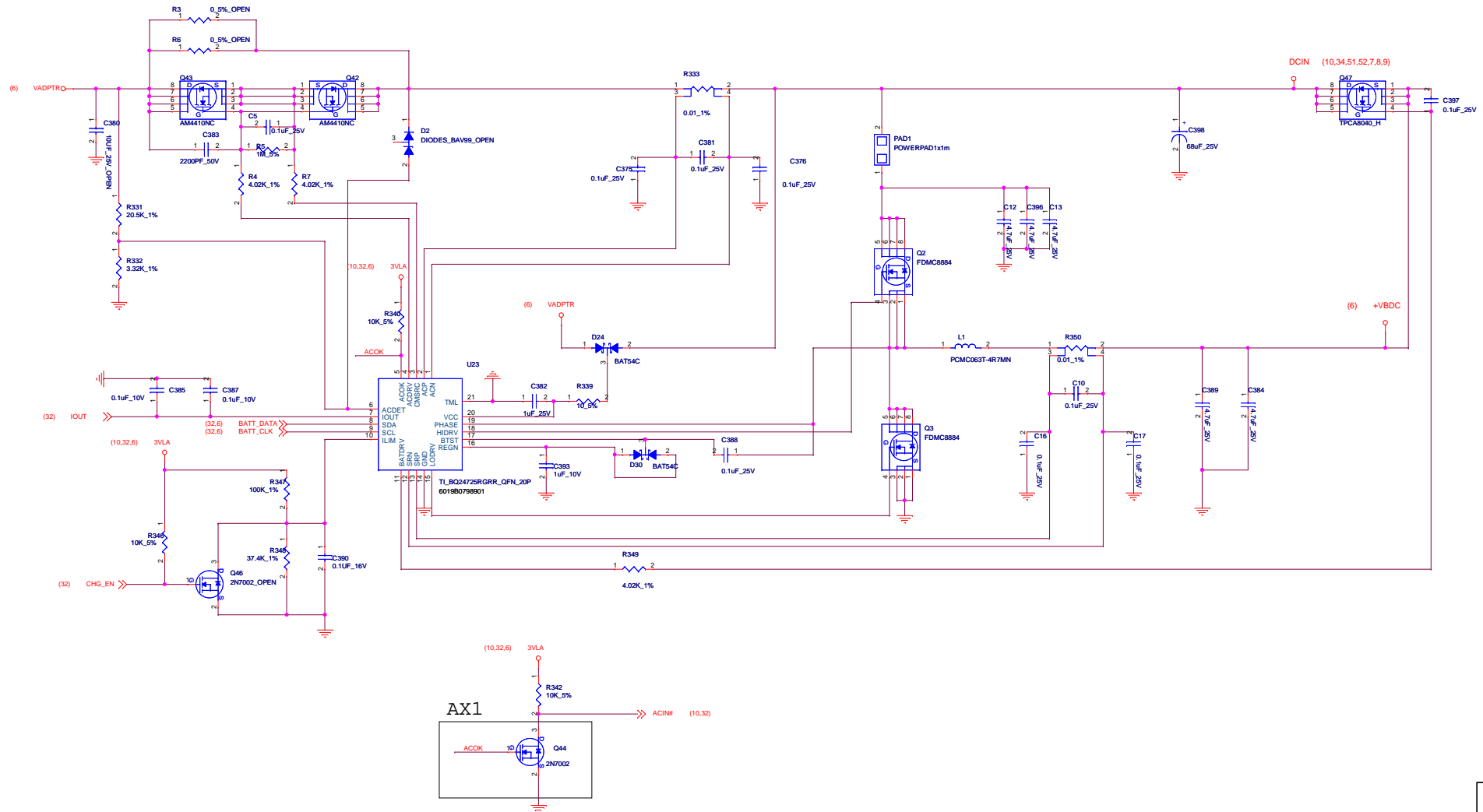
REV X01

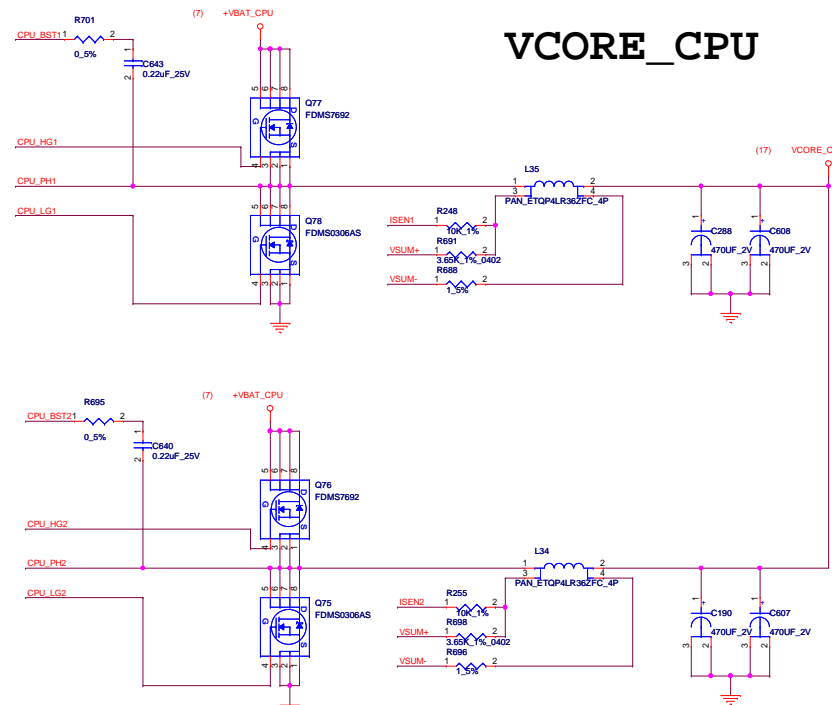
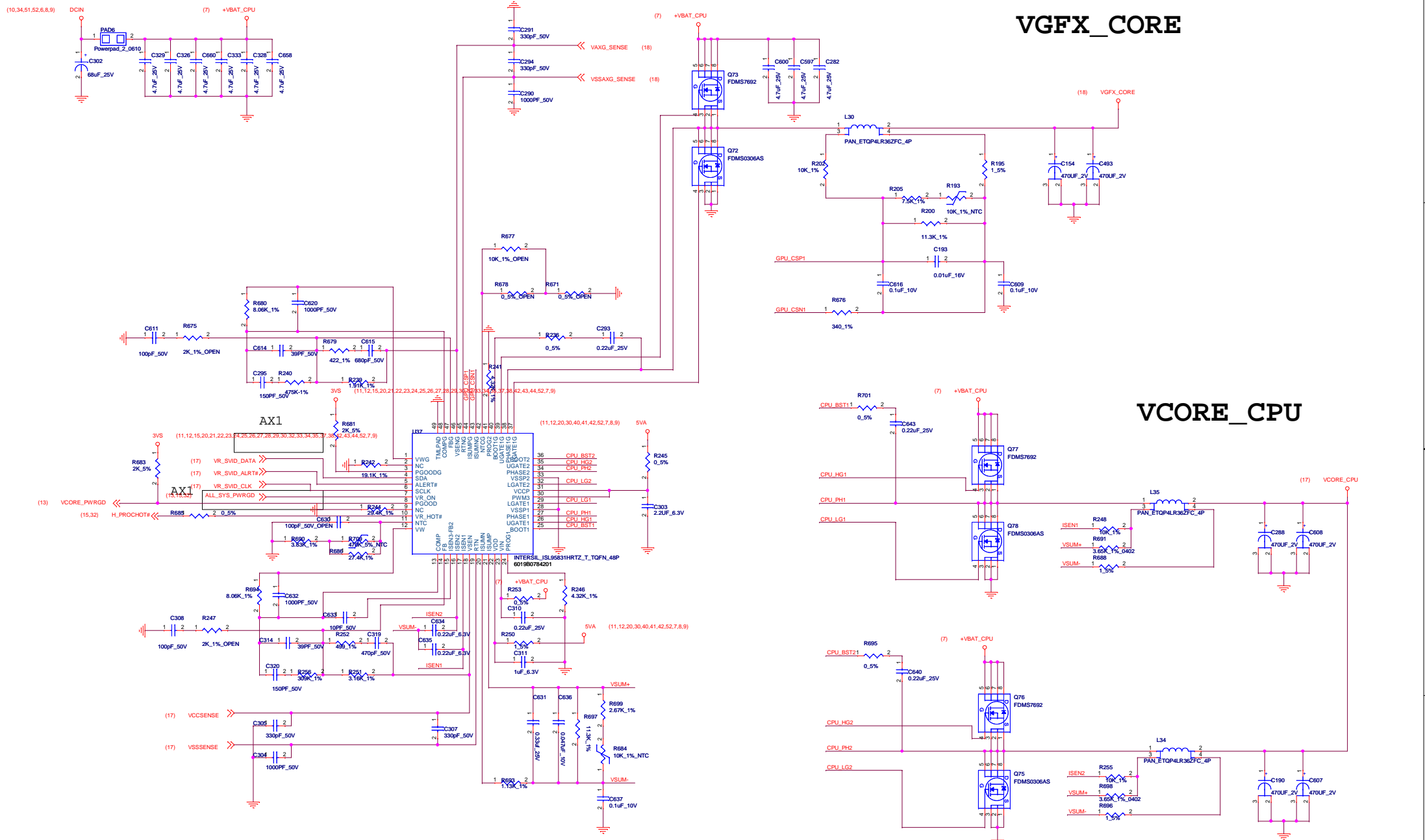
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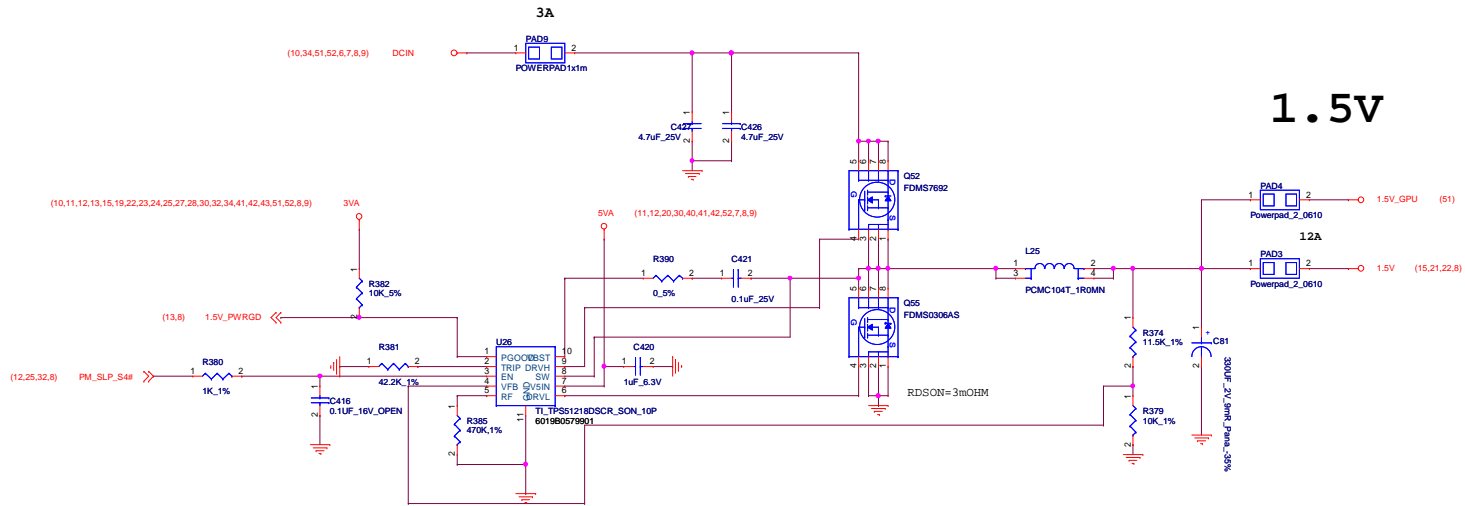
# AC/DC\_IN



# Battery CNN

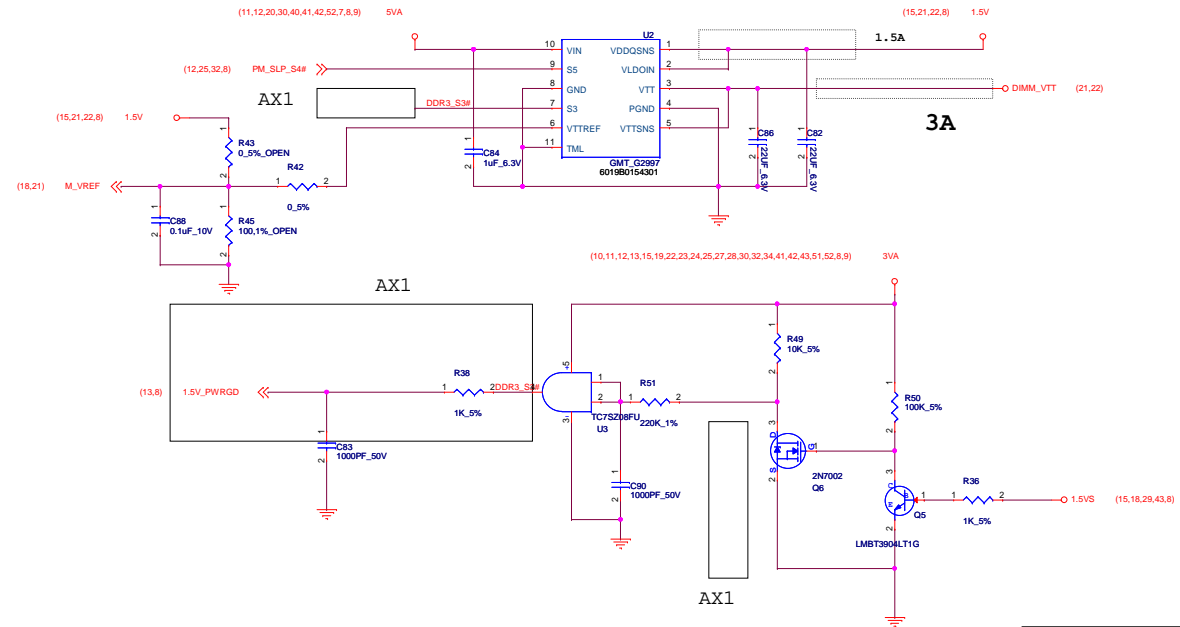






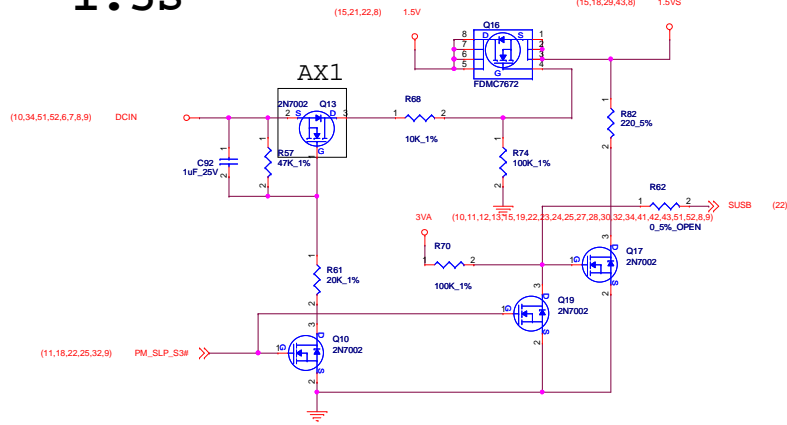
1.5V

## DIMM\_VTT



3A

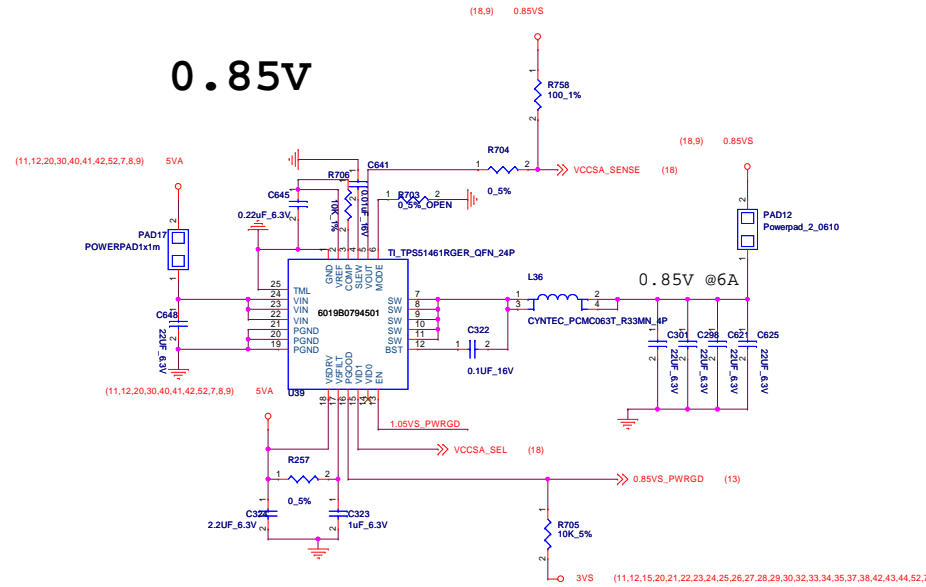
1.5S



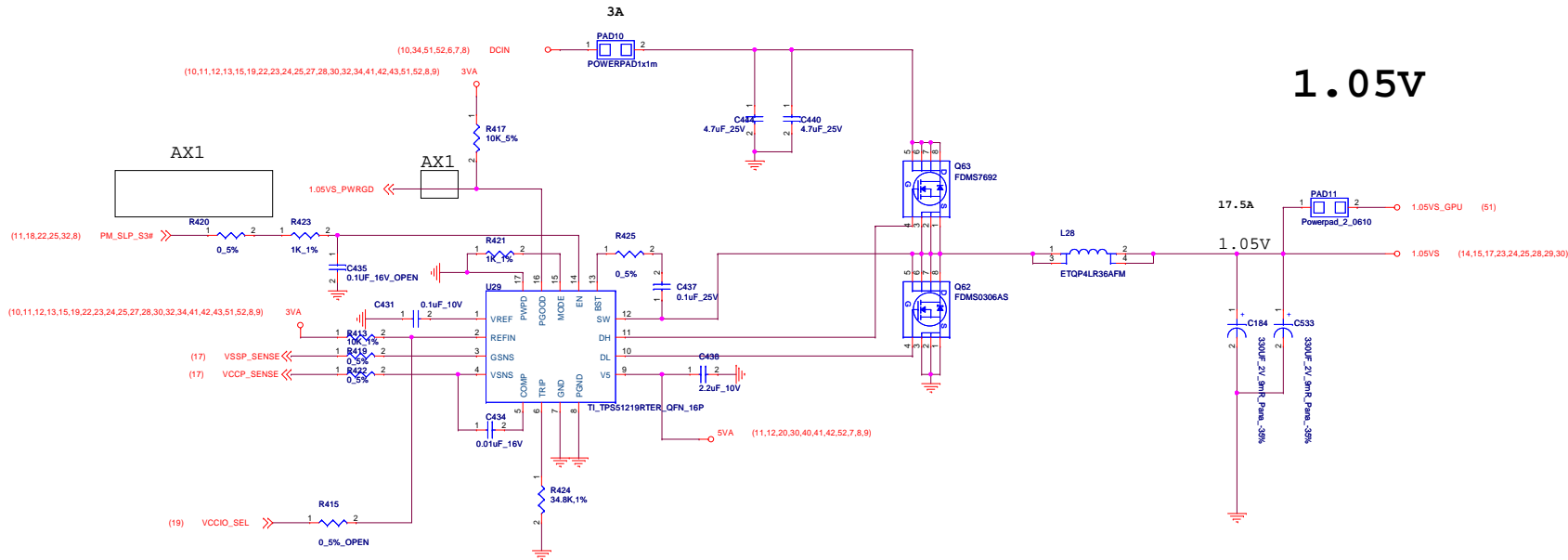
INVENTEC				
TITLE Strike				
CUSTOM CODE DOC NUMBER REV				
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0.85V

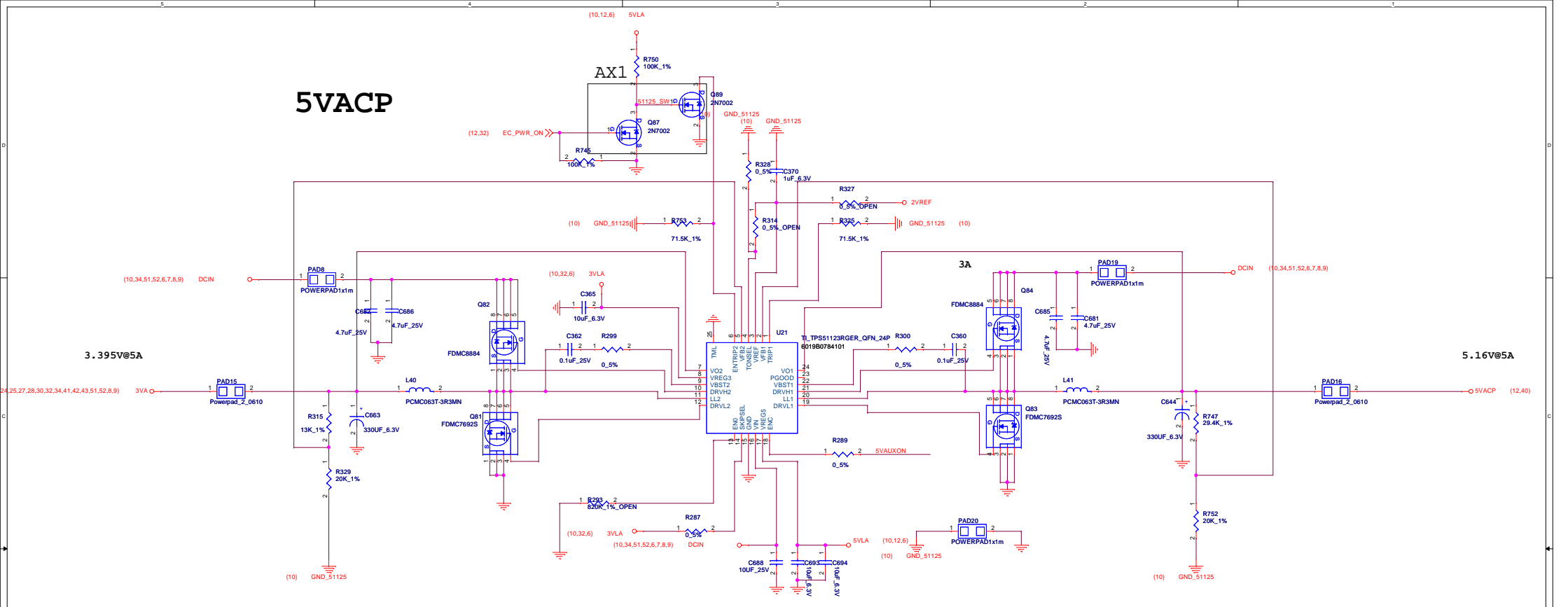


1.05V

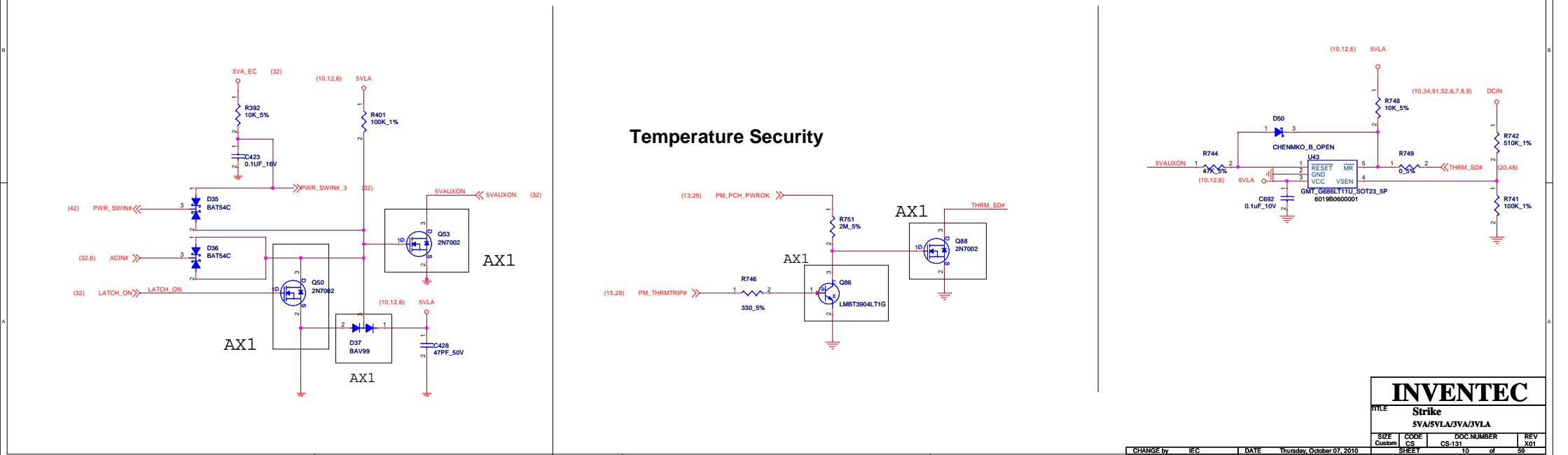


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1.05VS/VCCP			
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Custom	CS	CS-131	X01
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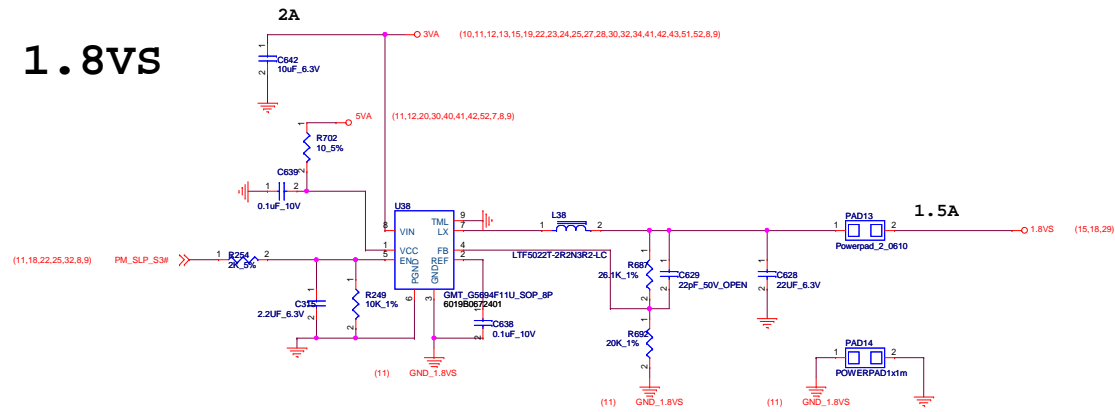
# 5VACP



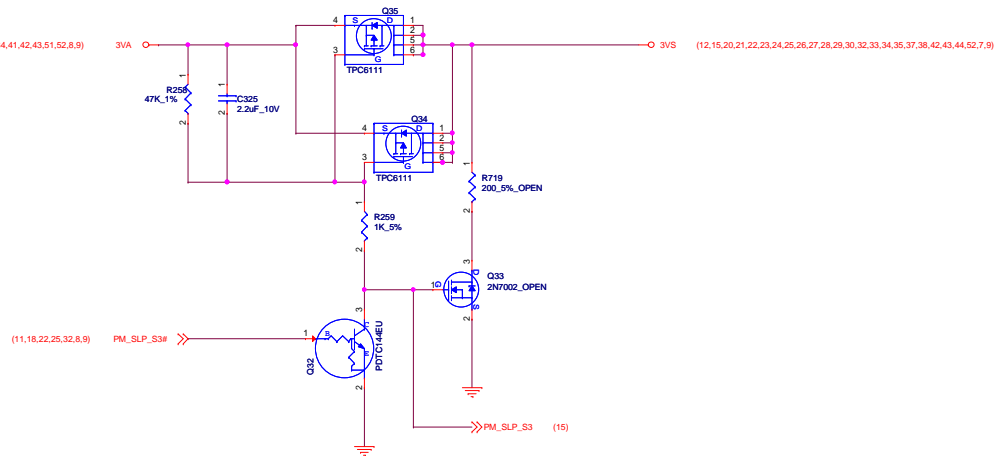
## Temperature Security



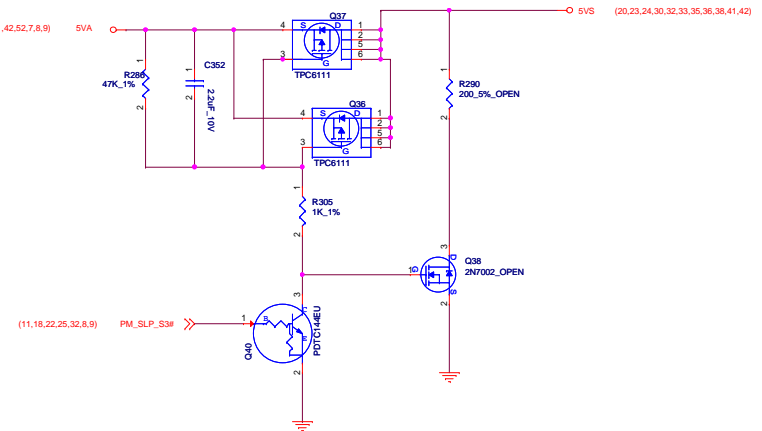
1.8VS



3VS

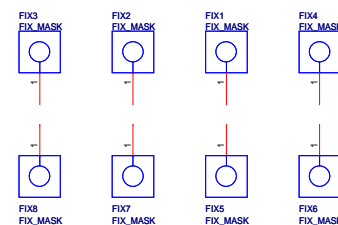


5VS



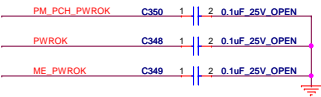
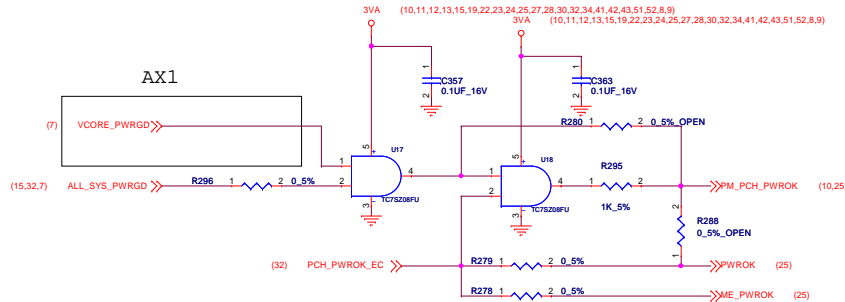
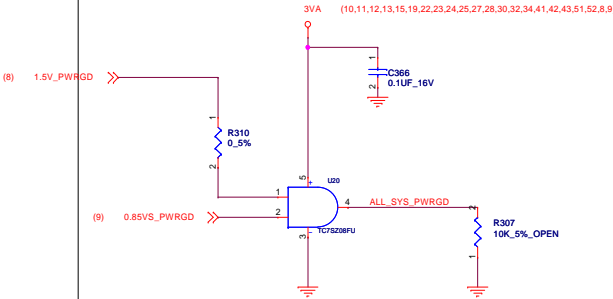
The diagram illustrates the connection between the MAT\_ARK2P60337YG\_60P 6012B03065901 module and the AX1 module. The MAT module is a blue component with a 60-pin header. The AX1 module is a black component with a 60-pin header. The connections are as follows:

- Power Connections:**
  - 3V5: Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60.
  - 3VA: Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60.
  - 5VA: Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60.
- Signal Connections:**
  - SMB\_DATA\_3A: Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60.
  - SMB\_CLK\_3A: Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60.
  - LAN\_D3# and LAN\_ON#: Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60.
  - PCIE\_WAKE# and LAN\_CABLE\_IN#: Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60.
  - PM\_SLP\_S4#: Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60.
  - USB\_P2- and USB\_P2+: Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60.
  - USB\_P3- and USB\_P3+: Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60.
  - CLK\_PCIE\_LAN and CLK\_PCIE\_LAN#: Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60.
  - BUF\_PLT\_RST#: Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60.
  - PCIE\_LAN\_RXP and PCIe\_LAN\_RXN: Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60.
  - PCIE\_LAN\_TXP and PCIe\_LAN\_TXN: Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60.
  - PCIE\_CLKREQ3#: Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60.

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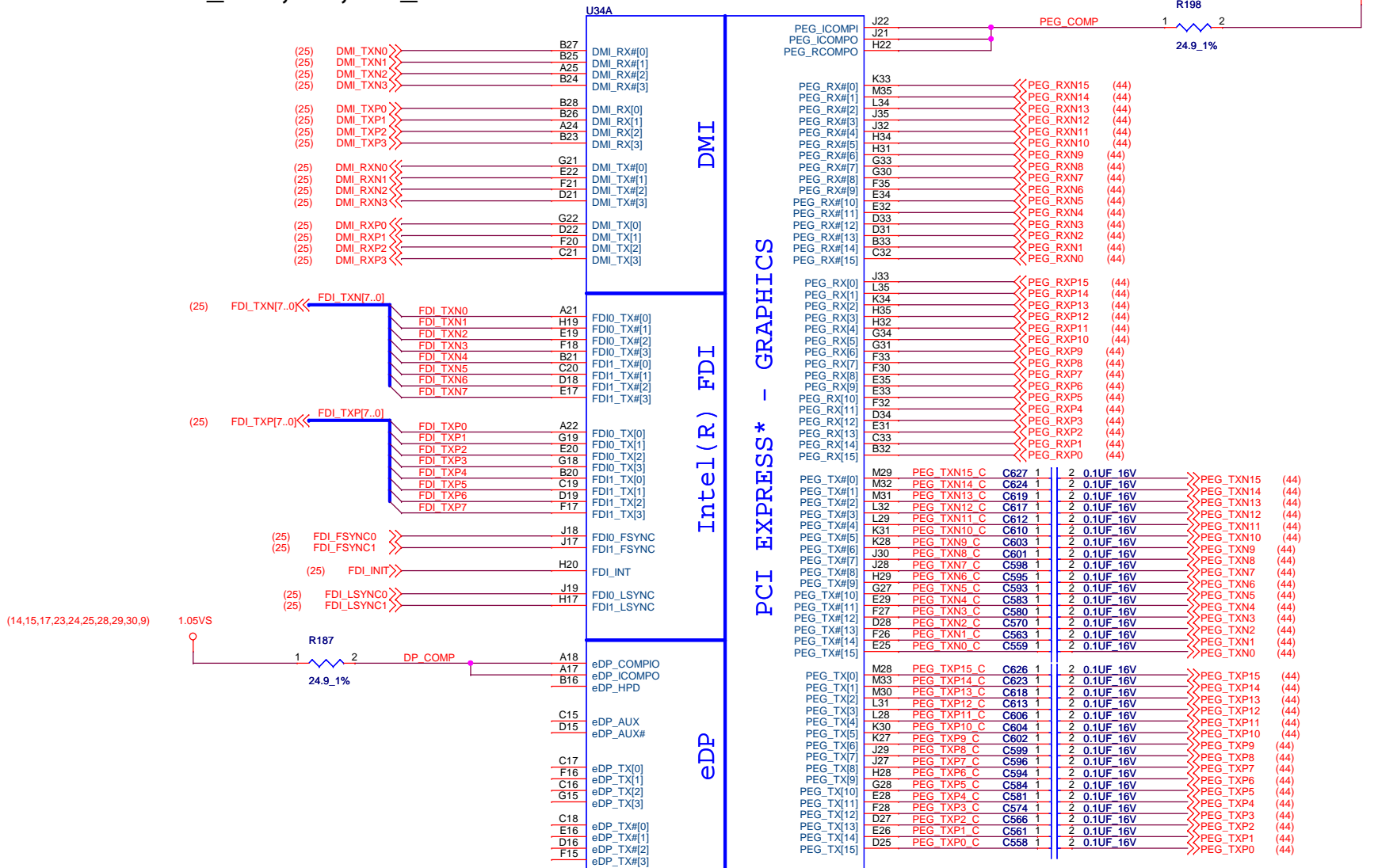
POWER SEQUENCE

AX1



INVENTEC			
TITLE			
Strike			
POWER SEQUENCE			
SIZE	CODE	DOC NUMBER	REV
Custom	ANS		X01
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Processor\_DMI,FDI,PCI\_e



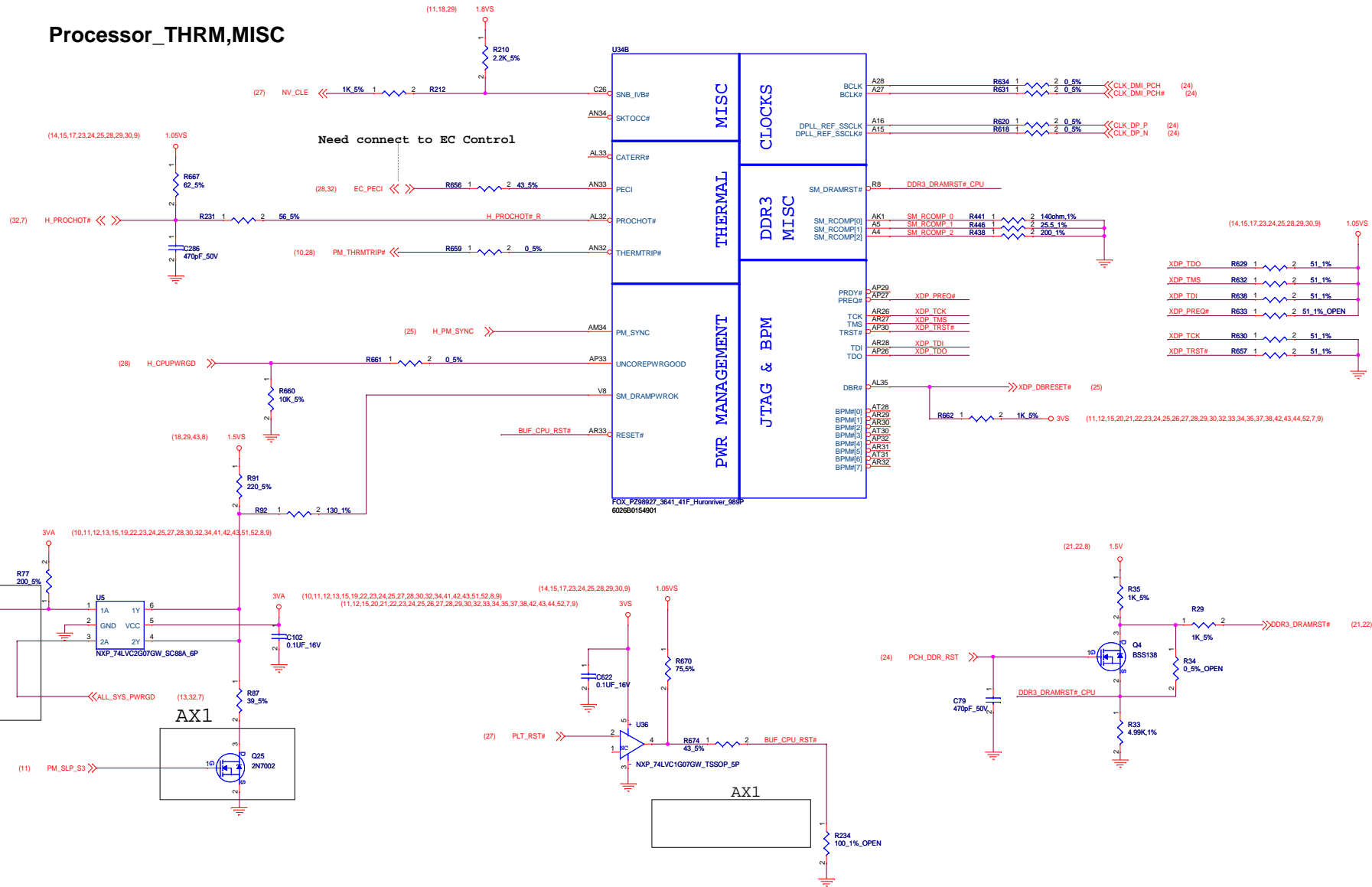
FOX PZ98927\_3641\_41F\_Huronriver\_989P  
6026B0154901

CLOSED TO CPU

INVENTEC			
TITLE			
Strike Processor(1/6)			
SIZE	CODE	DOC.NUMBER	REV
B	CS	CS-131	X01
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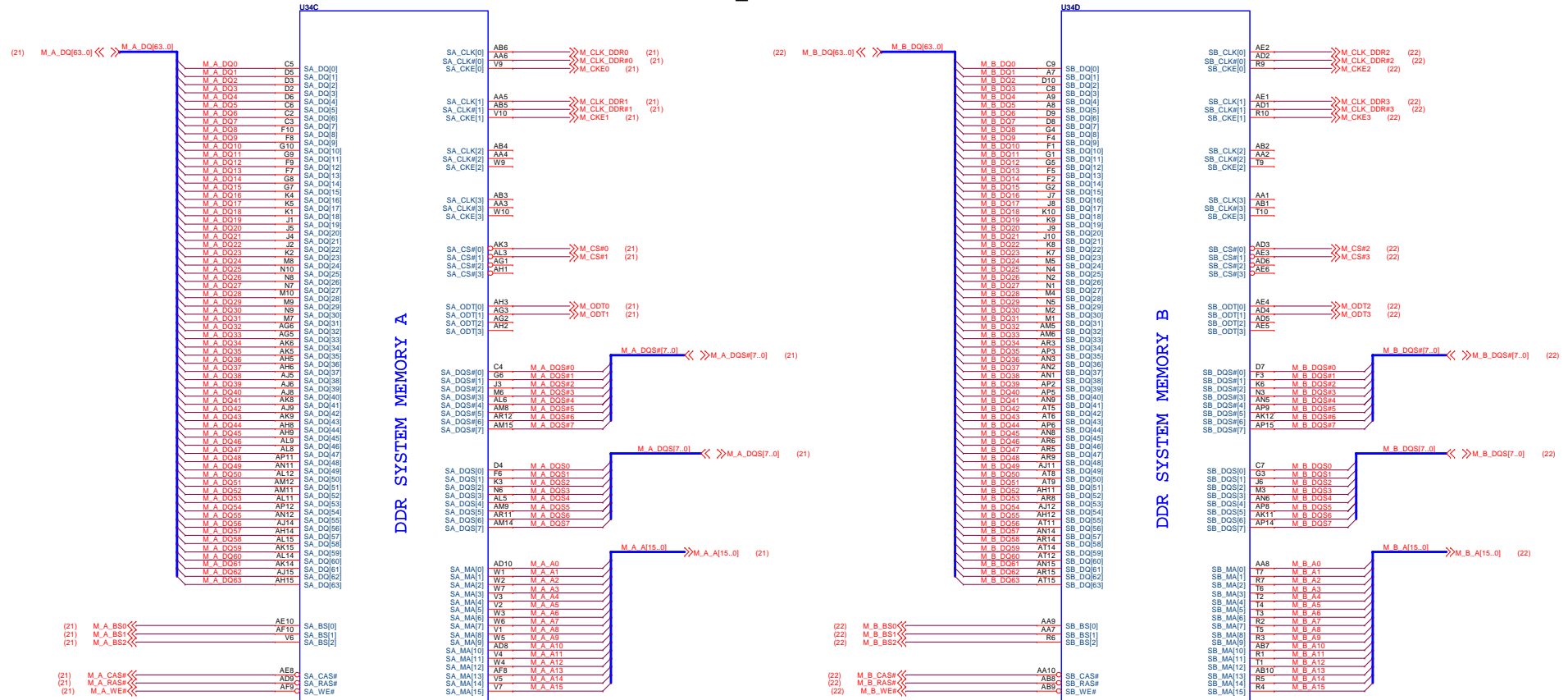
# Processor\_THRM,MISC



**INVENTEC**

TITLE			
Strike Processor(2/6)			
SIZE	CODE	DOC NUMBER	REV
C	CS	CS-131	X01
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# Processor\_DDR3



FOX\_P298927\_3641\_41F\_Huronriver\_989P  
6026B0154901

FOX\_P298927\_3641\_41F\_Huronriver\_989P  
6026B0154901

INVENTEC

Strike  
Processor(3/6)

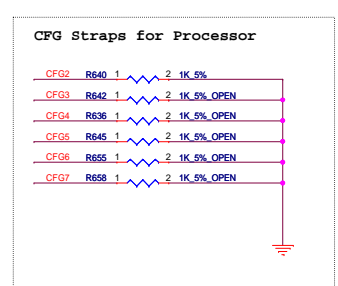
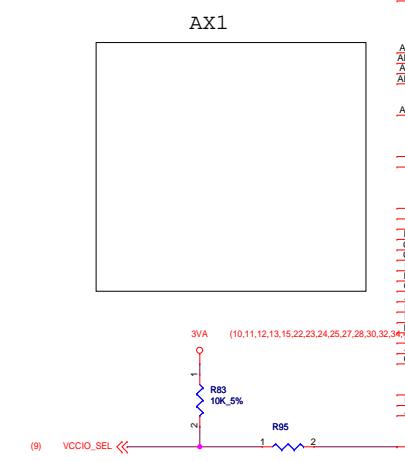
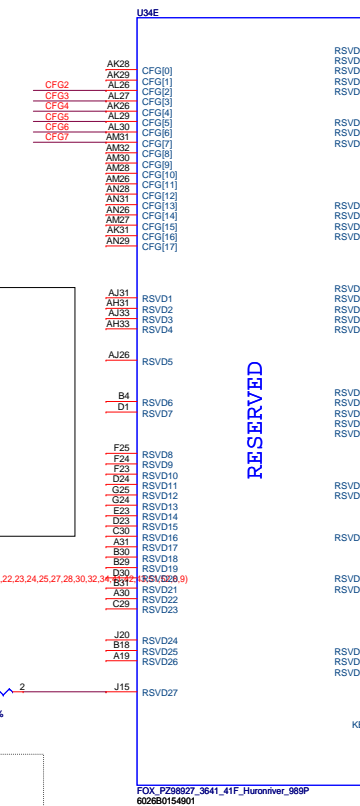
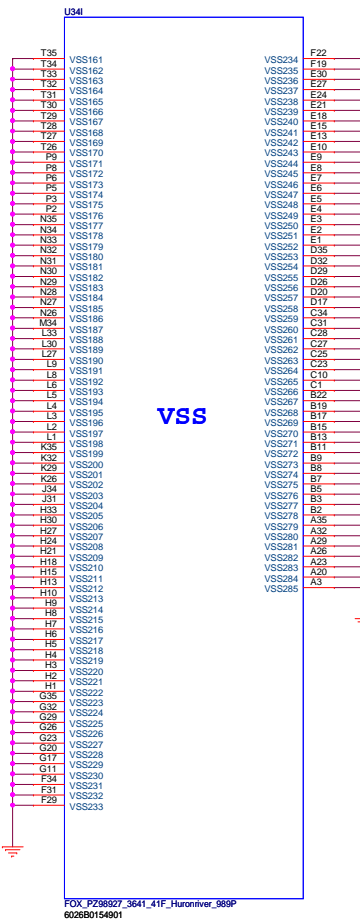
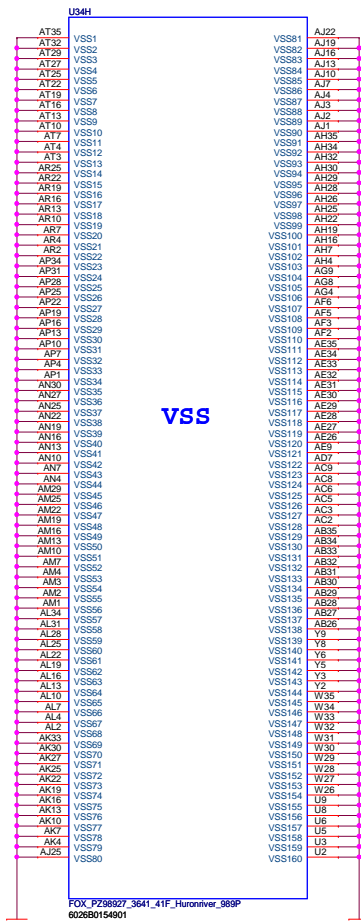
SIZE	CODE	DOC NUMBER	REV
Custom	CS	CS-131	X01

CHANGE by IEC DATE Thursday, October 07, 2010







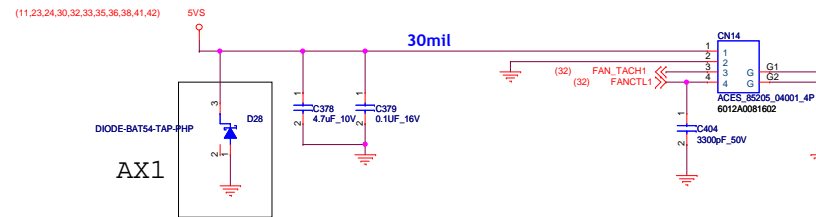


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation: Line # definition matches socket pin map definition 0:Lane Reversed
Display Port Presence Strap	
CFG2	1:(Default) Normal Operation: Line # definition matches socket pin map definition 0:Lane Reversed
PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default)x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1:(Default) PEG Train immediately following RESETB de assertion 0:PEG Wait for BIOS for training

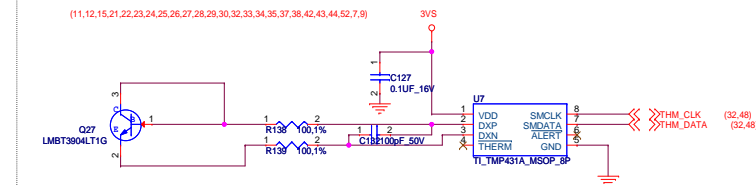
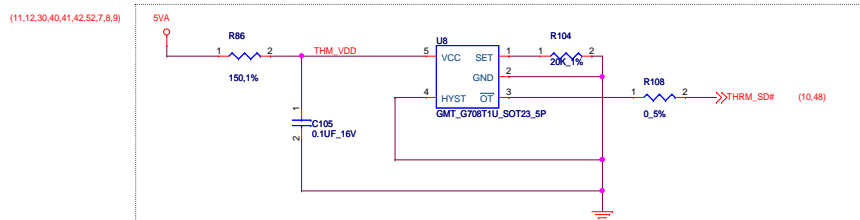
INVENTEC				
Strike Processor(6/6)				
TITLE	CODE	DOC NUMBER	REV	
SIZE C	CS	CS-131	19	59

## Fan control



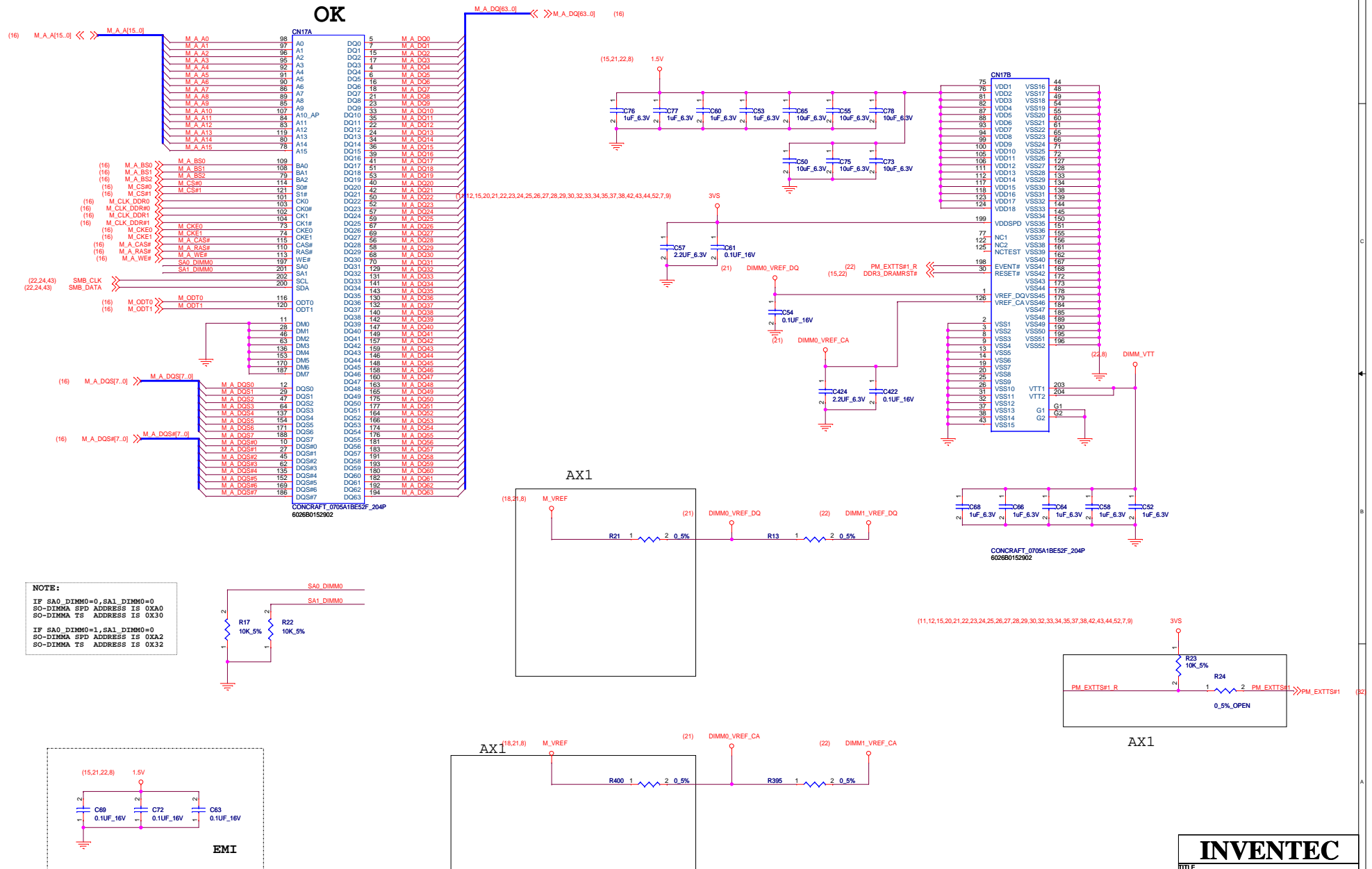
## GPU Thermal sensor

REMOTE thermal sensor  
Place near the hottest spot area under Palm-rest

**INVENTEC**

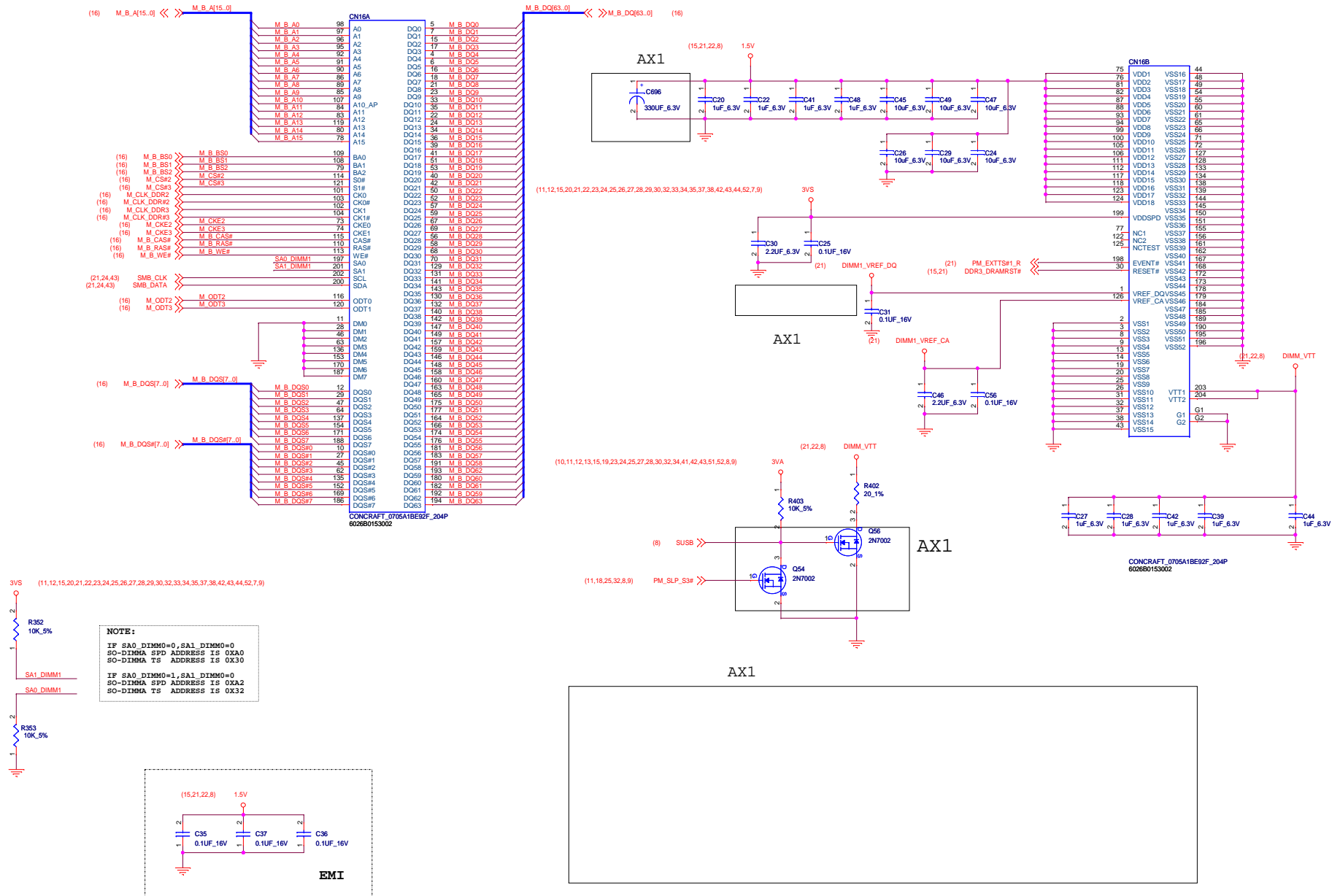
TITLE			
Strike Fan/Thermal			
SIZE	CODE	DOC. NUMBER	REV
C	CS	CS-131	X01
SHEET		20 of	59

## SO-DIMMO



## SO-DIMM 1

OK

**INVENTEC**

TITLE			
Strike			
DDR3 SDRAM SO-DIMM 2/2			
SIZE	CODE	DOC. NUMBER	REV
C	CS	CS-131	X01
SHEET		22	of 59

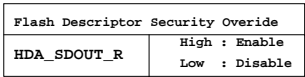
located on DIMM window area.

**CL1 CL2**

J1

JUMP2\_200\_32

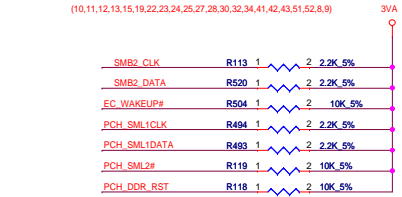
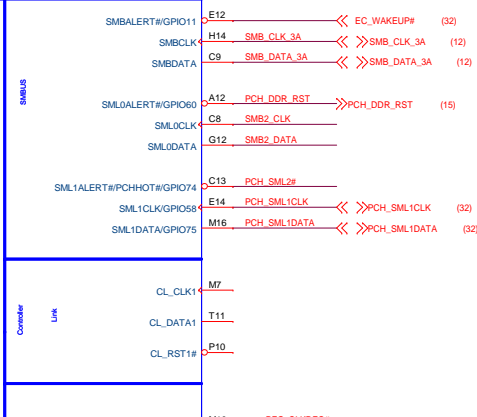
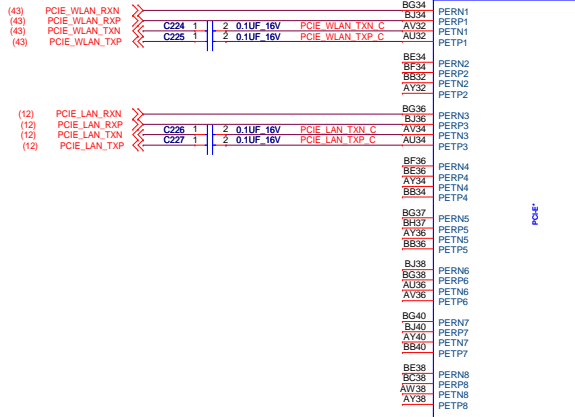
## 31



TITLE			
<p align="center"><b>Strike</b>  <b>PCH(SATA,RTC,SPI)</b></p>			
SIZE	CODE	DOC NUMBER	REV
C	CS	CS-131	X01
SHEET		23	of 59

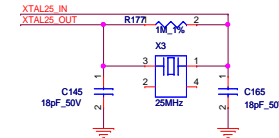
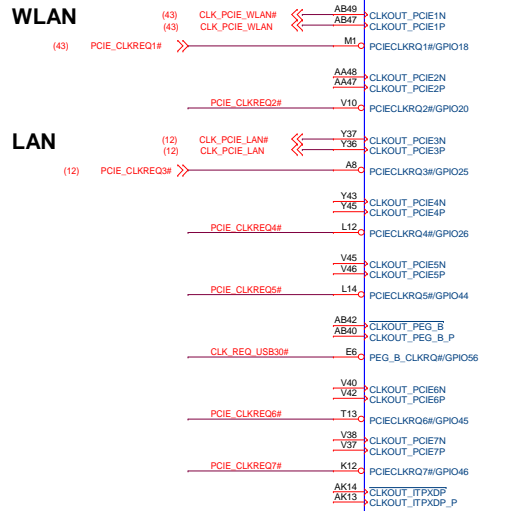
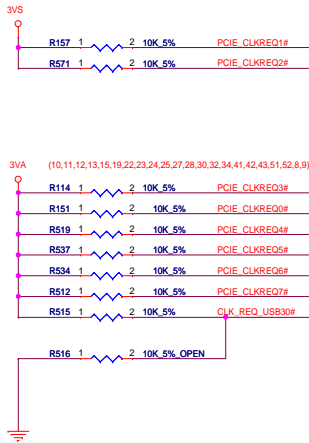
# WLAN

# PCIE LAN

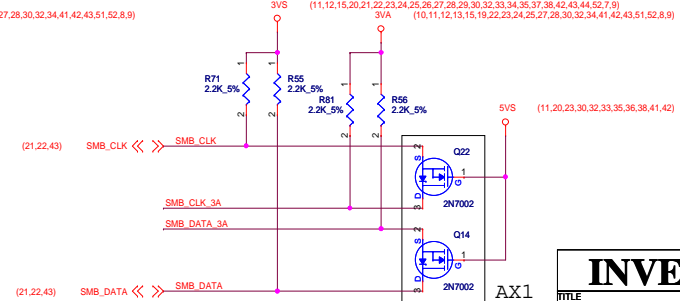
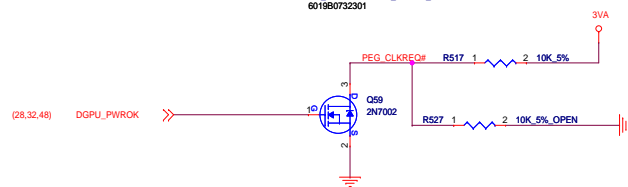


# WLAN

# LAN



PCIECLKREQ# 0,3,4,5,6,7 --- 3VA plane  
PCIECLKREQ# 1,2 --- 3VS plane



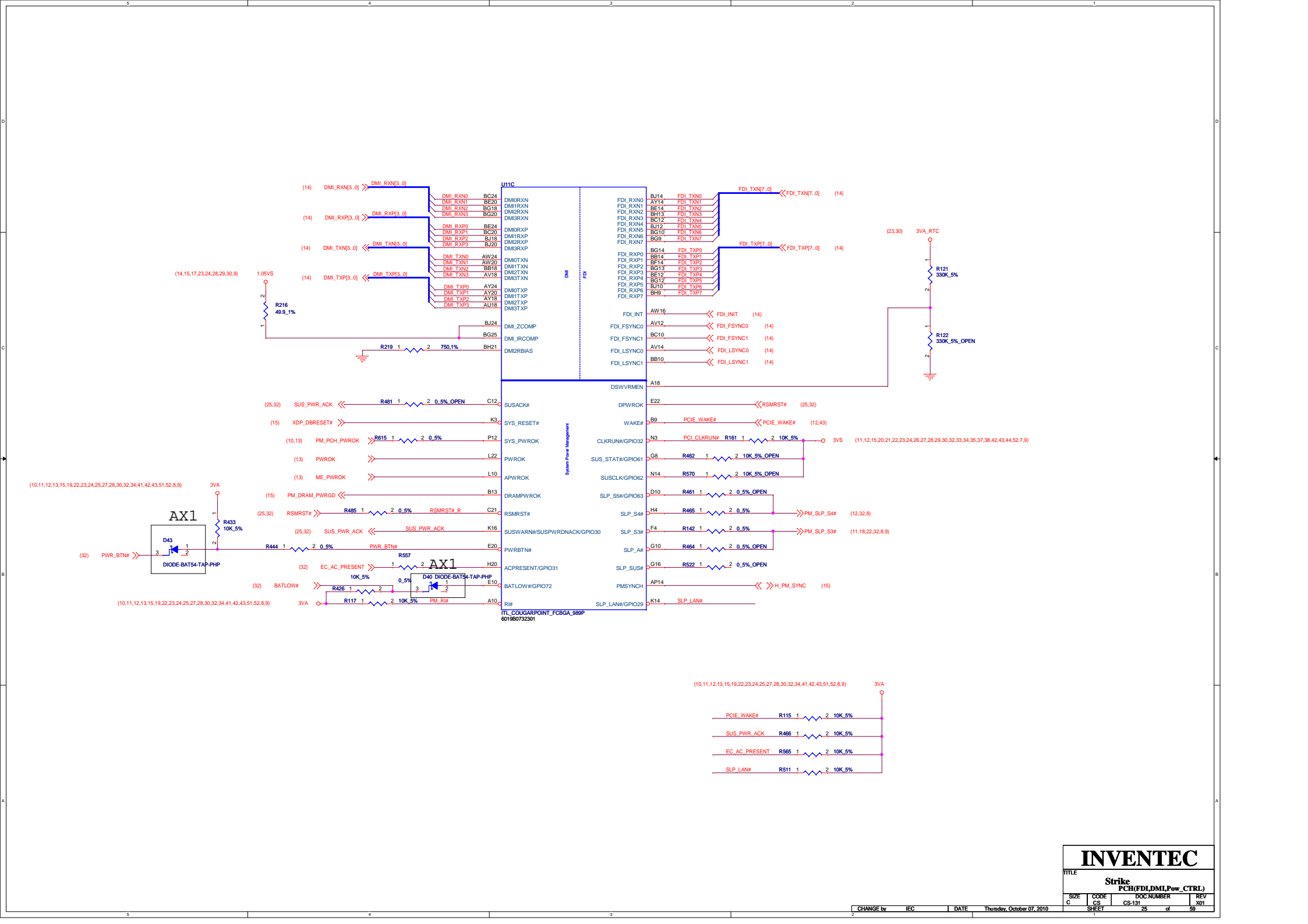
**INVENTEC**

Strike PCH(PCIE, I2C)

SIZE CODE CS 131  
SHEET 24 of 59

CHANGE by IEC DATE Thursday, October 07, 2010

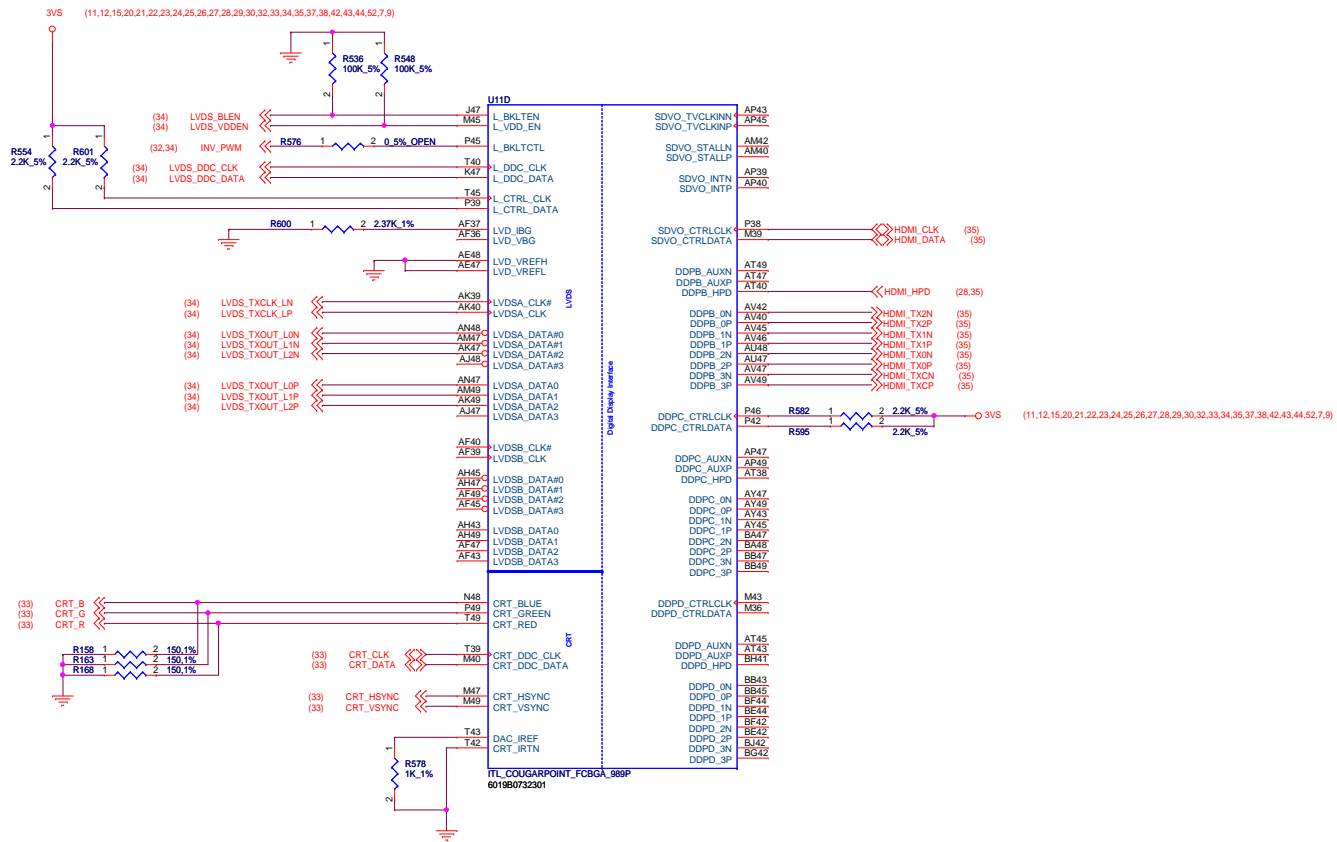




# INVENTEC

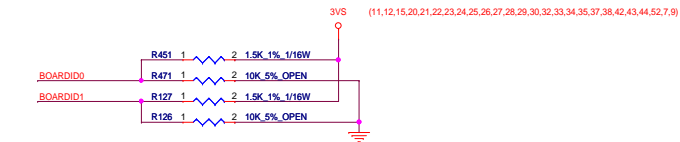
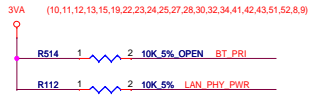
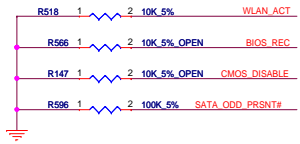
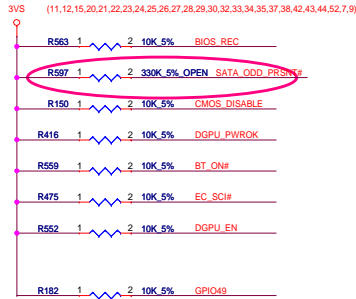
Strike FDL DML Pow\_CTRL

SIZE	CODE	DOC NUMBER	REV
C	CS	CS-131	X01



Place 150ohm termination resistor close to GMCH





(11,12,15,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37,38,42,43,44,52,7,9)

(10,11,12,13,15,19,22,23,24,25,27,28,30,32,34,41,42,43,51,52,8,9)

AX1

(24,32,48) DGPU\_PWROK <<>

(43) BT\_PRI <<>

(32,40) USB\_CTL1 <<>

(32,43) RF\_LAN\_KILL# <<>

(32,40) USB\_CTL2 <<>

SATA\_ODD\_PRSNT# R585 1 2 0.5% <<>

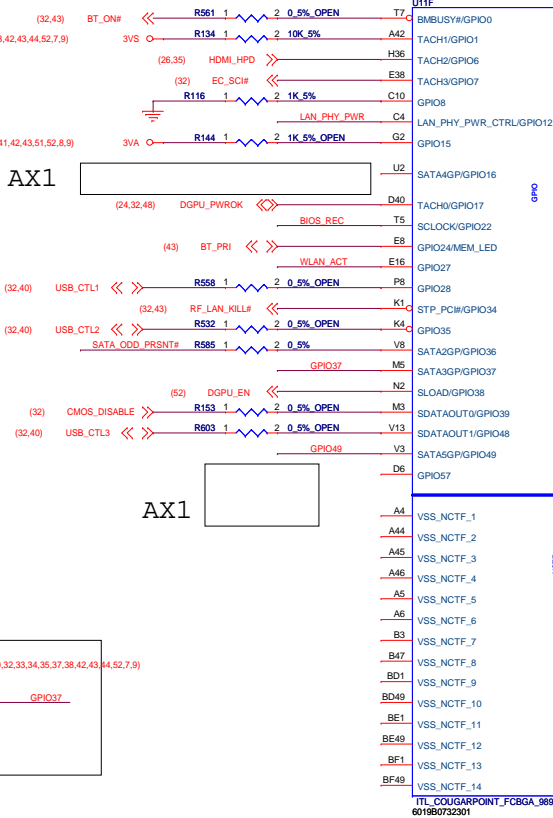
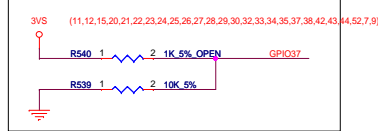
GPIO37

(52) DGPU\_EN <<>

(32) CMOS\_DISABLE <<>

(32,40) USB\_CTL3 <<>

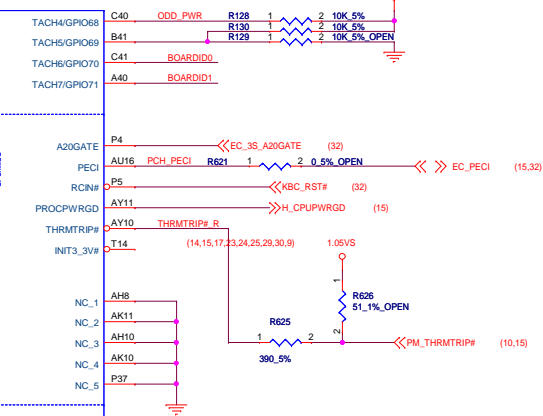
AX1



GPIO

NCTF

(11,12,15,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37,38,42,43,44,52,7,9)



VSS\_NCTF\_15 BG2

VSS\_NCTF\_16 BG48

VSS\_NCTF\_17 BH3

VSS\_NCTF\_18 BH47

VSS\_NCTF\_19 BJ4

VSS\_NCTF\_20 BJ44

VSS\_NCTF\_21 BJ45

VSS\_NCTF\_22 BJ46

VSS\_NCTF\_23 BJ5

VSS\_NCTF\_24 BJ6

VSS\_NCTF\_25 C2

VSS\_NCTF\_26 C48

VSS\_NCTF\_27 D1

VSS\_NCTF\_28 D49

VSS\_NCTF\_29 E1

VSS\_NCTF\_30 E49

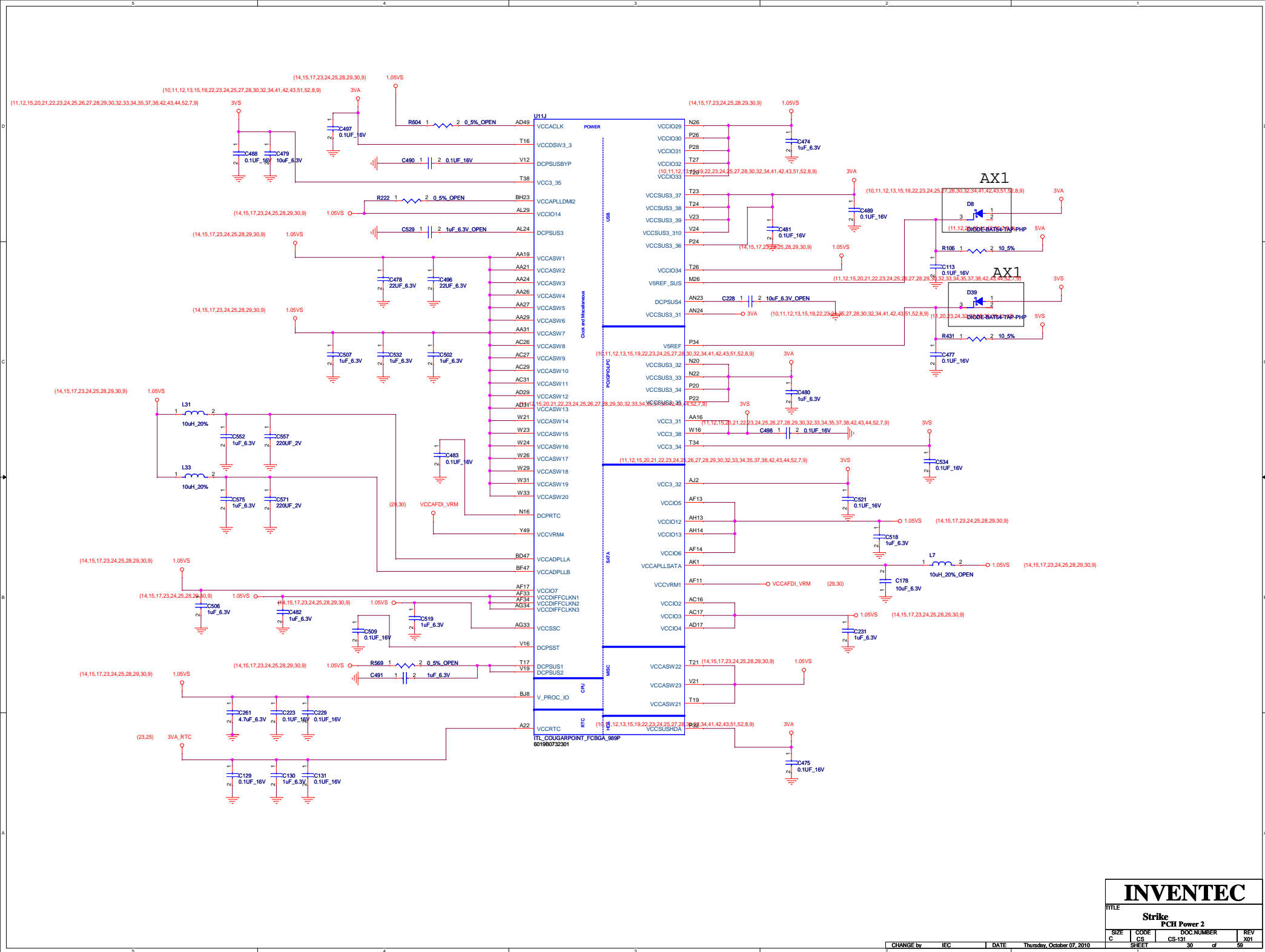
VSS\_NCTF\_31 F1

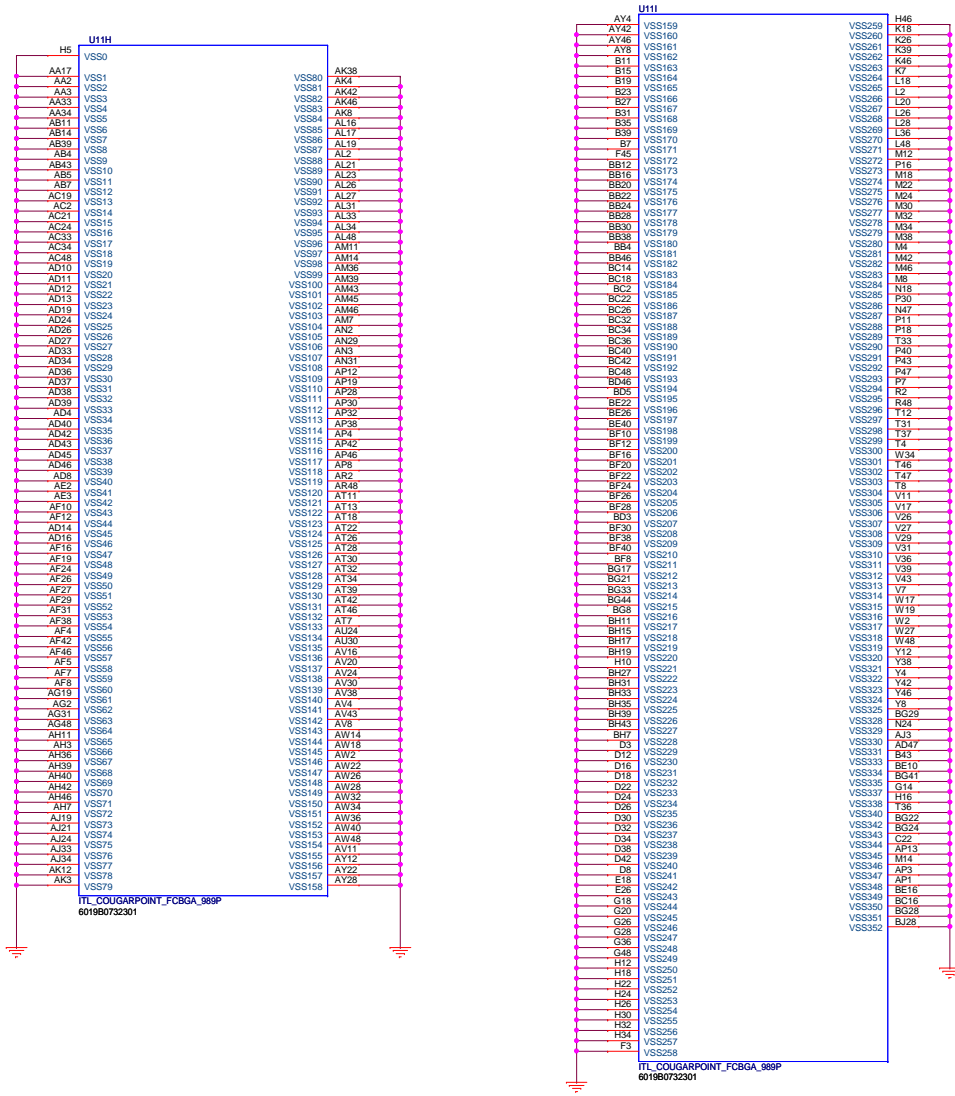
VSS\_NCTF\_32 F49

INVENTEC

TITLE			
Strike FCH(MISC,GPIO)			
SIZE	CODE	DOC NUMBER	REV
C	CS	CS-131	X01







<b>INVENTEC</b>			
TITLE			
Strike FCH GND			
SIZE	CODE	DOC NUMBER	REV
C	CS	CS-131	X01
SHEET		31	of 59

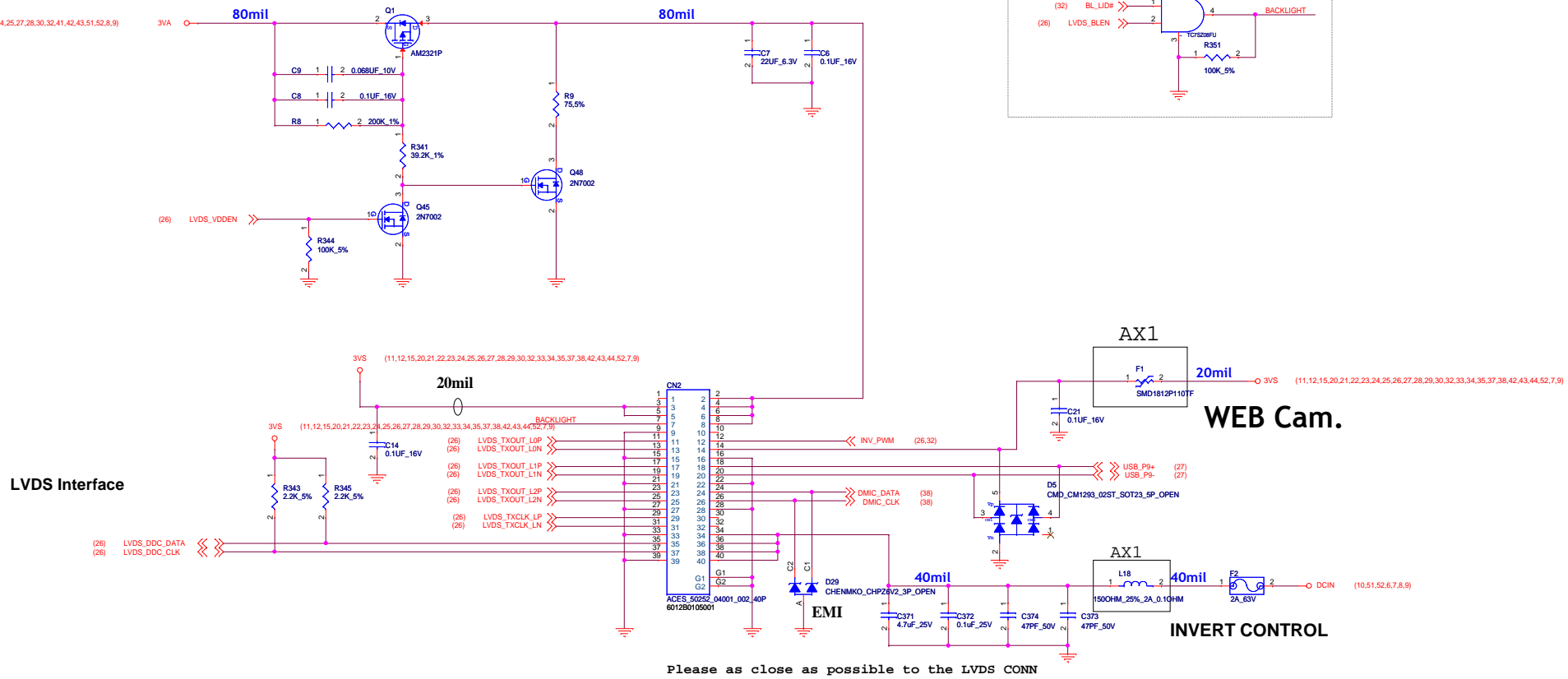
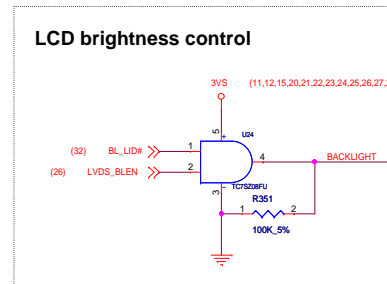




(11,12,15,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,37,38,42,43,44,52,7,9)

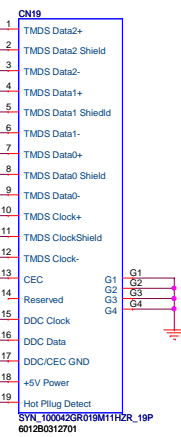
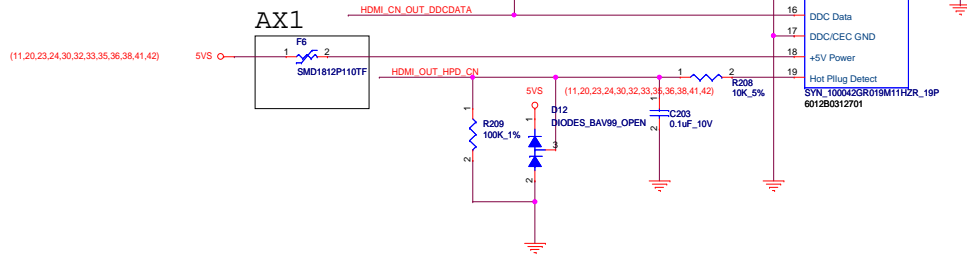
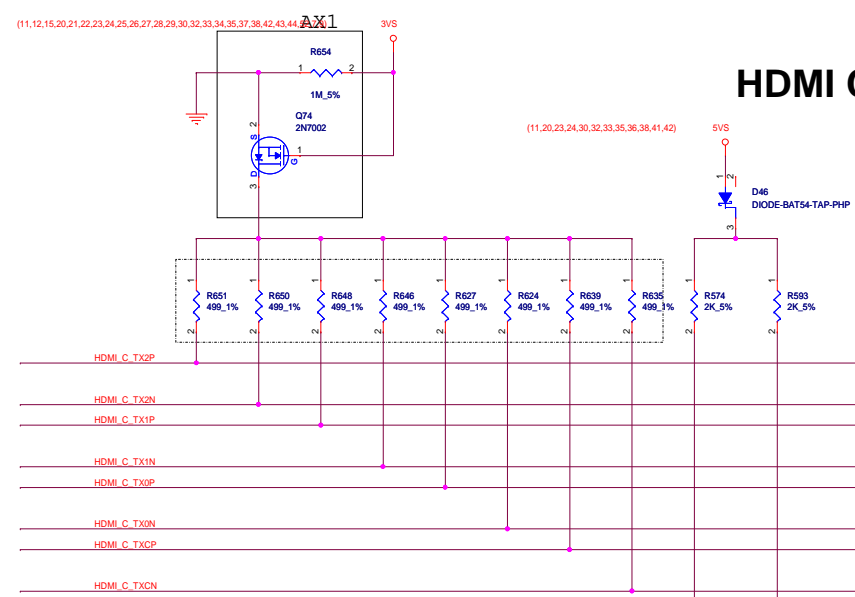
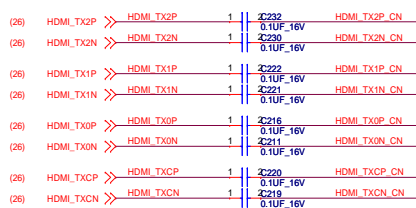


CHANGE by	IEC	DATE	Thursday, October 07, 2010
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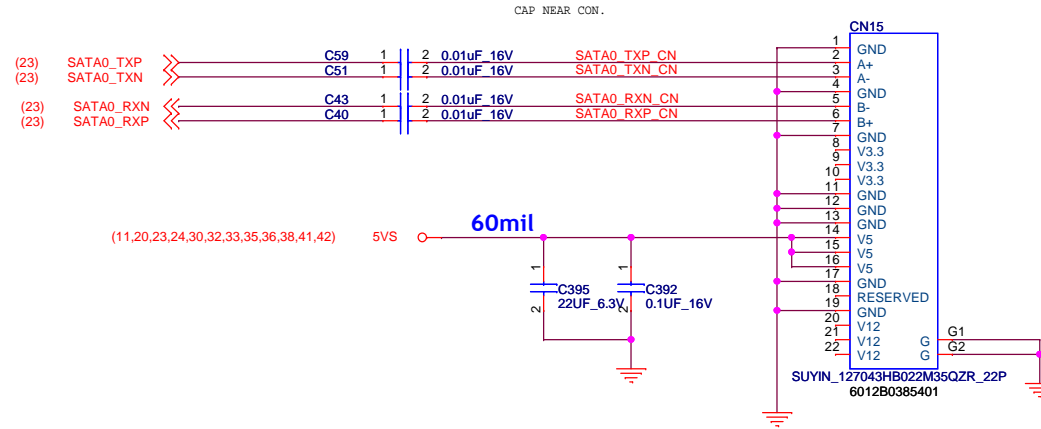


Please as close as possible to the LVDS CONN

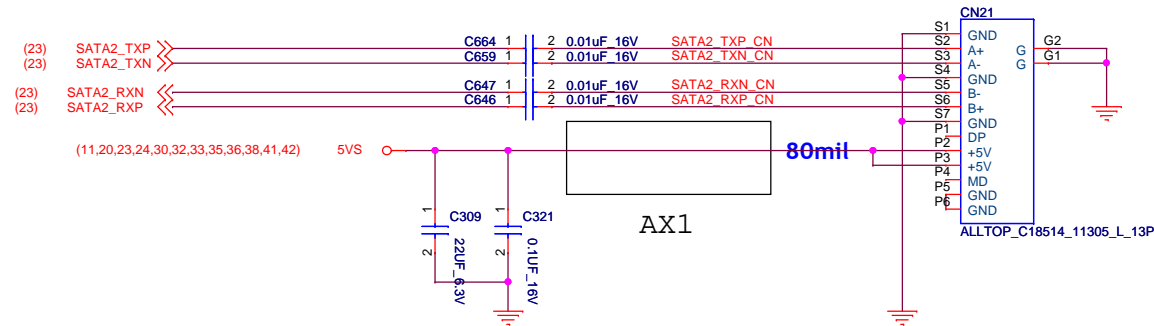
<b>INVENTEC</b>			
TITLE <b>Strike LVDS</b>			
SIZE C	CODE ES	DOC. NUMBER CS-131	REV X01
SHEET		34	of 59



# HDD I/F



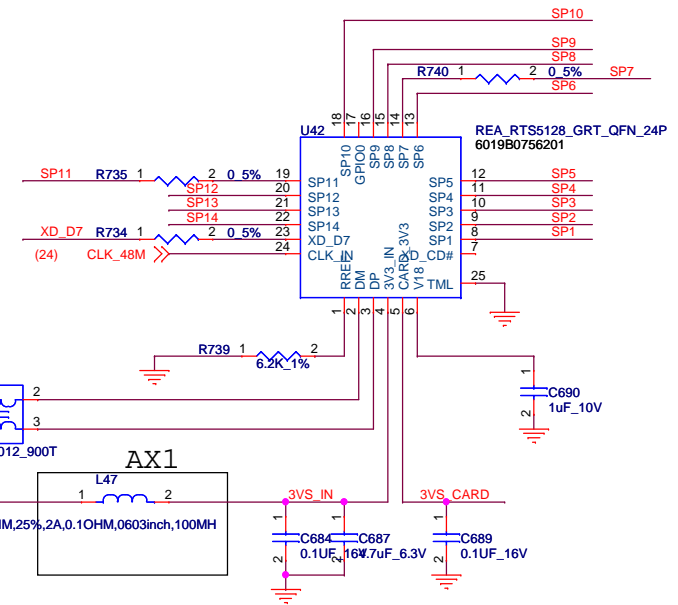
# ODD I/F



## INVENTEC

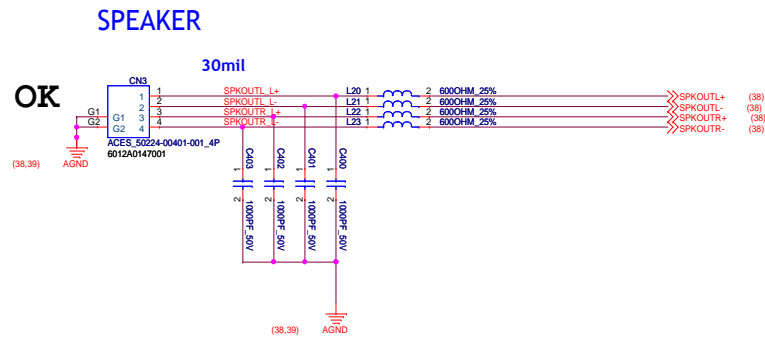
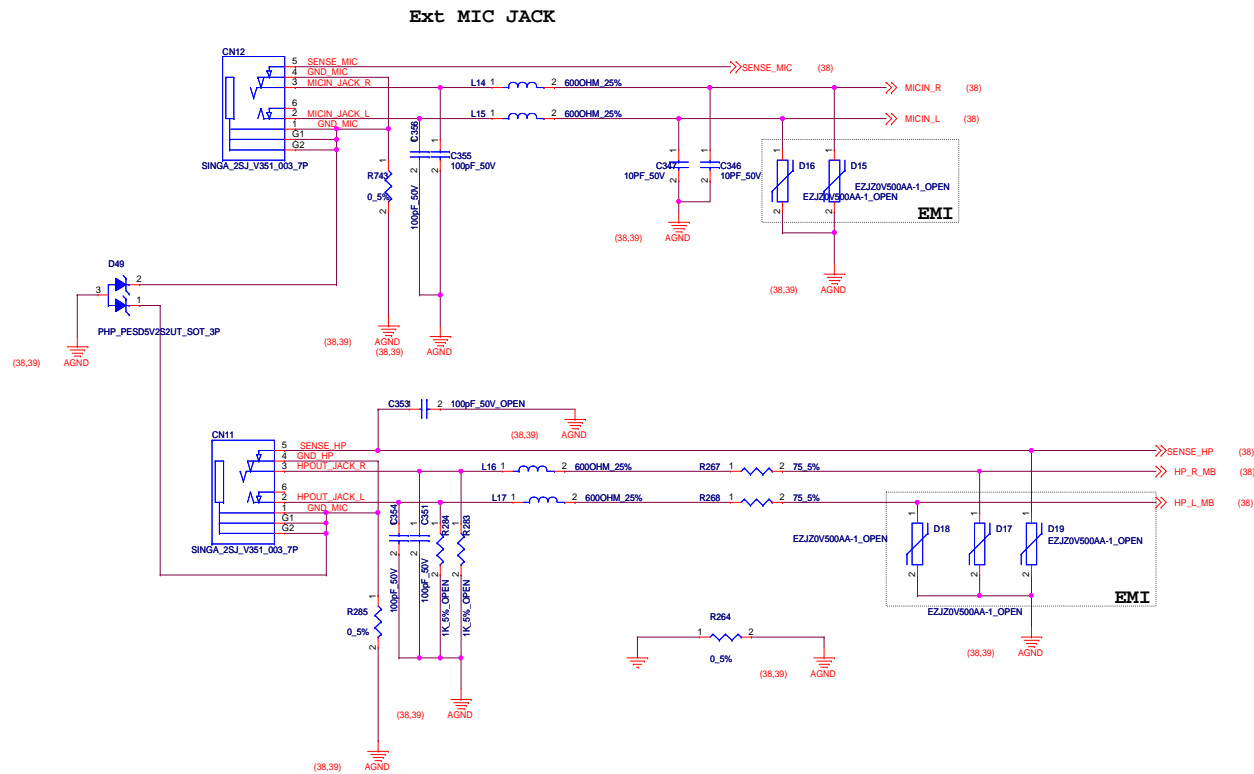
TITLE			
Strike HDD/ODD			
SIZE	CODE	DOC.NUMBER	REV
B	CS	CS-131	X01
SHEET		36 of 59	

CHANGE by IEC DATE Thursday, October 07, 2010

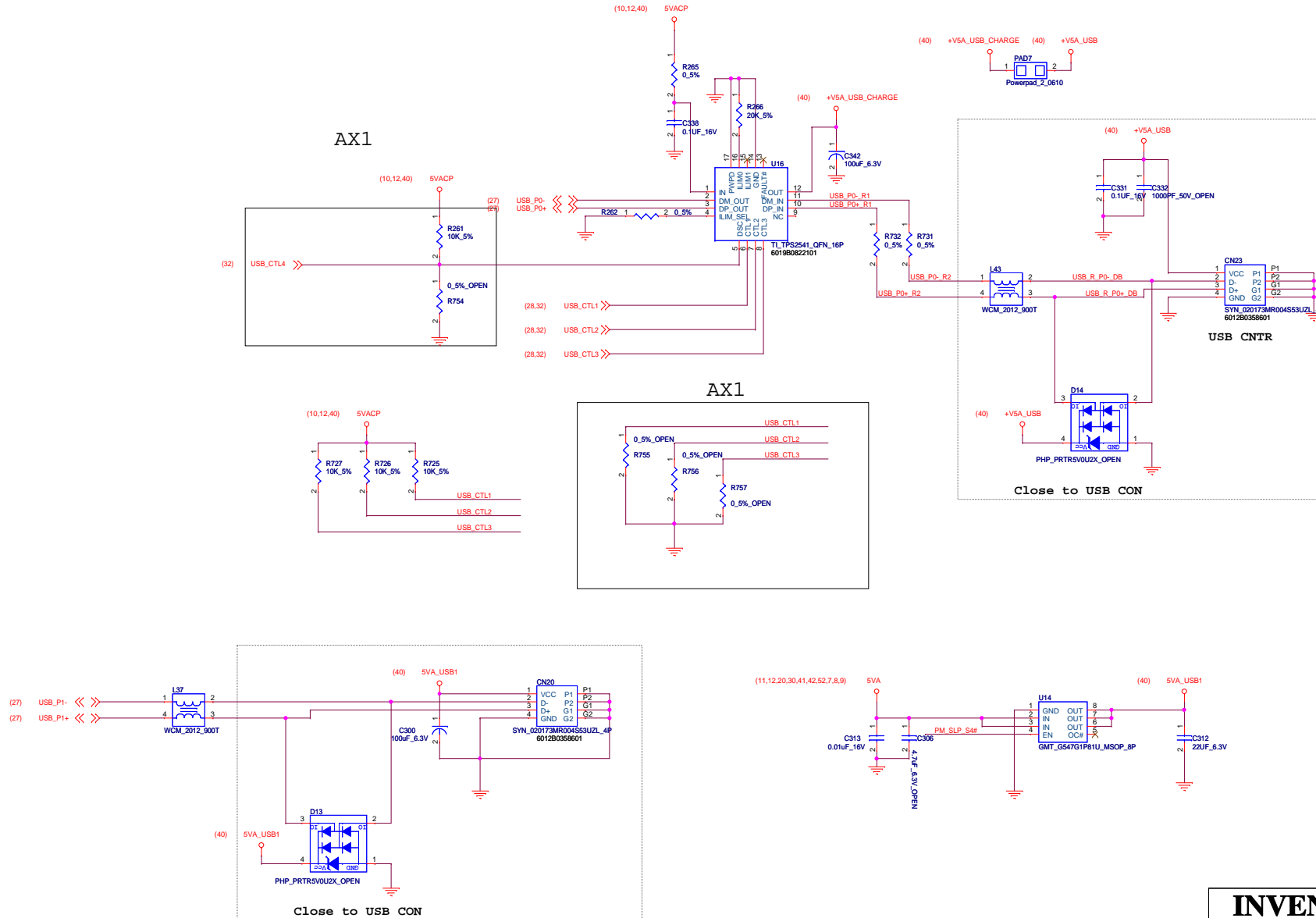


TITLE			
<b>Strike</b> <b>Card reader</b>			
SIZE	CODE	DOC.NUMBER	REV
B	CS	CS-131	X01
SHEET		37	of 59





# Power OFF Charge USB



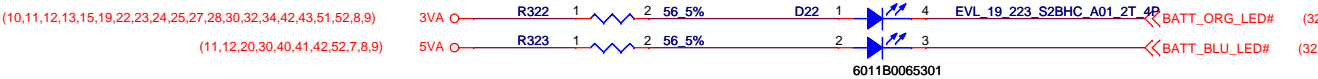
**INVENTEC**

TITLE			
Strike Charge USB			
SIZE	CODE	DOCNUMBER	REV
C	CS	CS-131	X01
SHEET		40	58





BLUE

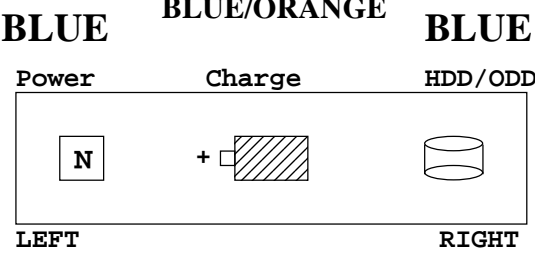


BLUE/ORANGE



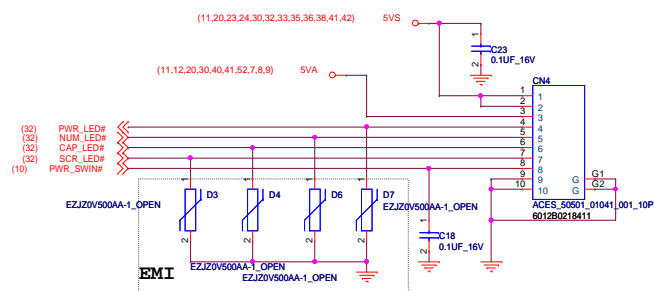
BLUE

LED Seat

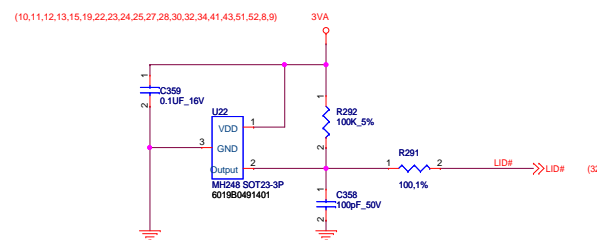


INVENTEC			
TITLE Strike LED			
SIZE B	CODE CS	DOC.NUMBER CS-131	REV X01
SHEET 1 41 of 59			

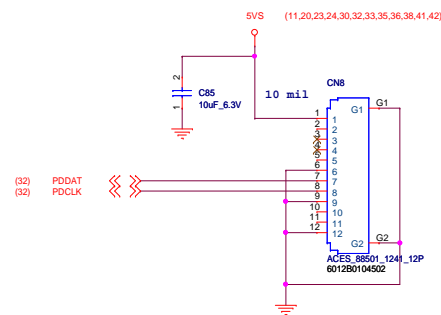
EMI POWER BUTTON BOARD



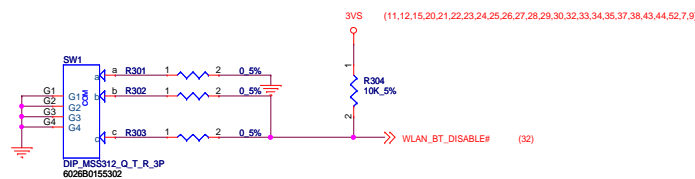
## HALL Switch



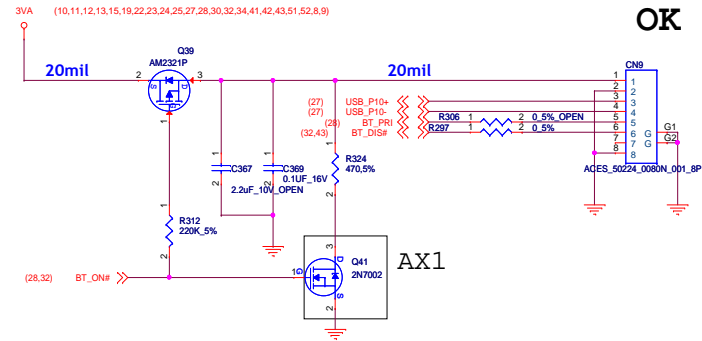
**GP CNN.**



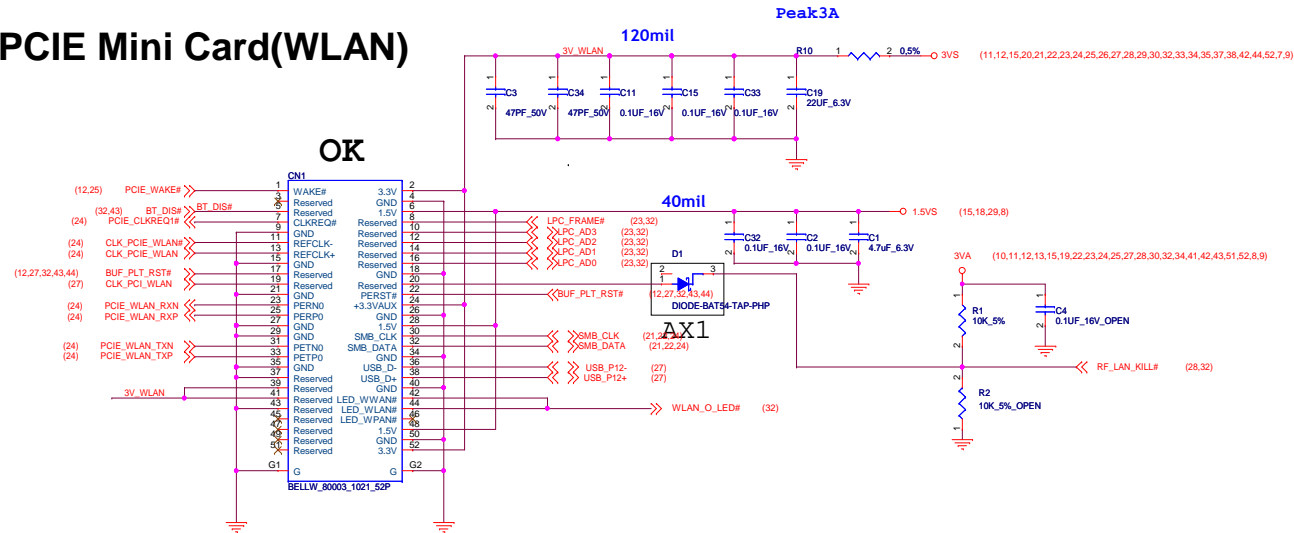
## (W-LAN, BT) sliding switch



## Bluetooth CNN.



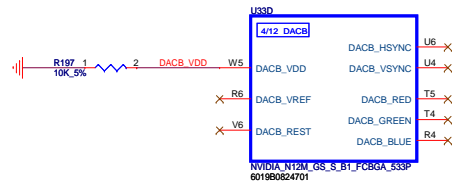
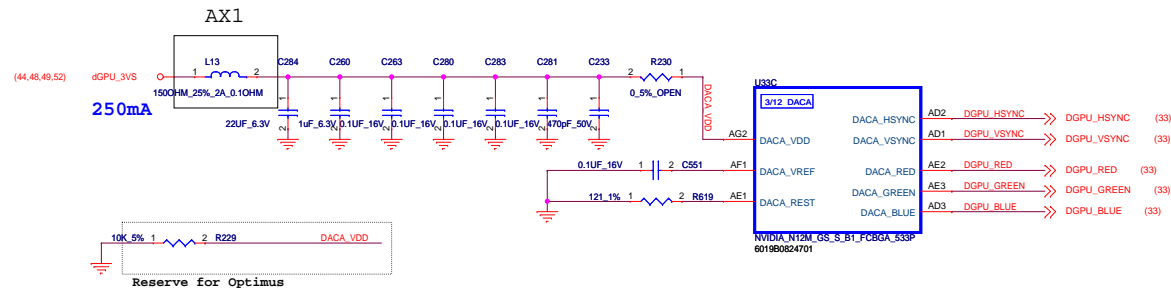
## PCIE Mini Card(WLAN)

**INVENTEC**

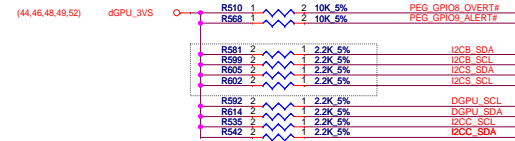
TITLE			
Strike WLAN/BT			
SIZE	CODE	DOC. NUMBER	REV
C	CS	CS-131	X01
SHEET		43 of	59



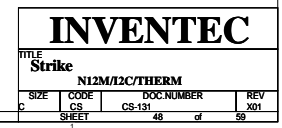








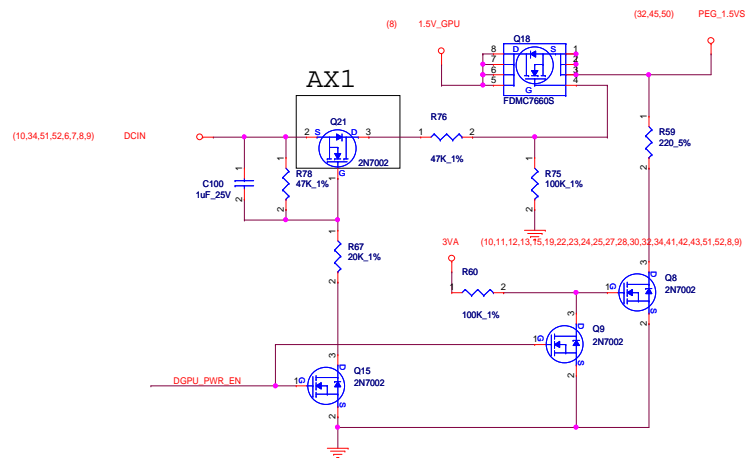
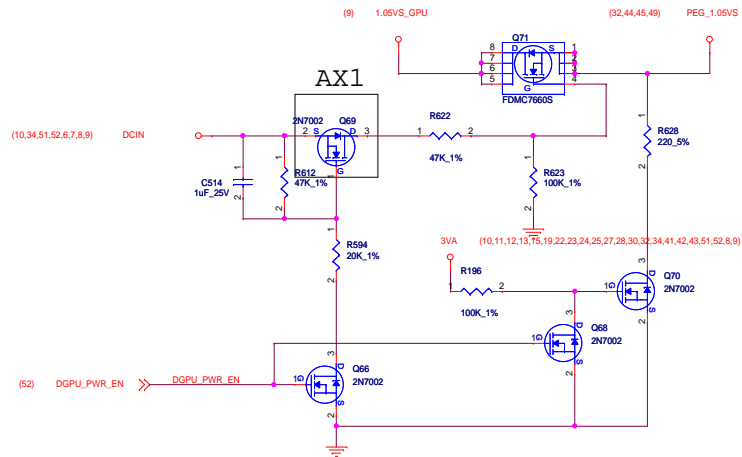
GPU Thermal Sensor  
Please close GPU side











# INVENTEC

TITLE			
Strike			
GPU Power			
SIZE	CODE	DOCNUMBER	REV
C	CS	CS-131	X01
SHEET		51	of 59



# Strike USB Board

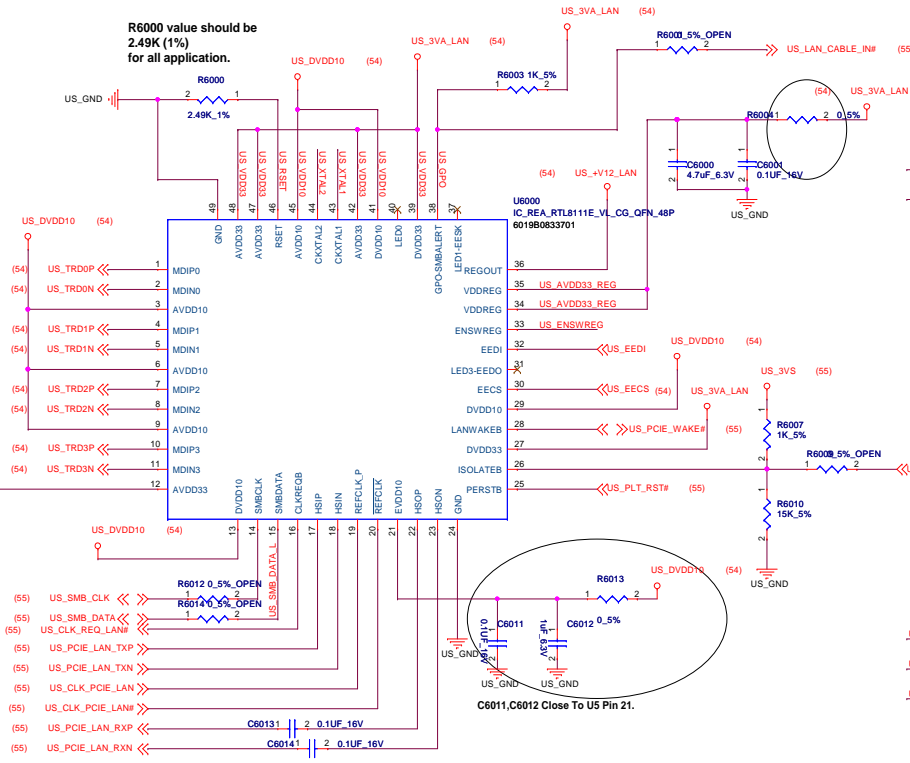
2010.10.06

Thursday, Jun. 26, 2008	1 <sup>st</sup> rd issue	A01
Monday, May 26, 2008	Second issue	A01
Thur., April 17, 2008	First issue	X01
DATE	CHANGE NO.	REV

DRAWER	EE	DATE	POWER	DATE	INVENTEC			
DESIGN					TITLE USB Board			
CHECK								
RESPONSIBLE								
SIZE=					SIZE	CODE	DOC NUMBER	REV
FILE NAME: XXXX-XXXXXX-XX					C	CS	K-CS-1310A22218-ALG	601
PN   XXXXXXXXXX					SHEET	53	of	59

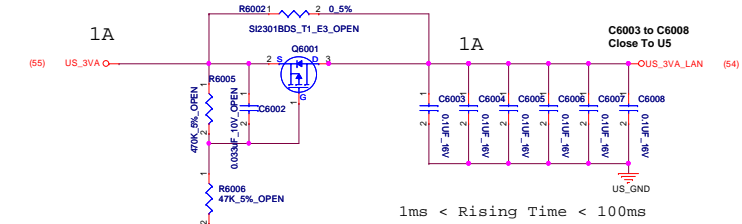
For RTL8111E-VB  
\* C6003 to C6008 are for VDD33 pins-- 12, 27, 39, 42, 47, 48.

R6000 value should be 2.49K (1%) for all application.



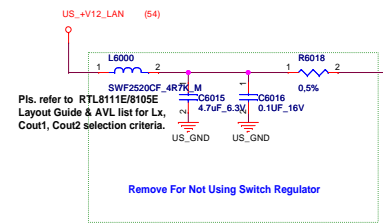
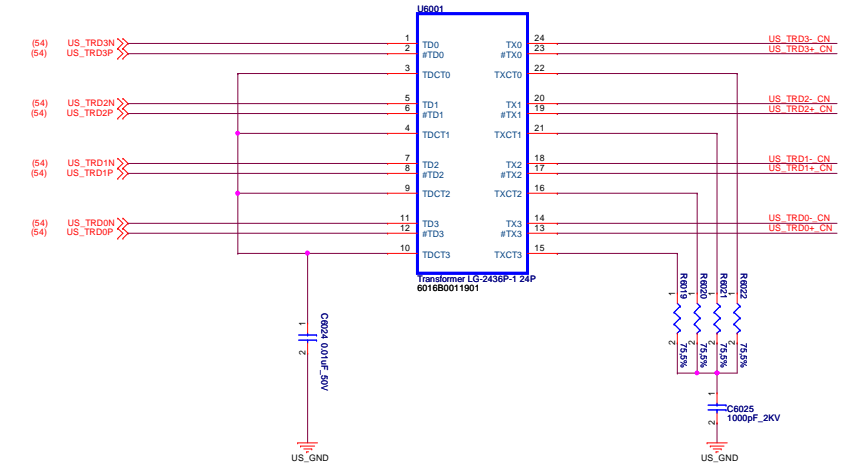
More Detail Layout Pls. Refer to Layout Guide

HIGH: Enable Switching Regulator  
LOW: Disable Switching Regulator

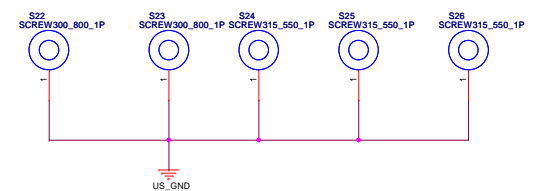
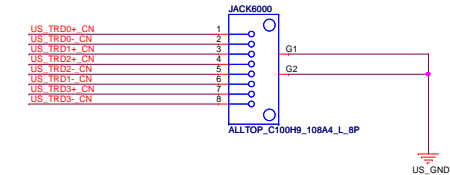


1ms < Rising Time < 100ms

\* C6017 to C6023 are for VDD10 pins-- 3, 6, 9, 13, 29, 41, 45.

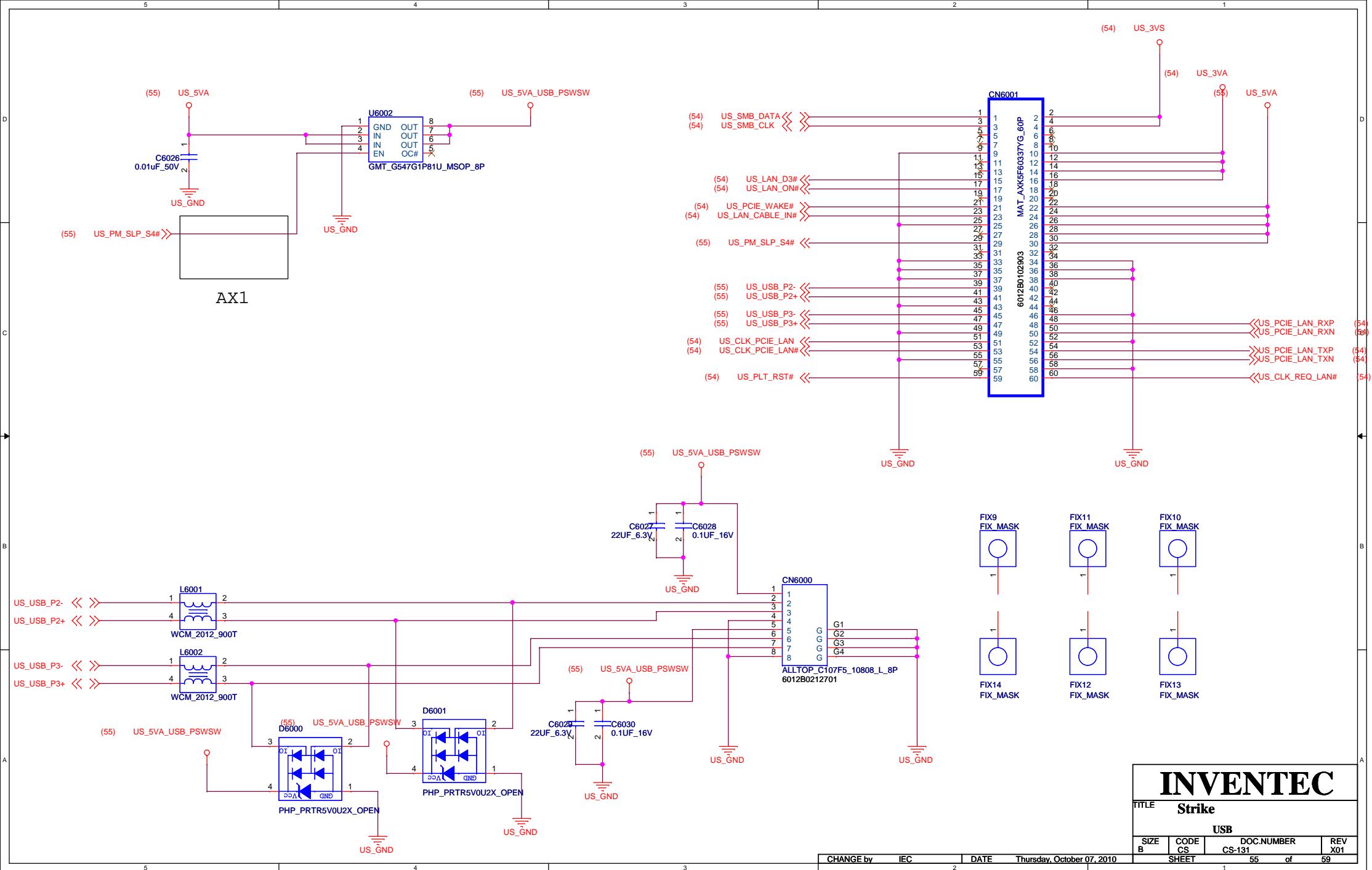


Remove For Not Using Switch Regulator



INVENTEC

Strike  
USB Board/LAN



# Strike

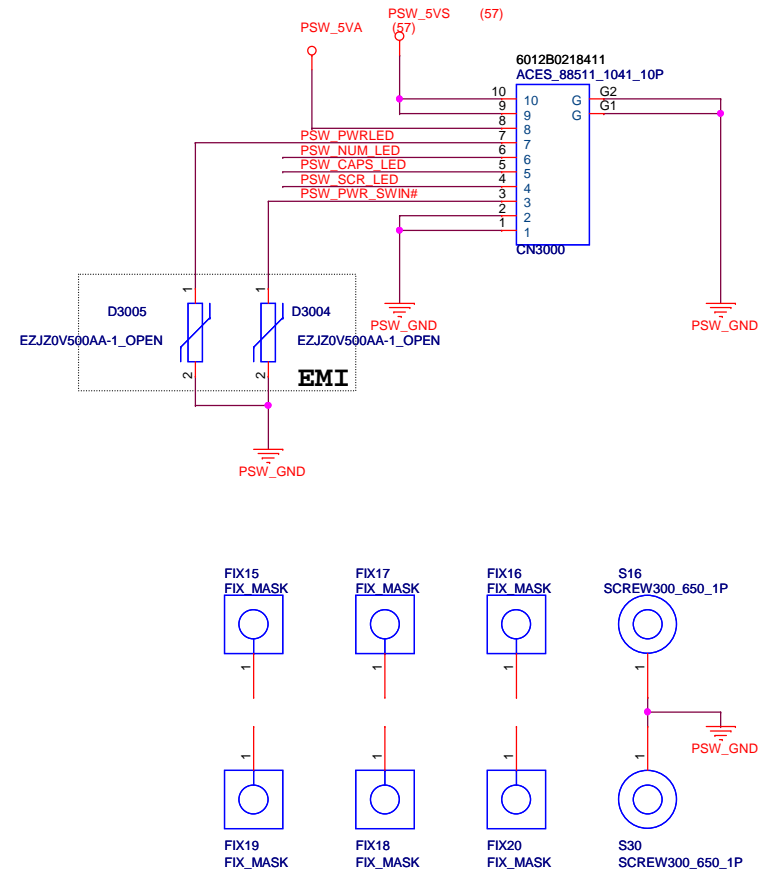
# PWR\_SW BOARD

2010.10.06

Thursday, Jun 26, 2008	1 <sup>st</sup> issue	A01
Monday, May 26, 2008	Second issue	A01
Thur., April 17, 2008	First issue	X01
DATE	CHANGE NO.	REV

DRAWER	EE	DATE	POWER	DATE	INVENTEC			
DESIGN					PWR_SW BOARD			
CHECK								
RESPONSIBLE								
SIZE=					SIZE	CODE	DOC NUMBER	REV
FILE NAME: XXXX-XXXXXX-XX					C	CS	K-CS-1310A22218-ALG	601
PN   XXXXXXXXXX					SHEET	56	of	59





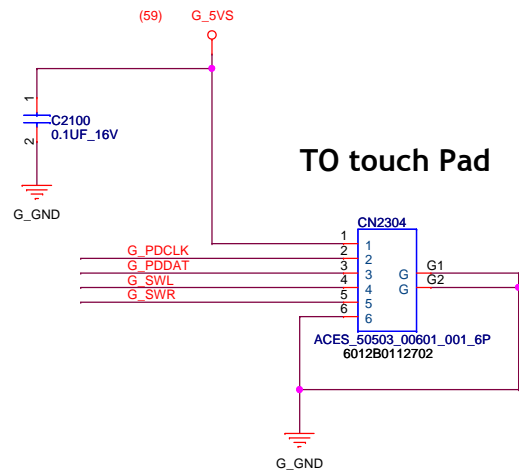
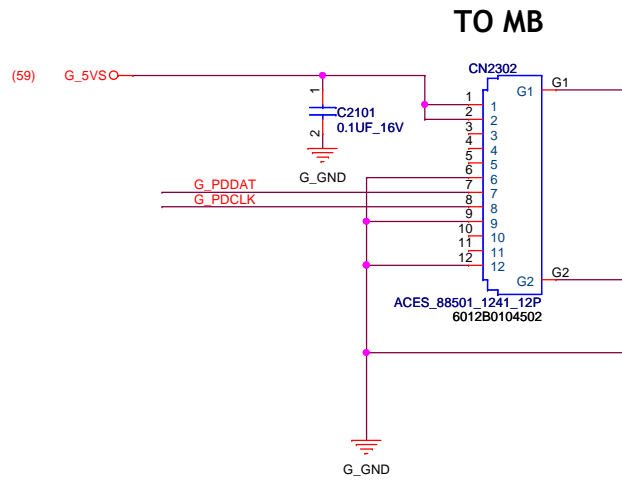
CHANGE by	BEN LEE	DATE	Thursday, October 07, 2010
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# Strike GP board

2010.10.06

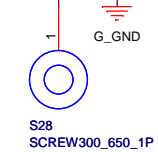
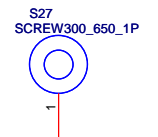
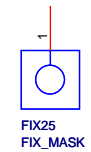
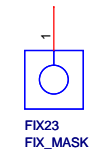
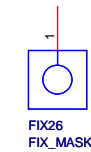
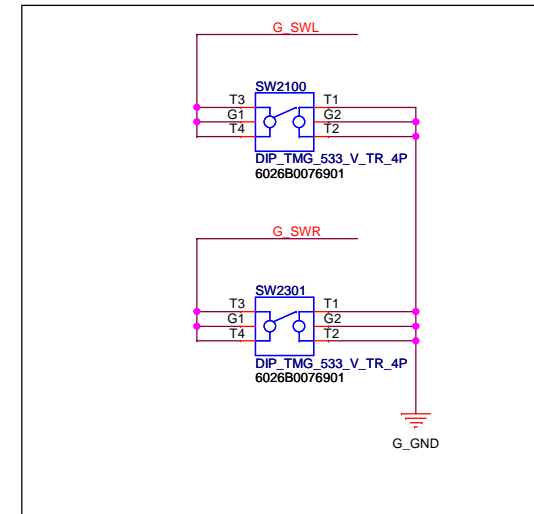
Thursday, October 07, 2010	CHANGE NO.	REV
DATE		

DRAWER	EE	DATE	POWER	DATE	<b>INVENTEC</b> Strike GP Board			
DESIGN								
CHECK								
RESPONSIBLE								
SIZE=					SIZE	CODE	DOC NUMBER	REV
FILE NAME: XXXX-XXXXXX-XX					C	CS	K-CS-1310A22489	B
PN   XXXXXXXXXX					STRET	SB	d	SB



AX1

## GP Button



# INVENTEC

TITLE			
Strike GP CNN			
SIZE	CODE	DOC NUMBER	REV
B	CS	K-CS-1310A22499	C
SHEET		59 of 59	

CHANGE by BEN LEE DATE Thursday, October 07, 2010