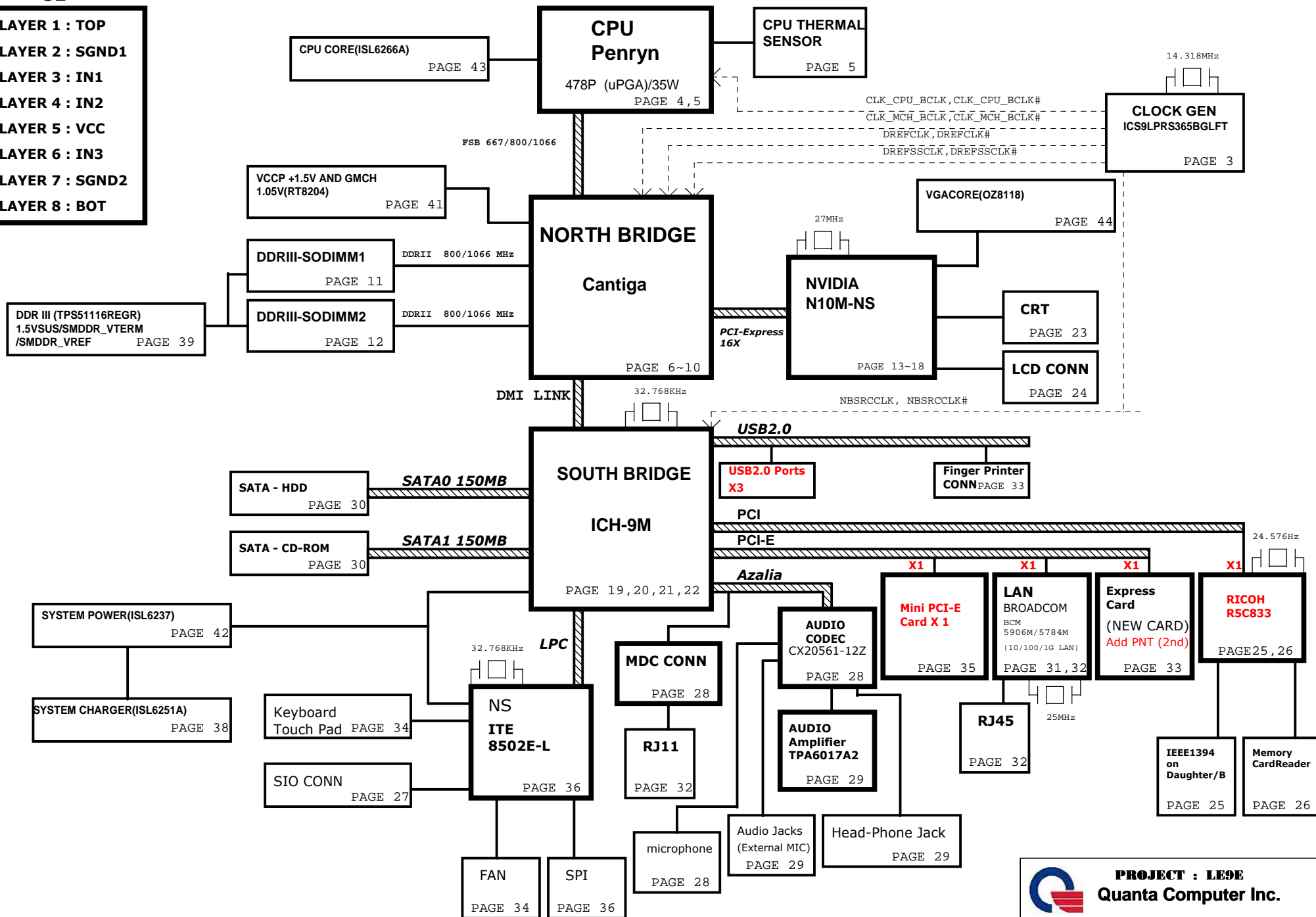


PCB STACK UP 8L

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT

LE9E BLOCK DIAGRAM

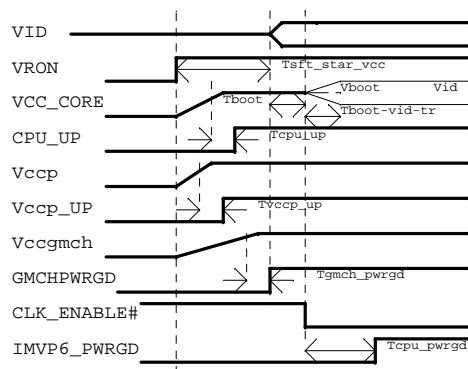
01



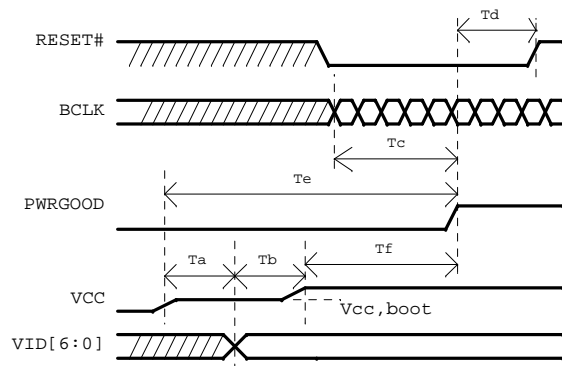
PCB Layers

Layer 1		TOP
Layer 2		GND
Layer 3		IN1
Layer 4		IN2
Layer 5		SVCC
Layer 6		IN3
Layer 7		GND
Layer 8		BOTTOM

Power On Sequencing Timing Diagram



MEROM Power-up Timing Specifications



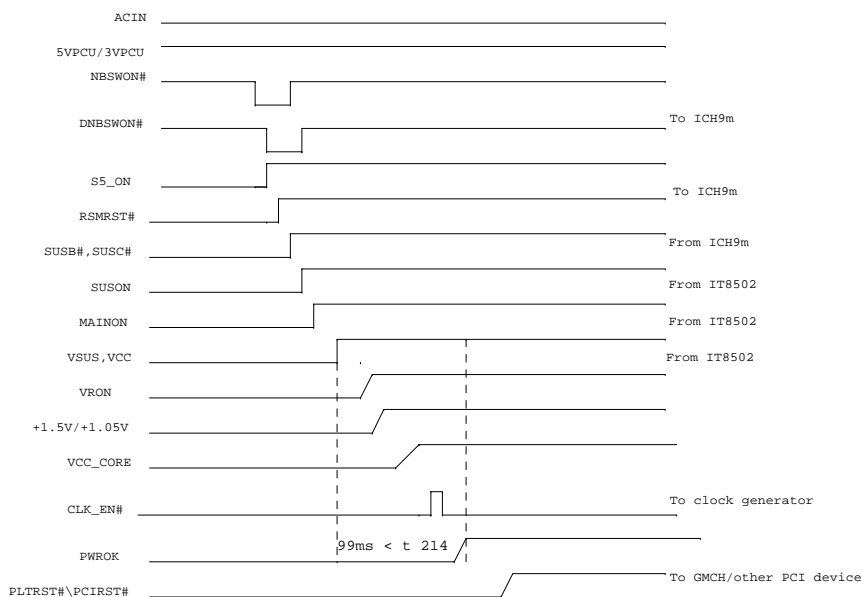
+1.05V

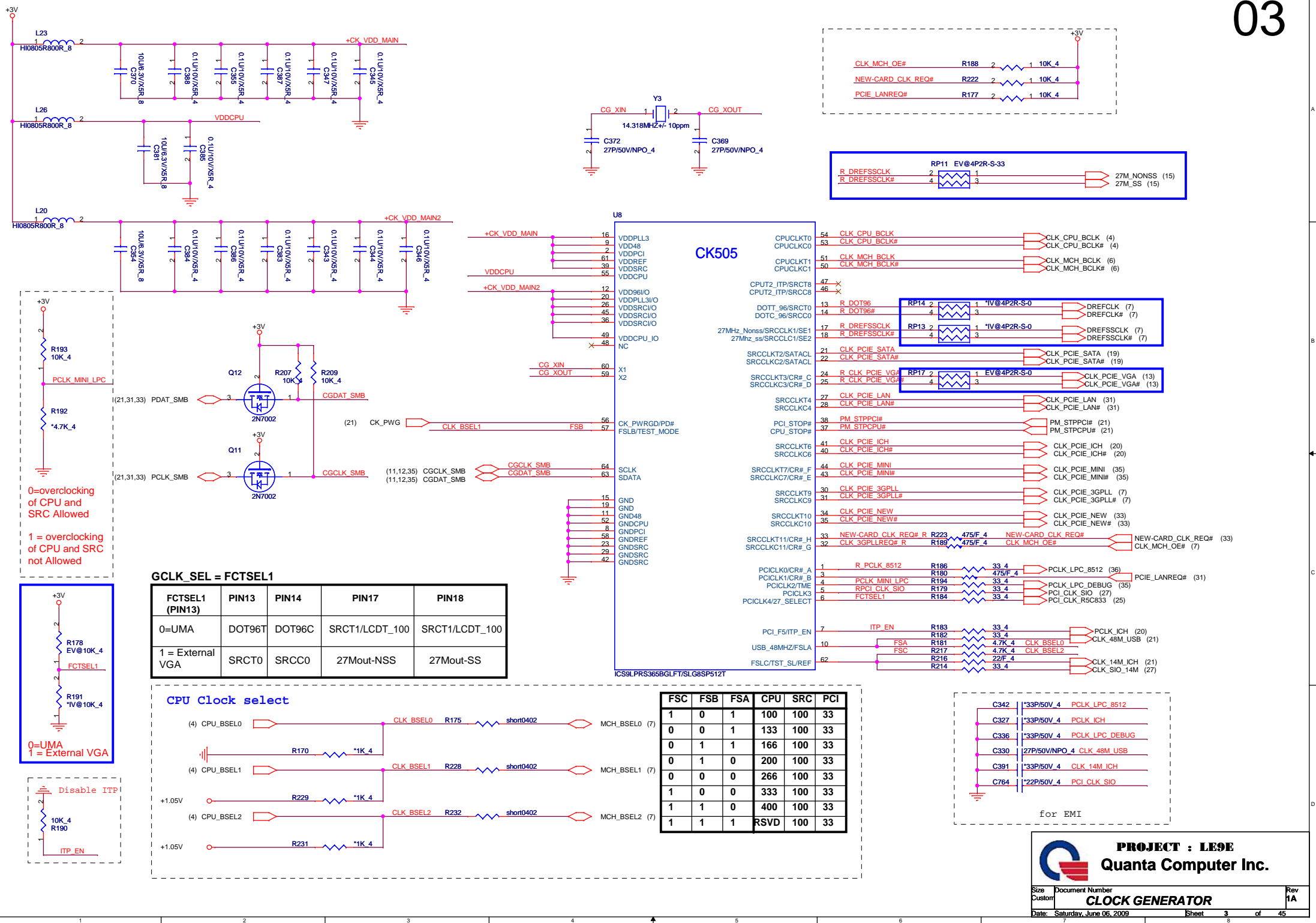
Ta=VCC and VCCP assertion to VID[6:0] valid
Tb=VID[6:0] stable to VCC valid
Tc=BCLK stable to PWRGOOD assertion
Td=PWRGOOD to RESET# de-assertion time
Te=Vcc,boot valid to PWRGOOD assertion time

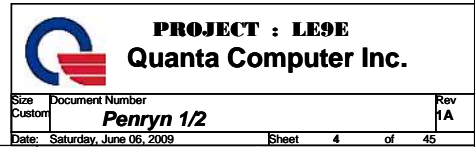
Voltage Rails

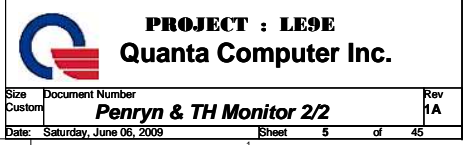
Voltage Rails	ON S0-S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	X				VRON
+1.5V	X				MAINON
+1.05V	X				MAINON
5V_S5/3V_S5	X	X	X	X	S5_ON
5VSUS/3VSUS/1.5VSUS	X	X			SUSON
SMDDDR_VTERM/+3V/+5V/+15V/+1.8V	X				MAINON
+VGACORE/+VGA1.1V	X				MAINON
LANVCC	X	X	X	X	LAN_ON
3VPCU	X	X	X	X	VL
5VPCU	X	X	X	X	VL

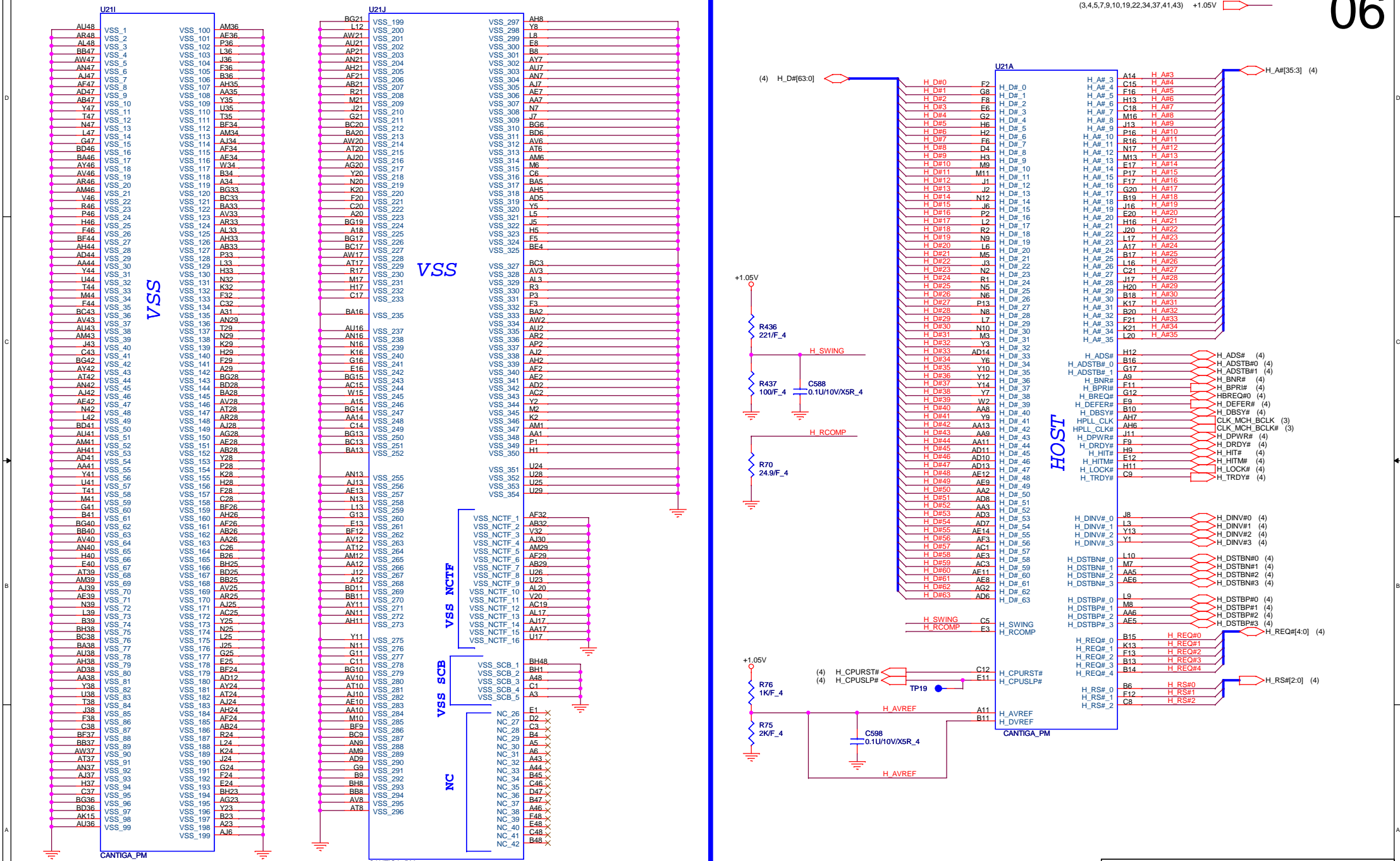
ACIN POWER ON TIMING



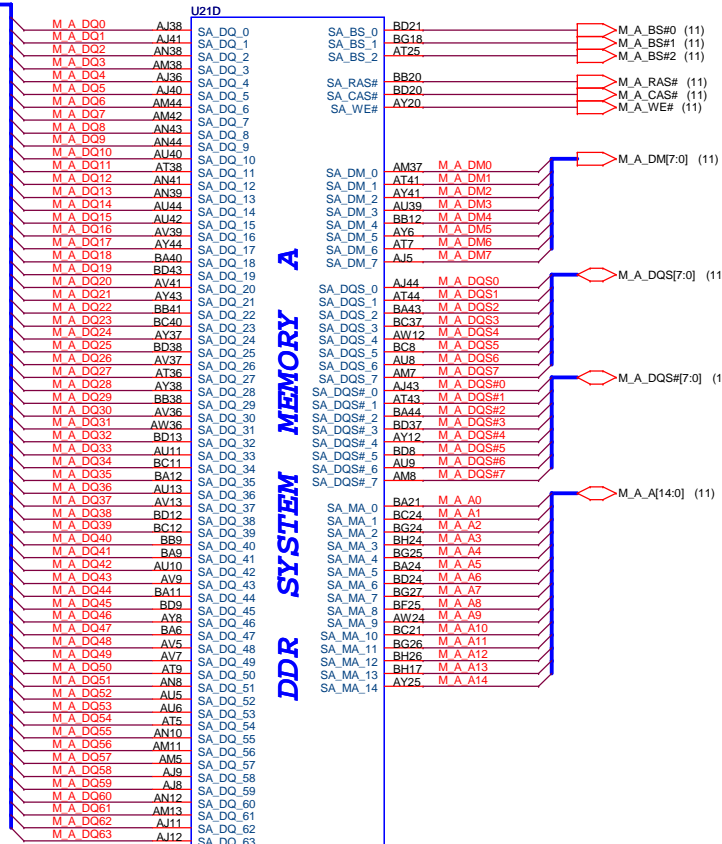




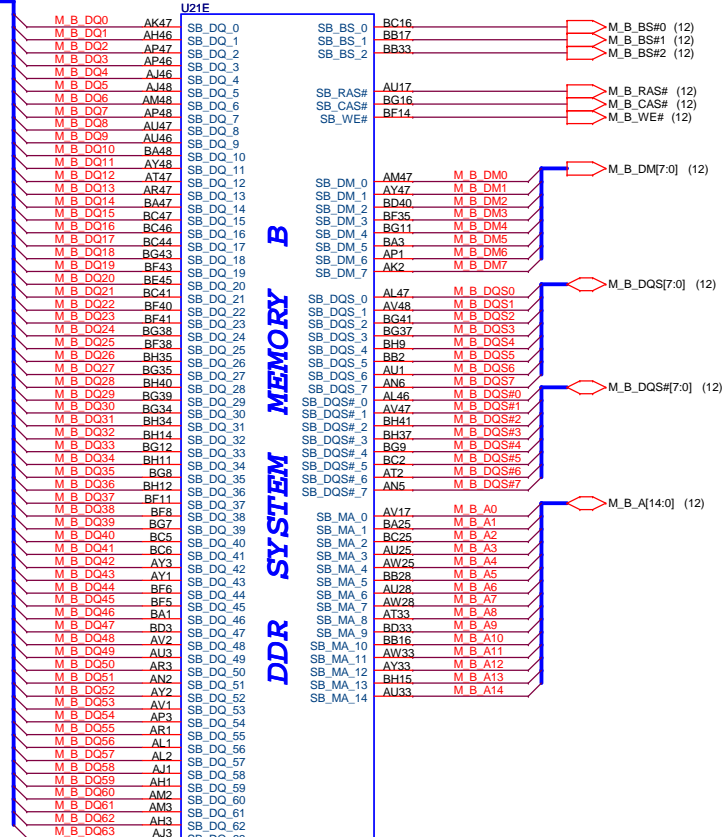




(11) M_A_DQ[63:0]

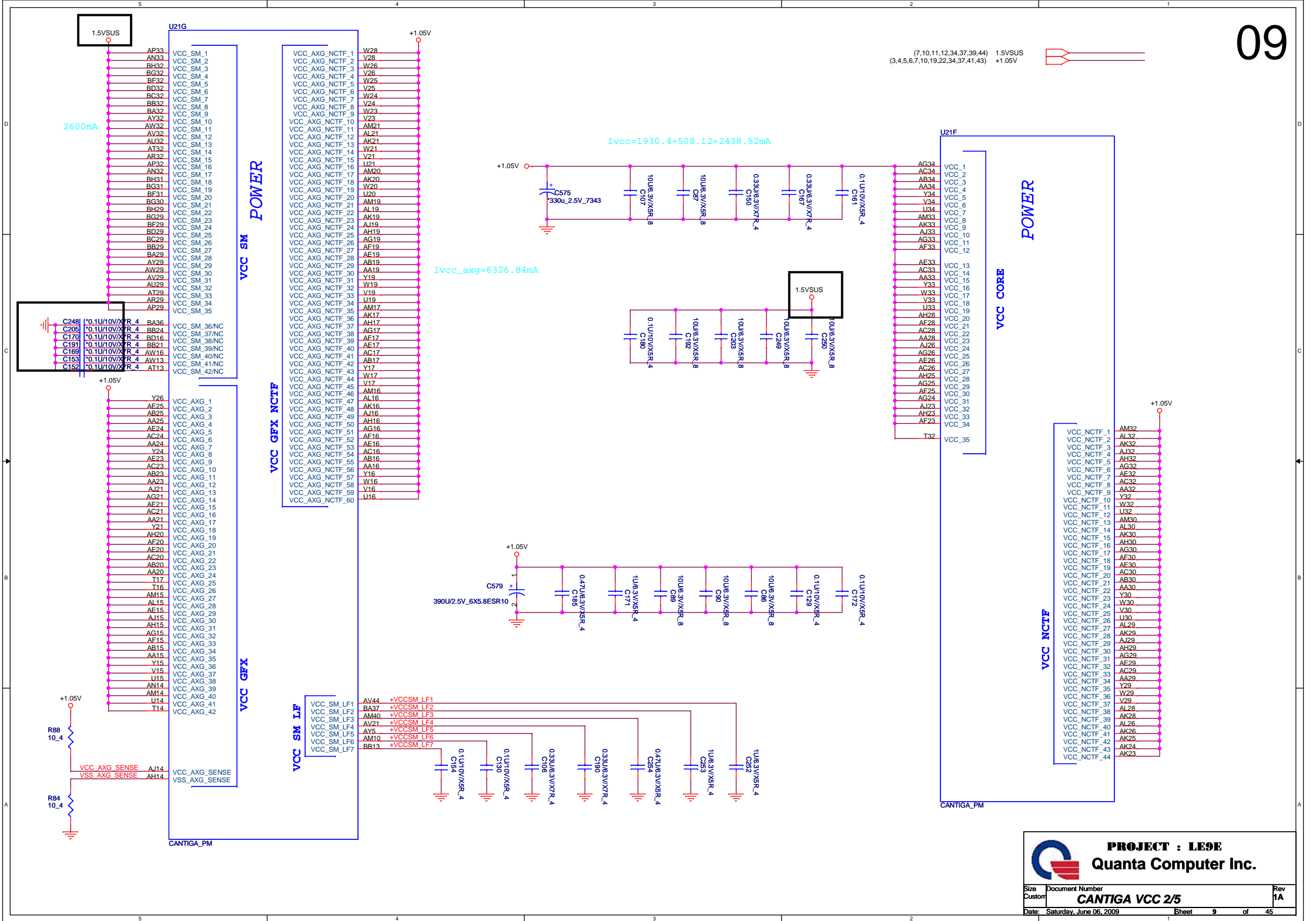


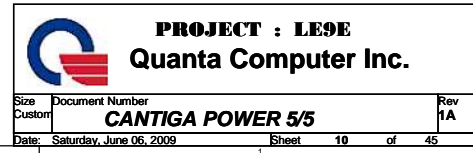
(12) M_B_DQ[63:0]

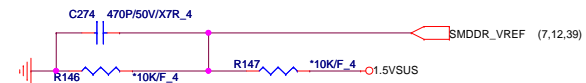
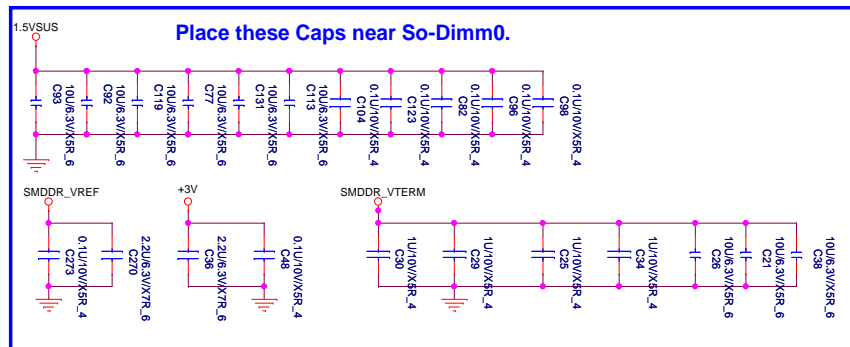
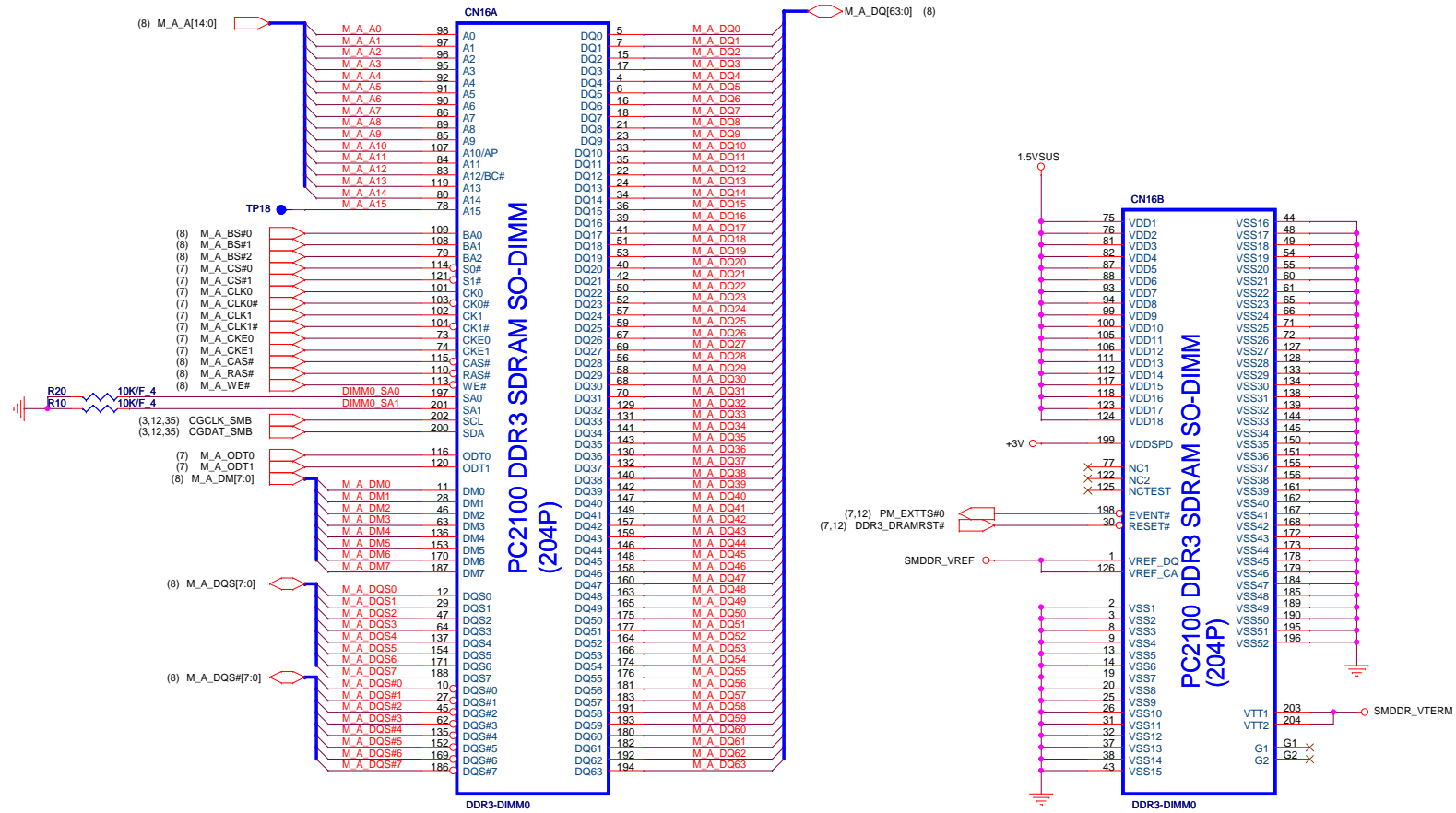


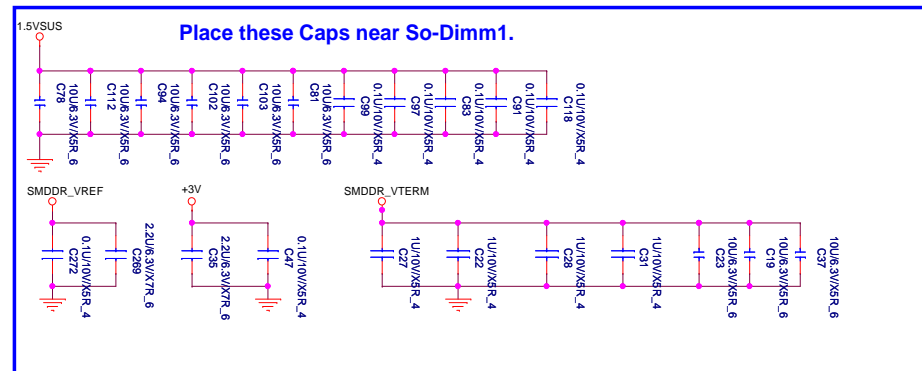
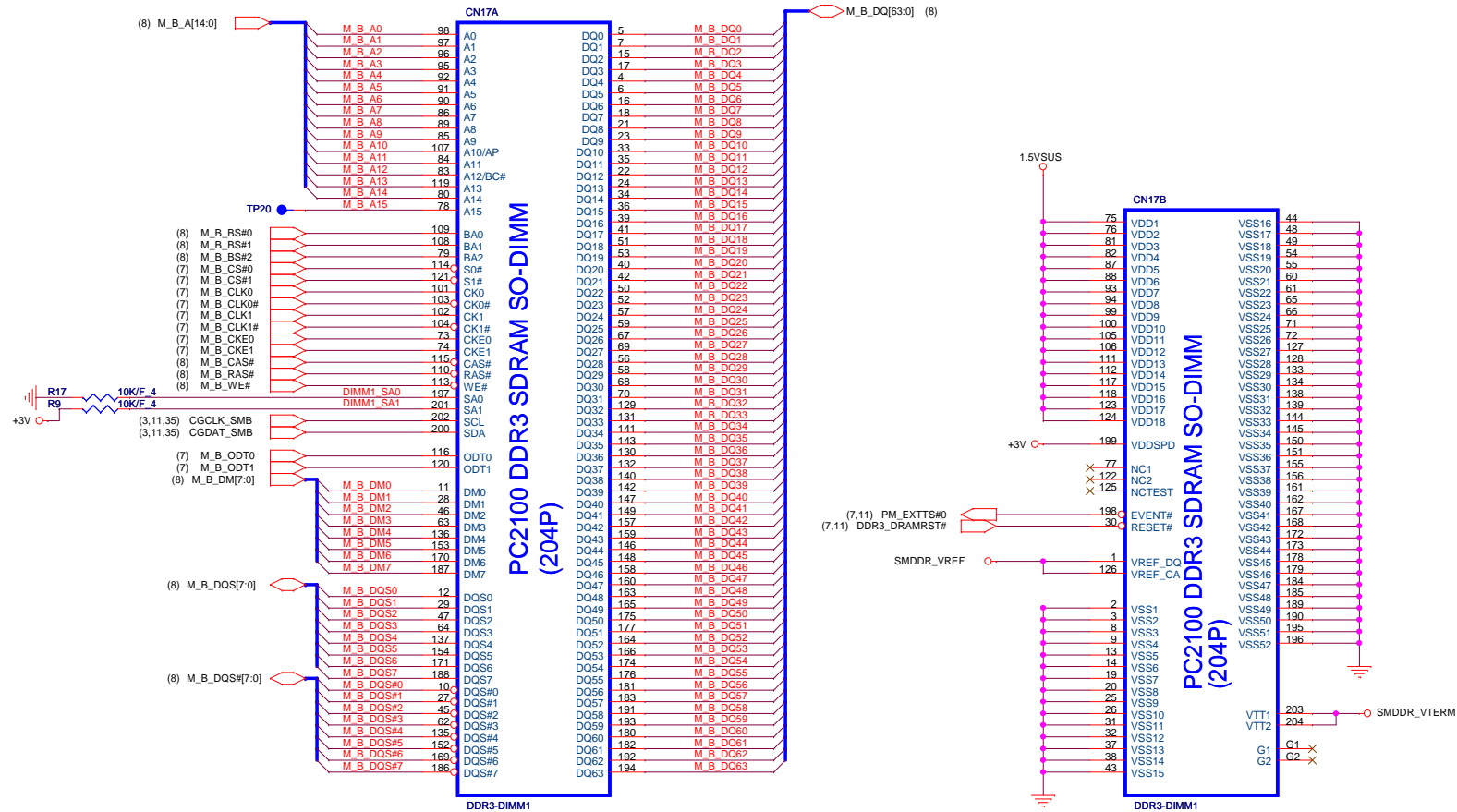
PROJECT : LE9E
Quanta Computer Inc.

(7,10,11,12,34,37,39,44) 1.5VSUS
(3,4,5,6,7,10,19,22,34,37,41,43) +1.05V

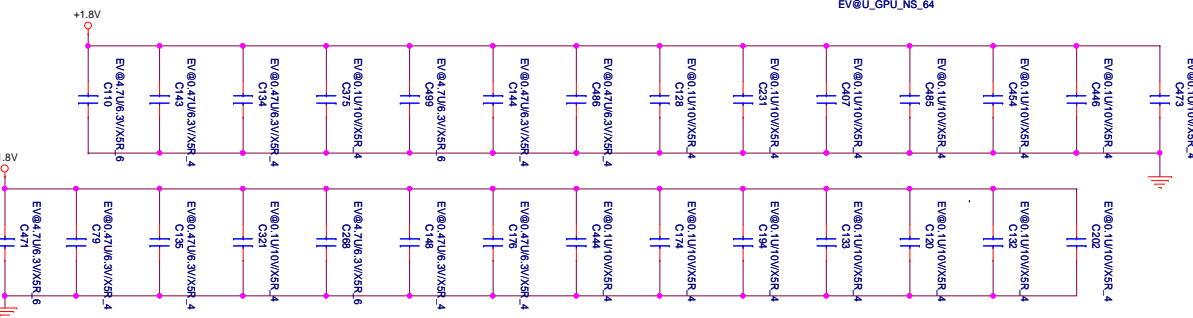
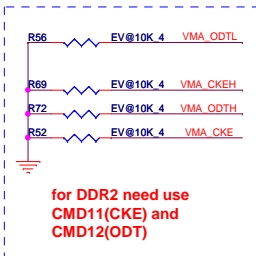
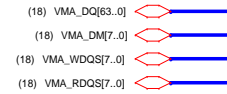
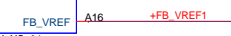
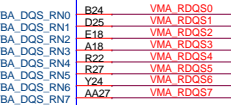
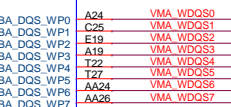
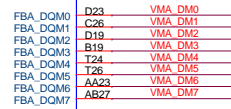
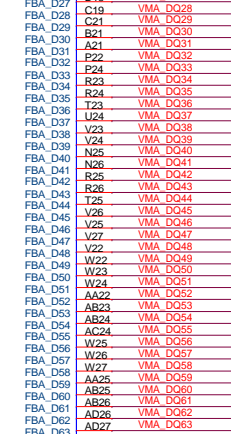
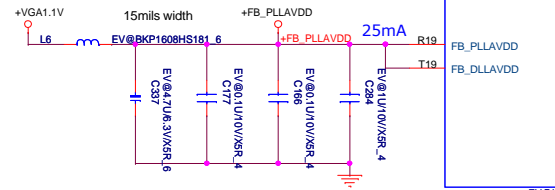
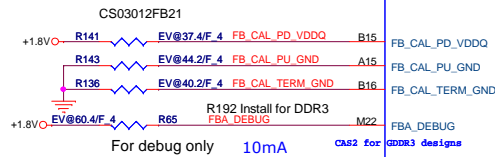
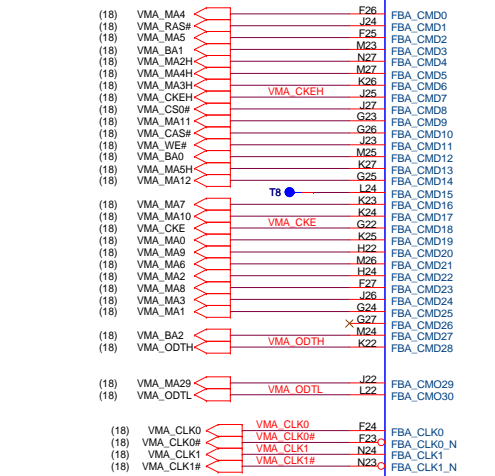


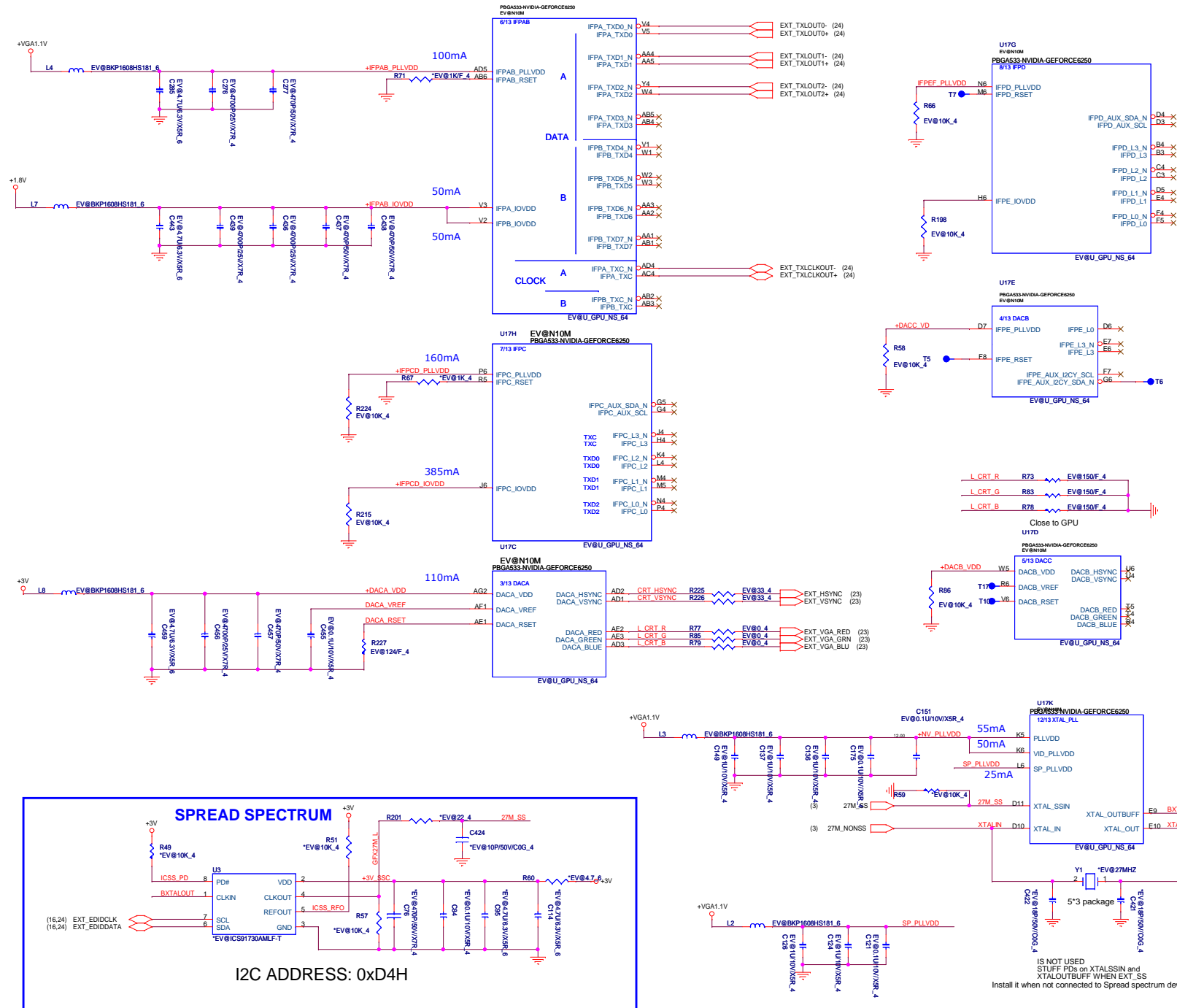


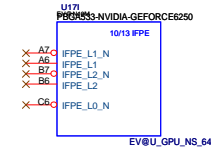
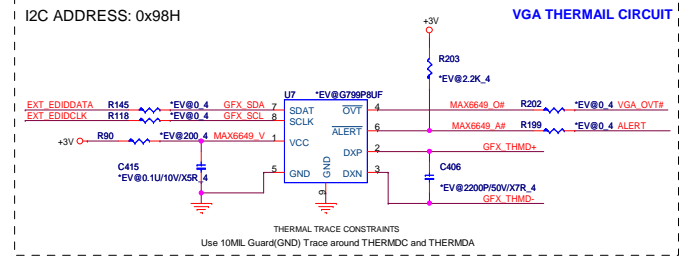
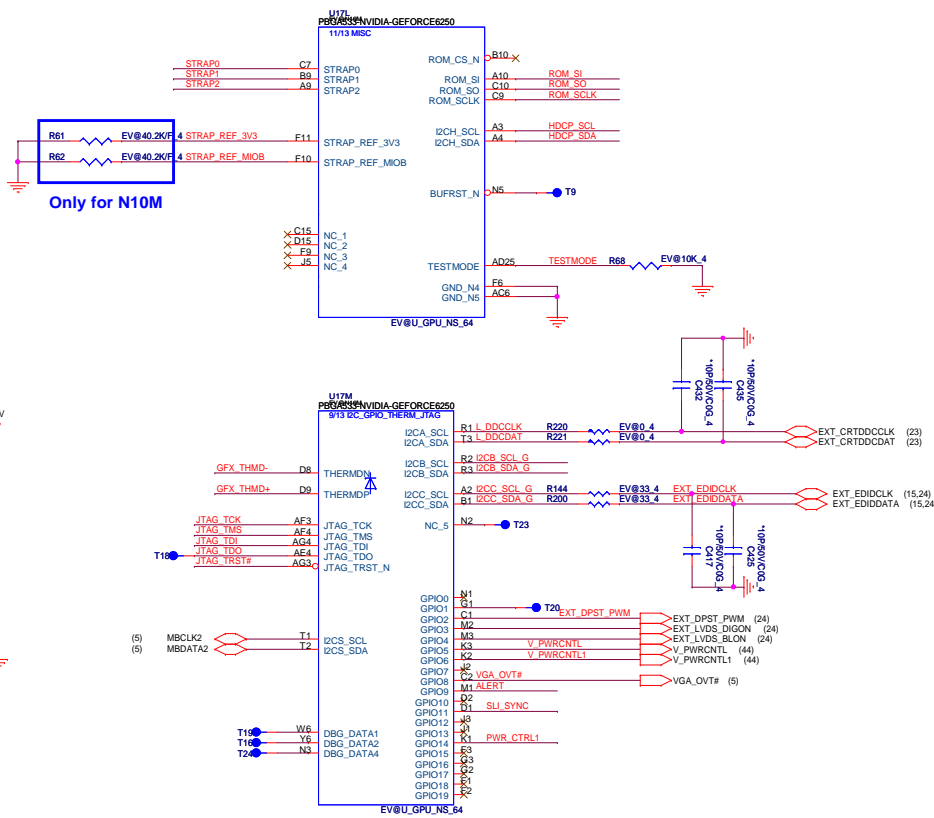




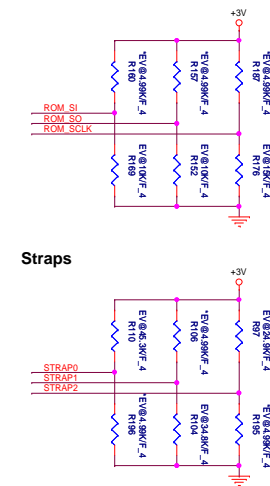








PCI_DEVID[4] / SUBVENDOR



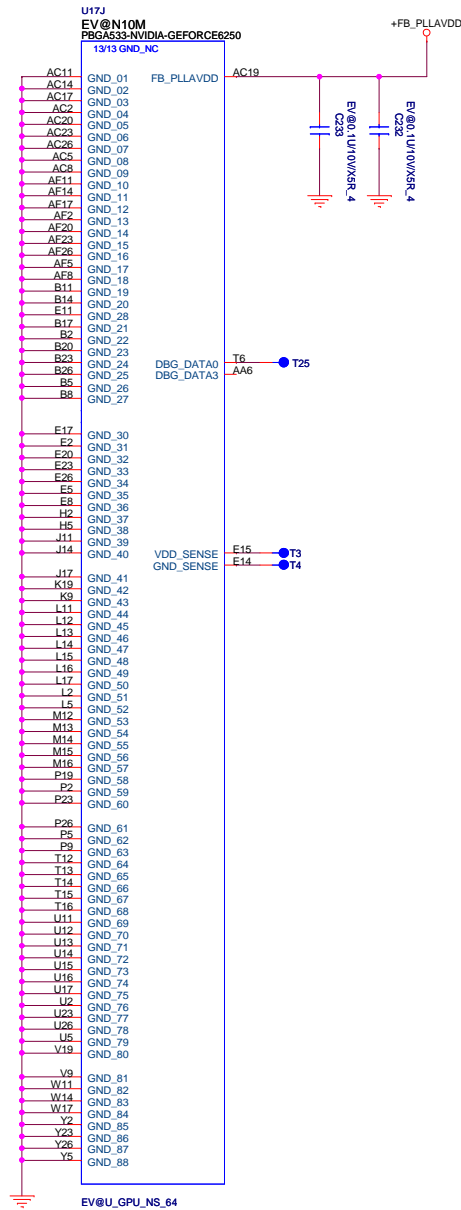
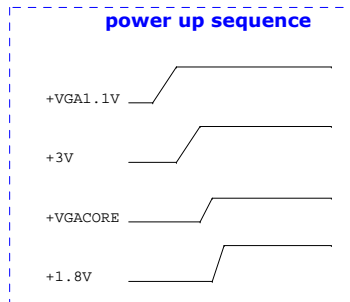
Logical Strap Bit Mapping

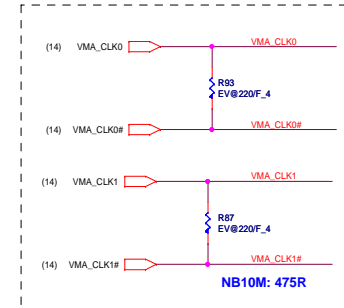
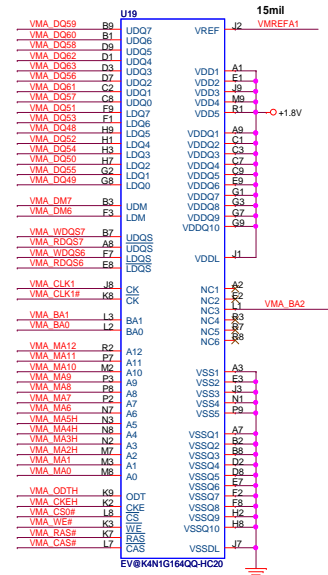
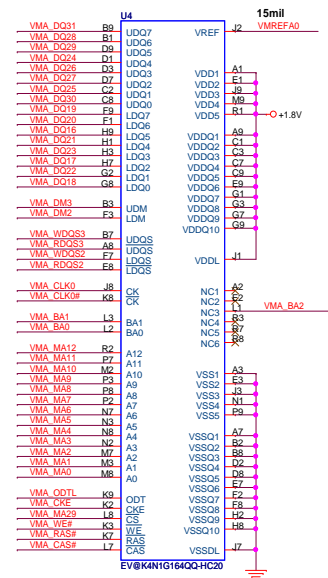
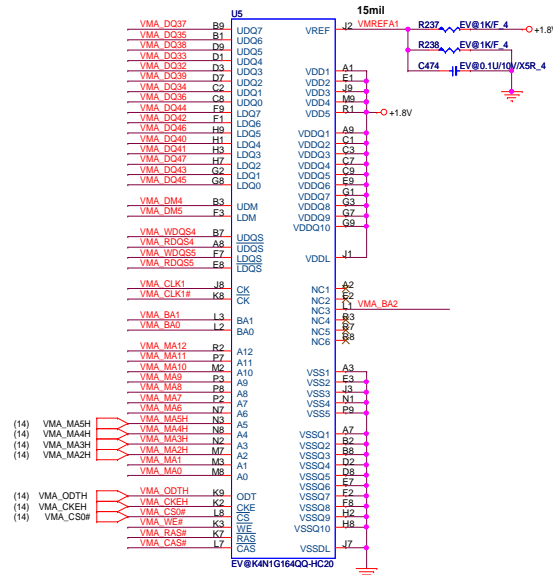
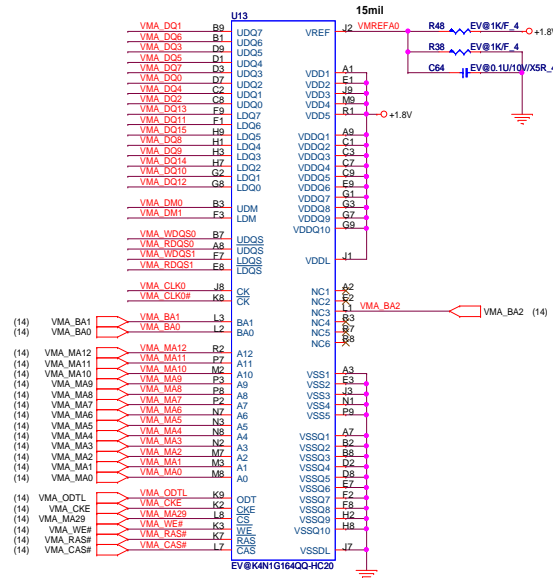
	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPIO ASSIGNMENTS

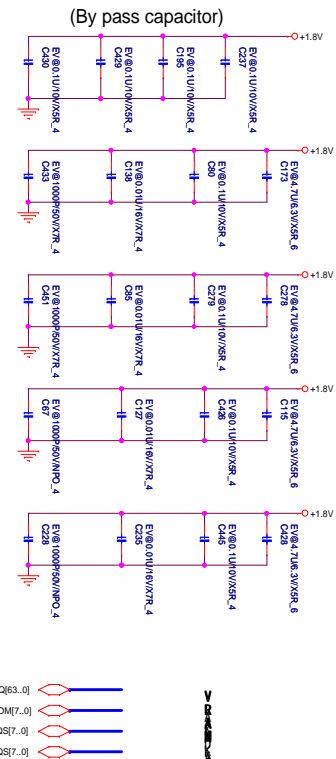
GPIO	NB9X	N10X	I/O	ACTIVE	Function Description
0	General Purpose	General Purpose	I/O	N/A	
1	HPD-C	HPD-C	I	N/A	Hot Plug Detect for IFP Link C
2	LCD0_BL_PWM	LCD0_BL_PWM	O	H	Panel Backlight Brightness Control (PWM Capable)
3	LCD0_VDD	LCD0_VDD	O	H	Panel Power Enable
4	LCD0_BL_PWM	LCD0_BL_PWM	O	H	Panel Backlight ON/OFF
5	GPU_VID0	GPU_VID0	O	N/A	GPU_VID0
6	GPU_VID1	GPU_VID1	O	N/A	GPU_VID1
7	GPU_VID2/MEM_VID	GPU_VID2	O	N/A	GPU_VID2
8	OVERT	OVERT	I/O	L	Thermal Over Temperature
9	FAN_PWM/ALERT	ALERT	I/O	L	Thermal Alert (PWM Capable)
10	MEM_VREF	MEM_VREF	O	N/A	Memory VREF Switch
11	SLI_SYNC	SLI_SYNC	I/O	L	SLI SYNC0
12	AC_DET	PWR_LEVEL (in)	I	N/A	Power Level Detect
13	PWR_CTRL0	MEM_VID (out)	O	L	MEM_VID0
14	PWR_CTRL1	PWR_CTRL1	O	N/A	Power Supply Control
15	HPD-E	HPD-E	I	N/A	Hot Plug Detect for IFP Link E
16	DVI_MODE1	FAN_PWM(out)	O	N/A	Fan PWM Control
17	HDMI_DETECT0	Reserved	N/A	N/A	
18	DVI_MODE1	Reserved	N/A	N/A	
19	HDMI_DETECT1	HPD-D	I	N/A	Hot Plug Detect for IFP Link D

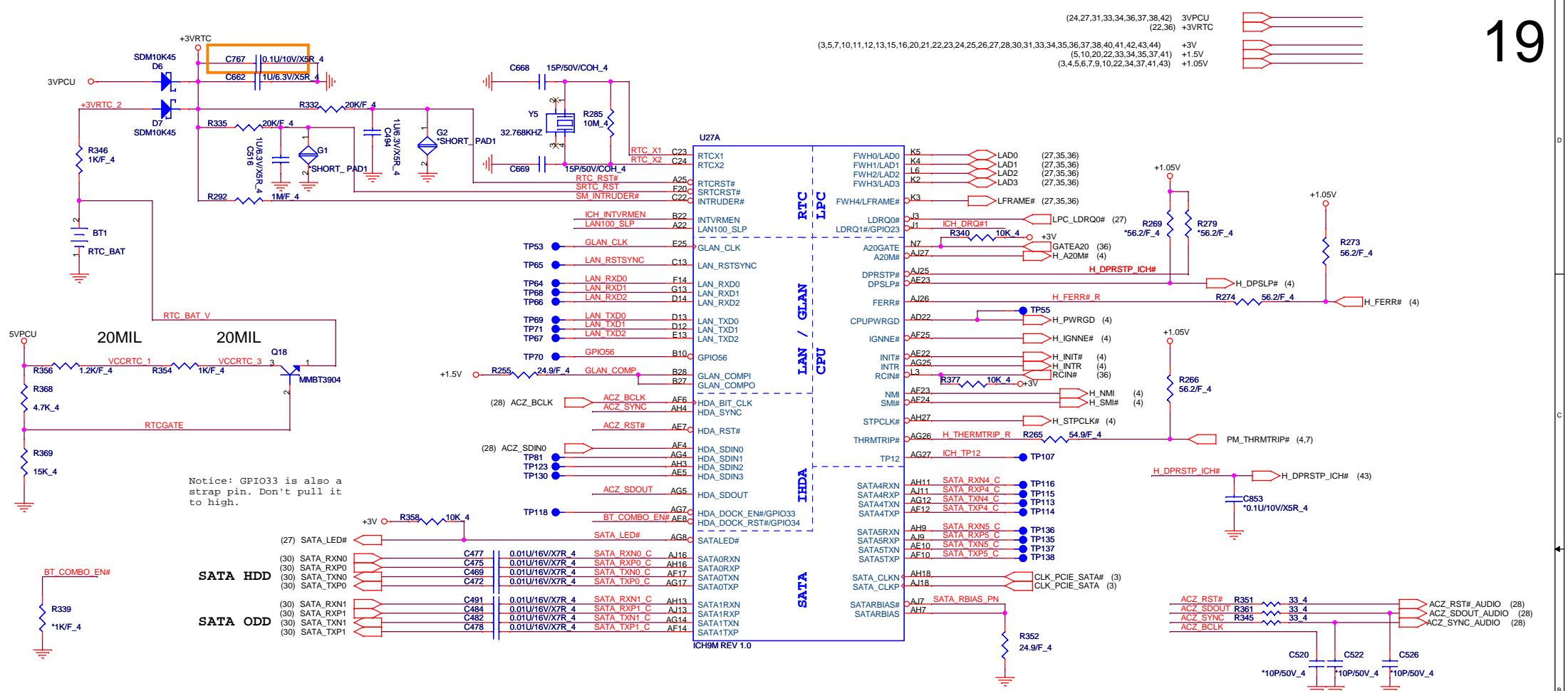
Starps	NB9X	N10X	Function Description
ROM_SO	XCLK 277 TVMODE(2) TVMODE(0)	XCLK 277 TVMODE(2) TVMODE(1) TVMODE(0)	55nm PU 5K/F ohm 40nm PD 10K/F ohm
ROM_SCLK	PCI DEVID EXT SUB_VENDOR SLOT_CLK_CFG PEX_PLL_EN_TERM	PCI DEVID EXT SUB_VENDOR SLOT_CLK_CFG PEX_PLL_EN_TERM	55nm/40nm PD 15K/F ohm
ROM_SI	RAMCFG(3) RAMCFG(2) RAMCFG(1) RAMCFG(0)	RAMCFG(3) RAMCFG(2) RAMCFG(1) RAMCFG(0)	Hynix PD 5K/F ohm Samsung PD 10K/F ohm Qimonda PD 15K/F ohm/ No 40nm use
Strap 2	PCI DEVID(3) PCI DEVID(2) PCI DEVID(1) PCI DEVID(0)	PCI DEVID(3) PCI DEVID(2) PCI DEVID(1) PCI DEVID(0)	55nm PU 25K/F ohm 40nm GS PU 10K/F ohm 40nm/NS PU 5K/F ohm 40nm/NS PU 25K/F ohm
Strap 1	3GIO PADCFG(3) 3GIO PADCFG(2) 3GIO PADCFG(1) 3GIO PADCFG(0)	3GIO PADCFG(3) 3GIO PADCFG(2) 3GIO PADCFG(1) 3GIO PADCFG(0)	40nm/NS PU 34.9K/F ohm
Strap 0	USER(3) USER(2) USER(1) USER(0)	USER(3) USER(2) USER(1) USER(0)	





CS14752FB11 RES CHIP 475 1/16W +-1%(0402)





SB Strap

ICH9-M Internal VR Enable strap
(Internal VR for VccSus1_05, VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
----------	---

ICH9-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1_05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
------------	---

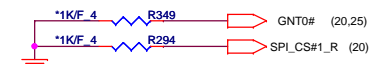
XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)



A16 swap override strap

PCI_GNT#3	Low = A16 swap override enabled Hi = Default
-----------	---



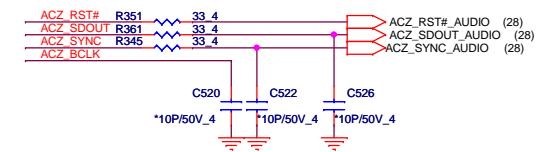
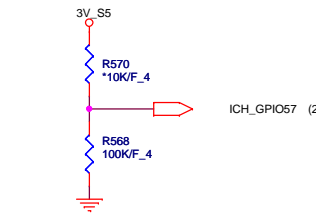
No Reboot Strap

ACZ_SPKR	Low: Default Hi: No reboot
----------	-------------------------------



TPM physical presence

ICH_GPIO57	Low: Default
------------	--------------



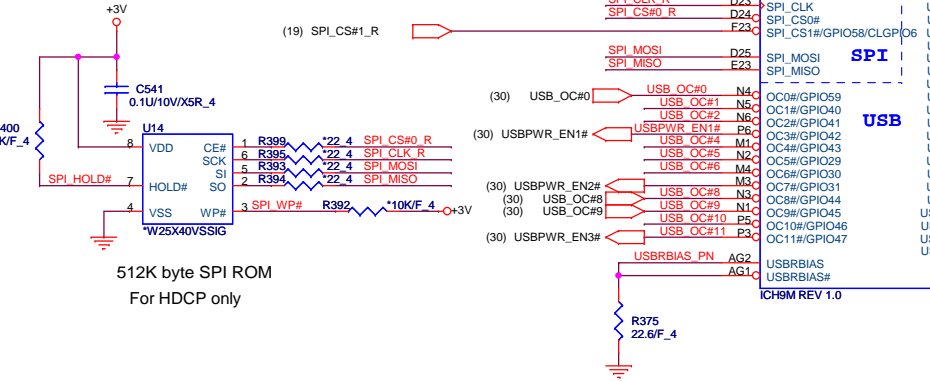
(5,10,19,22,33,34,35,37,41) +1.5V
(3,5,7,10,11,12,13,15,16,19,21,22,23,24,25,26,27,28,30,31,33,34,35,36,37,38,40,41,42,43,44) +3V
(21,28,33,35,36,37,38,43,44) 3VSUS



EXPRESS CARD (NEW CARD)

MINI CARD PCI-E (WLAN)

PCI-E-LAN



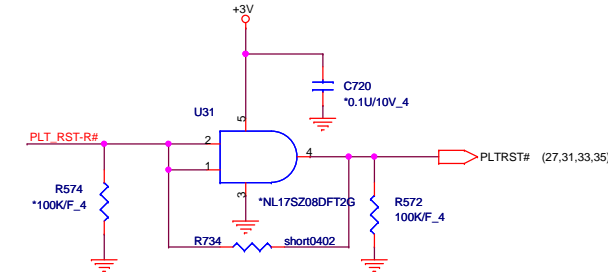
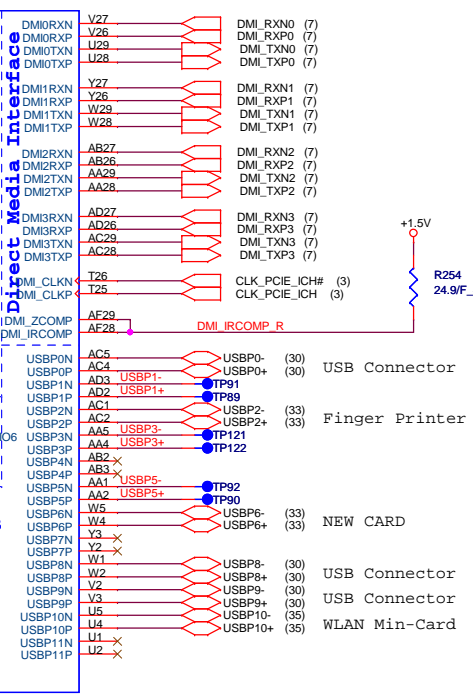
PCI-Express

USB

PCI

Interrupt I/F

ICH9M REV 1.0

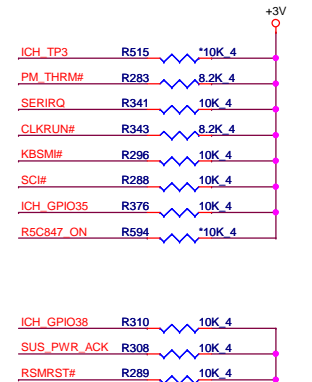
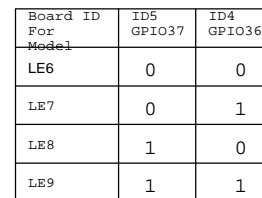
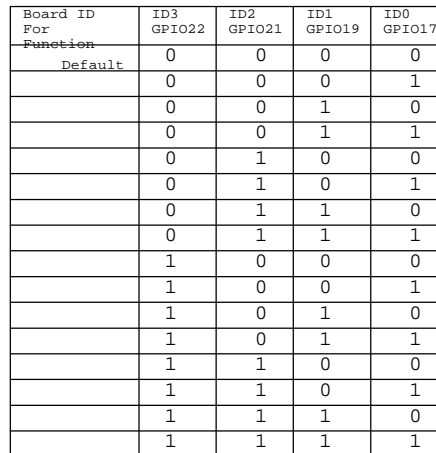
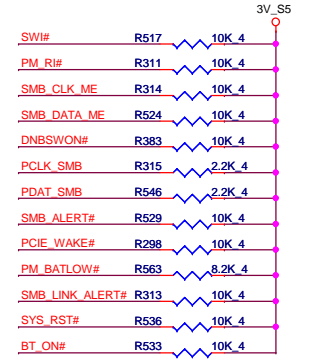


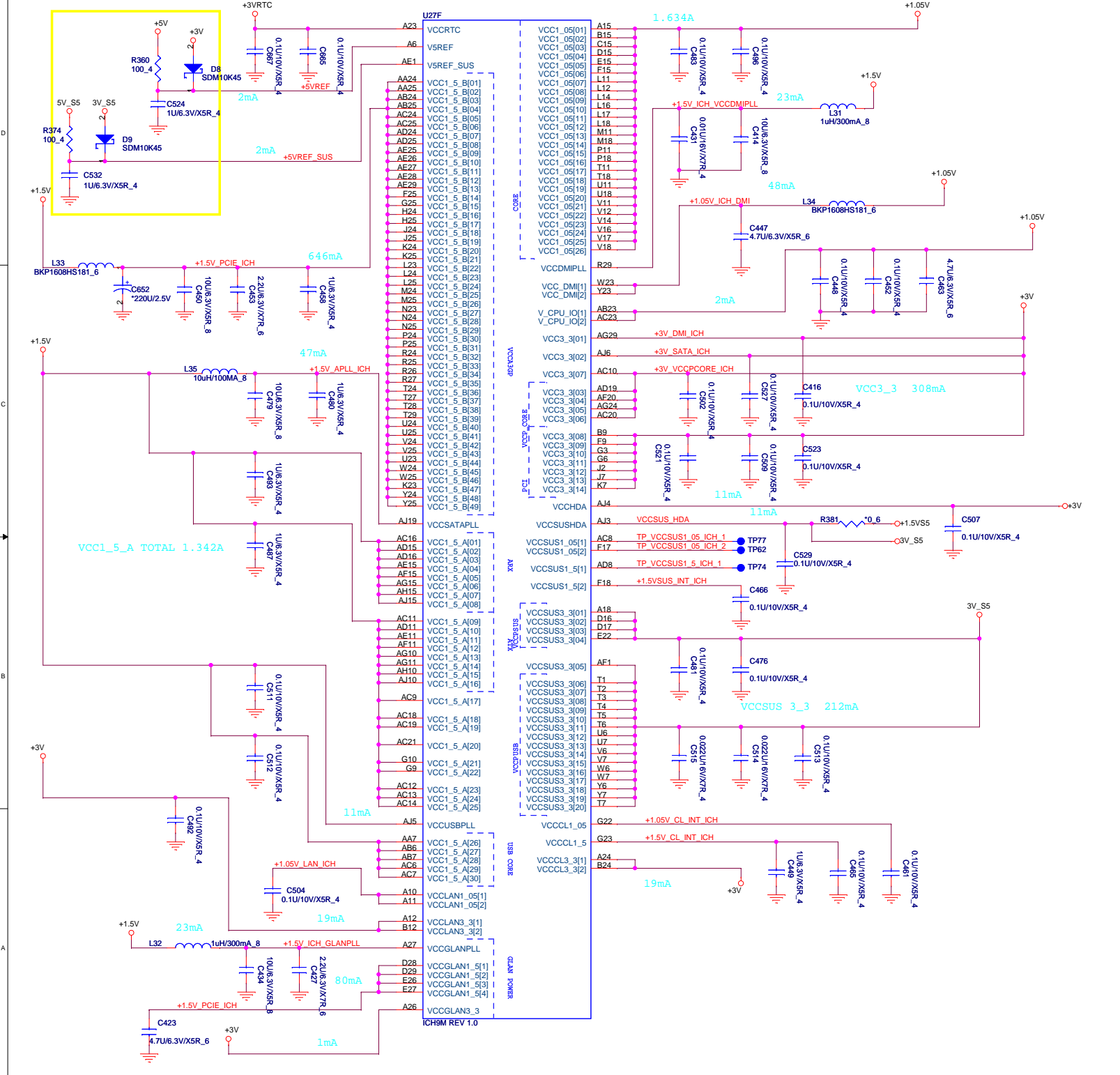
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTE#, F#	RICOH R5C833

PROJECT : LE9E
Quanta Computer Inc.

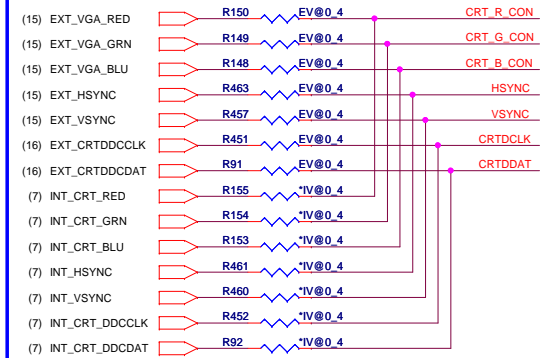
Size Custom Document Number **ICH9-M PCIE 2/4** Rev 1A

Date: Saturday, June 06, 2009 Sheet 20 of 45



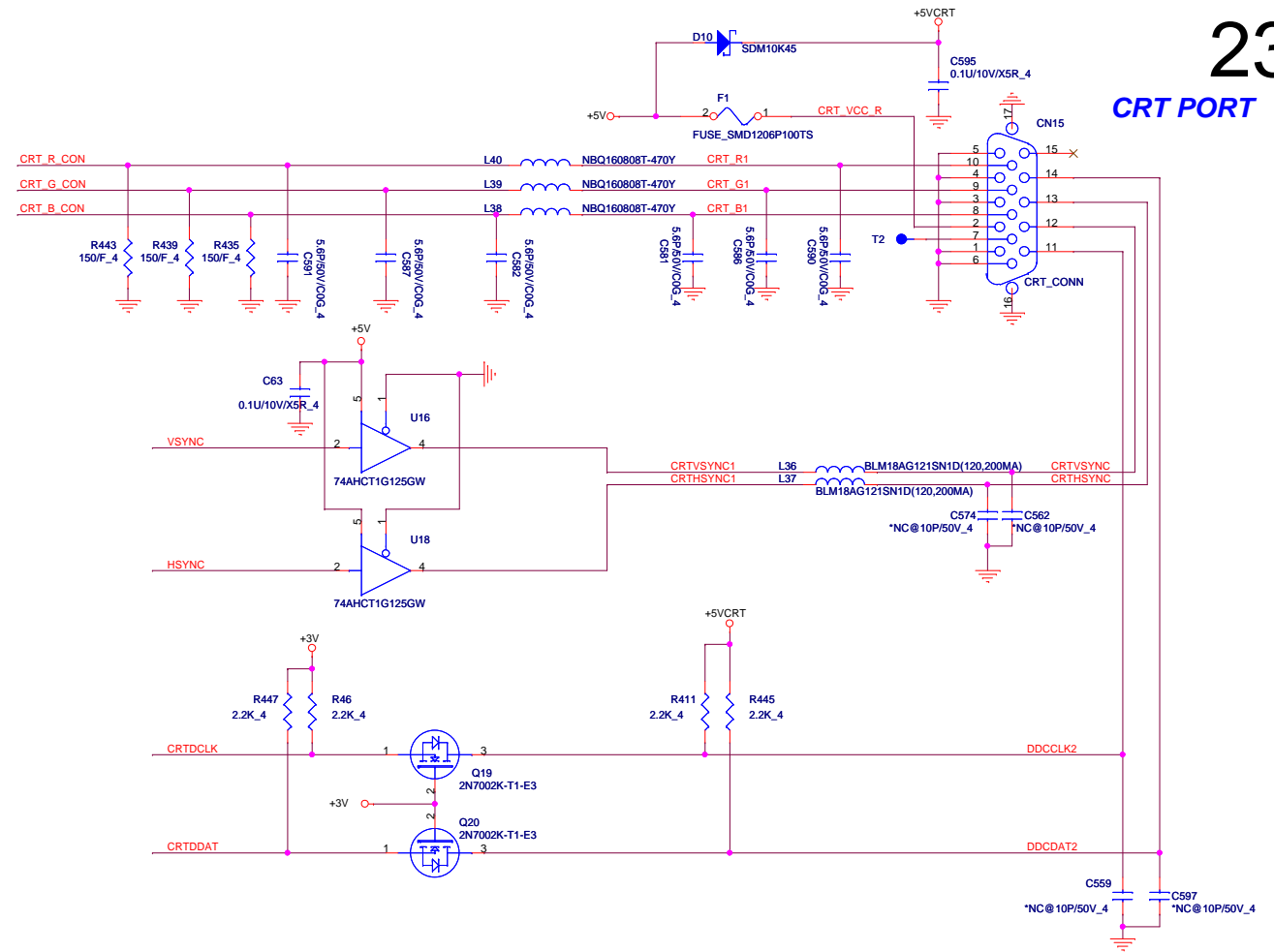


CRT SWITCH

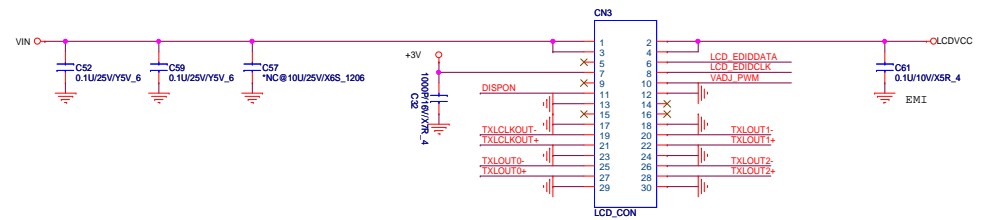
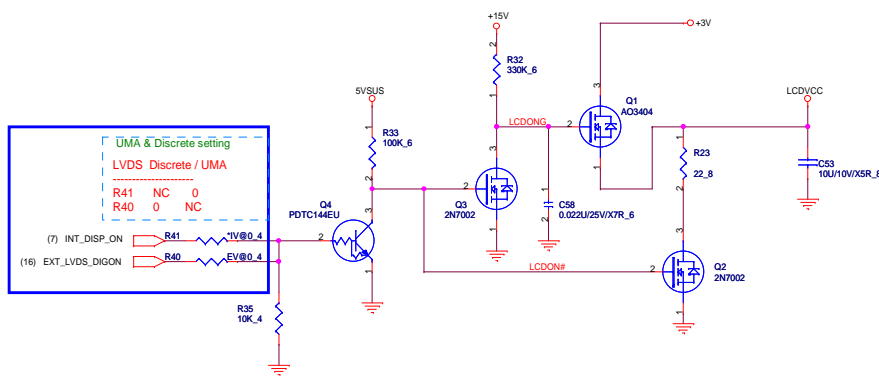
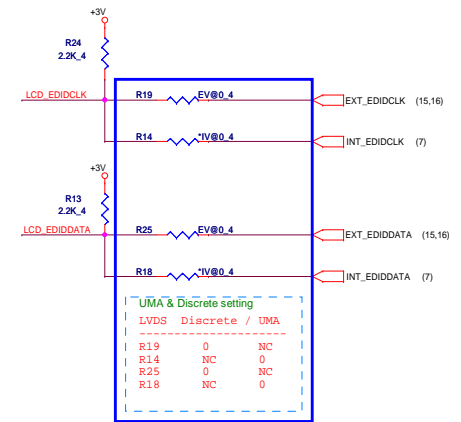
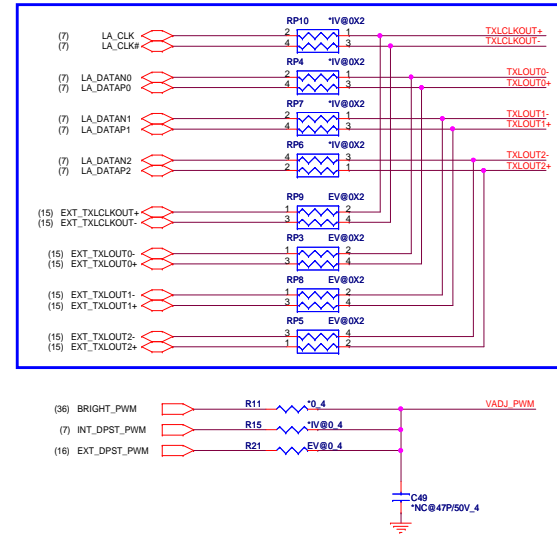
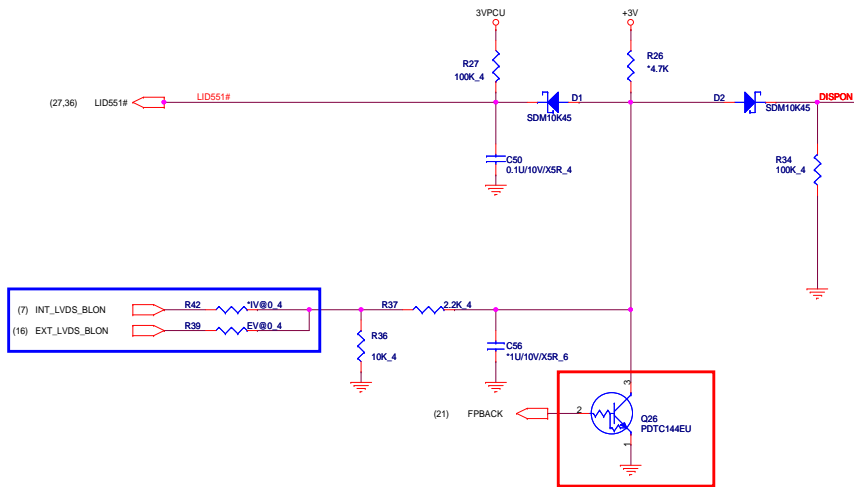


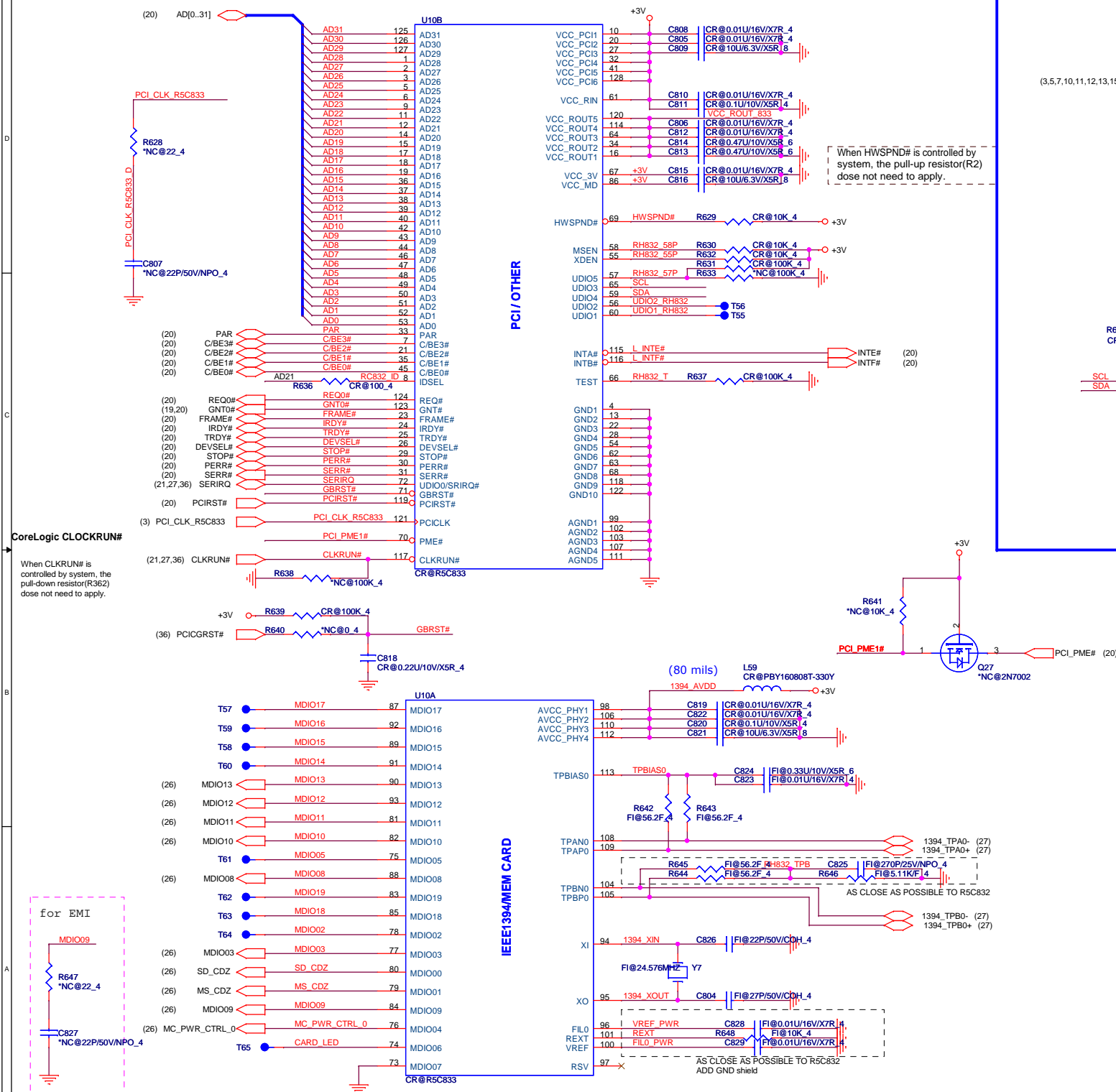
UMA & Discrete setting
LVDS Discrete / UMA

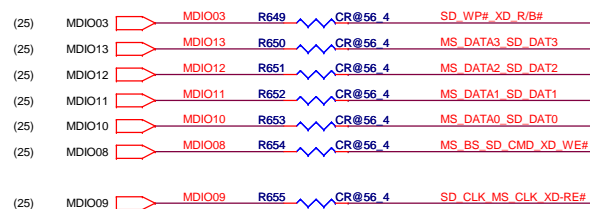
R150	0	NC
R149	0	NC
R148	0	NC
R463	0	NC
R457	0	NC
R451	0	NC
R91	0	NC
R155	NC	0
R154	NC	0
R153	NC	0
R461	NC	0
R460	NC	0
R452	NC	0
R92	NC	0



PROJECT : LE9E
Quanta Computer Inc.

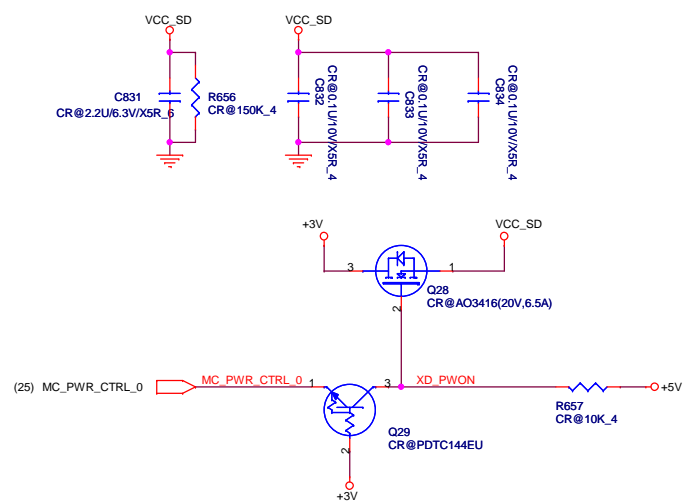






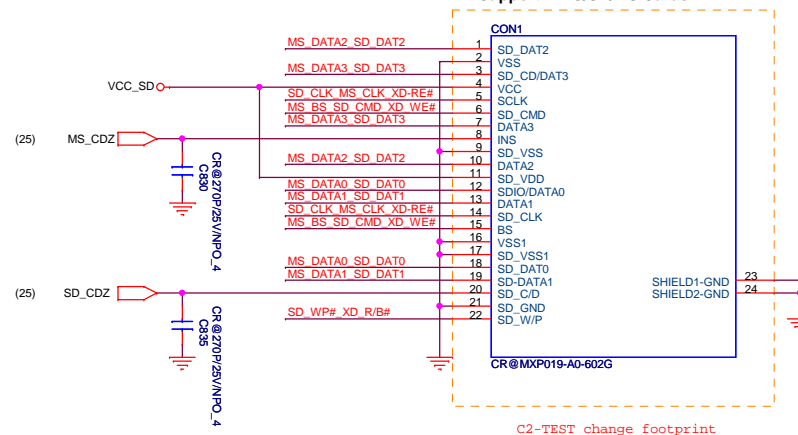
(3,5,7,10,11,12,13,15,16,19,20,21,22,23,24,25,27,28,30,31,33,34,35,36,37,38,40,41,42,43,44) +3V

(22,23,27,29,30,34,36,37,38) +5V



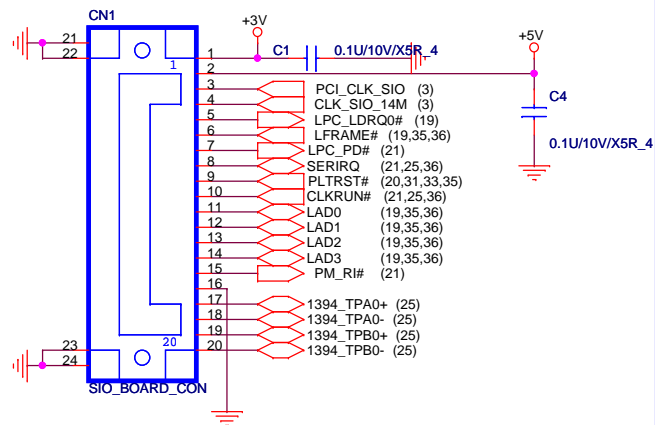
3 IN1 CARD-READER (PUSH-PUSH)

Support MMC/SD/MS Cards

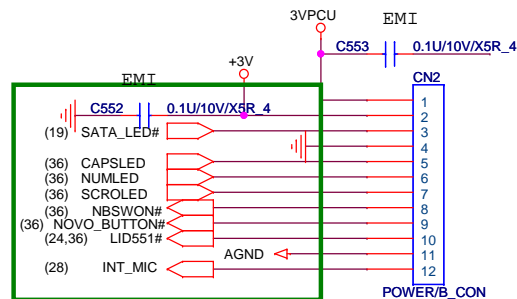


PROJECT : LE9E
Quanta Computer Inc.

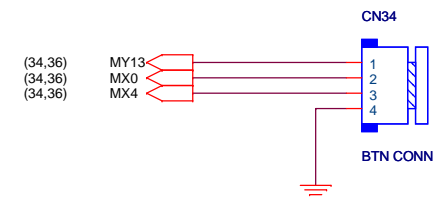
SIO BOARD



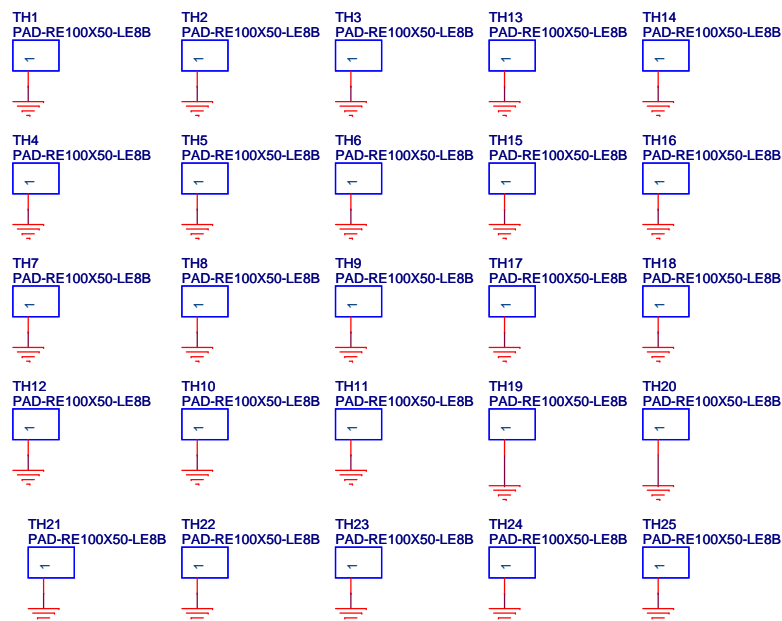
POWER BOARD

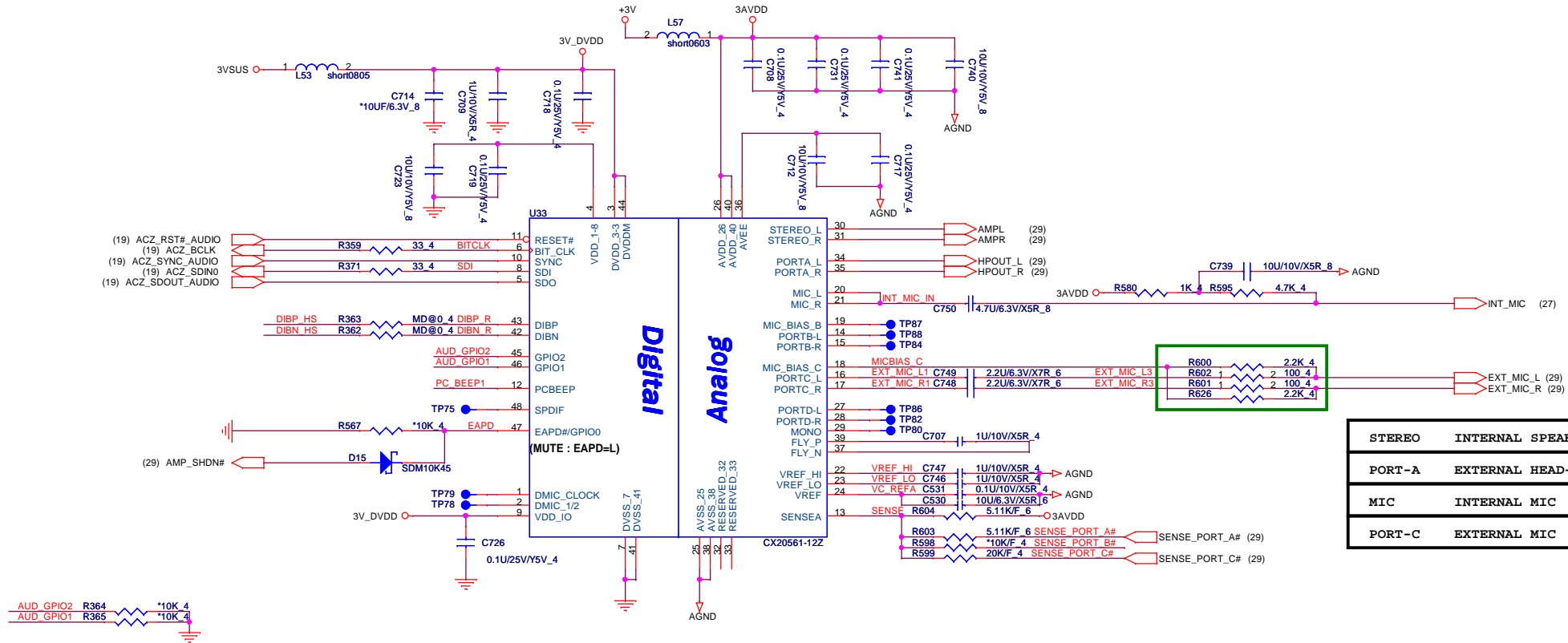


BUTTON BOARD



27

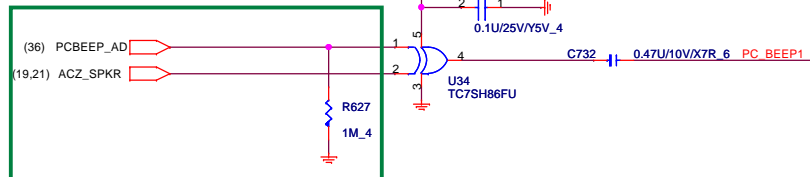




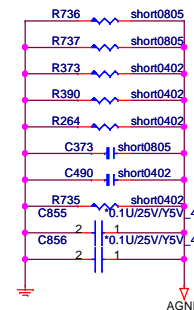
GAIN	10K GPIO RESISTORS	
	GPIO1	GPIO2
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-16dB	Omit	Populate

Default gain is -6dB without populating the 10K ohm pull down resistors going to GPIO1 and GPIO2

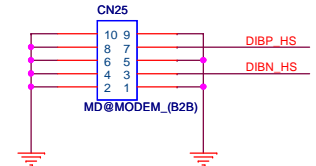
PC BEEP



FOR EMI SOLUTION

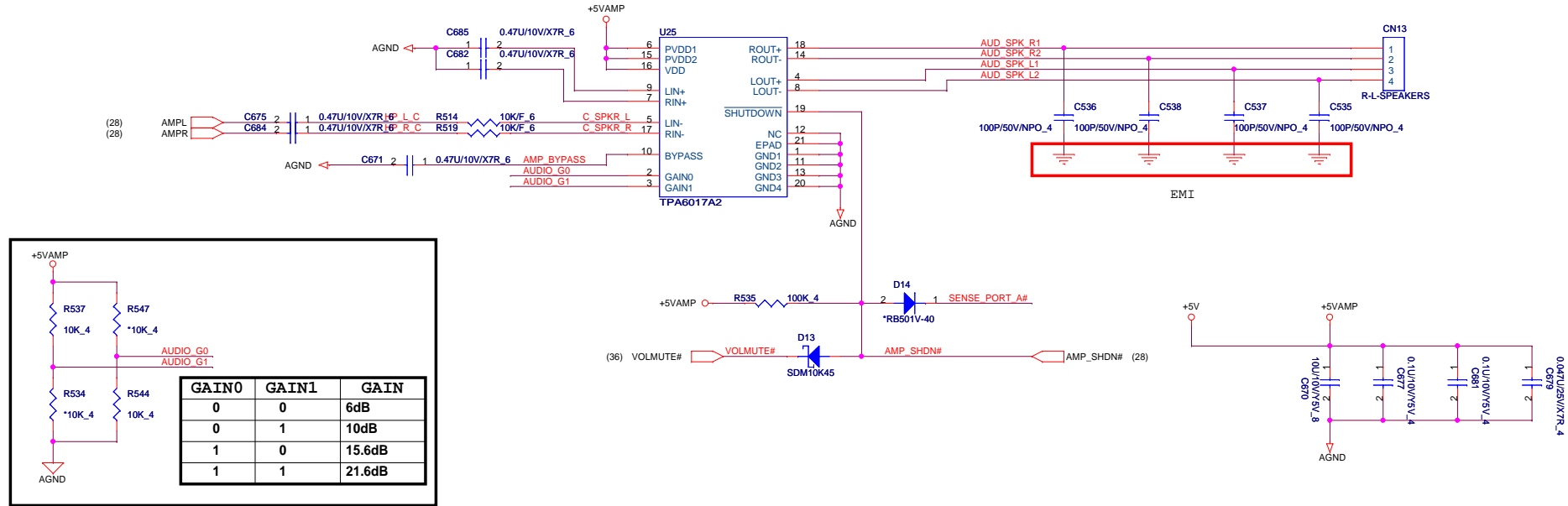


MODEM/B CONN.

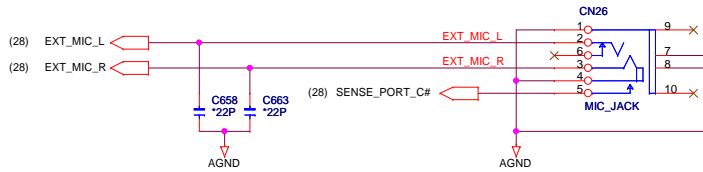


INTERNAL SPEAKER AMPLIFIER

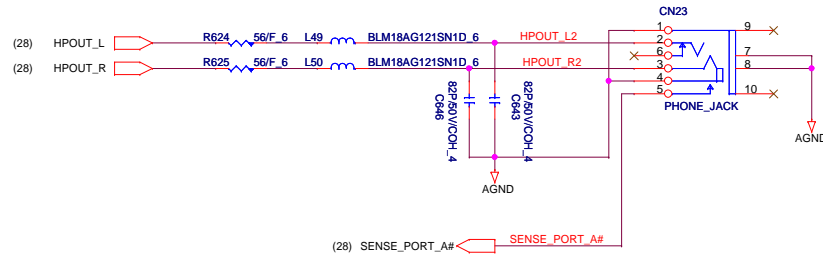
29



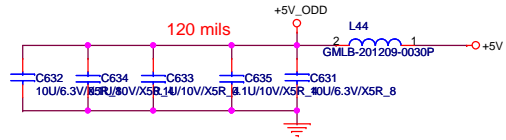
MIC-IN JACK



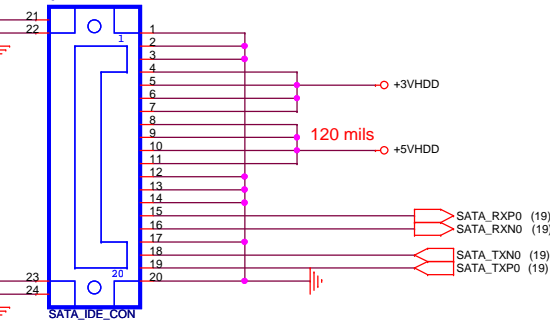
HEADPHONE



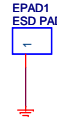
SATA CD-ROM



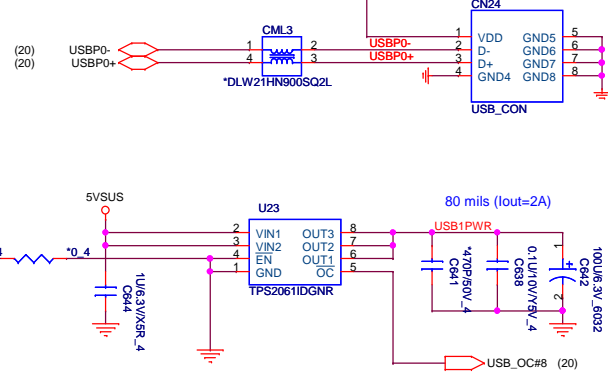
SATA-HDD CONNECTOR



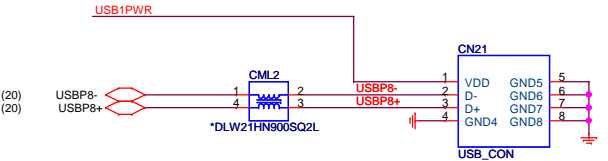
USBX3



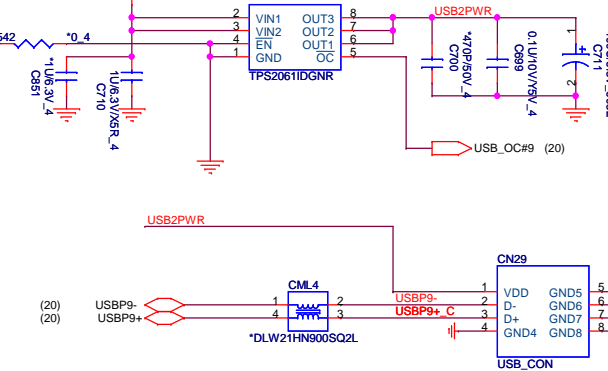
USB 0

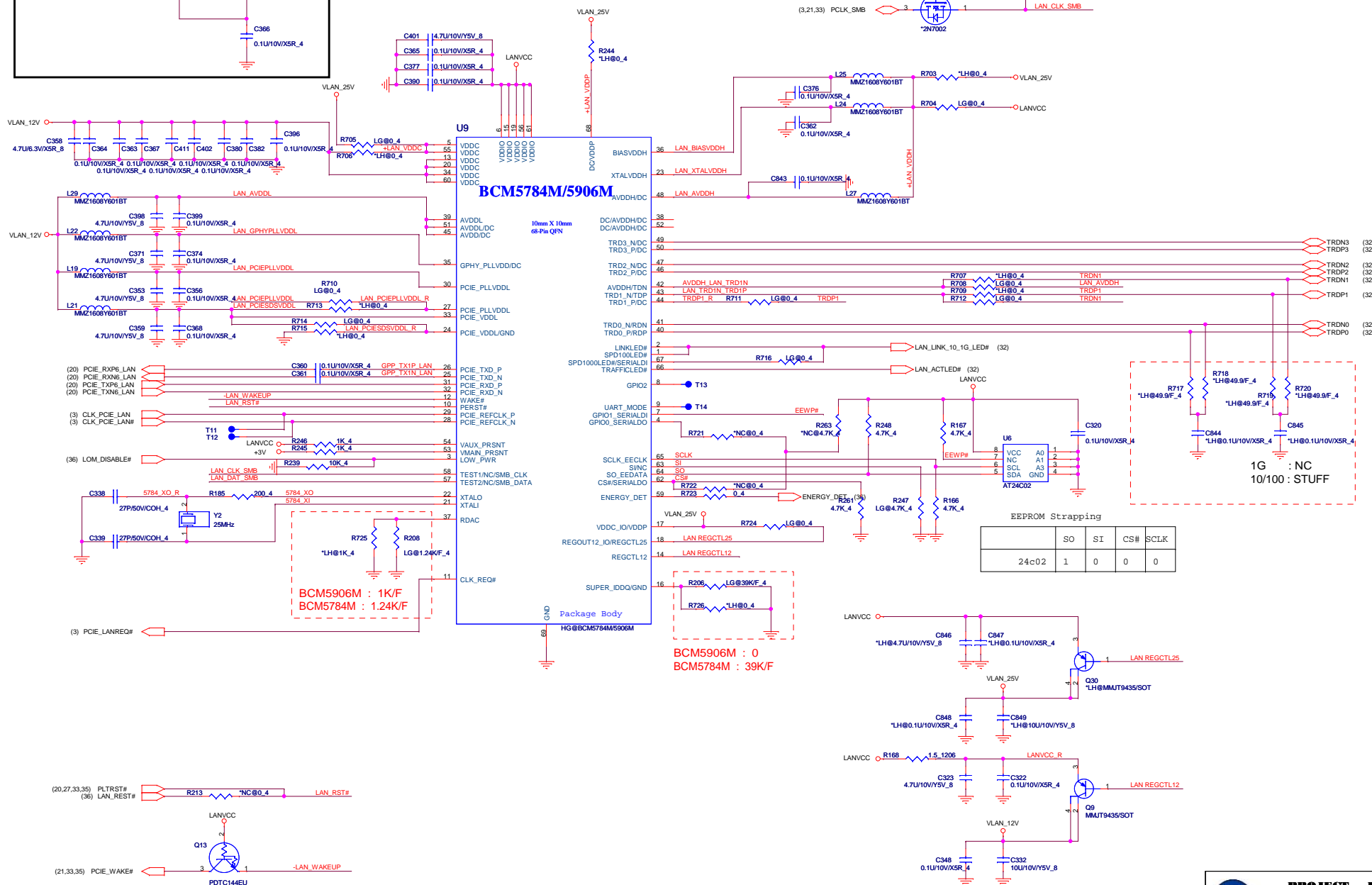
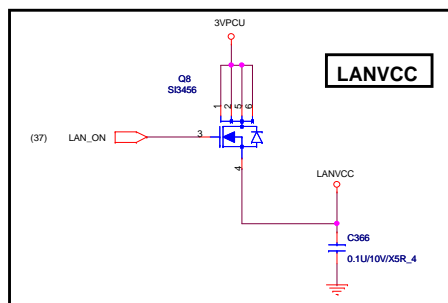


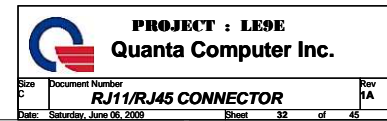
USB 1



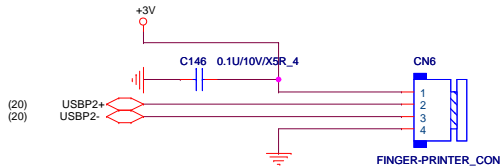
USB 2



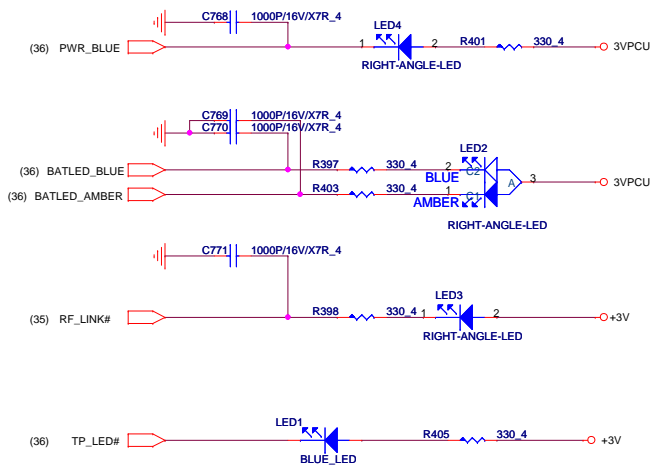




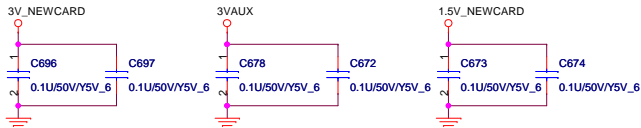
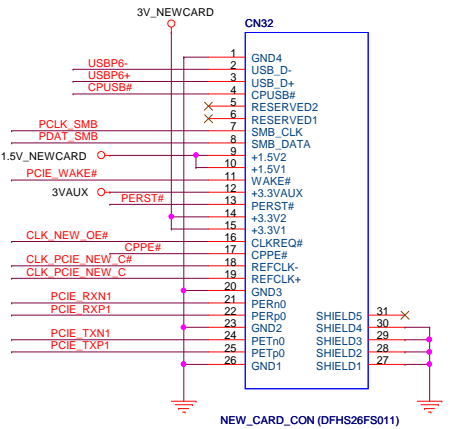
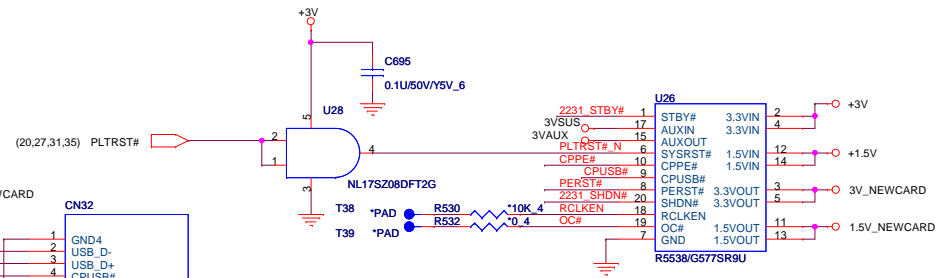
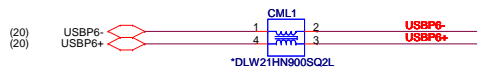
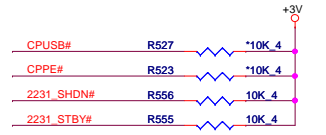
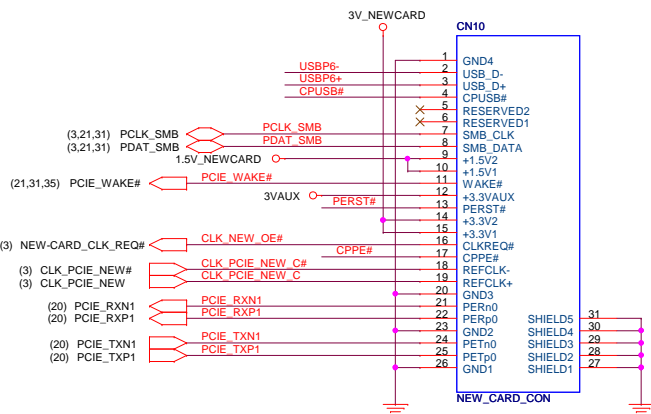
FINGER PRINTER



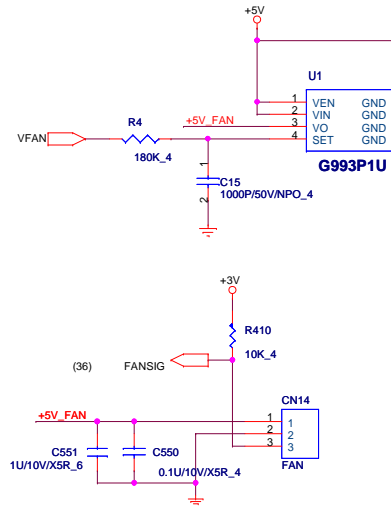
LED



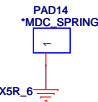
NEWCARD



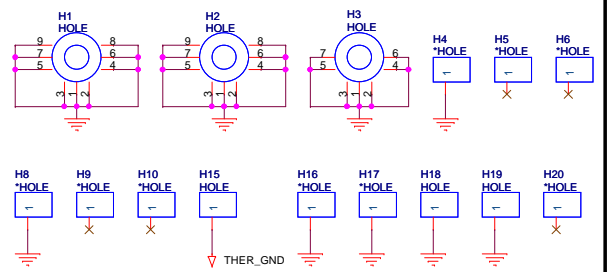
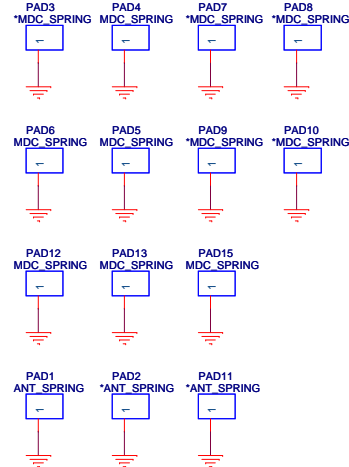
FAN CONTROL



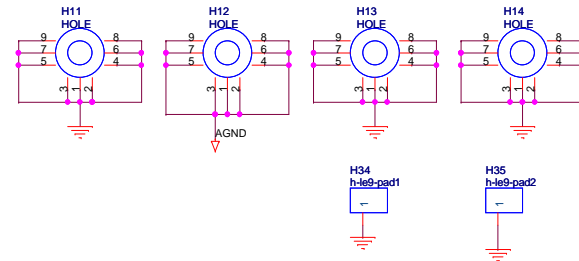
EMI PAD



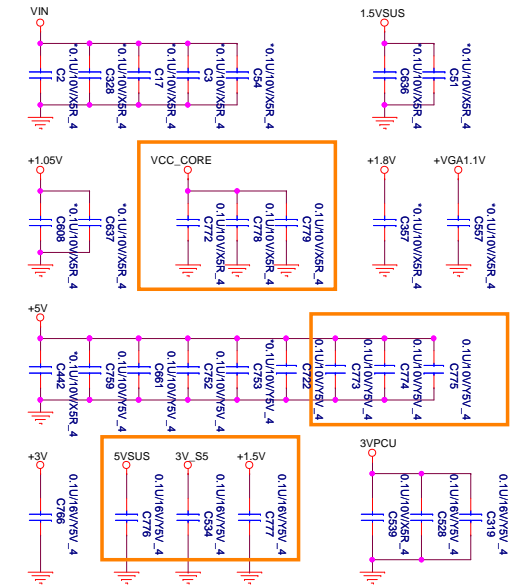
Springs



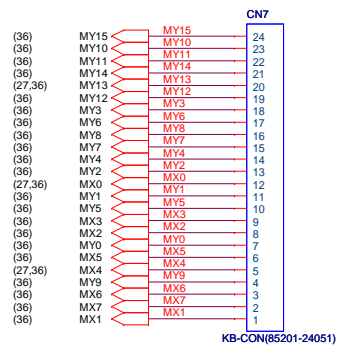
HOLES



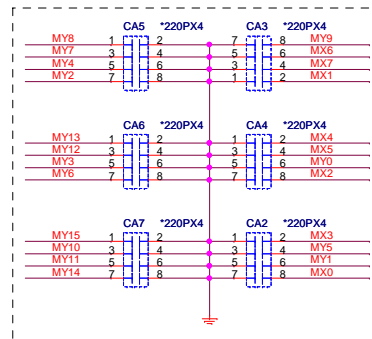
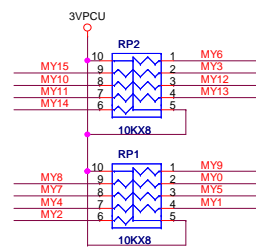
EMI CAPACITORS



KEYBOARD

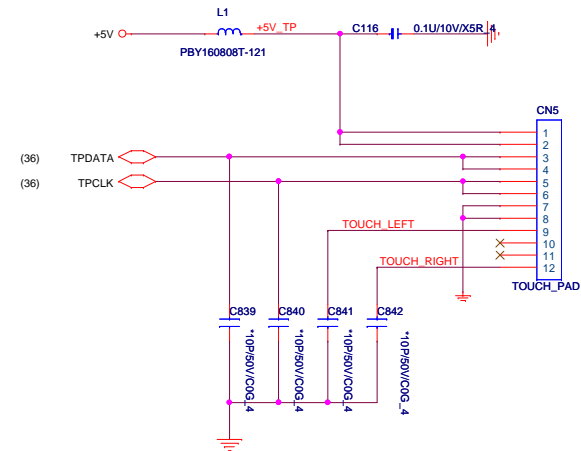


KB-CON(85201-24051)



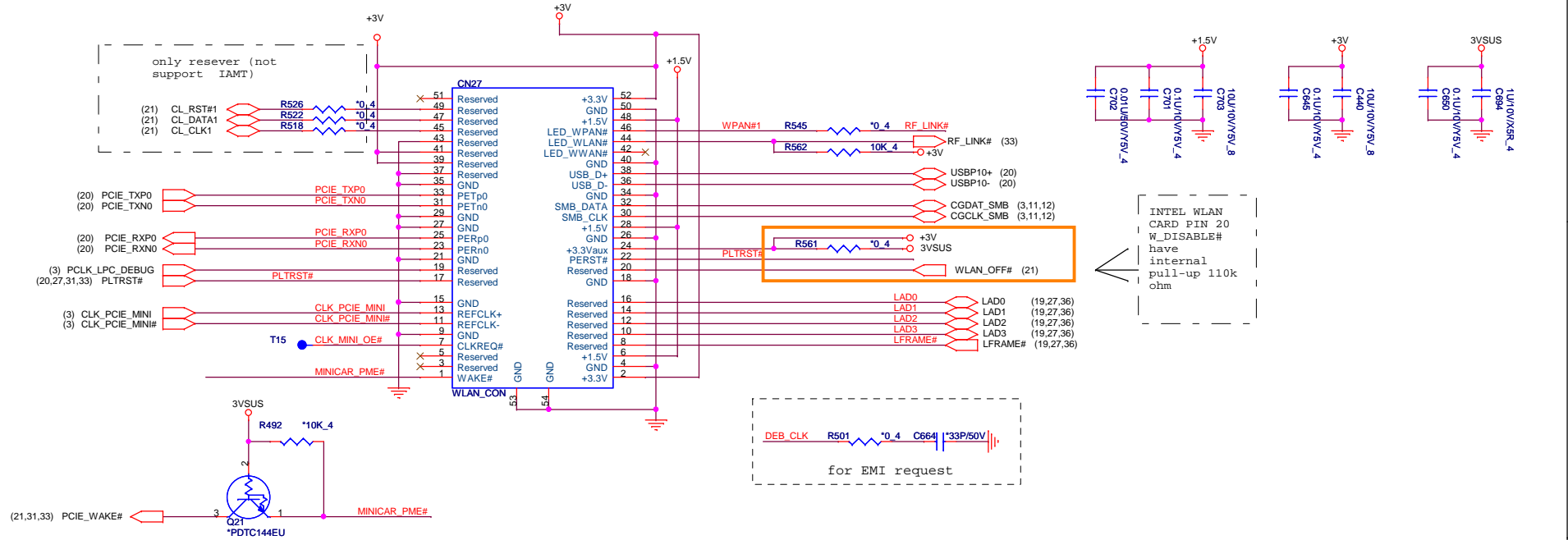
For EMI request

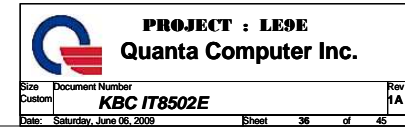
TOUCH PAD



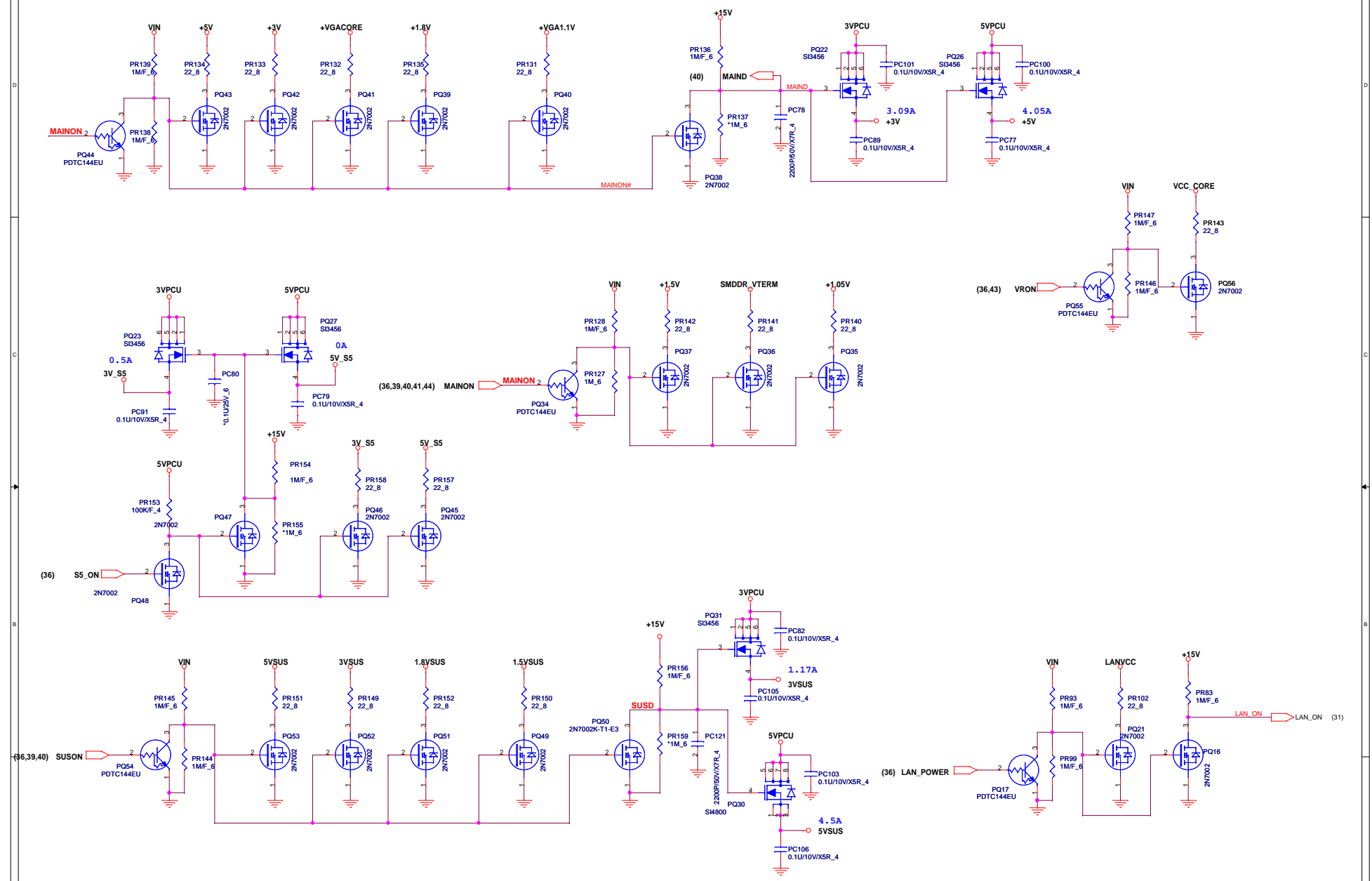
Mini PCI-E Card 1 WLAN

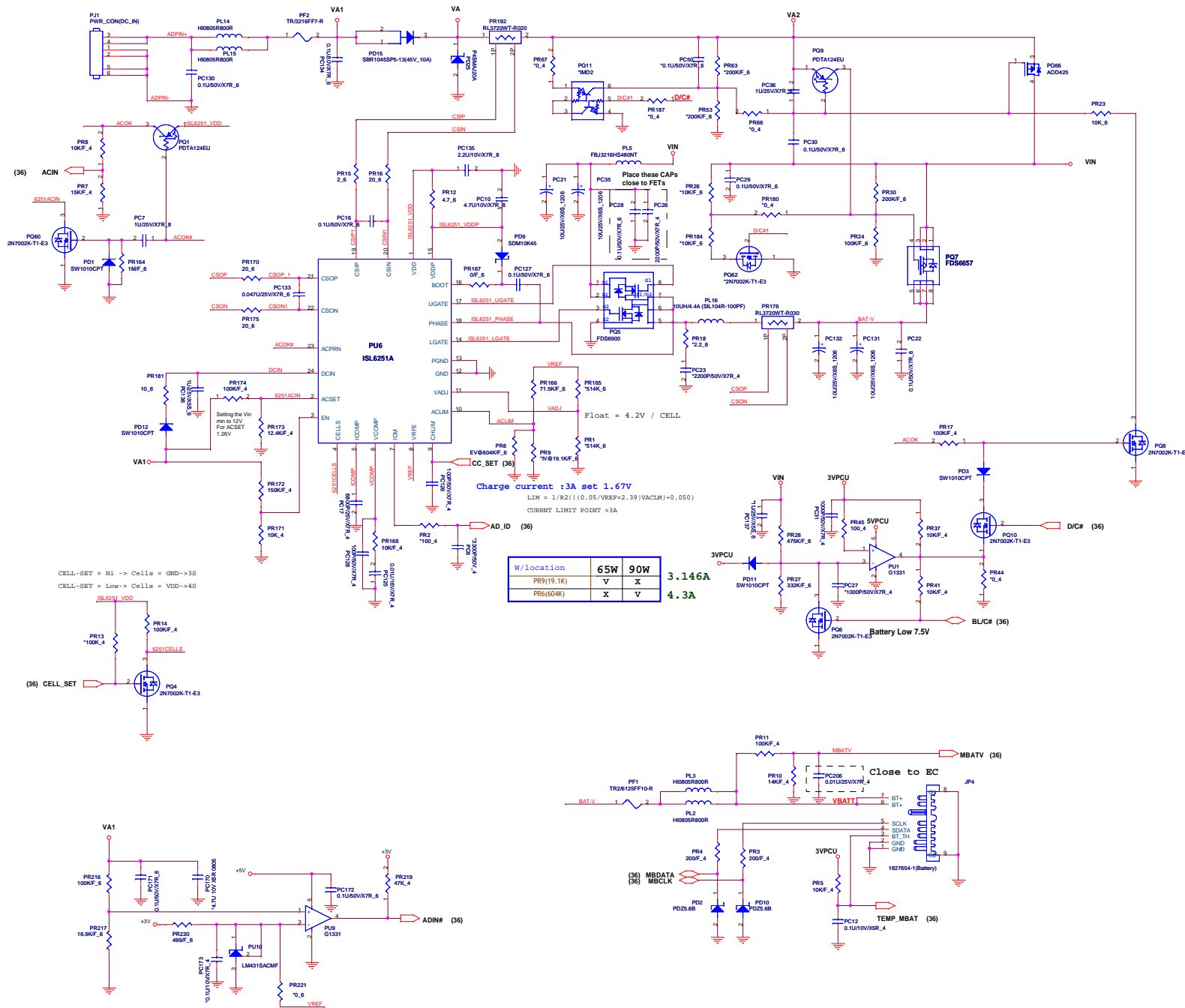
35

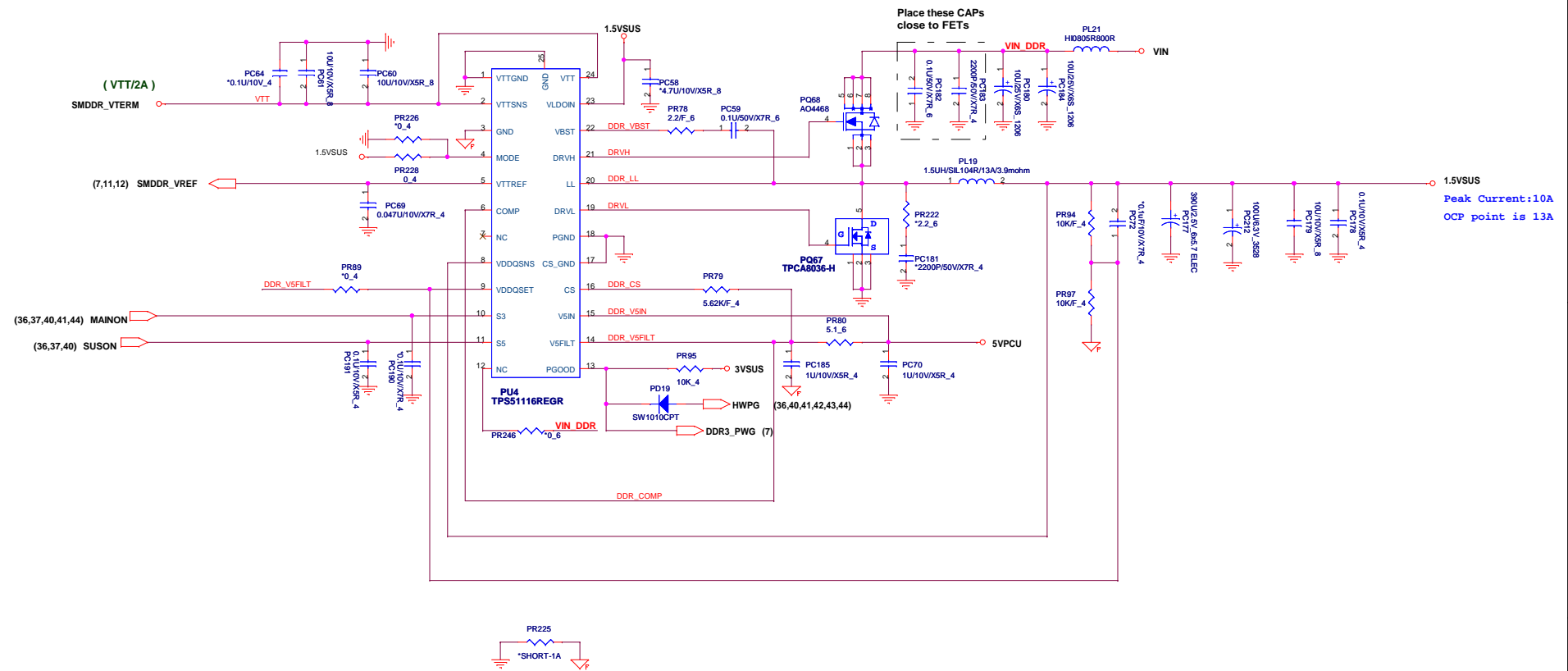


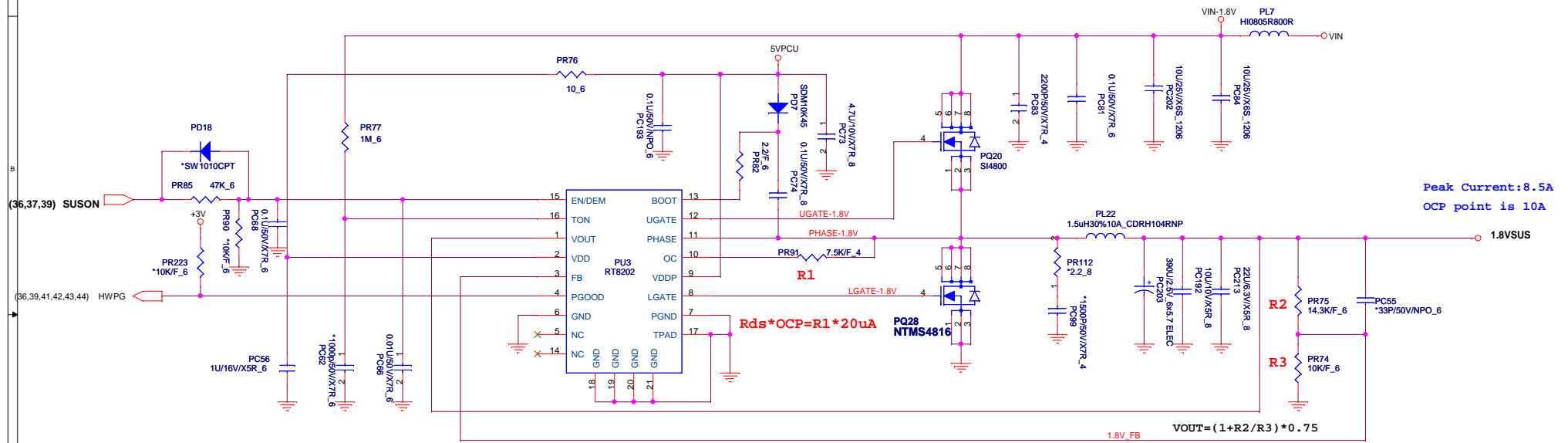


DISCHARGE



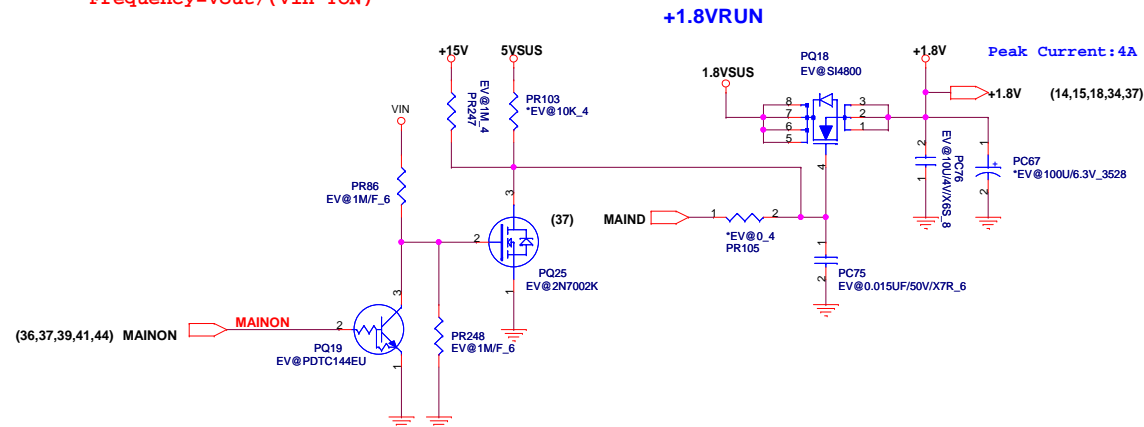


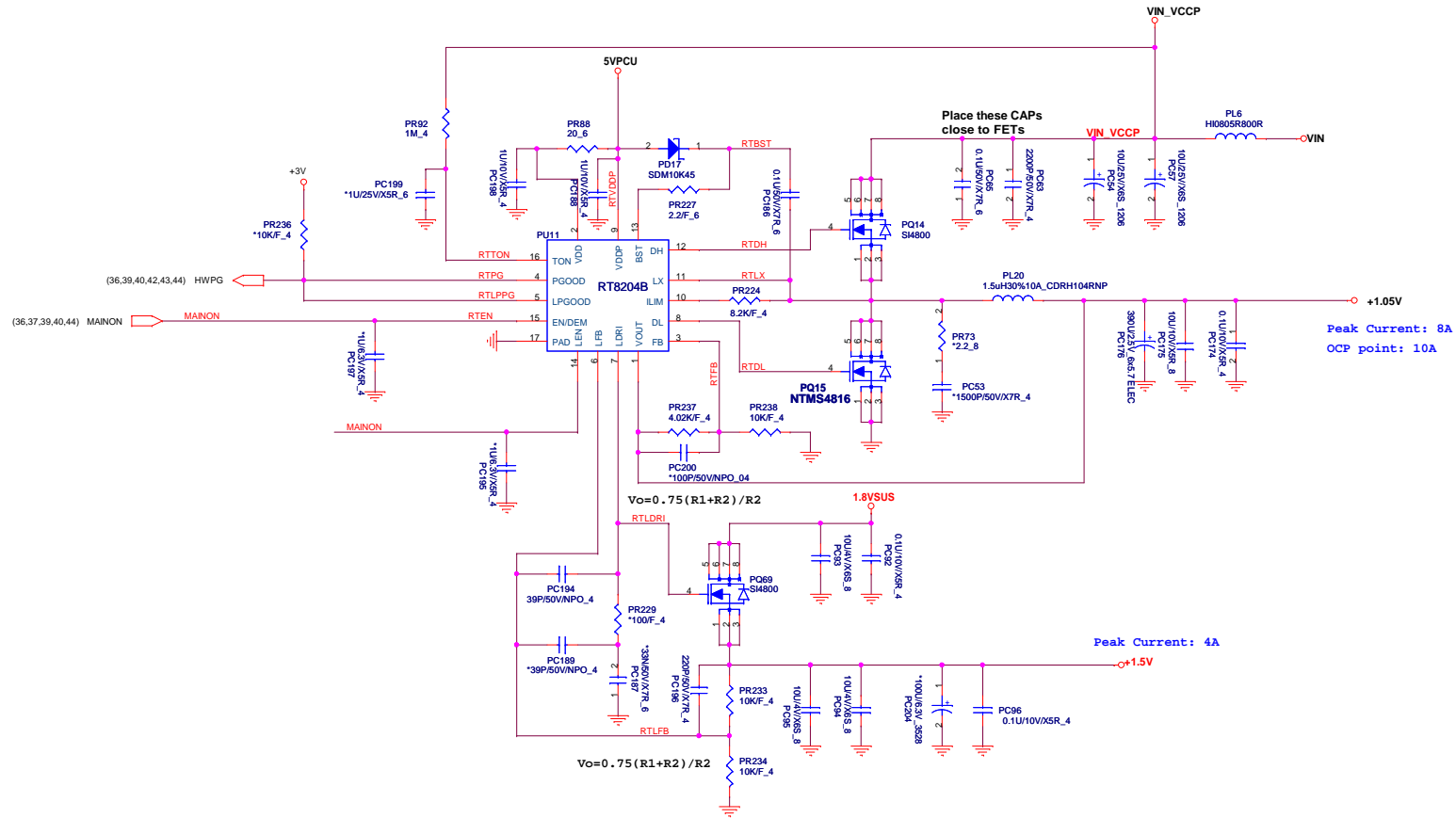




$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

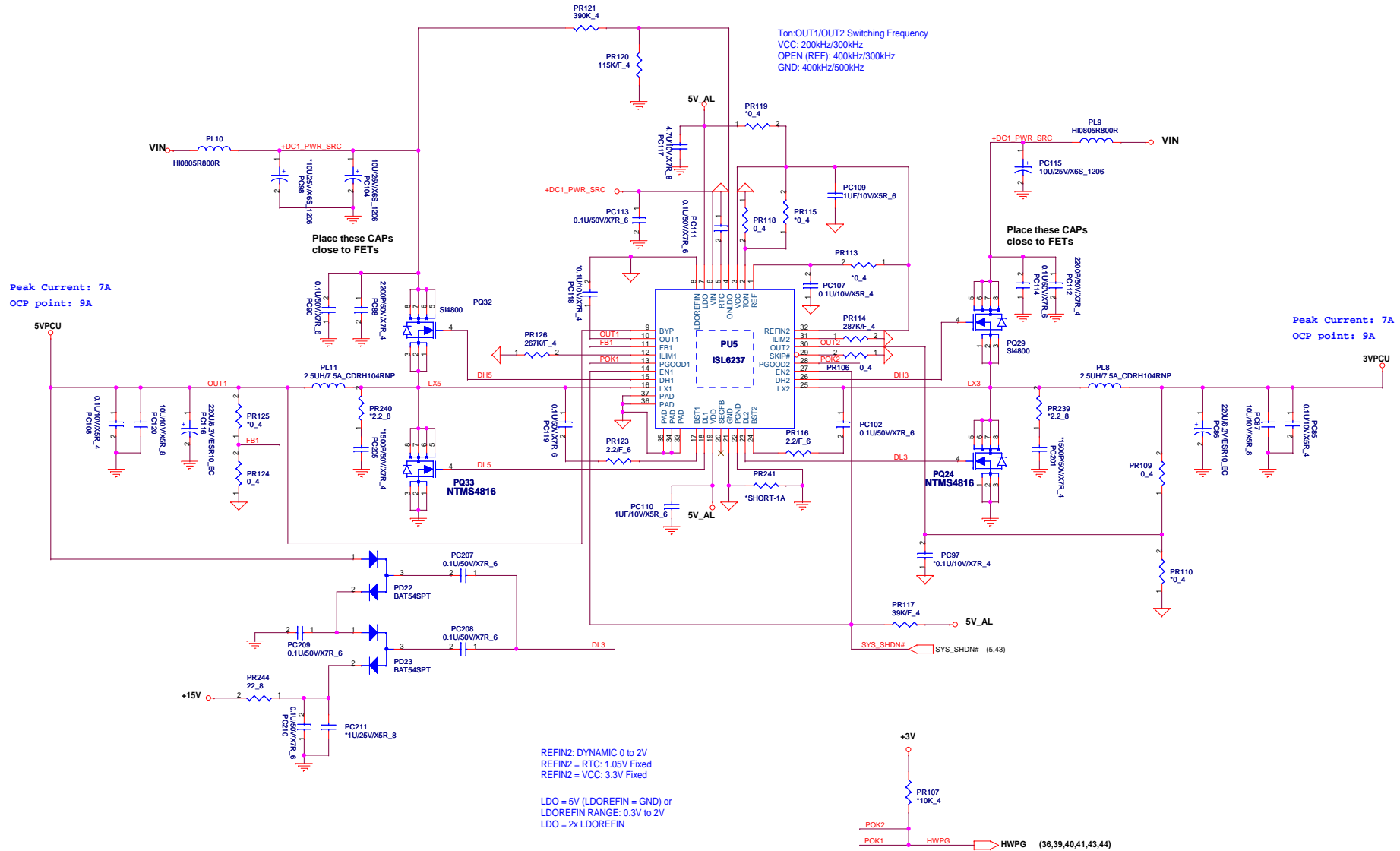
$$Frequency = Vout / (Vin * TON)$$



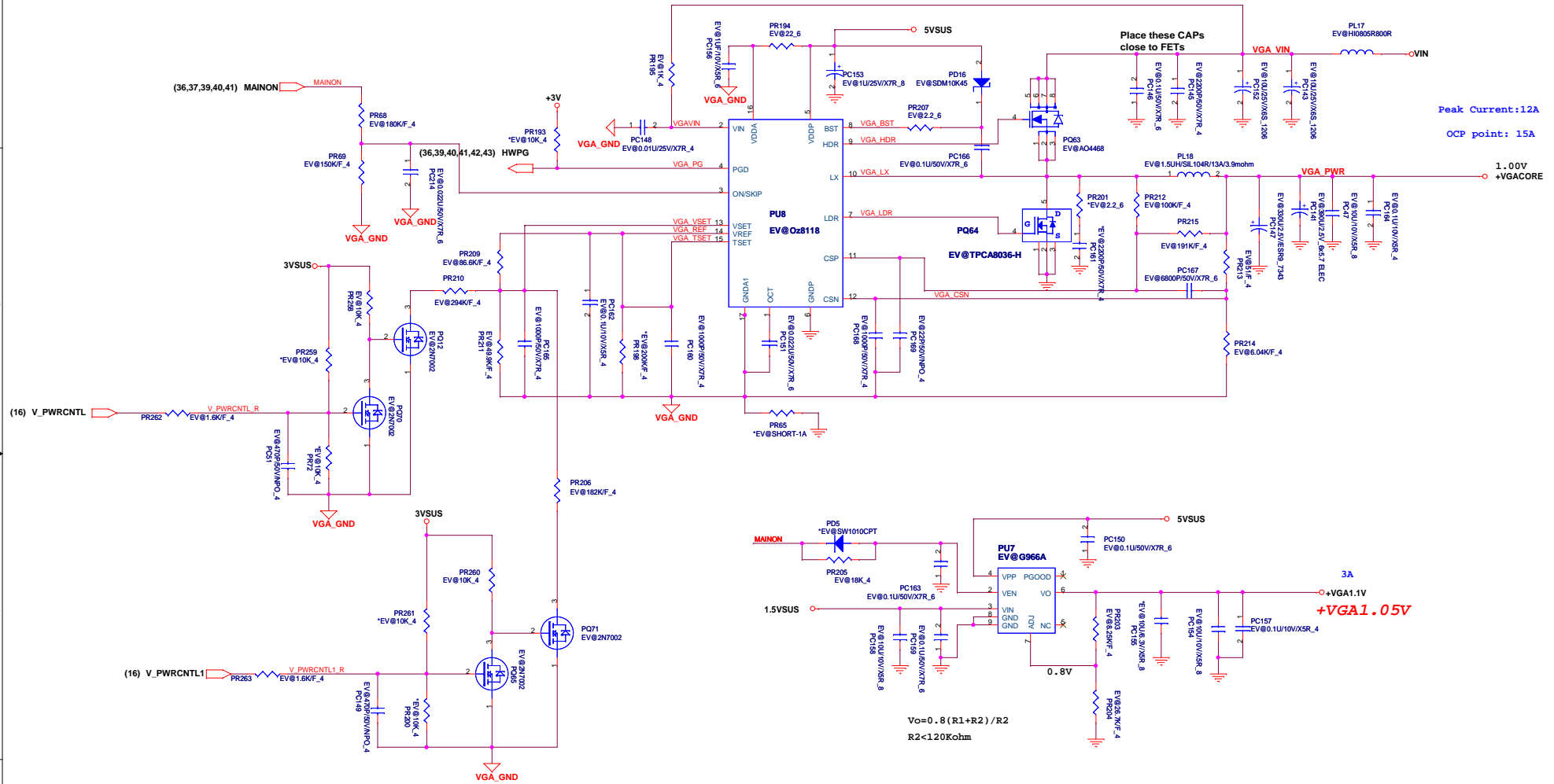


DC/DC 3VPCU/5VPCU/+15V

Ton:OUT1/OUT2 Switching Frequency
 VCC: 200kHz/300kHz
 OPEN (REF): 400kHz/300kHz
 GND: 400kHz/500kHz







V_PWRCNTL1	V_PWRCNTL	Vout (spec)
GPIO6	GPIO5	
0	0	0.80V
0	1	0.85V
1	0	0.90V
1	1	0.95V 1.00V

LE9E SYSTEM POWER BLOCK DIAGRAM

45

