

KAI Block Diagram

Project code : 91.4F601.001
PCB P/N : 05233
Revision : SA

CLK GEN
ICS954305
3

Intel CPU
Yonah/Merom
4,5

GDDR3 32MB
41

DDRII 533/667 Slot 0
11

DDRII 533/667 Slot 1
11

Calistoga
PM
6,7,8,9,10

nVIDIA
G72M-V G3-64
38,39,40

RGB CRT
13

LVDS
14

SVIDEO
13

1394
23

SD/SDIO/MMC
MS/MS Pro/xD
23,25

Ricoh
R5C832
CardReader
23,25

RJ45
CONN
26

10/100 NIC
Intel 82562
25

ICH7-M
15,16,17,18

USB 2.0

SATA

PATA

LPC Bus

CAMERA
30

BLUE
TOOTH
30

USB x 3
21

HDD
20

ODD
20

RJ11
CONN

MODEM
AMOM
WAKIKI
AUDIO CODEC
27

INTERNAL
ARRAY MIC

MIC IN

LINE OUT

SPDIF

OP AMP
APA2031
29

2CH
SPEAKER

Ricoh
R5538
26

New Card
26

Mini-Card
802.11a/b/g
24

Mini-Card
24

Capacity
Button

Touch
Pad
30

Int.
KB
30

CIR
30

Thermal
& Fan
G792
19

Flash ROM
1MB
31

KBC
ENE KB3910SF
29

DOCK
CIR MIC IN LINE OUT SPDIF TVOUT 10/100 Ethernet CIR

SYSTEM DC/DC
TPS51120

INPUTS OUTPUTS

DCBATOUT 5V_S5
3V_S5

SYSTEM DC/DC
MAX8743

INPUTS OUTPUTS

DCBATOUT 1D05V_S0
1D8V_S3

MAXIM CHARGER
MAX8725

INPUTS OUTPUTS

DCBATOUT BT+
18V 3.0A
5V 100mA

CPU DC/DC
MAX8736ETL

INPUTS OUTPUTS

DCBATOUT VCC_CORE
0.844~1.3V
44A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4
L7: GND
L8: Signal 5

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Block Diagram

Size
A3

Document Number

KAI

Rev
SA

Date: Thursday, November 24, 2005

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Calistoga Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6		0=Moby Dick 1=Calistoga
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	Reserved	
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO device present (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

History
11.18.2004: mini card not ready

125CV Spread Spectrum Select

SS3	SS2	SS1	SS0	Spread Amount%
0	0	0	0	-0.8
0	0	0	1	-1.0
0	0	1	0	-1.25
0	0	1	1	-1.5
0	1	0	0	-1.75
0	1	0	1	-2.0
0	1	1	0	-2.5
0	1	1	1	-3.0
1	0	0	0	+-0.3
1	0	0	1	+-0.4
1	0	1	0	+-0.5
1	0	1	1	+-0.6
1	1	0	0	+-0.8
1	1	0	1	+-1.0
1	1	1	0	+-1.25
1	1	1	1	+-1.5

PCI Routing

	IDSEL	IRQ	REQ/GNT
R5C832	25		0

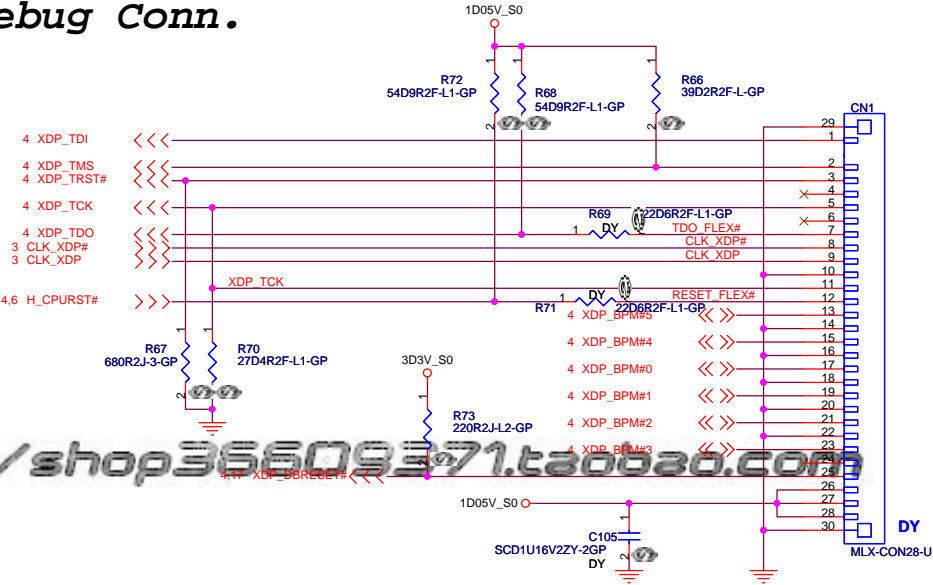
ICH7M Integrated Pull-up and Pull-down Resistors

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
----------------------------------------------------------------------------	----------------------

ITP Debug Conn.



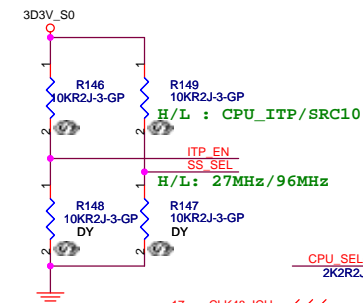
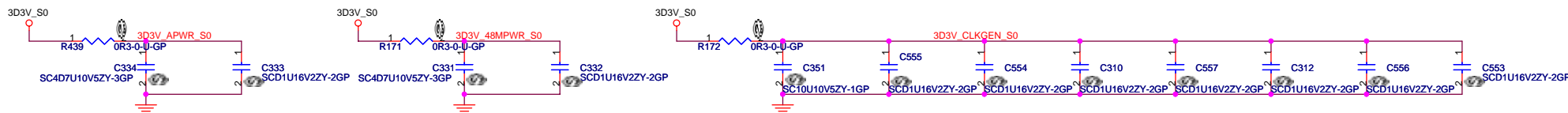
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ITP
KAI

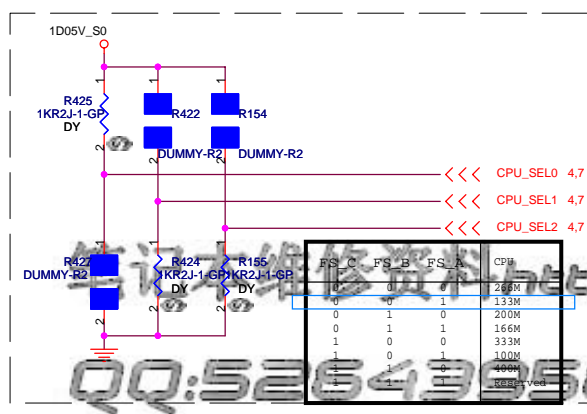
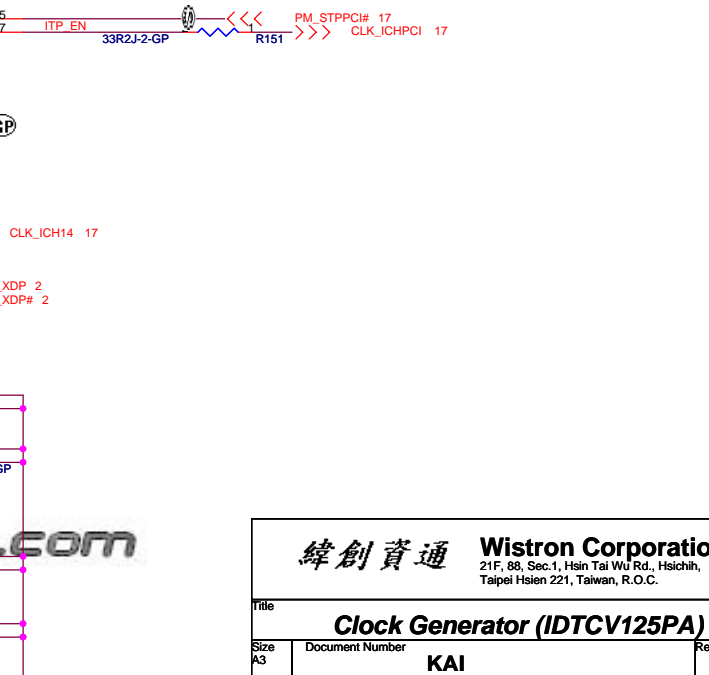
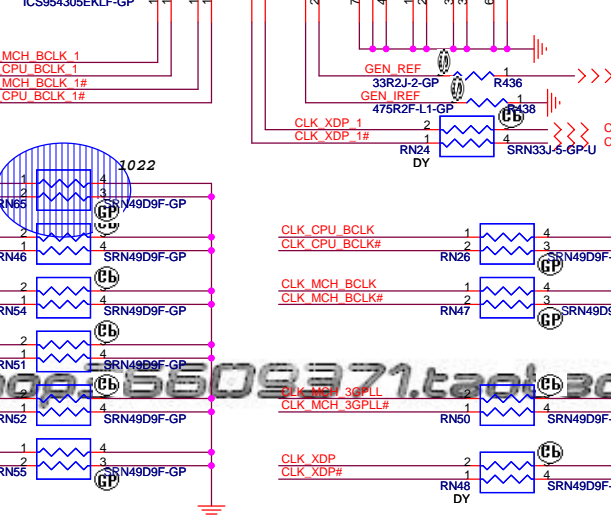
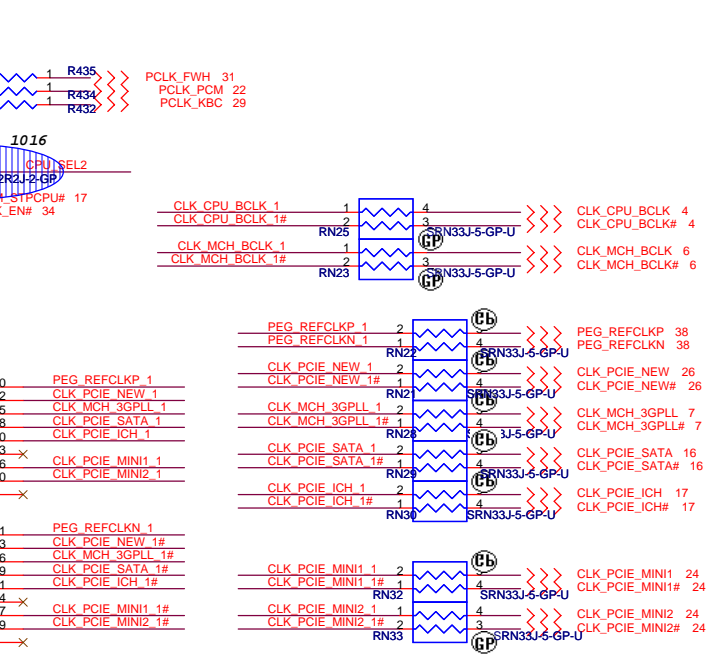
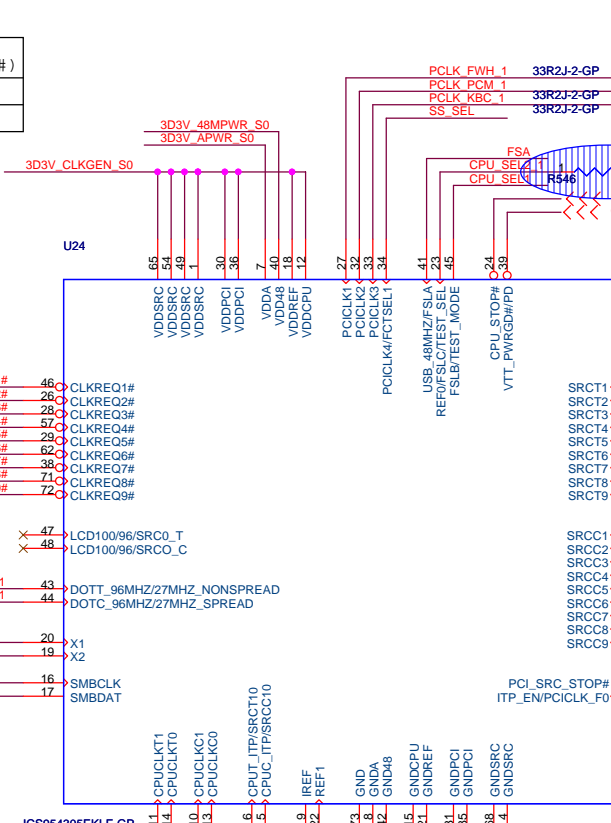
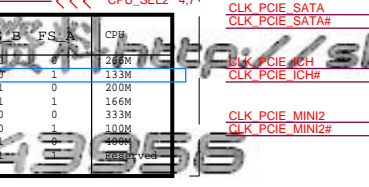
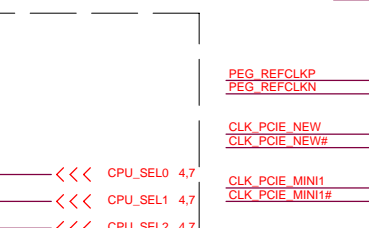
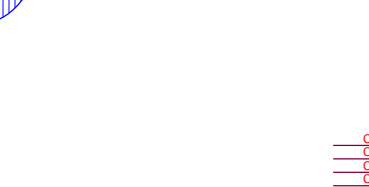
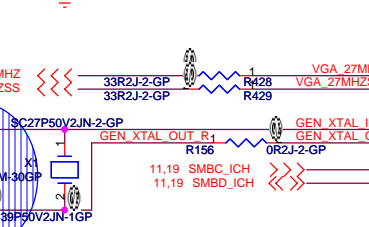
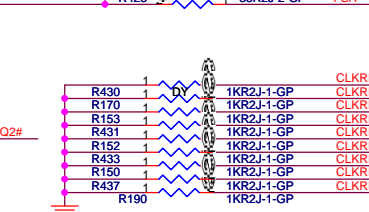
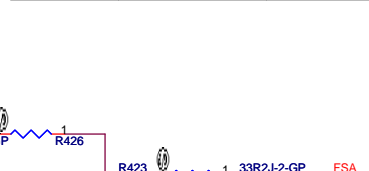
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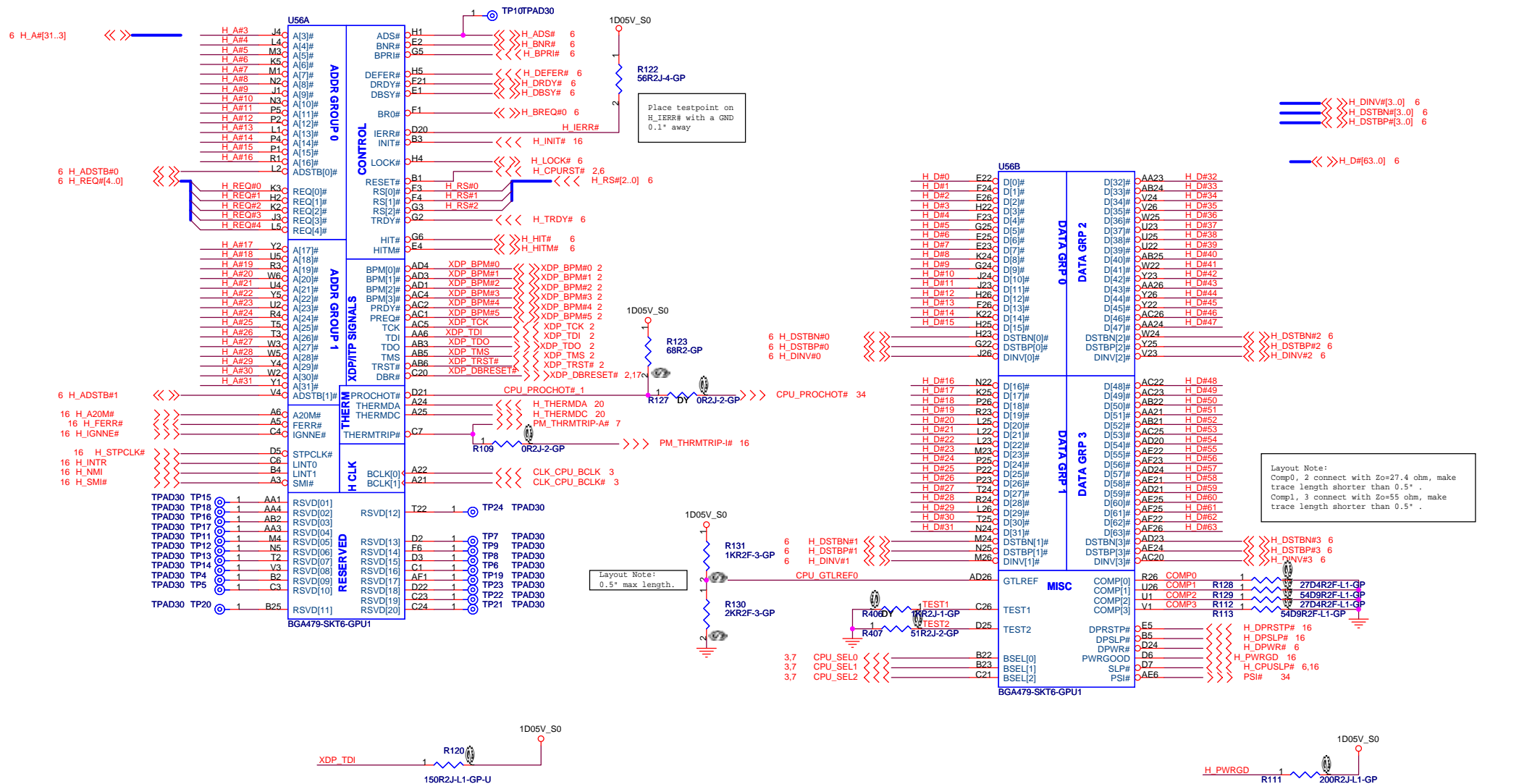
Monday, November 28, 2005

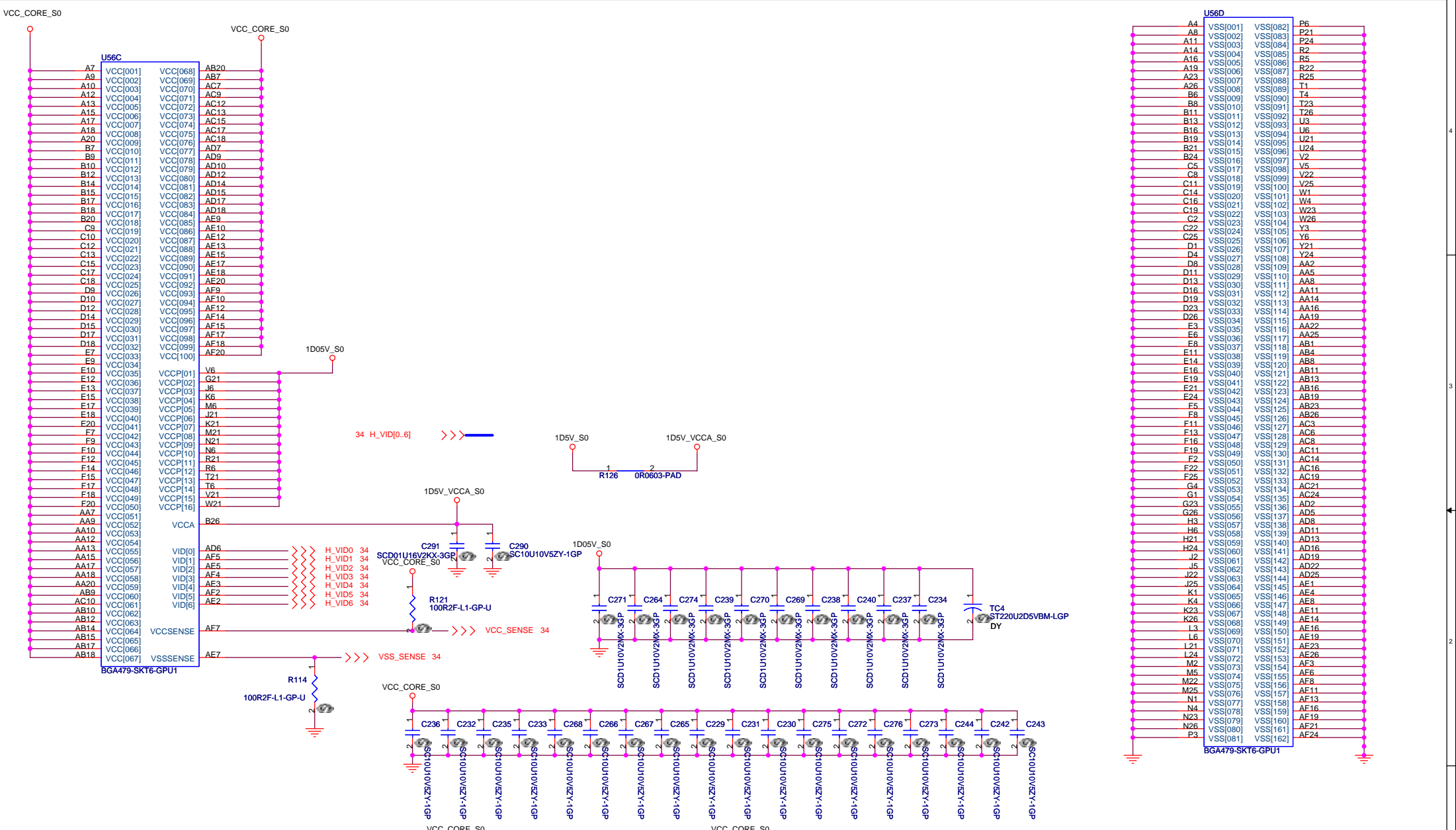
Sheet 2 of 44



IN (3D3V_S0)	EN (6218_PGOOD)	OUT (VTT_PWRGD#)
H	L	H
X	H	Hi - Z



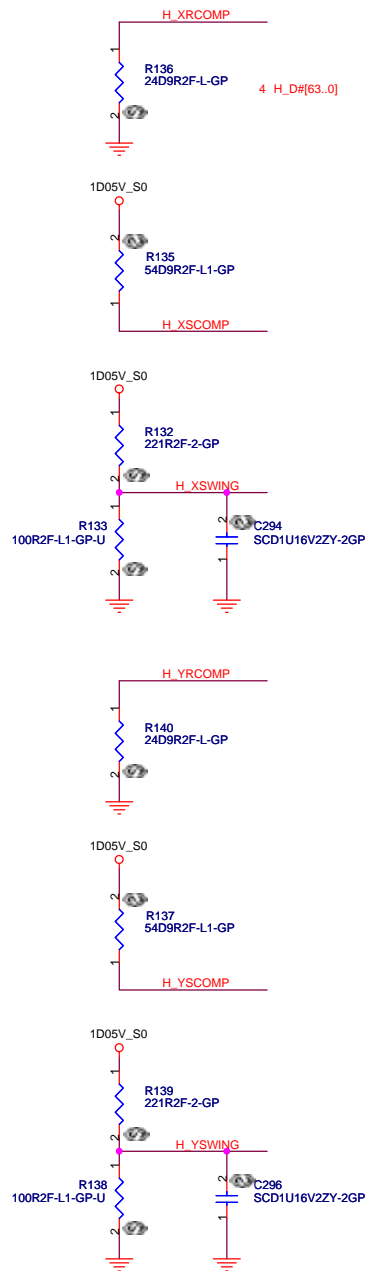




Layout Note:
VCCSENSE and VSSSENSE lines
should be of equal length.

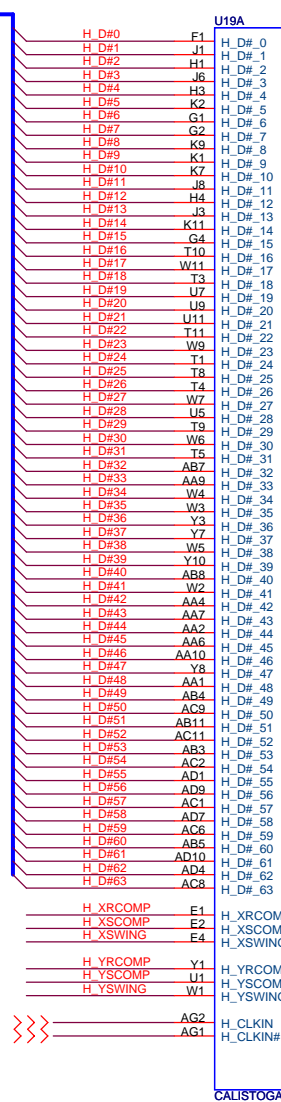
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U56D		
A4	VSS[001]	P6
A8	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	R2
A16	VSS[005]	R5
A19	VSS[006]	R22
A23	VSS[007]	R25
A26	VSS[008]	T1
B6	VSS[009]	T4
B8	VSS[010]	T23
B11	VSS[011]	T26
B13	VSS[012]	U3
B16	VSS[013]	U6
B19	VSS[014]	U21
B21	VSS[015]	U24
B24	VSS[016]	V2
C5	VSS[017]	V5
C8	VSS[018]	V22
C11	VSS[019]	V25
C14	VSS[020]	W1
C16	VSS[021]	W4
C19	VSS[022]	W23
C2	VSS[023]	W26
C22	VSS[024]	Y3
C25	VSS[025]	Y6
D1	VSS[026]	Y21
D8	VSS[027]	Y24
D11	VSS[028]	Y22
D13	VSS[029]	AA5
D16	VSS[030]	AA8
D19	VSS[031]	AA11
D23	VSS[032]	AA14
D26	VSS[033]	AA16
E3	VSS[034]	AA19
E6	VSS[035]	AA22
E8	VSS[036]	AA25
E11	VSS[037]	AB1
E14	VSS[038]	AB4
E16	VSS[039]	AB8
E19	VSS[040]	AB11
E21	VSS[041]	AB16
E24	VSS[042]	AB19
F5	VSS[043]	AB23
F8	VSS[044]	AB26
F11	VSS[045]	AC3
F13	VSS[046]	AC6
F16	VSS[047]	AC8
F19	VSS[048]	AC11
F2	VSS[049]	AC14
F22	VSS[050]	AC16
F25	VSS[051]	AC19
G4	VSS[052]	AC21
G1	VSS[053]	AC24
G23	VSS[054]	AD2
G26	VSS[055]	AD5
H3	VSS[056]	AD8
H6	VSS[057]	AD11
H21	VSS[058]	AD13
H24	VSS[059]	AD16
J2	VSS[060]	AD19
J5	VSS[061]	AD22
J22	VSS[062]	AD25
J25	VSS[063]	AE1
K1	VSS[064]	AE4
K4	VSS[065]	AE8
K23	VSS[066]	AE11
K26	VSS[067]	AE14
L3	VSS[068]	AE16
L6	VSS[069]	AE19
L21	VSS[070]	AE23
L24	VSS[071]	AE26
M2	VSS[072]	AF3
M5	VSS[073]	AF6
M22	VSS[074]	AF8
M25	VSS[075]	AF11
N1	VSS[076]	AF13
N4	VSS[077]	AF16
N23	VSS[078]	AF19
N26	VSS[079]	AF21
P3	VSS[080]	AF24
	VSS[081]	VSS[162]



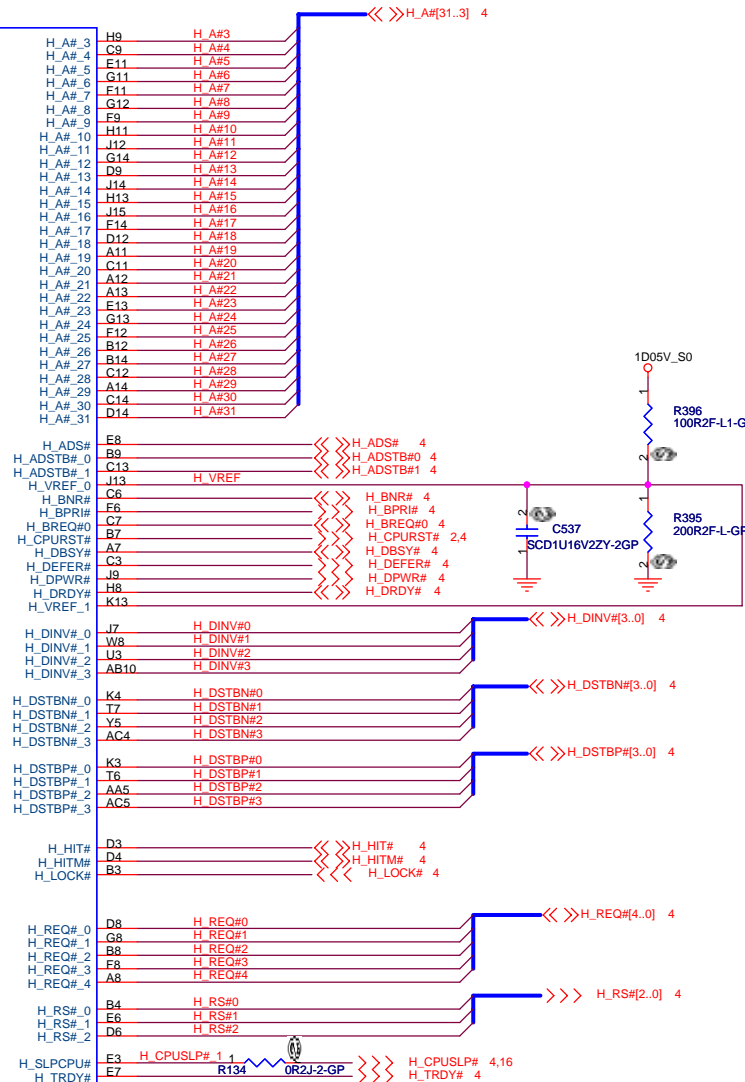
<<>>

3 CLK_MCH_BCLK
3 CLK_MCH_BCLK#



CALISTOGA

HOST



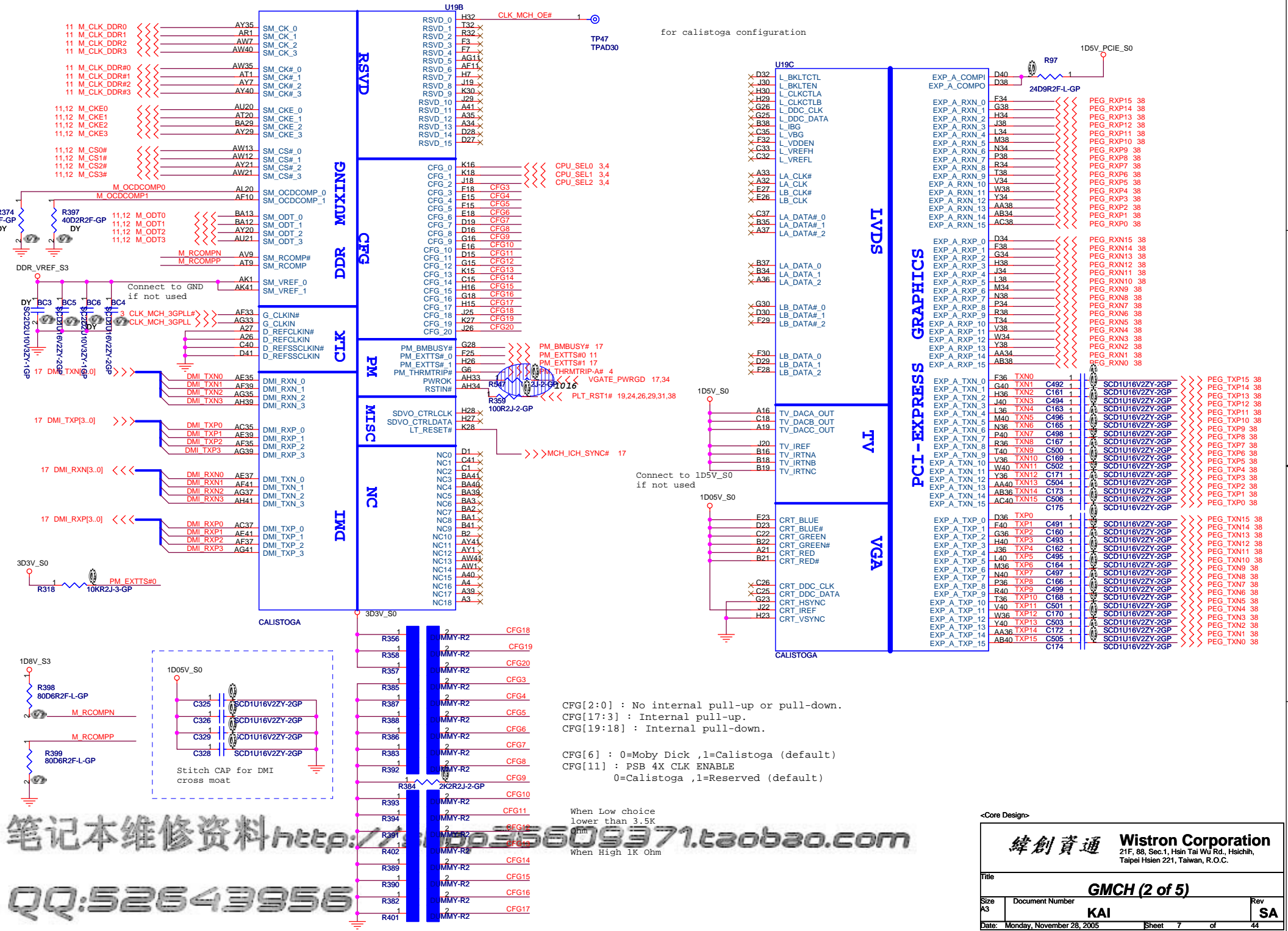
100mils or less
from GMCH pin

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<Core Design>

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Title			GMCH (1 of 5)		
Size	Document Number	KAI			Rev
A3					SA
Date:	Monday, November 28, 2005	Sheet	6	of	44



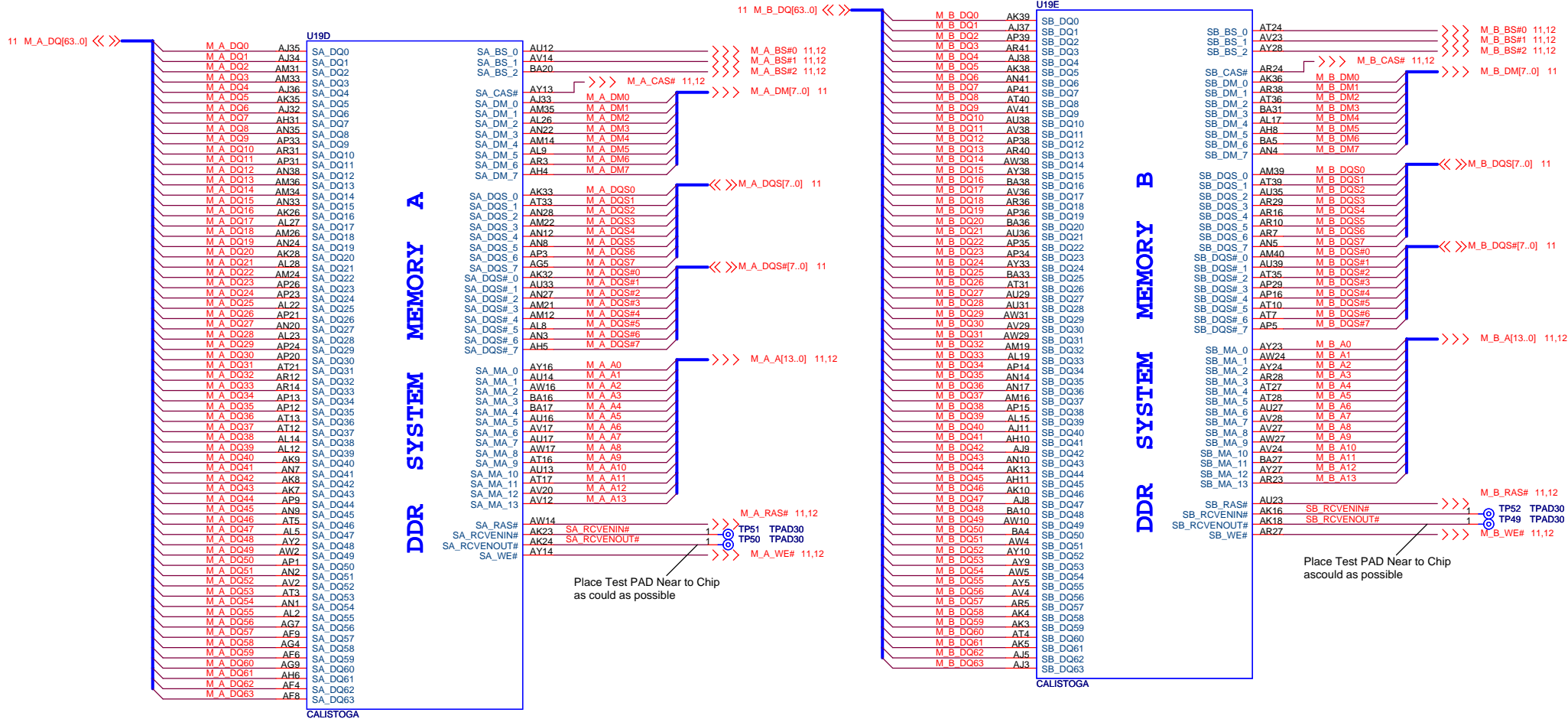
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CFG[2:0] : No internal pull-up or pull-down.
CFG[17:3] : Internal pull-up.
CFG[19:18] : Internal pull-down.

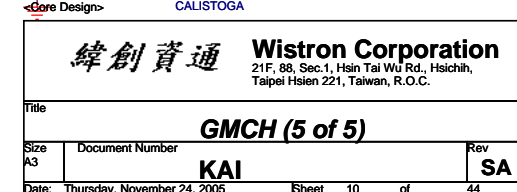
CFG[6] : 0=Moby Dick ,1=Calistoga (default)
CFG[11] : PSB 4X CLK ENABLE
0=Calistoga ,1=Reserved (default)

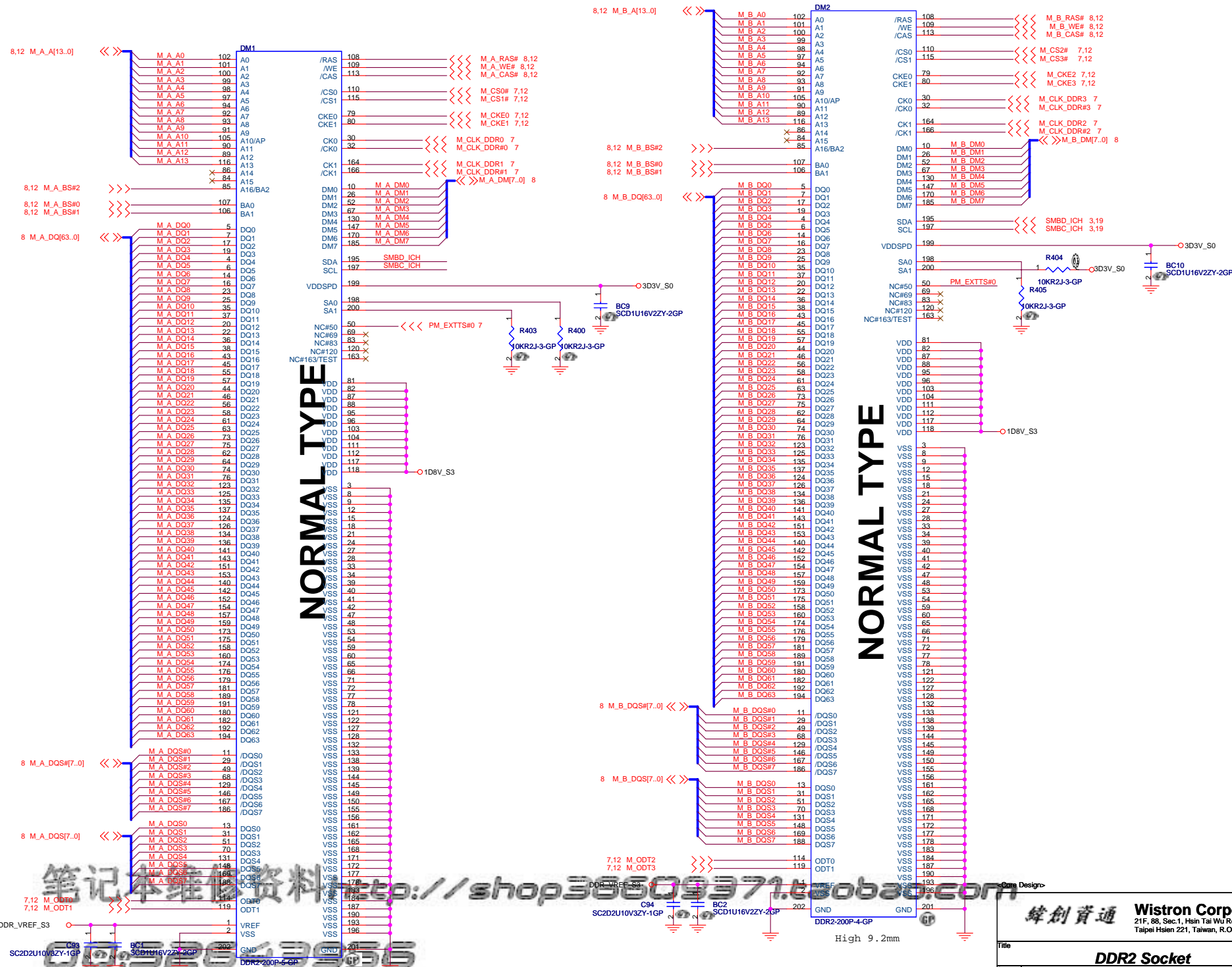
When Low choice
lower than 3.5K
Ohm
When High 1K Ohm

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Title GMCH (2 of 5)		
Size A3	Document Number KAI	Rev SA
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NORMAL TYPE

NORMAL TYPE

Core Design

Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
DDR2 Socket	
Size	Document Number
Custom	KAI
Date	Monday, November 28, 2005
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Rev	SA

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

8 7 6 5

RN13

1 2 3 4

M_B_A11
M_B_A8
M_B_A7

>>> M_CKE3 7,11

<<< M_A_A[13..0] 8,11

<<< M_B_A[13..0] 8,11

8 7 6 5

RN12

1 2 3 4

M_B_A0
M_B_A2
M_B_A1
M_B_A4

SRN56J-3-GP

8 7 6 5

RN15

1 2 3 4

M_B_A5
M_B_A8
M_B_A3
M_B_A10

SRN56J-3-GP

1 2

RN11

4 3

M_B_A13

>>> M_CS2# 7,11

1 2

SRN56J-4-GP

4

M_A_A10

>>> M_ODT1 7,11

RN17

8 7 6 5

RN16

1 2 3 4

M_B_BS#0 8,11
M_B_WE# 8,11
M_B_RAS# 8,11
M_B_BS#1 8,11

SRN56J-3-GP

8 7 6 5

RN14

1 2 3 4

M_CKE2 7,11
M_B_BS#2 8,11

SRN56J-3-GP

8 7 6 5

RN18

1 2 3 4

M_CS3# 7,11
M_B_CAS# 8,11
M_ODT2 7,11
M_ODT3 7,11

SRN56J-3-GP

8 7 6 5

RN44

1 2 3 4

M_A_RAS# 8,11
M_CS0# 7,11
M_ODT0 7,11

SRN56J-3-GP

8 7 6 5

RN42

1 2 3 4

M_A_A4
M_A_A2
M_A_A0

>>> M_A_BS#1 8,11

SRN56J-3-GP

8 7 6 5

RN9

1 2 3 4

M_A_WE# 8,11
M_A_BS#0 8,11
M_CS1# 7,11
M_A_CAS# 8,11

SRN56J-3-GP

8 7 6 5

RN10

1 2 3 4

M_CKE0 7,11
M_A_BS#2 8,11

SRN56J-3-GP

8 7 6 5

RN43

1 2 3 4

M_CKE1 7,11

SRN56J-3-GP

8 7 6 5

RN8

1 2 3 4

M_A_A8
M_A_A5
M_A_A3
M_A_A1

SRN56J-3-GP

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

C182 DY SCD1U16V2ZY-2GP
C254 DY SCD1U16V2ZY-2GP
C534 DY SCD1U16V2ZY-2GP
C511 DY SCD1U16V2ZY-2GP
C183 DY SCD1U16V2ZY-2GP
C253 DY SCD1U16V2ZY-2GP
C205 DY SCD1U16V2ZY-2GP
C204 DY SCD1U16V2ZY-2GP
C181 DY SCD1U16V2ZY-2GP
C513 DY SCD1U16V2ZY-2GP
C512 DY SCD1U16V2ZY-2GP
C206 DY SCD1U16V2ZY-2GP
C184 DY SCD1U16V2ZY-2GP

C208 DY SCD1U16V2ZY-2GP
C207 DY SCD1U16V2ZY-2GP
C214 DY SCD1U16V2ZY-2GP
C514 DY SCD1U16V2ZY-2GP
C515 DY SCD1U16V2ZY-2GP
C212 DY SCD1U16V2ZY-2GP
C213 DY SCD1U16V2ZY-2GP
C256 DY SCD1U16V2ZY-2GP
C258 DY SCD1U16V2ZY-2GP
C211 DY SCD1U16V2ZY-2GP
C186 DY SCD1U16V2ZY-2GP
C255 DY SCD1U16V2ZY-2GP
C215 DY SCD1U16V2ZY-2GP

Place these Caps near DM1

D8V_S3

C516 SC2D2U10V3ZY-1GP
C199 SC2D2U10V3ZY-1GP
C185 SC2D2U10V3ZY-1GP
C257 SC2D2U10V3ZY-1GP
C203 SC2D2U10V3ZY-1GP

C518 SCD1U16V2ZY-2GP
C517 SCD1U16V2ZY-2GP
C209 SCD1U16V2ZY-2GP
C200 SCD1U16V2ZY-2GP

Place these Caps near DM2

1D8V_S3

C535 SC2D2U10V3ZY-1GP
C202 SC2D2U10V3ZY-1GP
C201 SC2D2U10V3ZY-1GP
C198 SC2D2U10V3ZY-1GP
C251 SC2D2U10V3ZY-1GP

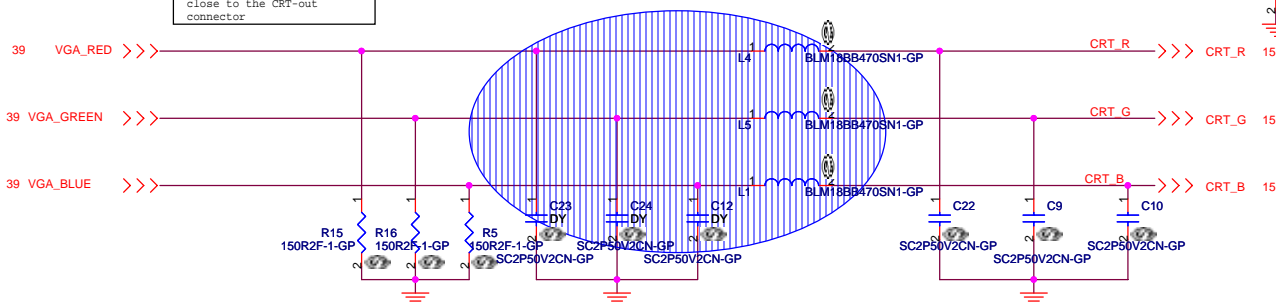
C252 SCD1U16V2ZY-2GP
C197 SCD1U16V2ZY-2GP
C210 SCD1U16V2ZY-2GP
C196 SCD1U16V2ZY-2GP

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Title	
DDR2 Termination Resistor Document Number	
Size A3	Rev SA
Date: Monday, November 28, 2005	
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CRT I/F & CONNECTOR

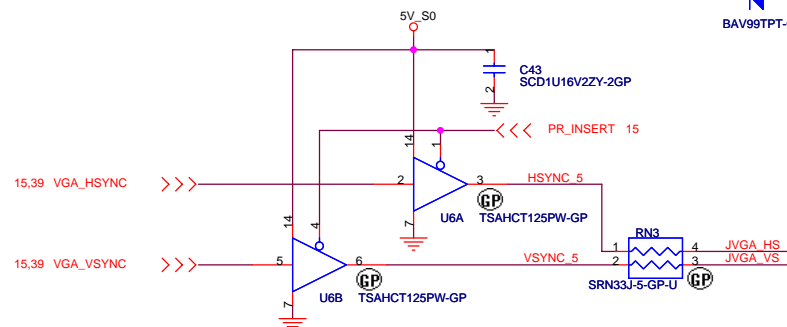
Layout Note:
Place these resistors
close to the CRT-out
connector



Layout Note:

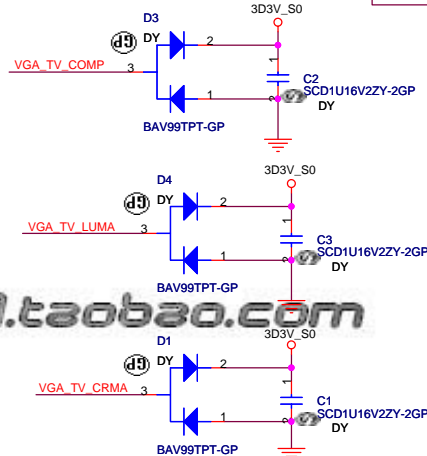
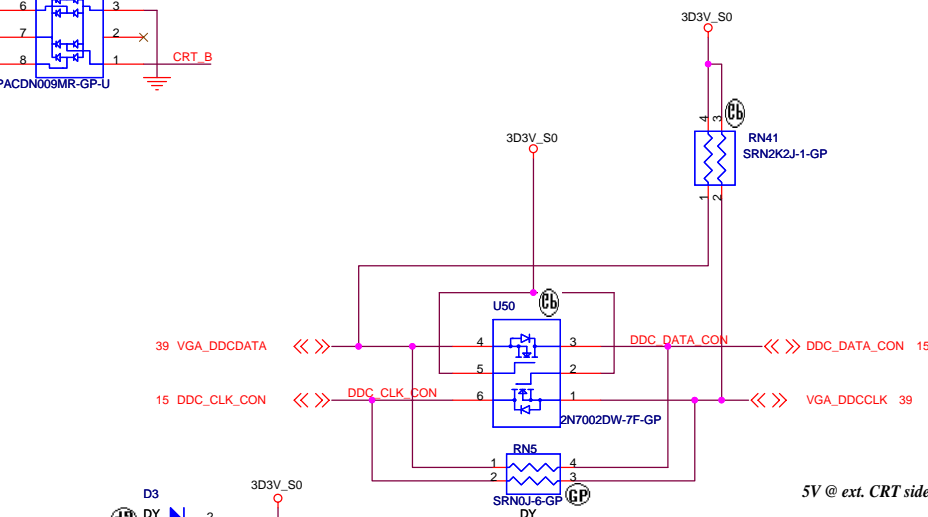
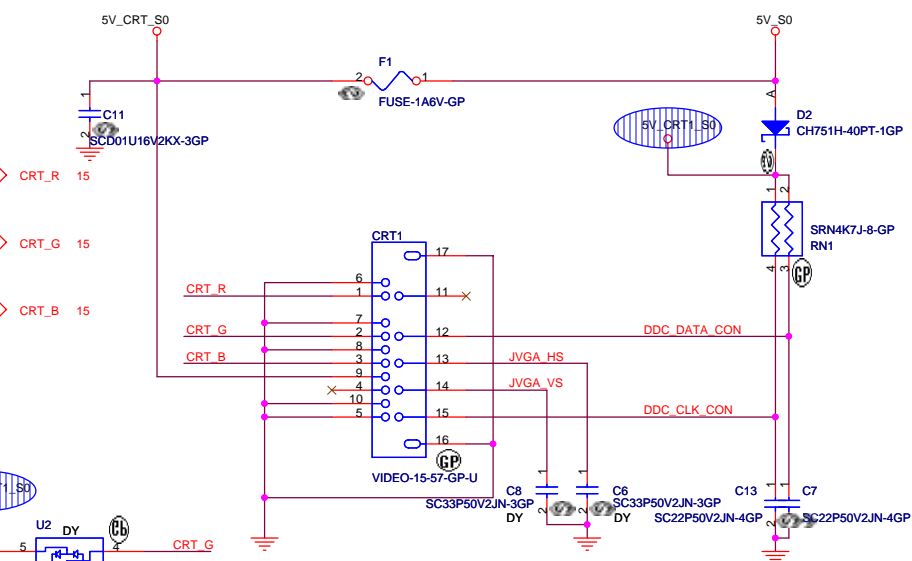
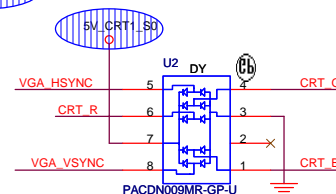
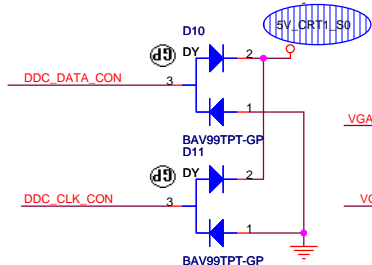
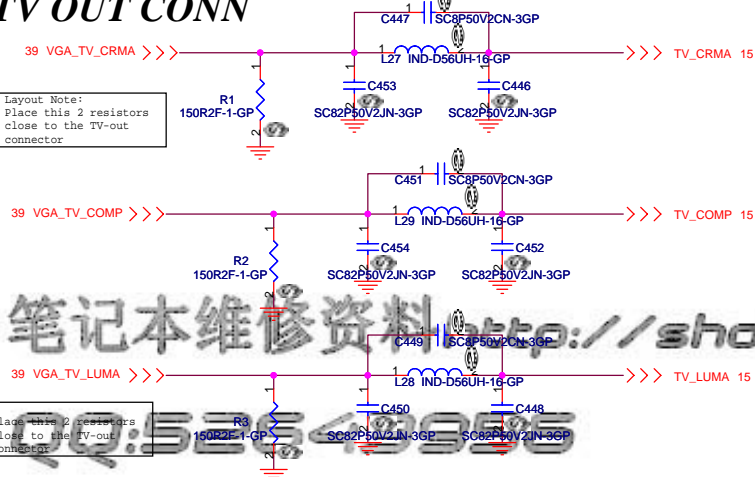
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift



TV OUT CONN

Layout Note:
Place this 2 resistors
close to the TV-out
connector



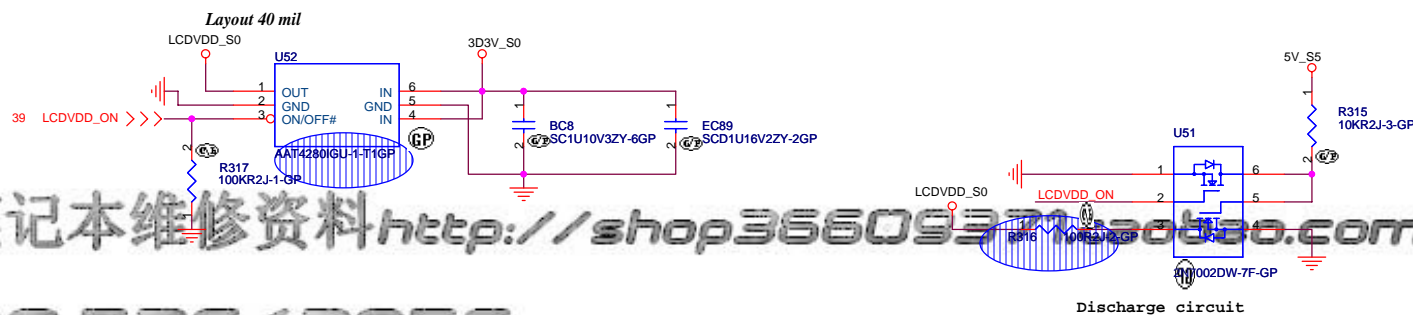
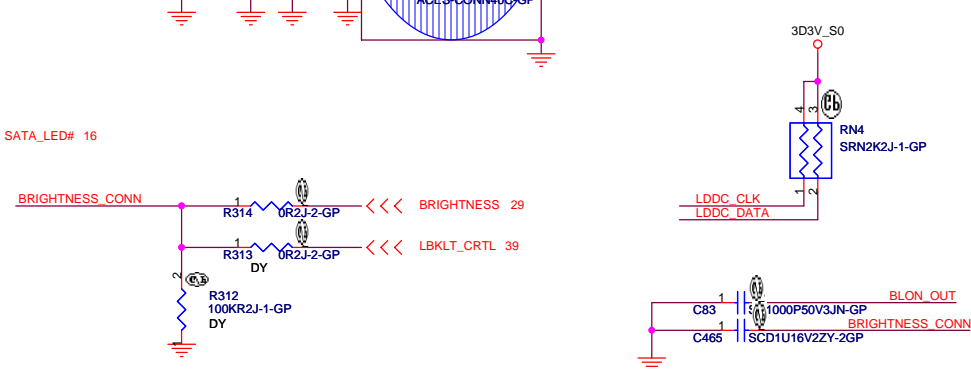
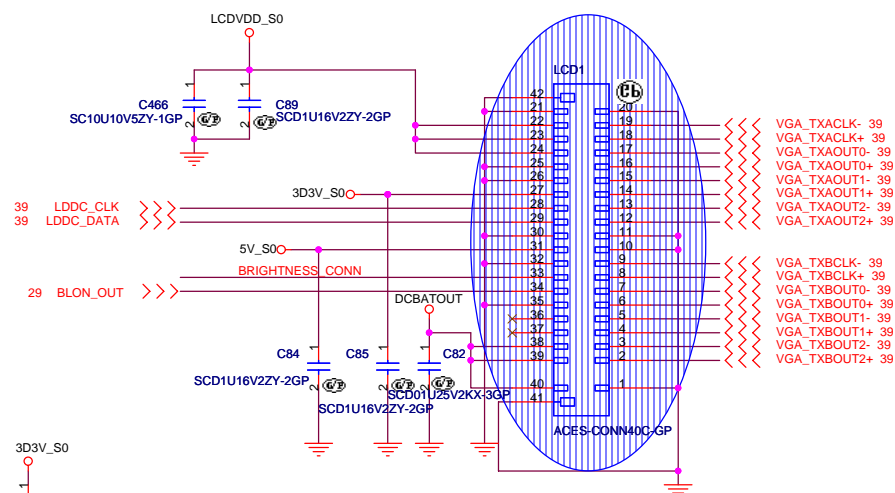
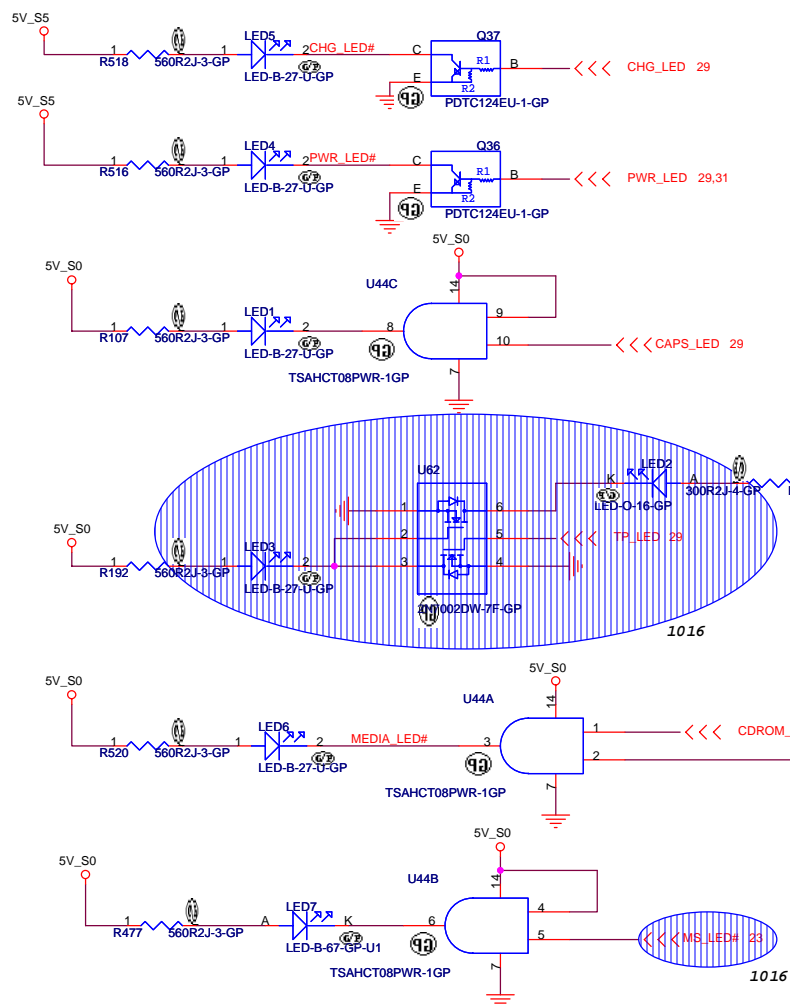
<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

CRT/TV Connector			
Size A3	Document Number	KAI	
Date: Monday, November 28, 2005	Sheet 13	of	44

LCD/INV CONN



笔记本维修资料 <http://shop36609377.taobao.com>

QQ:52643956

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LCD/Inverter Connector

Size	Custom
------	--------

Document Number

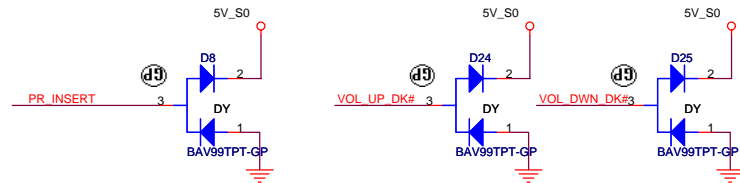
KAI

Rev	5
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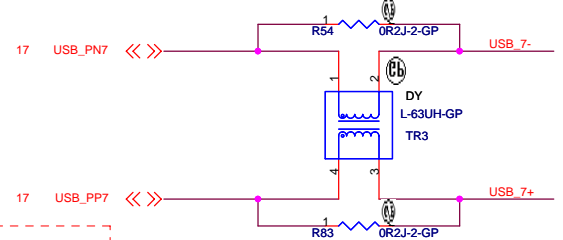
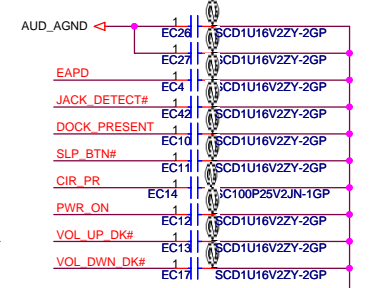
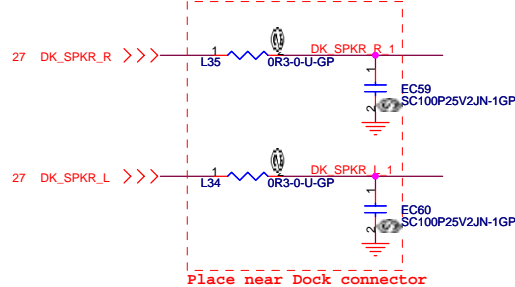
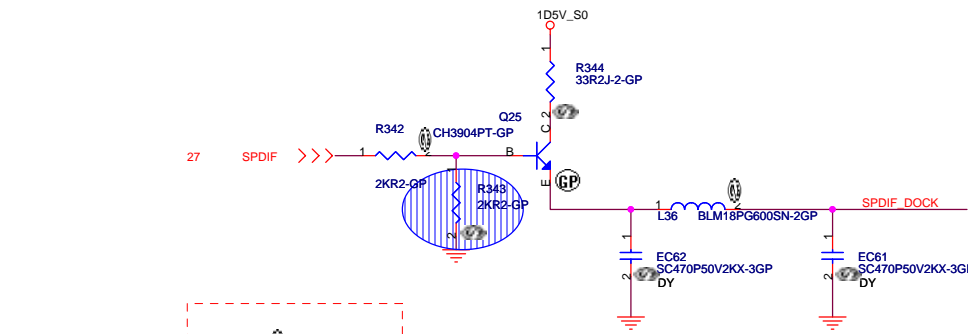
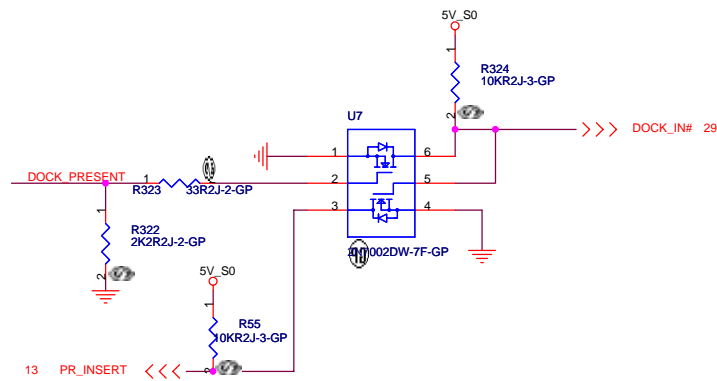
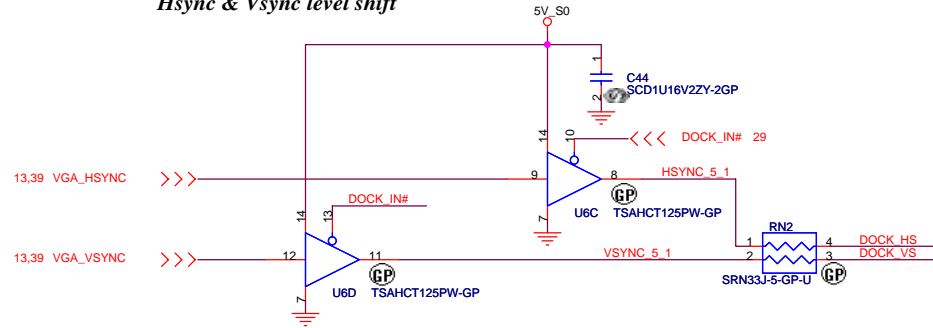
Date: Monday, November 28, 2005

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Docking Connector



Hsync & Vsync level shift



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QQ:52643956

緯創資通 Wistron Corporation
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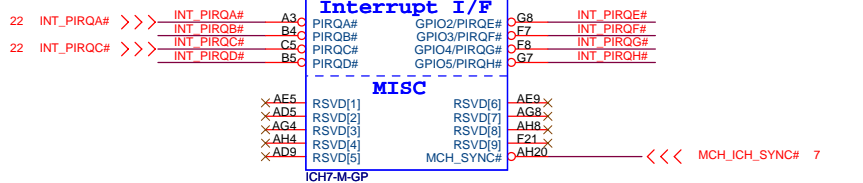
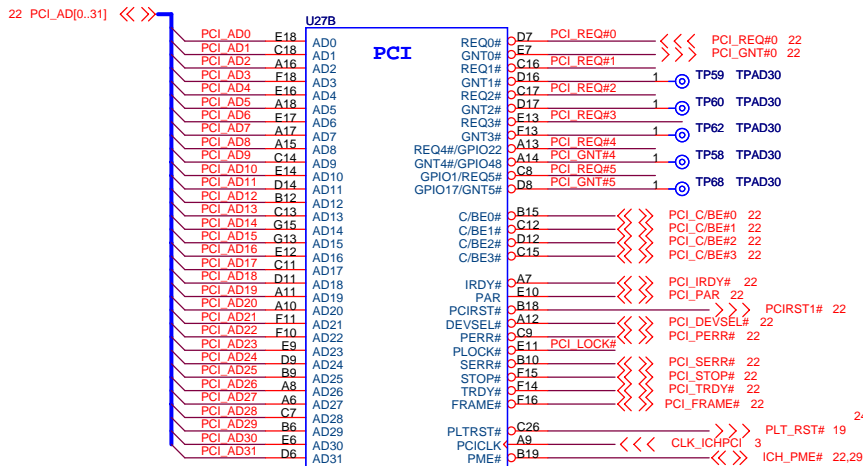
Board to board conn/ Docking

Title: **KAI**

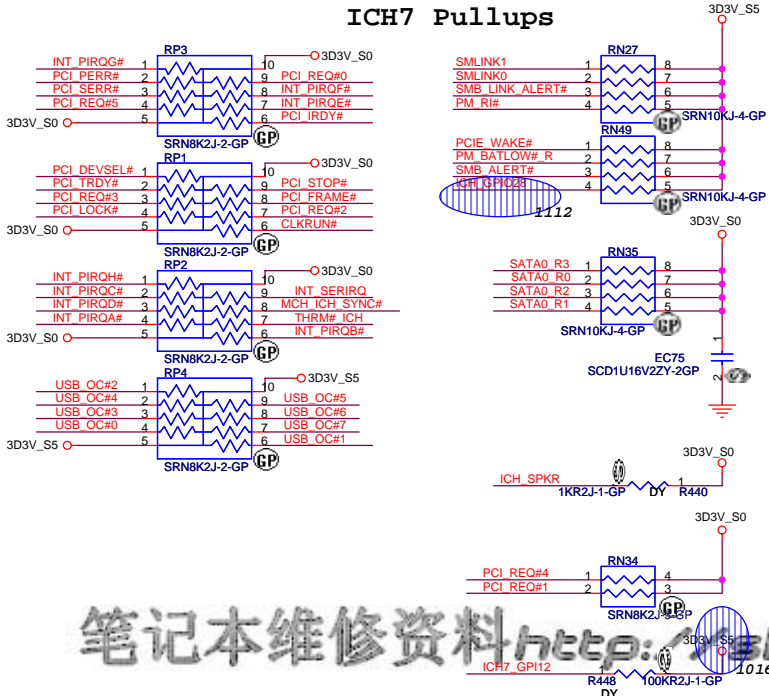
Size: A3 Document Number: **KAI** Rev: SA

Date: Monday, November 28, 2005 Sheet: 15 of 44



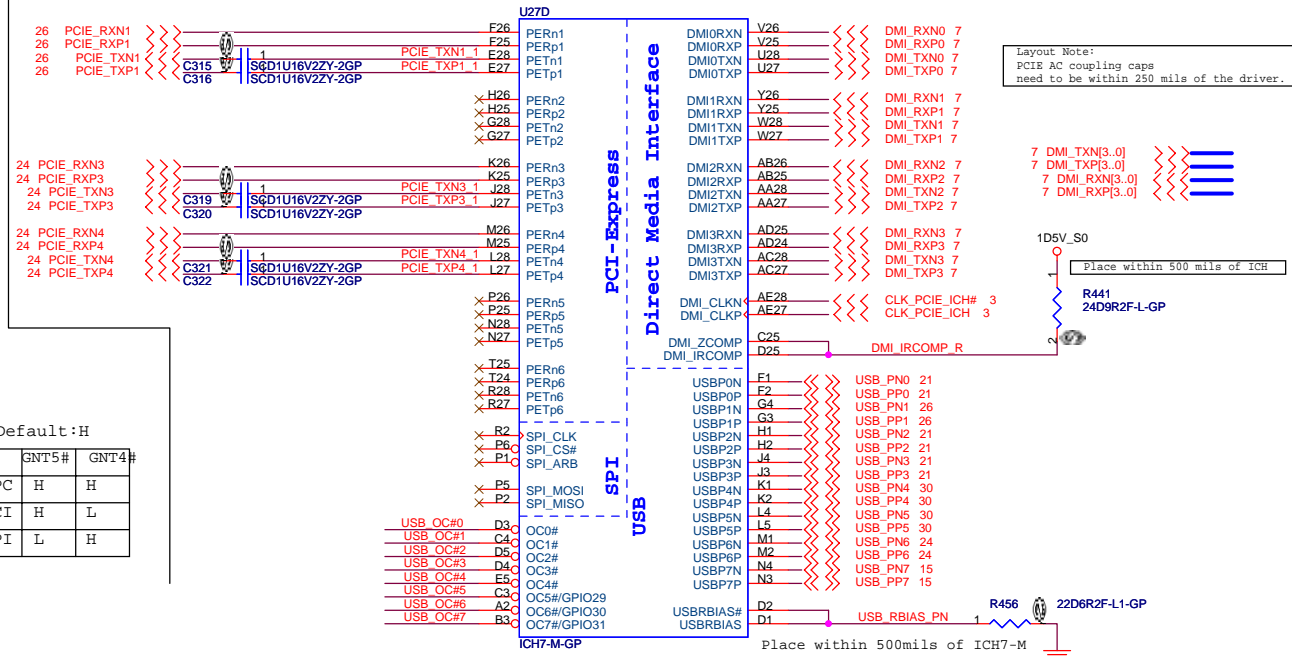
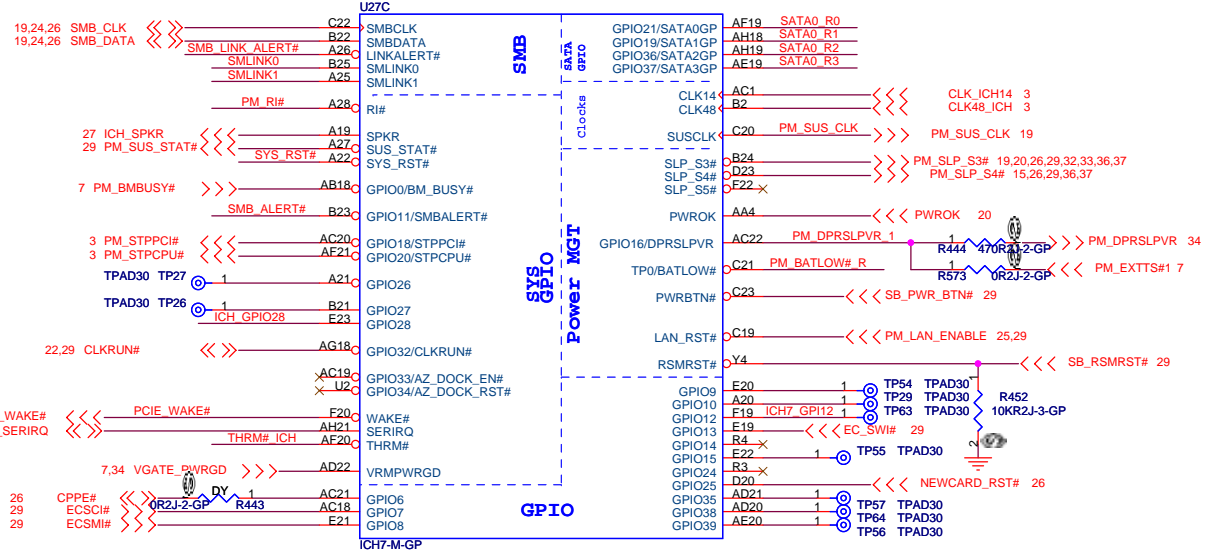


ICH7 Pullups



Default: H

	GNT5#	GNT4#
LPC	H	H
PCI	H	L
SPI	L	H



Layout Note:
PCIe AC coupling caps
need to be within 250 mils of the driver.

Place within 500 mils of ICH

Place within 500mils of ICH7-M

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QQ:52643956

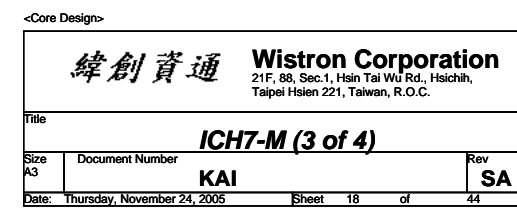
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

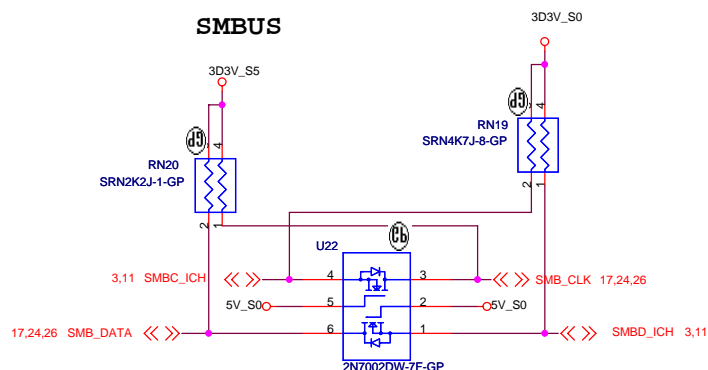
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Size: A3 Document Number: **KAI** Rev: **SA**

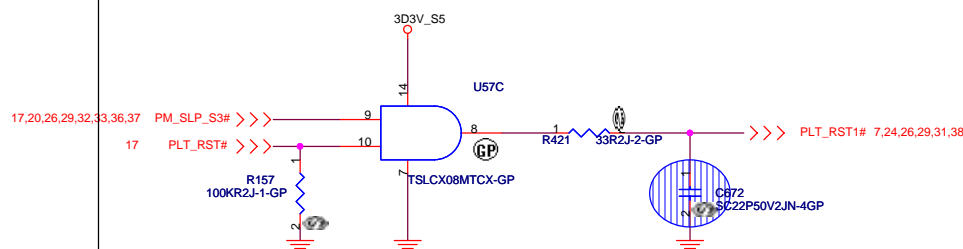
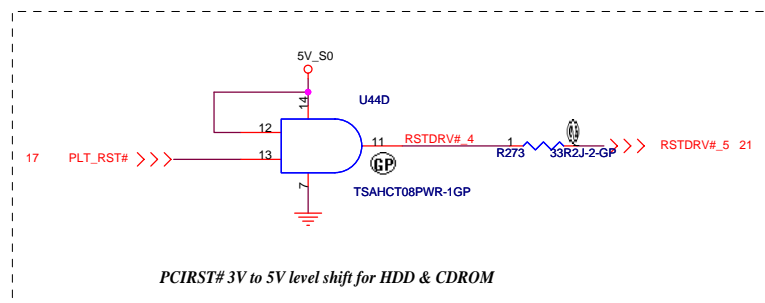
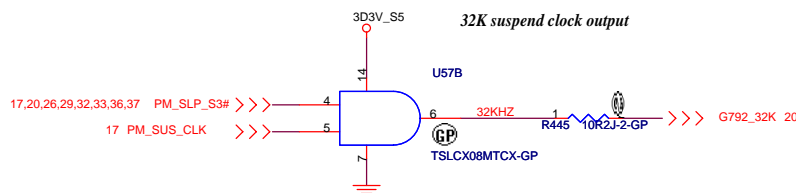
Date: Wednesday, November 30, 2005 Sheet: 17 of 44



SMBUS



Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

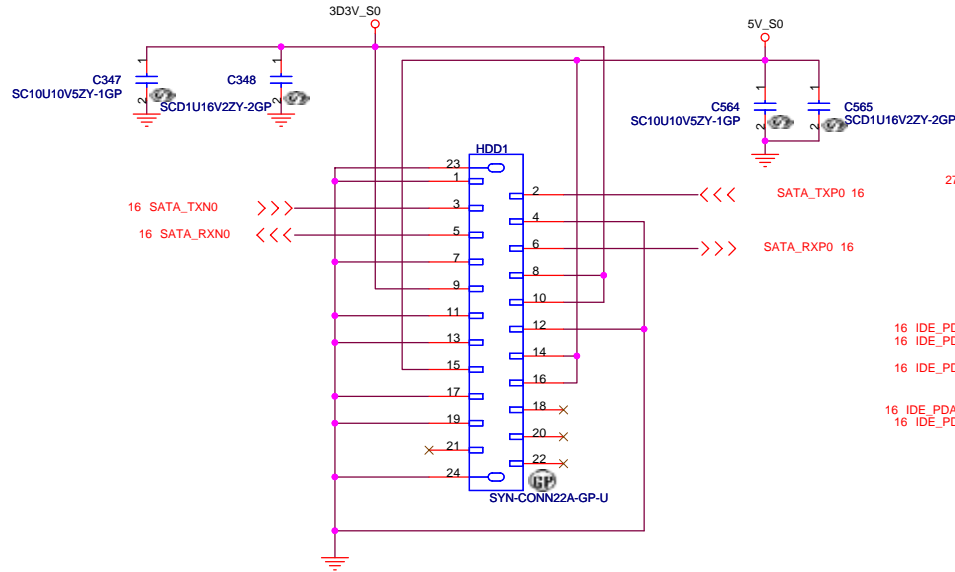


A4	VSS[1]	VSS[98]	P28
A23	VSS[2]	VSS[99]	R1
B1	VSS[3]	VSS[100]	R11
B8	VSS[4]	VSS[101]	R12
B11	VSS[5]	VSS[102]	R13
B14	VSS[6]	VSS[103]	R14
B17	VSS[7]	VSS[104]	R15
B20	VSS[8]	VSS[105]	R16
B28	VSS[9]	VSS[106]	R17
B28	VSS[10]	VSS[107]	R18
C2	VSS[11]	VSS[108]	T6
C6	VSS[12]	VSS[109]	T12
C27	VSS[13]	VSS[110]	T13
D10	VSS[14]	VSS[111]	T14
D18	VSS[15]	VSS[112]	T15
D21	VSS[16]	VSS[113]	T16
D24	VSS[17]	VSS[114]	T17
E1	VSS[18]	VSS[115]	U4
E2	VSS[19]	VSS[116]	U12
E4	VSS[20]	VSS[117]	U13
E8	VSS[21]	VSS[118]	U14
E15	VSS[22]	VSS[119]	U15
F3	VSS[23]	VSS[120]	U16
F4	VSS[24]	VSS[121]	U17
F5	VSS[25]	VSS[122]	U24
F12	VSS[26]	VSS[123]	U25
F27	VSS[27]	VSS[124]	U26
F28	VSS[28]	VSS[125]	V13
G1	VSS[29]	VSS[126]	V15
G2	VSS[30]	VSS[127]	V16
G5	VSS[31]	VSS[128]	V24
G6	VSS[32]	VSS[129]	V27
G9	VSS[33]	VSS[130]	V28
G14	VSS[34]	VSS[131]	W6
G18	VSS[35]	VSS[132]	W25
G21	VSS[36]	VSS[133]	W26
G24	VSS[37]	VSS[134]	W27
G25	VSS[38]	VSS[135]	Y3
G26	VSS[39]	VSS[136]	Y24
H3	VSS[40]	VSS[137]	Y27
H4	VSS[41]	VSS[138]	Y28
H5	VSS[42]	VSS[139]	AA1
H24	VSS[43]	VSS[140]	AA24
H27	VSS[44]	VSS[141]	AA25
H28	VSS[45]	VSS[142]	AA26
J1	VSS[46]	VSS[143]	AB4
J2	VSS[47]	VSS[144]	AB6
J5	VSS[48]	VSS[145]	AB14
J24	VSS[49]	VSS[146]	AB16
J25	VSS[50]	VSS[147]	AB19
J26	VSS[51]	VSS[148]	AB21
K24	VSS[52]	VSS[149]	AB24
K27	VSS[53]	VSS[150]	AB27
K28	VSS[54]	VSS[151]	AB28
L13	VSS[55]	VSS[152]	AC2
L15	VSS[56]	VSS[153]	AC5
L24	VSS[57]	VSS[154]	AC9
L25	VSS[58]	VSS[155]	AC11
L26	VSS[59]	VSS[156]	AD1
M3	VSS[60]	VSS[157]	AD3
M4	VSS[61]	VSS[158]	AD4
M5	VSS[62]	VSS[159]	AD7
M12	VSS[63]	VSS[160]	AD8
M13	VSS[64]	VSS[161]	AD11
M14	VSS[65]	VSS[162]	AD15
M15	VSS[66]	VSS[163]	AD19
M16	VSS[67]	VSS[164]	AD23
M17	VSS[68]	VSS[165]	AE2
M24	VSS[69]	VSS[166]	AE4
M27	VSS[70]	VSS[167]	AE8
M28	VSS[71]	VSS[168]	AE11
N1	VSS[72]	VSS[169]	AE13
N2	VSS[73]	VSS[170]	AE18
N5	VSS[74]	VSS[171]	AE21
N6	VSS[75]	VSS[172]	AE24
N11	VSS[76]	VSS[173]	AE25
N12	VSS[77]	VSS[174]	AE2
N13	VSS[78]	VSS[175]	AF4
N14	VSS[79]	VSS[176]	AF9
N15	VSS[80]	VSS[177]	AF11
N16	VSS[81]	VSS[178]	AF27
N17	VSS[82]	VSS[179]	AF28
N18	VSS[83]	VSS[180]	AG1
N24	VSS[84]	VSS[181]	AG3
N25	VSS[85]	VSS[182]	AG7
N26	VSS[86]	VSS[183]	AG11
P3	VSS[87]	VSS[184]	AG14
P4	VSS[88]	VSS[185]	AG17
P12	VSS[89]	VSS[186]	AG20
P13	VSS[90]	VSS[187]	AG25
P14	VSS[91]	VSS[188]	AH1
P15	VSS[92]	VSS[189]	AH3
P16	VSS[93]	VSS[190]	AH7
P17	VSS[94]	VSS[191]	AH12
P24	VSS[95]	VSS[192]	AH23
P27	VSS[96]	VSS[193]	AH27
P27	VSS[97]	VSS[194]	

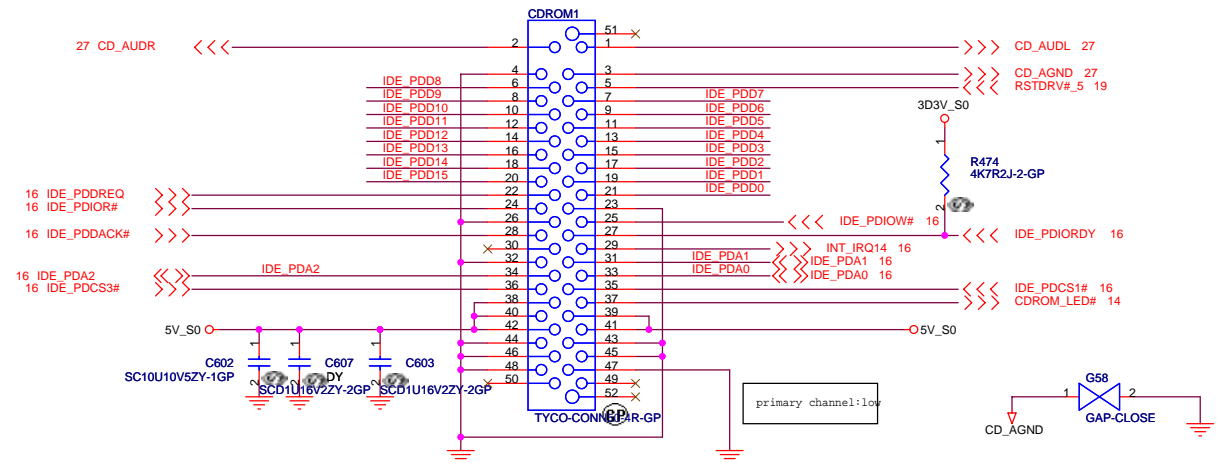
笔记本维修资料 <http://shop36609371.taobao.com>
 QQ:52643956



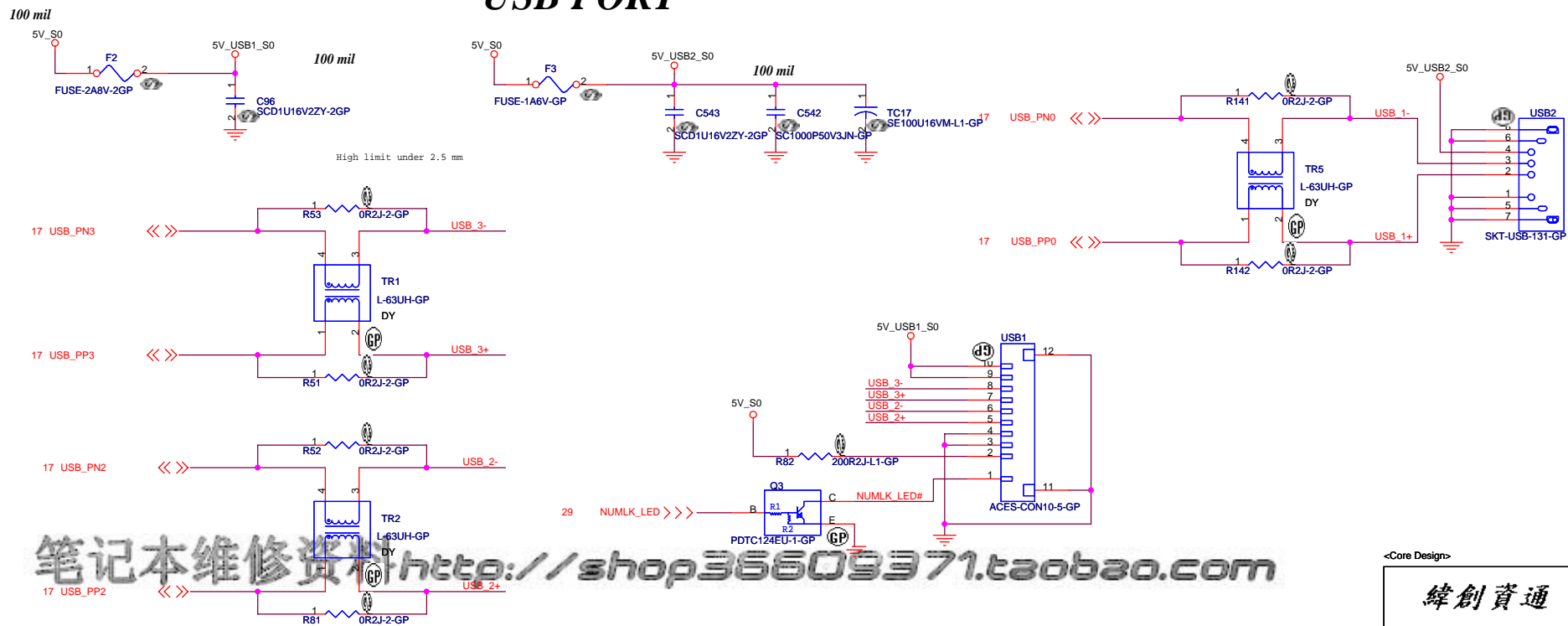
SATA HD Connector



CD-ROM CONNECTOR



USB PORT



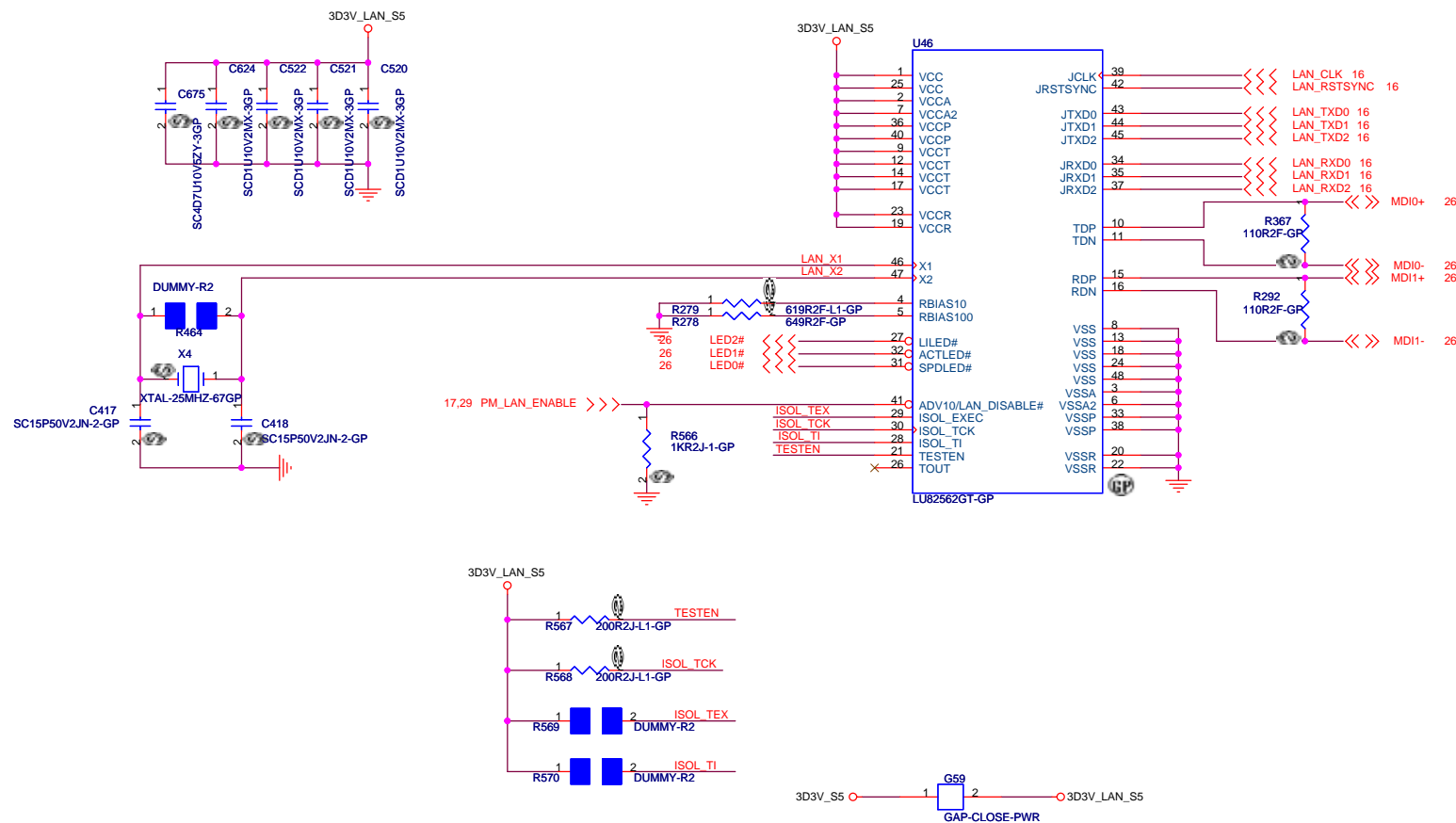
笔记本维修资料 <http://shop36609371.taobao.com>
QQ:52643956

<Core Design>

Mini Card Connector 1

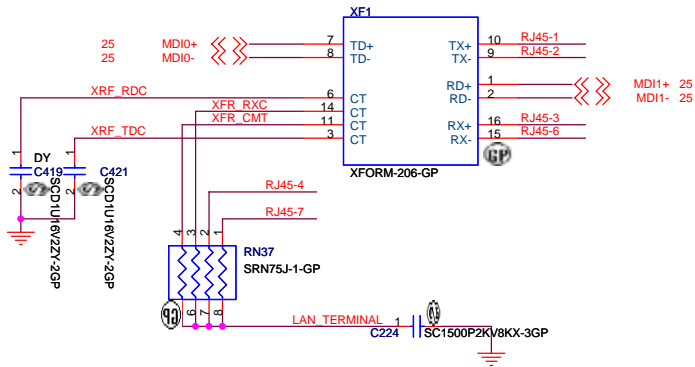


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MINI CARD CONN .			
Size A3	Document Number		Rev
	KAI		SA
Date:	Monday, November 28, 2005	Sheet	24 of 44



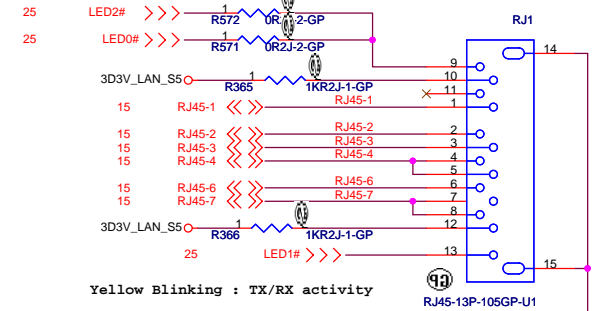
笔记本维修资料 <http://shop36609371.taobao.com>
 QQ:52643956

10/100M Lan Transformer



1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

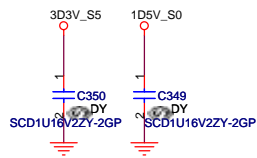
Green : Link 10/100 Mbps



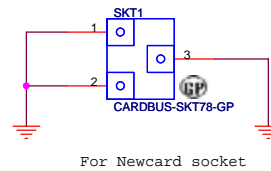
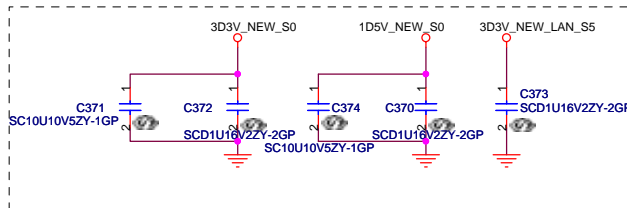
PIN09 : GREEN
PIN11 : ORANGE
PIN13 : YELLOW

NEWCARD Connector

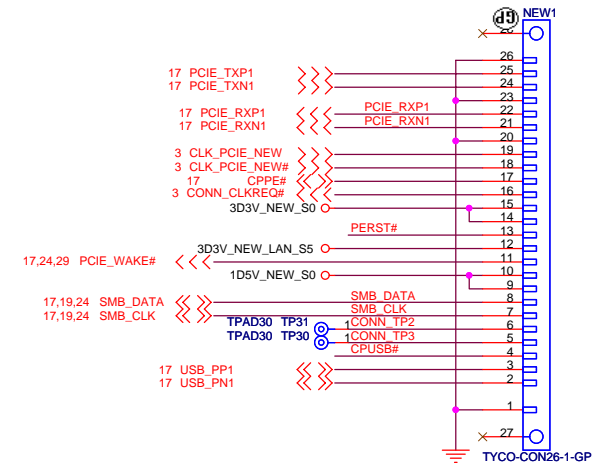
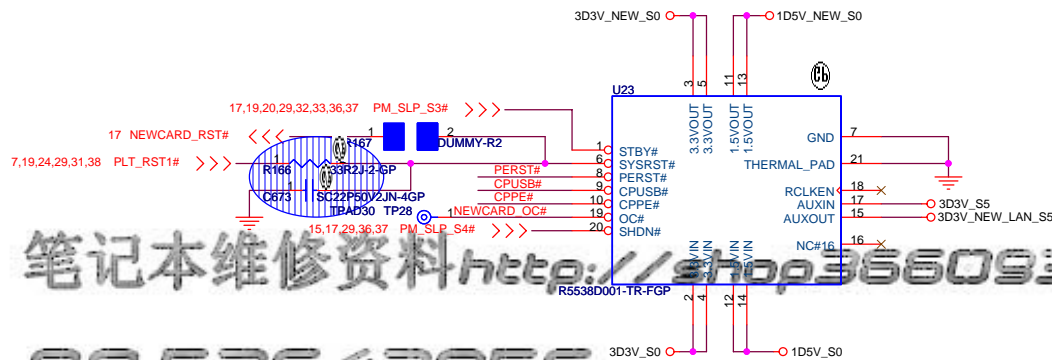
Place them Near to Chip



Place them Near to Connector



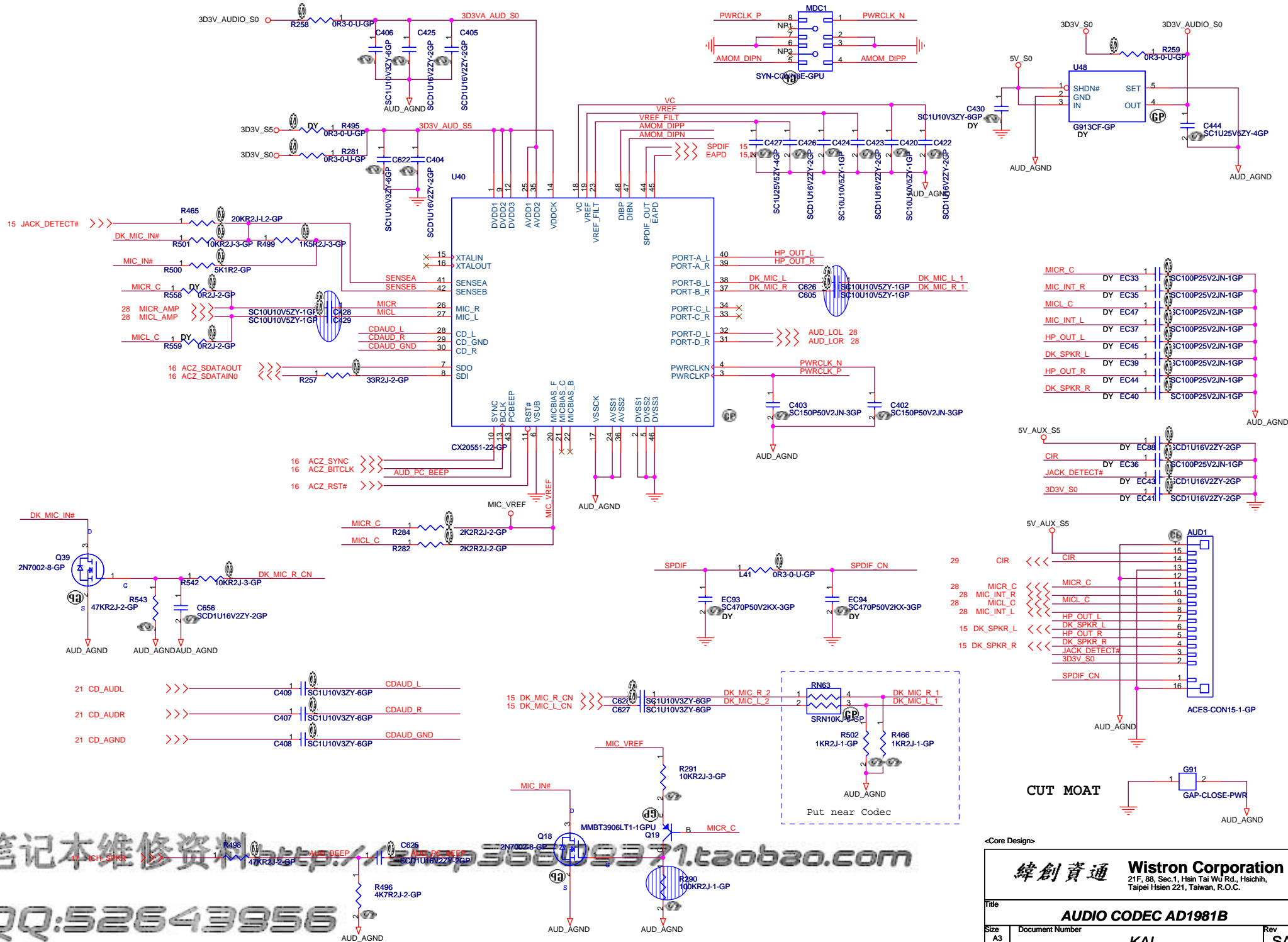
For Newcard socket

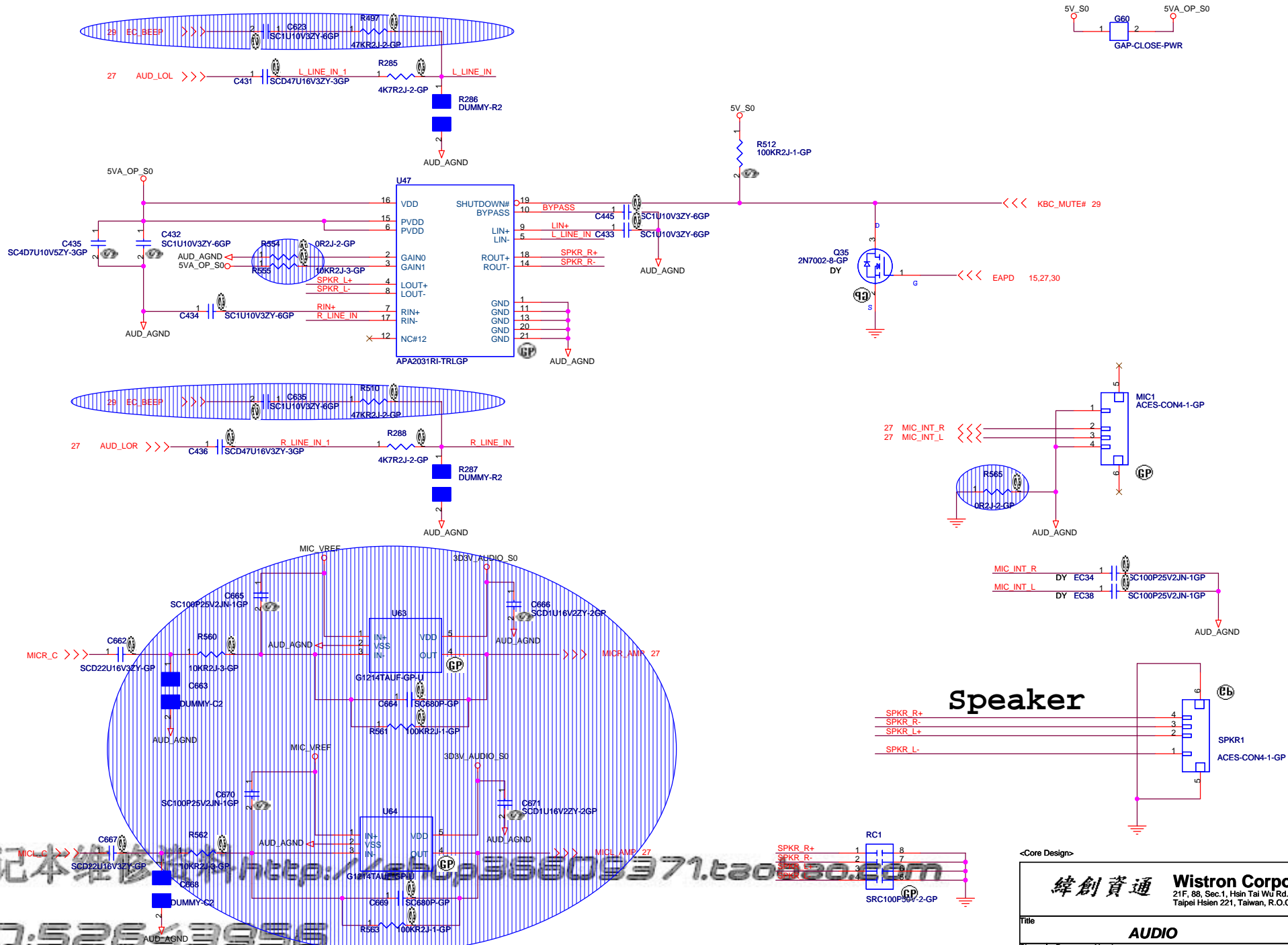


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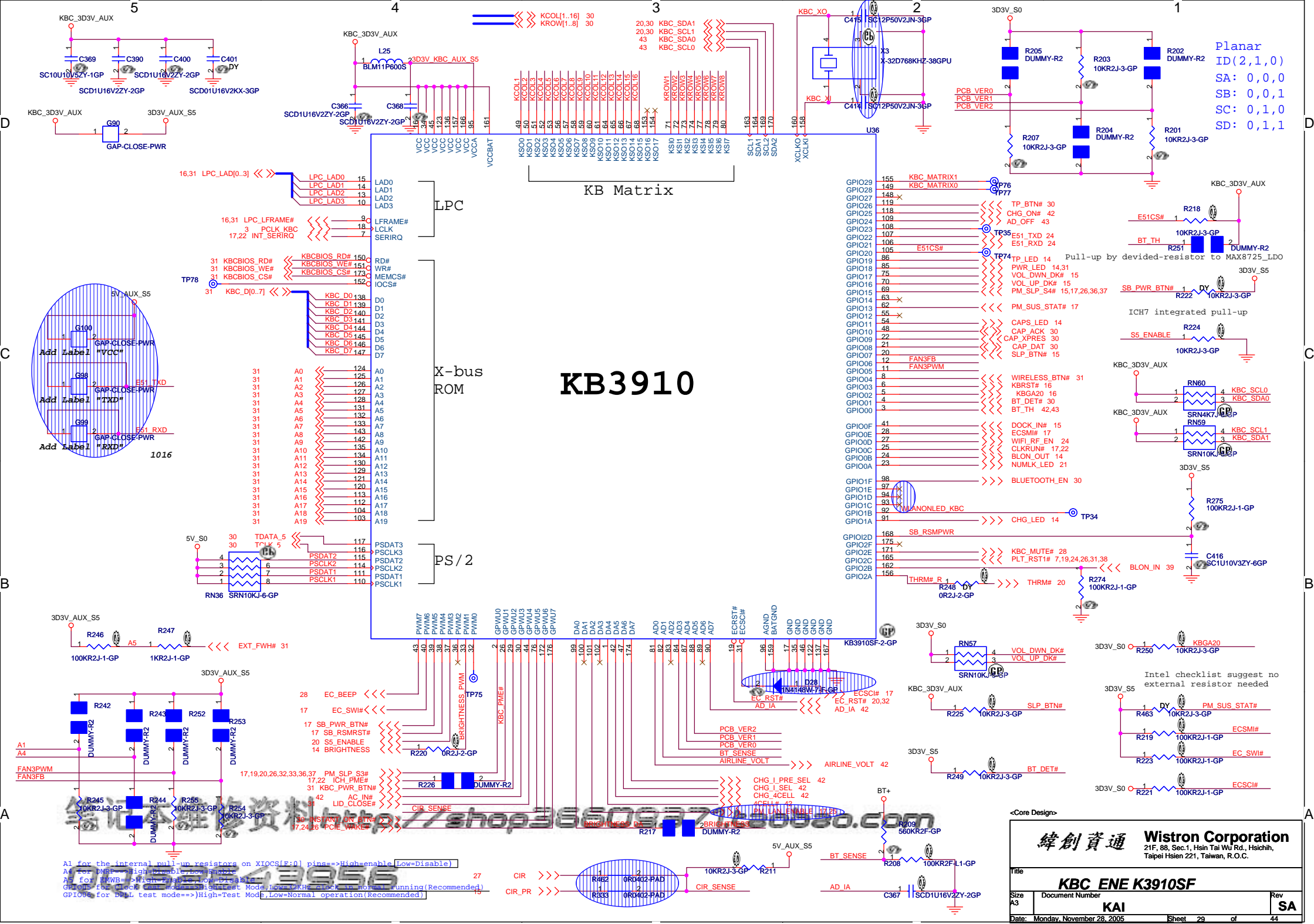
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	New Card		
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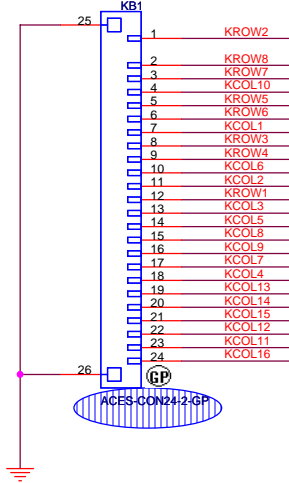


Internal KeyBoard Connector

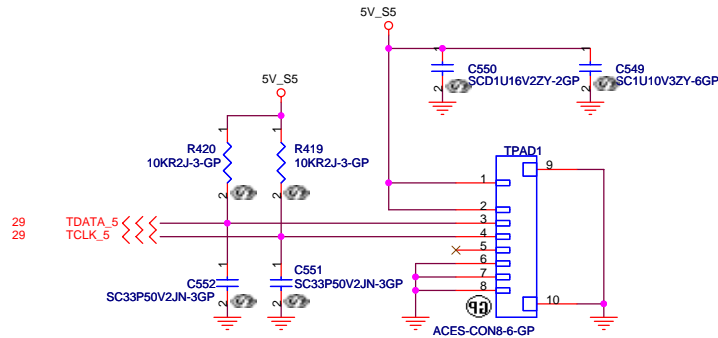
29 KROW[1..8] <<< 
29 KCOL[1..16] <<< 

Keyboard matrix (from vendor)

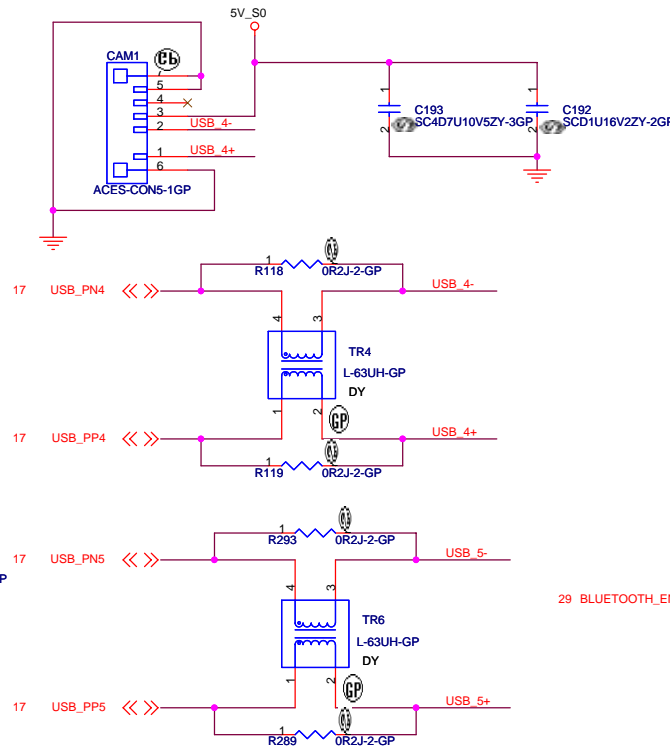
	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1



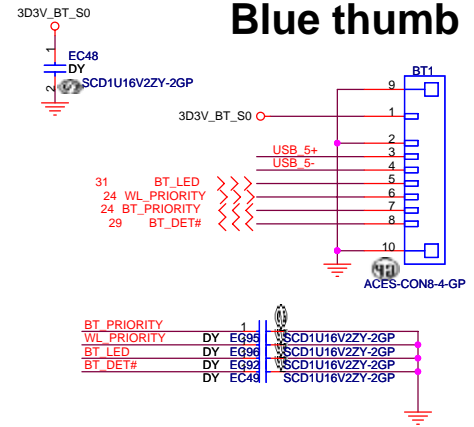
TouchPad Connector



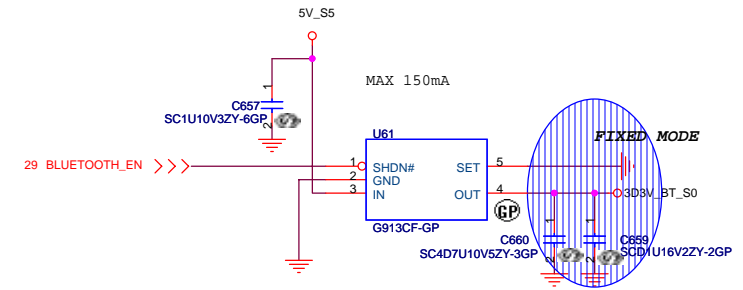
CAMERA



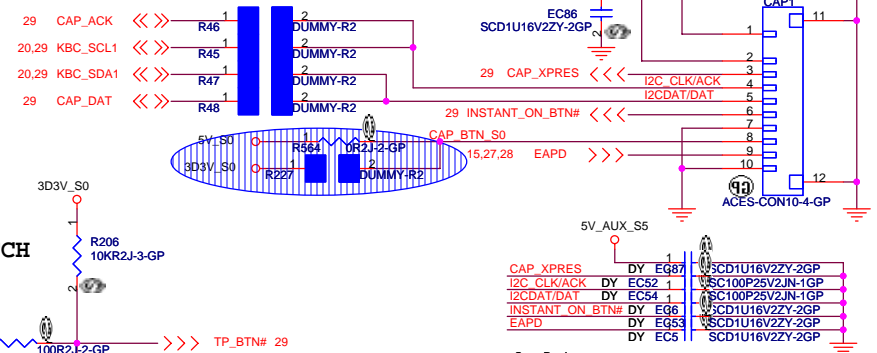
Blue thumb



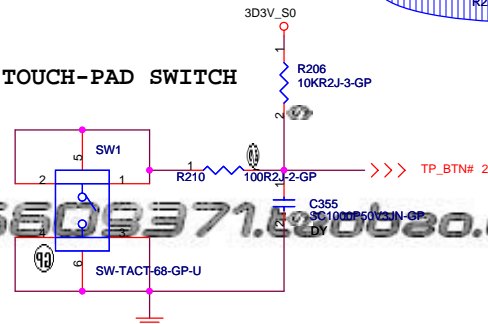
Close to BT1



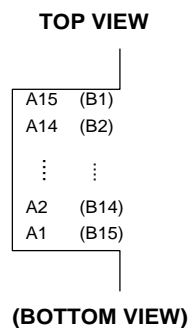
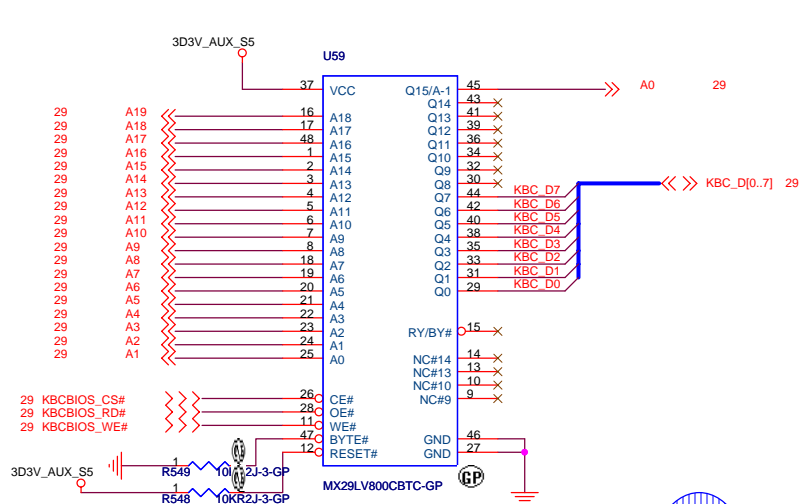
CAPACITY BUTTON



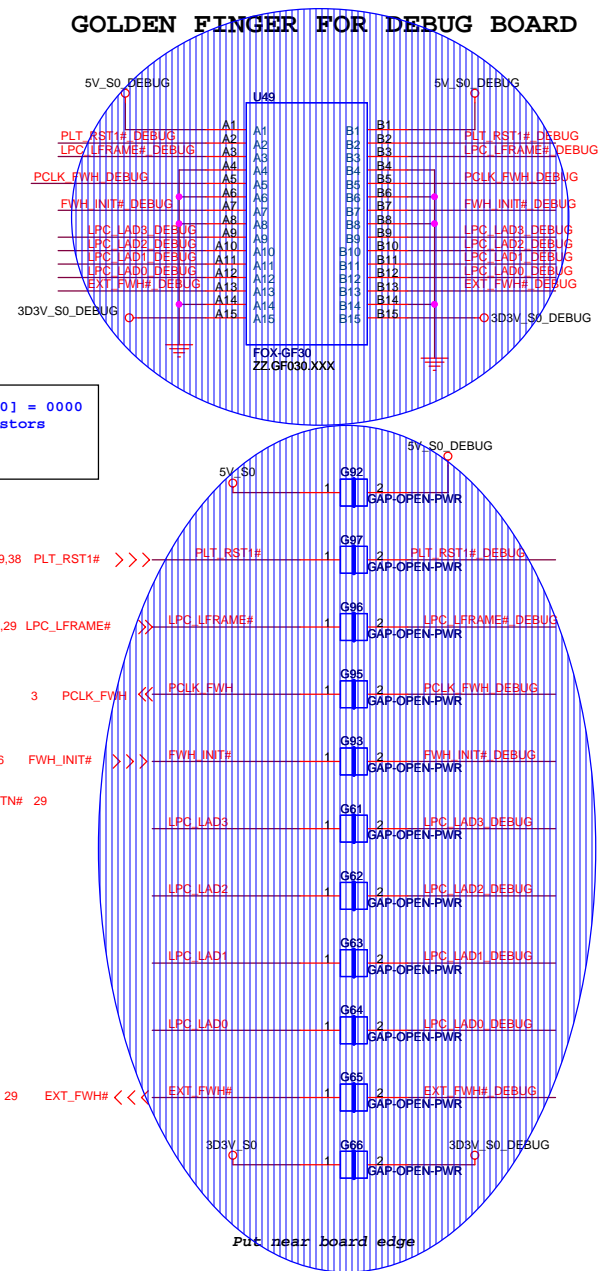
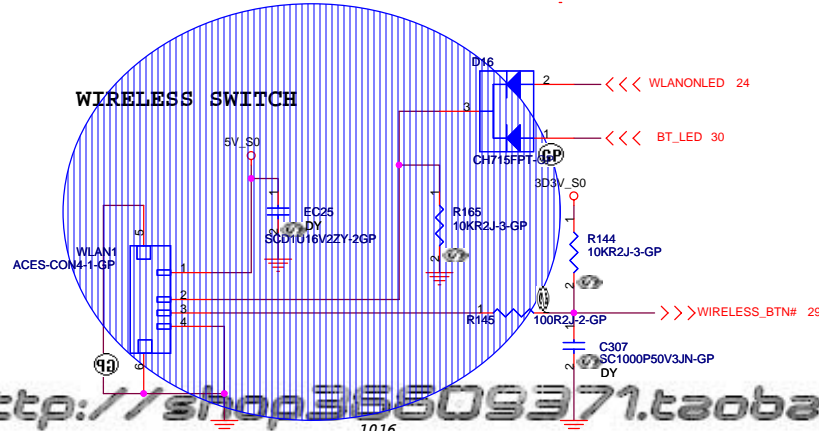
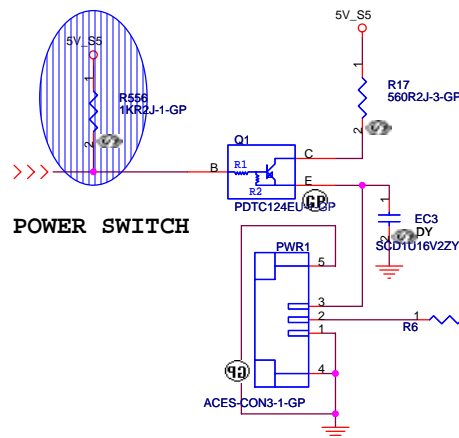
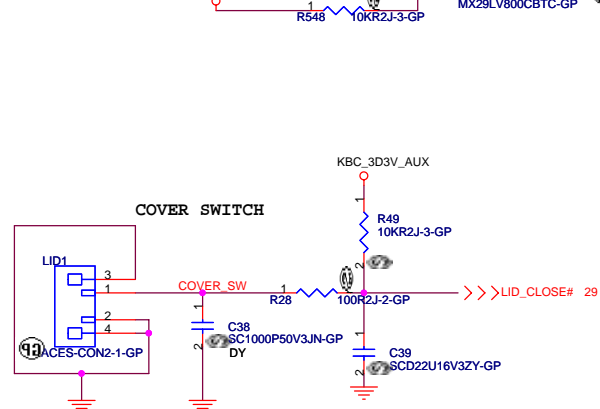
TOUCH-PAD SWITCH



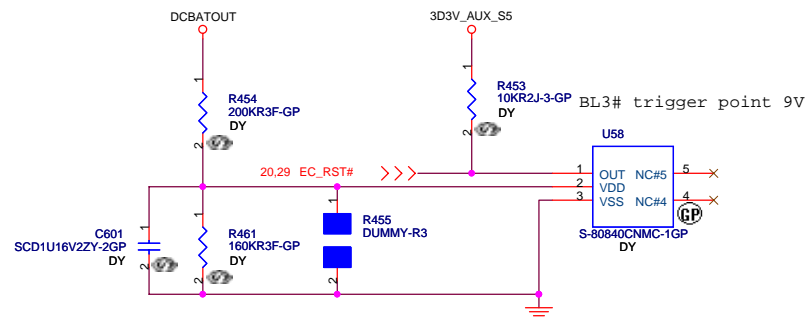
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QQ:52643956



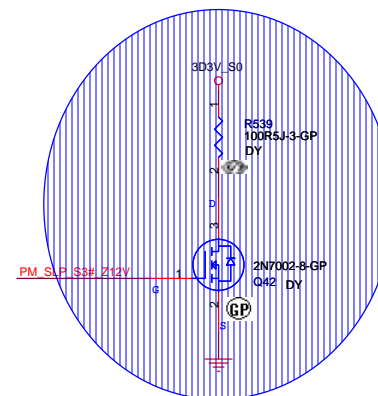
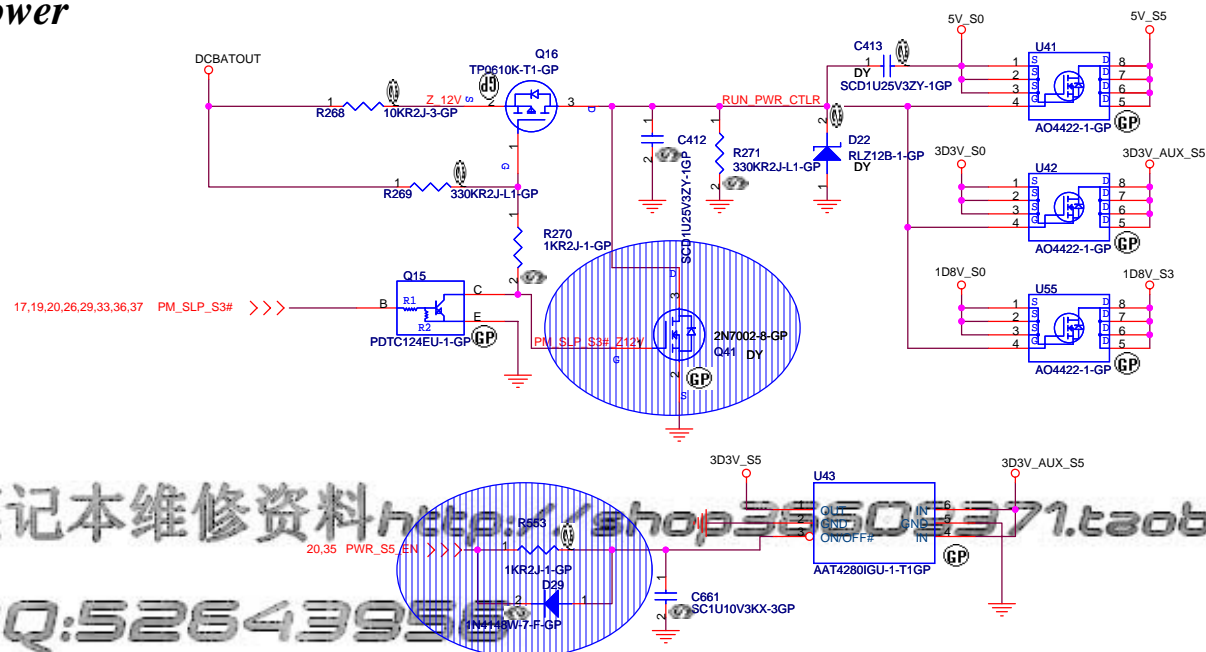
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



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QQ:52643956



Run Power



笔记本维修资料 <http://shop38509371.taobao.com>

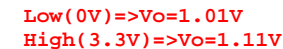
QQ:52643956

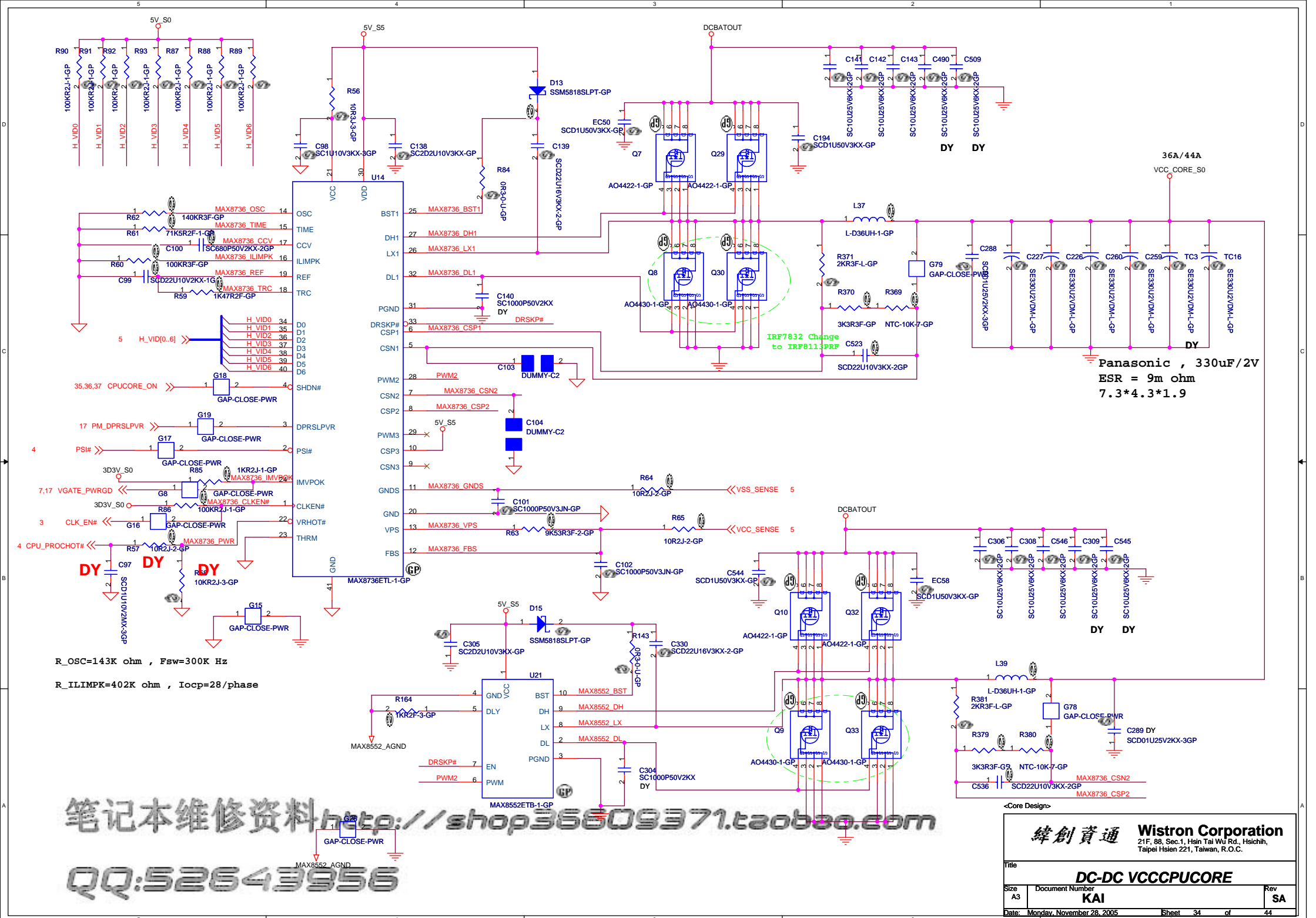
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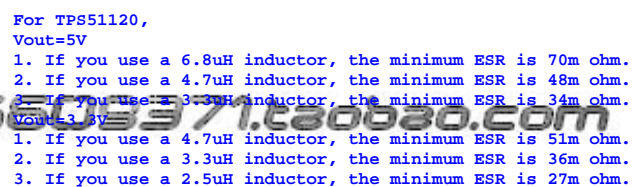
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
PWRPLANE&RESETLOGIC			
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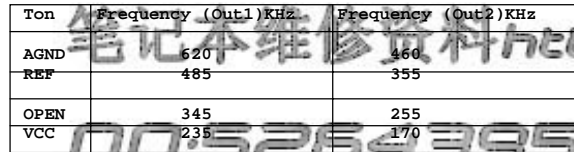




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$I_{ocp}=7.0*2 = 14A$
 $R_{ds,on}=17m\ ohm$
 $V_{cs2}=I_{ocp}*R_{ds,on}=28mV$
 $V_{ILIM2}=V_{cs2}/0.1=2.38V$

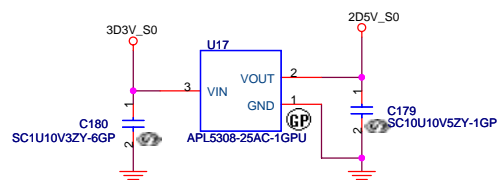
1D05V_S0/7A
OCP>=14A



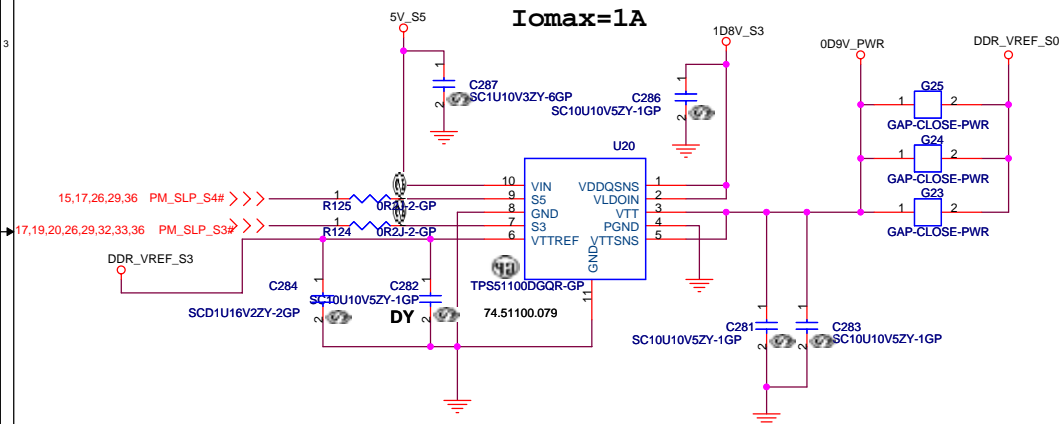
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
1D8V_S3/1D5V_S0			
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2D5V_S0
Iomax=300mA

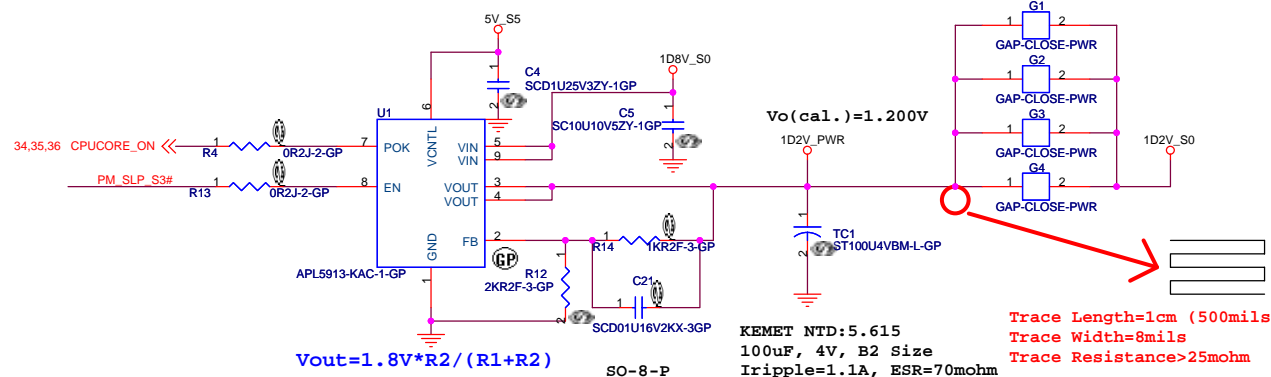


0D9V
Iomax=1A



$$Vo = 0.8 * (1 + (R1/R2))$$

1D2V_S0
Iomax=3A



$$Vout = 1.8V * R2 / (R1 + R2)$$

1D5V_S0
Iomax= 3 A

OCP=6A

Trace Length=3cm
Trace Width=5mils
Trace Resistance>80mohm

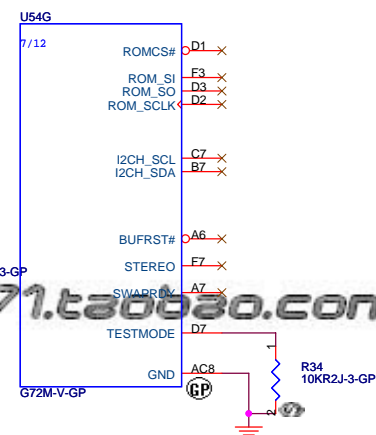
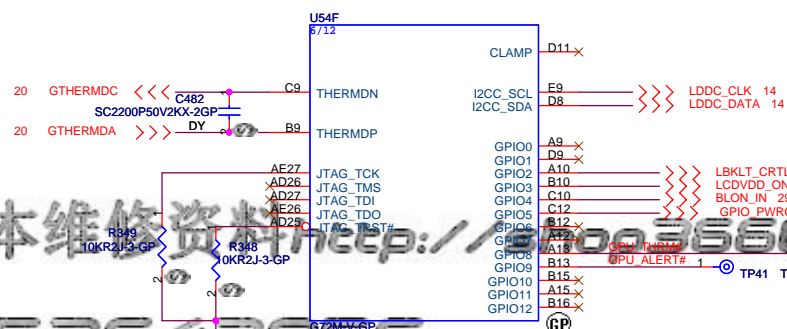
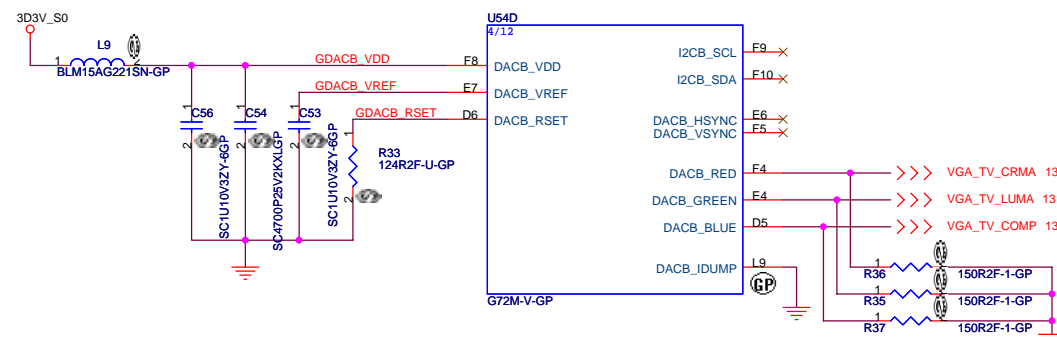
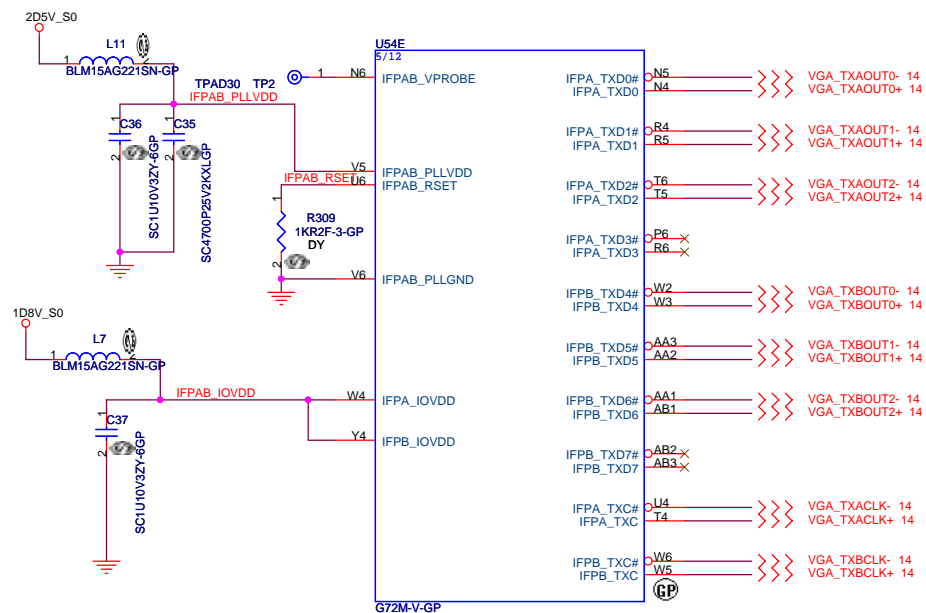
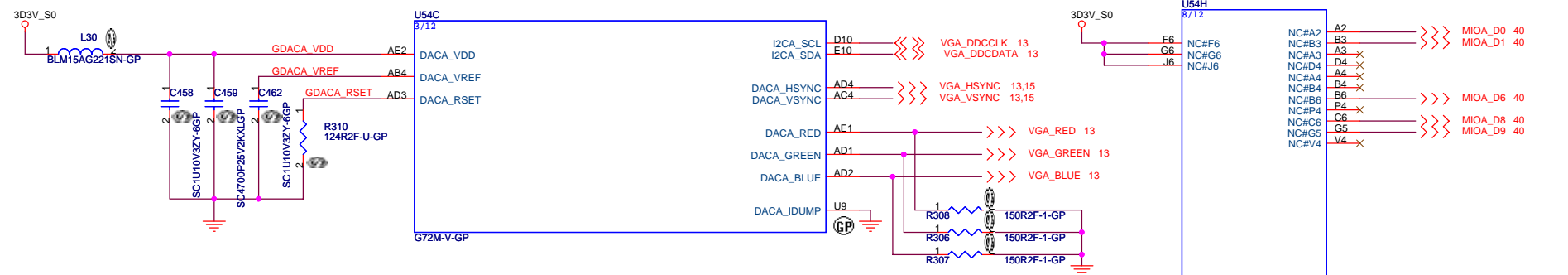
KEMET NTD:5.615
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm

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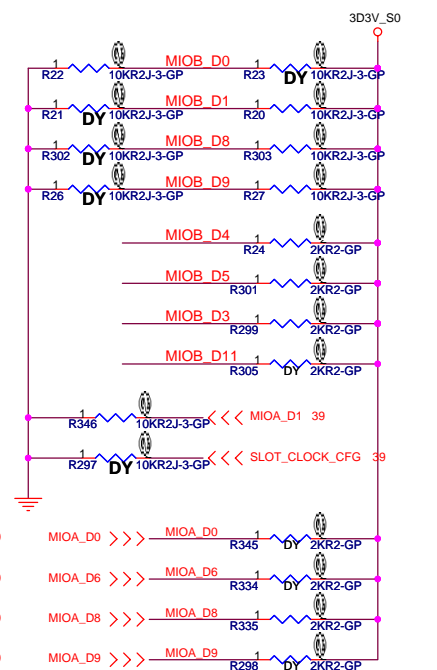
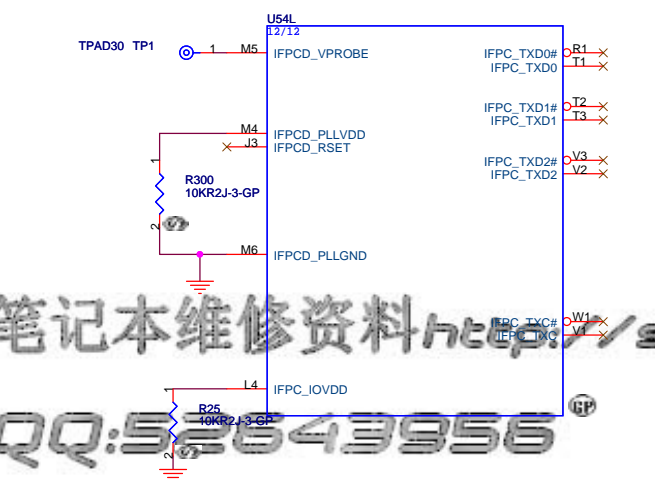
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0D9V_LDO/1D2V_LDO/1D5V_LDO/2D5V_LDO	
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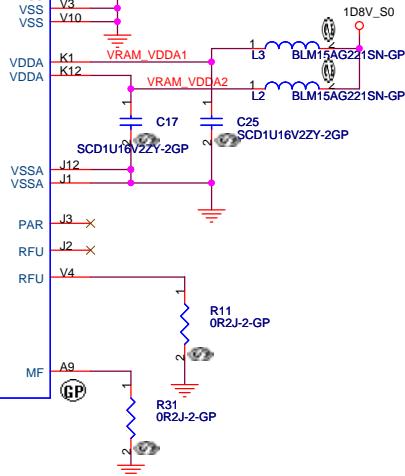
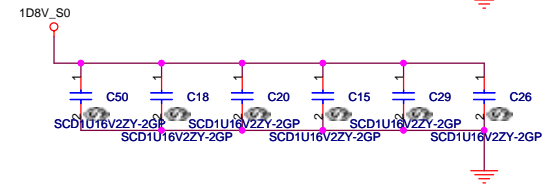
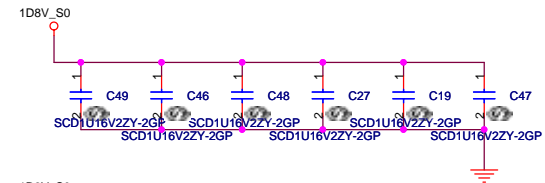
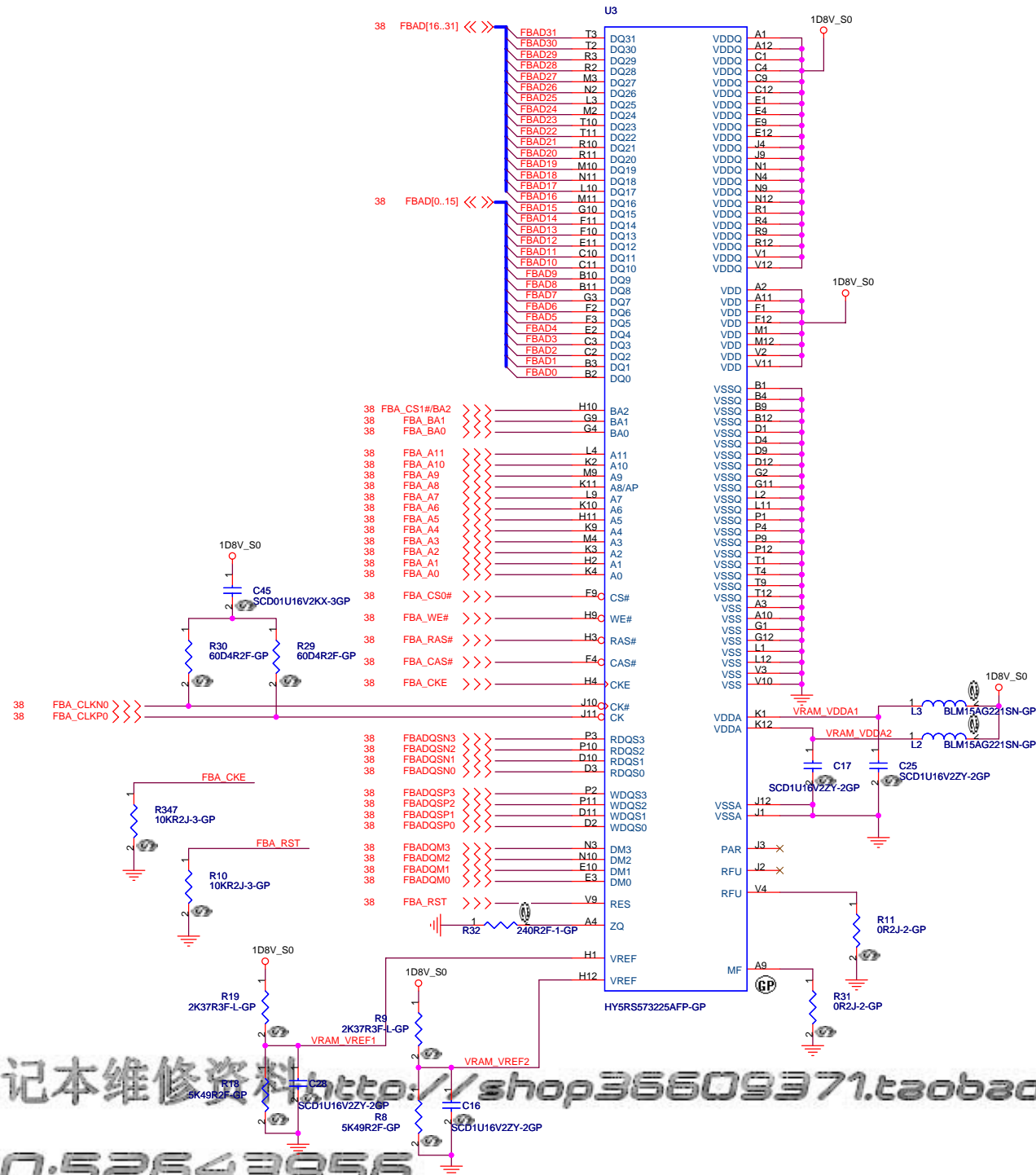


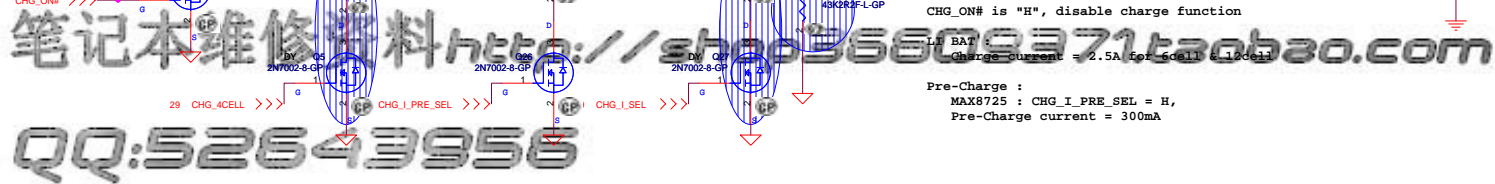
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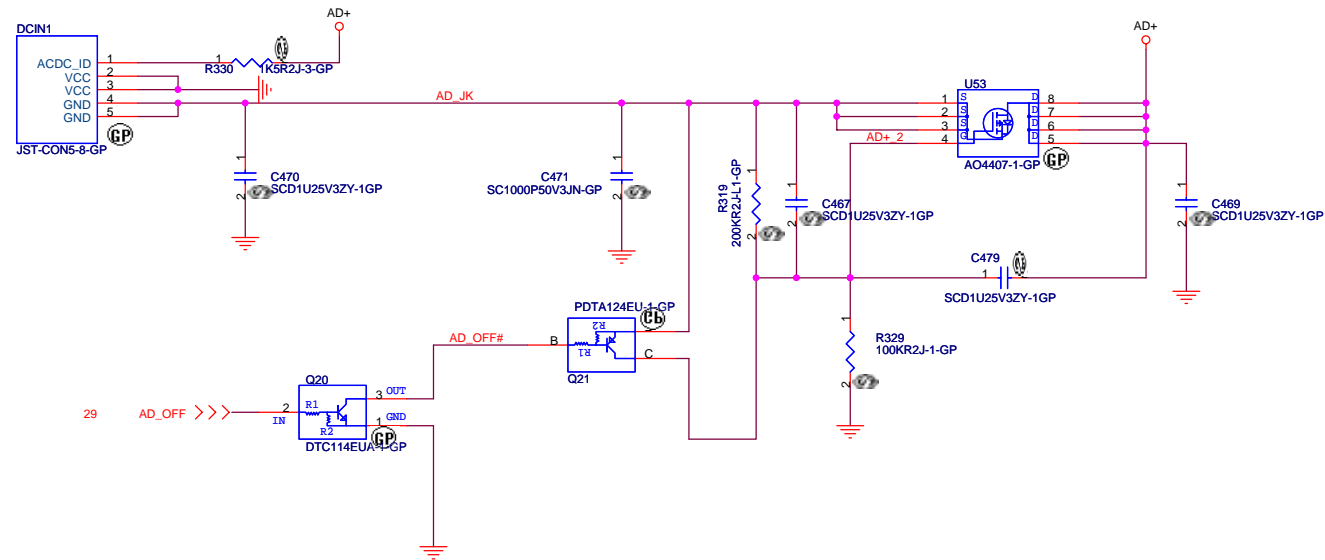
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GND	P2
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GND	B5
GND	E5
GND	I5
GND	P5
GND	U5
GND	Y5
GND	AC5
GND	H6
GND	AF6
GND	
GND	B8
GND	E8
GND	AD8
GND	K9
GND	P9
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GND	AD9
GND	AF9
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GND	E11
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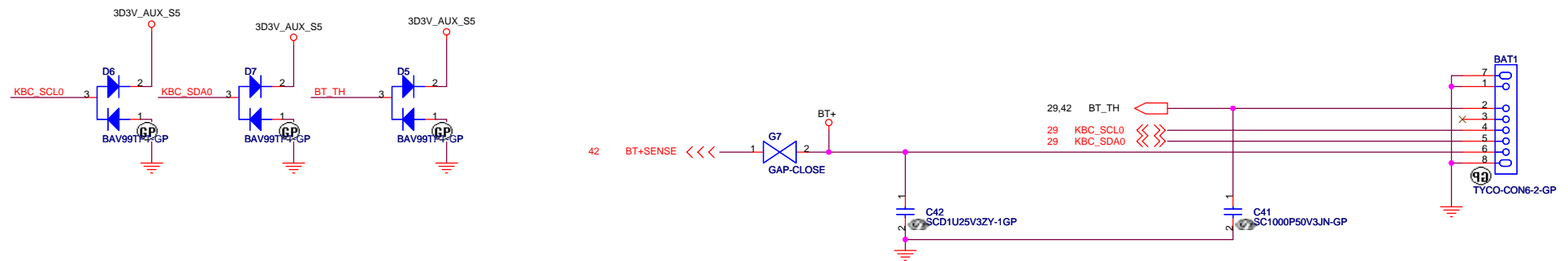




Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Title

AD/BATT CONN

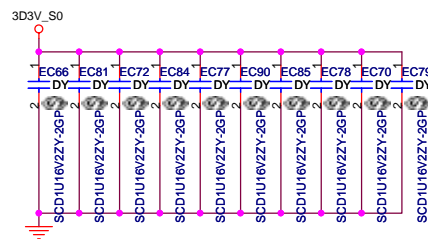
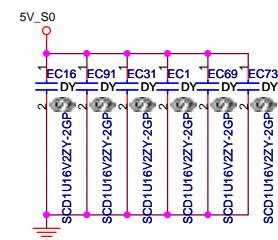
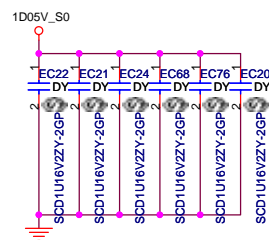
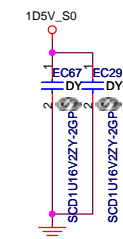
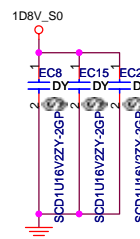
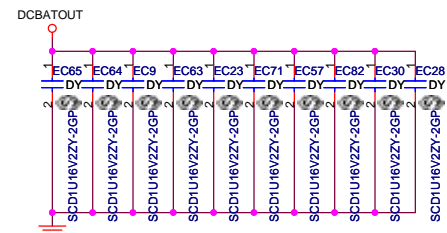
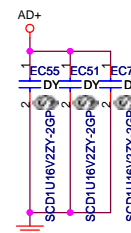
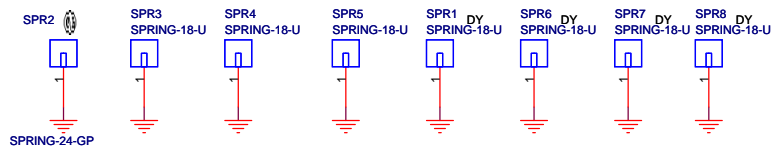
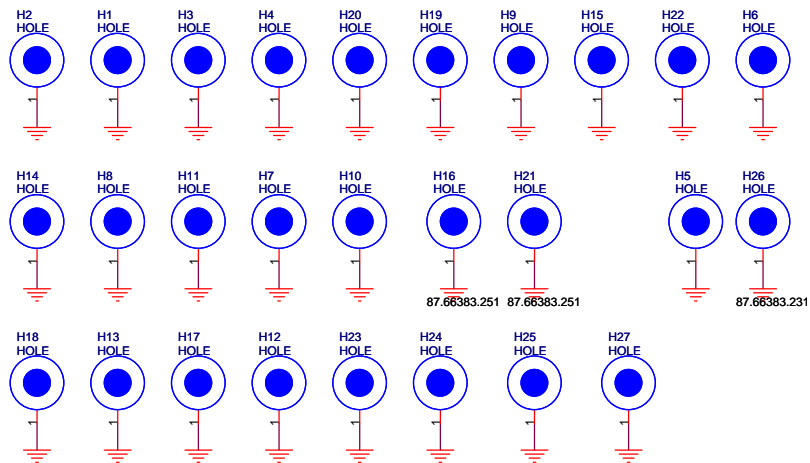
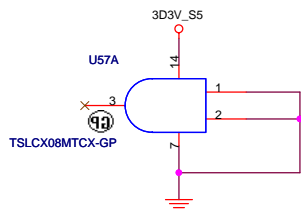
Size
A3

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Rev
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