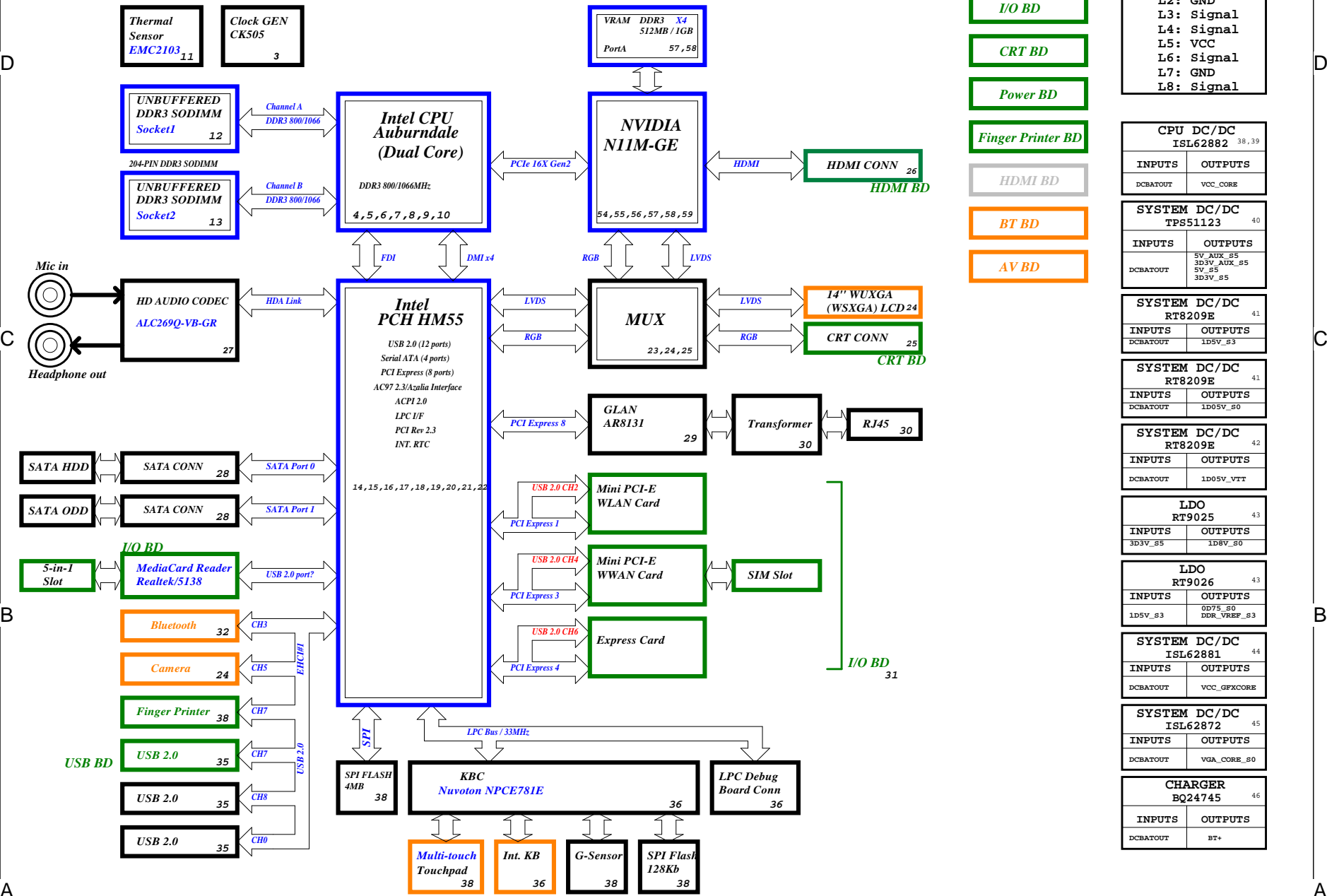


LA46 Switchable Graphics System Schematics

Project Code: 91.4GV01.001
PCB(Raw Card): 09911-1

www.bufanxiu.com



- USB BD
- I/O BD
- CRT BD
- Power BD
- Finger Printer BD
- HDMI BD
- BT BD
- AV BD

PCB LAYER	
L1:	Top
L2:	GND
L3:	Signal
L4:	Signal
L5:	VCC
L6:	Signal
L7:	GND
L8:	Signal

CPU DC/DC ISL62882	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51123	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

LDO RT9025	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

LDO RT9026	
INPUTS	OUTPUTS
1D5V_S3	0D75_S0 DDR_VREF_S3

SYSTEM DC/DC ISL62881	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

SYSTEM DC/DC ISL62872	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0

CHARGER BQ24745	
INPUTS	OUTPUTS
DCBATOUT	BT+

Name	Schematics Notes
SPKR	Reboot option at power-up. Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1): Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

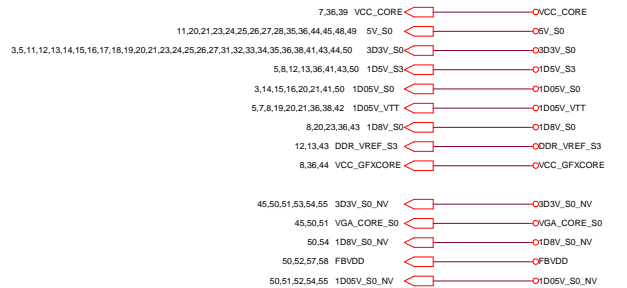
The diagram shows the timing relationship between VDD33, PEX_VDD, and various internal signals. VDD33 is a constant high signal. PEX_VDD is shown ramping up at any time, with a note indicating "PEX_VDD can ramp up any time". The internal signals INV-VDD, INV-IFPAB_IOVDD, and INV-FBVDDQ are shown as pulses that occur after PEX_VDD has started to ramp up. FBVDDQ is shown as a pulse that occurs after INV-FBVDDQ.

Timing diagram showing the power-up sequence for the system. The signals are:

- AD+
- 3D3V_AUX_S5
- 5V_AUX_S5
- SS_ENABLE (KBC)
- 5V_S5
- 3D3V_S5
- RSMRST# (KBC)
- LAN_PWR_ON
- 3D3V_LAN_S5
- KBC_PWRBTN#
- PM_PWRBTN#
- PM_SLP_S4#
- 1D5V_S3
- DDR3_VREF_S3
- PM_SLP_S3#
- 5V_S0
- 3D3V_S0
- 1D5V_S0
- 1D05V_S0
- 0D75V_S0
- ALL_PWRGD
- 1D05V_VTT
- VTT_PWRGD (H_VTT_PWRGD -> CPU, KBC)
- GFX_VR_EN
- VCC_GFXCORE

Key timing annotations:

- A delay of $>10\text{ms}$ is indicated between the RSMRST# (KBC) signal and the LAN_PWR_ON signal.
- The LAN_PWR_ON signal is labeled "can power after power switch press".



D

D

C

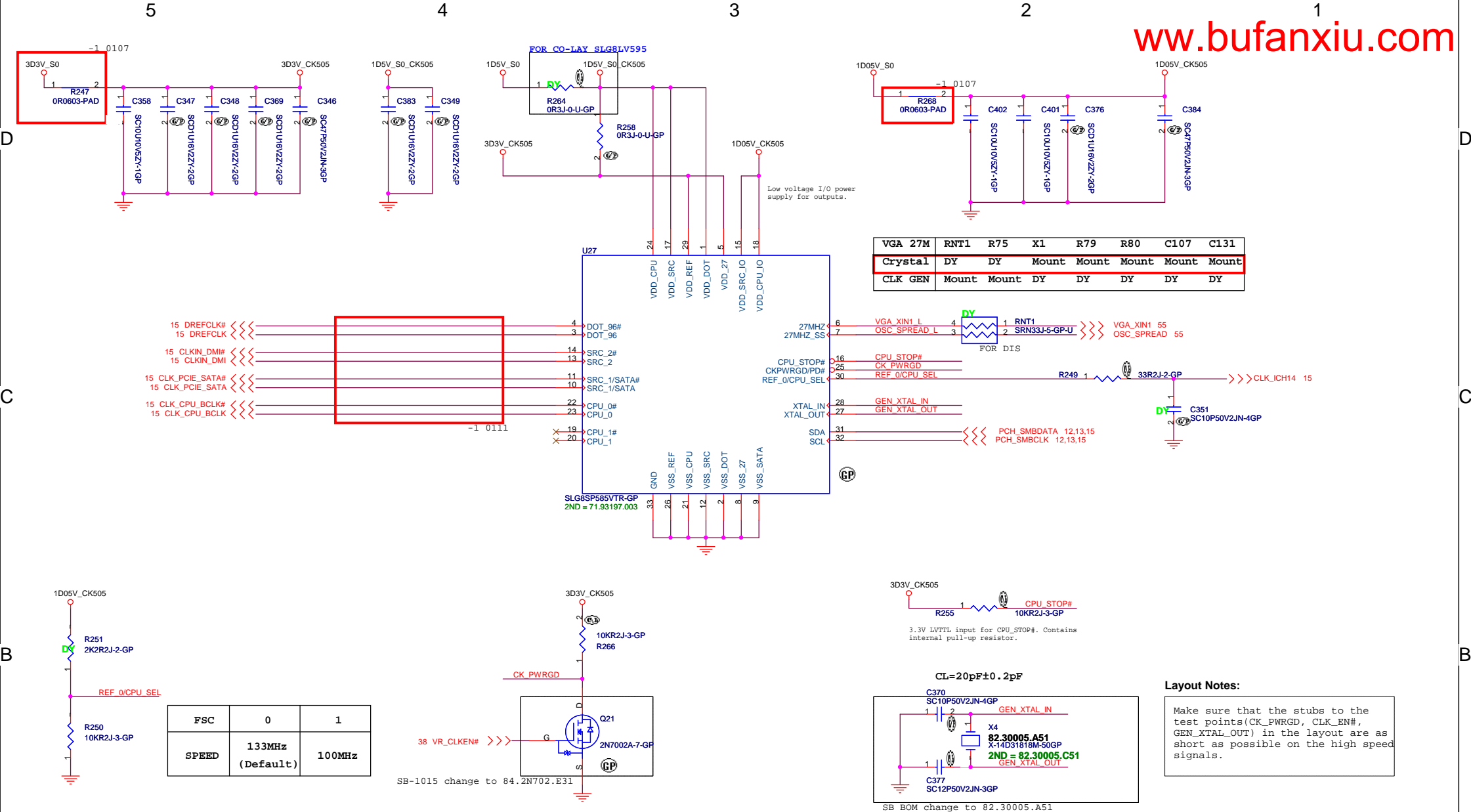
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B

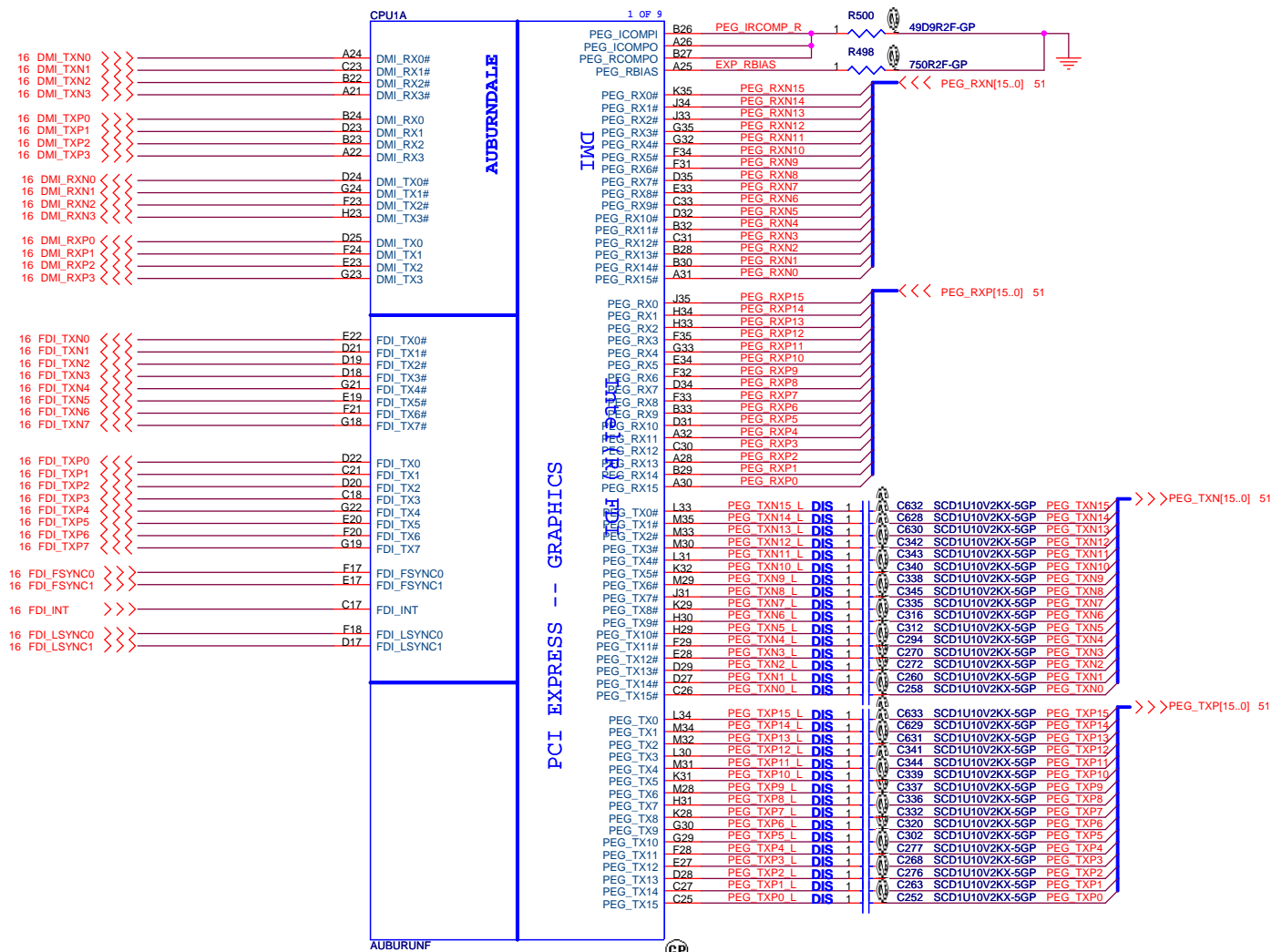
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A

A

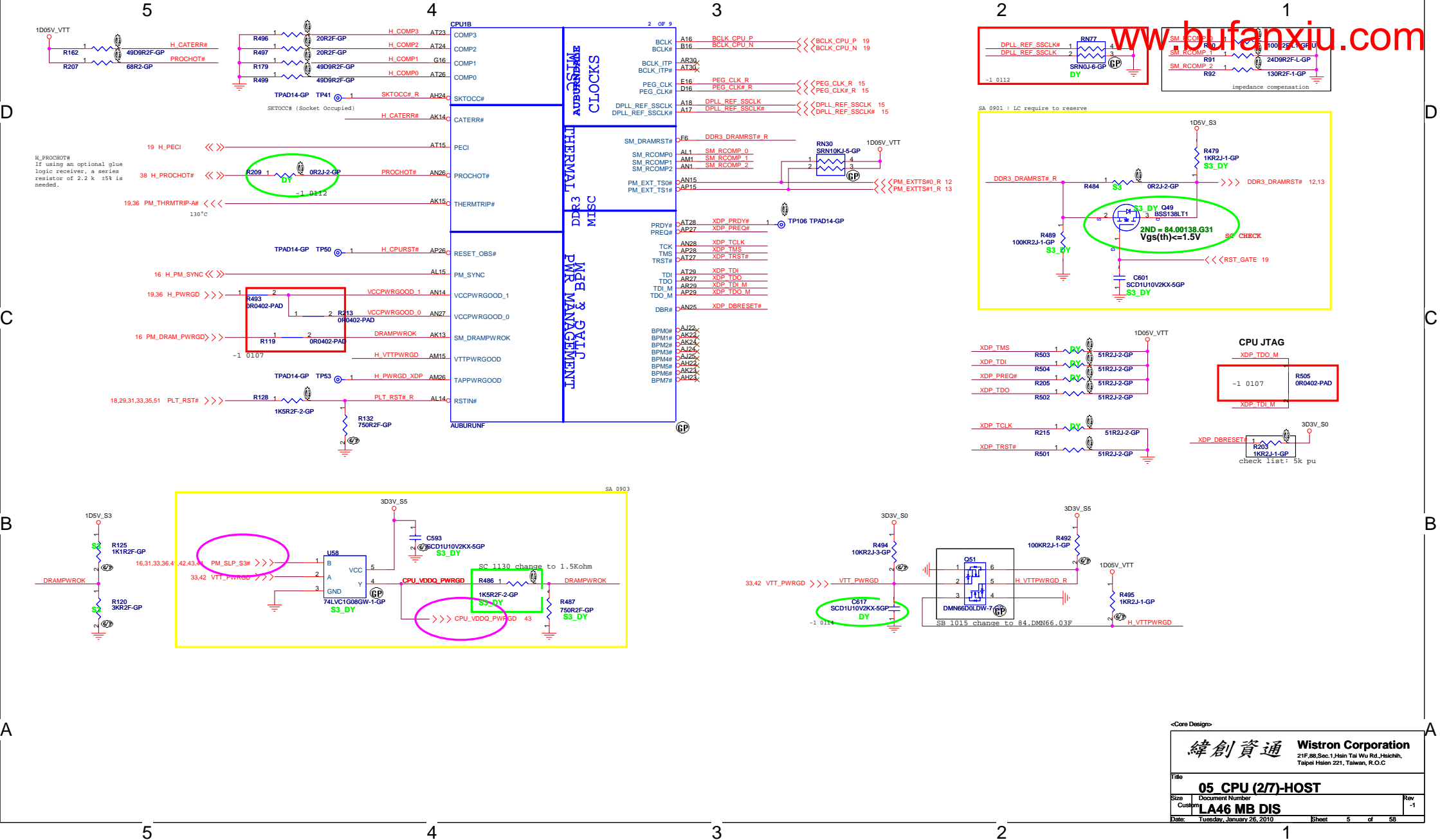


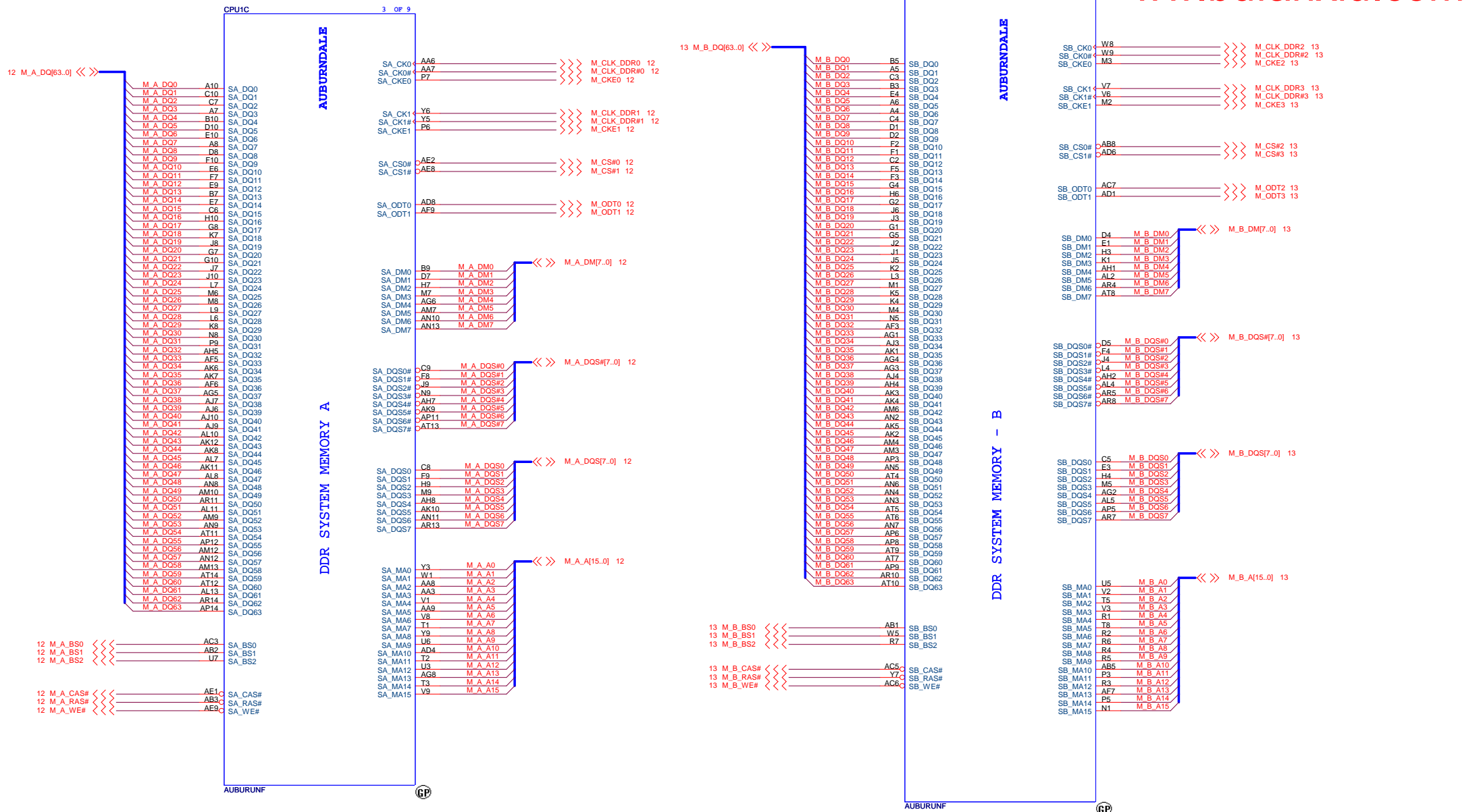
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緯創資通		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
04 CPU (17)-PEG / DMI / FDI			
Size			
A3			
Document Number			
LA46 MB DIS			
Date			
Tuesday, January 26, 2010			
Sheet			
4 of 58			
Rev			
-1			





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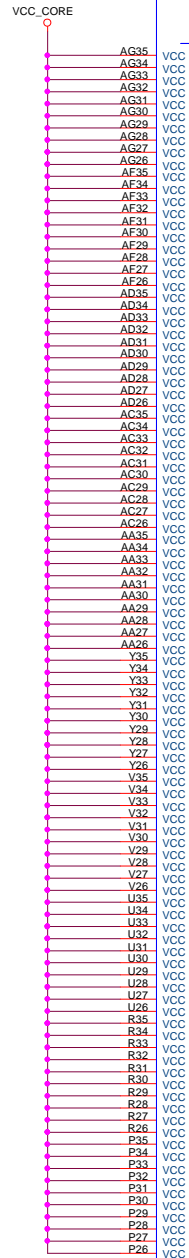
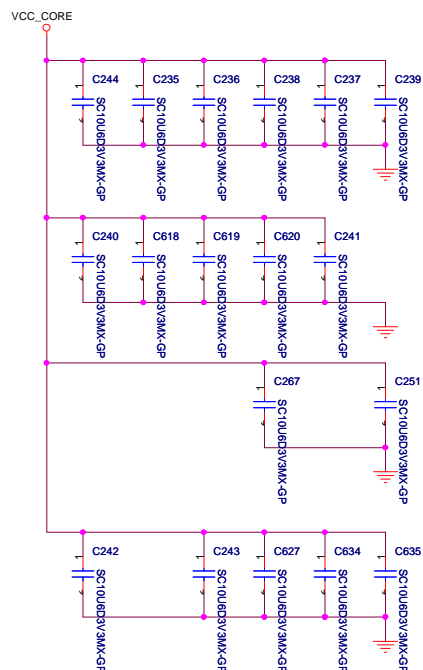
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Wistron Corporation

21F, 88, Sec. 1, Hsin Tai Wu Rd., Heichih,
Taippei Hsien 221, Taiwan, R.O.C

Title		06 CPU (3/7)-MEM INTERFACE	
Size	Document Number	LA46 MB DIS	Rev -1
Date:	Tuesday, January 26, 2010	Sheet 6 of 58	

PROCESSOR CORE POWER
48A -->Arrandale



AUBURNDALE

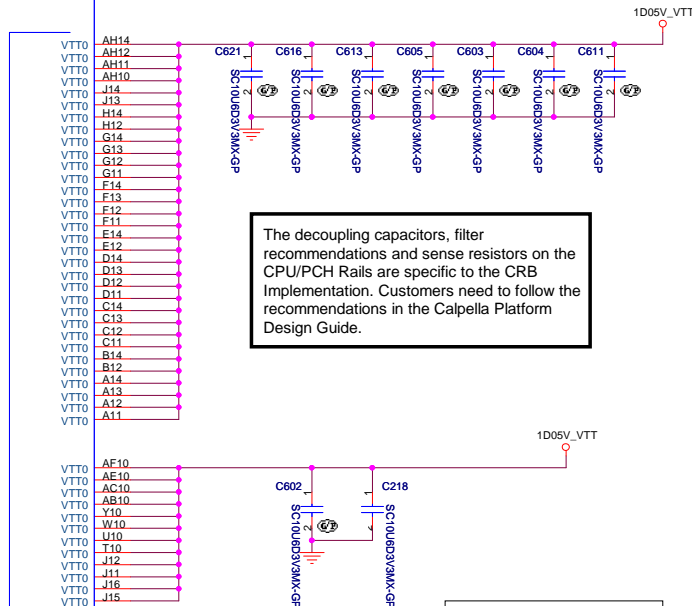
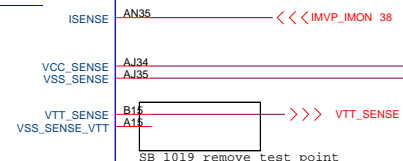
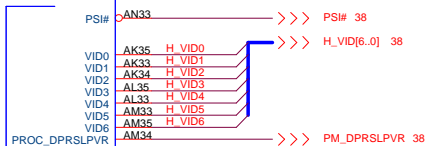
1.1V RAIL POWER

CPU CORE SUPPLY

POWER

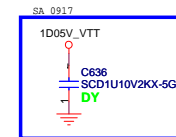
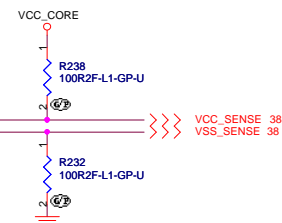
CPU VIDS

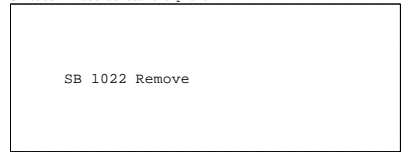
SENSE LINES



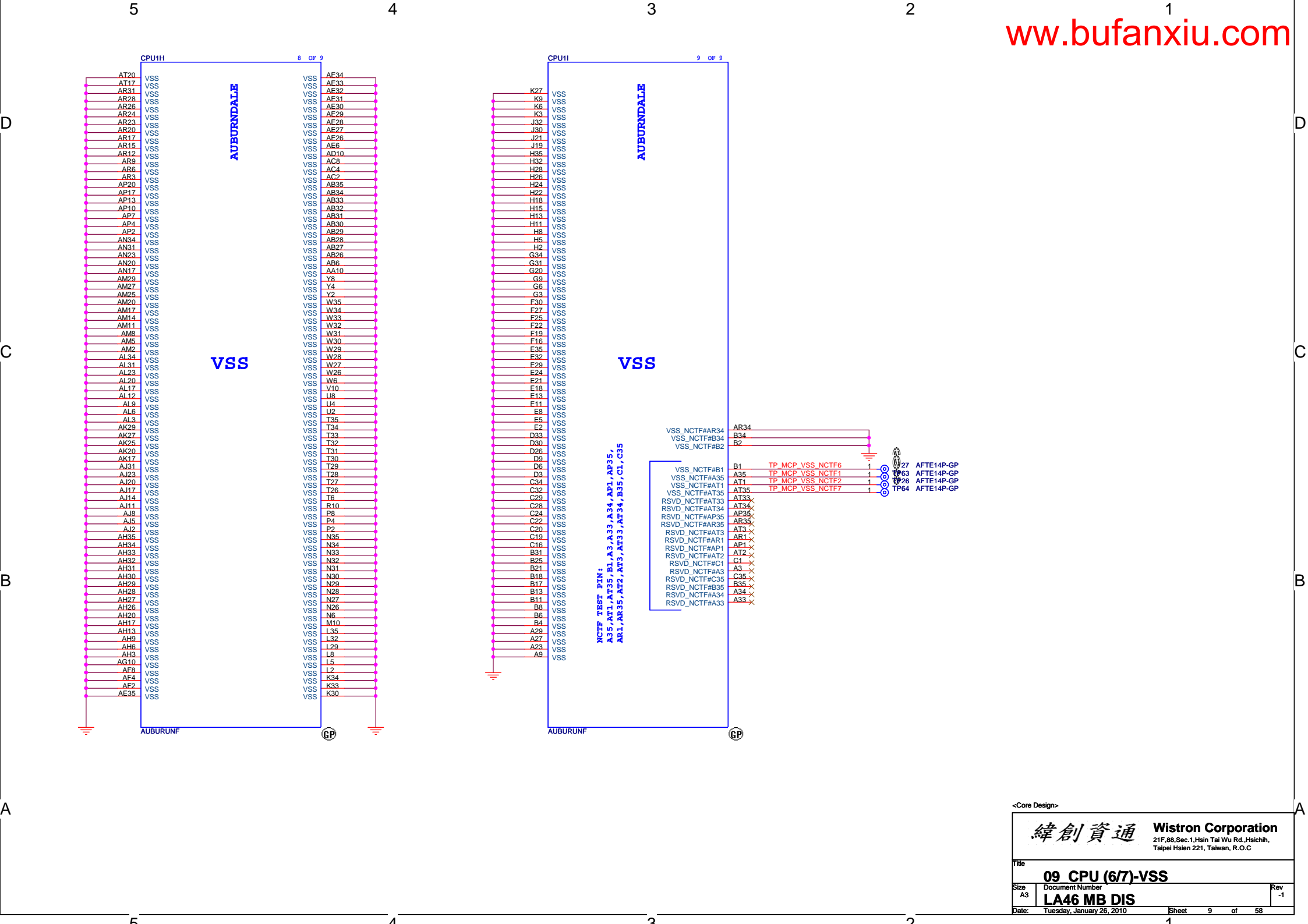
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V





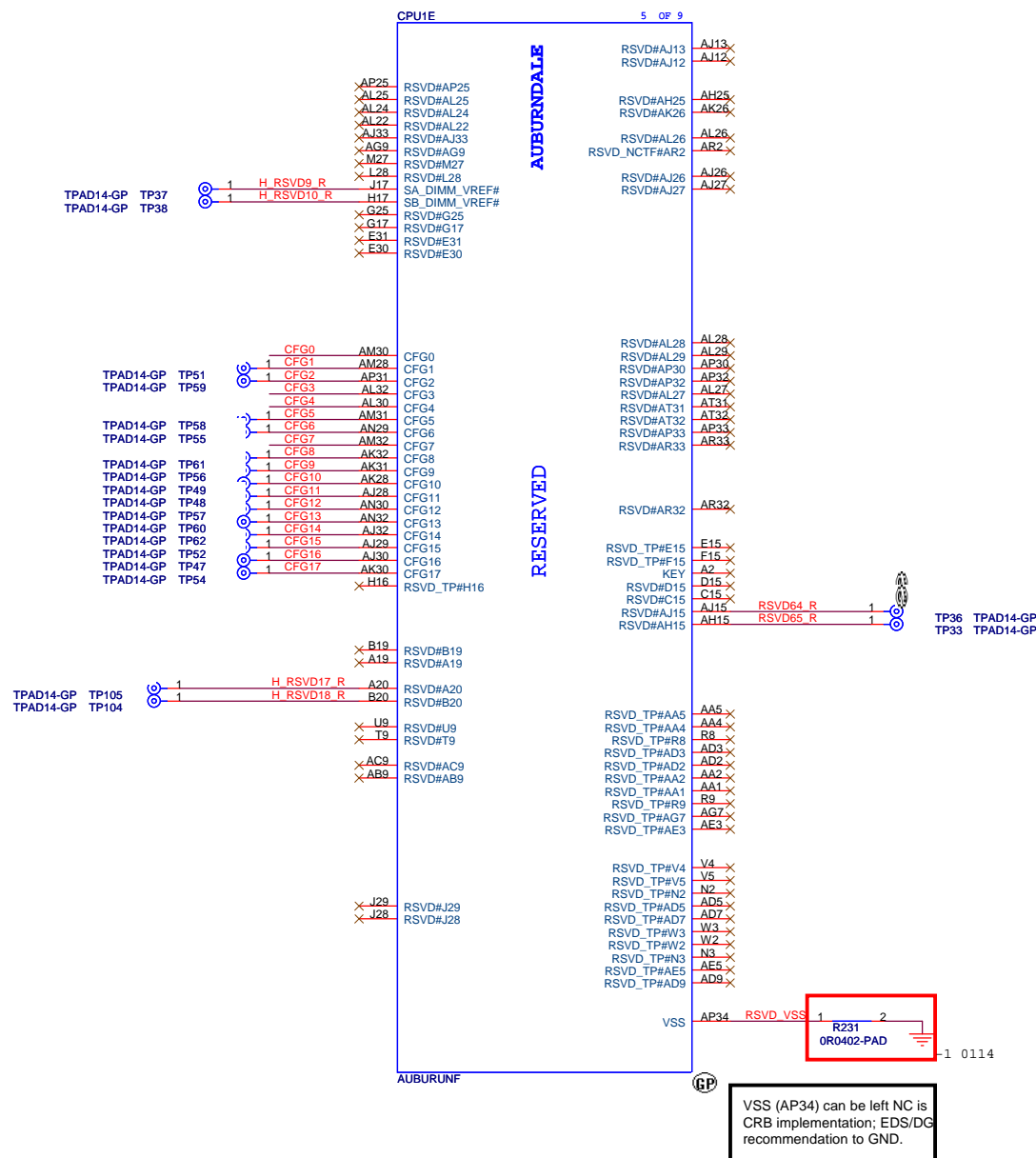
Please note that the VTT Rail Values are Auburndale
VTT=1.05V; Clarksfield
VTT=1.1V



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C

Title		09 CPU (6/7)-VSS	
Size	A3	Document Number	Rev .1
Date: Tuesday, January 26, 2010		Sheet 9	of 58

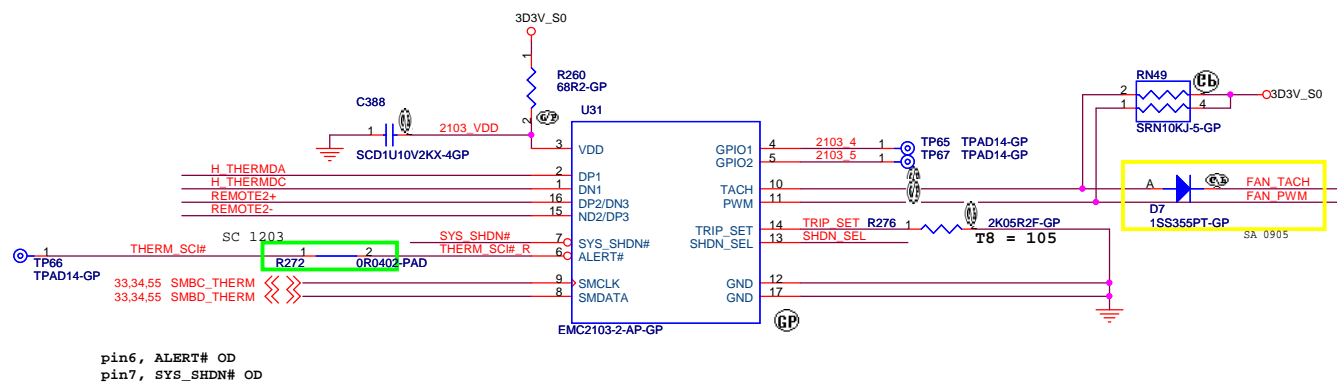
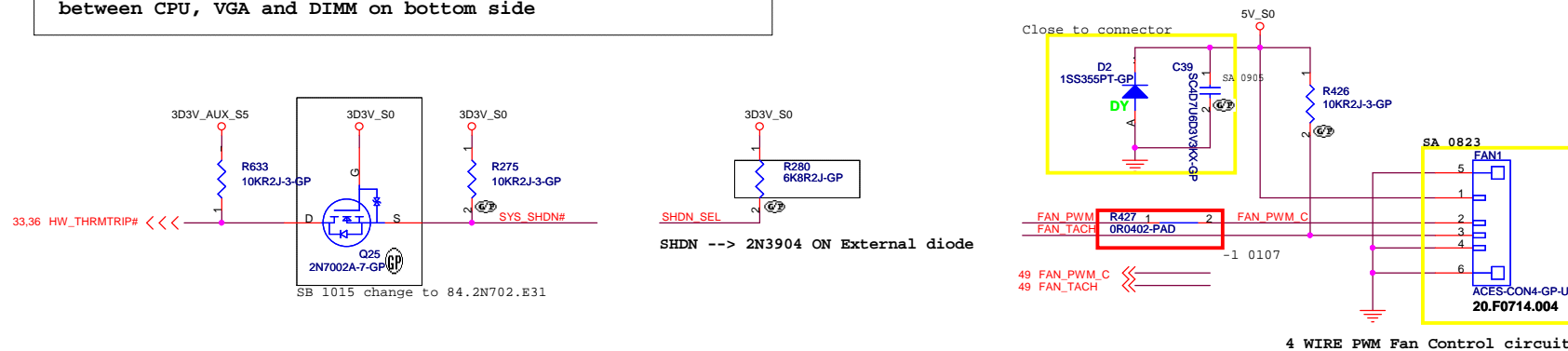
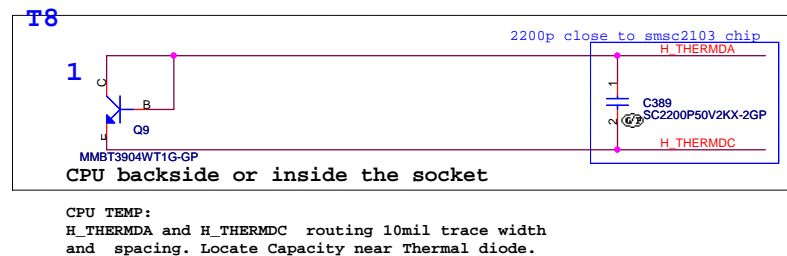


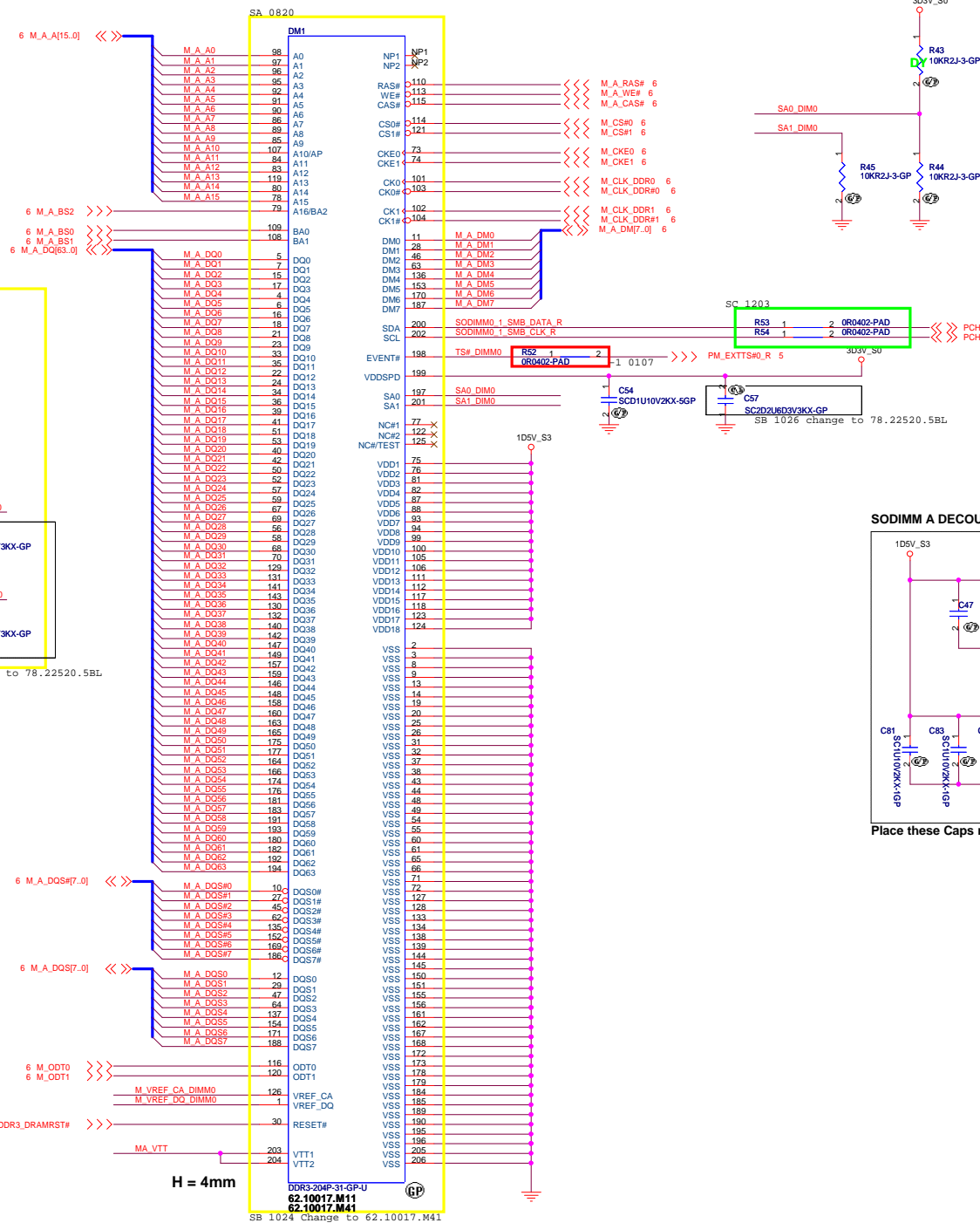
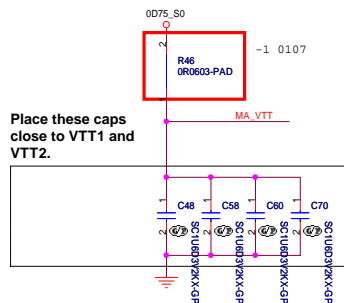
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

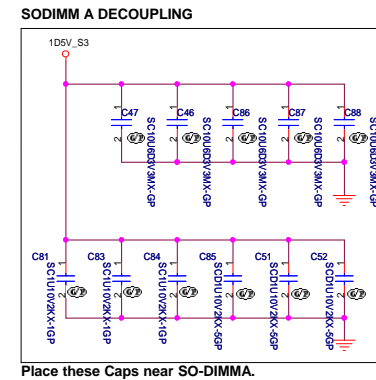
CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	<p>Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.</p> <p>Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report].</p> <p>For a common M/B design (for AUB and CFD) the pull-down resistor should be used. Does not impact AUB functionality.</p>



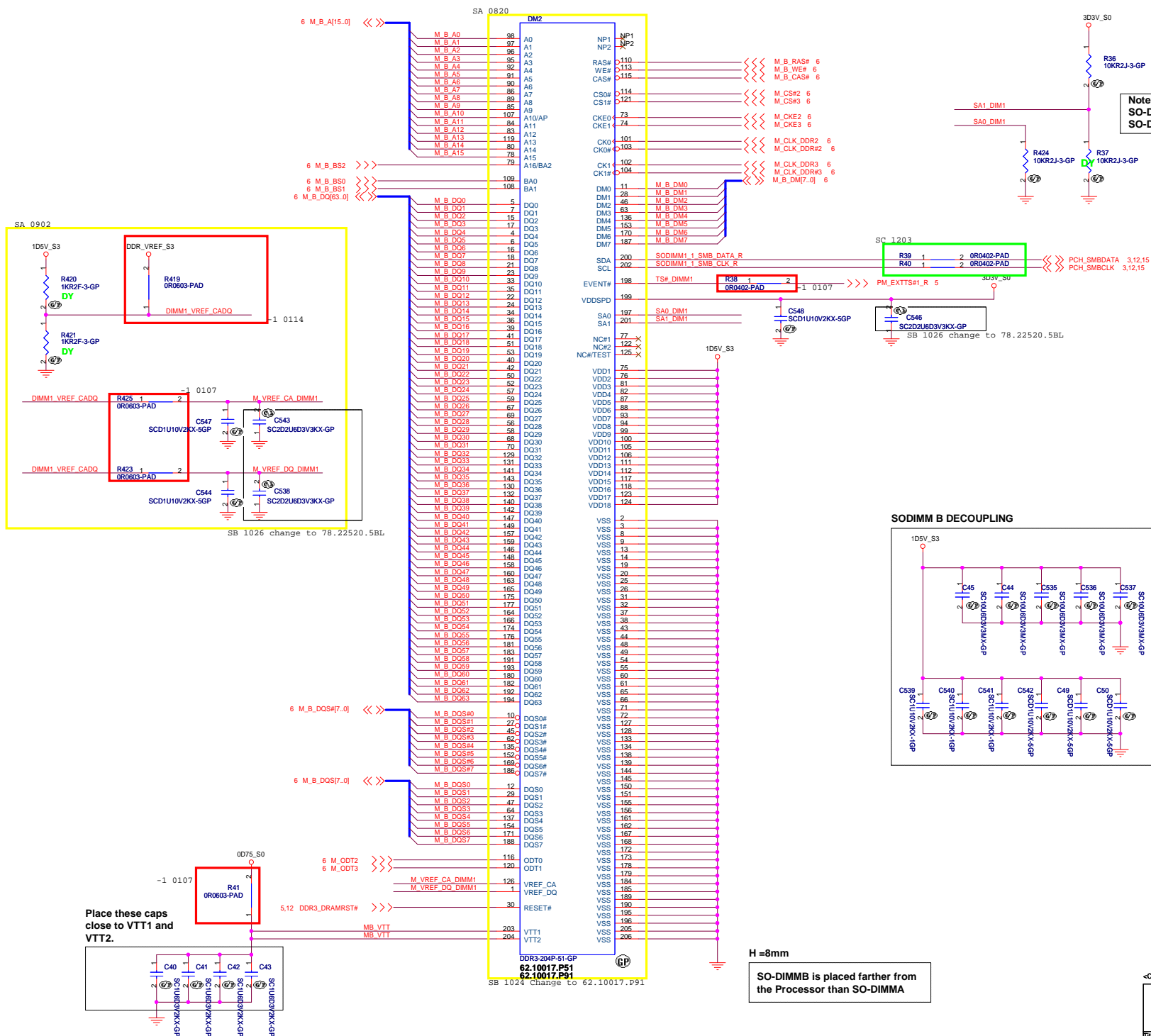


Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



Place these Caps near SO-DIMMA.



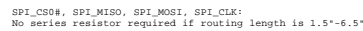
H = 8mm

SO-DIMMB is placed farther from the Processor than SO-DIMMA

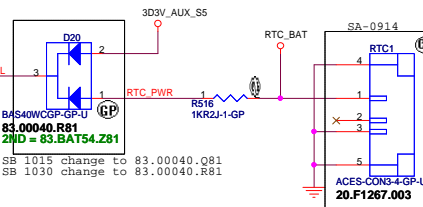
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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipai Hsien 221, Taiwan, R.O.C

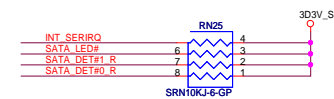
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13 DDR3-SODIMM2			
Size	Document Number	Rev	
Custom	LA46 MB DIS	-1	
Date:	Wednesday, January 27, 2010	Sheet	13 of 58

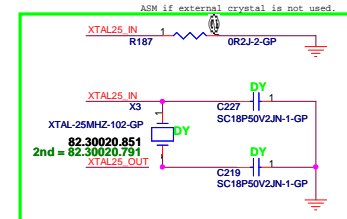
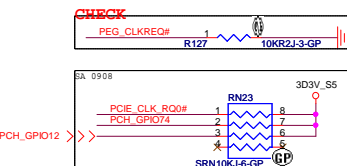


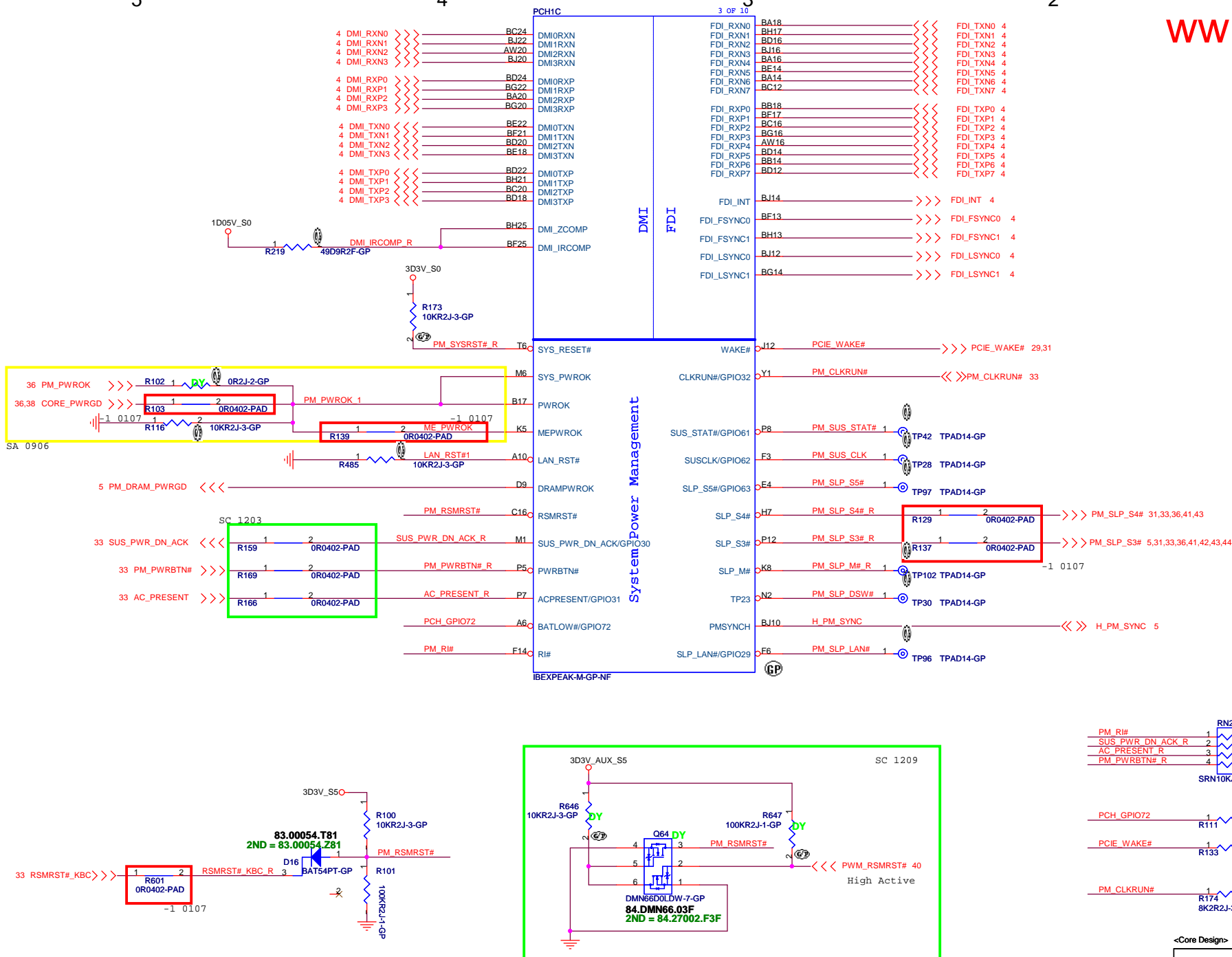
SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required

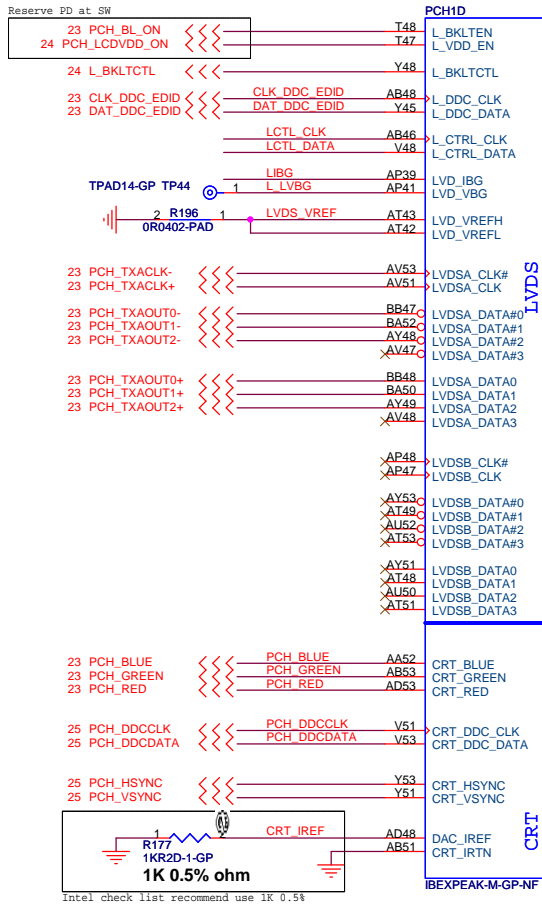
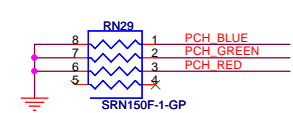
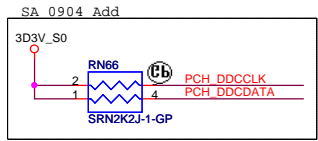
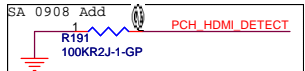
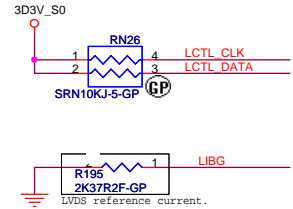
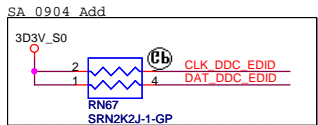
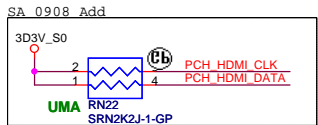


ODD





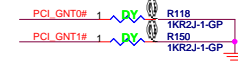
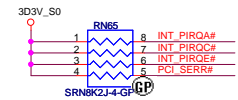
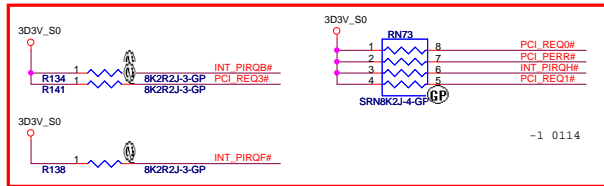




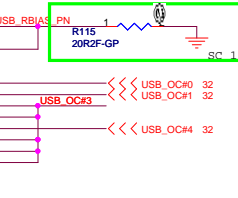
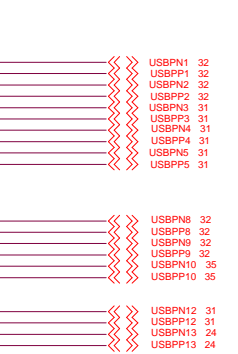
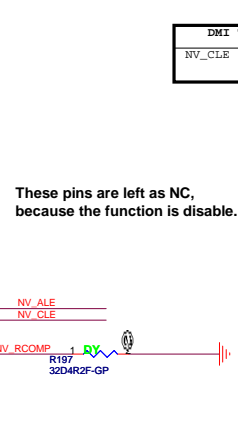
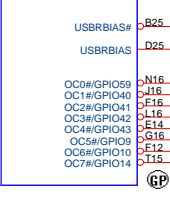
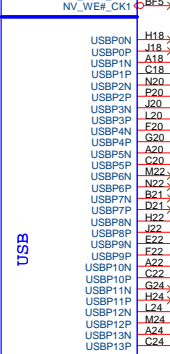
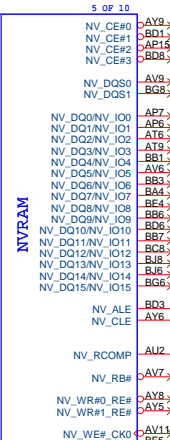
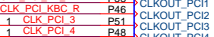
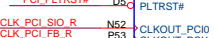
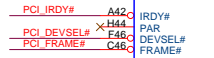
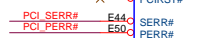
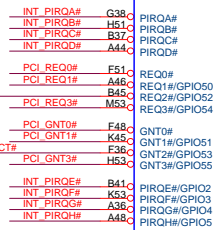
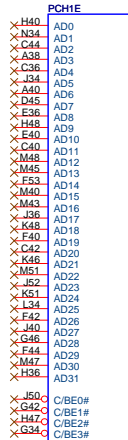
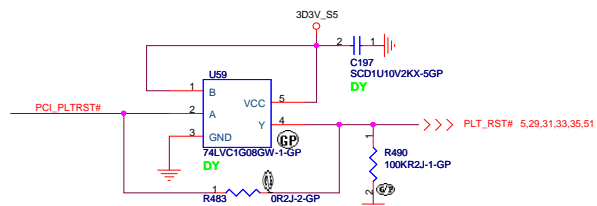
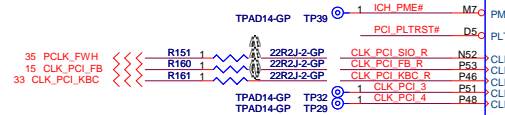
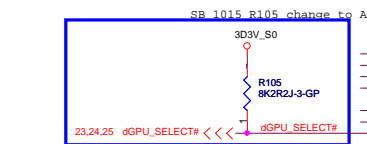
Digital Display Interface



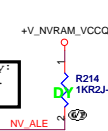
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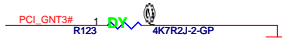
BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI



DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.



Pair	Device
0	NC
1	USB3
2	USB1
3	WLAN
4	Card Reader
5	WWAN
6	Disable (HM55)
7	Disable (HM55)
8	USB2
9	Blue Tooth
10	Finger Print
11	NC
12	Express Card
13	Camera



A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

OC#0	Port 0 & 1	EHCI
OC#1	Port 2 & 3	
OC#2	Port 4 & 5	
OC#3	Port 6 & 7	
OC#4	Port 8 & 9	EHCI
OC#5	Port 10 & 11	
OC#6	Port 12 & 13	
OC#7	Floater OC# (not used)	

<Core Design>

緯創資通

Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title		18 PCH (5/9)-PCI / USB	
Size	Document Number		Rev
Custom	LA46 MB DIS		-1
Date:	Tuesday, January 26, 2010	Sheet	18 of 58

D

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C

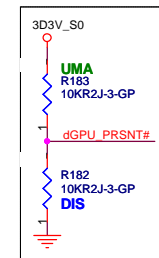
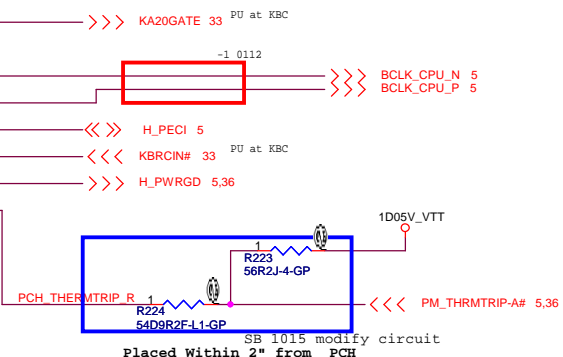
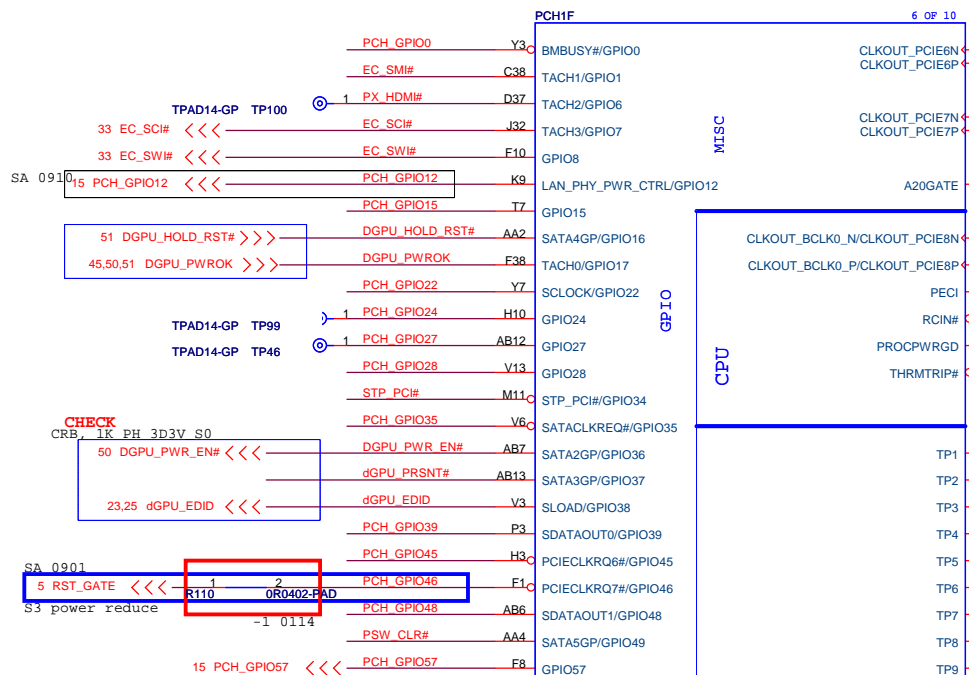
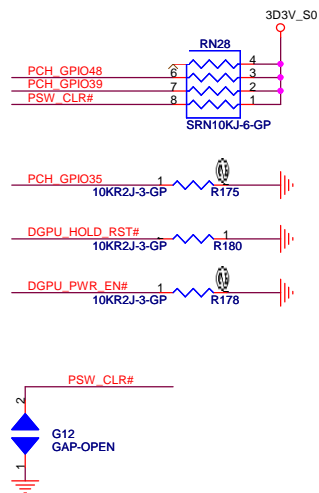
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B

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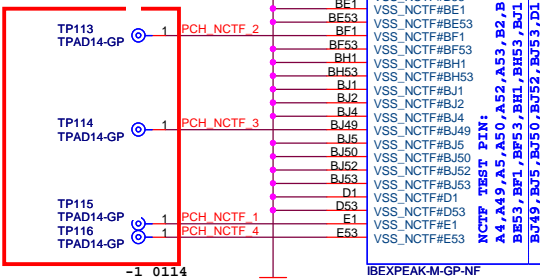
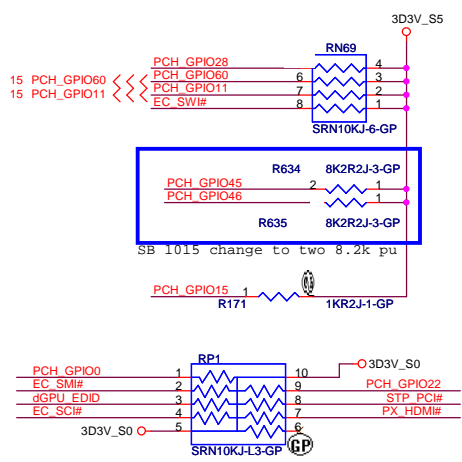


GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.

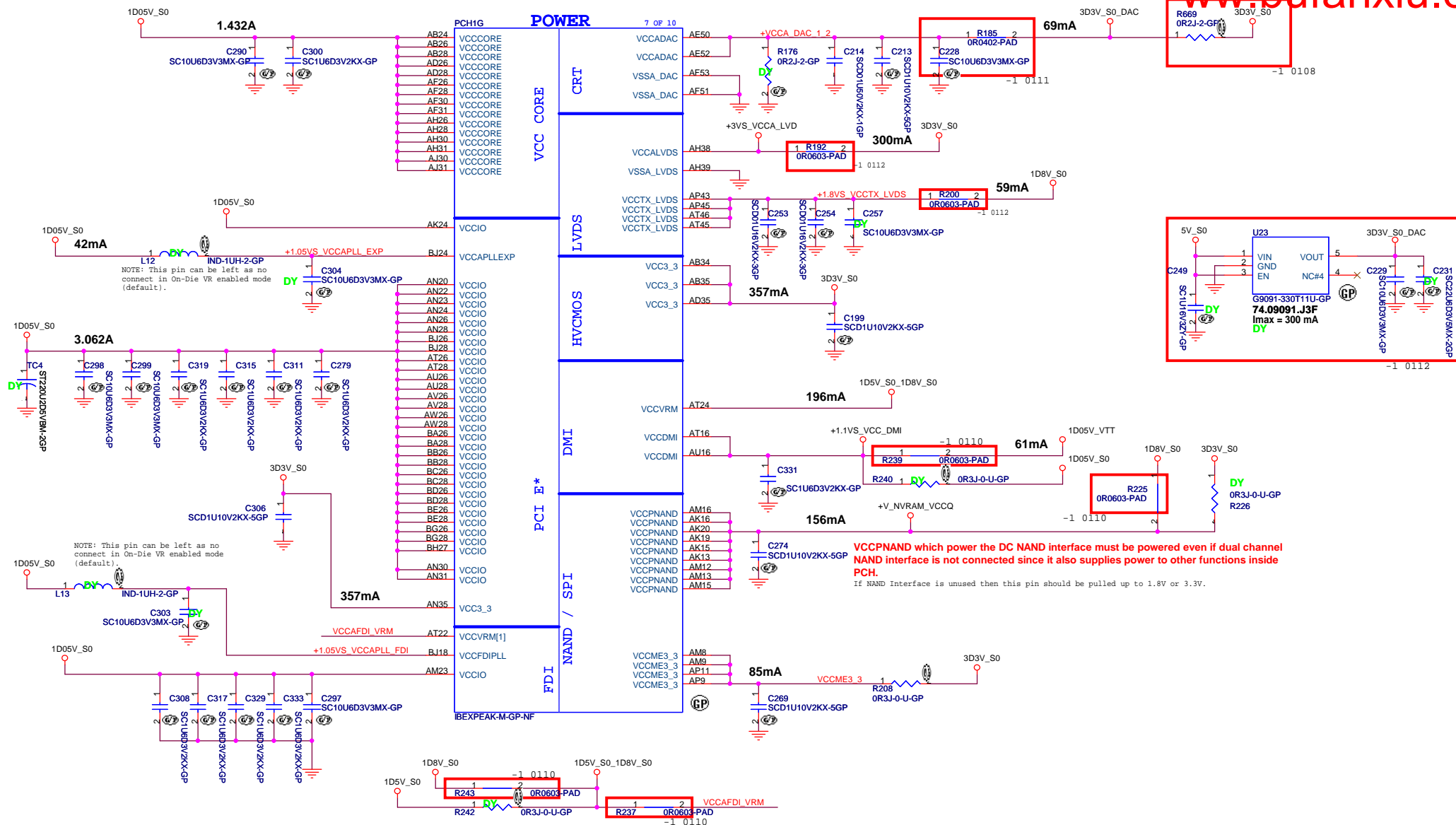
SATACLKREQ#:
When used as SATACLKREQ#,
this pin is open drain and should
use a pull-up resistor.

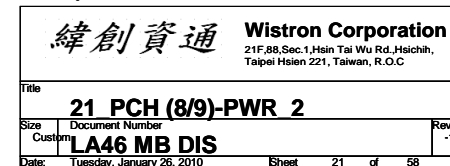


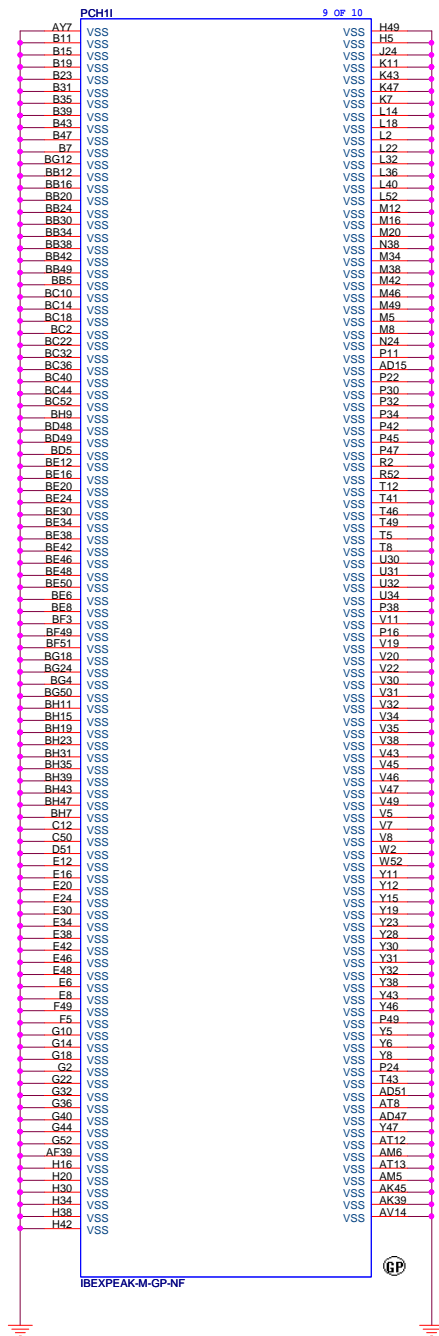
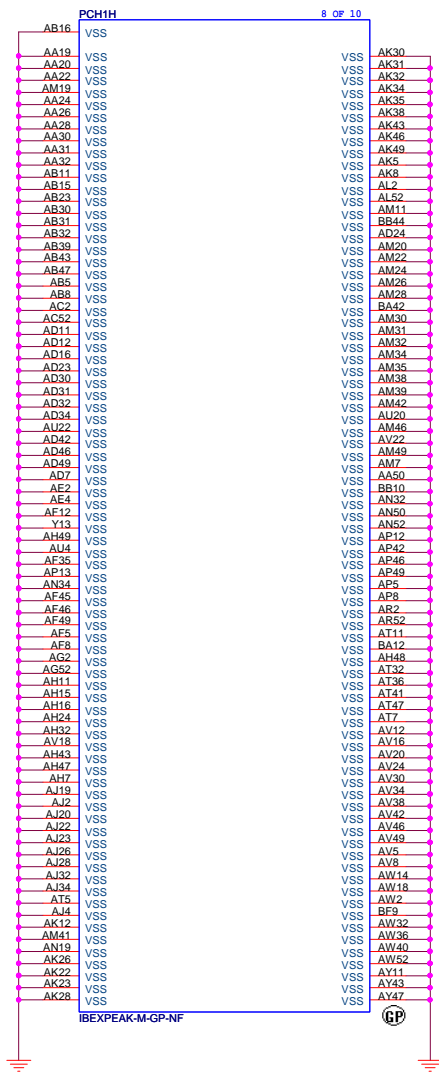
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緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title		19 PCH (6/9)-GPION/VSS NCTF/RSVD	
Size	A3	Document Number	LA46 MB DIS
Date	Tuesday, January 26, 2010	Sheet	19 of 58
Rev	-1		







<Core Design>

緯創資通

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Heichih,
Taipei Hsien 221, Taiwan, R.O.C

Title		22 PCH (9/9)-VSS
Size	Document Number	LA46 MB DIS
Custom		
Date:	Tuesday, January 26, 2010	Sheet 22 of 58

D

C

B

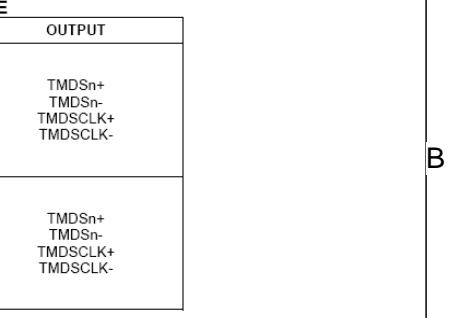
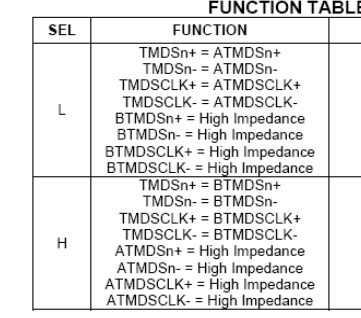
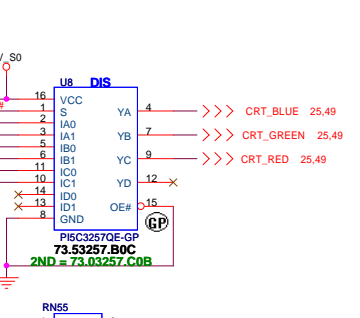
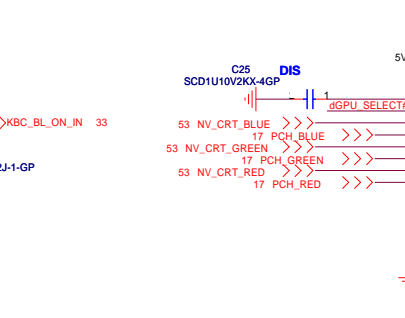
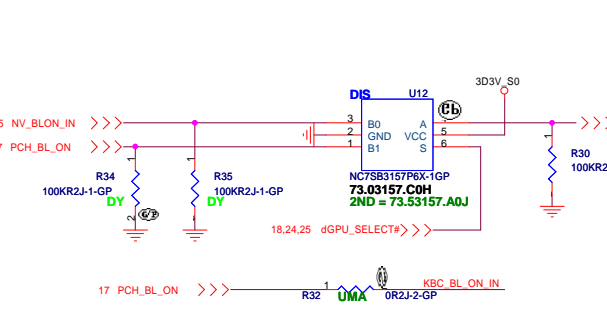
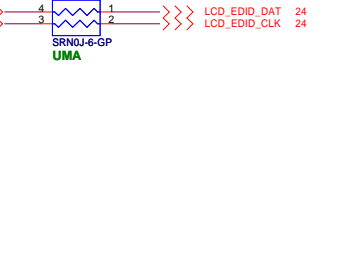
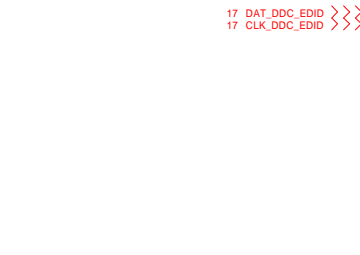
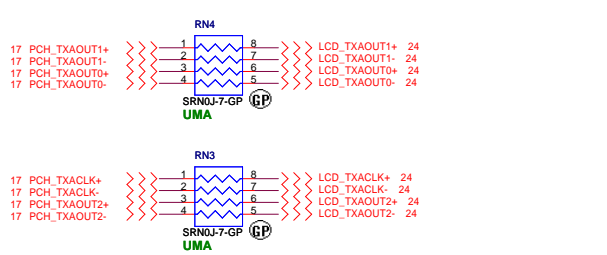
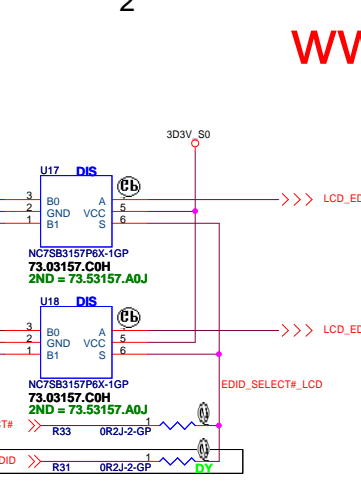
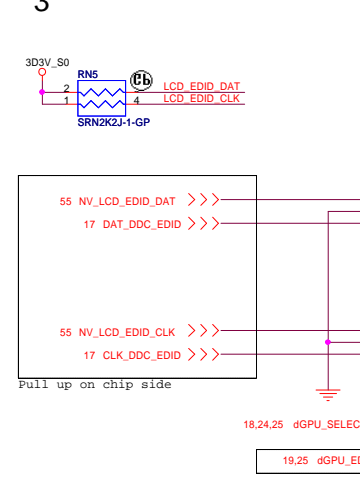
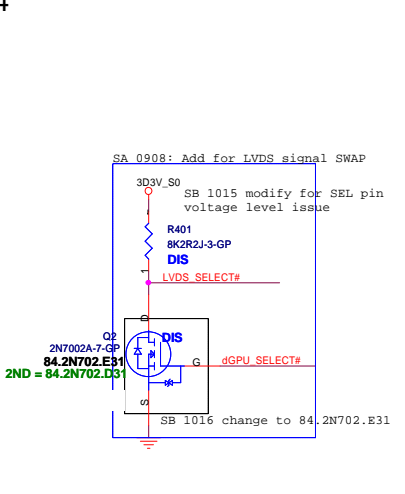
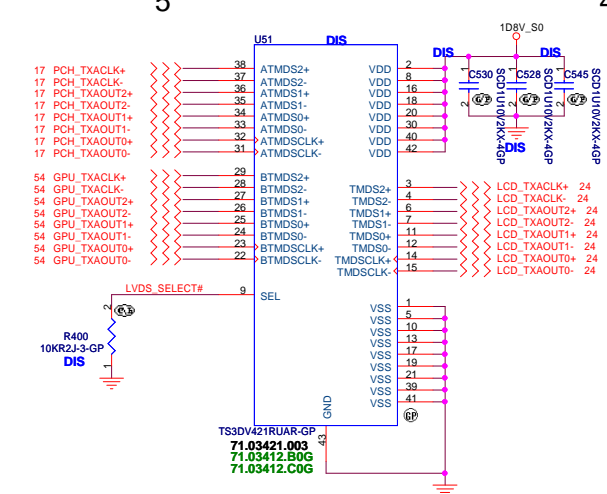
A

D

C

B

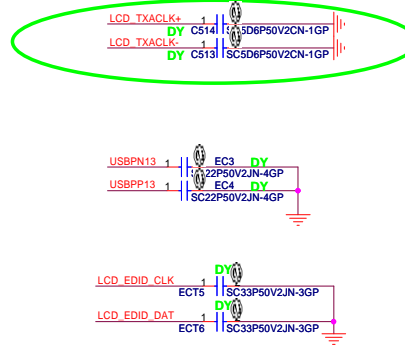
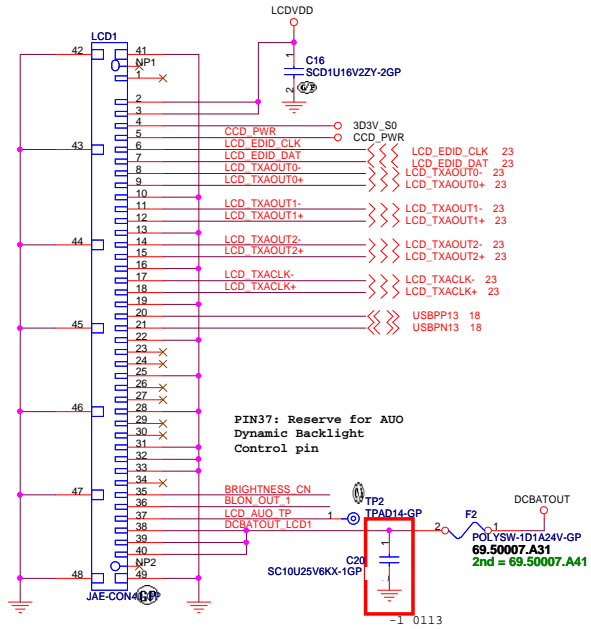
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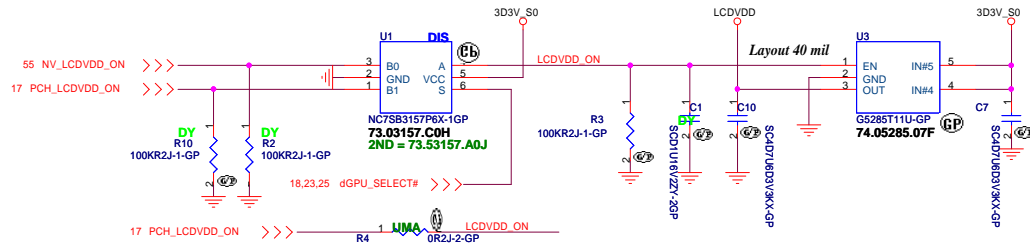
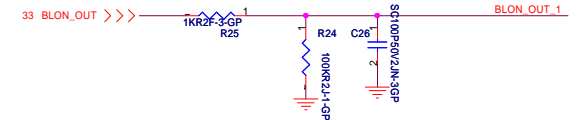
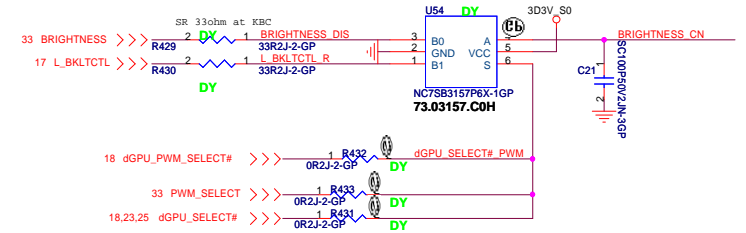
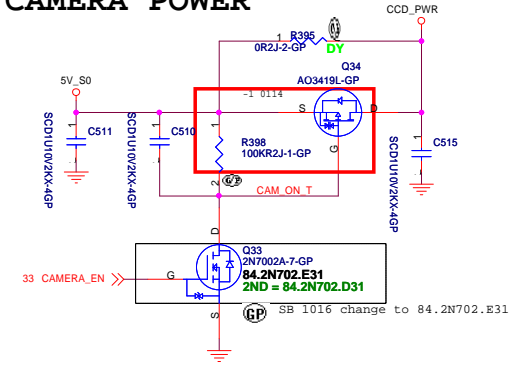
FUNCTION TABLE		
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

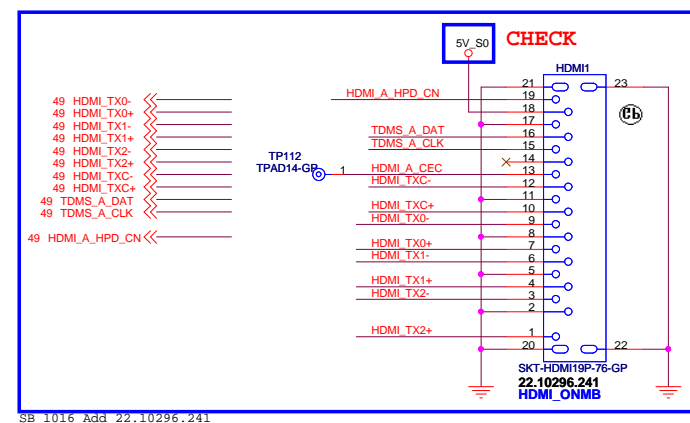
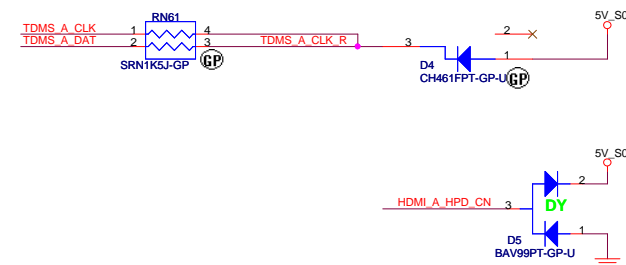
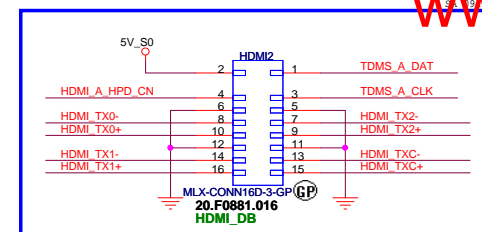
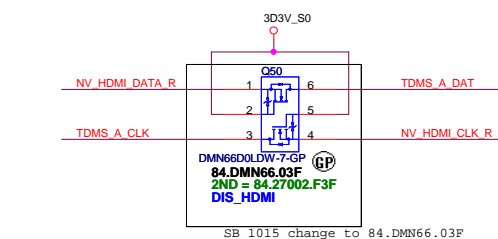
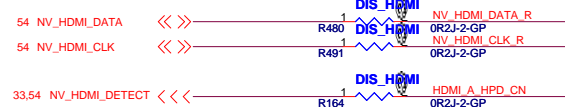
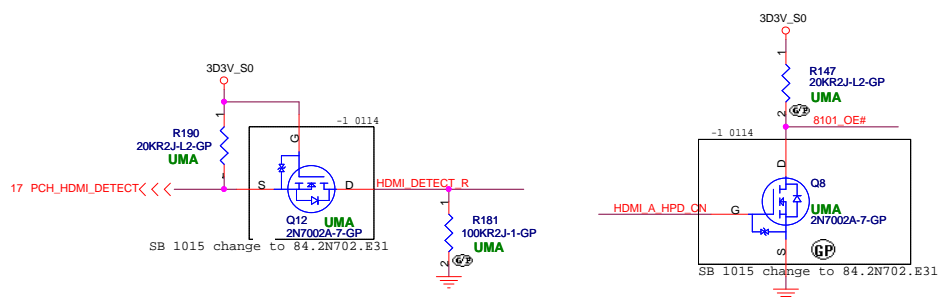
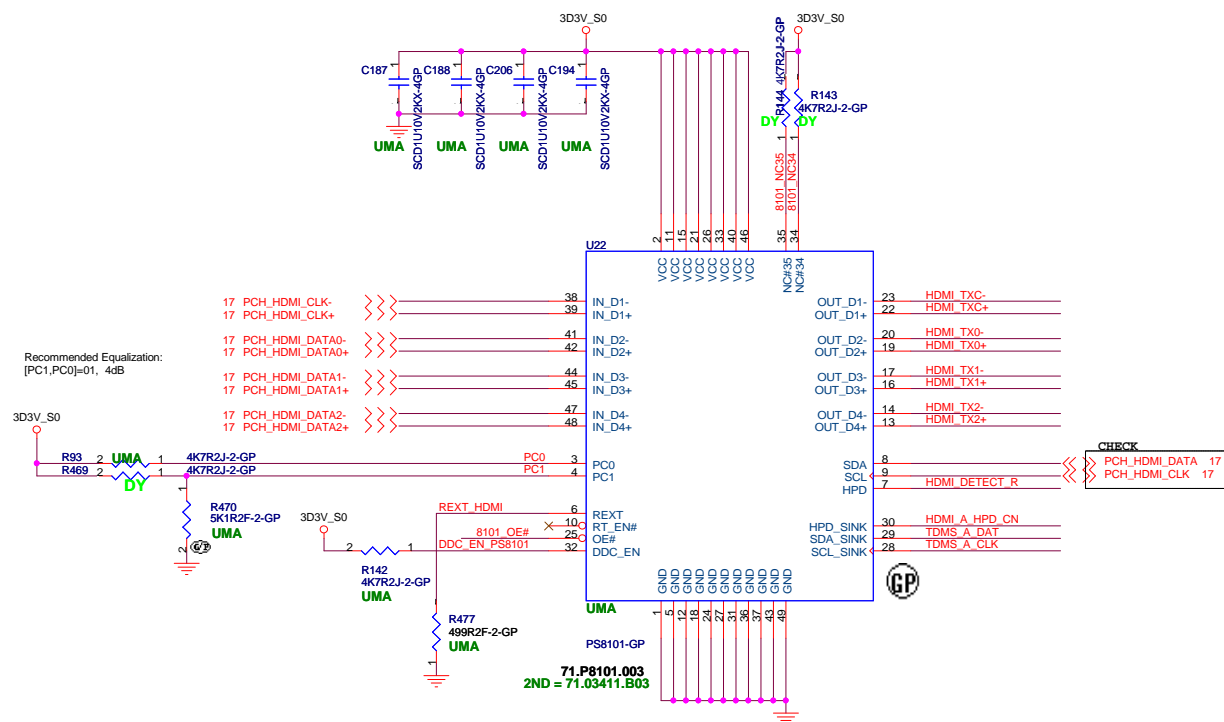
E	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

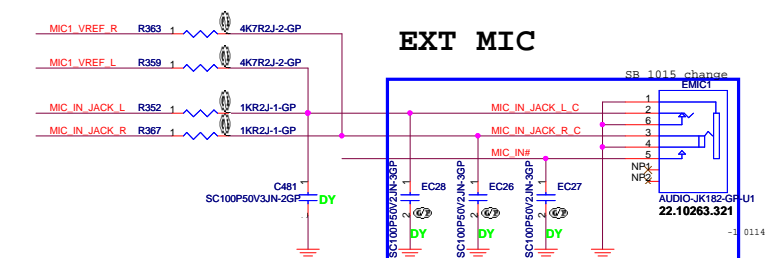
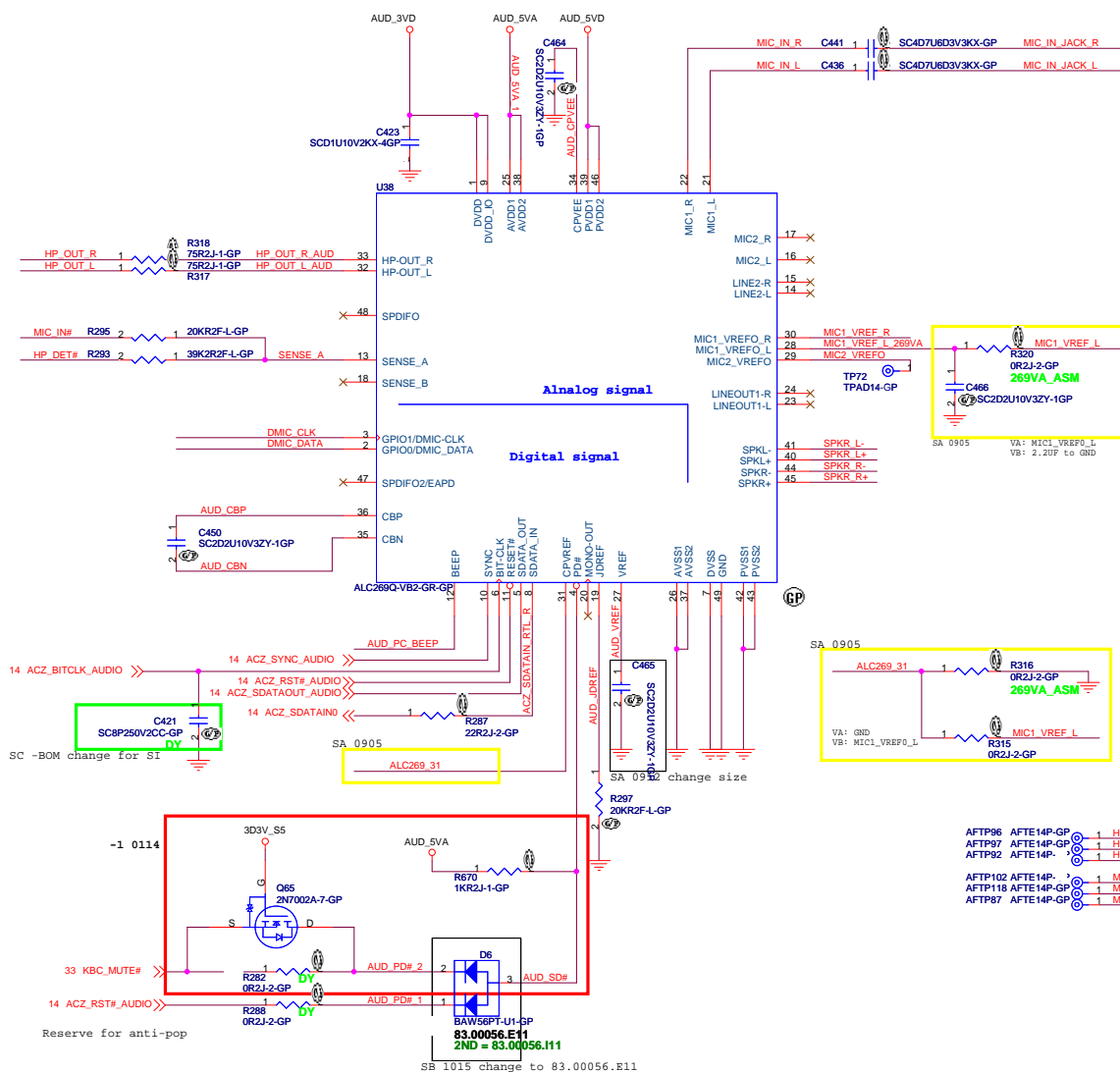
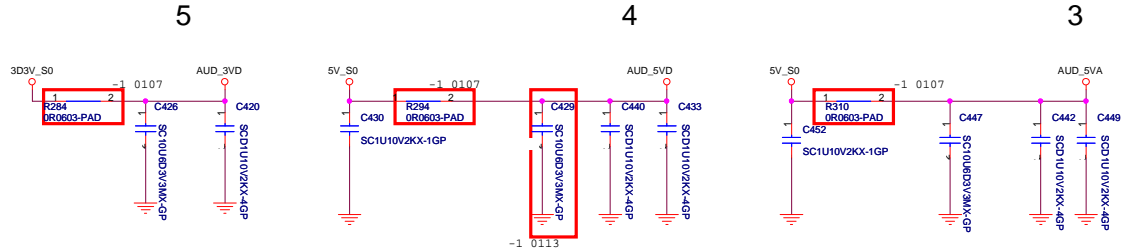
LCD/INVERTER/CCD CONN

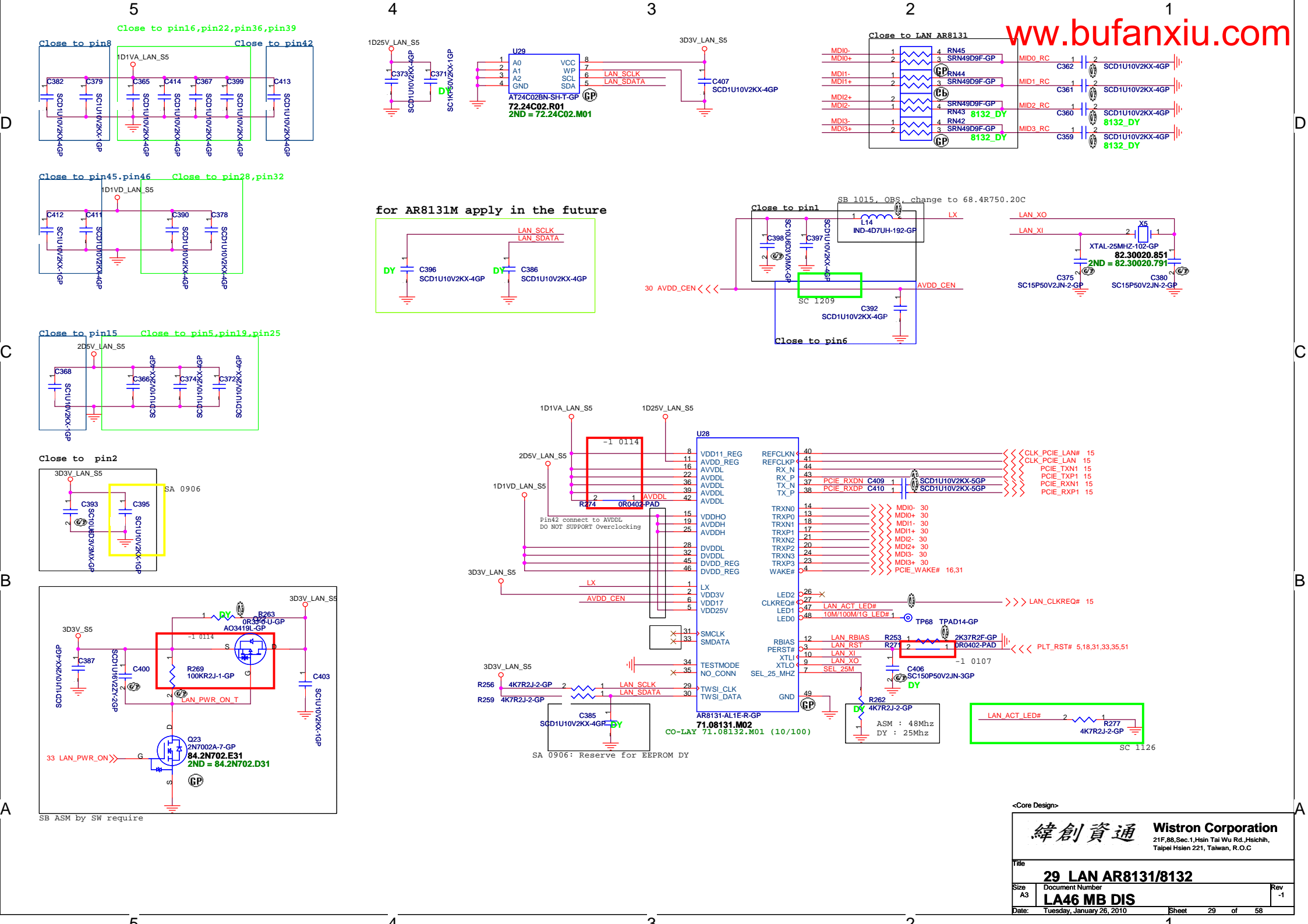


CAMERA POWER



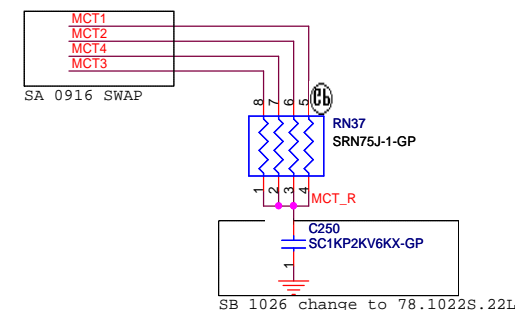




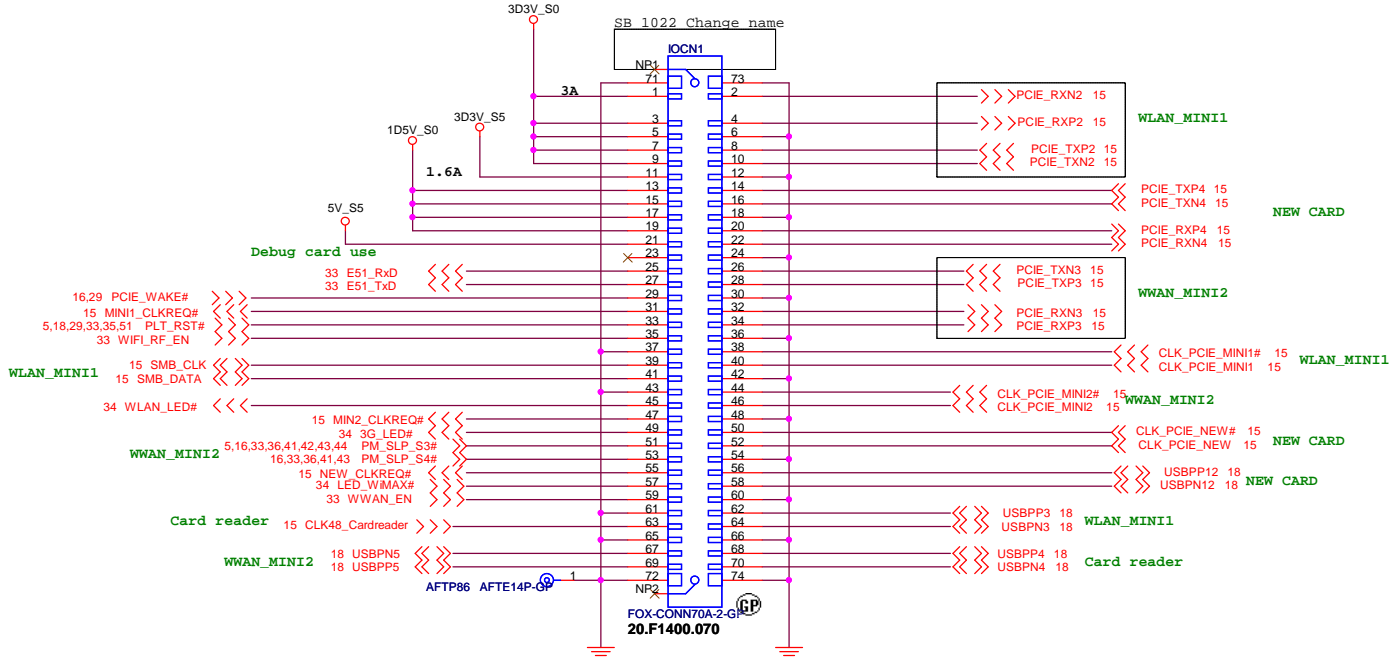


- A

LAN Connector



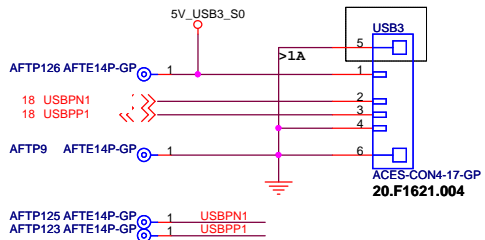
Size	Document Number	Rev
Custom	LA46 MB DIS	-1
Date:	Tuesday, January 26, 2010	Sheet 30 of 58



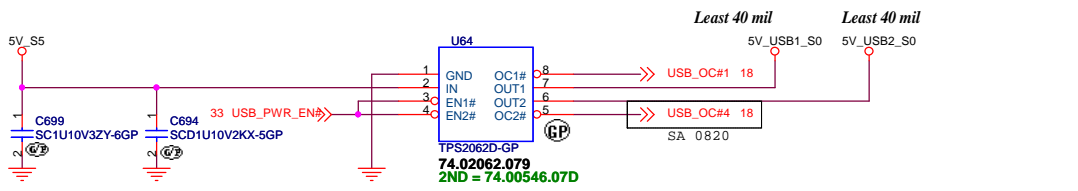
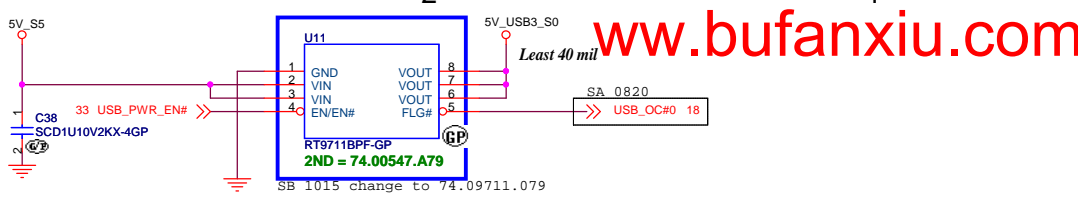
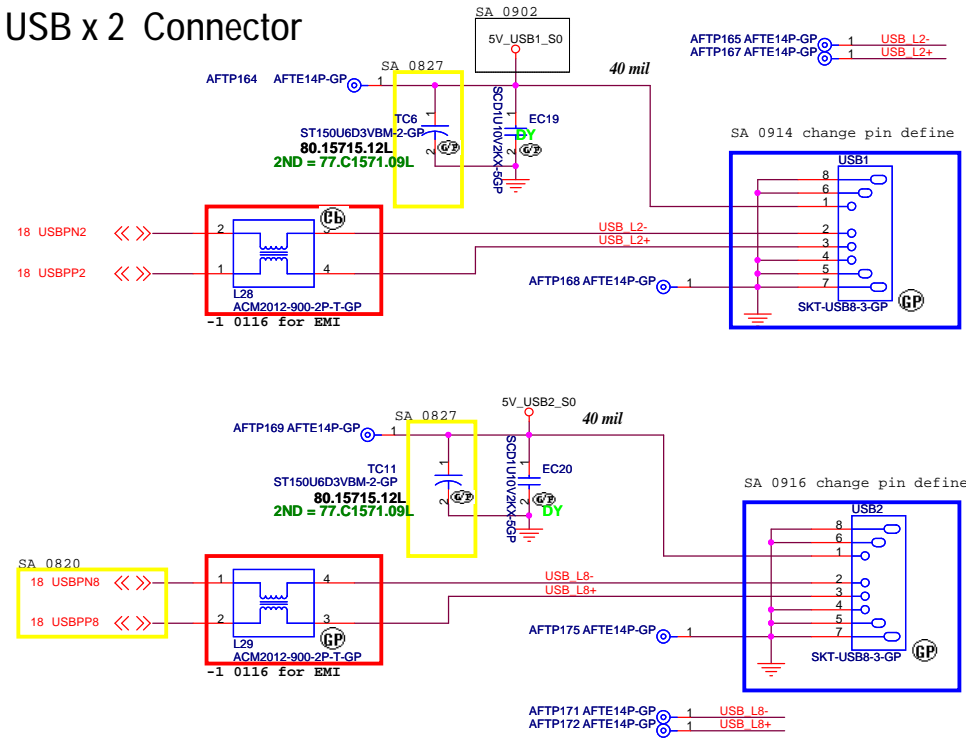
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AFTP103 AFTE14P	1	3D3V_S5
AFTP104 AFTE14P-GP	1	1D5V_S0
AFTP99 AFTE14P	1	5V_S5
AFTP98 AFTE14P-GP	1	E51_RxD
AFTP93 AFTE14P-GP	1	E51_TxD
AFTP91 AFTE14P	1	PCIE_WAKE#
AFTP84 AFTE14P	1	MINI1_CLKREQ#
AFTP180 AFTE14P-GP	1	CLK_PCIE_MINI1#
AFTP188 AFTE14P	1	CLK_PCIE_MINI1
AFTP109 AFTE14P	1	PCIE_RXN2
AFTP108 AFTE14P	1	PCIE_RXP2
AFTP105 AFTE14P	1	PCIE_TXN2
AFTP106 AFTE14P-GP	1	PCIE_TXP2
AFTP185 AFTE14P	1	PLT_RST#
AFTP184 AFTE14P	1	WIF_RF_EN
AFTP182 AFTE14P-GP	1	SMB_CLK
AFTP181 AFTE14P	1	SMB_DATA
AFTP180 AFTE14P	1	WLAN_LED#
AFTP178 AFTE14P	1	MIN2_CLKREQ#
AFTP187 AFTE14P	1	USBPN3
AFTP189 AFTE14P-GP	1	USBPN3
AFTP177 AFTE14P	1	CLK_PCIE_MINI2#
AFTP179 AFTE14P	1	CLK_PCIE_MINI2
AFTP194 AFTE14P-GP	1	USBPN4
AFTP193 AFTE14P-GP	1	USBPN4
AFTP176 AFTE14P-GP	1	CLK48_Cardreader
AFTP101 AFTE14P-GP	1	PCIE_TXP4
AFTP100 AFTE14P	1	PCIE_TXN4
AFTP95 AFTE14P	1	PCIE_RXP4
AFTP94 AFTE14P-GP	1	PCIE_RXN4
AFTP174 AFTE14P-GP	1	CLK_PCIE_NEW#
AFTP173 AFTE14P	1	CLK_PCIE_NEW#
AFTP80 AFTE14P	1	USBPN12
AFTP79 AFTE14P	1	USBPN12
AFTP81 AFTE14P-GP	1	3G_LED#
AFTP78 AFTE14P	1	PM_SLP_S3#
AFTP82 AFTE14P	1	PM_SLP_S4#
AFTP83 AFTE14P	1	NEW_CLKREQ#
AFTP89 AFTE14P	1	PCIE_TXN3
AFTP88 AFTE14P-GP	1	PCIE_TXP3
AFTP90 AFTE14P	1	PCIE_RXN3
AFTP85 AFTE14P	1	PCIE_RXP3
AFTP192 AFTE14P	1	USBPN5
AFTP191 AFTE14P	1	USBPN5
AFTP177 AFTE14P-GP	1	LED_WMAX#
AFTP76 AFTE14P	1	WWAN_EN

USB3

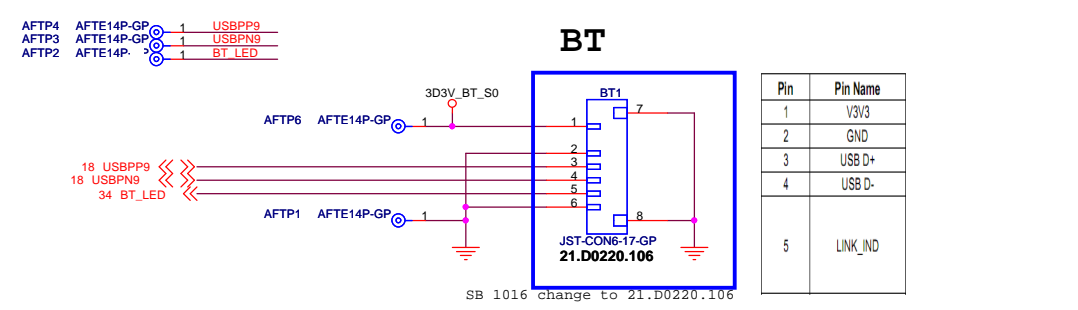
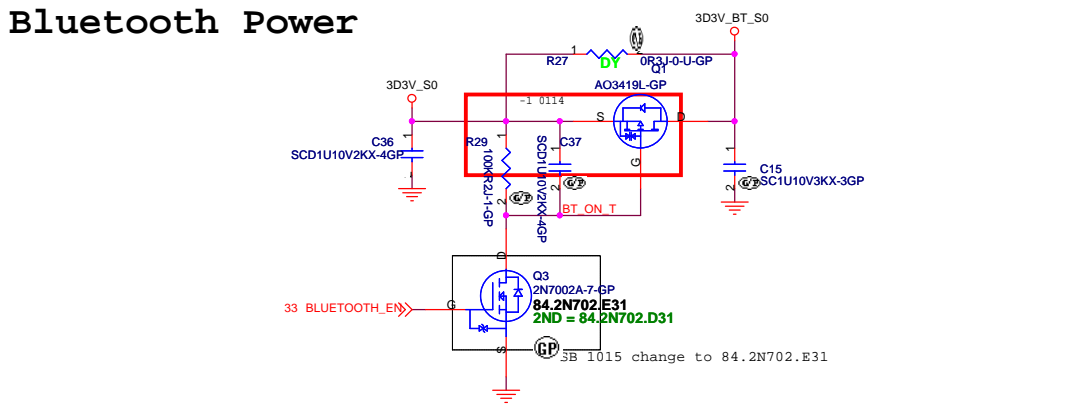
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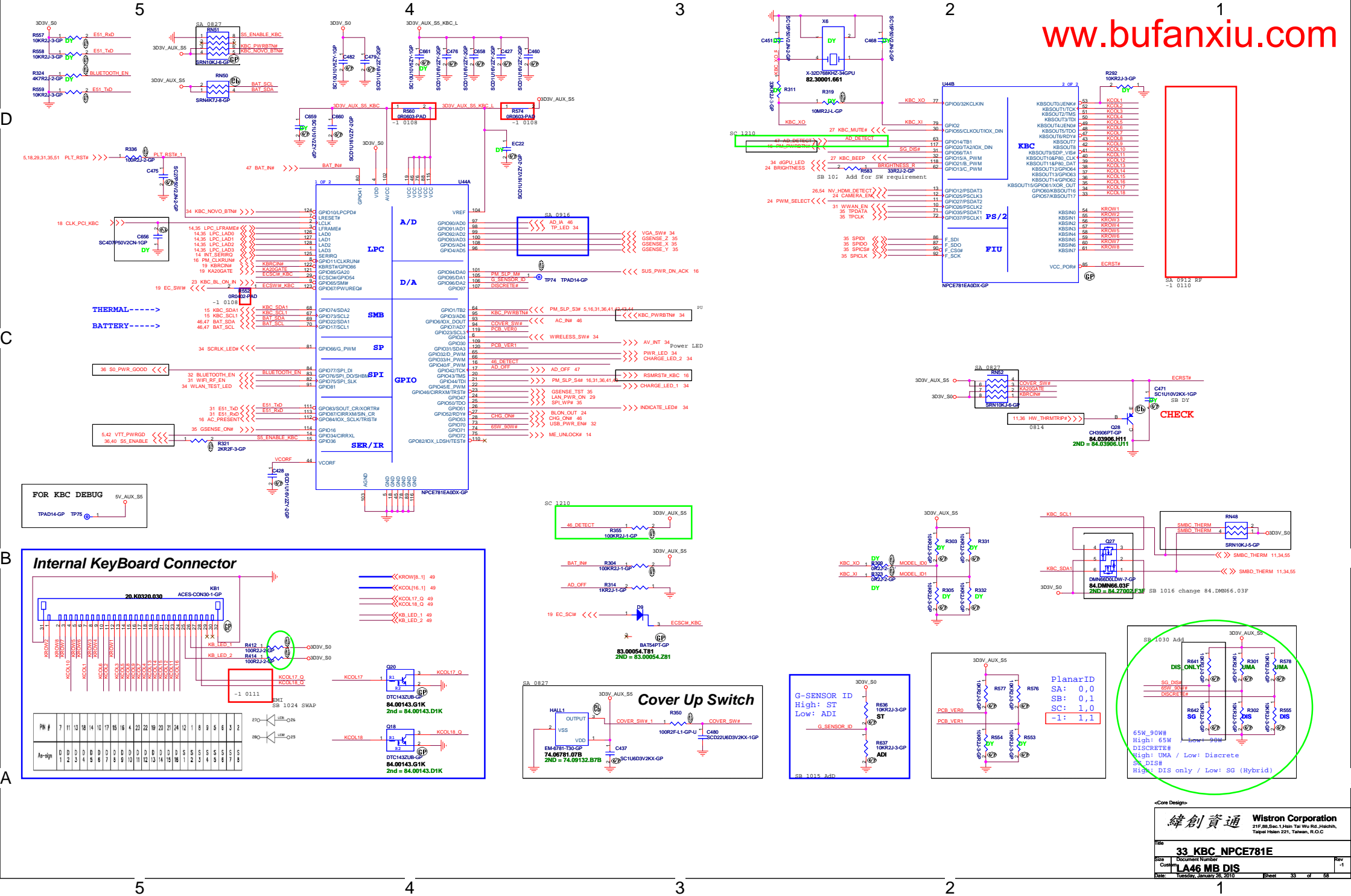


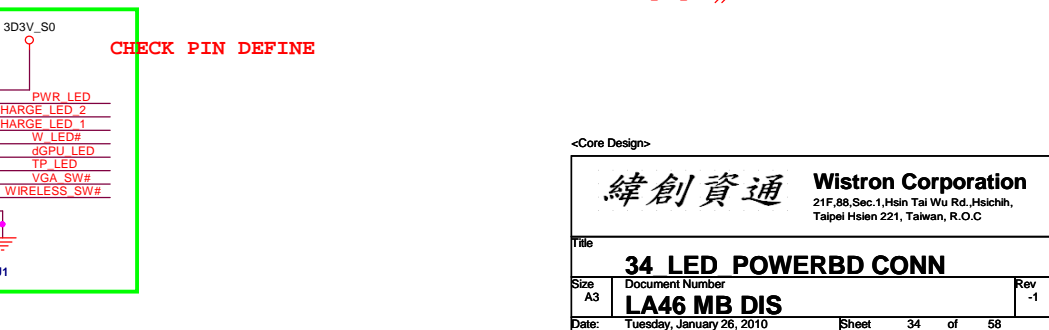
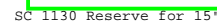
USB x 2 Connector

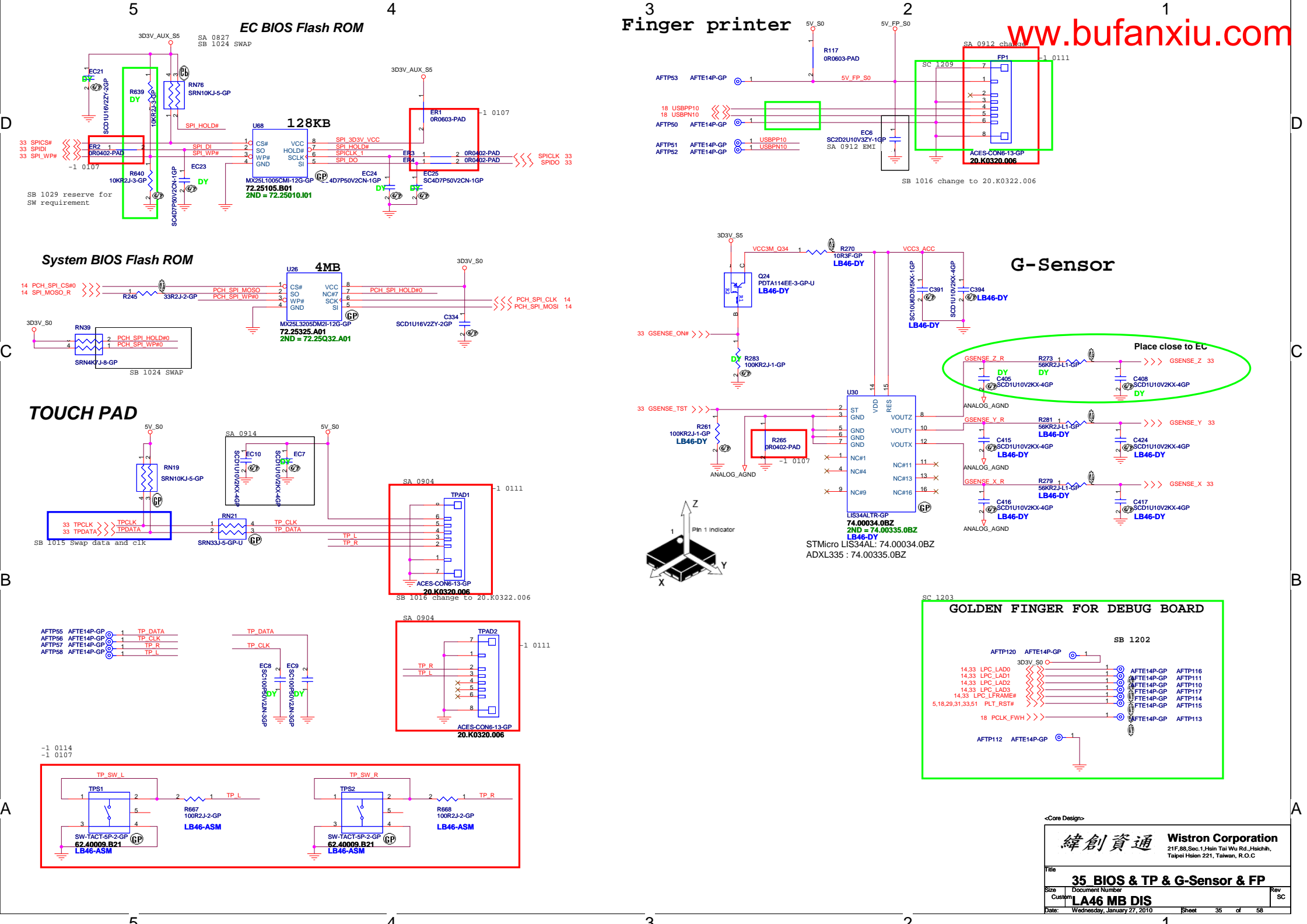


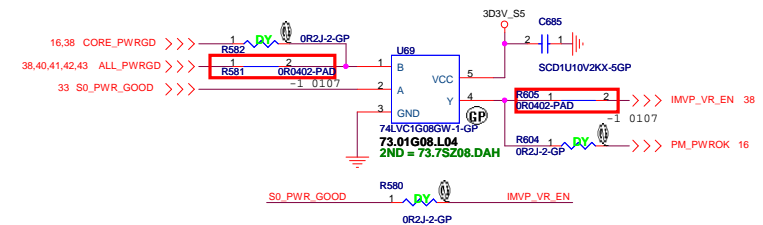
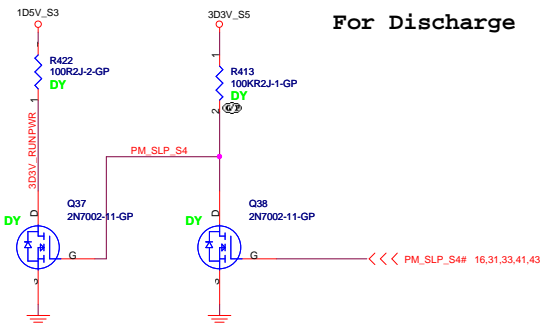
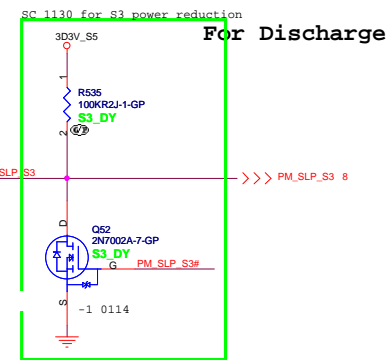
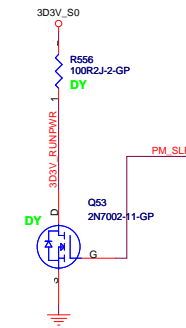
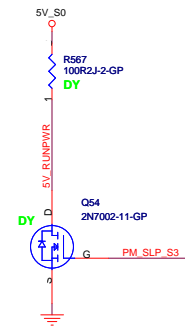
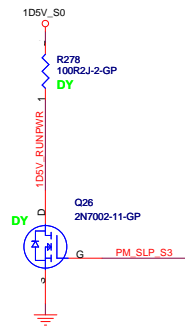
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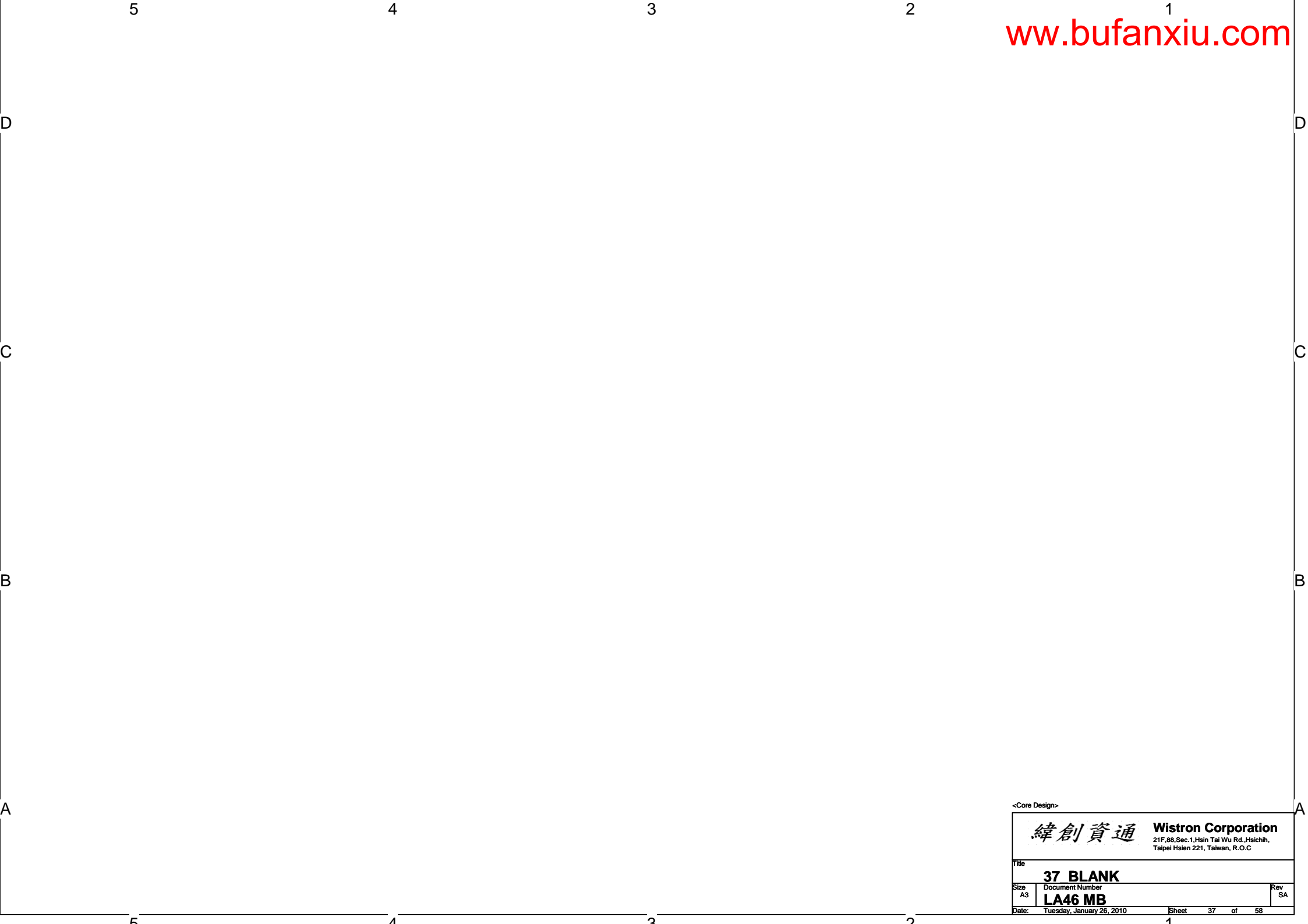


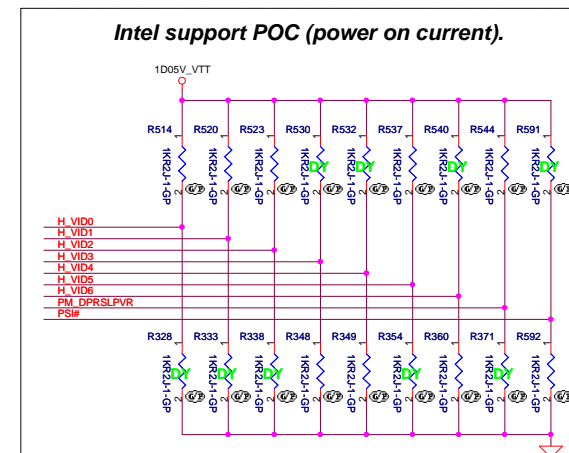
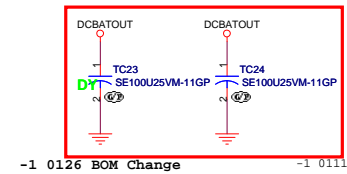


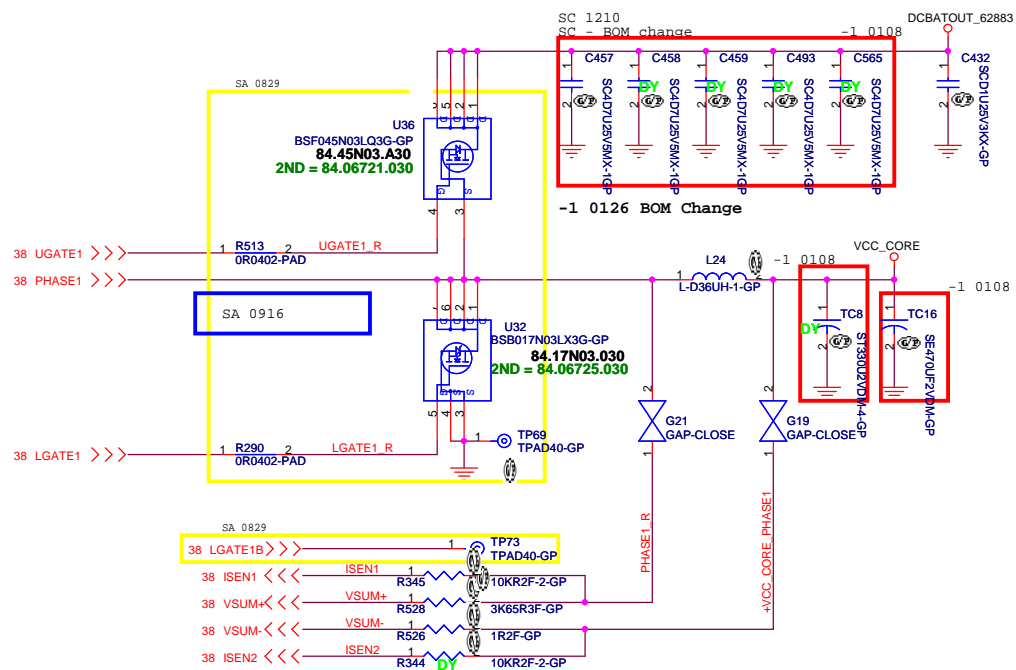
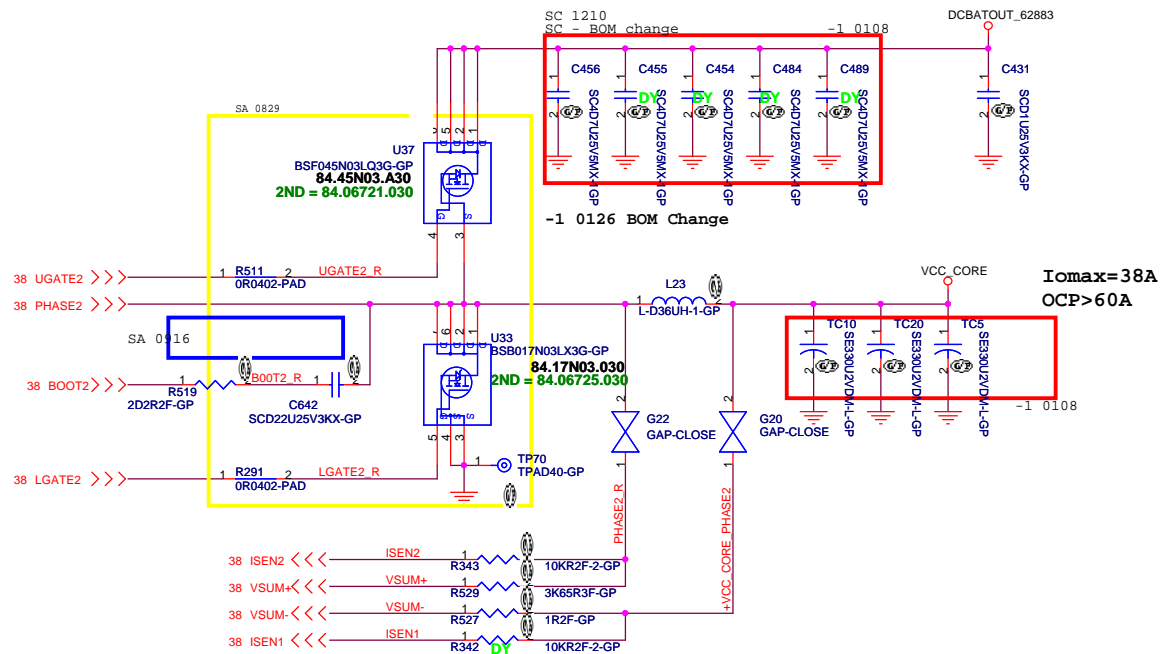




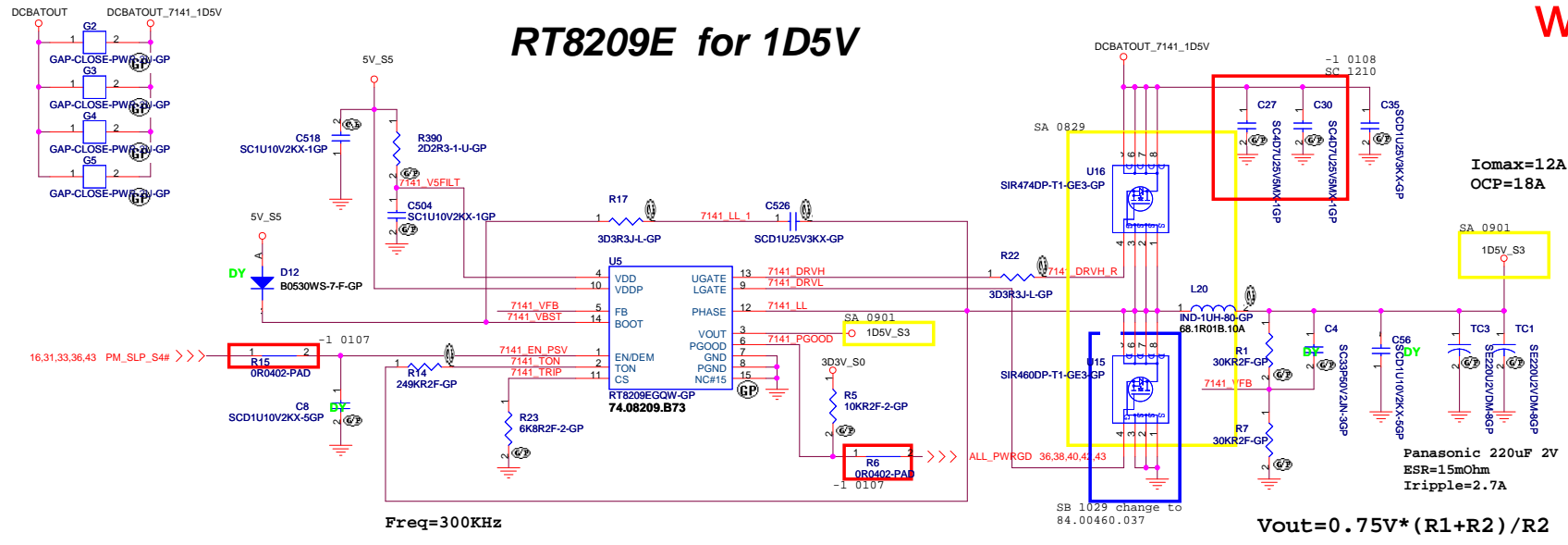




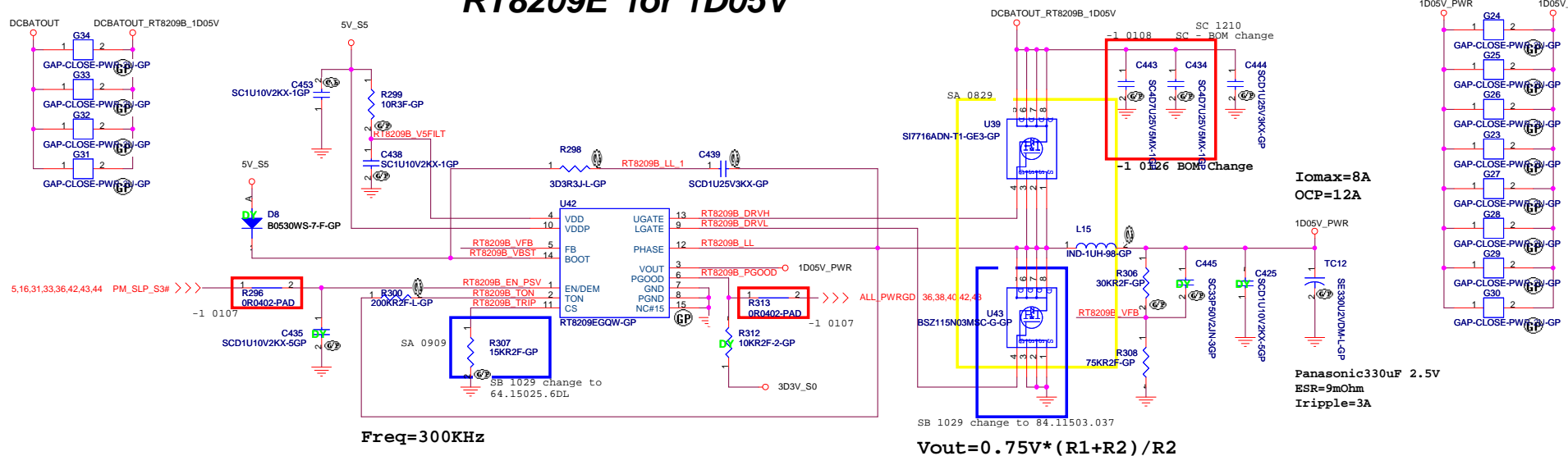




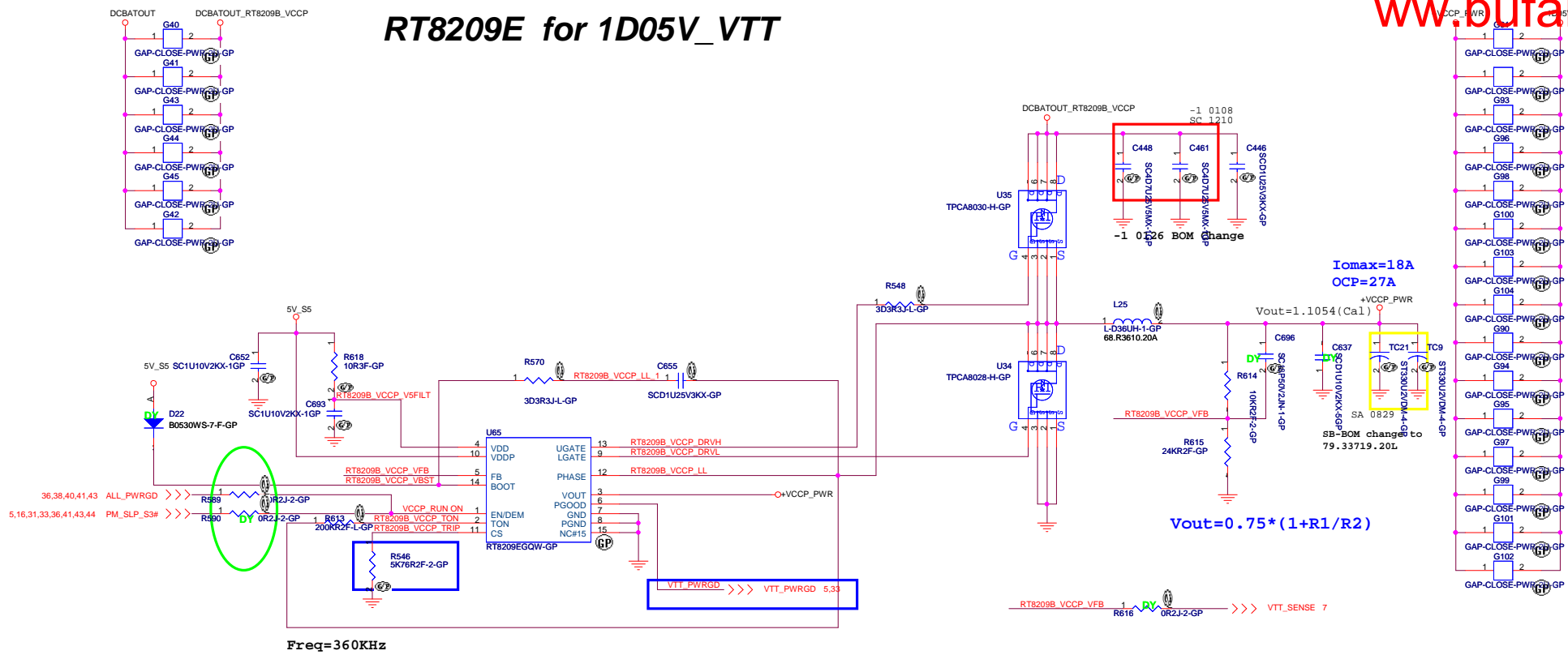
RT8209E for 1D5V



RT8209E for 1D05V



RT8209E for 1D05V_VTT



Freq=360KHz

$$V_{out} = 0.75 * (1 + R1/R2)$$

Iomax=18A
OCP=27A

RT8209B_VCCP_VFB
R615
24KR2F-GP
N-1-GP
24KR2F-2-GP
SA 0829
SB-BOM change
79.33719.20L

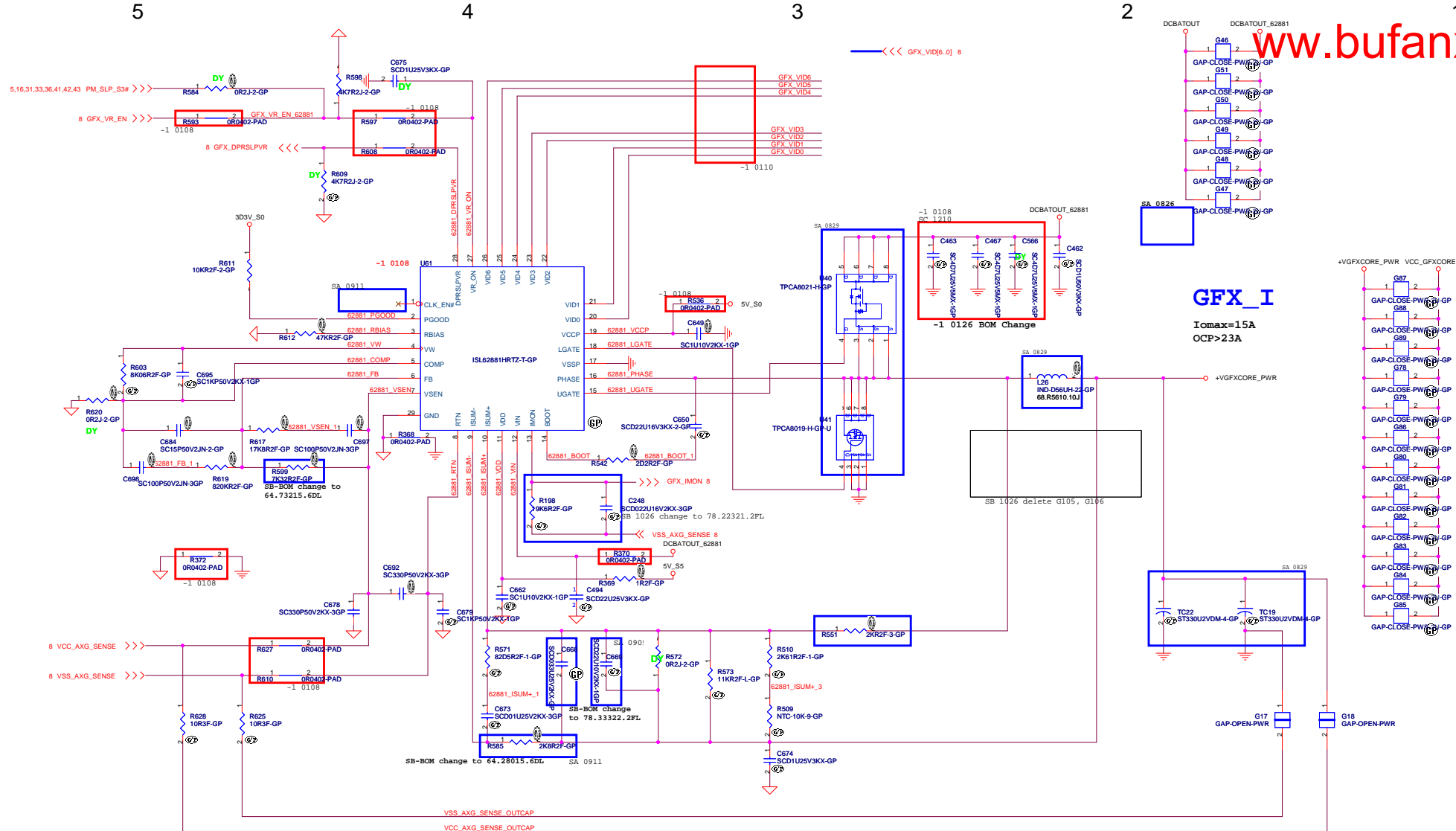
B 1 DY 0R2J-2-GP >>> VTT_SENSE

<Core Design>

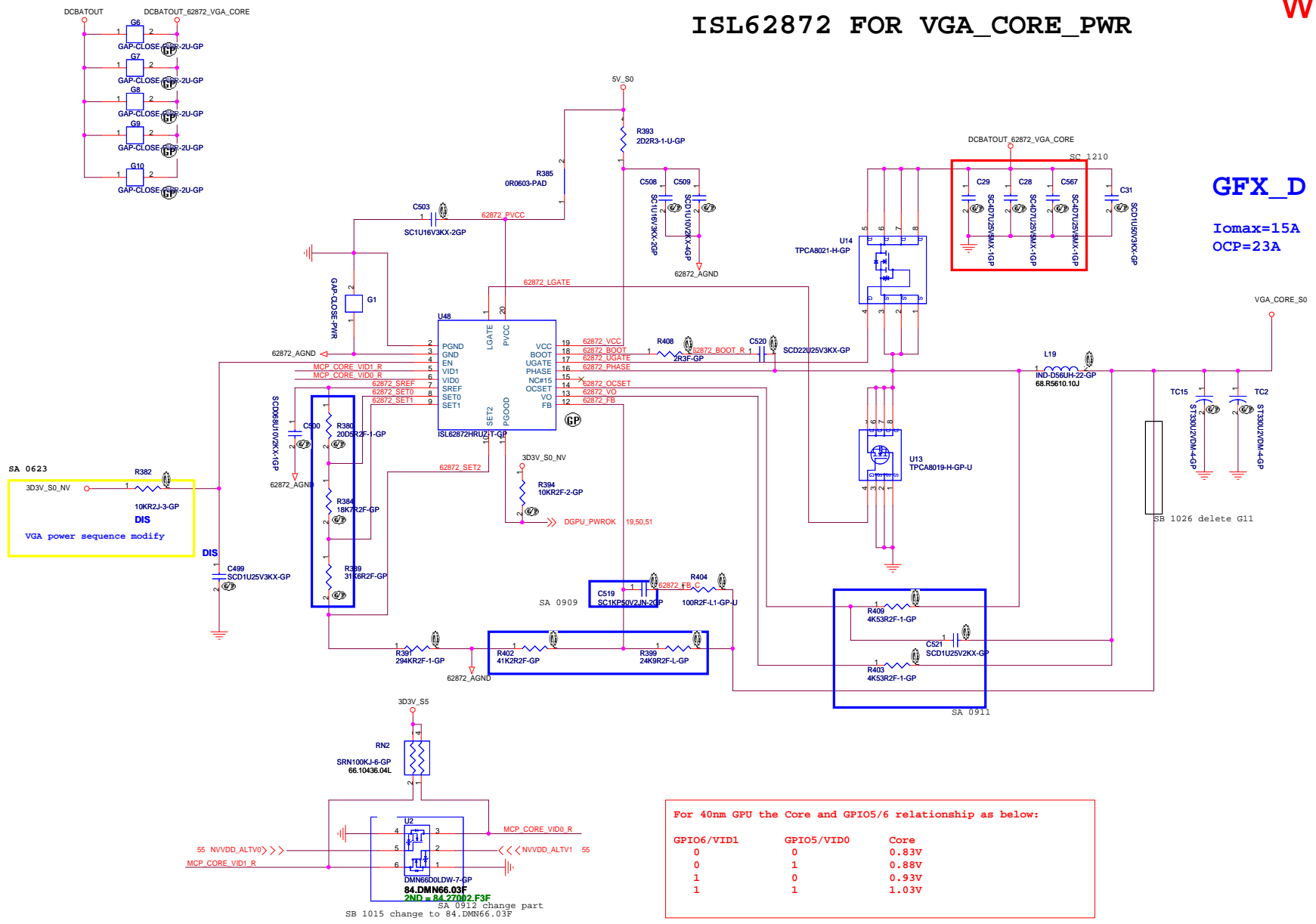
緯創資通

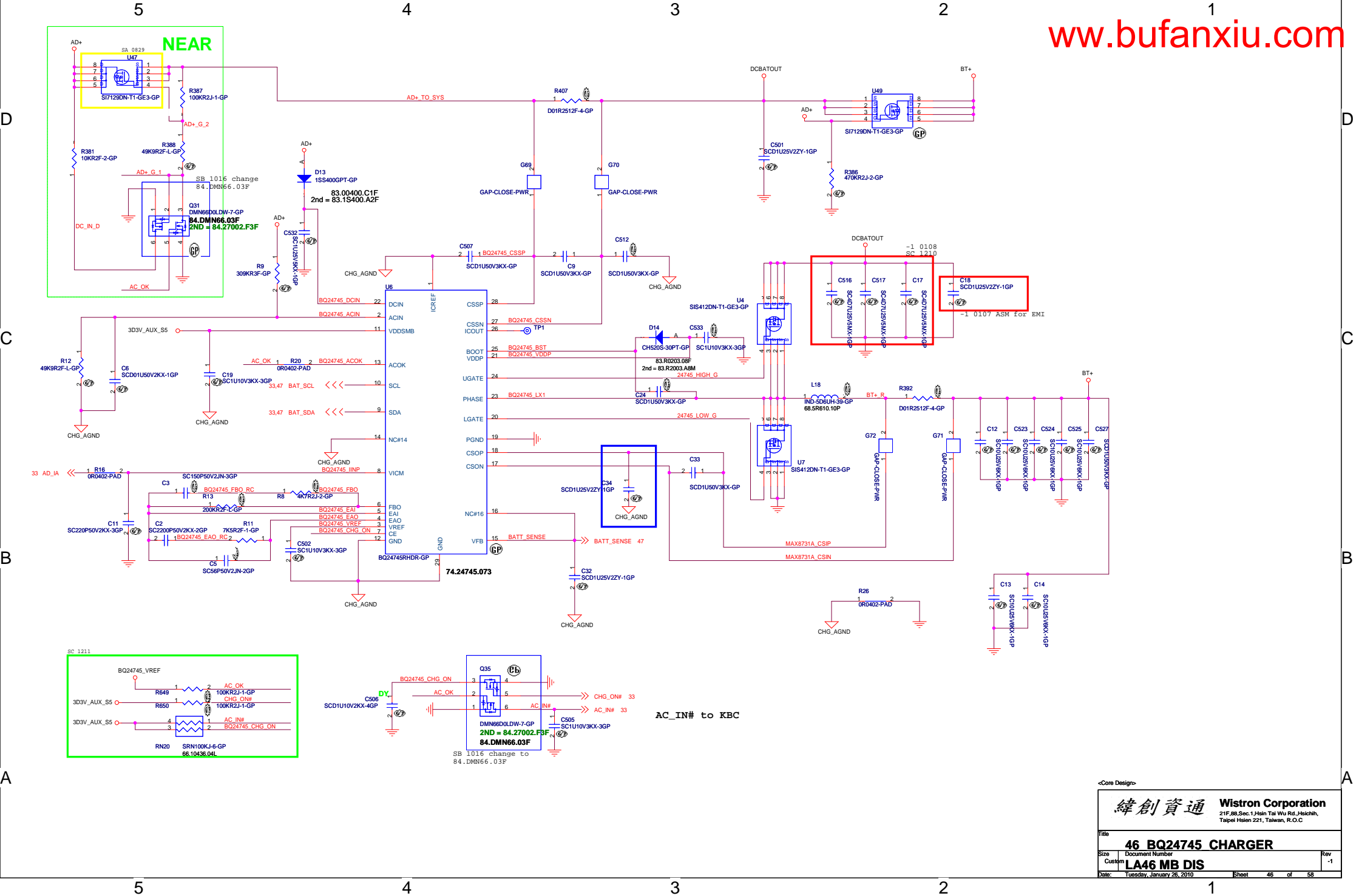
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title			
42 RT8209E 1D05V VTT			
Size	Document Number	Rev	
Custom	LA46 MB DIS	-1	
Date:	Wednesday, January 27, 2010	Sheet	42 of 58



ISL62872 FOR VGA_CORE_PWR





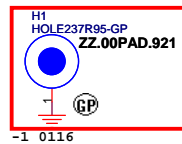
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4

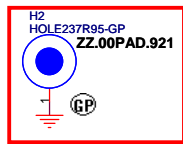
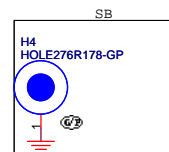
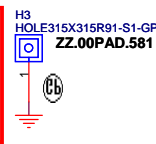
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2

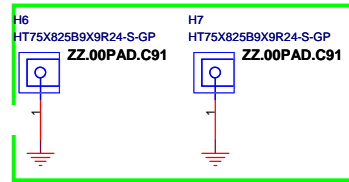
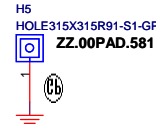
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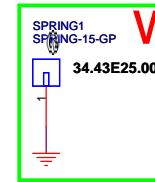
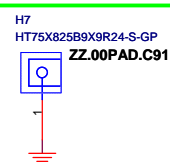
-1 0116

SC 1130 Remove H2
-1 0110

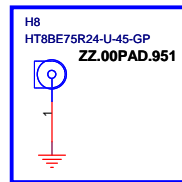
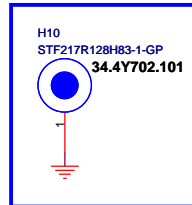
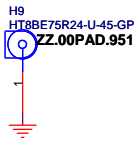
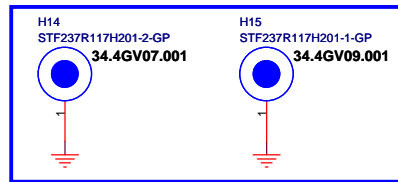
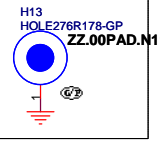
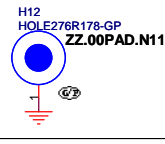
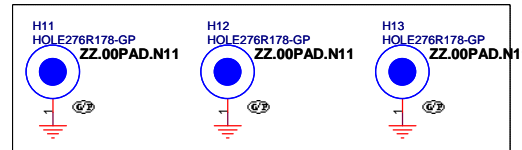
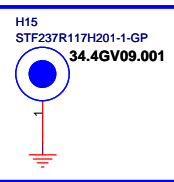
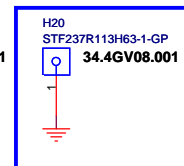
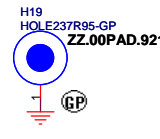
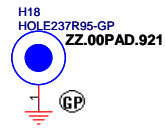
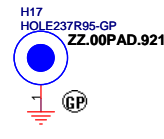
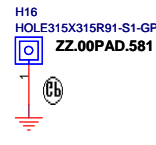
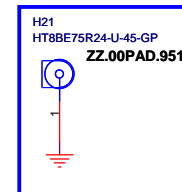
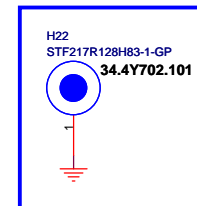
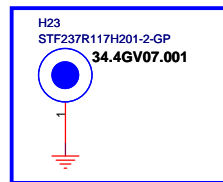
ZZ.00PAD.N11



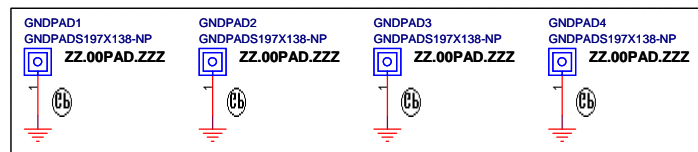
SC 1130 CHECK, H6,H7 change to ZZ.00PAD.C91



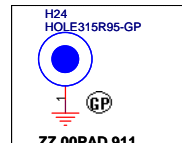
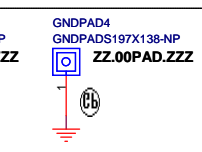
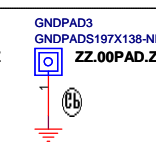
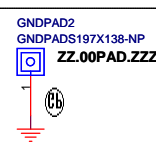
SC 1209

SB 1016 change to
ZZ.00PAD.951SB 1016 change to
34.4Y702.101SB 1016 change to
34.4GV07.001SB 1016 change to
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to ZZ.00PAD.951SB 1016 change to
34.4Y702.101

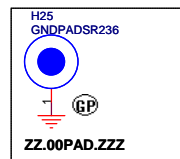
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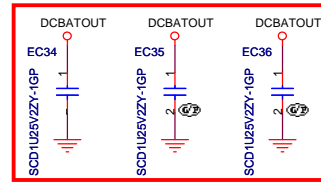
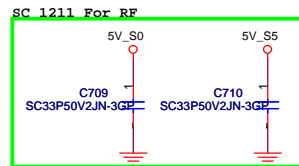
SB 1019 Add GND PAD



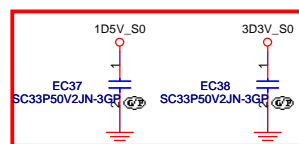
SB 1021 Add ZZ.00PAD.911



SB 1021 Add GNDPADSR236



-1 0107 ASM for EMI



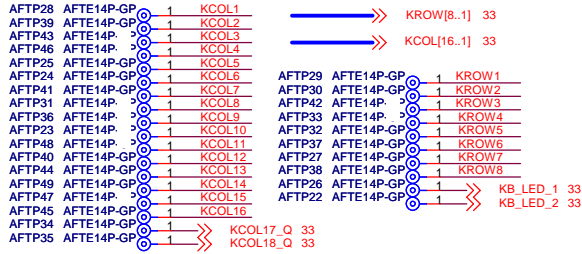
-1 0116

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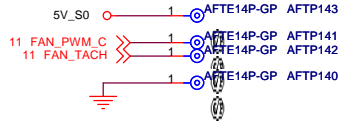
緯創資通

Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

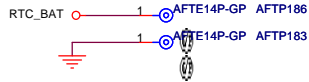
Near KB1 Keyboard



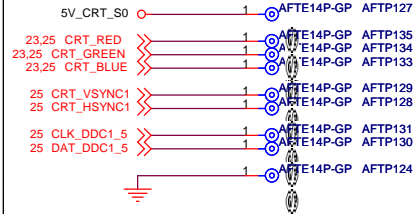
Near FAN1



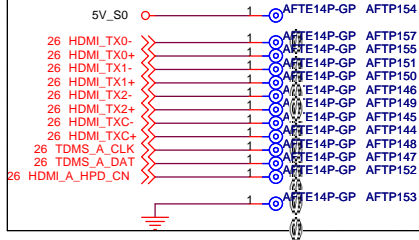
Near RTC1



Near CRT_CN1



Near HDMI_CN1



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Title			
49 AFTE TP			
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Date:	Tuesday, January 26, 2010	Sheet	49 of 58

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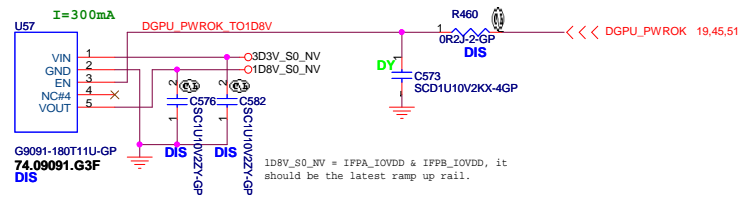
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+1.5V to FBVDD Transfer

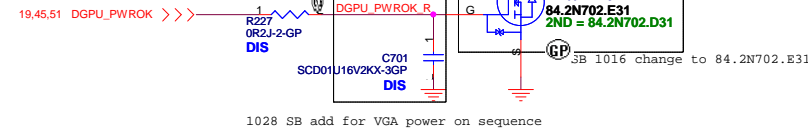
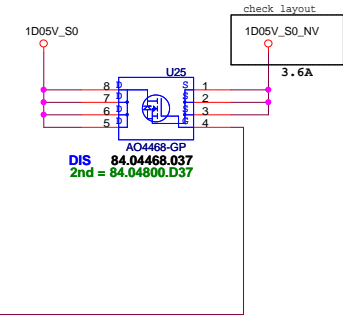
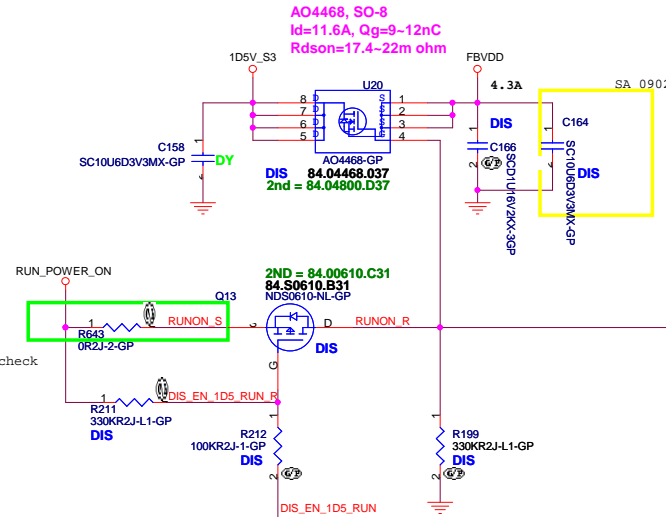
+1.05V to 1.05V NV Transfer

www.bufanxiu.com

+3VS to 1.8V Transfer



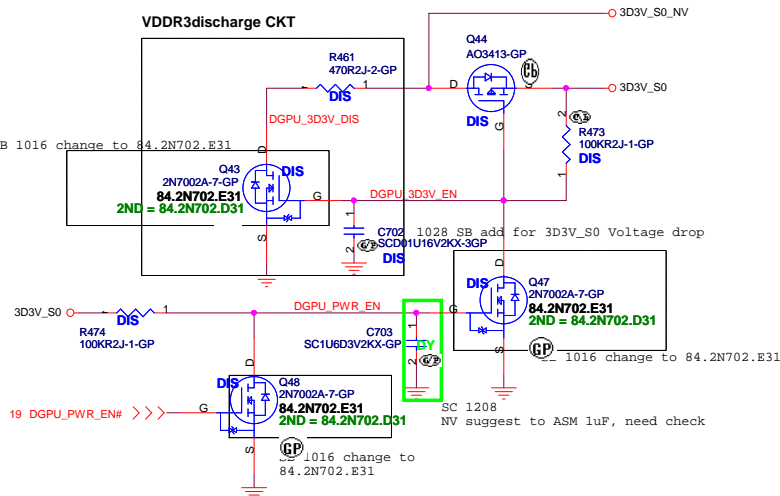
SC 1208
NV suggest to use 200K, need check



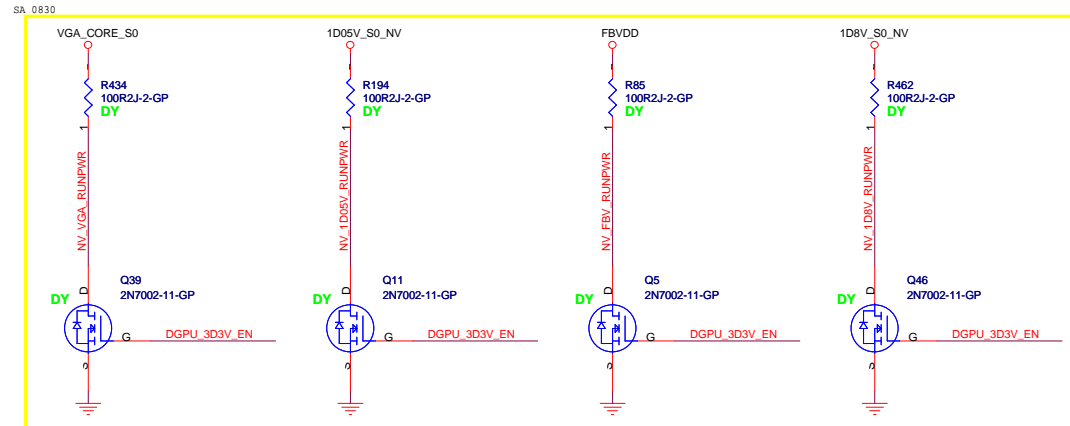
+3VS to 3.3V_DELAY Transfer

3.3v (580mA)

VDDR3discharge CKT



system turn on 3D3V_S0_NV --> VGA_CORE_S0
DGPU_PWROK --> FBVDD, 1D05V_S0_NV, 1D8V_S0_NV



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipai Hsien 221, Taiwan, R.O.C

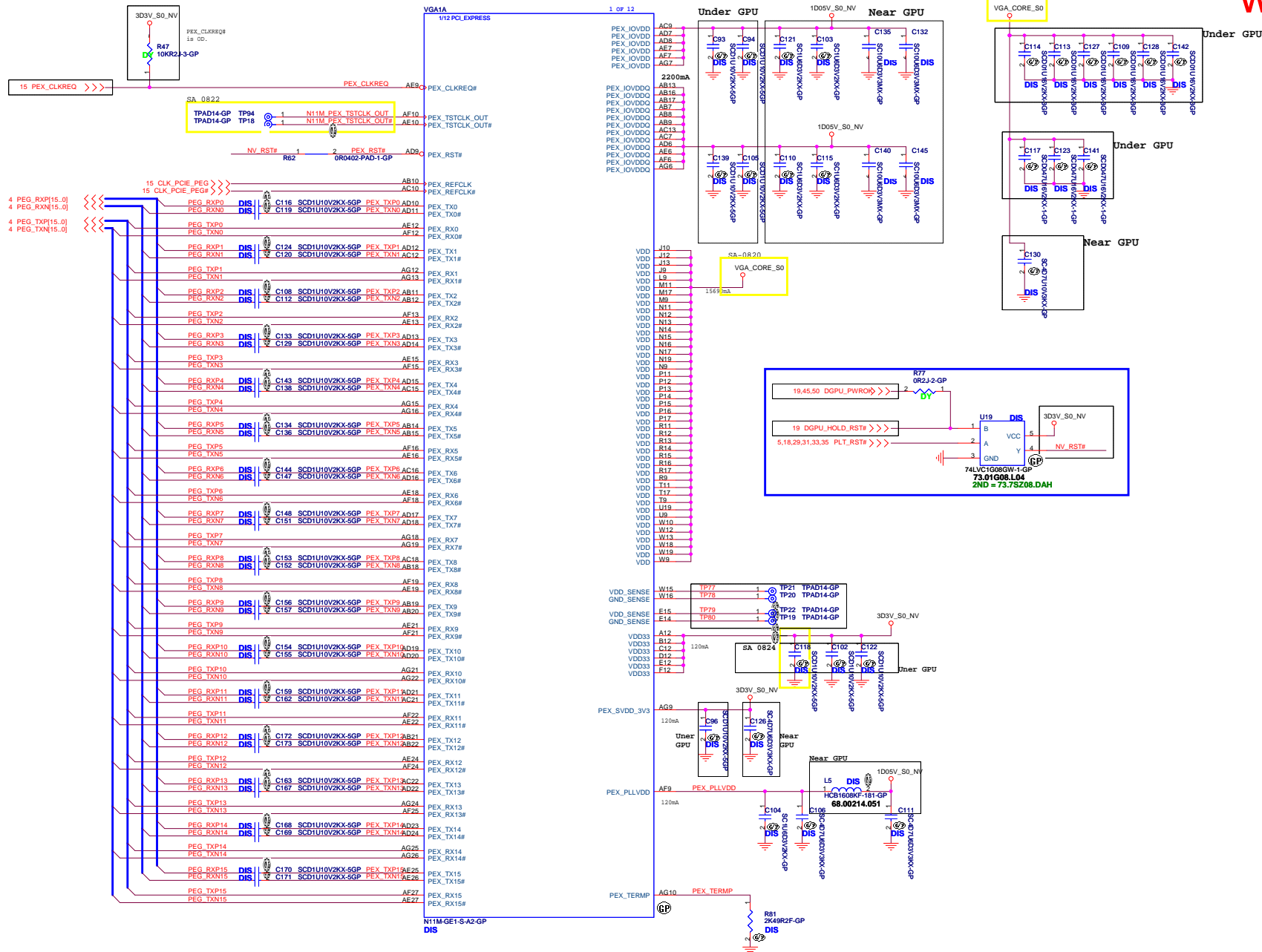
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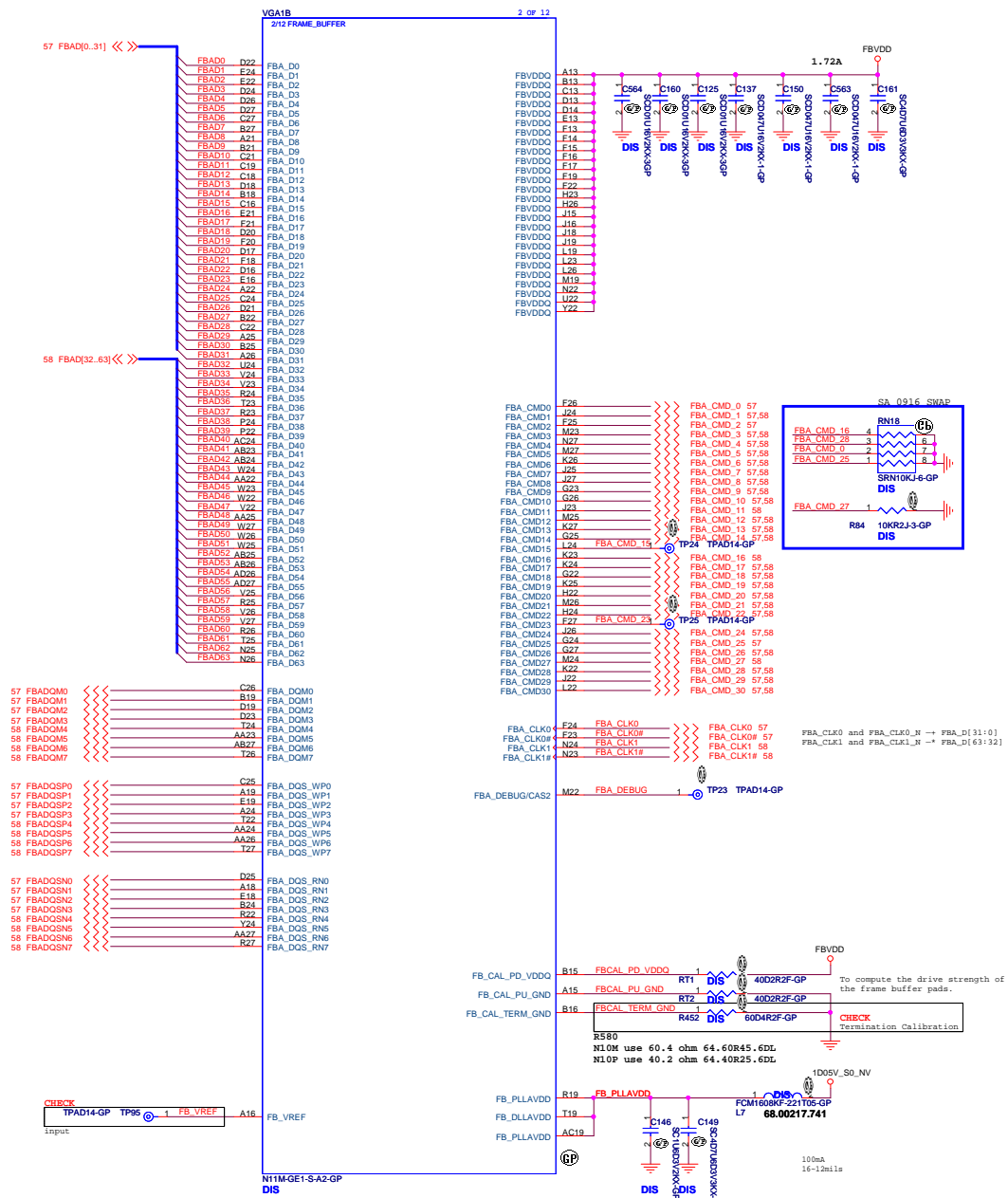
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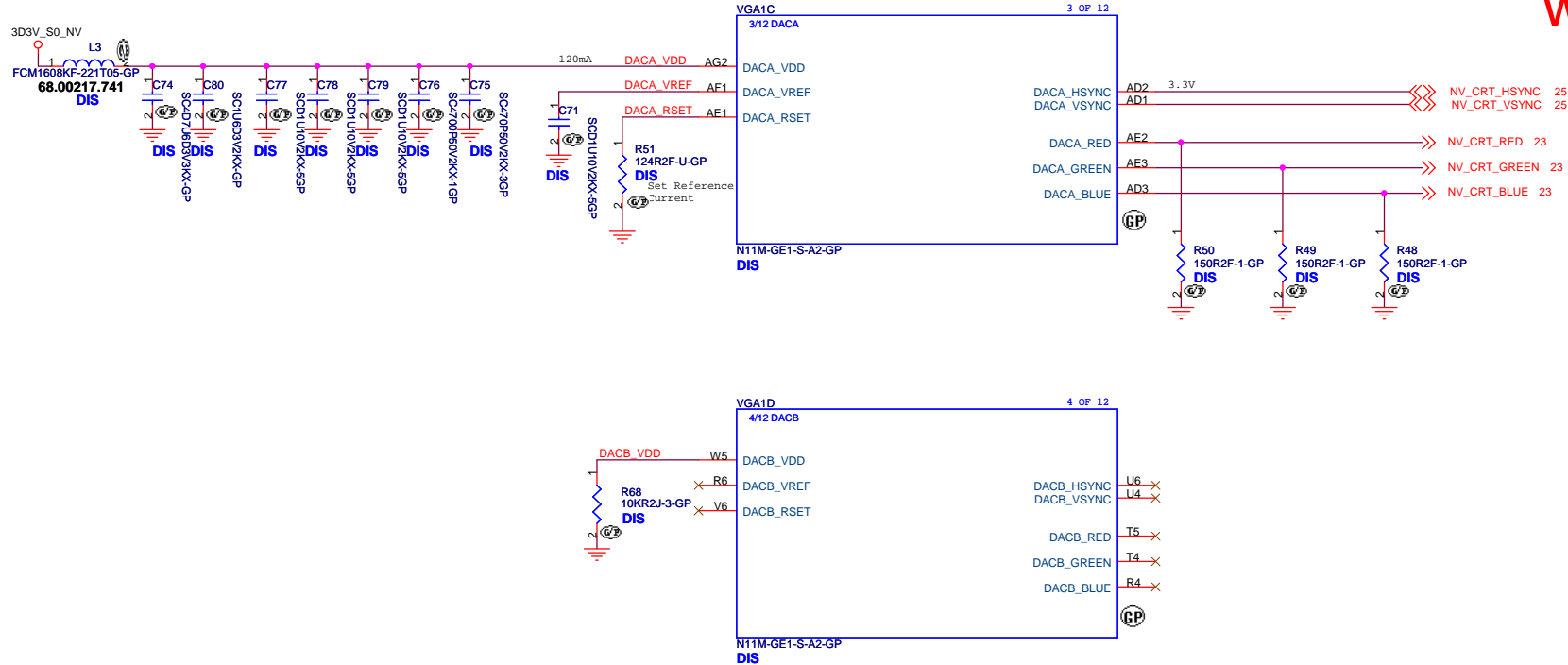
Date: Tuesday, January 26, 2010

Sheet 50 of 58

Rev -1

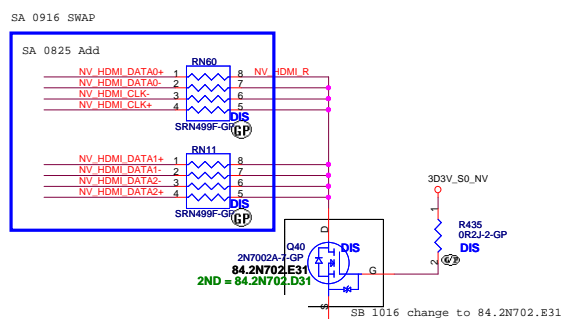
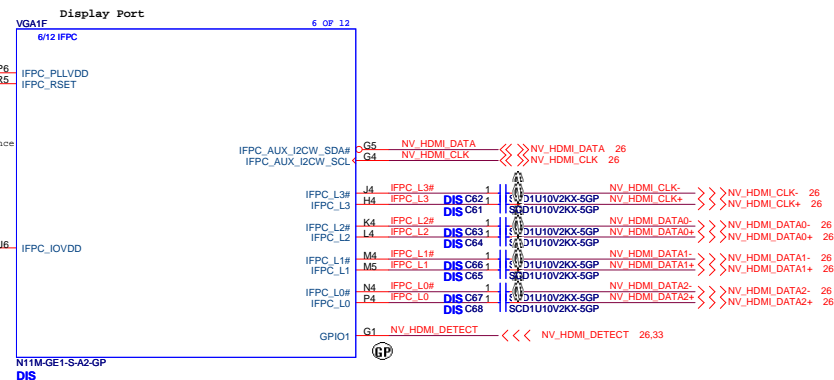
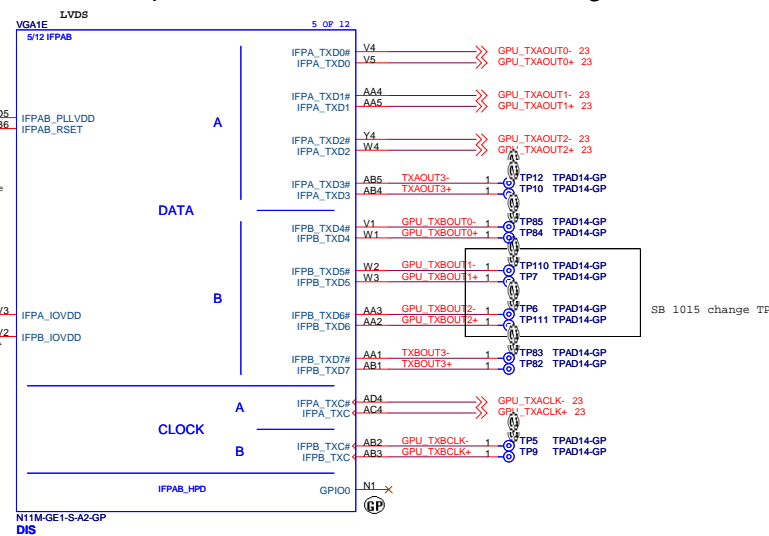
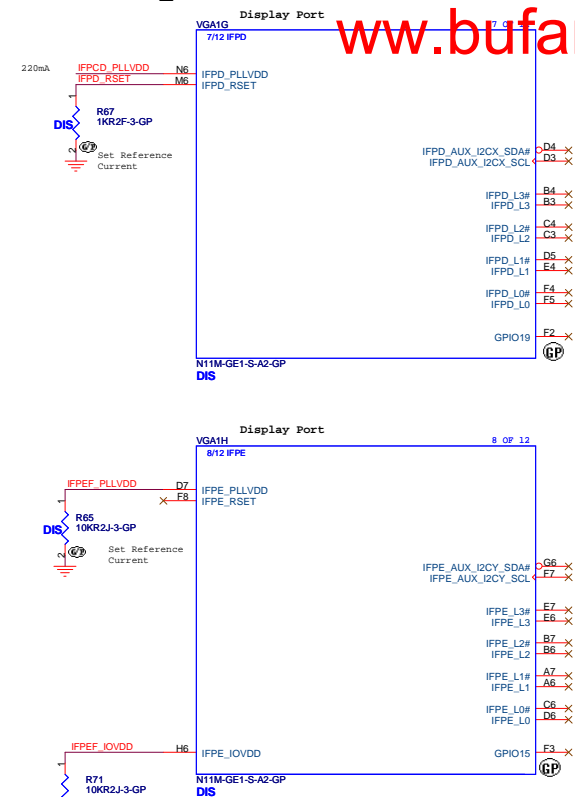




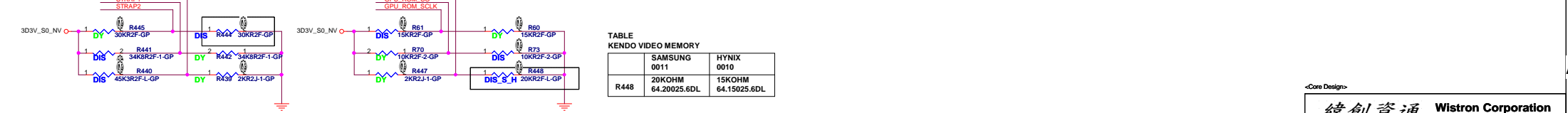
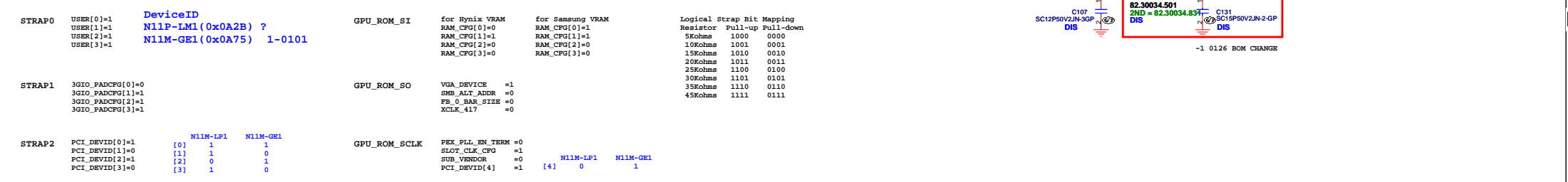
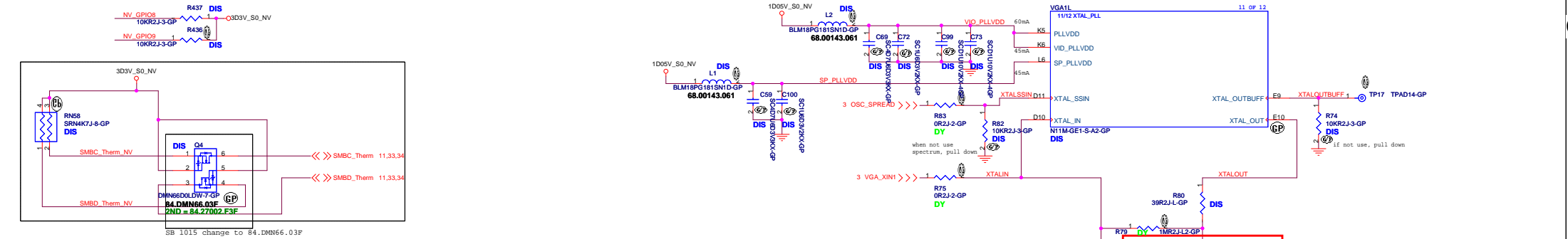
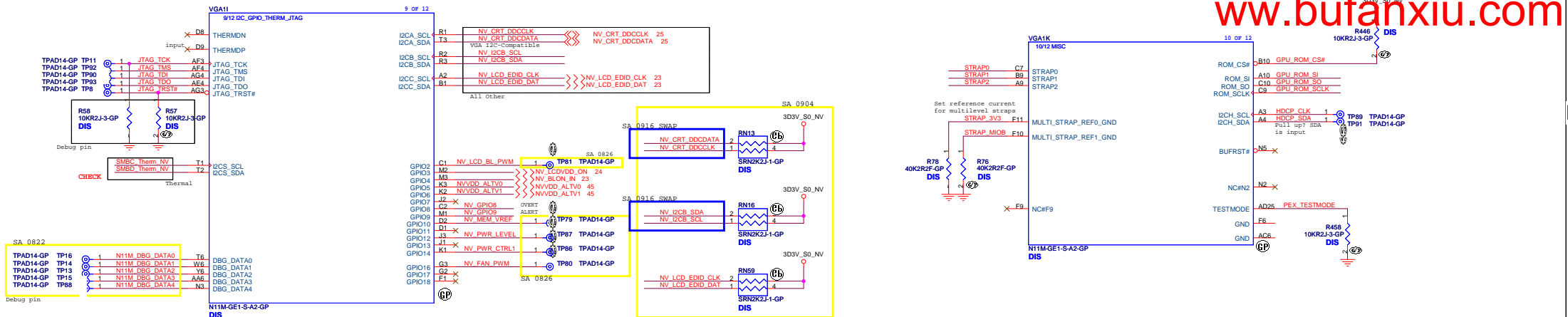


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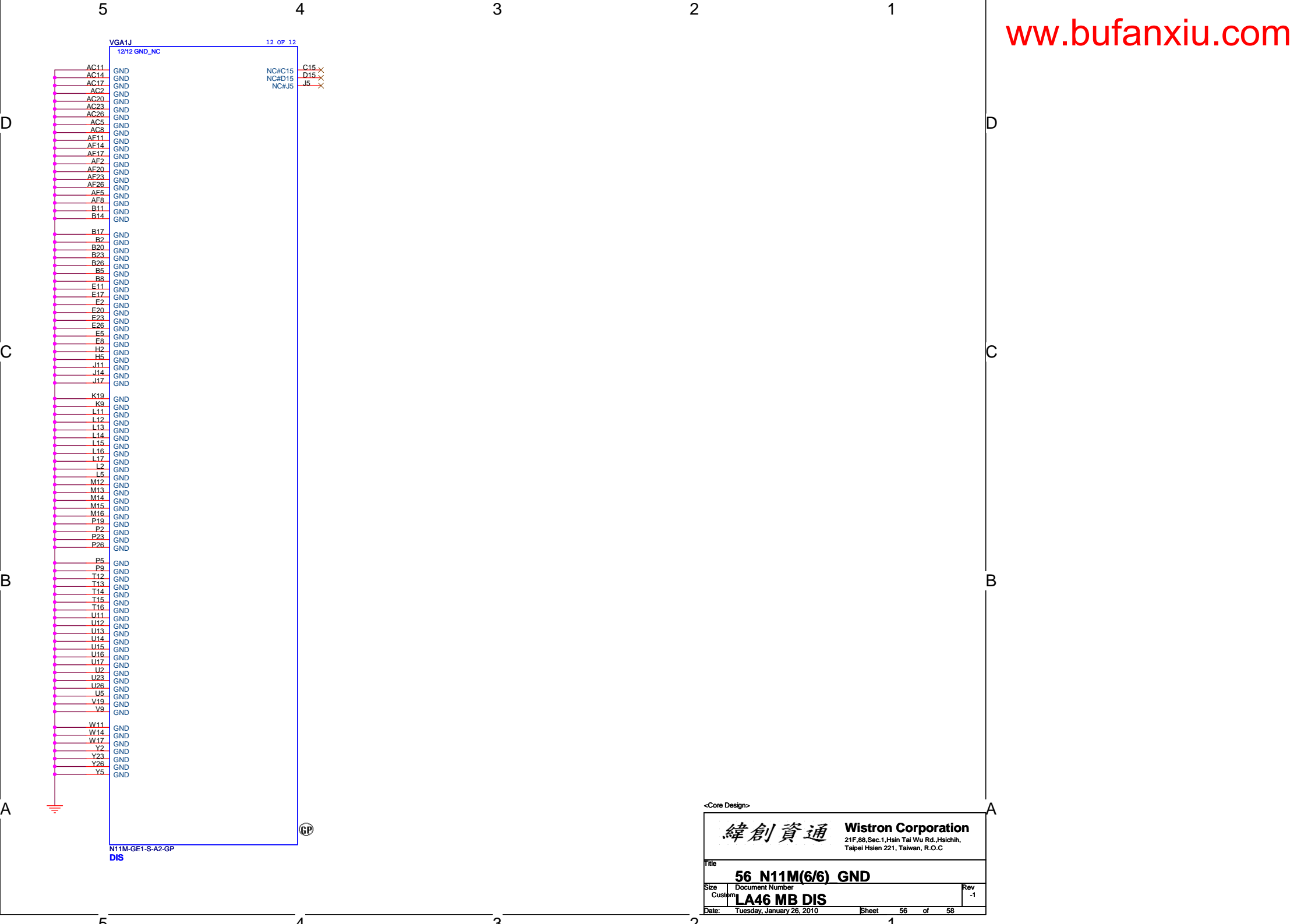
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		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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53 N11M(3/6) DAC			
Size	Document Number		Rev
Custom	LA46 MB DIS		-1
Date:	Tuesday, January 26, 2010	Sheet	53 of 58



Direct HDMI Connection



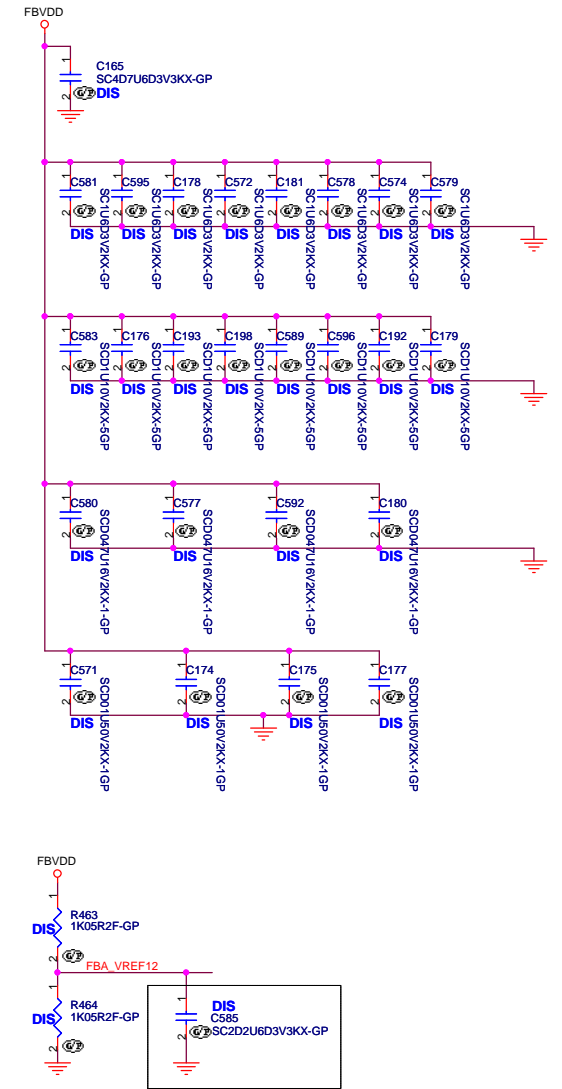
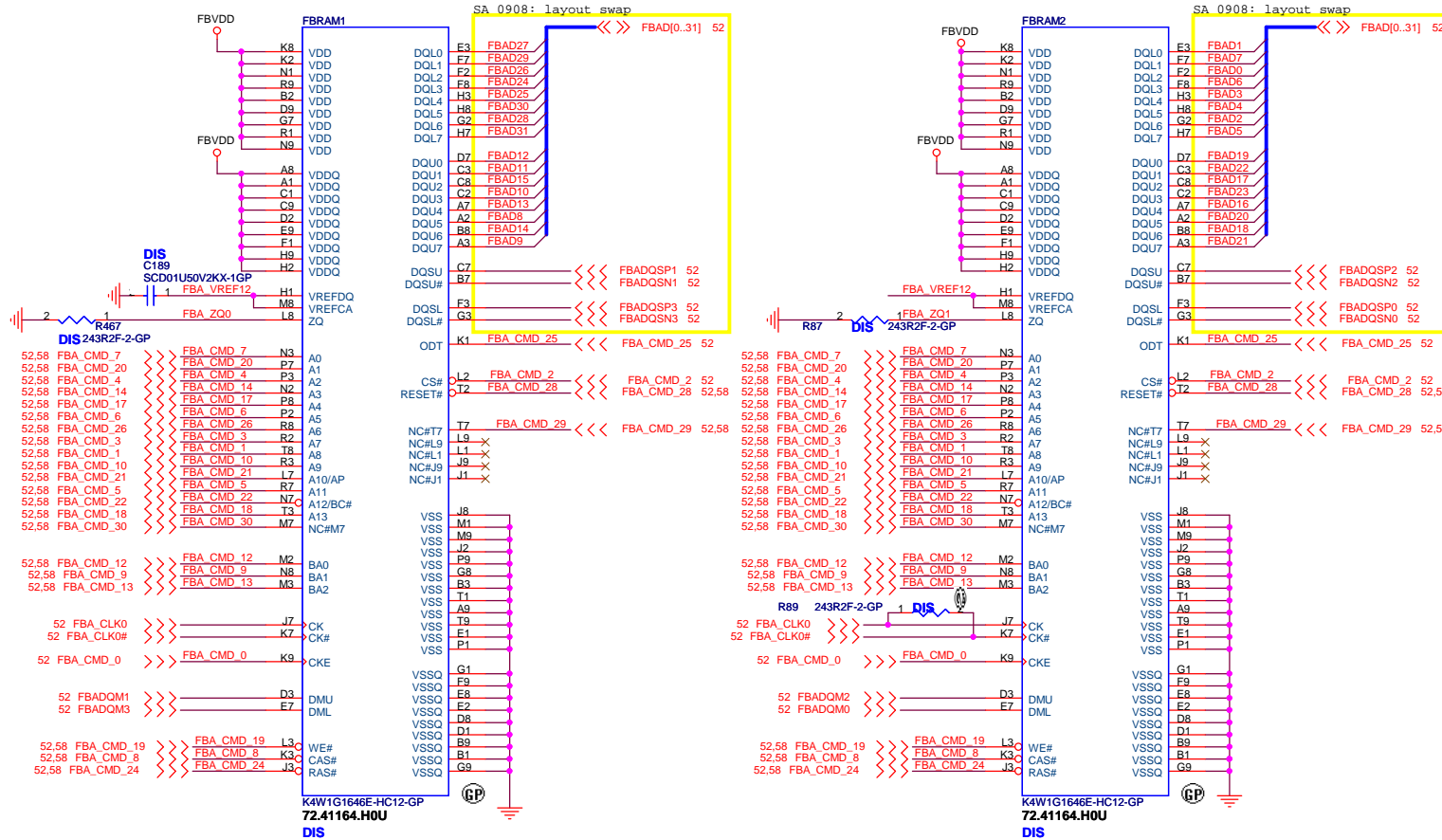
KENDO VIDEO MEMORY		
	SAMSUNG	HYNIX
R448	20KOHM	15KOHM
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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C			
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56 N11M(6/6) GND			
Size	Document Number	Rev	
Custom	LA46 MB DIS	-1	
Date:	Tuesday, January 26, 2010	Sheet	56 of 58

Mode C Command Mapping



2nd: 72.51G63.C0U (IC SDRAM H5TQ1G63BFR-12C FBGA)

