Enrico 14

Muxless Discrete/UMA Schematics Document

AMD Ontario CPU FT1

AMD GPU Seymour XT

FCH HUDSON M1

PCB :10265

2010-04-21

REV : A00

DY :None Installed
UMA:UMA and Muxless platform installed
DIS_PX:DIS and Muxless platform installed
PSL:10mW internal schematic
10mW: 10mW schematic installed
Surge: Surege schematic installed
GIGA: GIGA schematic installed
10/100: 10/100 schematic installed
ROB: ROBOSON GPU installed

<Variant Name>

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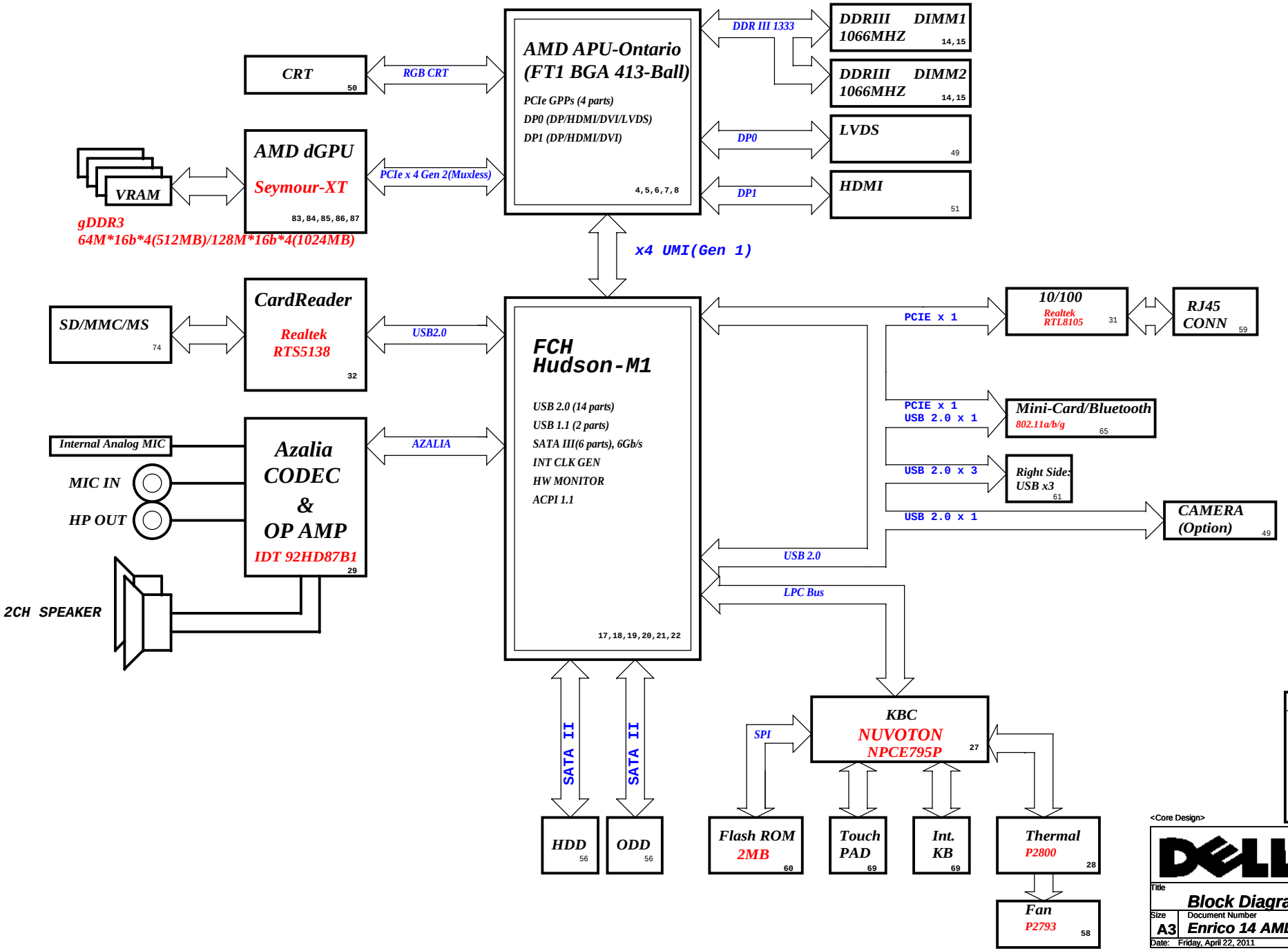
Title: Cover Page		
Size: A3	Document Number: Enrico 14 AMD	Rev: A00
Date: Friday, April 22, 2011	Sheet 1 of 109	

Project code : 91.4IU01.001
PCB P/N :
Revision : 10265-1

AMD Brazos UMA/Discrete Block Diagram



CHARGER	
BQ24707	40
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC	
TPS51125A	41
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5

APU Core/NB Power	
ISL6265CHRTZ-T	42, 43
INPUTS	OUTPUTS
DCBATOUT	APU_VDD APU_VDDNB

DDRIII SUS	
TPS51216RUKR	44
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

DDRIII VTT	
TPS51216RGER	44
INPUTS	OUTPUTS
DCBATOUT	0D75V_S0

APU VDDR/VDDP	
TPS51218	46
INPUTS	OUTPUTS
DCBATOUT	1D1V_S5

AMD APU/FCH CORE Power	
TPS51218	46
INPUTS	OUTPUTS
DCBATOUT	1V_S0

AMD GPU CORE	
RT8208BGQW	92
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

AMD GPU CORE	
RT8015B	47
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

PCB LAYER
L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

<Core Design>

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Title: Block Diagram

Size	Document Number	Rev
A3	Enrico 14 AMD	A00

Date: Friday, April 22, 2011 Sheet 2 of 109

REQUIRED SYSTEM STRAPS

	AZ_SDOUT	PCI_CLK1	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1	LPC_CLK2
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT	Enable boot timer function
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)	Disable boot fail timer function DEFAULT

TYPE ENABLED	EC_PWM2	EC_PWM3
Reserved	2.2-kohm 5% pull-down	2.2-kohm 5% pull-down
LPC ROM	Not connected.	2.2-kohm 5% pull-down
SPI ROM	2.2-kohm 5% pull-down	Not connected.
Reserved	Not connected.	Not connected.

Note: EC_PWM2, EC_PWM3 default have internal 10kohm PU.

USB Table

Pair	USB Device
0	USB 2.0 EXT.Port1
1	Mini Card1 (WLAN)
2	USB 2.0 EXT.Port1
3	NC
4	NC
5	NC
6	USB 2.0 EXT.Port1
7	CCD Camera
8	NEWCARD
9	Card Reader
10	NC
11	NC
12	NC
13	NC

PCIe Routing

	APU
LANE0	LAN
LANE1	~~WWAN~~
LANE2	WLAN
LANE3	~~CardReader~~

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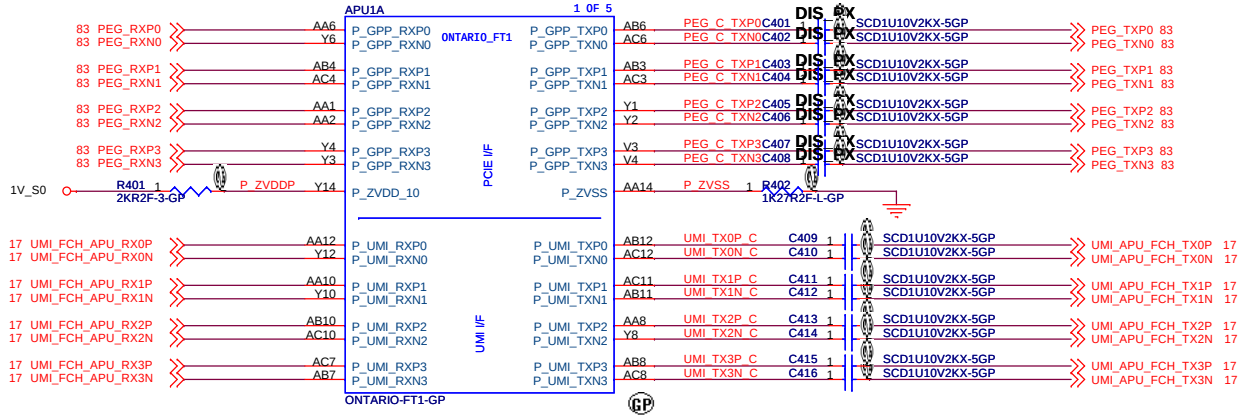
Title: Table of Content

Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 3 of 109

SSID = CPU



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Title		
APU_PCIE(1/5)		
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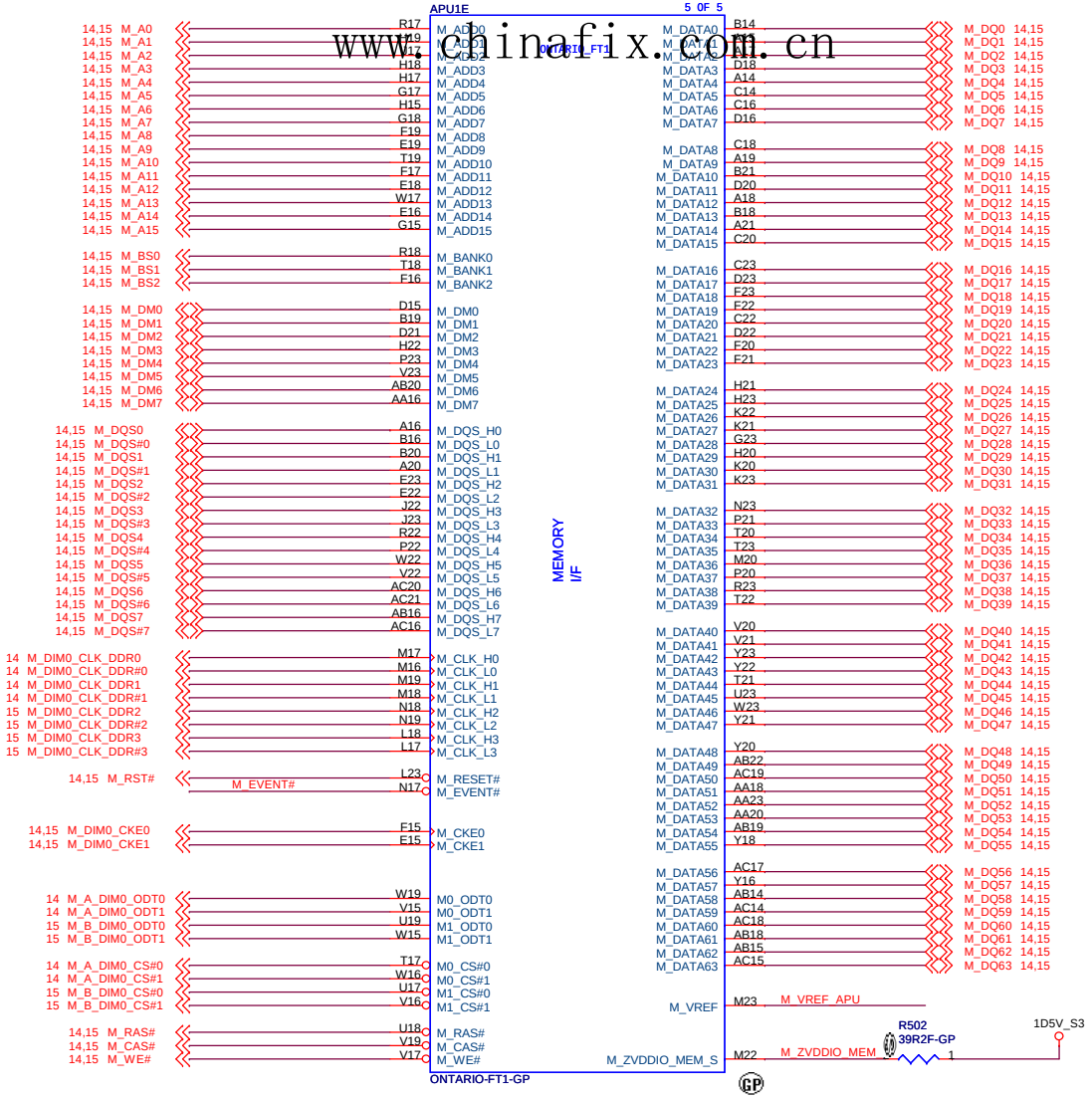
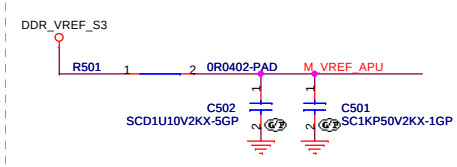
Date: Friday, April 22, 2011	Sheet 4 of 109	

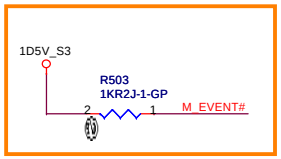
SSID = CPU



APU_VREF



LAYOUT: place them close to APU



AMD Confirm: PU Needed even if not used

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Title: APU_DDR(2/5)

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Date: Friday, April 22, 2011 | Sheet 5 of 109

SSID = CPU

SVC	SVD	Boot Voltage (VCC/GND)	Boot Voltage (open)
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.1
1	1	0.8	0.9

Brazos:
DP1 --> HDMI

Sabine:
DP0 --> LVDS
DP1 --> CRT
DP2 --> HDMI

HDMI

LVDS Panel

APU1B 2 OF 5
ONTARIO-FT1-GP

0809 Change to 1k

0802 Change to H_PROCHOT#

0819

0811 Remove level shifter

0811 AMD Nick change

Thripthrip# add integrated PU 10K

84.T3904.C11
2ND = 84.03904.P11
3rd = 84.03904.L06
MMBT3904-4-GP

CPU exceeds to 125℃

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Title: APU_COntrol&Debug(3/5)

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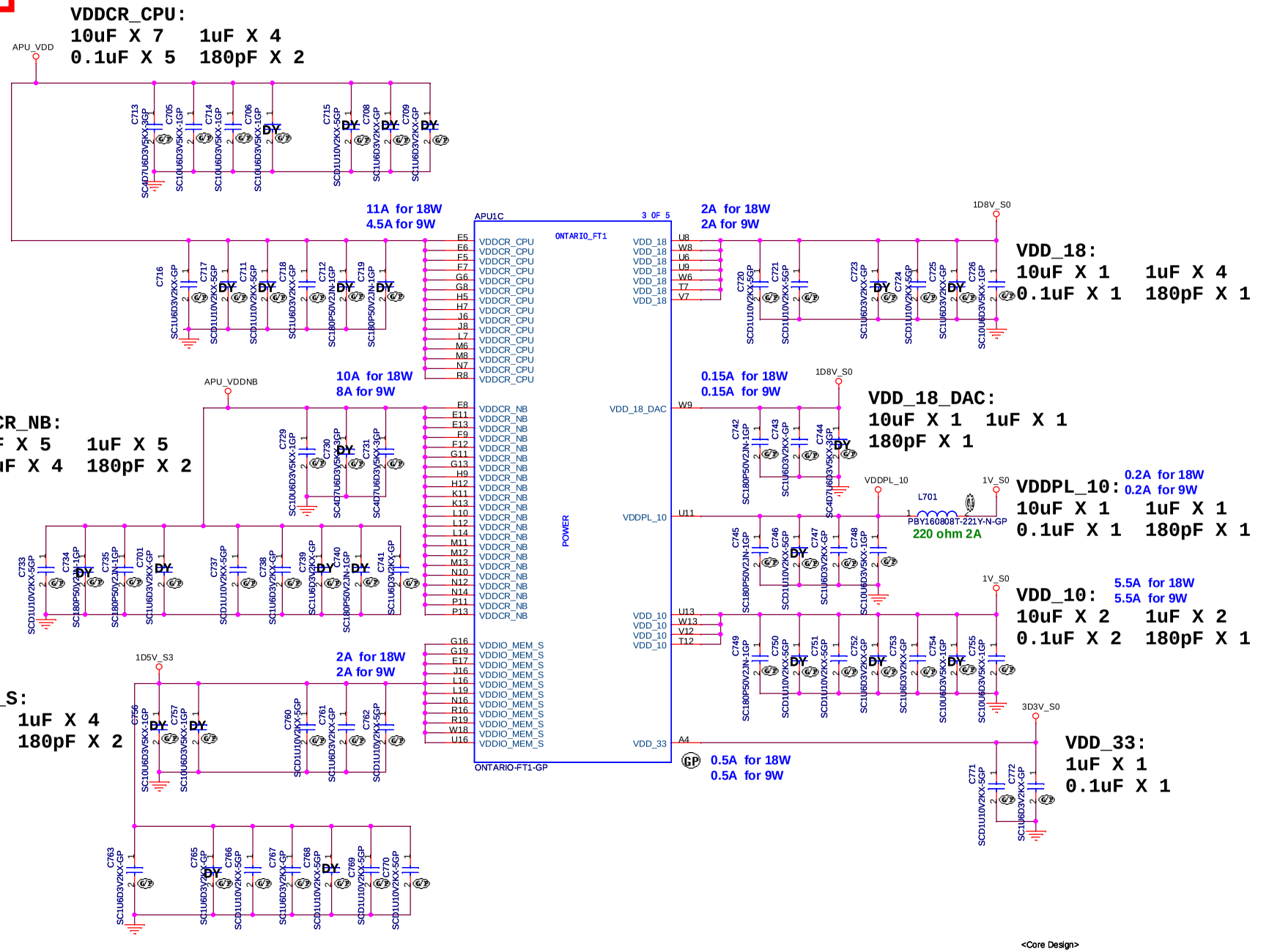
Date: Friday, April 22, 2011 | Sheet 6 of 109

SSID = CPU



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Title: APU_Power(4/5)

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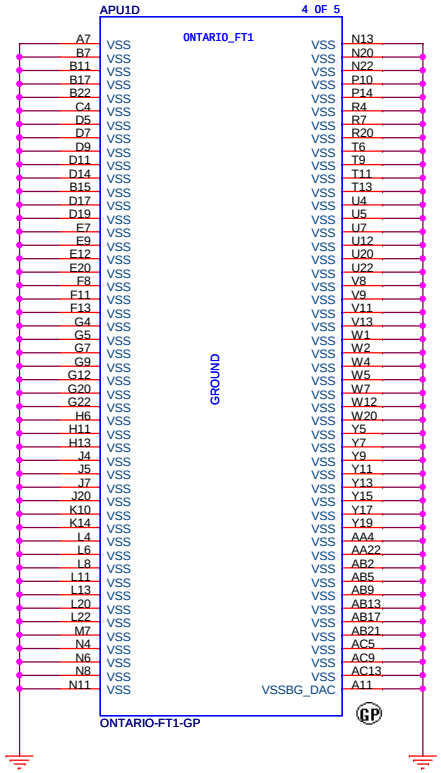
Date: Friday, April 22, 2011 Sheet 7 of 109

SSID = CPU



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Title	APU_VSS(5/5)	
Size: A3	Document Number: Enrico 14 AMD	Rev: A00
Date: Friday, April 22, 2011	Sheet 8 of 109	

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Size: A3	Document Number: Enrico 14 AMD	Rev: A00
Date: Friday, April 22, 2011	Sheet 9 of 109	

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Date: Friday, April 22, 2011 | Sheet 11 of 109

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Size: A3 | Document Number: *Enrico 14 AMD* | Rev: *A00*

Date: Friday, April 22, 2011 | Sheet 12 of 109

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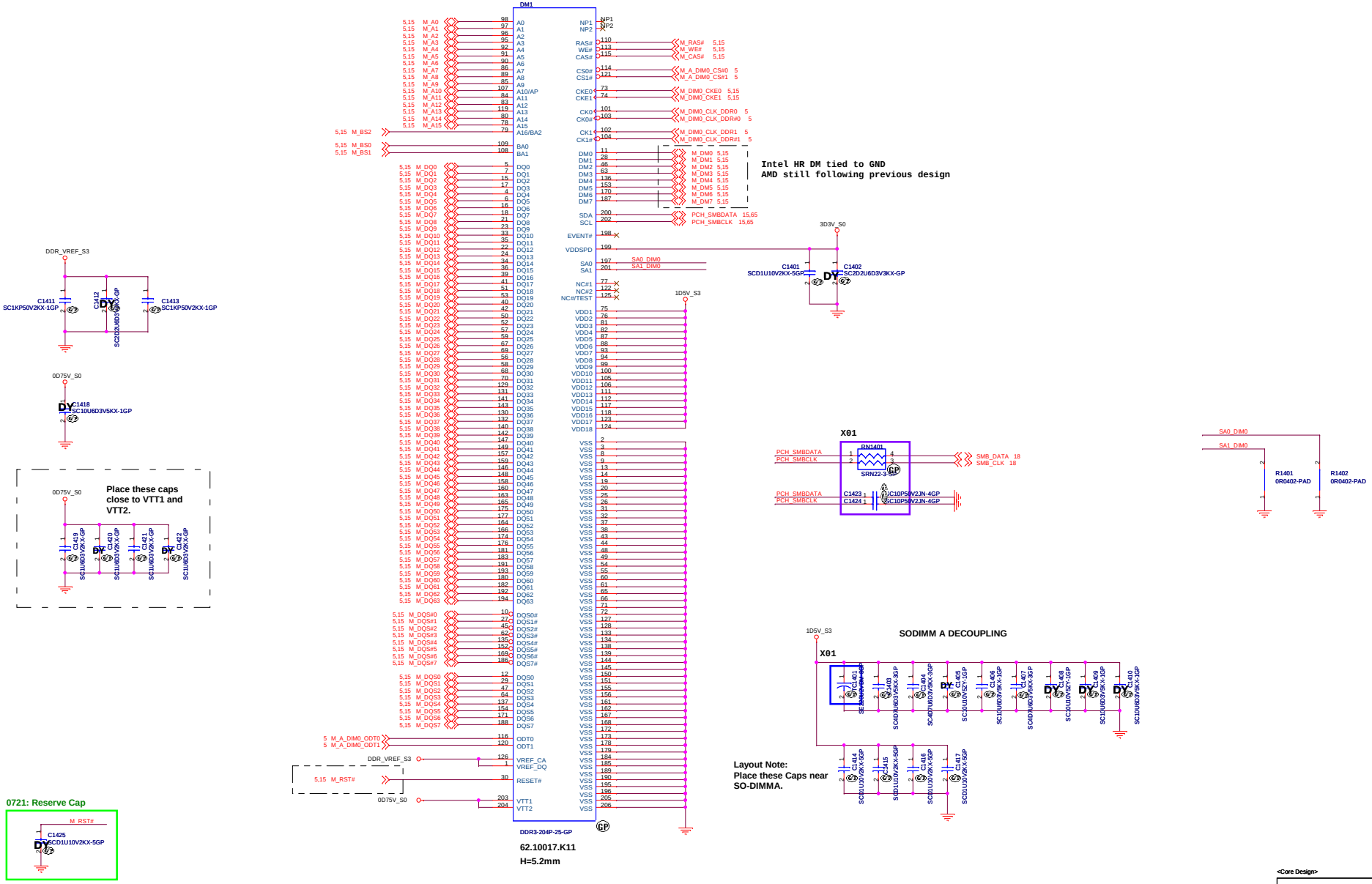
Date: Friday, April 22, 2011 | Sheet 13 of 109

SSID = MEMORY



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Title: DDR3-SODIMM1

Size | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 14 of 109

SSID = MEMORY

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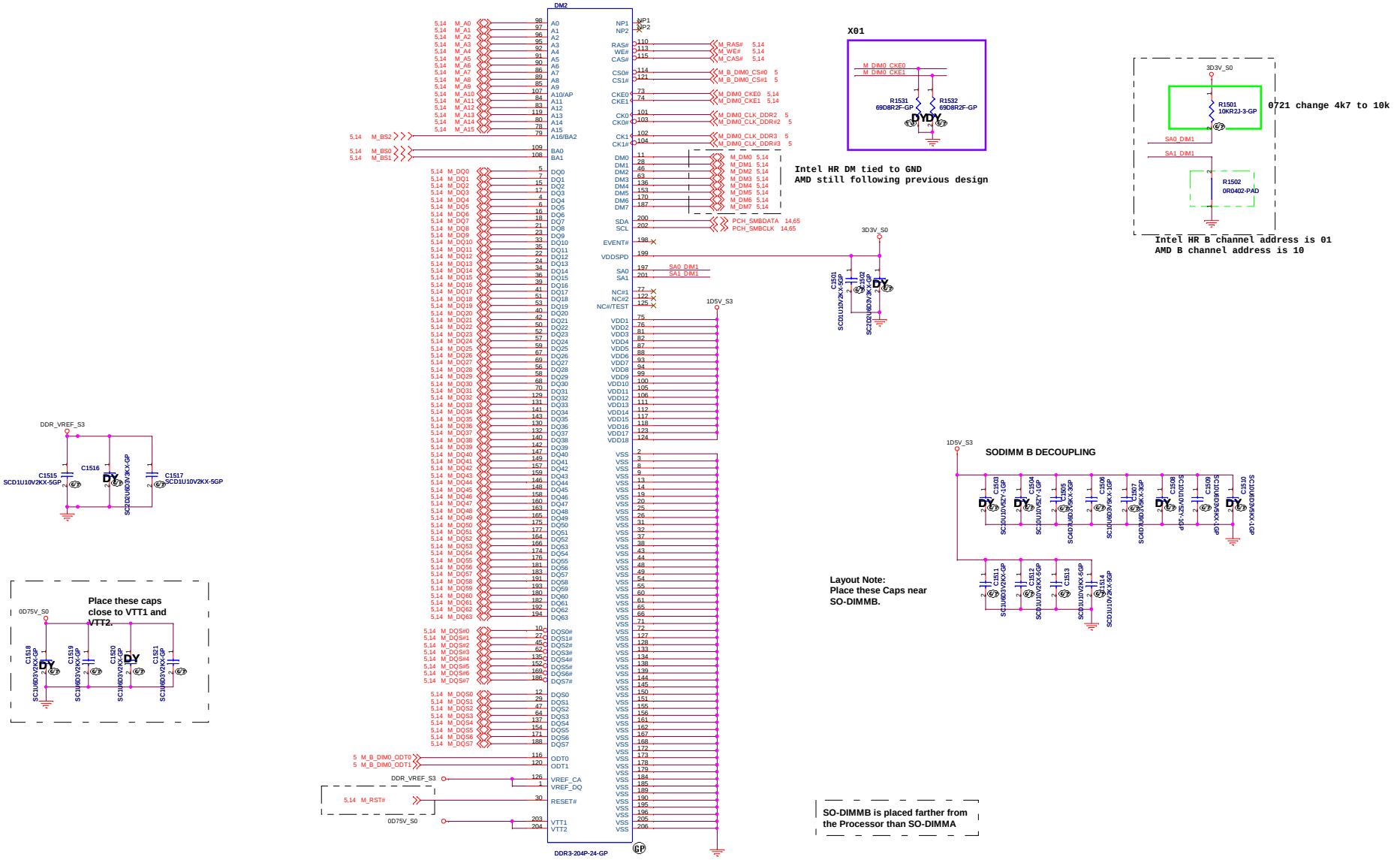

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Title: DDR3-SODIMM2

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Date: Friday, April 22, 2011 | Sheet 15 of 109

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Title
Reserved

Size	Document Number	Rev
A3	***Enrico 14 AMD***	***A00***

Date: Friday, April 22, 2011 Sheet 16 of 109

SSID = FCH

0721 Change CAP 10V to 16V

GPP CLK port	Device	CLKREQ#
0	New Card	0
1	WLAN	1
2	WWAN	2
3	LAN	3
4	X	
5	X	
6	X	
7	X	
8	X	

14M_25M_48M_OSC

connection to devices that will use this clock as a PLL input. The 14-MHz output is intended for use as an auxiliary clock only. The 24Mhz, 25-MHz, 48-MHz, and 50-MHz clock outputs can be used as PLL inputs. Clock output is not available in S3/S5 state, device that need clock in S3/S5 state shouldn t be connected to this clock output. Leave unconnected if not used.

EXT clock_Gen

if LAN support Wake on S5, do not use clock from FCH, have use X'tal

Use 48Mhz CLK For 5138

0811 EMI

33MHZ

0712

KBC

folloiwng Intel HR netname

LDT_STP# connection is just for chipset automation purpose. It is an automatic test for AMD validation team only

0709

Muxless support
PE_GPIO0 ->VGA_RESET
PE_GPIO1 ->VGA_PowerEnable

checklist:No PU Res
Integrated Resistor PU10K

integrated PU

0806

0819

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Title: HUDSON-M1_ACPI/PCI/CLK(1/6)
Size: A2 | Document Number: Enrico 14 AMD | Rev: A00
Date: Friday, April 22, 2011 | Sheet 17 of 109

SSID = FCH

Integrated PU is not supported when the pin is configured for USB over current function.

0720: Change From 2.2K and POP

0720 POP

AMD recommand external PU

Rename 0712

Confirm with SW, RSMRST# from KBC is push-pull. It can be drived high by SW.

Pair	USB Device
0	USB 2.0 EXT.Port1
1	Mini Card1 (WLAN)
2	USB 2.0 EXT.Port1
3	NC
4	NC
5	NC
6	USB 2.0 EXT.Port1
7	CCD Camera
8	NEWCARD
9	Card Reader
10	NC
11	NC
12	NC
13	NC

if not used SMBUS or GPIO ,PD 10K

0719 AMD Confirm

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Title: HUDSON-M2(2/6)

Size: | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 18 of 109

0721 Change CAP to 10n

SSID = FCH

SATA HDD

SATA ODD

56 SATA_TXP0 / 56 SATA_TXN0 → C1901 / C1902 SCD01U16V2KX-3GP → SATA_TXP0_C / SATA_TXN0_C

56 SATA_RXN0_C / 56 SATA_RXP0_C

56 SATA_TXP1 / 56 SATA_TXN1 → C1903 / C1904 SCD01U16V2KX-3GP → SATA_TXP1_C / SATA_TXN1_C

56 SATA_RXN1_C / 56 SATA_RXP1_C

PLACE SATA AC DECOUPLING CAPS CLOSE TO FCH

FCH1B — HUDSON-1 — 2 OF 5

SERIAL ATA

AH9	SATA_TX0P
AJ9	SATA_TX0N
AJ8	SATA_RX0N
AH8	SATA_RX0P
AH10	SATA_TX1P
AJ10	SATA_TX1N
AG10	SATA_RX1N
AF10	SATA_RX1P
AG12	SATA_TX2P
AF12	SATA_TX2N
AJ12	SATA_RX2N
AH12	SATA_RX2P
AH14	SATA_TX3P
AJ14	SATA_TX3N
AG14	SATA_RX3N
AF14	SATA_RX3P
AG17	SATA_TX4P
AF17	SATA_TX4N
AJ17	SATA_RX4N
AH17	SATA_RX4P
AJ18	SATA_TX5P
AH18	SATA_TX5N
AH19	SATA_RX5N
AJ19	SATA_RX5P
AB14	SATA_CALRP
AA14	SATA_CALRN
AD11	SATA_ACT#_GPIO67
AD16	SATA_X1
AC16	SATA_X2

1D1V_SATA_S0 — R1902 / R1903 1KR2F-3-GP → SATA_CALP / SATA_CALN

68 SATA_LED#

[checklist]:integrated Clock Mode=>Left unconnected

GPIOD

AH28	FC_CLK
AG28	FC_FBCLKOUT
AF26	FC_FBCLKIN
AF28	FC_OE#_GPIOD145
AG29	FC_AVD#_GPIOD146
AG26	FC_WE#_GPIOD148
AF27	FC_CE1#_GPIOD149
AE29	FC_CE2#_GPIOD150
AF29	FC_INT1_GPIOD144
AH27	FC_INT2_GPIOD147
AJ27	FC_ADQ0_GPIOD128
AJ26	FC_ADQ1_GPIOD129
AH25	FC_ADQ2_GPIOD130
AH24	FC_ADQ3_GPIOD131
AG23	FC_ADQ4_GPIOD132
AH23	FC_ADQ5_GPIOD133
AJ22	FC_ADQ6_GPIOD134
AG21	FC_ADQ7_GPIOD135
AF21	FC_ADQ8_GPIOD136
AH22	FC_ADQ9_GPIOD137
AJ23	FC_ADQ10_GPIOD138
AF23	FC_ADQ11_GPIOD139
AJ24	FC_ADQ12_GPIOD140
AJ25	FC_ADQ13_GPIOD141
AG25	FC_ADQ14_GPIOD142
AH26	FC_ADQ15_GPIOD143

GPIOD[150:128] are open drain GPIO pins where as GPO160 is an open drain GPO pin. These pins are not programmed to GPIO mode by default.

If use as GPIO, need to pull up to 1.8V_RUN

W5	FANOUT0_GPIO52
W6	FANOUT1_GPIO53
Y9	FANOUT2_GPIO54 → FCH_PROCHOT# C → TP1902
SATA_ODD_PWRGT 56	support ODD Zero power
W7	FANIN0_GPIO56
V9	FANIN1_GPIO57
W8	FANIN2_GPIO58
B6	TEMPIN0_GPIO171 → GPIO171
A6	TEMPIN1_GPIO172 → FCH_USB3.0PORT_EN#
A5	TEMPIN2_GPIO173 → MB_THRMDA_FCH
B5	TEMPIN3_TALERT#_GPIO174 → APU_TALERT# → R1904 0R0402-PAD → APU_ALERT#_FCH 6
C7	TEMP_COMM

HW MONITOR

A3	VIN0_GPIO175 → PSW_CLR#
B4	VIN1_GPIO176 → VRAM_SIZE1
A4	VIN2_GPIO177 → VRAM_SIZE2
C5	VIN3_GPIO178 → MEM_1V5
A7	VIN4_GPIO179 → MEM_1V35
B7	VIN5_GPIO180 → VIN_VDDIO
B8	VIN6_GBE_STAT3_GPIO181 → VIN_VDDR
A8	VIN7_GBE_LED3_GPIO182 → GPIO182

SPI ROM

J5	SPI_DI_GPIO164 → FCH_SPI_DI → TPAD14-GP TP621
E2	SPI_DO_GPIO163 → FCH_SPI_SI → TPAD14-GP TP620
K4	SPI_CLK_GPIO162 → FCH_SPI_CLK → TPAD14-GP TP619
K9	SPI_CS1#_GPIO165 → FCH_SPI_CS0# → TPAD14-GP TP618
G2	ROM_RST#_GPIO161 → FCH_SPI_WP# → TPAD14-GP TP617

HUDSON-M1-1-GP

G27	NC#G27
Y2	NC#Y2

VDDIO	MEM_1V5	MEM_1V35
1.5V	H	Don't Care
1.35V	L	H

XTAL
1'nd 82.30020.851
2'nd 82.30020.791

RN1902: 1 GPIO171, 2 FCH_USB3.0PORT_EN#, 3 MEM_1V5, 4 MB_THRMDA_FCH — SRN10KJ-8-GP

RN1901: 1 VIN_VDDR, 2 GPIO182, 3 VIN_VDDIO, 4 MEM_1V35 — SRN10KJ-8-GP

if not used HWM or GPIO ,PD 10K

R1911 10KR2J-3-GP → PSW_CLR#

3D3V_S5 — R1908 2G (10KR2J-3-GP) → VRAM_SIZE1 / VRAM_SIZE2 — R1909 / R1910 10KR2J-3-GP → 512M

[VRAM_SIZE1:VRAM_SIZE2]
LL=512M / HL=1G / LH=2G

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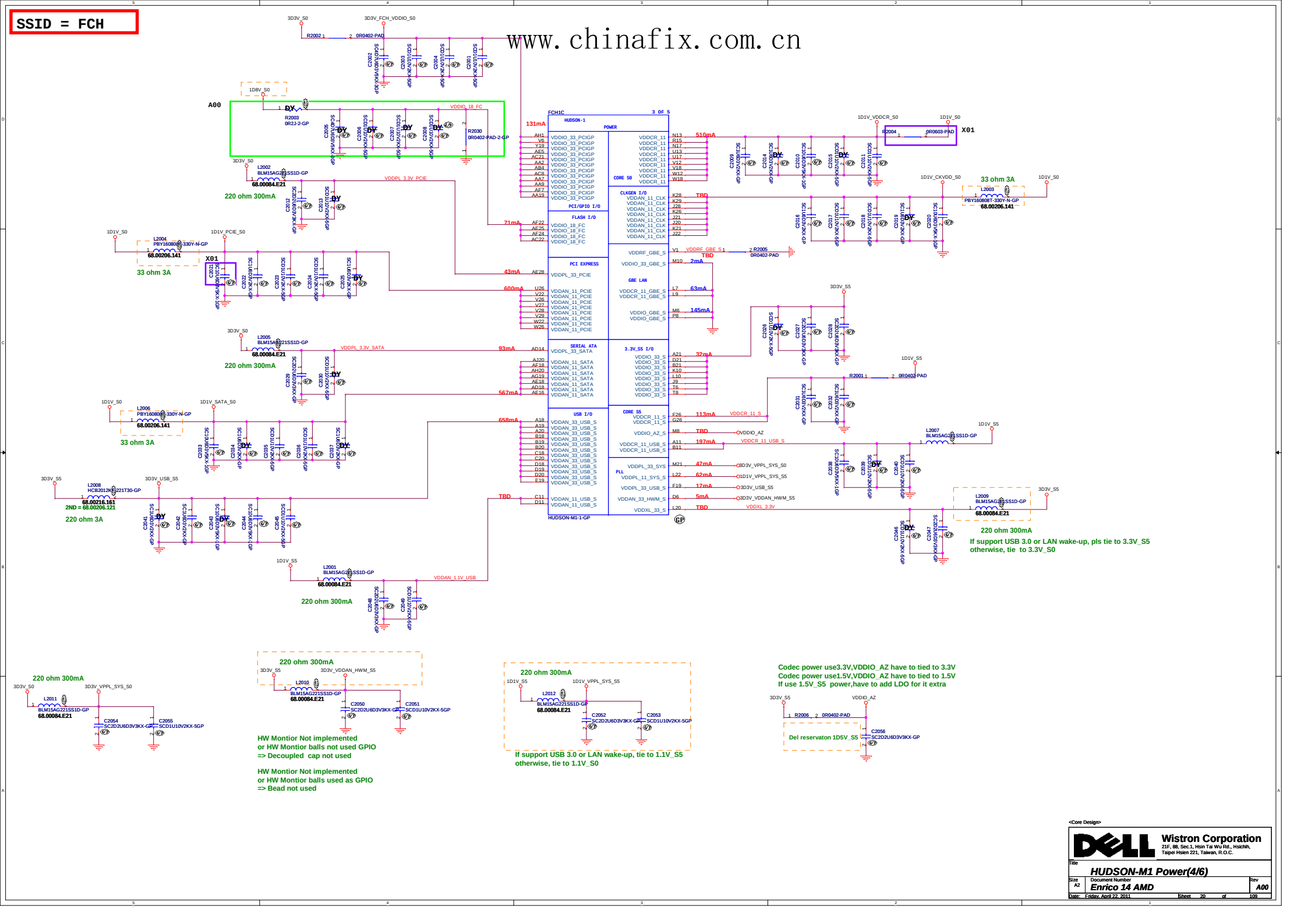
Title: HUDSON-M1 SATA/HWM/SPI(3/6)

Size | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 19 of 109

SSID = FCH



<Core Design>

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Title: HUDSON-M1 Power(4/6)

Size	Document Number	Rev
A2	Enrico 14 AMD	A00

Date: Friday, April 22, 2011 Sheet 20 of 109

SSID = FCH

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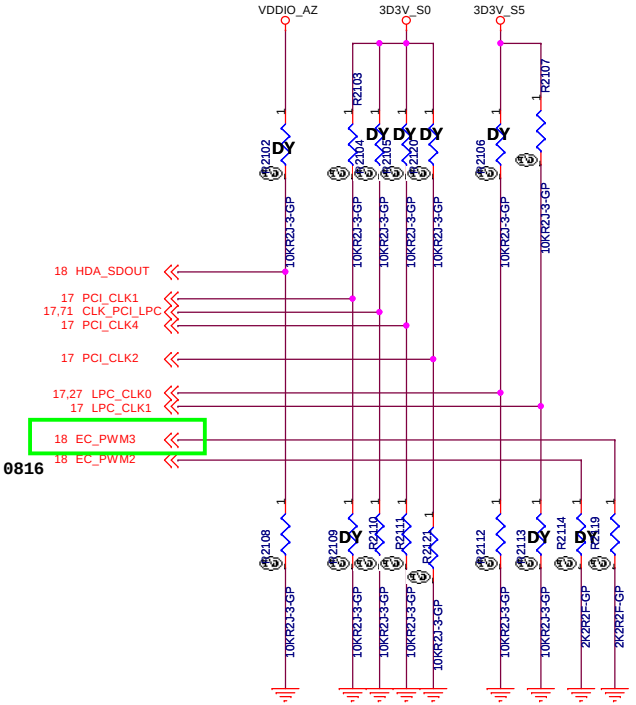
REQUIRED STRAPS



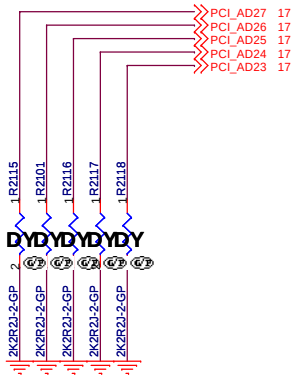
REQUIRED SYSTEM STRAPS

	AZ_SDOUT	PCI_CLK1	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1	LPC_CLK2
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT	Enable boot timer function
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)	Disable boot fail timer function DEFAULT

TYPE ENABLED	EC_PWM2	EC_PWM3
Reserved	2.2-kohm 5% pull-down	2.2-kohm 5% pull-down
LPC ROM	Not connected.	2.2-kohm 5% pull-down
SPI ROM	2.2-kohm 5% pull-down	Not connected.
Reserved	Not connected.	Not connected.

Note: EC_PWM2, EC_PWM3 default have internal 10kohm PU.

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: FCH has 15K internal PU FOR PCI_AD[27:23]

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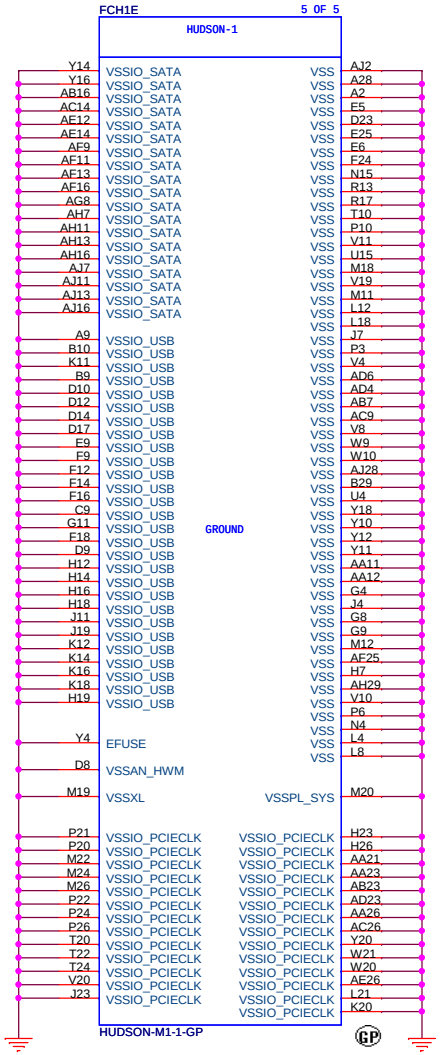
Title	HUDSON_STRAPPING_(5/6)	
Size A3	Document Number Enrico 14 AMD	Rev A00
Date: Friday, April 22, 2011	Sheet 21 of 109	

SSID = FCH



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Title: *Reserved*

Size	Document Number	Rev
A3	*Enrico 14 AMD*	*A00*

Date: Friday, April 22, 2011 Sheet 22 of 109

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Title: *Reserved*

Size	Document Number	Rev
A3	*Enrico 14 AMD*	*A00*

Date: Friday, April 22, 2011 Sheet 23 of 109

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Title: *Reserved*

Size: A3 | Document Number: *Enrico 14 AMD* | Rev: *A00*

Date: Friday, April 22, 2011 | Sheet 24 of 109

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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Enrico 14 AMD* | Rev: *A00*

Date: Friday, April 22, 2011 | Sheet 25 of 109

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Title: *Reserved*

Size: A3 | Document Number: *Enrico 14 AMD* | Rev: *A00*

Date: Friday, April 22, 2011 | Sheet 26 of 109

SSID = KBC

PCB VERSION ADC(PIN8)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
A00	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
DV14_DIS	100.0K	10.0K	3.0V
Reserved	100.0K	20.0K	2.75V
DV15_UMA	100.0K	33.0K	2.48V
Reserved	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

NOTE:
Locate resistors R2719 and R2722 close to the NPCE791L.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

EC_GPIO47 High Active

PSL SOLUTION

10mW SOLUTION

VBACKUP

PSL_IN1

PSL_OUT

EC GPIO standard PH/PL

0729 Add from page94 to here

0804 Add short pad separate

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE795PA0DX

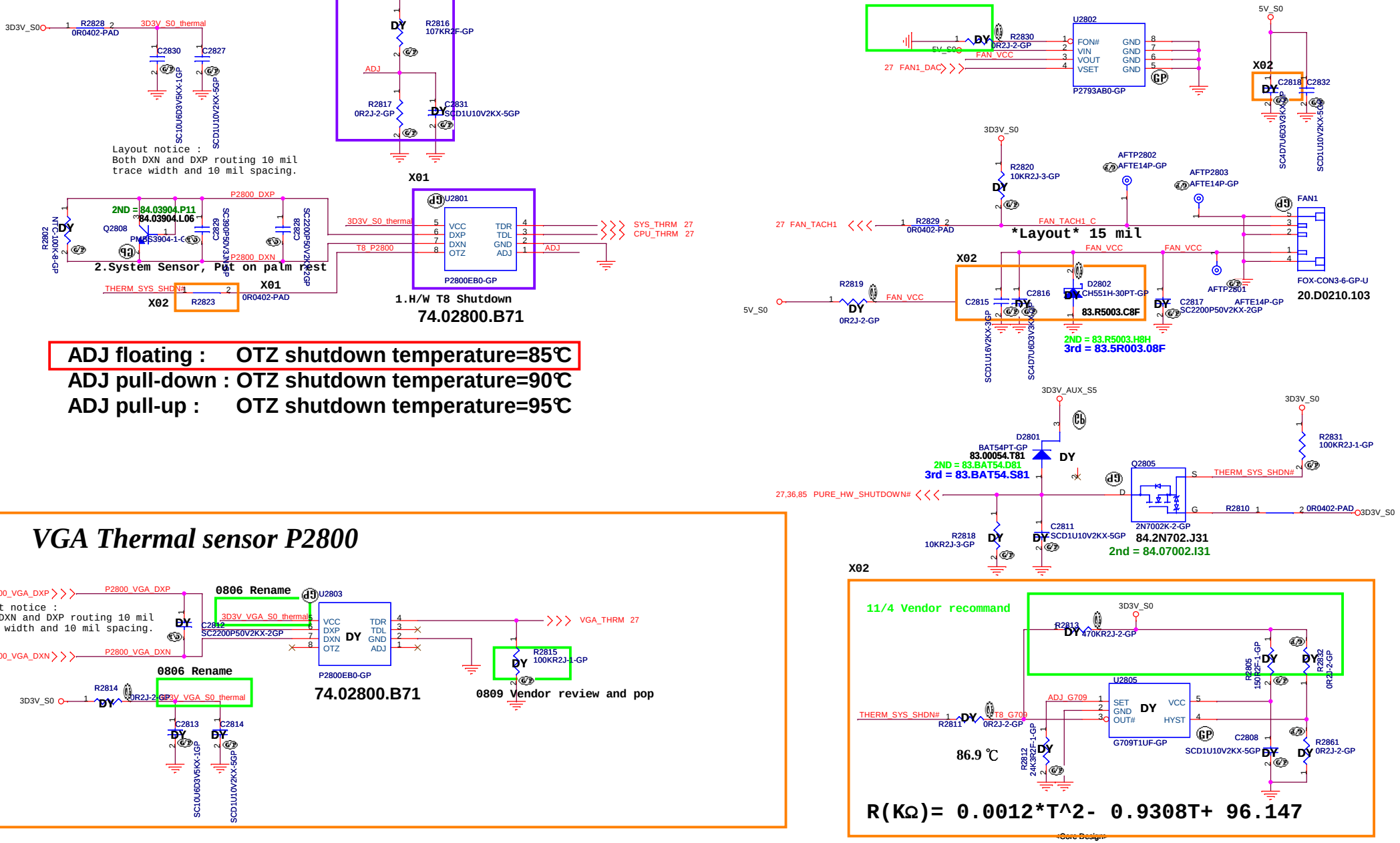
Size: A2 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 27 of 109

SSID = Thermal

Fan controller P2793

0721 Pull-down: full speed, R2830 dummy.



ADJ floating : OTZ shutdown temperature=85℃
ADJ pull-down : OTZ shutdown temperature=90℃
ADJ pull-up : OTZ shutdown temperature=95℃

X02

VGA Thermal sensor P2800

X02

11/4 Vendor recommand

R(KΩ)= 0.0012*T^2- 0.9308T+ 96.147

Wistron Corporation
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Title: Thermal/Fan Controllor EMC2102
Size: A3 | Document Number: Enrico 14 AMD | Rev: A00
Date: Friday, April 22, 2011 | Sheet 28 of 109

SSID = AUDIO

U2901 71.92H87.A03 92HD87B1A5NDGXTBX8-GP

0625 Modify:
AUD_DMIC_CLK&AUD_DMIC_IN0 connector to LVDS pin define.

0707 Modify:
updated U2901 part number from data base.

2010/06/30 Change to 92HD87 (71.92H87.A03)

Close to codec

CLOSE TO CODEC

Put C2921 and C2922 close to codec

0809 Vendor recommand

0730 Add internal MIC

From SB

From EC

AUD_PC_BEEP
Trace width>15 mils

0707 Modify:
Change R2911,R2914,R2917 change to 0ohm 0603 from short pad.

MIC IN

0719 Modify:
Move RN2901 to closed AUDIO CODEC from speaker connector.

Azalia I/F EMI

Close to Pin13

Close to Pin14

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Title: Audio Codec 92HD87B1

Size	Document Number	Rev
A3	Enrico 14 AMD	A00

Date: Friday, April 22, 2011 Sheet 29 of 109

<Core Design>

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Title: AMP		
Size: A3	Document Number: Enrico 14 AMD	Rev: A00
Date: Friday, April 22, 2011	Sheet 30 of 109	

SSID = LOM

LAN CHIP

11/18 change L3101 to slime type

60 mils X01

L3101 IND-4D7UH-192-GP

LANOUP_1.05S CTR_L10A_R

0721

EVDD10 R3117 0R0603-PAD C3106 SC1U10V3ZY-6GP

R3115 0R0603-PAD DVDD10

C3120 C3115 SC4D7U6D3V3KX-GP X5R

C3113 C3109 C3114 C3117 SCD1U16V2ZY-2GP

40 mils

3D3V_LAN_S5 C3118 C3121 C3119 SCD1U16V2ZY-2GP

R3104 0R0603-PAD AVDD33_REG

C3101 C3111 SC4D7U6D3V3KX-GP SCD1U10V2ZY-2GP X5R

U3101 RTL8105E-VC-GR-LF-GP

R3113 2K49R2F-GP

3D3V_LAN_S5 DVDD10 LANXOUT LANXIN GPO

AVDD33 AVDD33 RSET AVDD10 CKXTAL2 CKXTAL1 AVDD33 NC#41 LED0 DVDD3 GPO LED1/EESK

GND

59 LAN_MDI0P 59 LAN_MDI0N MDIP0 MDIN0 AVDD10

59 LAN_MDI1P 59 LAN_MDI1N MDIP1 MDIN1

DVDD10 NC#6 NC#7 NC#8 NC#9 NC#10 NC#11 NC#12

3D3V_LAN_S5

REGOUT VDDREG VDDREG ENSWREG EEDI LED3/EEDO EECS DVDD10 LANWAKE# DVDD33 ISOLATE# PERST#

LANOUP_1.05S AVDD33_REG AVDD33_REG ENSWREG EEDI/SDA

R3107 10KR2J-3-GP DVDD10

PCIE_WAKE# 18,27

3D3V_LAN_S5 ISOLATE#

PLT_RST# LAN X02

R3110 1KR2J-1-GP

R3109 15KR2F-GP

3D3V_S0

DVDD10 NC#14 NC#15 CLKREQ# HSIP HSIN REFCLK_P REFCLK_N EVDD10 HSOP HSON GND

TPAD14-GP TP3101 DVDD10

0720

CLK_LAN_REQ# R

PCIE_TXP0

PCIE_TXN0

CLK_PCIE_LAN

CLK_PCIE_LAN#

EVDD10

PCIE_RXP0_C

PCIE_RXN0_C

C3131 SCD1U10V2KX-4GP

For Switch Regulator enable

3D3V_LAN_S5 R3105 0R0402-PAD R3106 0R2J-2-GP DY

X01

3D3V_S0 R3102 10KR2J-3-GP DY

3D3V_LAN_S5 R3101 10KR2J-3-GP DY

CLK_LAN_REQ# EN

Q3101 PMBS3904-1-GP

84.03904.L06

2ND = 84.03904.P11

CLK_LAN_REQ# R

PCIE_CLK_LAN_RQ1# 18

R3133 0R2J-2-GP DY

X01

3D3V_LAN_S5 PCIE_WAKE# 10KR2J-3-GP DY R3122

X01

X02

LANXOUT C3102 SC18P50V2JN-1-GP

X3101 XTAL-25MHZ-155-GP

LANXIN C3103 SC18P50V2JN-1-GP

C3105 SCD1U10V2KX-5GP

PCIE_RXP0_C PCIE_RXN0_C C3104 SCD1U10V2KX-5GP

PCIE_RXP0 17 PCIE_RXN0 17

PCIE_TXP0 PCIE_TXN0

PCIE_TXP0 17 PCIE_TXN0 17

CLK_PCIE_LAN 17 CLK_PCIE_LAN# 17

3D3V_S0 R3119 0R3J-0-U-GP DY

3D3V_LAN_S5

R3120 0R3J-0-U-GP DY

3D3V_S5 C3130 SCD1U10V2KX-4GP

PA102FMG-GP-U Q3103

main: 84.00102.031

2nd: 84.03403.031

R3121 10KR2J-3-GP X02 C3125 SC1U10V2KX-1GP

C3129 SCD1U10V2KX-4GP C3128 SCD1U10V2KX-4GP

R3118 1KR2J-1-GP PM_LAN_ENABLE_R

LAN_ENABLE_R_C

27 PM_LAN_ENABLE

Q3102 2N7002K-2-GP

X02 R3134 100KR2J-1-GP

X02

3D3V_LAN_S5

RN3101 SRN10KJ-5-GP

Q3104 PMBS3904-1-GP

17,65,71,83 PLT_RST#

PLT_RST# LAN

R3108 0R2J-2-GP DY

X01

RTL8111E-Stuff

RTL8105E-DY

3D3V_LAN_S5 R3103 1KR2J-1-GP DY GPO

R3114 10KR2J-3-GP EEDI/SDA

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Title: LOM

Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 31 of 109

SSID = SDIO

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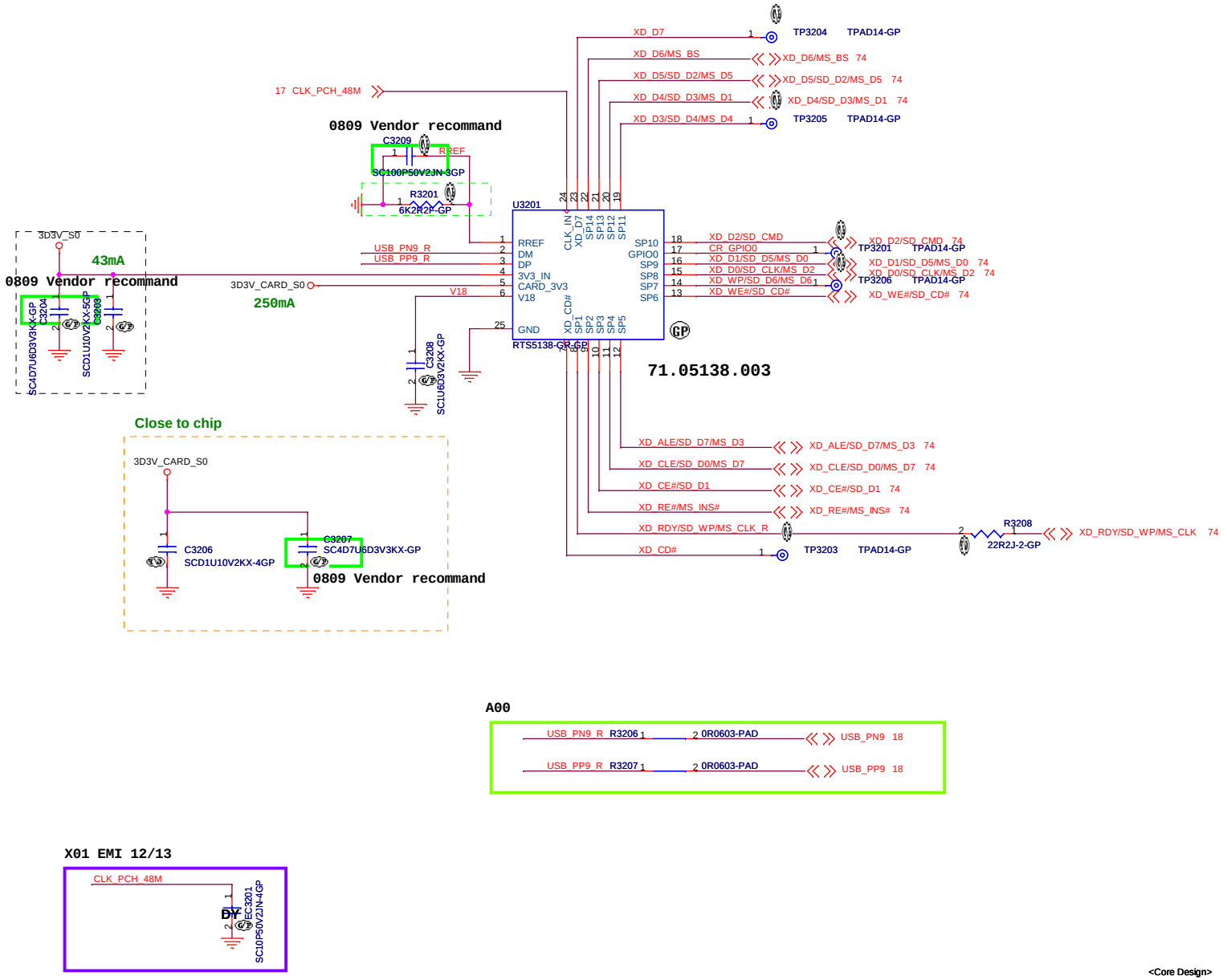

A00

X01 EMI 12/13

<Core Design>

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Title: *Reserved*

Size	Document Number	Rev
A3	*Enrico 14 AMD*	*A00*

Date: Friday, April 22, 2011 Sheet 32 of 109

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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Enrico 14 AMD* | Rev: *A00*

Date: Friday, April 22, 2011 | Sheet 33 of 109

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<Core Design>

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Size: A3 | Document Number: *Enrico 14 AMD* | Rev: *A00*

Date: Friday, April 22, 2011 | Sheet 34 of 109

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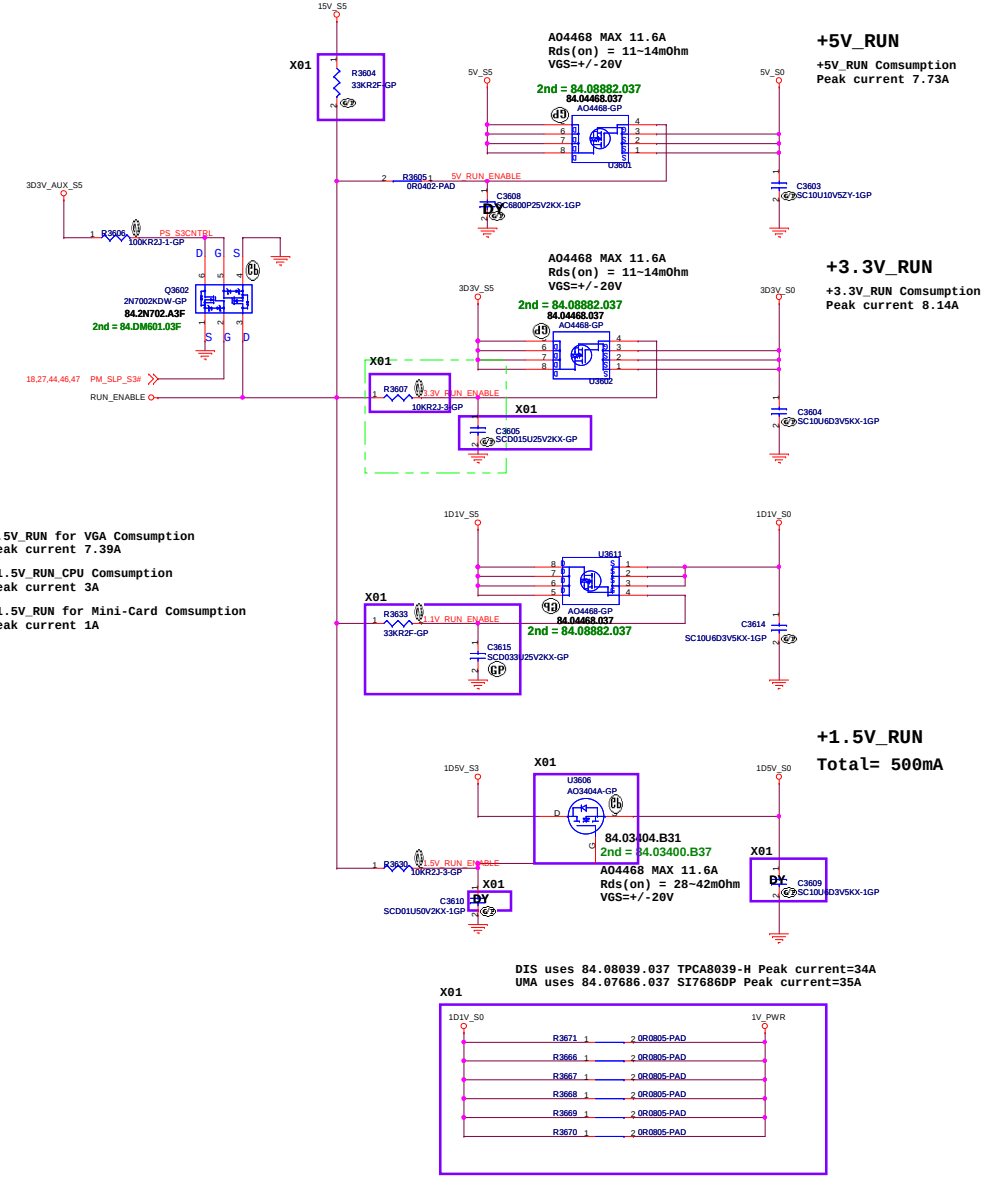
Title: *Reserved*

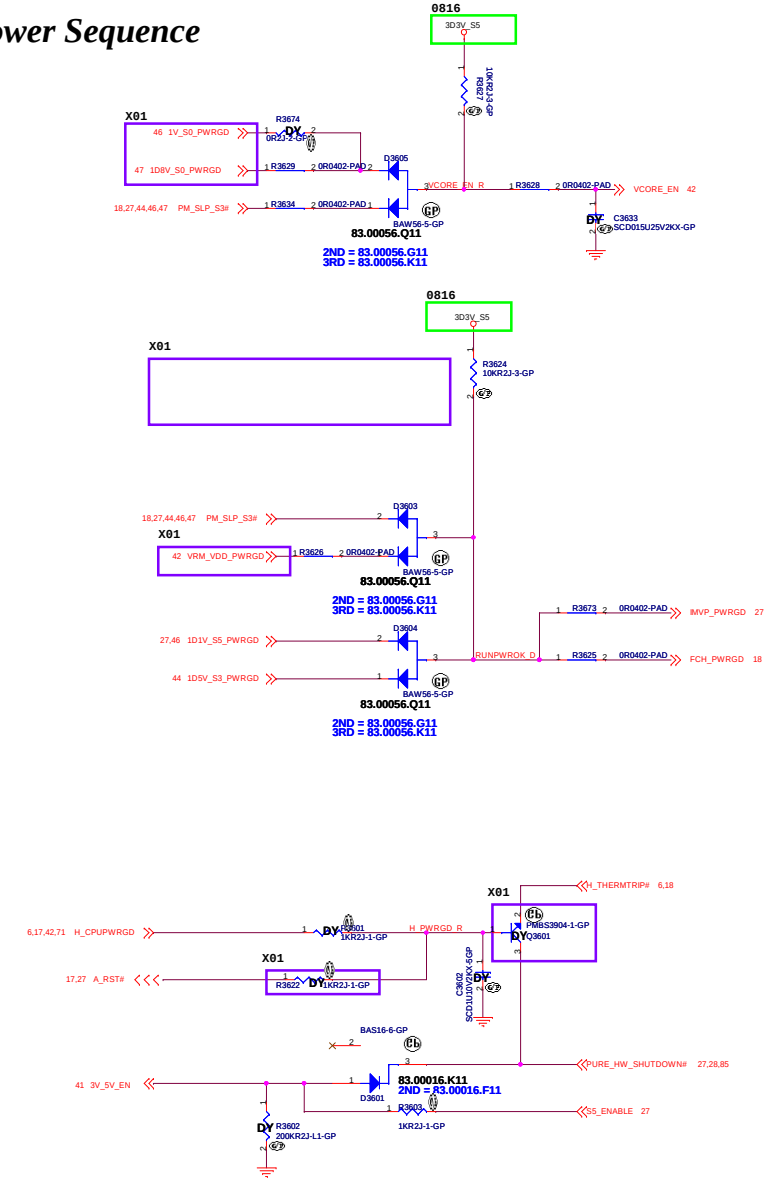
Size: A3 | Document Number: *Enrico 14 AMD* | Rev: *A00*

Date: Friday, April 22, 2011 | Sheet 35 of 109

ROSA Run Power



Power Sequence



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Power On Logic

Size: A2 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 36 of 109

<Core Design>

Wistron Corporation
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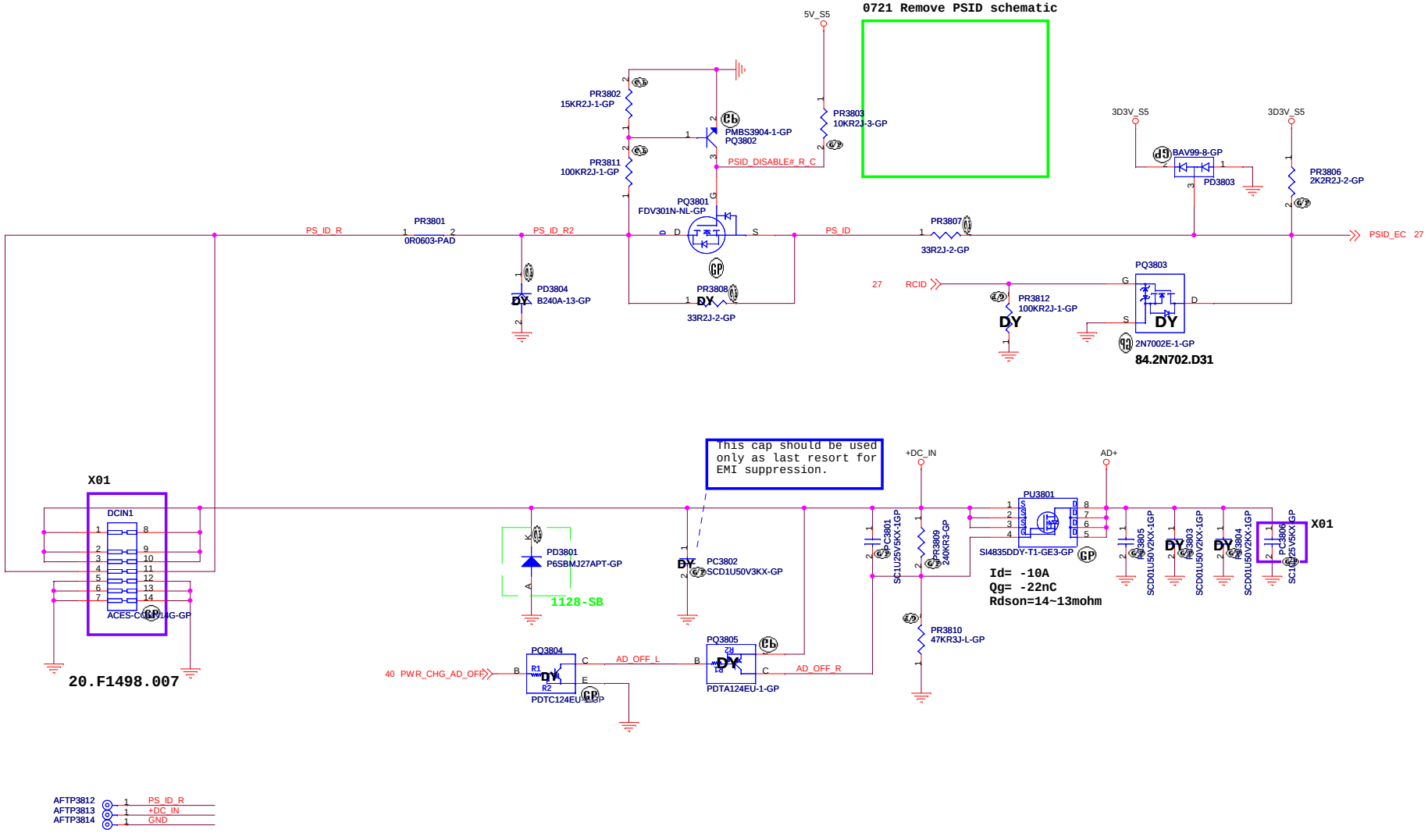
Title: Power Plane Enable

Size	Document Number	Rev
A3	Enrico 14 AMD	A00

Date: Friday, April 22, 2011 Sheet 37 of 109

SSID = PWR.Support

DCin CONN



<Core Design>

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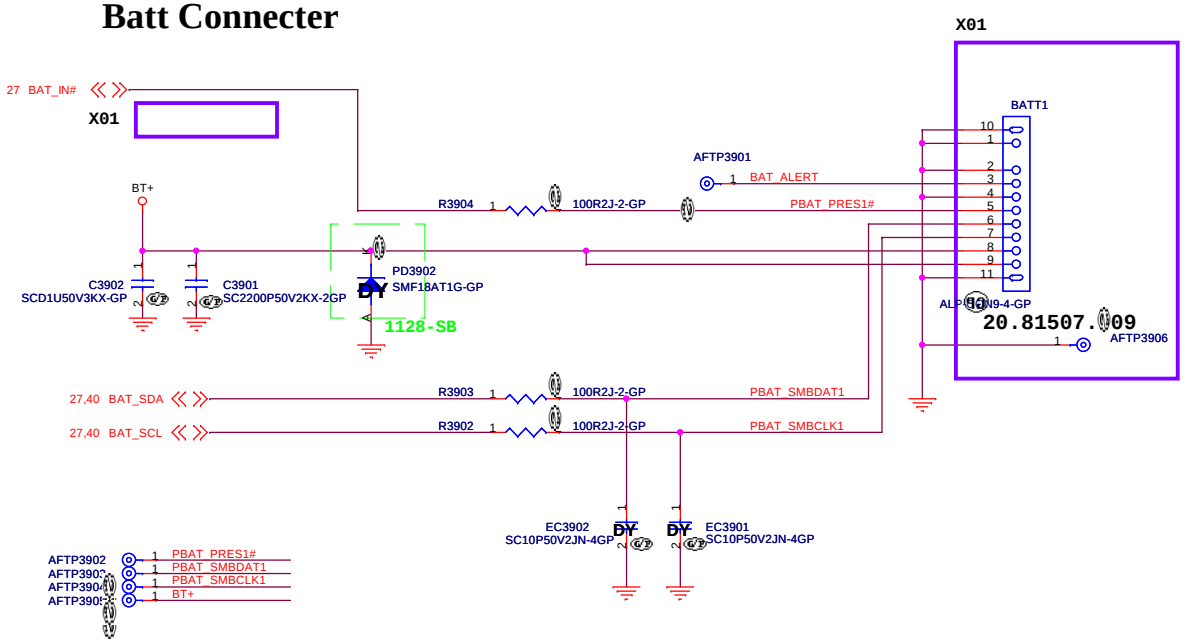
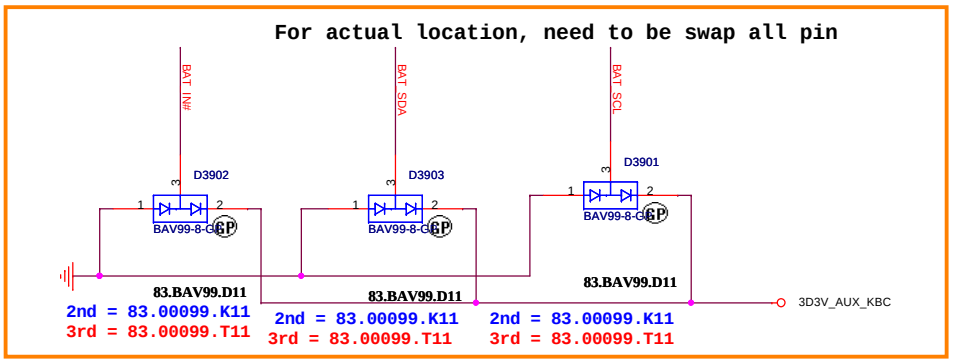
Title	DCIN JACK	
Size: Custom	Document Number: Enrico 14 AMD	Rev: A00
Date: Friday, April 22, 2011	Sheet 38 of 109	

SSID = BATT CONN

Batt Connecter



Close to Batt Connector



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Title	BATT CONN	
Size A3	Document Number: Enrico 14 AMD	Rev: A00
Date: Friday, April 22, 2011	Sheet 39 of 109	

SSID = Charger

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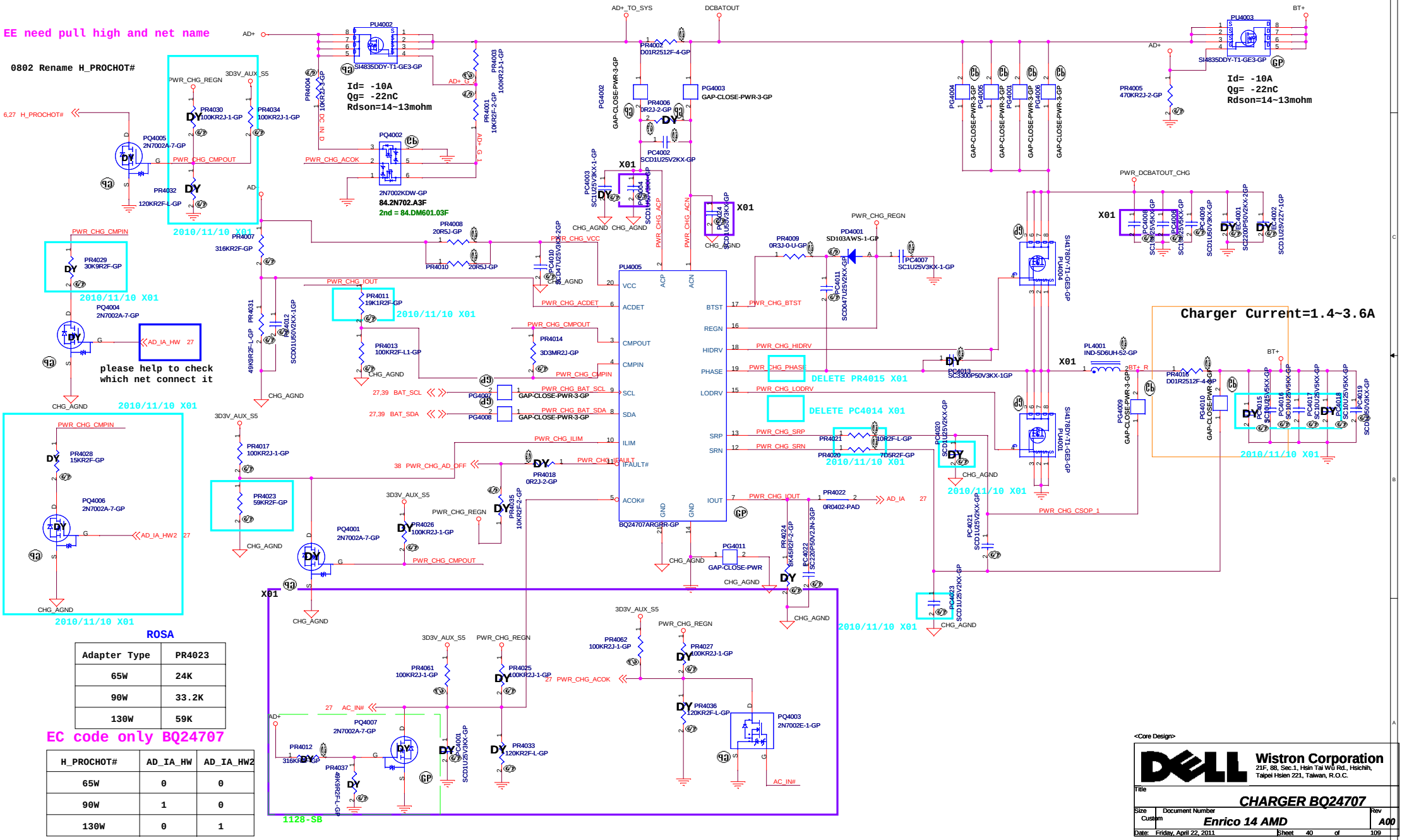

ROSA

Adapter Type	PR4023
65W	24K
90W	33.2K
130W	59K

EC code only BQ24707

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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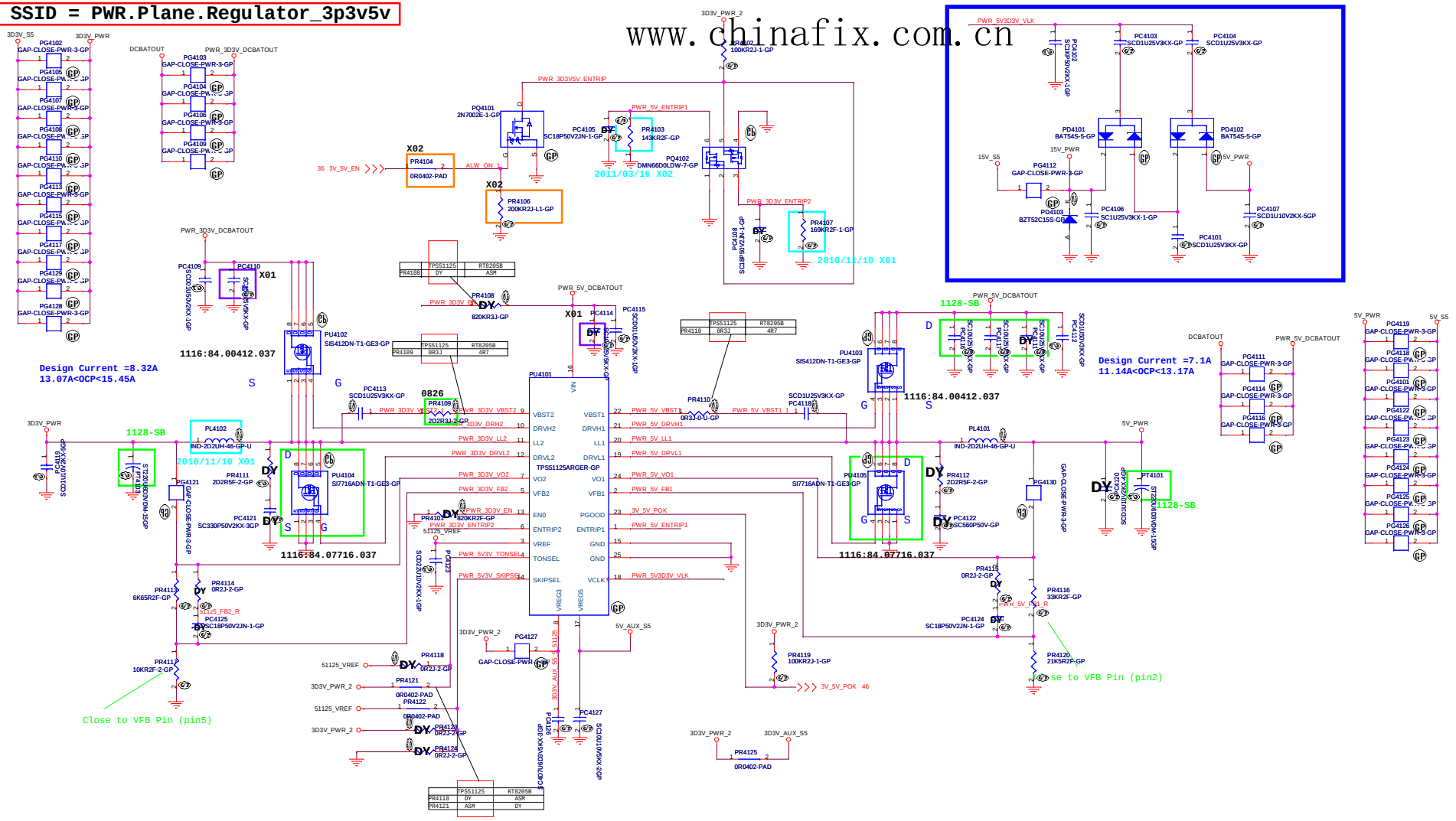
Title: CHARGER BQ24707

Size: Custom | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 40 of 109

SSID = PWR.Plane.Regulator_3p3v5v



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: TPC8061-H / 21mohm/30mOhm@4.5Vgs/ 84.08061.037
L/S: TPCA8065-H / 12mohm/15mOhm@4.5Vgs/ 84.08065.037

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

TPS51125:

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

RT8205B:

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
H/S: TPC8061-H / 21mohm/30mOhm@4.5Vgs/ 84.08061.037
L/S: TPCA8065-H / 12mohm/15mOhm@4.5Vgs/ 84.08065.037

<Core Design>

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Title: TPS51125_5V/3D3V

Size	Document Number	Rev
A2	Enrico 14 AMD	A00

Date: Friday, April 22, 2011 Sheet 41 of 109

SSID = PWR.Plane.CORE.REG

Pleae help to check the net whether can change to 3D3V_S5

2010/11/10 X01

Peak Current=11
Design Current =7.7A
16.5A<OCP<18.7A

PR4208 close to PL4201

Close to CPU socket

Parallel

Close to CPU socket

Parts close to PWM IC

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1uH PCMC063T-1R0MN Cyntec 9mohm/10mohm Isat =22Arms 68.1R01A.20B
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/79.33719.L01
O/P cap: 330U 2V EEFSX0D331XE 6mOhm 3,5Arms Panasonic/79.33719.20L
H/S: SIR712DP/ POWERPAK/10.3mOhm/12.4mOhm@4.5Vgs/ 84.00172.037
L/S: SiR460DP/ POWERPAK/ 4.9mOhm/ 6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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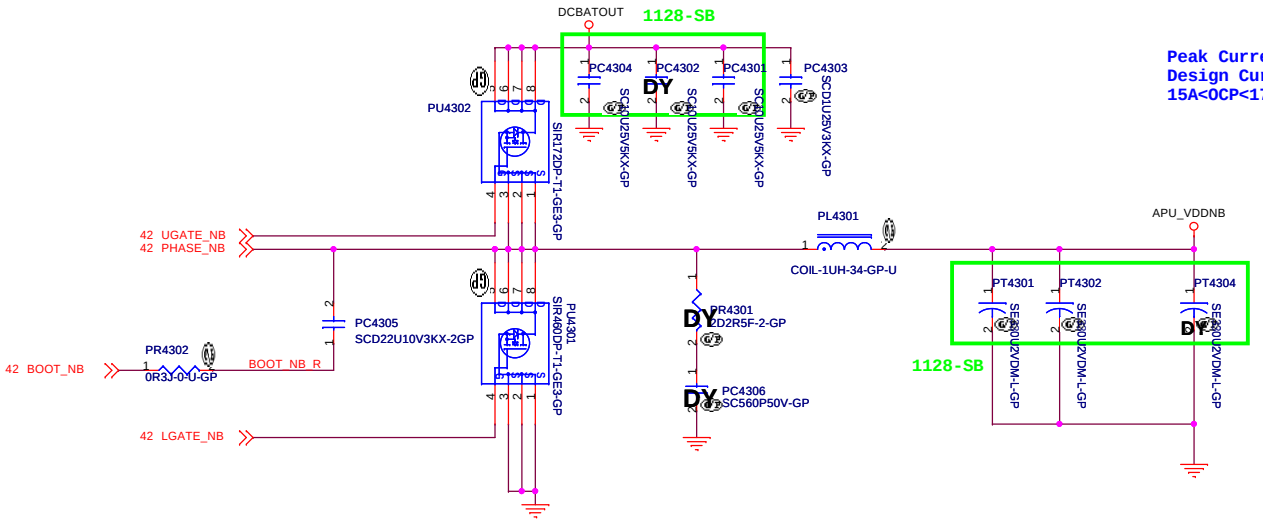
Title: VREG : +VCC_CORE&+VDDNB

Size	Document Number	Rev
A3	Enrico 14 AMD	A00

Date: Friday, April 22, 2011 Sheet 42 of 109

SSID = PWR.Plane.VDDNB.REG



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1uH PCMC063T-1R0MN Cyntec 9mohm/10mohm Isat =22Arms 68.1R01A.20B
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/79.33719.L01
H/S: SIR712DP/ POWERPAK/10.3mOhm/12.4mOhm@4.5Vgs/ 84.00172.037
L/S: SiR460DP/ POWERPAK/ 4.9mOhm/ 6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

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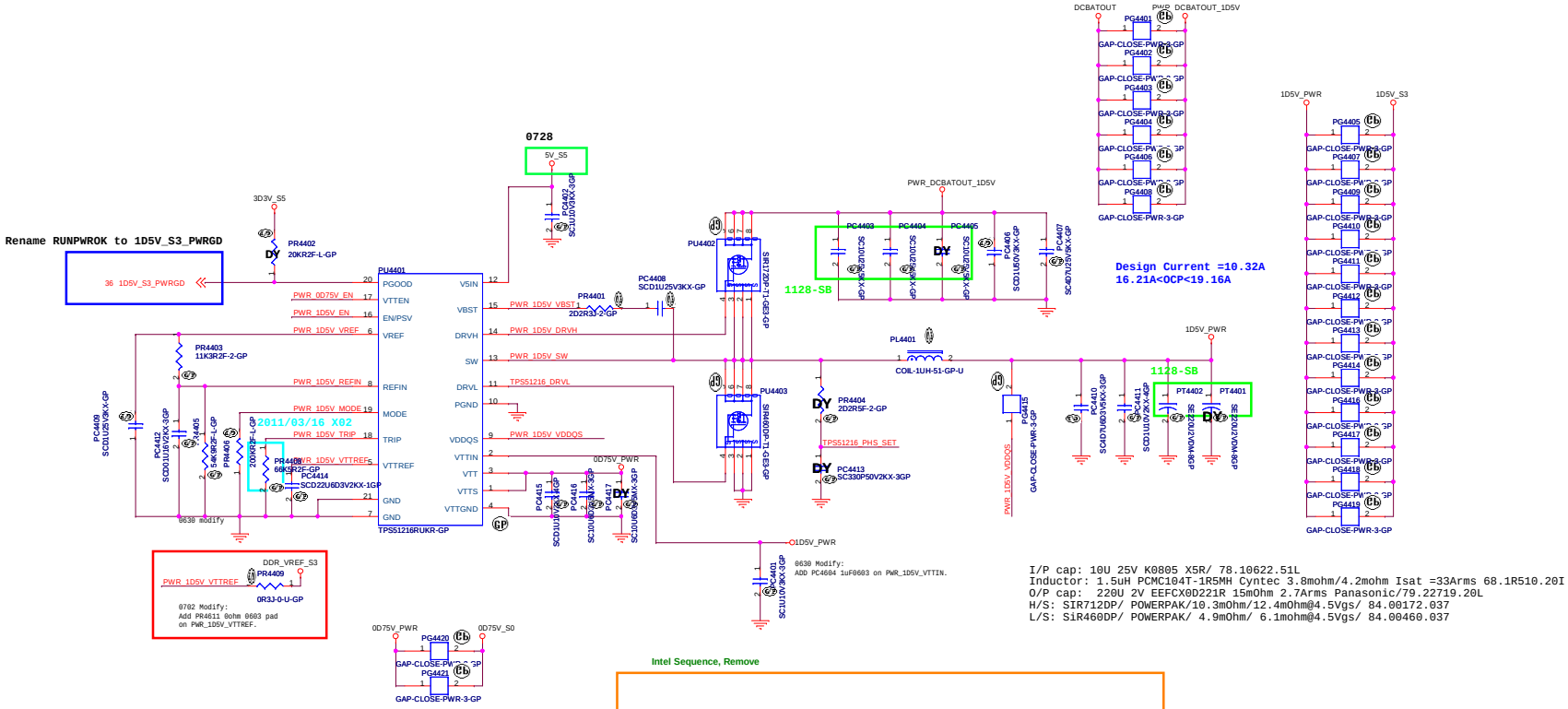
Title: TPS51218 VDDNB
Size: A3
Document Number: Enrico 14 AMD
Rev: A00
Date: Friday, April 22, 2011
Sheet 43 of 109

SSID = PWR.Plane.Regulator_1p5v0p75v



Design Current =10.32A
16.21A<OCP<19.16A

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.5uH PCMC104T-1R5MH Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.20I
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms Panasonic/79.22719.20L
H/S: SIR712DP/ POWERPAK/10.3mOhm/12.4mOhm@4.5Vgs/ 84.00172.037
L/S: SiR460DP/ POWERPAK/ 4.9mOhm/ 6.1mohm@4.5Vgs/ 84.00460.037

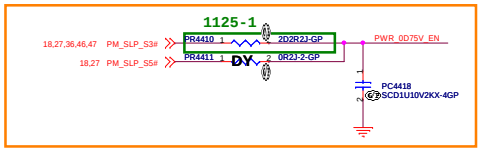
State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

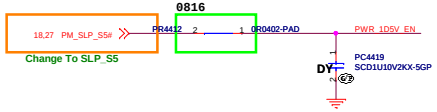
MODE

PR4406	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

Intel Sequence, Remove

Add For Sequence





<Core Design>

Wistron Corporation
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Title: RT8207_1D5V_S3
Size: Custom | Document Number: Enrico 14 AMD | Rev: A00
Date: Friday, April 22, 2011 | Sheet 44 of 109

(Blanking)

<Core Design>

Wistron Corporation
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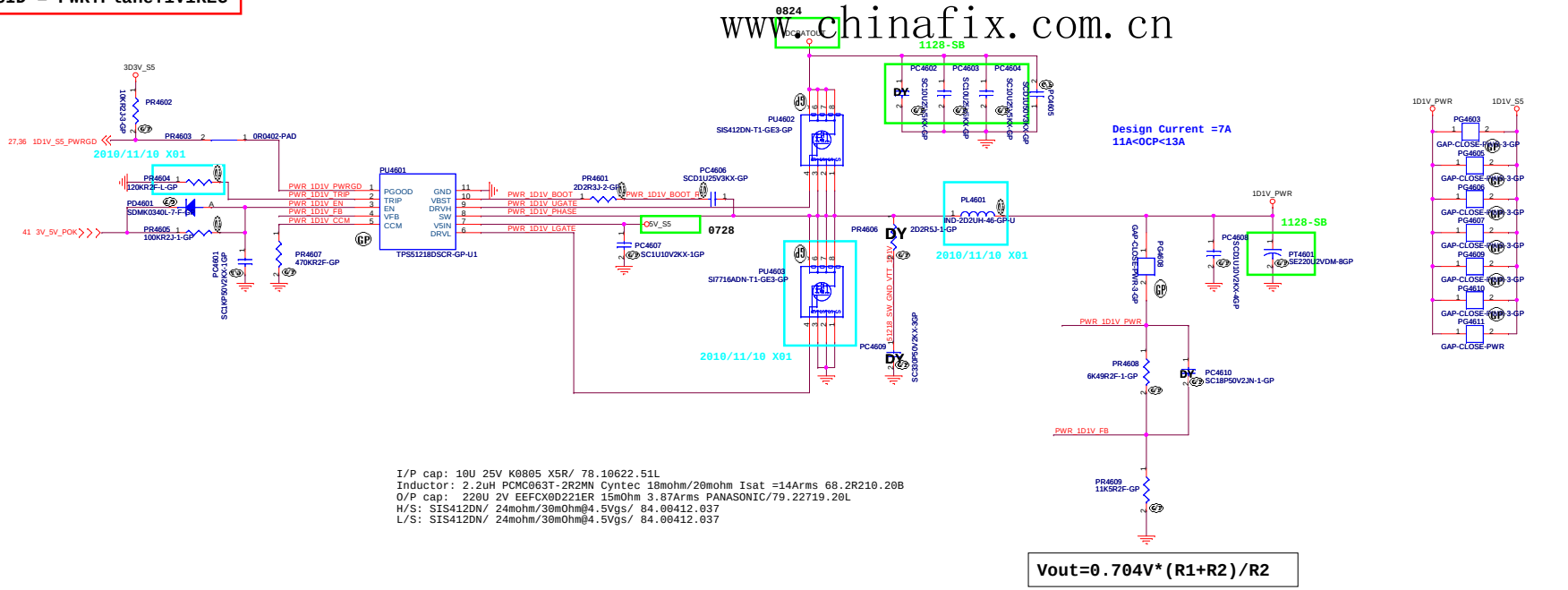
Taipei Hsien 221, Taiwan, R.O.C.

Title: VDDR & VDDP

Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 45 of 109

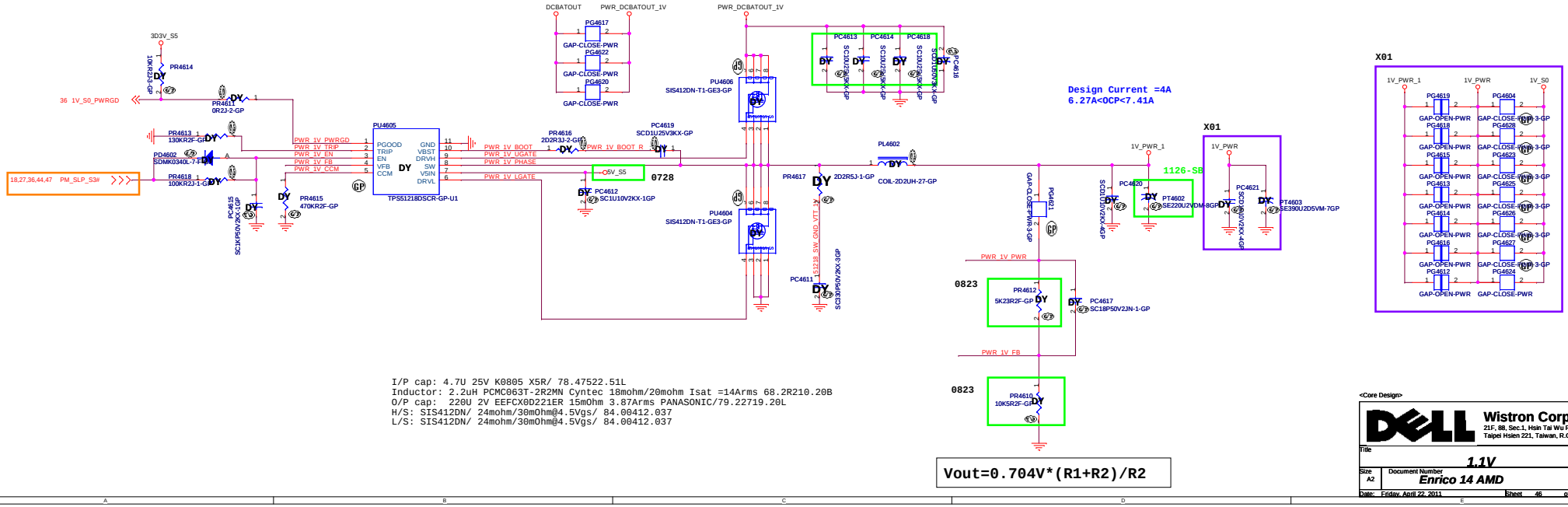
SSID = PWR.Plane.1V1REG



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 3.87Arms PANASONIC/79.22719.20L
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037

Vout=0.704V*(R1+R2)/R2

SSID = PWR.Plane.1VREG



I/P cap: 4.7U 25V K0805 X5R/ 78.47522.51L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 3.87Arms PANASONIC/79.22719.20L
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037

Vout=0.704V*(R1+R2)/R2

<Core Design>

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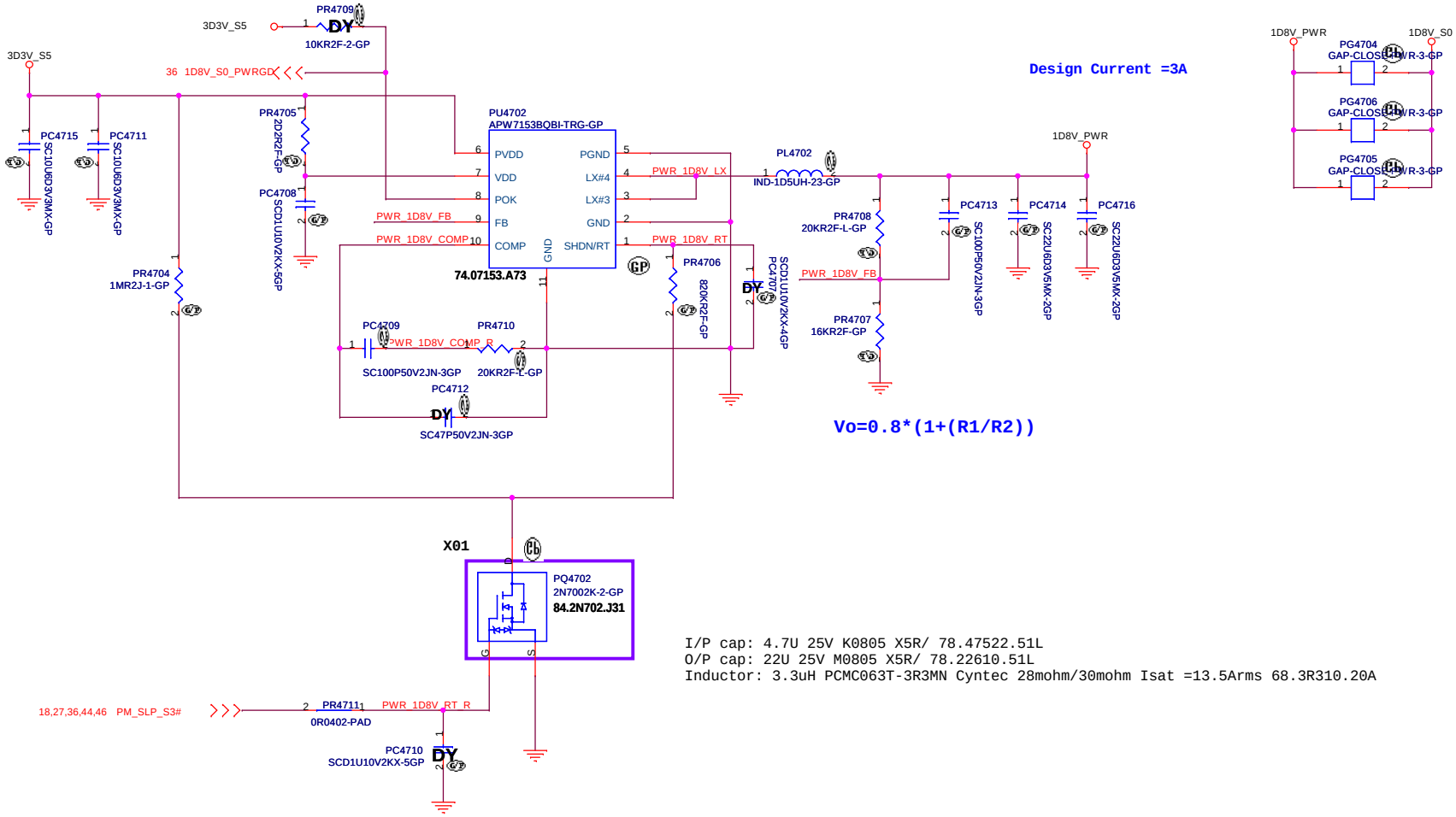
Title	1.1V	
Size: A2	Document Number: Enrico 14 AMD	Rev: A00
Date: Friday, April 22, 2011	Sheet 46 of 109	

SSID = PWR.Plane.1V8REG

APW7153B for 1D8V_S0



Vo=0.8*(1+(R1/R2))

I/P cap: 4.7U 25V K0805 X5R/ 78.47522.51L
O/P cap: 22U 25V M0805 X5R/ 78.22610.51L
Inductor: 3.3uH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A

<Core Design>

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Title: RT8015B_1D8V_S0

Size	Document Number	Rev
A3	Enrico 14 AMD	A00

Date: Friday, April 22, 2011 Sheet 47 of 109

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<Core Design>

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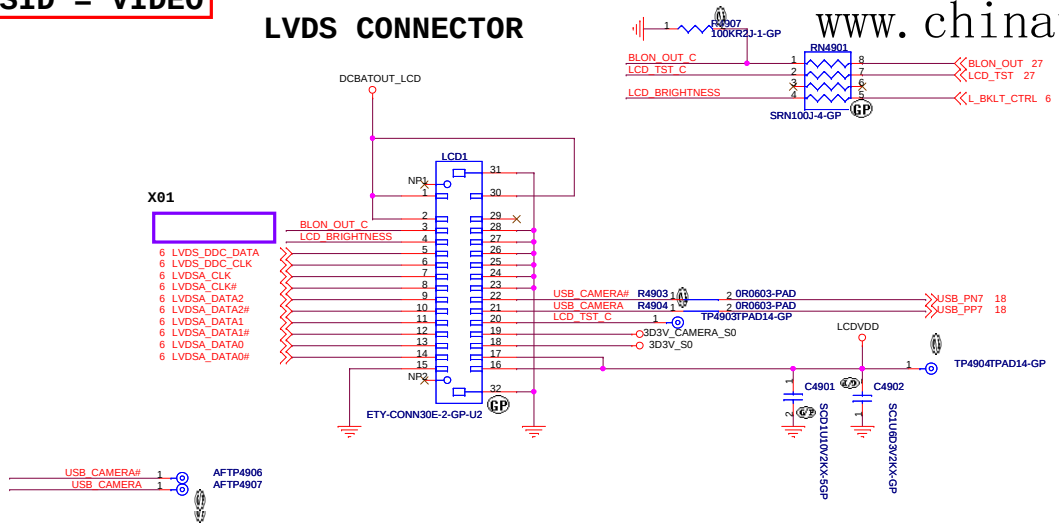
Title: *Reserved*

Size: A3 | Document Number: *Enrico 14 AMD* | Rev: *A00*

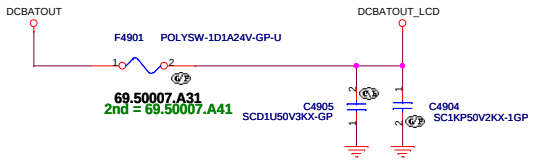
Date: Friday, April 22, 2011 | Sheet 48 of 109

SSID = VIDEO

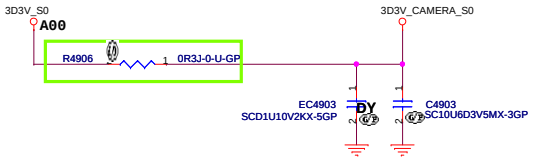
LVDS CONNECTOR



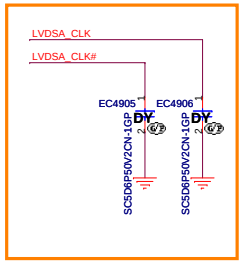
INVERTER POWER

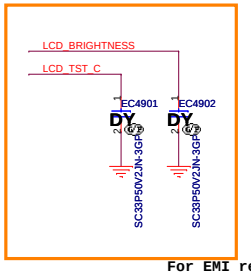


Camera Power

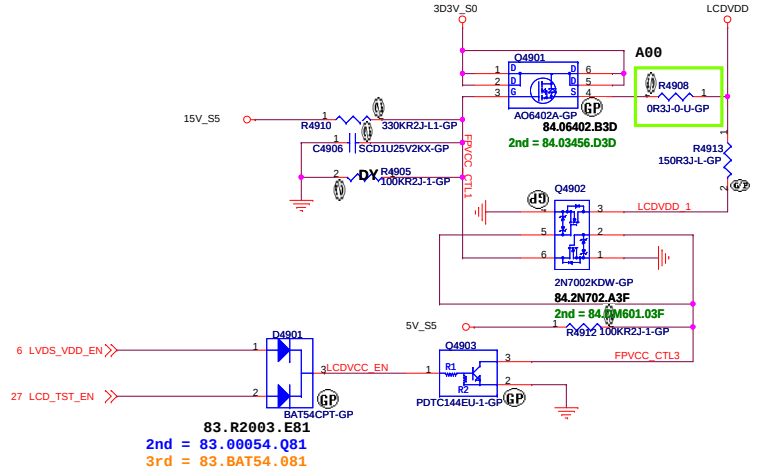


Close to LVDS connector





For EMI request



<Core Design>

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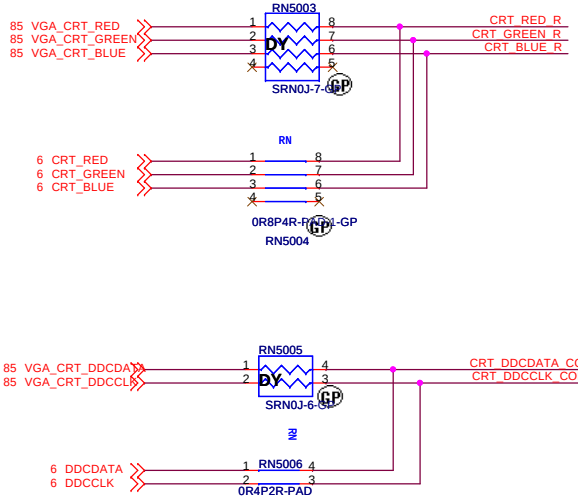
Title: LCD/Inverter Connector

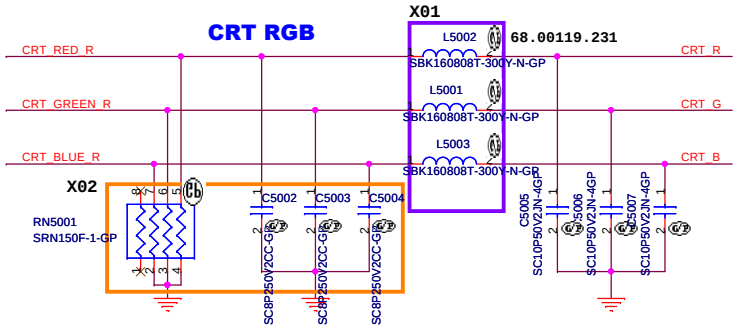
Size	Document Number	Rev
Custom	Enrico 14 AMD	A00

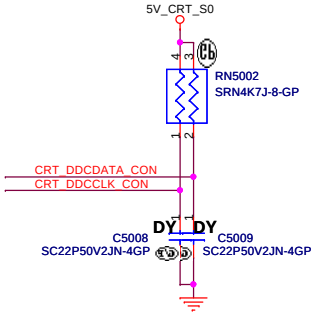
Date: Friday, April 22, 2011 Sheet 49 of 109

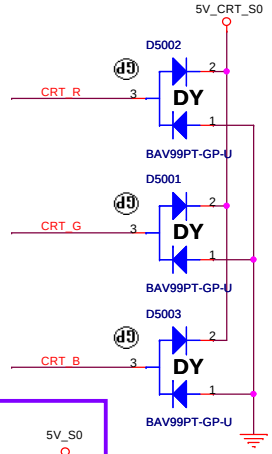
SSID = VIDEO

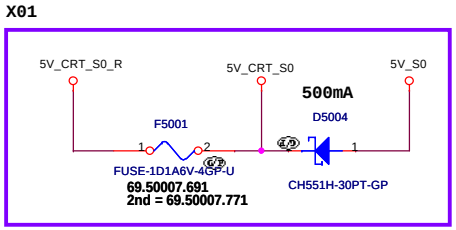
Layout Note:
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

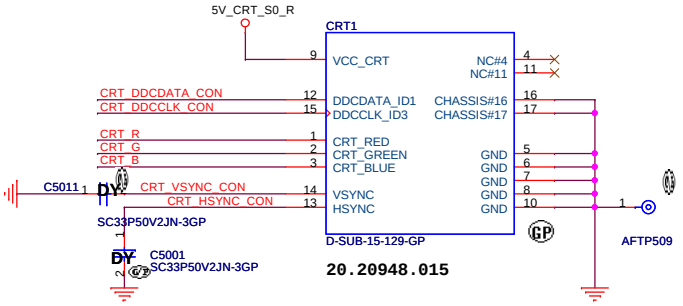






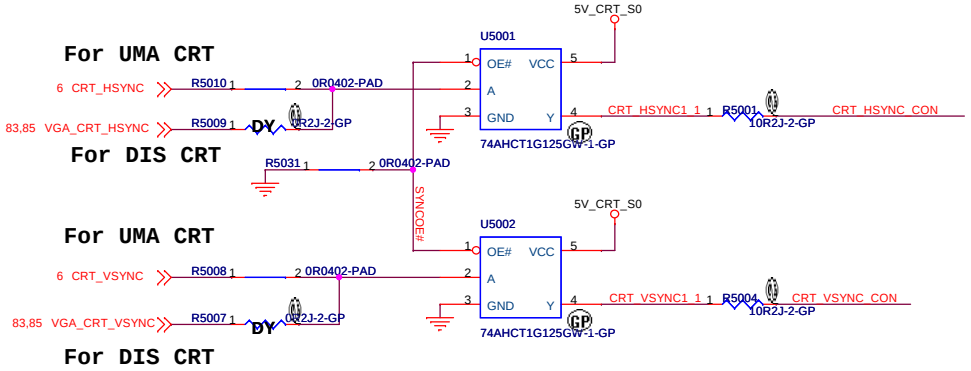


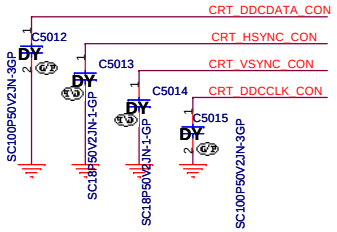


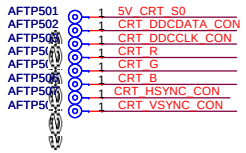


X01

CRT Hsync & Vsync level shift







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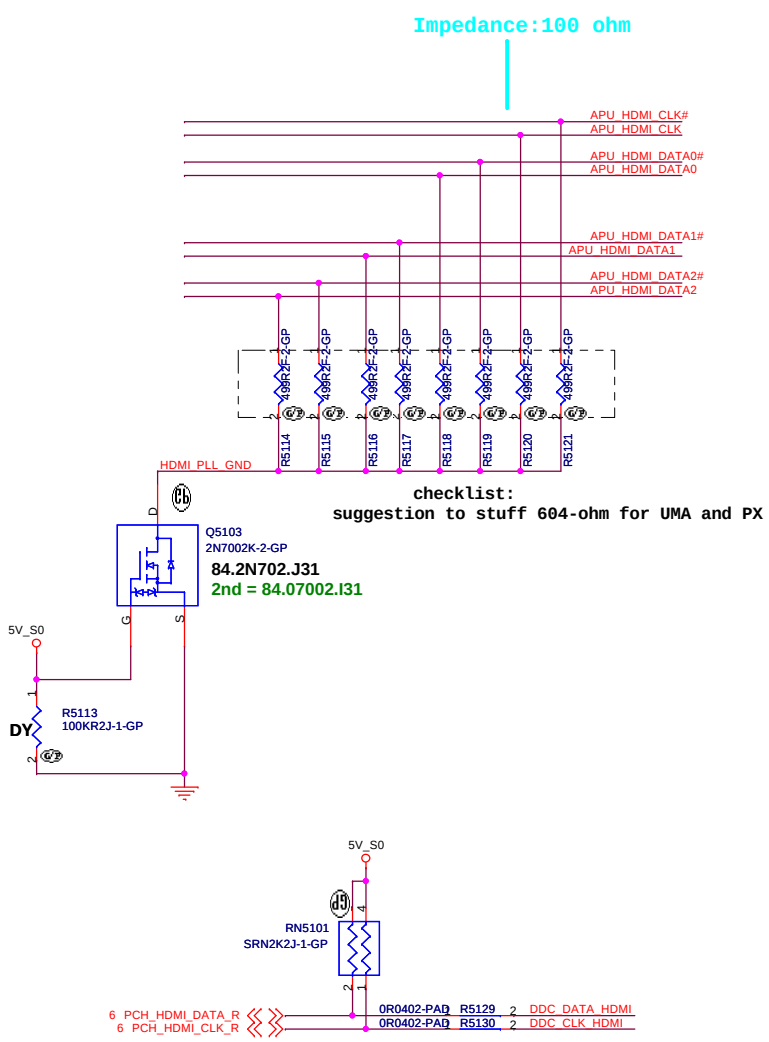
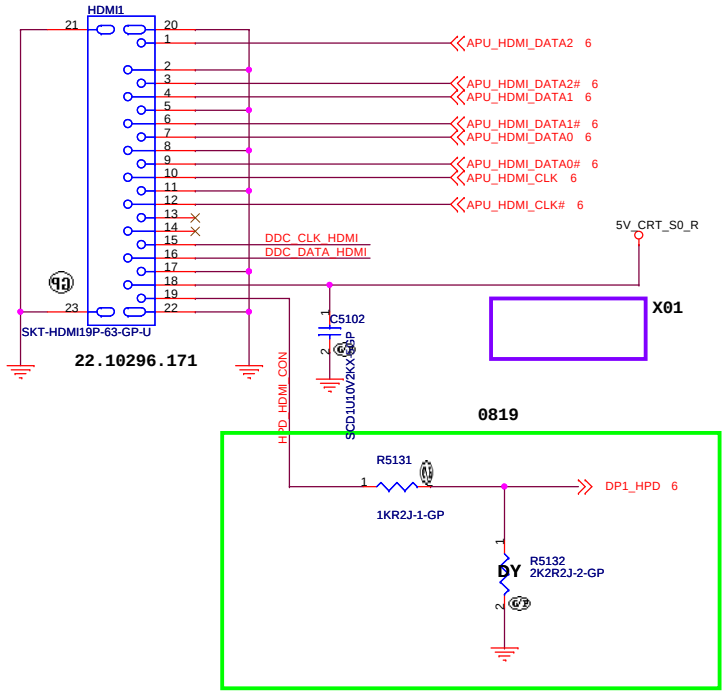
Title	DCIN	
Size: A3	Document Number: Enrico 14 AMD	Rev: A00
Date: Friday, April 22, 2011	Sheet 50 of 109	

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

HDMI CONN





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Title		
HDMI Level Shifter/Connector		
Size: A3	Document Number: Enrico 14 AMD	Rev: A00
Date: Friday, April 22, 2011	Sheet 51 of 109	

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Title
eDP

Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 52 of 109

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Title: *Reserved*

Size: A3 | Document Number: *Enrico 14 AMD* | Rev: *A00*

Date: Friday, April 22, 2011 | Sheet 53 of 109

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<Core Design>

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Title: *Reserved*

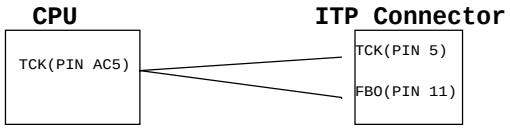
Size: A3 | Document Number: *Enrico 14 AMD* | Rev: *A00*

Date: Friday, April 22, 2011 | Sheet 54 of 109

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



<Core Design>

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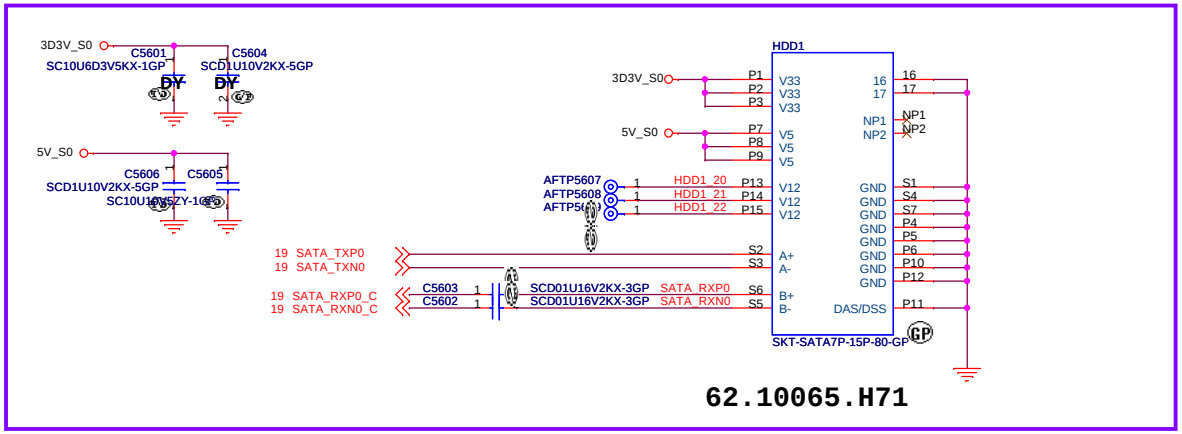
Title: ITP		
Size: A3	Document Number: Enrico 14 AMD	Rev: A00
Date: Friday, April 22, 2011	Sheet 55 of 109	

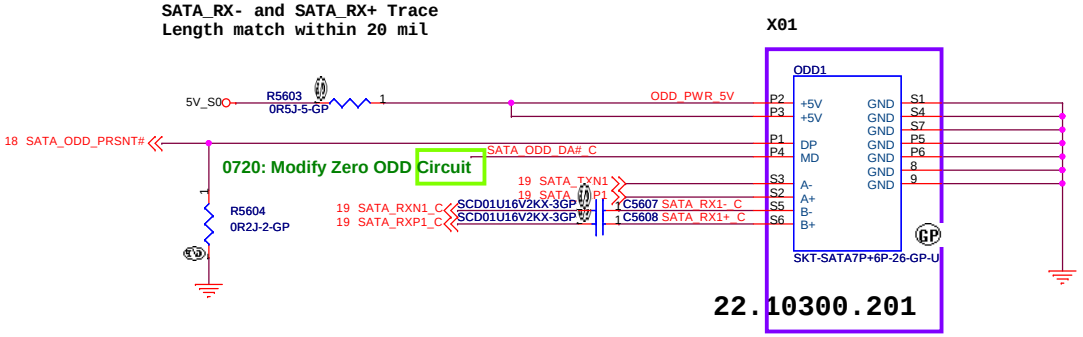
SSID = SATA

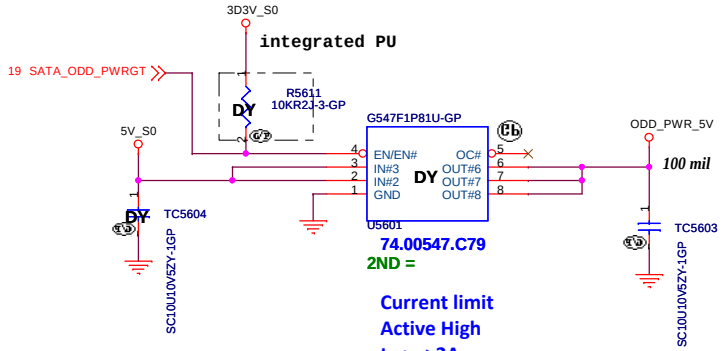
SATA HDD Connector



ODD Connector

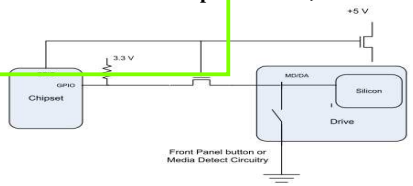
SATA_RX- and SATA_RX+ Trace
Length match within 20 mil



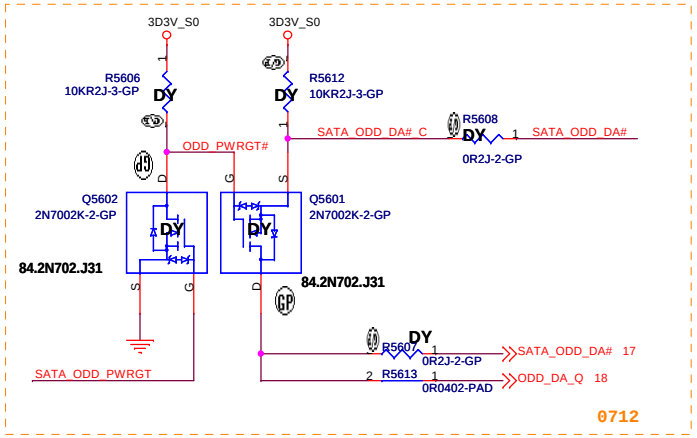


0721 Remove ODD_DA PU

When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON



0720: Modify Zero ODD Circuit



<Core Design>

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Title: HDD/ODD

Size	Document Number	Rev
A3	Enrico 14 AMD	A00

Date: Friday, April 22, 2011 Sheet 56 of 109

SSID = ESATA

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Title

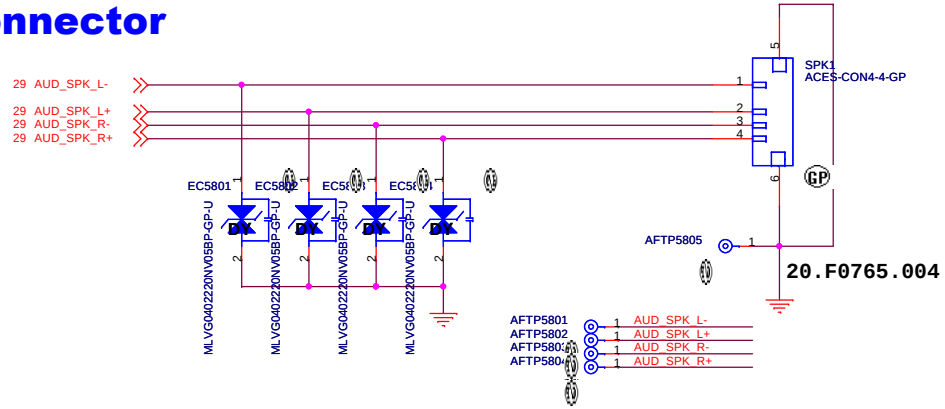
ESATA/USB Charger

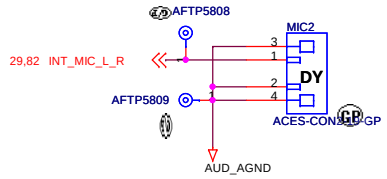
Size	Document Number	Rev
A3	Enrico 14 AMD	A00

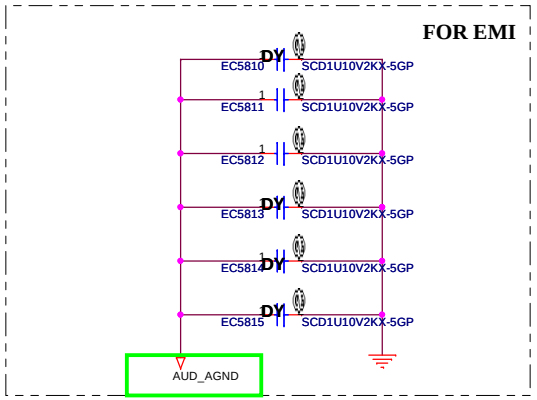
Date: Friday, April 22, 2011 Sheet 57 of 109

SSID = AUDIO

Speaker Connector







0804 Change to AGND

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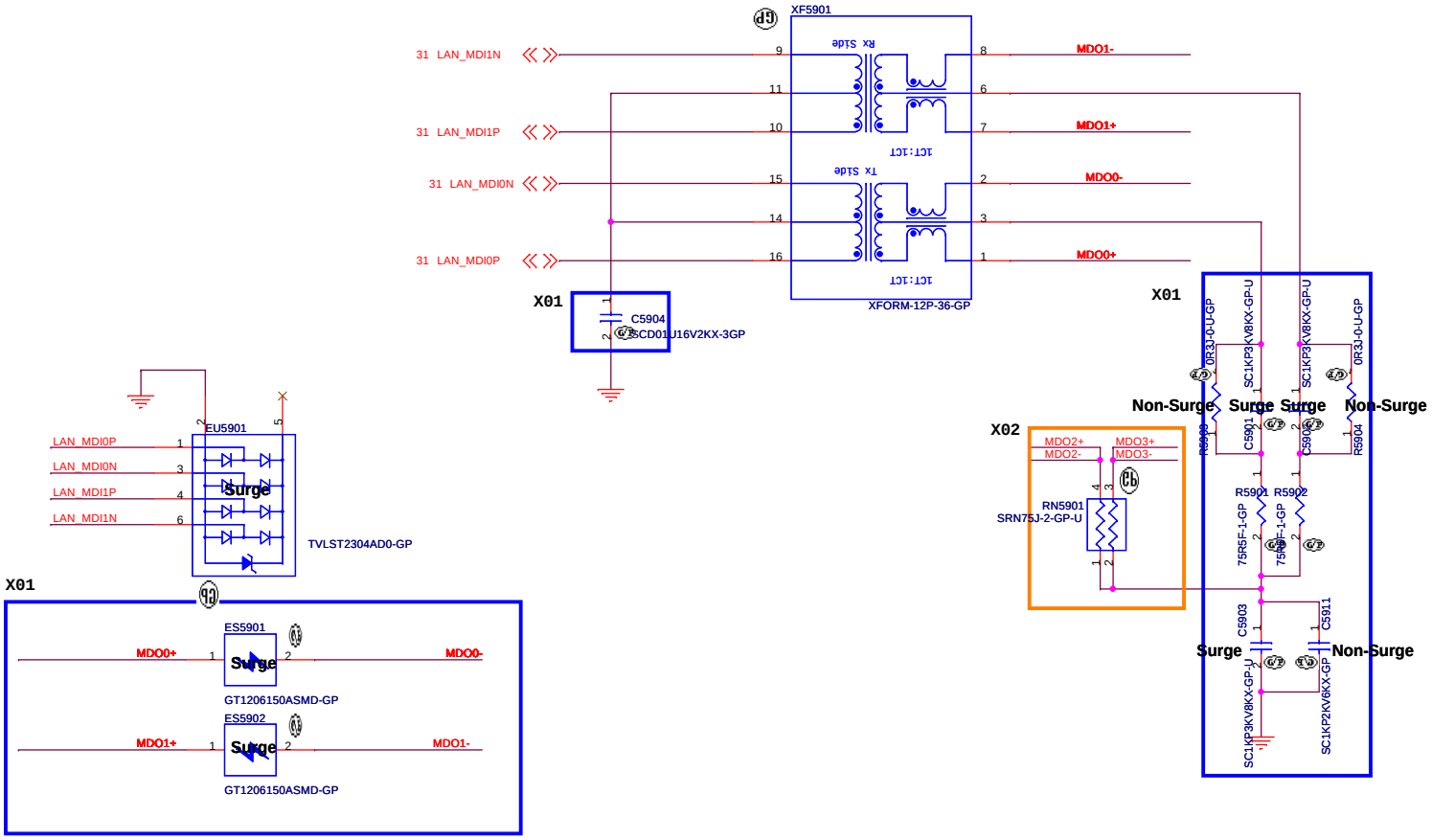
Title: Audio Jack

Size	Document Number	Rev
A3	Enrico 14 AMD	A00

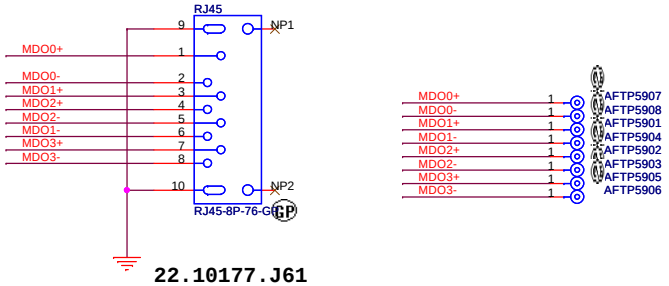
Date: Friday, April 22, 2011 Sheet 58 of 109

SSID = LOM

LAN TransFormer



RJ45



22.10177.J61

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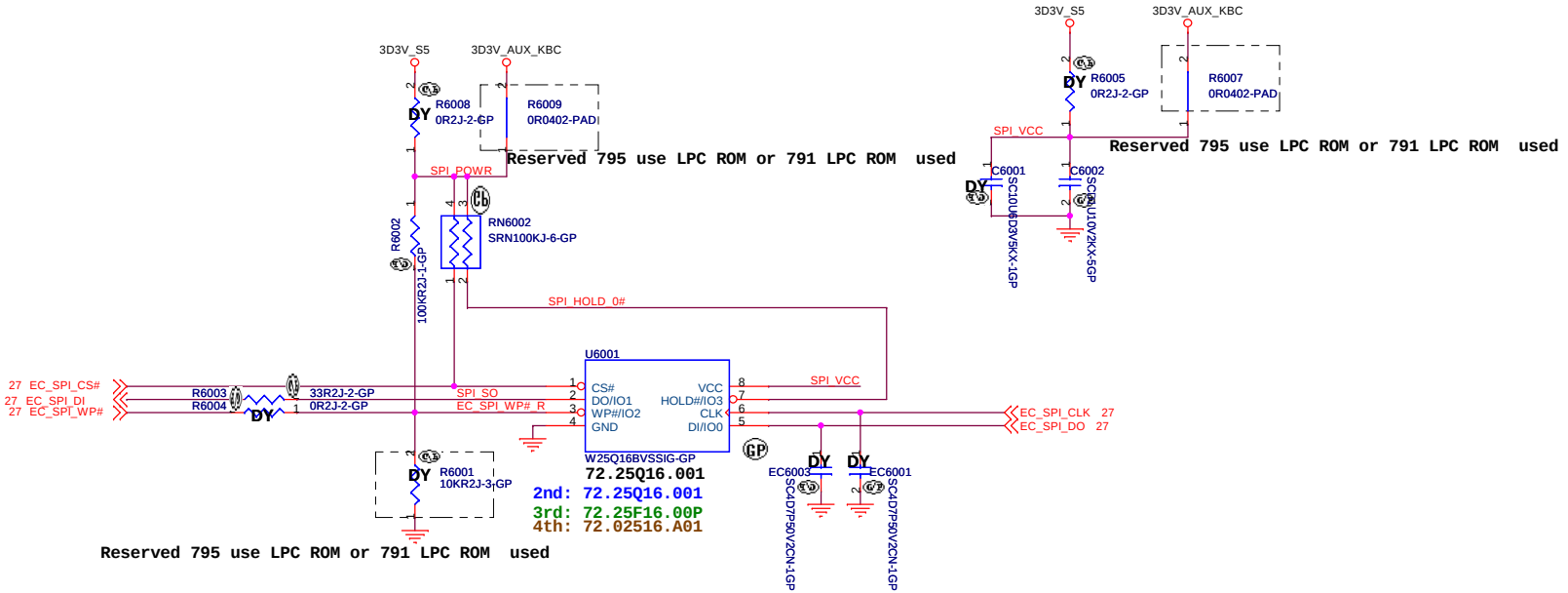
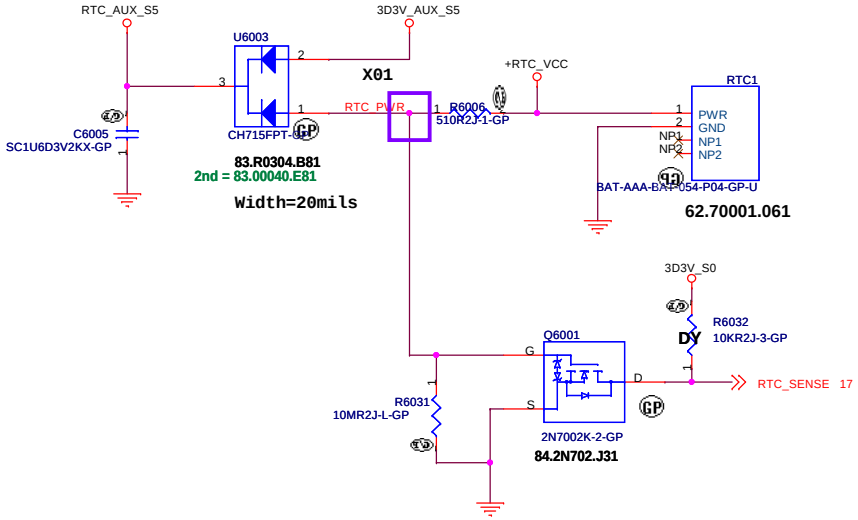
Title	LAN	
Size A3	Document Number: Enrico 14 AMD	Rev A00
Date: Friday, April 22, 2011	Sheet 59 of 109	

SSID = Flash.ROM

SPI FLASH ROM (2M byte) for KBC



SSID = RBATT



<Core Design>

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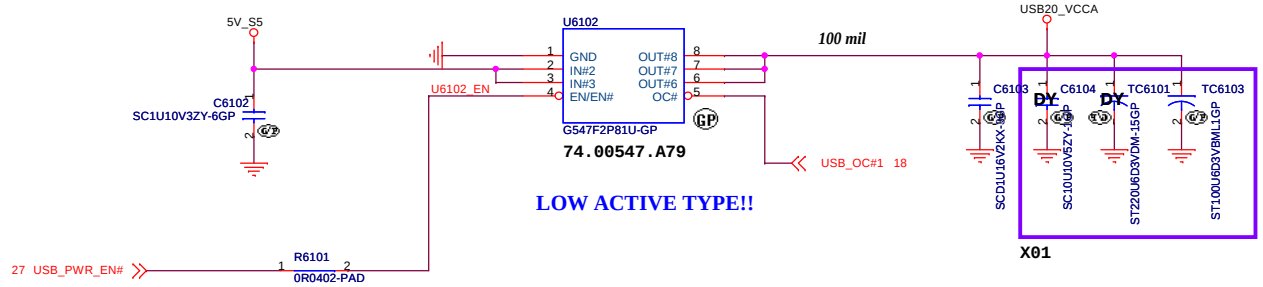
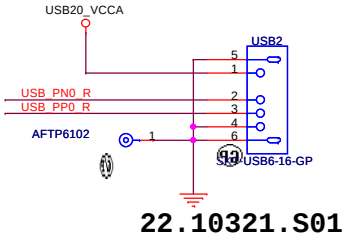
Title	Flash/RTC	
Size: A3	Document Number: Enrico 14 AMD	Rev: A00
Date: Friday, April 22, 2011	Sheet 60 of 109	

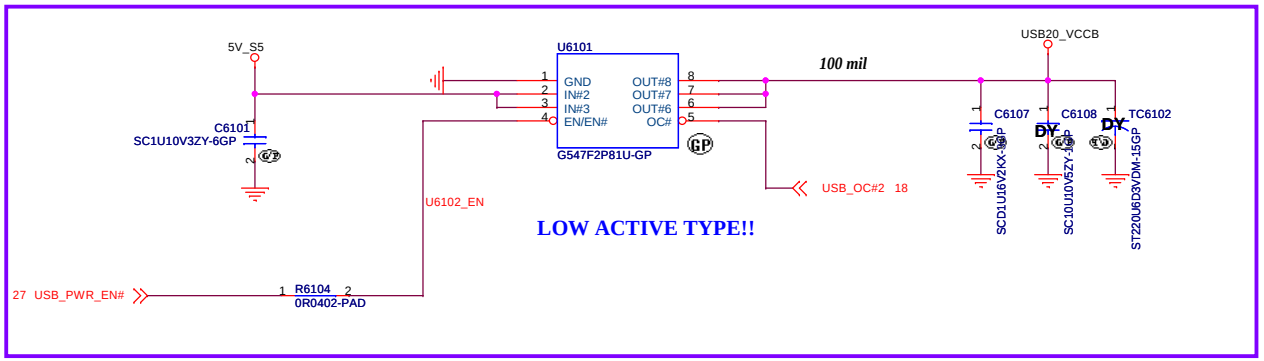
SSID = USB

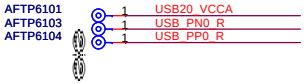
www.chinafix.com.cn



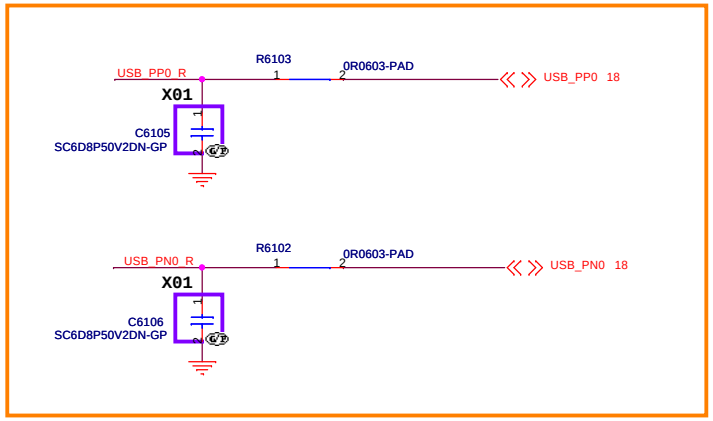


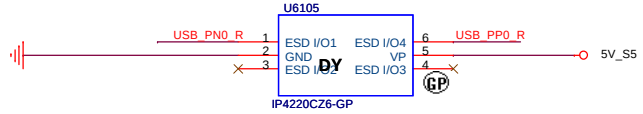
X01





X02





<Core Design>

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Title: USB Power SW

Size | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 61 of 109

(Blanking)

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Title: USB 3.0

Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 62 of 109

SSID = User.Interface

(Blanking)

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Title: Bluetooth

Size	Document Number	Rev
A3	Enrico 14 AMD	A00

Date: Friday, April 22, 2011 Sheet 63 of 109

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

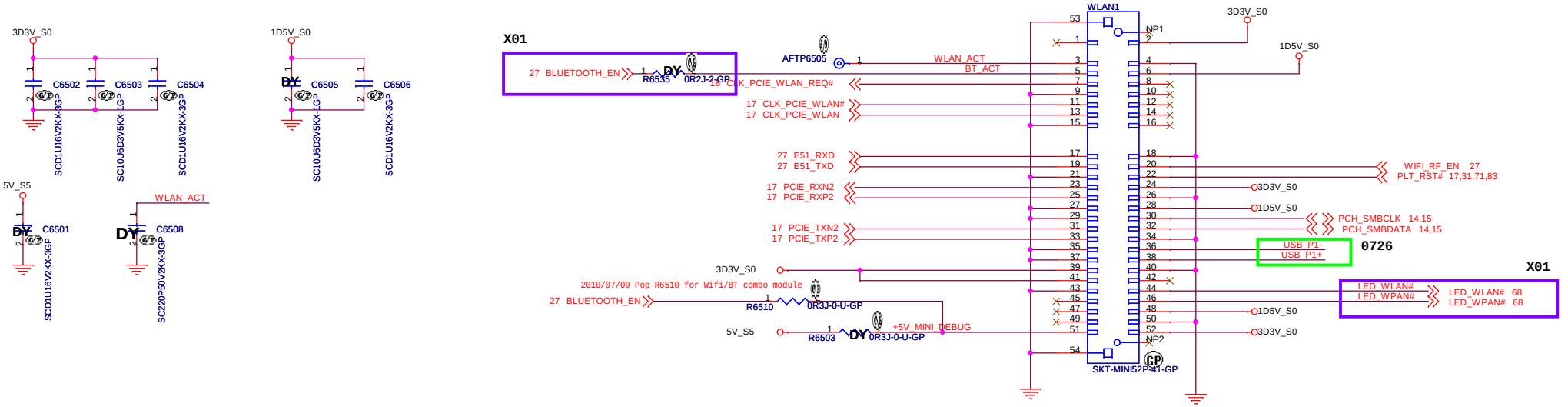
Title: F/P

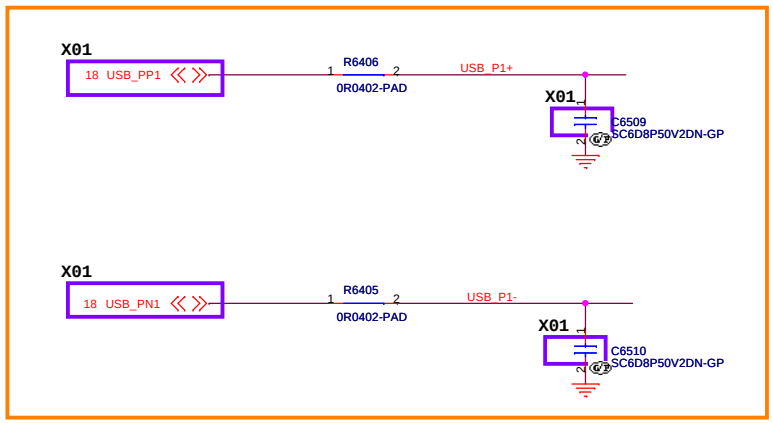
Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 64 of 109

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)





05/19 Add Common Mode Choke
2010/07/16 Change CMC L6401 to smaller 69.10118.001 (the same same as other CMCs on MB) and rename L6401 to TR6501.
Change R6406,R6405 to 0R 0402 size

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/ITP CONN

Size	Document Number	Rev
A3	Enrico 14 AMD	A00

Date: Friday, April 22, 2011 Sheet 65 of 109

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN

Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 66 of 109

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

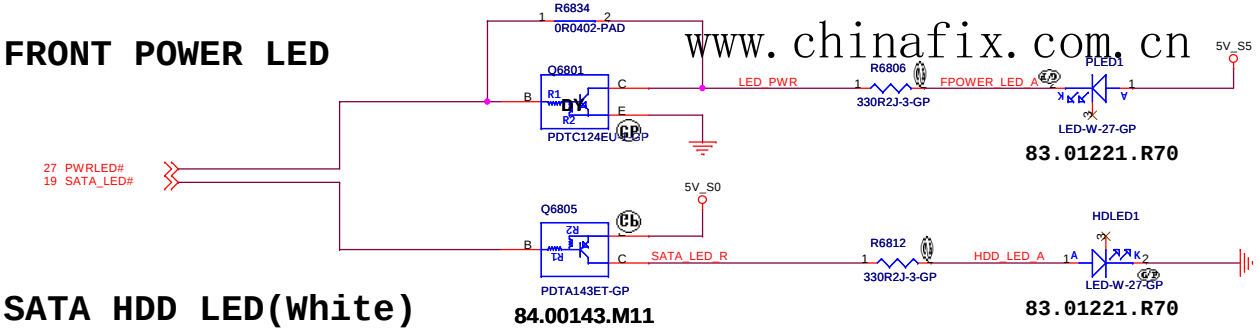
Size: A3 | Document Number: *Enrico 14 AMD* | Rev: *A00*

Date: Friday, April 22, 2011 | Sheet 67 of 109

SSID = User.Interface

X01

FRONT POWER LED

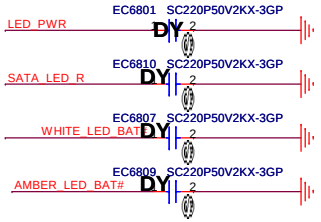


83.01221.R70

84.00143.M11

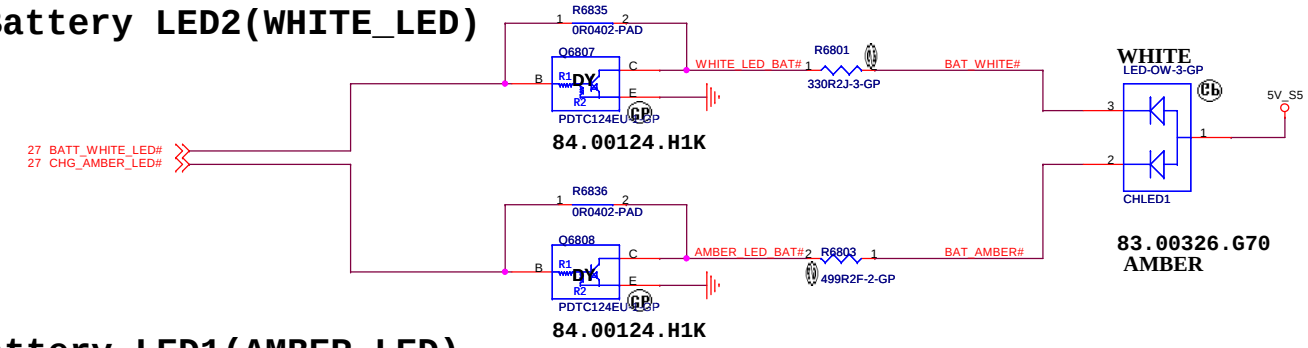
83.01221.R70

SATA HDD LED(White)



X01

Battery LED2(WHITE_LED)



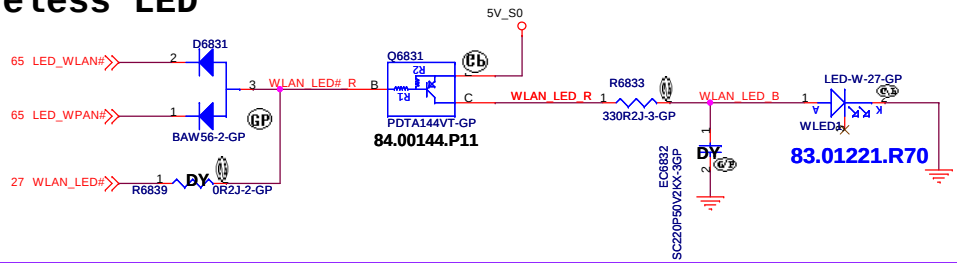
84.00124.H1K

84.00124.H1K

83.00326.G70
AMBER

Battery LED1(AMBER_LED)

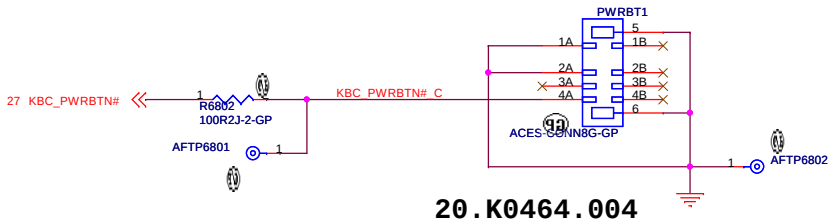
Wireless LED



84.00144.P11

83.01221.R70

Power button



20.K0464.004

<Core Design>

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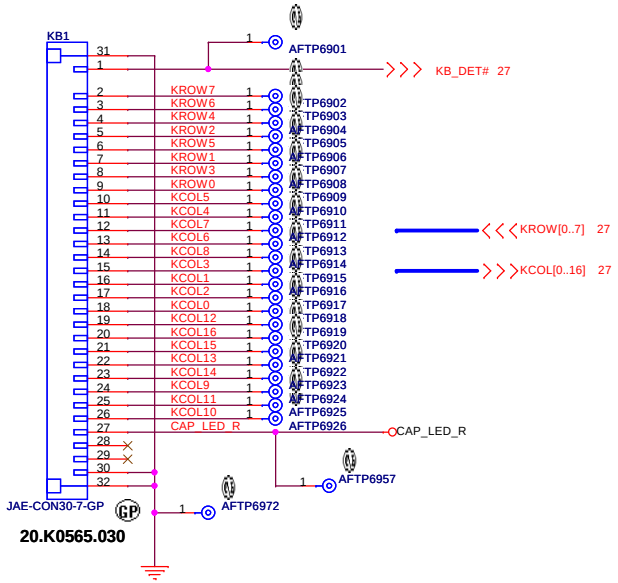
Taipei Hsien 221, Taiwan, R.O.C.

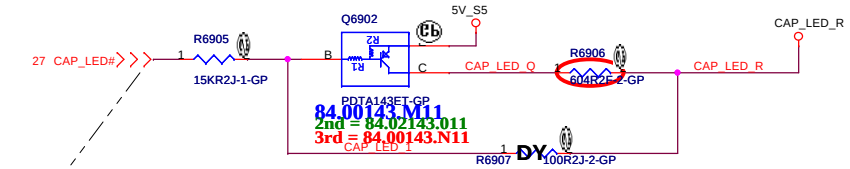
Title	LED Bard/Power Button	
Size A3	Document Number: Enrico 14 AMD	Rev: A00
Date: Friday, April 22, 2011	Sheet 68 of 109	

X01

SSID = KBC

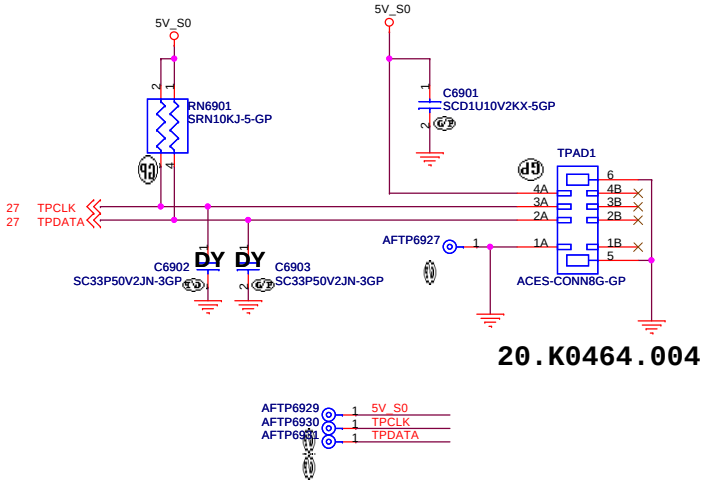


20101116 X02 Modify:
Change R6906 to 1K from 390ohm for
fine tune LED illumination.
20101118 X02:
Dell recommand: change all white LEDs resistor to 620 ohm.
20101202 X02:
Dell recommand: change all white LEDs resistor to 604 ohm.



CAP_LED:(X01 Low actived)
Connect to KB driving internal LED directly.(MAX 25mA)

TouchPad Connector



<Core Design>

Wistron Corporation
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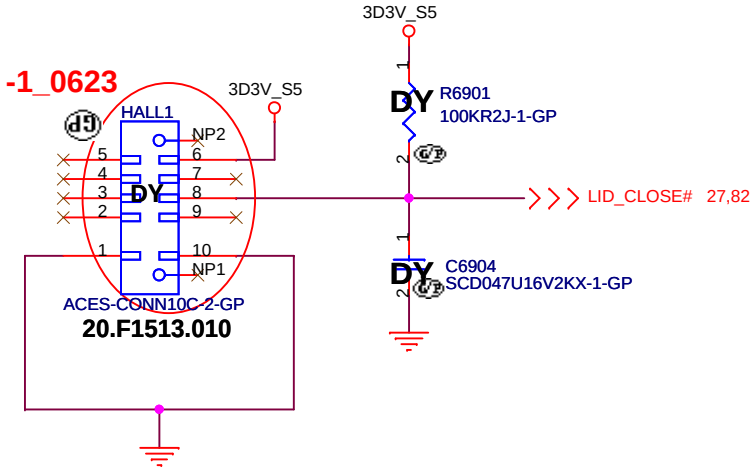
Taipei Hsien 221, Taiwan, R.O.C.

Title	Key Board/Touch Pad	
Size: A3	Document Number: Enrico 14 AMD	Rev: A00
Date: Friday, April 22, 2011	Sheet 69 of 109	

SSID = Hall.Sensor



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

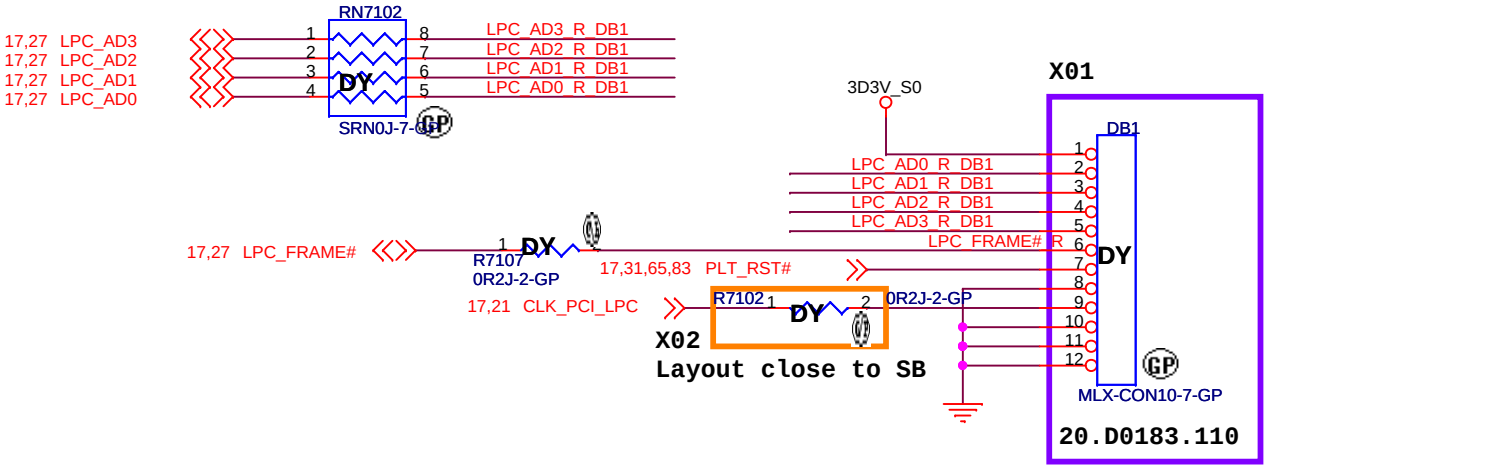
Title: ***Hall Effect Sensor***

Size	Document Number	Rev
A4	***Enrico 14 AMD***	***A00***

Date: Friday, April 22, 2011 Sheet 70 of 109

SSID = Debug

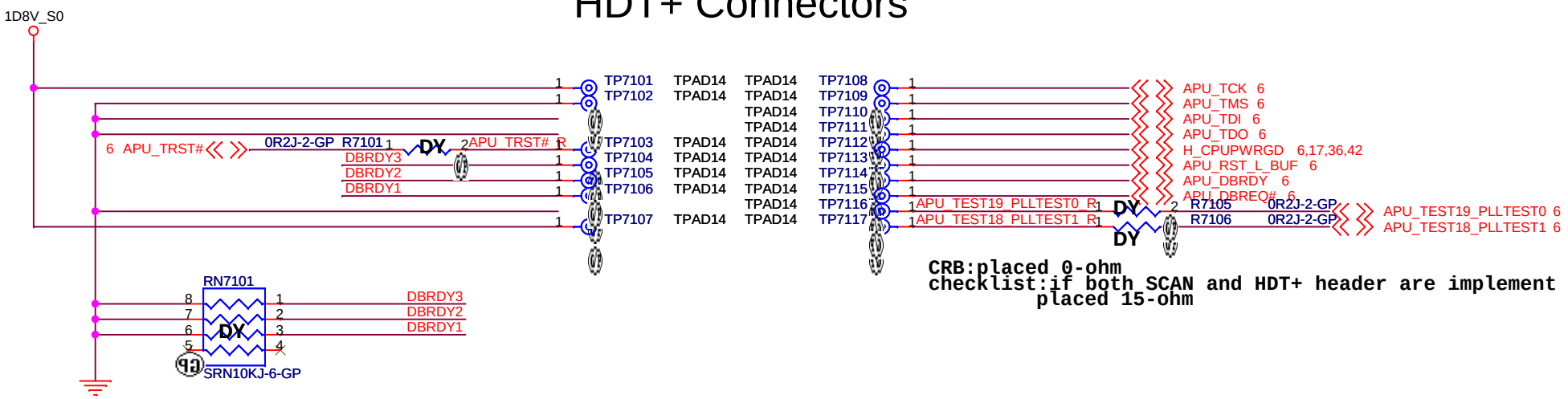
www.chinafix.com.cn



PCB Footprint = PAD-10P-177042

DY HDT+

HDT+ Connectors



CRB:placed 0-ohm
checklist:if both SCAN and HDT+ header are implement placed 15-ohm

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Dubug connector***	
Size: A4	Document Number: ***Enrico 14 AMD***	Rev: ***A00***
Date: Friday, April 22, 2011	Sheet 71 of 109	

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RESERVED

Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 72 of 109

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

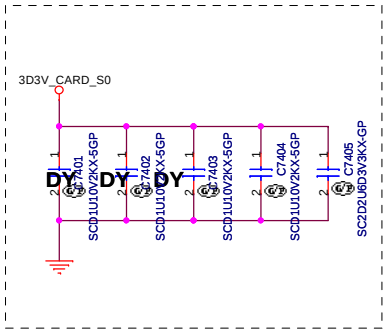
Title: *Reserved*

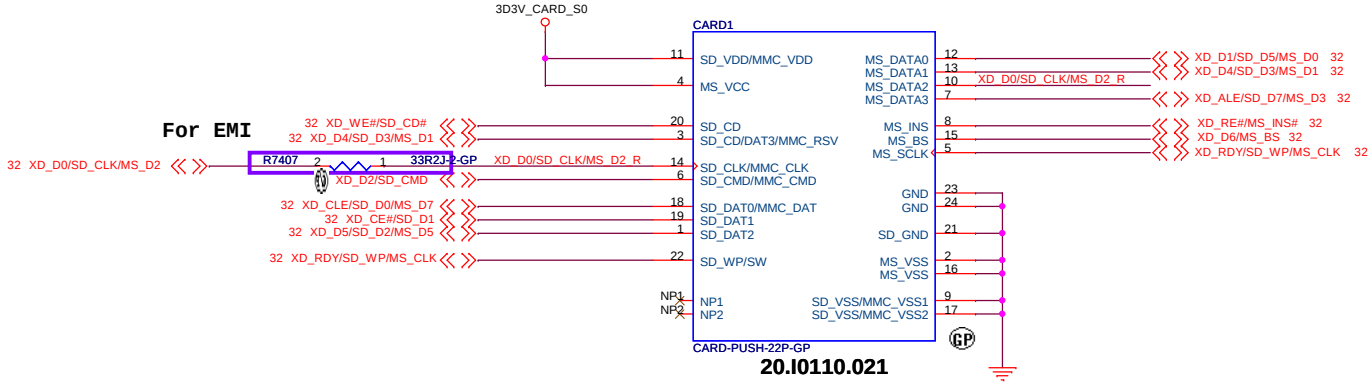
Size: A3 | Document Number: *Enrico 14 AMD* | Rev: *A00*

Date: Friday, April 22, 2011 | Sheet 73 of 109

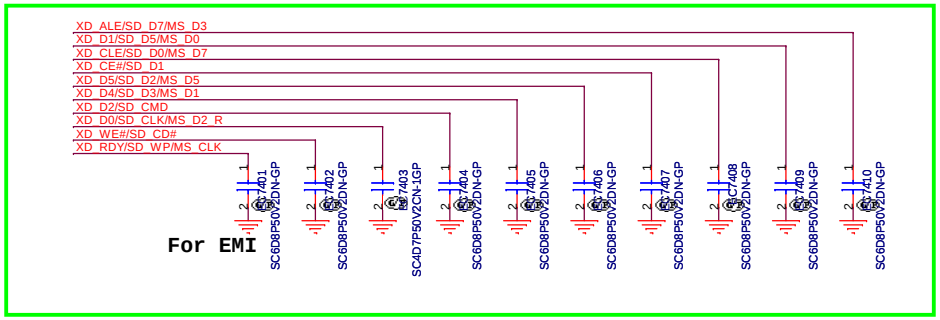
SSID = SDIO

SD/XD/MS Card Reader





0810 Vendor Recommand



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader Connector

Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 74 of 109

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Express Card

Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 75 of 109

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Enrico 14 AMD* | Rev: *A00*

Date: Friday, April 22, 2011 | Sheet 76 of 109

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Enrico 14 AMD* | Rev: *A00*

Date: Friday, April 22, 2011 | Sheet 77 of 109

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	Enrico 14 AMD	A00

Date: Friday, April 22, 2011 Sheet 78 of 109

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Enrico 14 AMD* | Rev: *A00*

Date: Friday, April 22, 2011 | Sheet 79 of 109

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Enrico 14 AMD* | Rev: *A00*

Date: Friday, April 22, 2011 | Sheet 80 of 109

(Blanking)

<Core Design>

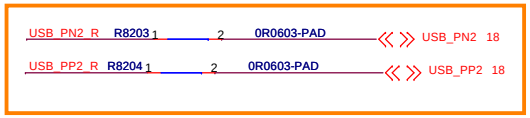
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
UNUSED PARTS/EMI Capacitors

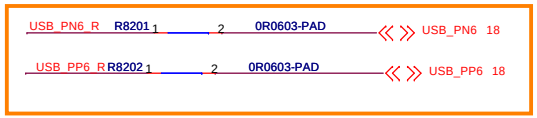
Size	Document Number	Rev
A3	*Enrico 14 AMD*	*A00*

Date: Friday, April 22, 2011 Sheet 81 of 109

X02



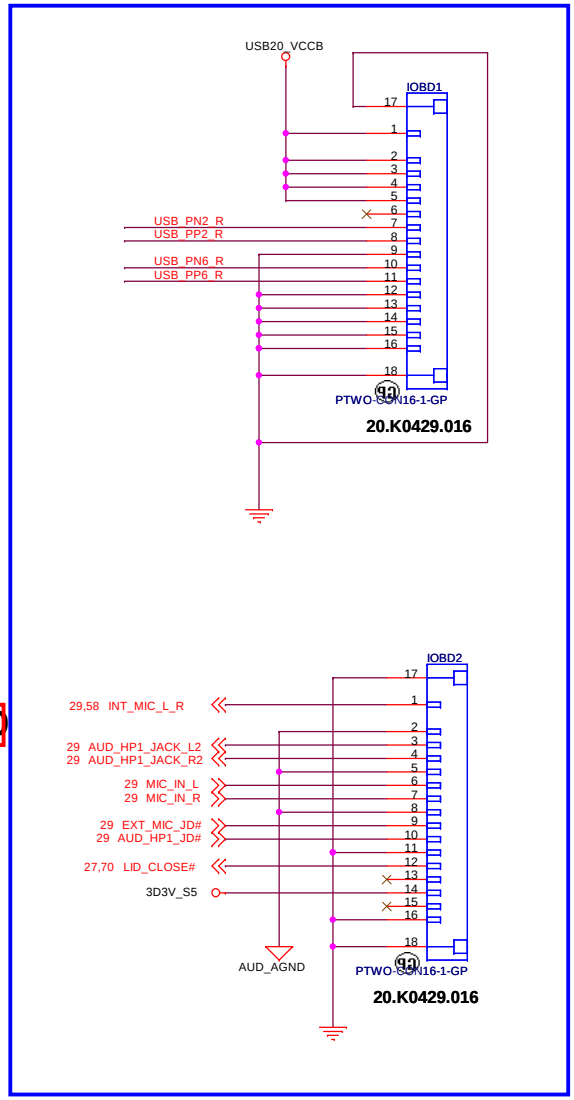
X02



SSID = USB

SSID = AUDIO

X01



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***IO Board Connector***

Size	Document Number	Rev
A3	***Enrico 14 AMD***	***A00***

Date: Friday, April 22, 2011 Sheet 82 of 109

SSID = VIDEO

VGA1A 1 OF 7

PCI EXPRESS INTERFACE

DIS_PX

4 PEG_TXP0	PEG_TXP0	AE30	PCIE_RX0P	PCIE_TX0P	AH30	PEG_C_RXP0 C8306 DIS_PX	SCD1U10V2KX-5GP	PEG_RXP0 4
4 PEG_TXN0	PEG_TXN0	AE31	PCIE_RX0N	PCIE_TX0N	AG31	PEG_C_RXN0 C8305 DIS_PX	SCD1U10V2KX-5GP	PEG_RXN0 4
4 PEG_TXP1	PEG_TXP1	AE29	PCIE_RX1P	PCIE_TX1P	AG29	PEG_C_RXP1 C8303 DIS_PX	SCD1U10V2KX-5GP	PEG_RXP1 4
4 PEG_TXN1	PEG_TXN1	AD28	PCIE_RX1N	PCIE_TX1N	AF28	PEG_C_RXN1 C8304 DIS_PX	SCD1U10V2KX-5GP	PEG_RXN1 4
4 PEG_TXP2	PEG_TXP2	AD30	PCIE_RX2P	PCIE_TX2P	AF27	PEG_C_RXP2 C8310 DIS_PX	SCD1U10V2KX-5GP	PEG_RXP2 4
4 PEG_TXN2	PEG_TXN2	AC31	PCIE_RX2N	PCIE_TX2N	AF26	PEG_C_RXN2 C8309 DIS_PX	SCD1U10V2KX-5GP	PEG_RXN2 4
4 PEG_TXP3	PEG_TXP3	AC29	PCIE_RX3P	PCIE_TX3P	AD27	PEG_C_RXP3 C8308 DIS_PX	SCD1U10V2KX-5GP	PEG_RXP3 4
4 PEG_TXN3	PEG_TXN3	AB28	PCIE_RX3N	PCIE_TX3N	AD26	PEG_C_RXN3 C8307 DIS_PX	SCD1U10V2KX-5GP	PEG_RXN3 4
		AB30	PCIE_RX4P	PCIE_TX4P	AC25			
		AA31	PCIE_RX4N	PCIE_TX4N	AB25			
		AA29	PCIE_RX5P	PCIE_TX5P	Y23			
		Y28	PCIE_RX5N	PCIE_TX5N	Y24			
		Y30	PCIE_RX6P	PCIE_TX6P	AB27			
		W31	PCIE_RX6N	PCIE_TX6N	AB26			
		W29	PCIE_RX7P	PCIE_TX7P	Y27			
		V28	PCIE_RX7N	PCIE_TX7N	Y26			
		V30	PCIE_RX8P	PCIE_TX8P	W24			
		U31	PCIE_RX8N	PCIE_TX8N	W23			
		U29	PCIE_RX9P	PCIE_TX9P	V27			
		T28	PCIE_RX9N	PCIE_TX9N	U26			
		T30	PCIE_RX10P	PCIE_TX10P	U24			
		R31	PCIE_RX10N	PCIE_TX10N	U23			
		R29	PCIE_RX11P	PCIE_TX11P	T26			
		P28	PCIE_RX11N	PCIE_TX11N	T27			
		P30	PCIE_RX12P	PCIE_TX12P	T24			
		N31	PCIE_RX12N	PCIE_TX12N	T23			
		N29	PCIE_RX13P	PCIE_TX13P	P27			
		M28	PCIE_RX13N	PCIE_TX13N	P26			
		M30	PCIE_RX14P	PCIE_TX14P	P24			
		L31	PCIE_RX14N	PCIE_TX14N	P23			
		L29	PCIE_RX15P	PCIE_TX15P	M27			
		K30	PCIE_RX15N	PCIE_TX15N	N26			

CLOCK

17 CLK_PCIE_VGA	AK30	PCIE_REFCLKP
17 CLK_PCIE_VGA#	AK32	PCIE_REFCLKN

CALIBRATION

Y22 PCIE_CALRP	R8321 DIS_PX 1K27R2F-L-GP	1V_VGA_S0
AA22 PCIE_CALRN	R8315 DIS_PX 2KR2F-3-GP	

PWRGOOD N10

PERST# AL27

2010/06/10
Move CAPs close to CPU

R8314 DIS_PX 10KR2F-2-GP PWRGOOD

ATI_RST# — R8316 DIS_PX 0R0402-PAD — VGA_RST#

DY C8312 ROBSON-GP-U SC47P50V2JN-3GP

71.ROBSO.M01

Colay with Seymour-XT-S3
(71.SEYMR.M01)

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
GPIO8_ROMSO	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
GPIO21_BB_EN	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

2010/06/11

2010/06/11 Need to check **PIN STRAPS**

3D3V_VGA_S0

85 TX_PWRS_ENB	R8301 DIS_PX	3KR2J-2-GP	
85 TX_DEEMPH_EN	R8302 DIS_PX	3KR2J-2-GP	2010/07/13 Stuff for 5.0GT/S
85 BIF_GEN2_EN_A	R8303 DIS_PX	10KR2J-3-GP	
85 GPIO8_ROMSO	R8304 DY	10KR2J-3-GP	
85 VGA_DIS	R8305 DY	10KR2J-3-GP	
85 CONFIG0	R8306 DIS_PX	10KR2J-3-GP	
85 CONFIG1	R8307 DY	10KR2J-3-GP	
85 CONFIG2	R8308 DY	10KR2J-3-GP	
50,85 VGA_CRT_VSYNC	R8309 DY	10KR2J-3-GP	
50,85 VGA_CRT_HSYNC	R8310 DY	10KR2J-3-GP	
85 BIOS_ROM_EN	R8313 DY	10KR2J-3-GP	
85 GPIO5_AC_BATT	R8318 DY	10KR2J-3-GP	
85 GPIO21_BB_EN	R8317 DY	10KR2J-3-GP	

3D3V_VGA_S0

85 JTAG_TMS_VGA	R8325 DY	10KR2J-3-GP
	R8328 DY	10KR2J-3-GP
84 TESTEN	R8327 DIS_PX	5K11R2F-L1-GP
85 JTAG_TRST#_VGA	R8326 DY	10KR2J-3-GP
85 JTAG_TCK_VGA	R8329 DY	10KR2J-3-GP

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

X01

17,86 1D5V_VGA_PWOK — R8330 0R2J-2-GP DY

93 1D8V_S0_VGA_PG — R8324 0R0402-PAD DIS_PX

C8311 DY SCD1U10V2KX-4GP

U8301 74LVC1G08GW-1-GP DIS_PX 73.01G08.L04 2ND = 73.7SZ08.DAH

3D3V_VGA_S0

U8302_Y

17 PE_GPIO0

U8302 74LVC1G08GW-1-GP DIS_PX 73.01G08.L04 2ND = 73.7SZ08.DAH

3D3V_VGA_S0

PLT_RST# — R8323 0R2J-2-GP DY — ATI_RST#

ATI_RST# 85

17,31,65,71 PLT_RST# — R8322 DY 0R2J-2-GP

0820 6,17 APU_RST# — R8331 DIS_PX 0R0402-PAD

	PE_GPIO0
dGPU mode	H
IGPU	L
IGPU with BACO	H

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

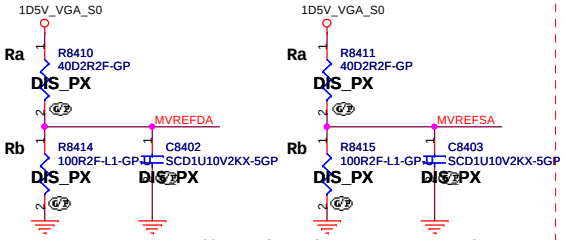
Title: GPU PEG/STRAPPING(1/5)

Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 83 of 109

SSID = VIDEO

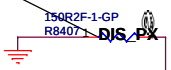
PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

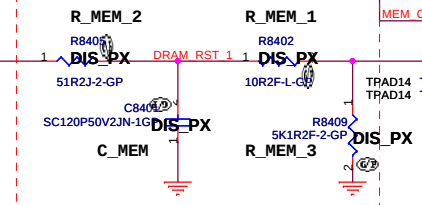


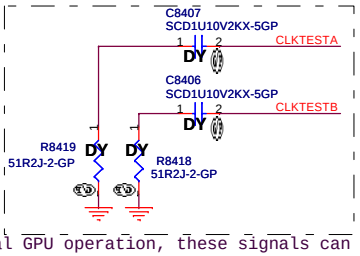
DDR3/GDDR3 Memory Stuff Option (ROBSON-S3/SEYMOUR-XT-S3)

	DDR5	DDR3
MVDDQ	1.5V	1.5V/1.8V
Ra	40.2R	40.2R
Rb	100R	100R

DPC_CALR (Park/Robson-S3):
Analog calibration.
Connect DPxx_CALR to GND through a 150-Ω (1%) resistor.







** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Designator	For SEYMOUR	For Robson
R_MEM_1	10R	10R
R_MEM_2	50R	50R
R_MEM_3	5K	5K
C_MEM	120pF	120pF

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except R_MEM_2

For normal GPU operation, these signals can be left floating (do not populate the capacitors and resistors).

2010/07/06
Schematics check list:
A pull-down resistor is required.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)

Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 84 of 109

Memory ID Table

DVPDATA[0:3]	Description
0000	DDR3 SAMSUNG-K4W1G1646G-BC11(900MHz)64M*16
0001	DDR3 Hynix-H5TQ1G63DFR-11C (900MHz) 64M*16
0010	DDR3 SAMSUNG K4W2G1646C-HC11 (900MHz) 128M*16
0011	DDR3 Hynix-H5TQ2G63BFR-11C (900MHz) 128M*16

DVPDATA[0:3] Default: Internal Pull down

SSID = VIDEO

LVDS Interface

For Seymour,
DPC_PVDD is DPC_VDD18 2010/06/11
DPC_PVSS and all DPC_VSSR are DP_VSSR

X02

2010/07/15 Modify:
Q8501 change to dual 2n7002.
Add R8512,R8521,C8529 for Q8501 pin2 turn on timming control.

0804 Modify for DV14 Config

MEM_ID Control

2010/06/11

2010/07/07 Remove TP8517,TP8518,TP8506,TP8519,TP8512

0723 Add SMBUS

2010/07/07
Change to RSVD based on DS v3.05

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

2010/07/06
Schematics check list:
A 1-M ohm resistor must be connected between XTALIN and XTALOUT when a crystal is used.

2010/07/06

80.30034.641
2nd 80.30034.651
3rd 80.30034.681

Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

71.ROBSO.M01
Colay with Seymour-XT-S3
(71.SEYMR.M01)

0820

0723 Add SMBUS

AUXP PD 100K
AUXN PU 100K
Draw on EDP circuit page

71.ROBSO.M01

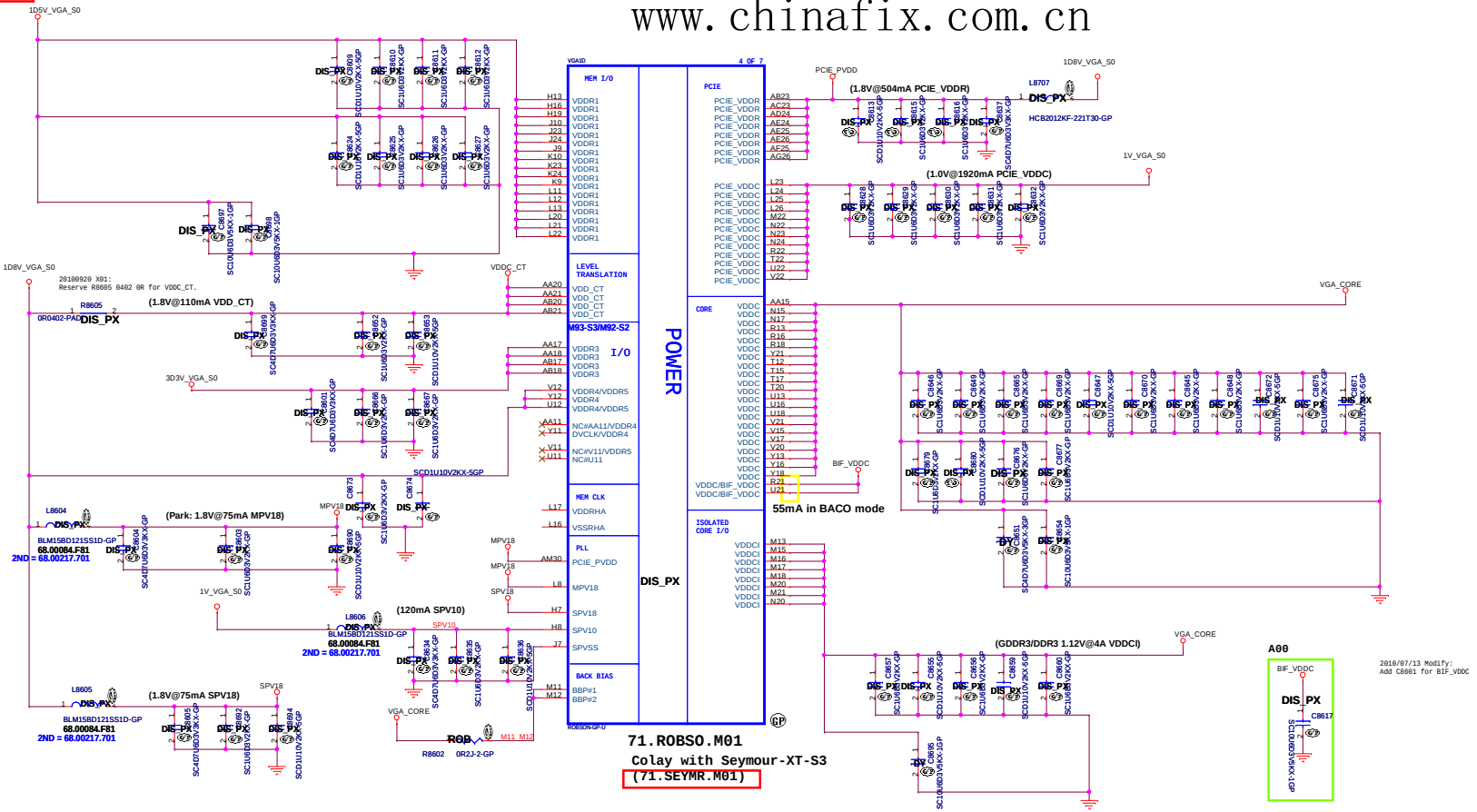
X01

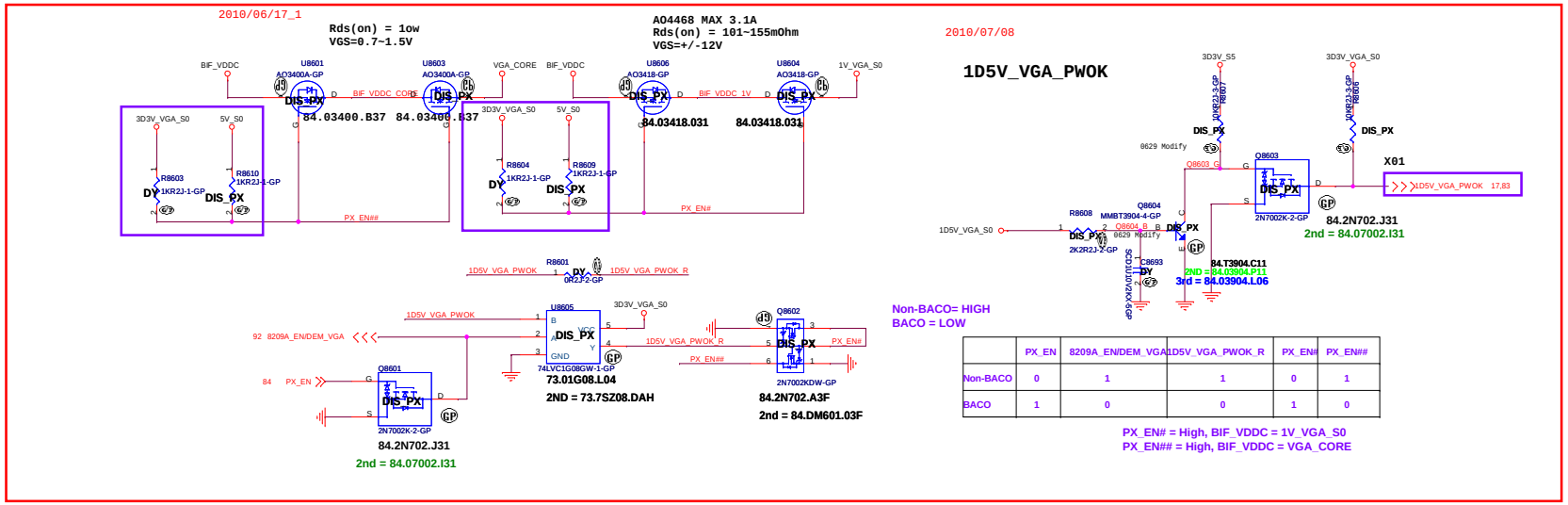
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)
Size: A2 | Document Number: Enrico 14 AMD | Rev: A00
Date: Friday, April 22, 2011 | Sheet 85 of 109

SSID = VIDEO





	PX_EN	8209A_EN/DEM_VGA	1D5V_VGA_PWOK_R	PX_EN#	PX_EN##
Non-BACO	0	1	1	0	1
BACO	1	0	0	1	0

<Core Design>

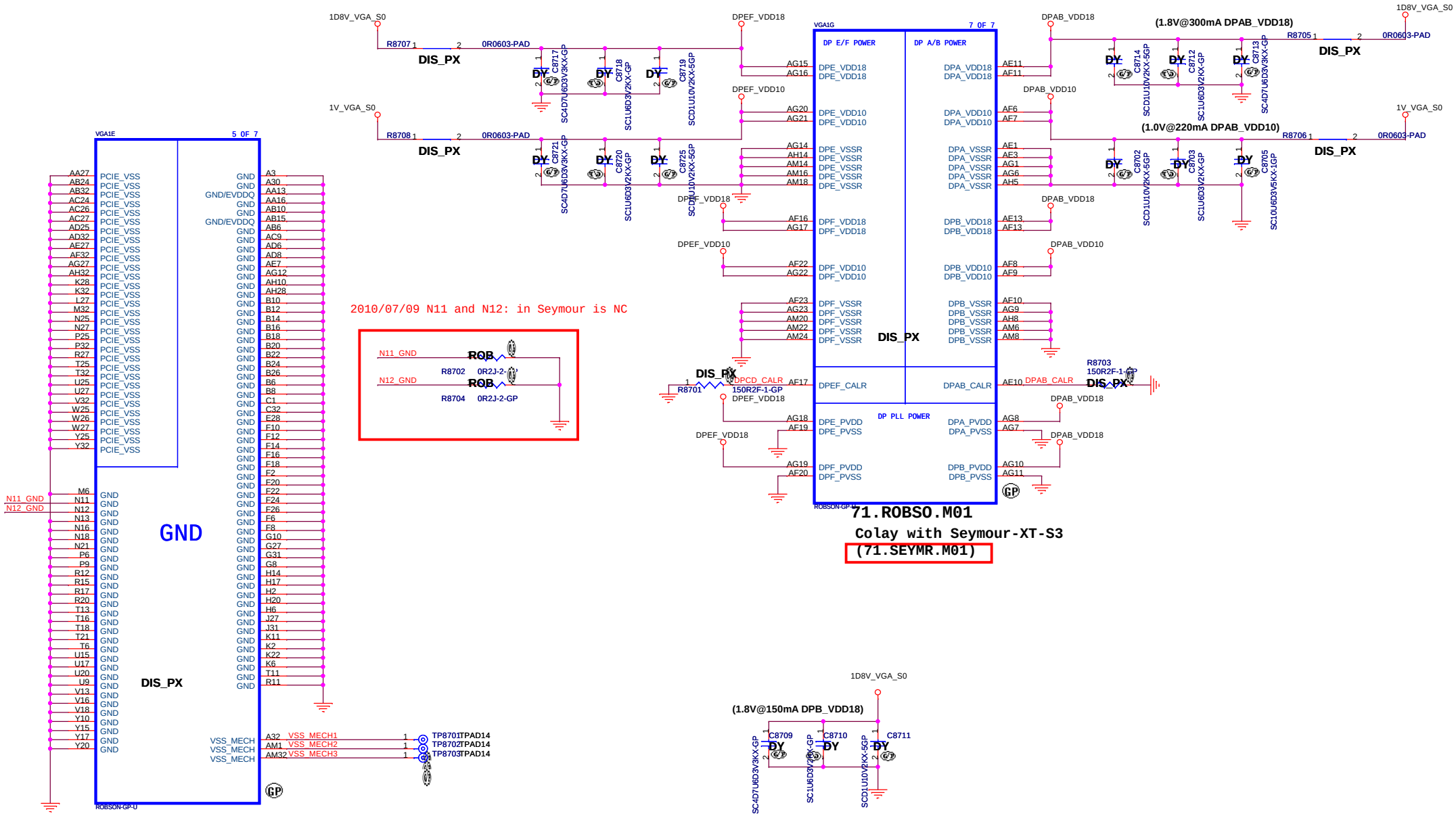
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER(4/5)

Size: A2 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 86 of 109

SSID = VIDEO



<Core Design>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	GPU_DPPWR/GND(5/5)
Size: A3	Document Number: Enrico 14 AMD
Rev: A00	
Date: Friday, April 22, 2011	Sheet 87 of 109

SSID = VIDEO

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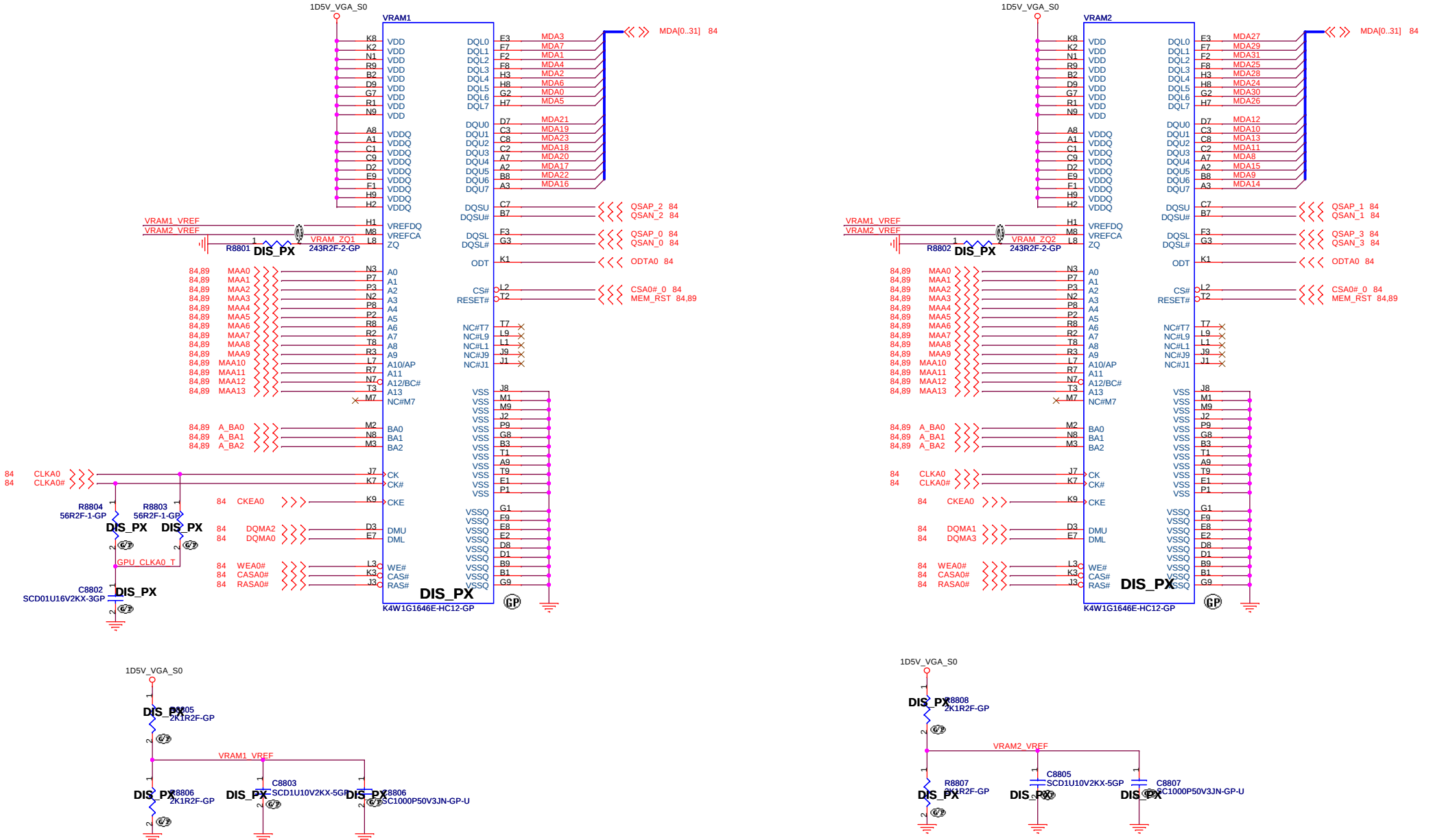


<Core Design>

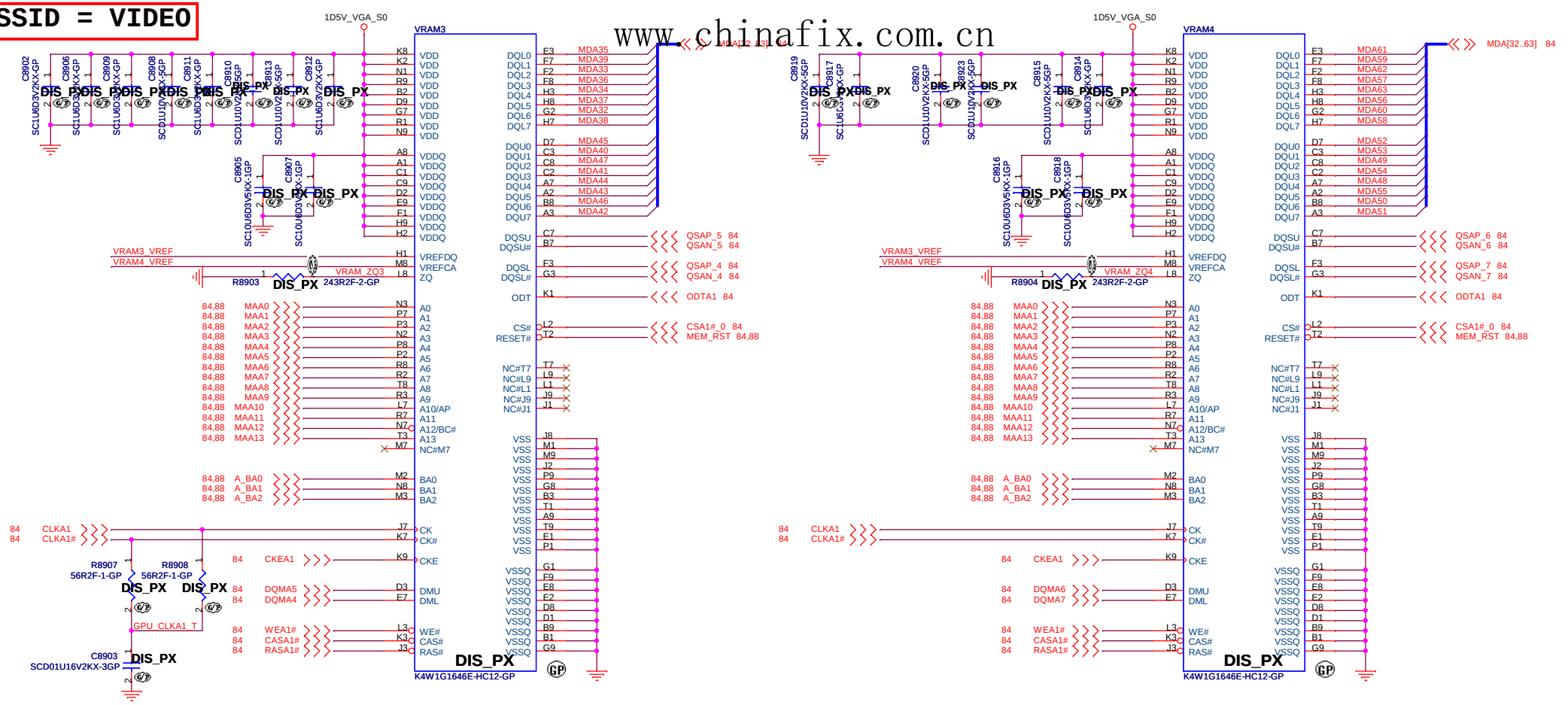
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

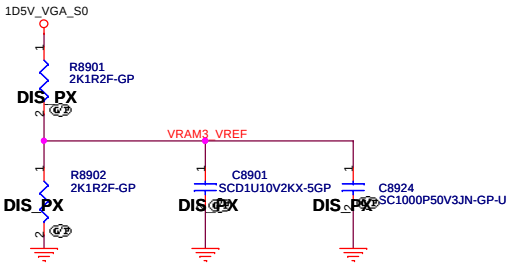
Title: GPU-VRAM1,2 (1/4)

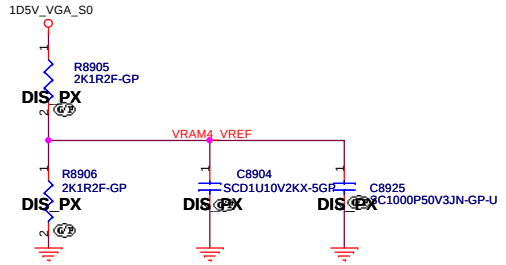
Size	Document Number	Rev
A3	Enrico 14 AMD	A00

Date: Friday, April 22, 2011 Sheet 88 of 109

SSID = VIDEO







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
A3	Enrico 14 AMD	A00

Date: Friday, April 22, 2011 Sheet 89 of 109

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 90 of 109

(Blanking)

<Core Design>

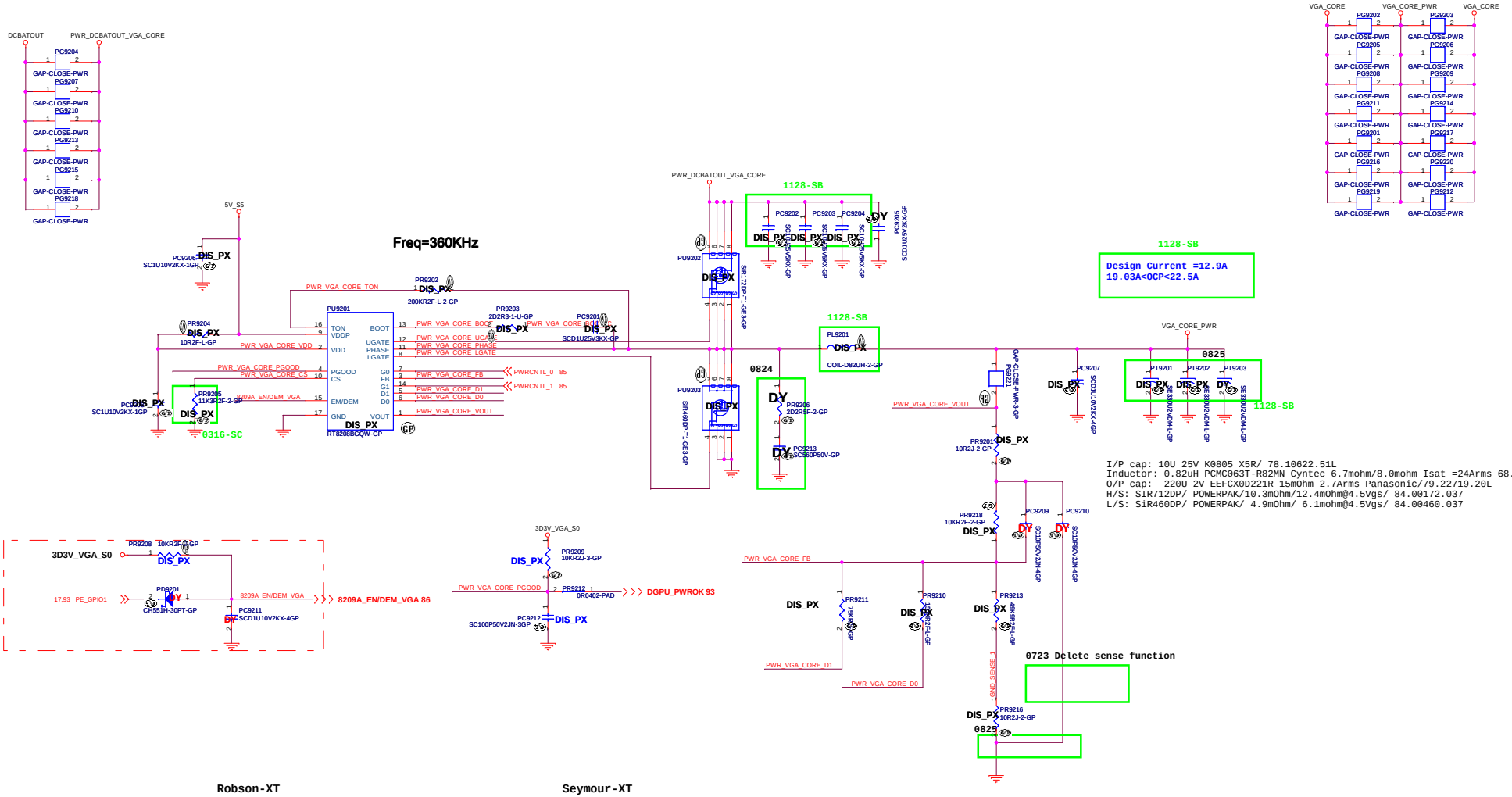
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (4/4)

Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 91 of 109

SSID = PWR.Plane.Regulator_VGACORE



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 0.82uH PCMC063T-R82MN Cyntec 6.7mohm/8.0mohm Isat =24Arms 68.R8210.10V
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms Panasonic/79.22719.20L
H/S: SIR712DP/ POWERPAK/10.3mOhm/12.4mOhm@4.5Vgs/ 84.00172.037
L/S: SiR460DP/ POWERPAK/ 4.9mOhm/ 6.1mohm@4.5Vgs/ 84.00460.037

Robson-XT

PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
L	L	1.12V
L	H	N/A
H	L	0.95V
H	H	0.9V

Vout=0.75V*(R1+R2)/R2

For ROBSON
PR9210=44.2K(64.44225.6DL)
PR9211=150K(64.15035.6DL)

Seymour-XT

PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
L	L	1.05V
L	H	1V
H	L	N/A
H	H	0.9V

Vout=0.75V*(R1+R2)/R2

For Seymour
PR9210=150K(64.15035.6DL)
PR9211=75K(64.75025.6DL)

X01

<Core Design>

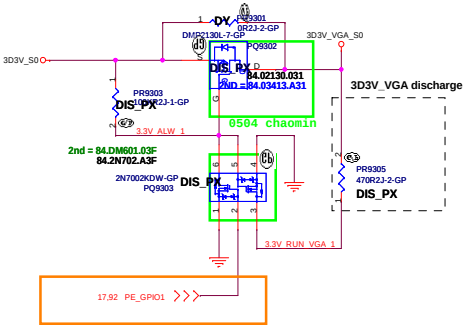
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208B_+VGA_CORE

Size	Document Number	Rev
A2	Enrico 14 AMD	A00

Date: Friday, April 22, 2011 Sheet 23 of 49

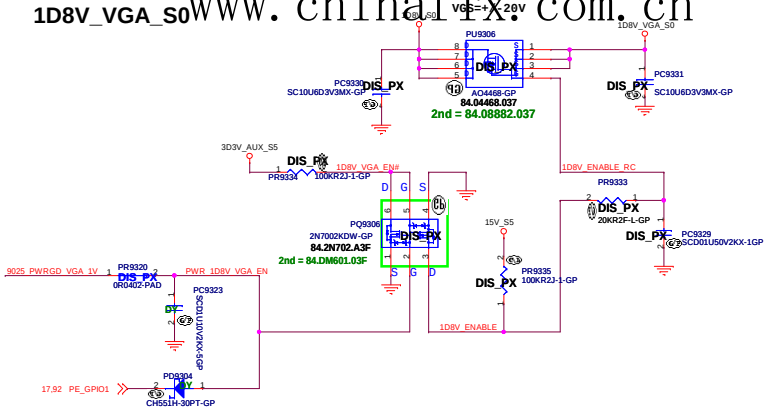
+3VS to 3.3V_DELAY Transfer



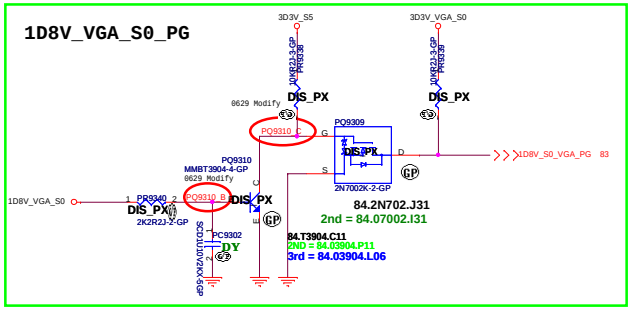
Different To Intel, AMD Is High Active

	PE_GPIO0	PE_GPIO1
dGPU mode	H	H
IGPU	L	L
IGPU with BACO	H	H

1D8V_VGA_S0



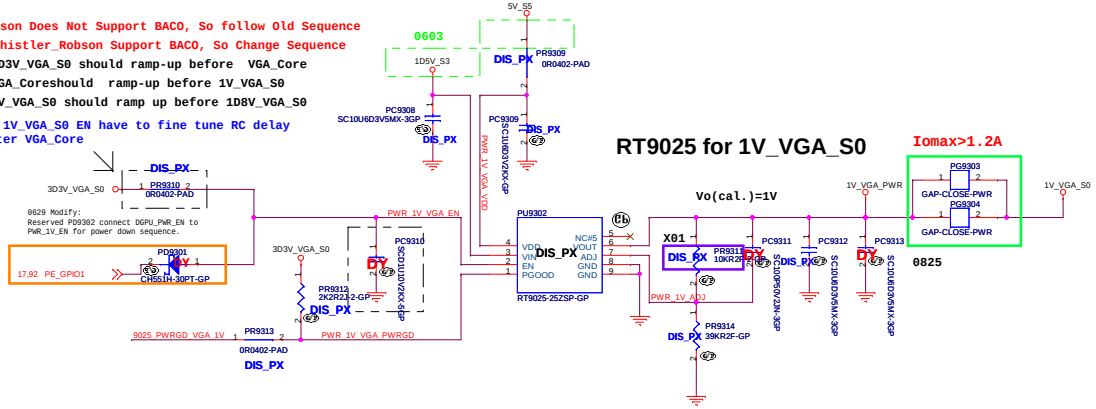
1D8V_VGA_S0_PG



Park_Madison Does Not Support BACO, So follow Old Sequence
Seymour_Whistler_Robson Support BACO, So Change Sequence

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Coreshould ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

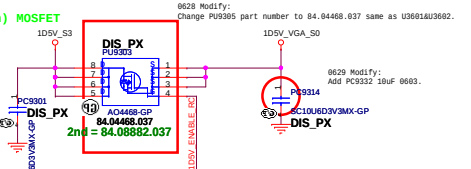


RT9025 for 1V_VGA_S0

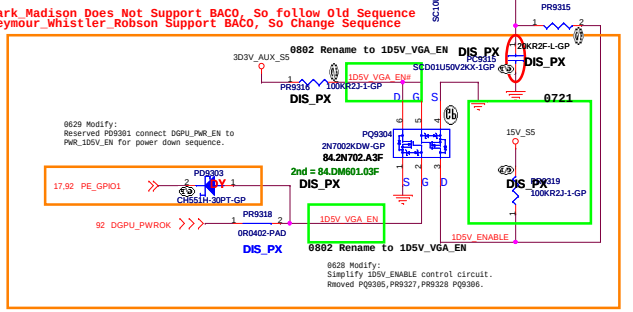
1D5V_VGA_S0

change low Rds(on) MOSFET

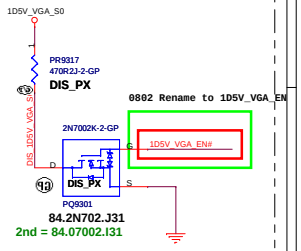
AO4468 MAX 11.6A
Rds(on) = 11~14mOhm
VGS=+/-20V



Park_Madison Does Not Support BACO, So follow Old Sequence
Seymour_Whistler_Robson Support BACO, So Change Sequence



Discharge Circuit



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size	Document Number	Rev
A2	Enrico 14 AMD	A00

Date: Friday, April 22, 2011 Sheet 93 of 109

SSID = VIDEO

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LVDS_Switch*

Size	Document Number	Rev
	Enrico 14 AMD	*A00*

Date: Friday, April 22, 2011 Sheet 94 of 109

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<Core Design>

Wistron Corporation

Reserved

Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 29, 2011 | Sheet 1 of 1

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

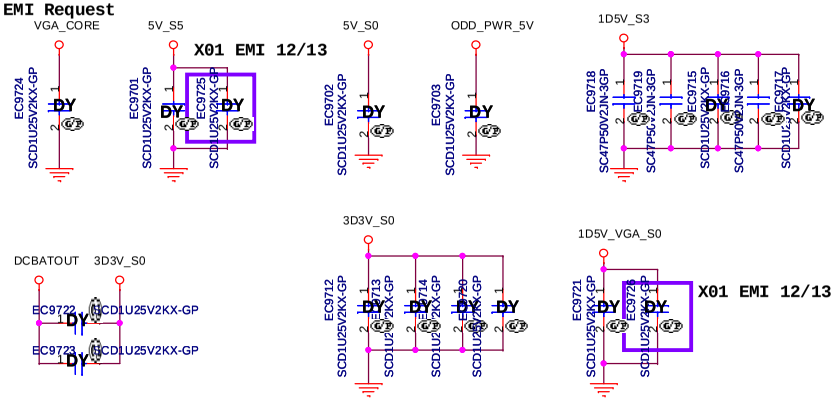
Title: *Touch Panel*

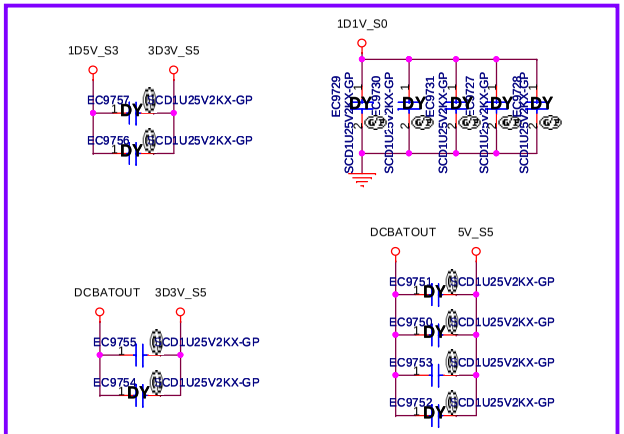
Size: A3 | Document Number: *Enrico 14 AMD* | Rev: *A00*

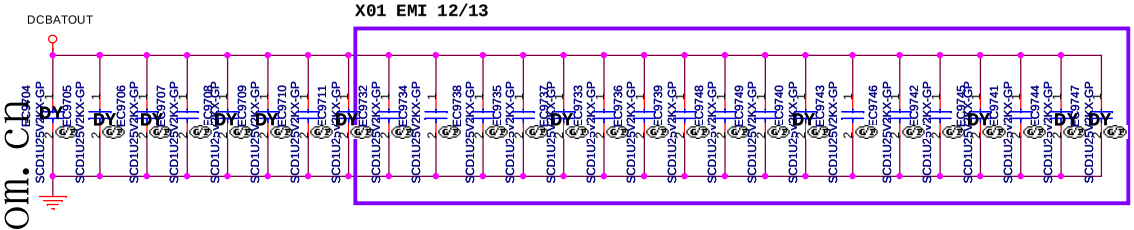
Date: Friday, April 22, 2011 | Sheet 96 of 109

0824 EMI Request

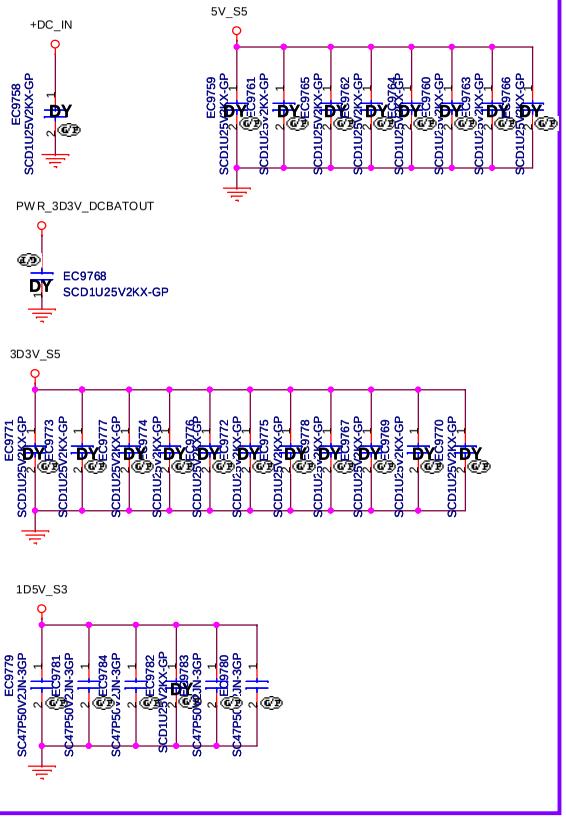
X01 EMI 12/13

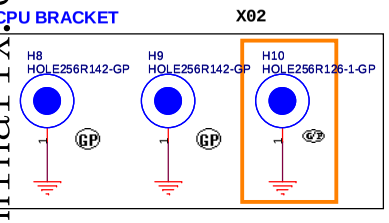


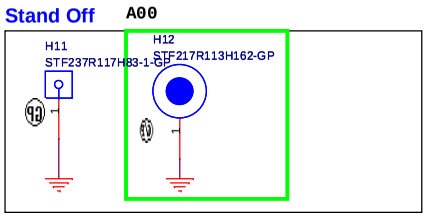


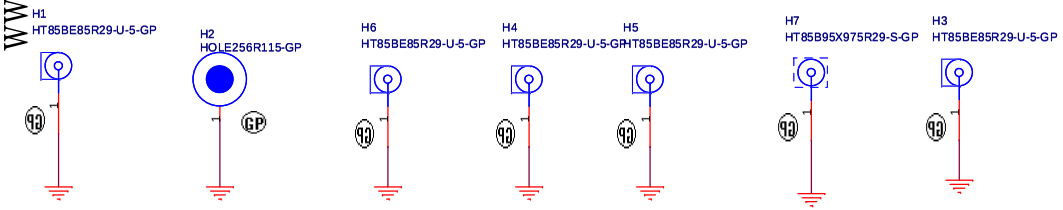


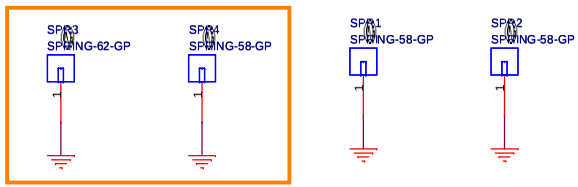
X01 EMI 12/16











<Core Design>

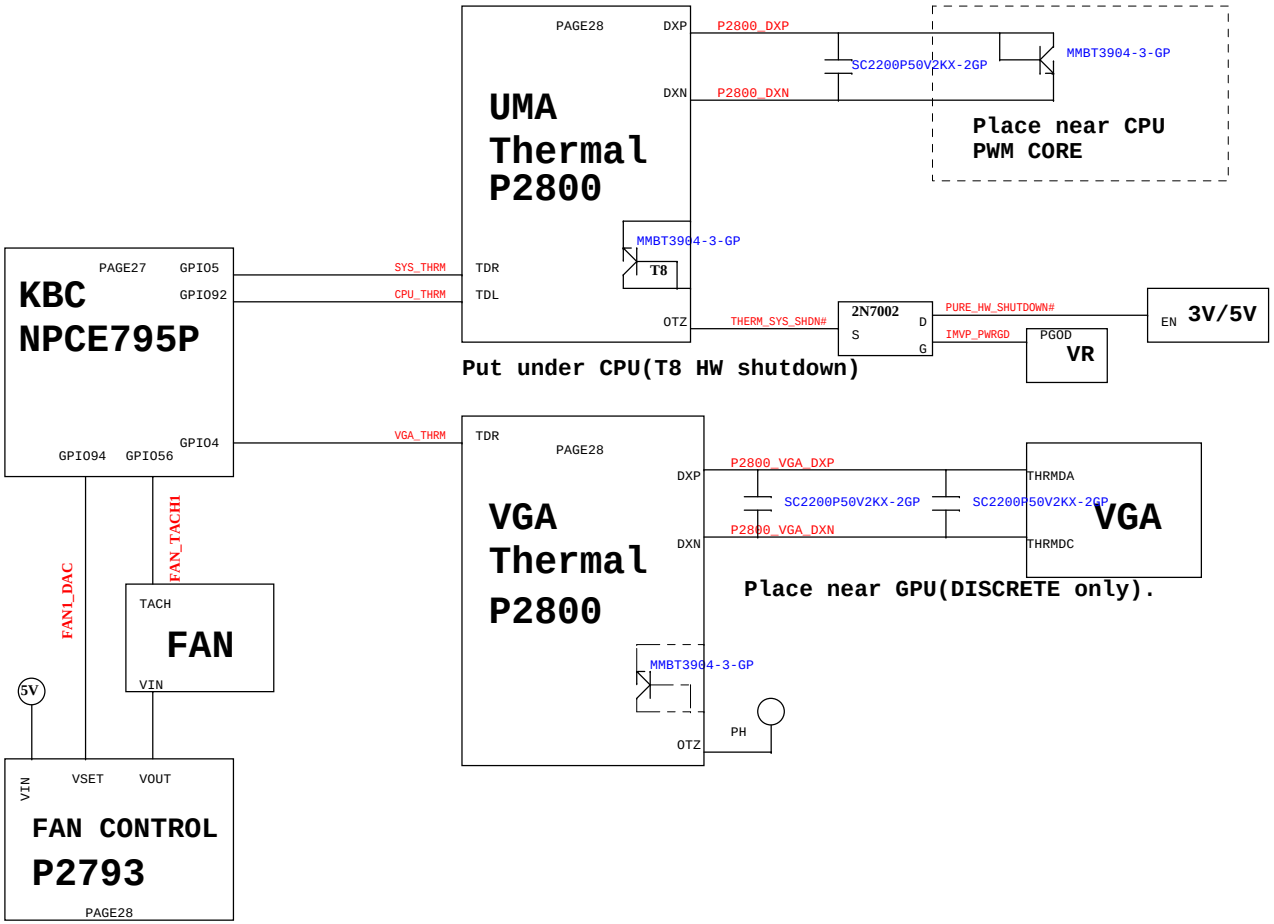
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/CAP

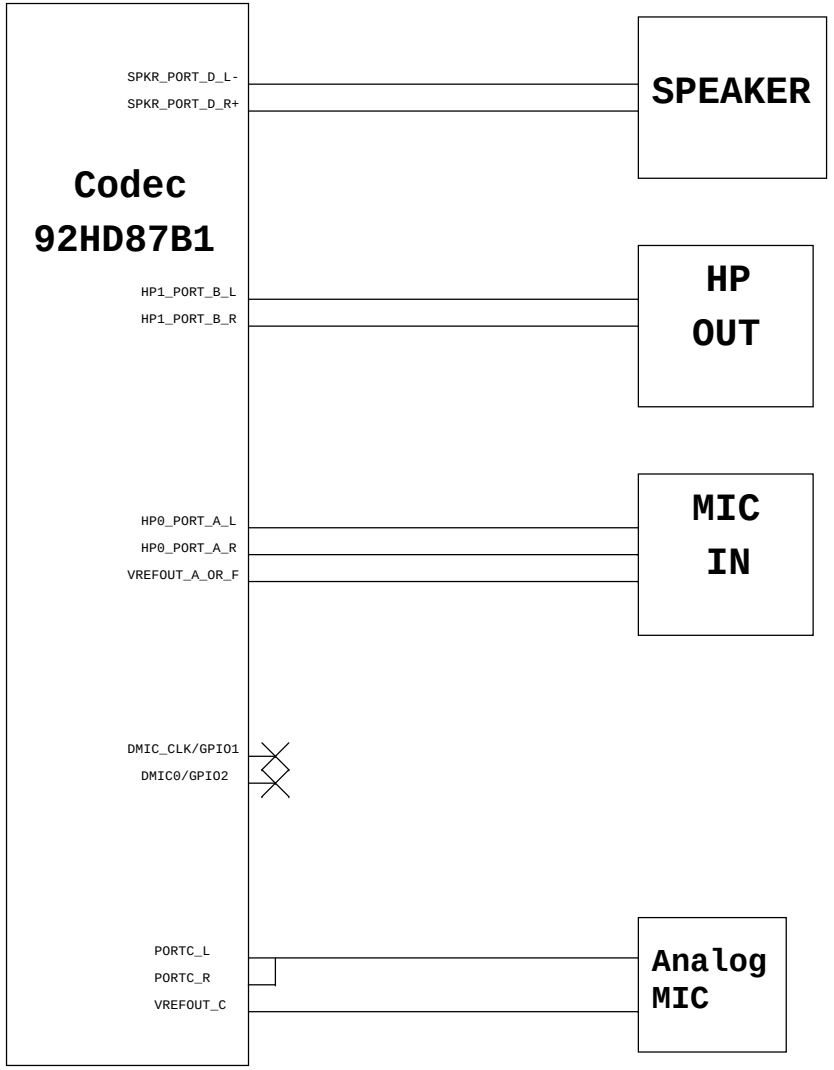
Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 97 of 109

Thermal Block Diagram



Audio Block Diagram



<Core Design>

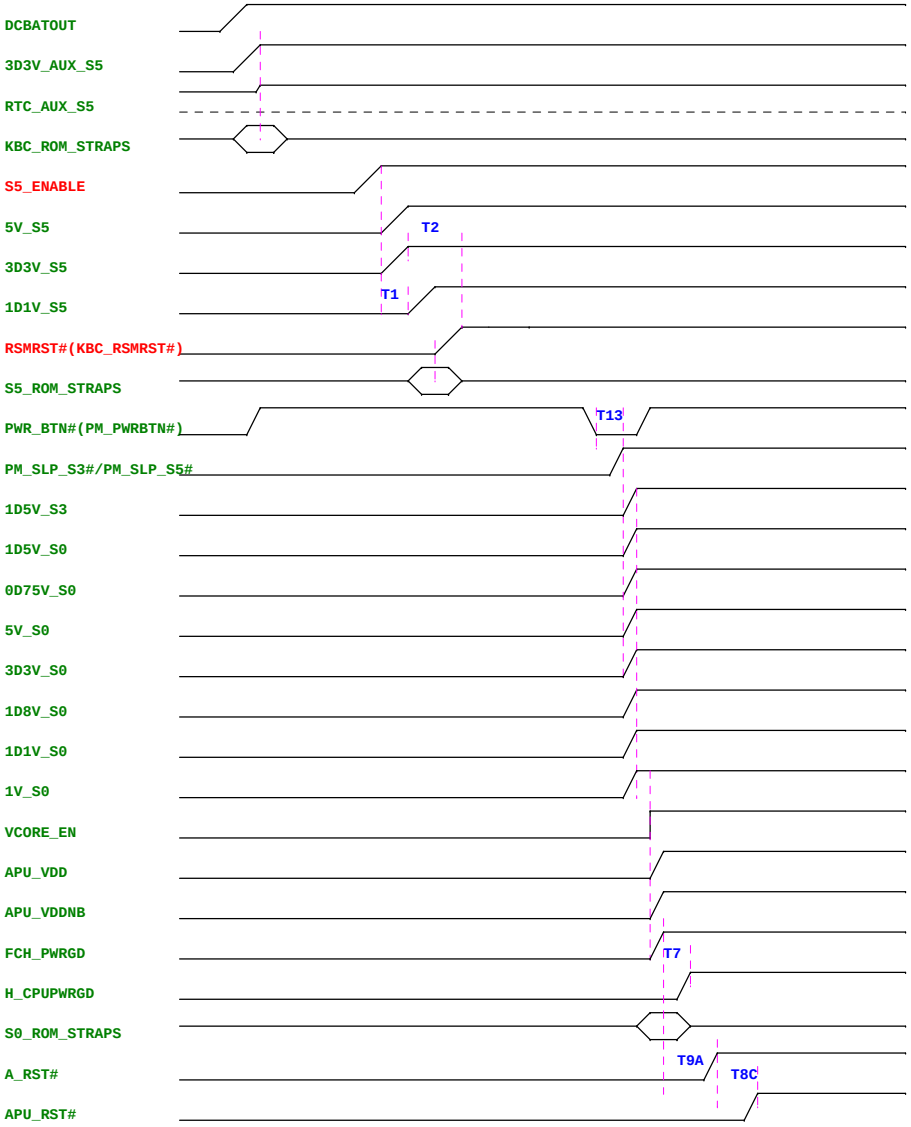
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL/AUDIO BLOCK DIAGRAM

Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 98 of 109

POWER SEQUENCE



	Min	Max	Description
T1	-	-	+3.3V_S5 to +1.1V_S5
T2	10 ms	-	+3.3V_S5 to resume reset (RSMRST#).
T7	98 ms	150 ms	FCH PWRGOOD assertion to LDT_PG assertion delay.
T8C	1.0 ms	2.3 ms	PCIRST# to LDT_RST#.
T9A	101 ms	113 ms	FCH PWR_GOOD to A_RST#.
T13	8 ns	-	PwrButton to SLP_S3# / SLP_S5# de-assertion

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER SEQUENCE

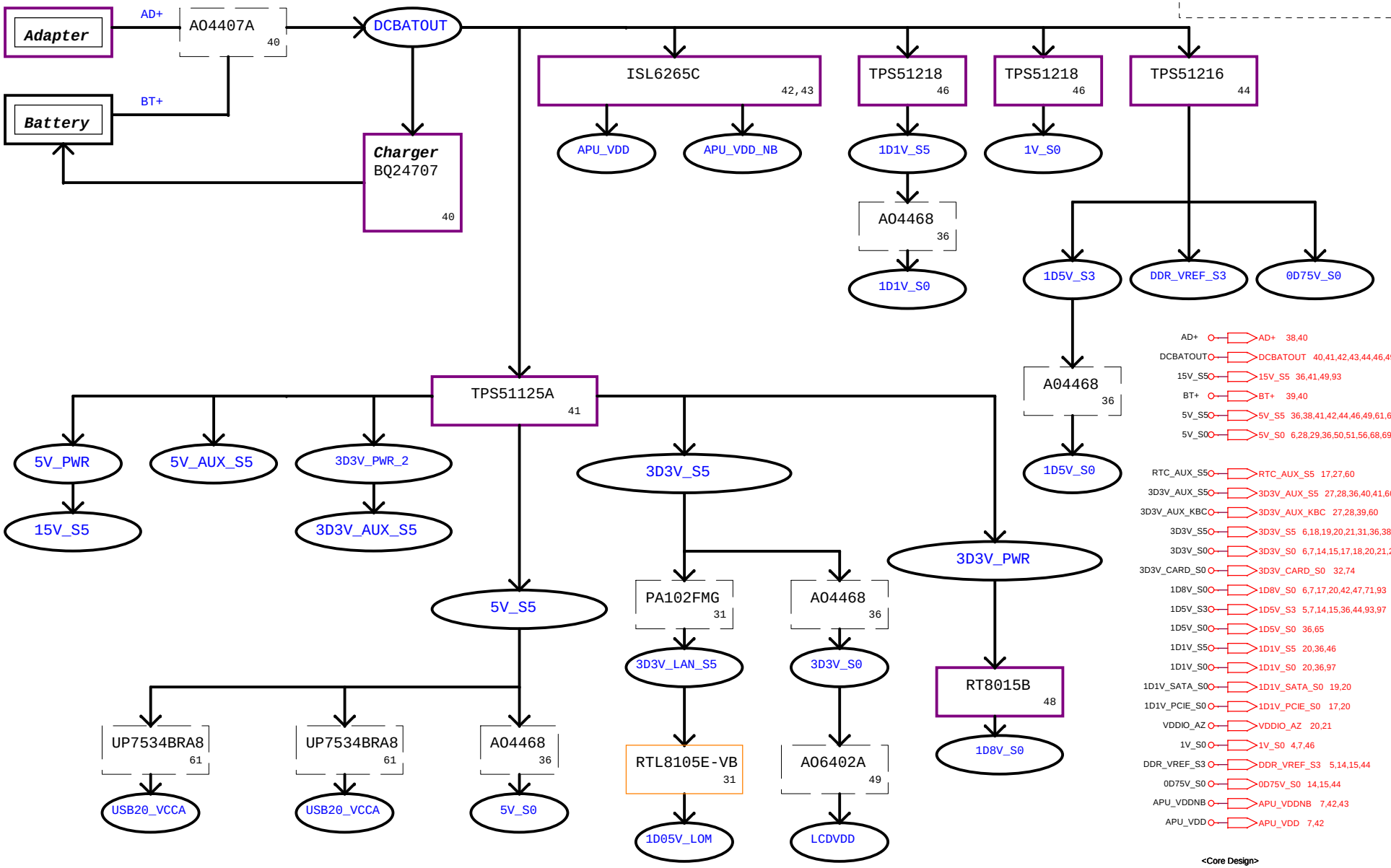
Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 99 of 109

Power Delivery Block Diagram

Power Shape

Regulator | LDO | Switch



AD+ → AD+ 38,40
DCBATOUT → DCBATOUT 40,41,42,43,44,46,49,92,97
15V_S5 → 15V_S5 36,41,49,93
BT+ → BT+ 39,40
5V_S5 → 5V_S5 36,38,41,42,44,46,49,61,65,68,69,92,93,97
5V_S0 → 5V_S0 6,28,29,36,50,51,56,68,69,86,97

RTC_AUX_S5 → RTC_AUX_S5 17,27,60
3D3V_AUX_S5 → 3D3V_AUX_S5 27,28,36,40,41,60,93
3D3V_AUX_KBC → 3D3V_AUX_KBC 27,28,39,60
3D3V_S5 → 3D3V_S5 6,18,19,20,21,31,36,38,41,42,44,46,47,60,70,82,86,93,97
3D3V_S0 → 3D3V_S0 6,7,14,15,17,18,20,21,27,28,29,31,32,36,42,49,56,60,65,71,93,97
3D3V_CARD_S0 → 3D3V_CARD_S0 32,74
1D8V_S0 → 1D8V_S0 6,7,17,20,42,47,71,93
1D5V_S3 → 1D5V_S3 5,7,14,15,36,44,93,97
1D5V_S0 → 1D5V_S0 36,65
1D1V_S5 → 1D1V_S5 20,36,46
1D1V_S0 → 1D1V_S0 20,36,97
1D1V_SATA_S0 → 1D1V_SATA_S0 19,20
1D1V_PCIE_S0 → 1D1V_PCIE_S0 17,20
VDDIO_AZ → VDDIO_AZ 20,21
1V_S0 → 1V_S0 4,7,46
DDR_VREF_S3 → DDR_VREF_S3 5,14,15,44
0D75V_S0 → 0D75V_S0 14,15,44
APU_VDDNB → APU_VDDNB 7,42,43
APU_VDD → APU_VDD 7,42

<Core Design>

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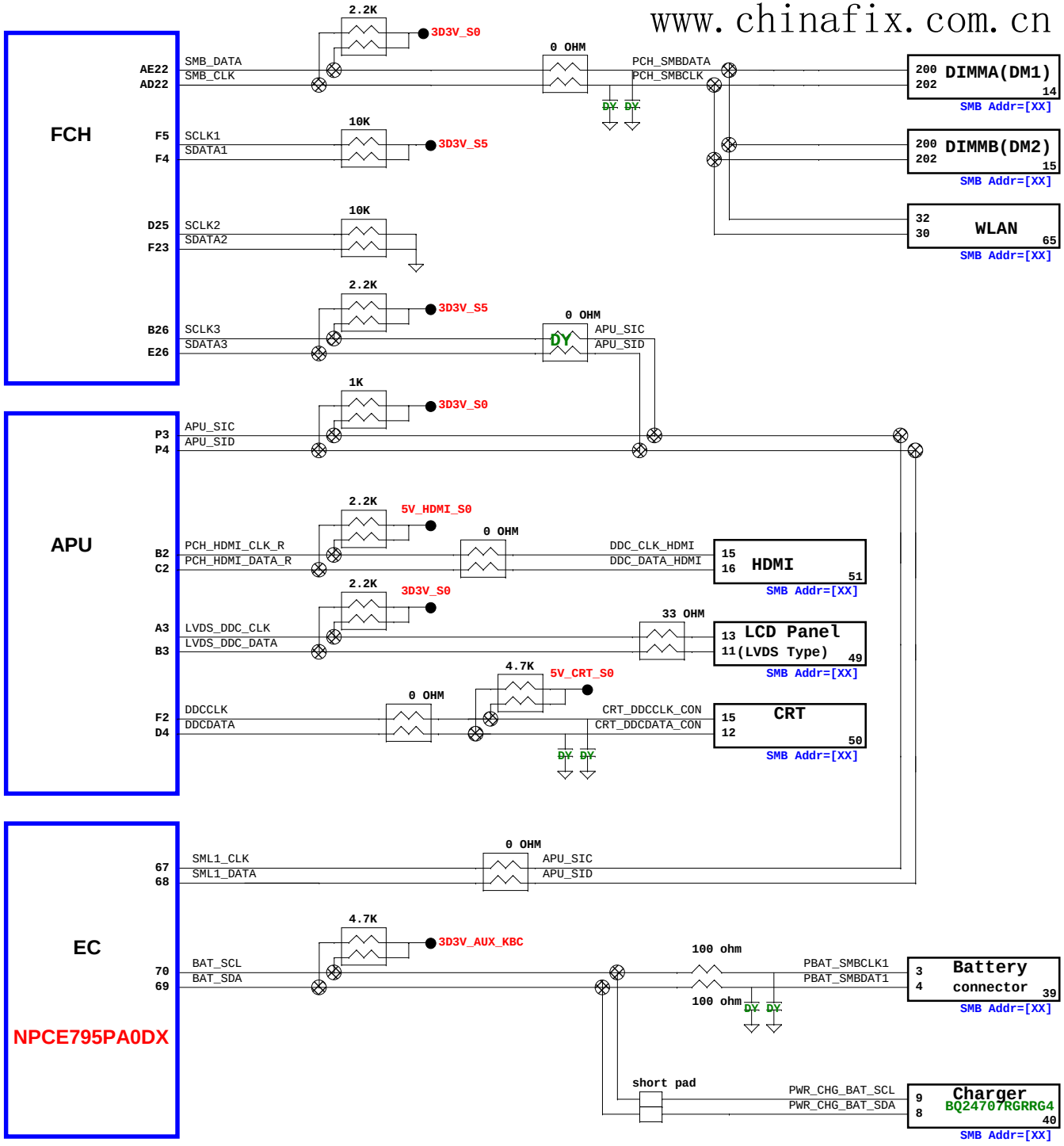
Title: Power Block Diagram		
Size: A3	Document Number: Enrico 14 AMD	Rev: A00
Date: Friday, April 22, 2011	Sheet 100 of 109	



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Title: SMBUS BLOCK DIAGRAM

Size	Document Number	Rev
A2	Enrico 14 AMD	A00

Date: Friday, April 22, 2011 Sheet 101 of 109

Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER
	X01	9/23	50	Delete F5001, Share Fuse with HDMI	EE
			71	DUMMY Debug Port DB1,RN7102, R7107	EE
			27	Change R2724 value to 20K, X01 Version	EE
			39,56	Change BATT1,ODD1,HDD1 Connector	ME
			27	Add C2722 0.1uF between Q2703 G&S pin for fixed leakage voltage to 3D3V_AUX_KBC under DC mode.	EE
			27	Add Q2706 2N7002 to avoid leakage loop from 3D3V_S5 to 3D3V_AUX_KBC issue when 10mW latched fail timing. Un-stuff C2713 to follow the standard schematics.	EE
			28	Change U2801, U2803 to 74.02800.A71	EE
	X01	9/29	61	Change U6102 to 74.07534.079	EE
			50	Change L5001,L5002,L5003 bead to 0402 size:68.00217.991	EE
			38,59,69, 82	Change DCIN1,RJ45,TPAD1,IOBD1 Connector	ME
			82	Change IOBD1 Pin define	EE
	X01	10/13	6	Dummy APU_SIC, APU_SID level shifter, pop R644,R645	EE
			6	Add level shifter for H_Thermtrip#	EE
			36	DUMMY Q3601,R3622 for reserved	EE
			28	Change R2816,R2822 to 107KR,R2817 ,R2821to 226KR for new version P2800 chip	EE
			39	Delete R3901 for double pull high	EE
			49	Delete R4902 for double resister	EE
			27	Change PURE_HW_SHUTDOWN#(R2705) power rail to 3D3V_AUX_KBC	EE
	X01	10/20	92	Change PR9213 to 75K, PR9211 to 150K for VGA_CORE (Robson-LP)Output	Power
			27,36	Add GPIO97 for IMVP_PWRGD control ,Change D3605.2 to 1V_S0_PWRGD,Delete D3606, Change D3603.1 to VRM_VDD_PWRGD for sequence	EE
			86	Modify 1D5V_VGA_PWRGD to 1D5V_VGA_PWOK	EE
			31	Dummy R3101,R3102,Q3101,R3108 for leakage	EE
			36,47	Change R3607 to 10K,C3605 to 15n,PR4711 to 0ohm, PC4710 DY, C3610 DY, R3633 to 33K, C3615 to 33n,R3604 to33K for sequence	EE

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Title: Change notes

Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 102 of 109

Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER
	X01	10/20	20	Change R2004 to 0603 size for current tolerance	EE
			93	Change PR9311 to 10K for 1V_VGA Voltage	Power
			61,65	Add C6105,C6106,C6509,C6510 to 6.8p for solve SIV USB fail	EE
			27	Change RN2705 8P4R to 4P2R and R2715, RN2705 DY	EE
			40	Add PR4061 PR4062 100KR, empty other parts for fine tune sequence for leakage	EE
		10/27	85,17	Modify C8524,C8525=12p, C1715,C1717=18p for crystal frequence match	EE
			68	Add LED for WLAN	EE
			14	Change RN1401 to 22 ohm and pop C1423,C1424 for solved SMBus SIV Fail	EE
		11/10	38	Change DCIN CONN pin define	EE
			31	Solved leakage issue follow DV15	EE
			68	Modify Wireless LED schematic	EE
			85	Change L8502,L8503,L8507,L8505,L8513 to short pad for power	EE
			17,31	Modify C1720=15p, C3102=15p for crystal frequence match	EE
			28	Add G709 for thermal solution	EE
			68	Delete RN6802,RN6801	EE
			83~89	Change GPU from Robson LP to Seymour XT	EE
		11/17	46	DY 1V to merge 1D1V	EE
			27	Add two model ID for config	EE
			58	Delete MIC2 and move mic1 to IO Board	EE
			92	Update Seymour and Robson power plan setting(PR9219,PR9210,PR9214,PR9211)	EE
			87	Pop R8421 for check list request	EE
			68	Modify power LED schematic and charger LEDs	EE
				Merge with power schematic	Power
			27	Add LID_CLOSE# pull high	EE

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Title		
Change notes		
Size A3	Document Number Enrico 14 AMD	Rev A00
Date: Friday, April 22, 2011	Sheet 103 of 109	

Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER
			50,51	Modift CRT,HDMI share fuse schematic	EE
	X01	11/24	31	Change L3101 to slime type and add R3101 GIGA mark for 10/100 internal PU	EE
			27	Change R2726, R2710 to F tolerance for accurate level to KBC	EE
			27,65,68	Change WLAN LED design to meet on/off behavior SPEC	EE
			27	Change RTC_POWER from RTC_AUX_S5 to 3D3V_AUX_S5 for saving RCT power and no influence on PSL	EE
			6	Pull up LTDP0_HPD to 5V from AMD SCL 1.04	EE
			6	Change RN634 to 2K2R follow AMD SCL 1.03	EE
			6	Add level shifter for LVDS SMBus follow AMD SCL 1.04	EE
			59	Rename part reference for Lan ESD	EMI
			31	Set R3101 BOM option for 8105E DY	EE
			31	Add RTC sense schematic	EE
		12/2	27	Reserved R2778 for EC power switch logic circuit.	EE
			27	Set R2769 empty, Duplicated function in page 40.	EE
			28	Reserve R2861 for hysteresis	EE
			36	Reserve C3633 for power up sequence tunning	EE
			49	Modify TP4906,TP4907 to AFTP	EE
			17,31	Change 25MHZ, 32.768K to small size by source recommand	Sourcer
			2	Modify Block Diagram	EE
			36	Change U3606 P/N	EE
			59	Modify Transformer schenatic from GIGA to 10/100 for latest config	EE
			6	Remove level shifter for LVDS SMBus(AMD confirm)	EE
			40	Reserve snuber 2.2ohm+560p for EMI solution	EMI
			50	Change L5001,L5002 and L5003 from 220hm to 30ohm for EMI Solution	EMI
			50	Change 2N7002E to 2N7002K for EOL	Sourcer

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Title: Change notes

Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 104 of 109

Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER
			27	Modify R2776 to 64.9K	EE
			59	Modify R5903,R5904 to 0603 size	EE
			27	Change R2739 to 1% tolerance	EE
			6	Change RN634 form 2.2KR to 1KR by AMD suggestion	EE
			65,68	Change WLAN LED indicator for reserve EC and module circuit	EE
			60	Change Q6001.G from +RTC_VCC to RTC_PWR	EE
			15	Reserve R1531 and R1532 69.8R for memory glitch issue	EE
			36,46	Stuff 0R and change to open-gap for merge power rail	EE
			47	Change PQ4701 to ESD 2KV for Vendor EOL	EE
			38,39	PD3801 change to P6SMBJ58A,PD3902 change to SMF18AT1G	Power
			40	Add PQ4007 PR4012 and PR4037 to improve AC_IN# delay issue	Power
			All	Change reference from PTCxx to PTxx for meet SMT Process	Power
			41,42,44, 46,92	Change PC4111,PC4116,PC4117,PC4204,PC4223,PC4203,PC4301,PC4302,PC4304,PC4403,PC4404,PC4405,PC4602,PC4603, PC4604,PC4613,PC4614,PC4618,PC9202,PC9203,PC9204 to 10u 0805 size	Power
			92	PR9205 change to 13 Kohm for OCP setting	Power
			6	Remove SIC,SID level shifter	EE
		12/7	36	Reserve 1V_S0_PWRGD link for 1V_S0 power rail	EE
			38	Change PD3801: 83.P6SMB.DAG(YS) change to 83.P6SBM.DAG(CHENMKO).	Power
			86	Change U8601.U8603,U8604,U8606 pin G to 5v_S0	EE
			28	Remove R2822,R2821,C2819 and NC U2803 OTZ pin	EE
			36	Dummy C3609	EE
			49	Change R4903,R4904 to 0603 size	EE
			17	Add RTC detect pin on REQ1#_GPIO40	EE
			61,65	Move C6105,C6106,C6509,C6510 to Connector side	EE
			61	Pop TC6102 and DY on IO Board side	EE

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Title: Change notes		
Size: A3	Document Number: Enrico 14 AMD	Rev: A00
Date: Friday, April 22, 2011	Sheet 105 of 109	

Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER
			71	Pop DB1,RN7102,R7107 for debug	EE
			74	DY EC7401,EC7403 for reserve	EE
			36,46	Add PC4621 and PT4603 1V_PWR and change 1V_S0 to 1V_PWR	EE
			14,59	Rename C59011 to C5901 and Change TC4101 to 79.22719.20L	EE
			46	Dummy 1V power generator foe back up solution	EE
			40	Add PR4063,PC4025 for EMI Snaber solution	EMC
		12/7_1	17	Reserve damping resistor R1766 for crystal drive level adjustment	EE
			65	Reserve BT_ACT for future module extension	EE
			69	Change KB connector	EE
		12/8	69	Add Caps led schematic and change AD_IA_HW2 to GPIO50, PCIE_RST# to GPIO36, CAP_LED change to GPIO30	EE
		12/10	27	Add R2780 and DY R2732,Q2702 for EC "PROCHOT_EC" pin from PP to OD type	EE
		12/13	68,82	Change IOBD2 and PWBTN1 pin define	EE
			38,40,41	PC3806 PC4006 PC4008 PC4110 and PC4114 change to 10uF 25V 0805 size (78.10622.51L)	Power
			28	Change U2801,U2803 to B version(74.02800.B71)	EE
			97	Add EMI Solution	EMI
		12/14	40	Change PC4004 and PC4024 from 1uF to 0.1uF (78.10424.2BL)	Power
			28	DY R2816,R2817,C2831 for set ADJ floating	EE
			61	DY TC6102 for reserve on IO board	EE
		12/15	82	Change IOBD2 pin define and connector	EE, ME
			20	Chnage R2004 to 0402 size	EE
			17	Change R1766 location and change to 1KR for Put Rd at chip output side and suppress amplitude.	EE
		12/17	6,65	Swap RN605,TR6501 for Layout	EE
			97	Add EMI Solution	EMI
			36	Change C3615 tolerance from 16V to 25V for component derating high voltage tolerance	EE

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Title: Change notes

Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 106 of 109

Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER
			36	Delete R2779 for LID_Close# double pull high	EE
		12/21	59	Change C5904 to 0.01u from vendor recommand	EE
			50	Modify CRT Hsync & Vsync level shift follow DV15	EE
			46	Modify 1V_S0 Schematic	EE
		12/21_1	42	DY PR4214,PR4402 for pull up on R3624	EE
		12/22	61	DY C6104,C6108	EE
		12/22_1	56	Change HDD1 CONN to 62.10065.H71	ME
			61	DY TC6101, Stuff TC6103	EE
		12/23	20	Change to 10u 0805 size	EE
		12/23_1		Implement OPI Solution	EE
		12/27		Crooect VGA setting, PR9210:150K, PR9211:75K	EE
	X02	03/03	41	Change PR4104 to 0 ohm,PR4106 to 200K	EE
			83	DY R8309,R8310 to solve device error	EE
			31	Move C3125 to Q3101.S ,R3134 to 100k to solve unnecessary pulse	EE
				Change C3102,C3103 to 18P from vendor recommand	EE
			17	Change RN1701 to 22 ohm for solve SIV solution	EE
			50	Change RN5001 to 150 ohm for solve SIV solution	EE
				Stuff C5002,C5003,C5004	EE
			97	Add SPR3,SPR4	ME
			59	Add RN5901 for nonuse Giga lan	EE
			50,59,97	Change CRT ,TPAD1,RJ45 CONN, H10 Hole and add SPR3,SPR4	ME
		03/07	83~87	Change VGA P/N to 71.ROBSO.M01	EE
			85	DY R8525,R8526 and Q8501 for nonuse	EE
			28	DY R2813,R2805,R2832,C2808,U2805,R2812,R2811, Stuff R2823 for P2800	EE

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Title: Change notes

Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 107 of 109

Change notes -

VERSON	DATE	Page	Modify List	OWNER
		28,85	DY U2803,R2815,R2812,R2814,C2813,C2814. stuff RN8501,Q8503 for GPU temperature by SMBus	EE
	03/09	27	DY D2701,D2704 and D2705, Add R2781,R2782 and R2783 for connect directly	EE
		97	Change SPR3 to 34.39S07.003	EE
		38,39	Rename AFPP3811,3812,3813,3814,3901,3902,3903,3904 to AFTP	EE
	03/10	38,60	Delete AFTP6001,AFTP6002,AFTP3811	EE
		17	Change C1719,C1720 to 18p for vendor recommand	EE
		40	Delete PR4063 and PC4025 for EMI Solution	EE
	03/10_1	71	Add R7102 to reserved	EE
		27	Change R2724 to 33k for SC PCB version	EE
		31	Add RN3101,Q3104 and R3108 to solve Lan leakage issue	EE
	03/11	41,42,47	Change power gap P/N	EE
			Change 0 ohm to short pad	EE
		61,65,82	Delete TR6101,TR6501,TR8202,TR8201 CMC	EE
	03/16	41	Change PR4103 from 150Kohm to 143Kohm for 5V OCP setting	Power
		44	Change PR4408 from 75Kohm to 66.5Kohm for 1.5V OCP setting	Power
		92	Change PR9205 from 13Kohm to 11 Kohm for VGA OCP setting	Power
		47	Change PC4709 from 1.5KpF to 100pF for comp	Power
		46	Dummy PC4602 and POP PC4604.	Power
	03/17	28	DY C2818,D2802,C2816 and Stuff C2815	EE
	03/22	40	DY PQ4007,PR4037,PR4012 for new version IC	EE
A00	04/07	49	Add 0 ohm at Q4901.4 for reserved to avoid module leakage	EE
		71	Change DB1 foorprint to PAD-10P-177042 for factory request	EE
		18	Change R1818 to 0 ohm for reserved non-zero power ODD	EE
	04/11	18	Change R2724 to 47K for X-build version	EE

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Title: Change notes		
Size: A3	Document Number: Enrico 14 AMD	Rev: A00
Date: Friday, April 22, 2011	Sheet 108 of 109	

Change notes -

VERSON	DATE	Page	Modify List	OWNER
	4/12	40	DY PR4029,PR4028,PQ4004 and PQ4006 for nouse because just use 65W adapter	EE
		40	Change C8617 to 10u for CRB to avoid voltage drop	EE
		20	DY C2005,C2007, and add R2030 for nonuse	EE
		97	Change H12,H13 to 34.4HL17.001 for ME asked	ME
	4/12_1	97	Delete H13 for ME asked	ME
		18	Change EC1801 to 22p for EMI solution	EMC
	4/13	68	Change R6806,R6812,R6801,R6833 to 330 ohm for brightness	EE
	4/15	56	DY R5612, Pop Q5602 for modify Zero power ODD	EE
		51	Chnage RN5004 to ZZ.0R08P.ZHH to modify layout symbol is short pad	EE
	4/17	28	Change R2817 to 0 ohm for setting T8 temperature from 85 to 90 degree to pass reliability test	EE
	4/21	56	DY U5601,TC5604,R5606,Q5601,R1818,R5612, Stuff R5604,R5603 for remove Zero power ODD	EE

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Title: Change notes

Size: A3 | Document Number: Enrico 14 AMD | Rev: A00

Date: Friday, April 22, 2011 | Sheet 109 of 109