

# Compal confidential

## Schematics Document

### Mobile Yonah uFCPGA with Intel Calistoga\_PM+ICH7-M core logic

2005-08-26

REV:0.2

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Model:HAQAA

File Name : LA-3011P

# NAPA

*Mobile Yonah*

*uFCPGA-479 CPU*

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*Thermal Sensor*  
*ADM1032AR*

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*Clock Generator*  
*ICS9LPRS325AKLFT*

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*Accelerometer*  
*LIS3L02AQ3TR*

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*H\_A#(3..31)*

*FSB*

533/667MHz

*H\_D#(0..63)*

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*Dual Channel*

*DDR2-SO-DIMM X2*  
*BANK 0, 1, 2, 3*

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*945PM*

*PCBGA 1466*

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*PCI-E BUS*

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*CardBus Controller*  
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*5in1 Slot*

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*Intel ICH7-M*

*mBGA-652*

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*USB2.0*

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*Audio CKT*  
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*AMP & Audio Jack*  
*TPA0232*

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*MDC1.5*

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*USB conn x1*  
*(Docking)*

(port 6)

*USB2.0 HUB /*  
*FP Conn*

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(port 4,5)

*BT Conn*

(port 7)

*USB conn x2*  
*(Sub Board)*

(port 2,3)

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*USBx1*

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*LPC BUS*

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*Power On/Off CKT.*

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*Power Circuit DC/DC*

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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (18.5V)	NA	NA	NA
B+	AC or battery power rail for power circuit	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V power rail for Processor I/O and MCH/ICH core power	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDRII Vtt	ON	OFF	OFF
+1.5VS	1.5V switched power rail for PCI-E interface	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail for MCH video PLL	ON	OFF	OFF
+2.5VALW	3.3V always on power rail	ON	ON	ON*
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_VCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

Internal PCI Devices

DEVICE	Bus	PCI Device ID	IDSEL #
LAN	1	D8	AD24
Azalia	0	D27	AD11
PCI-E	0	D28	AD12
USB1.1/2.0	0	D29	AD13
PCI to PCI (DMI to PCI)	0	D30	AD14
AC97 MODEM	0	D30	AD14
AC97 Audio	0	D30	AD14
PATA/SATA	0	D31	AD15
LPC I/F	0	D31	AD15
SMBUS	0	D31	AD15
CPU I/F	0	D31	AD15
DMA	0	D31	AD15
PMU	0	D31	AD15

External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
CARD BUS	D6	AD22	2	ABCD

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 1%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0.100 V
1	8.2K +/- 1%	0.216 V	0.250 V	0.289 V
2	18K +/- 1%	0.436 V	0.503 V	0.538 V
3	33K +/- 1%	0.712 V	0.819 V	0.875 V
4	56K +/- 1%	1.036 V	1.185 V	1.264 V
5	100K +/- 1%	1.453 V	1.650 V	1.759 V
6	200K +/- 1%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

SKU ID Table

SKU ID	SKU
0	
1	
2	
3	
4	
5	
6	
7	

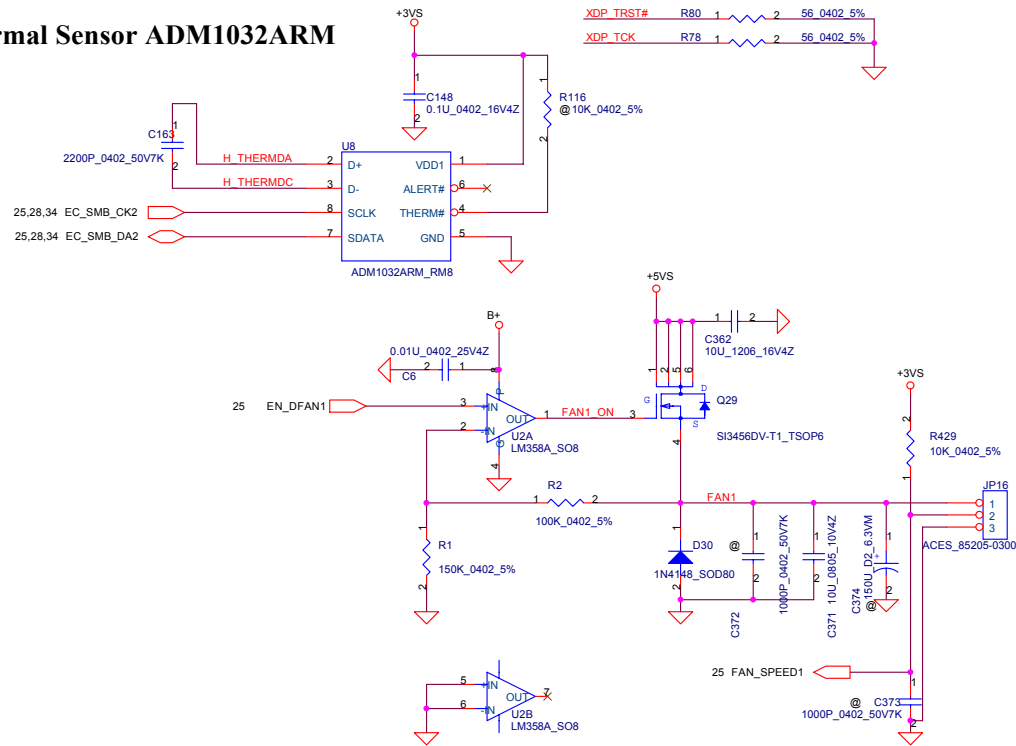
BTO Option Table

BTO Item	BOM Structure
VGA	PM@ GM@
LAN	82573G@ 82573L@ 82573@ 82562@
INT MIC.	45MIC@
DOCKING	WD@ WOD@
CIR	CIR@
FIR	FIR@
SUPER I/O	217@ SI207@
Battery	45@

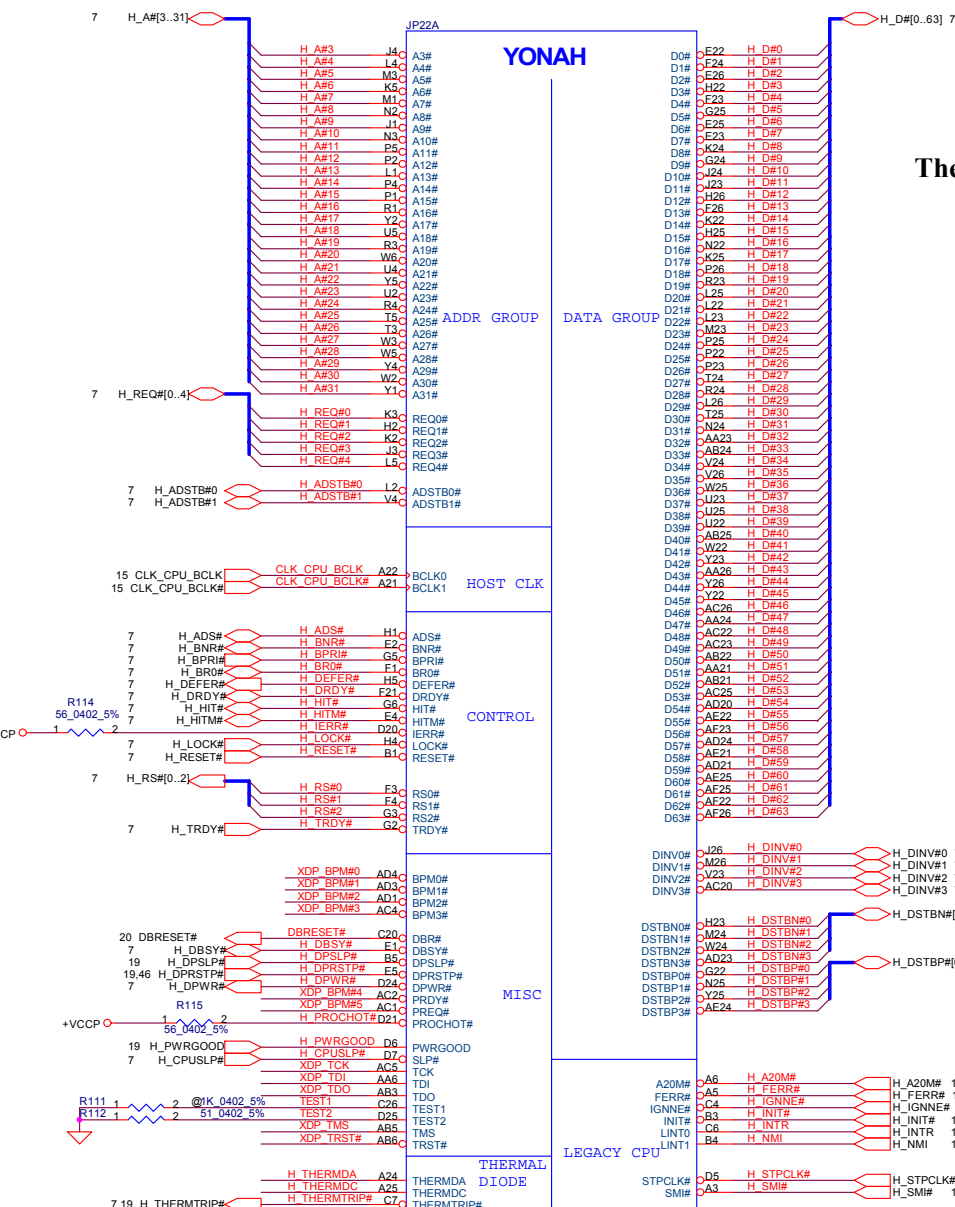
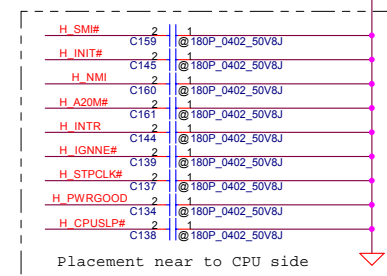
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This shall place near CPU

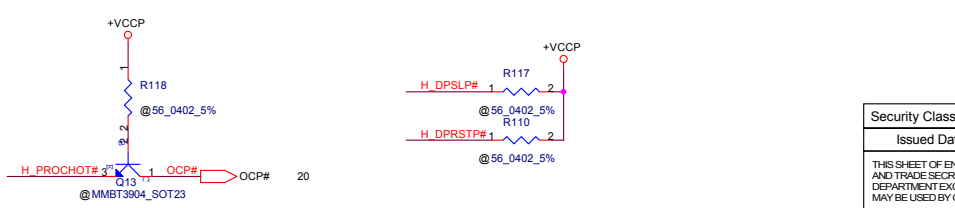
## Thermal Sensor ADM1032ARM



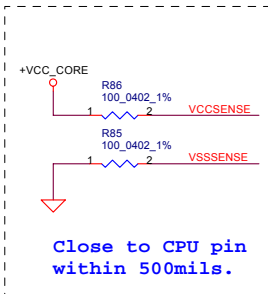
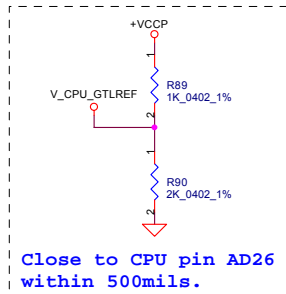
Placement near to ICH7



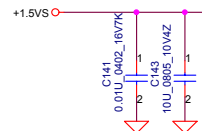
H\_THERMDA, H\_THERMDC routing together.  
Trace width / Spacing = 10 / 10 mil



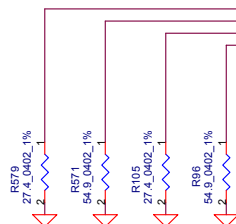
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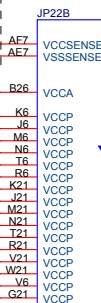
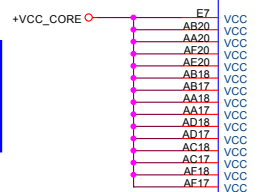
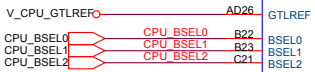
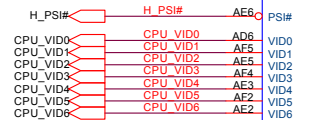
Length match within 25 mils  
The trace width 18 mils space  
7 mils



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

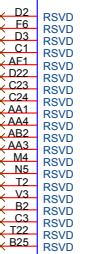


Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.

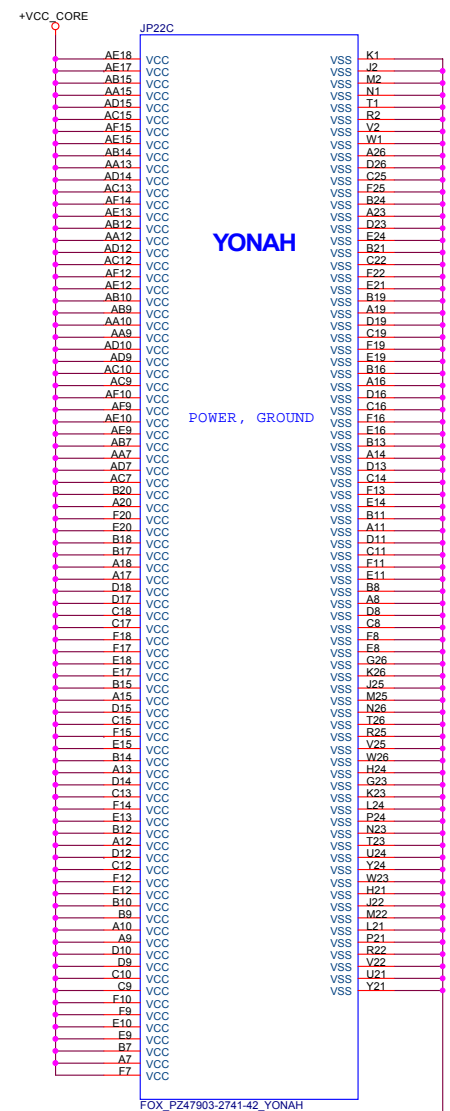


YONAH

POWER, GROUND, RESERVED SIGNALS AND NC



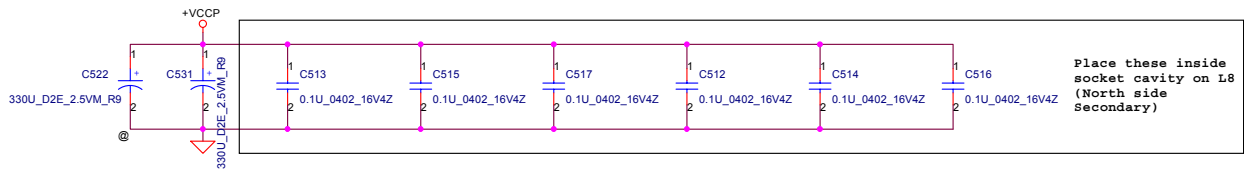
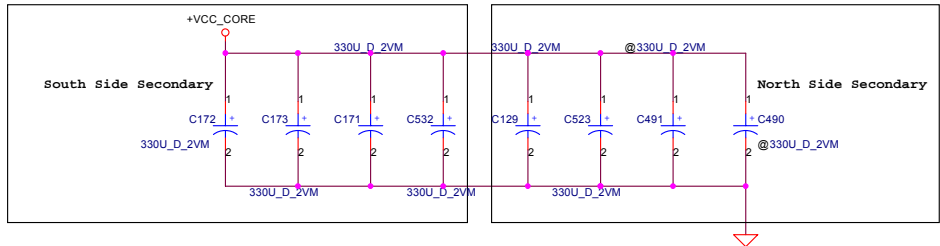
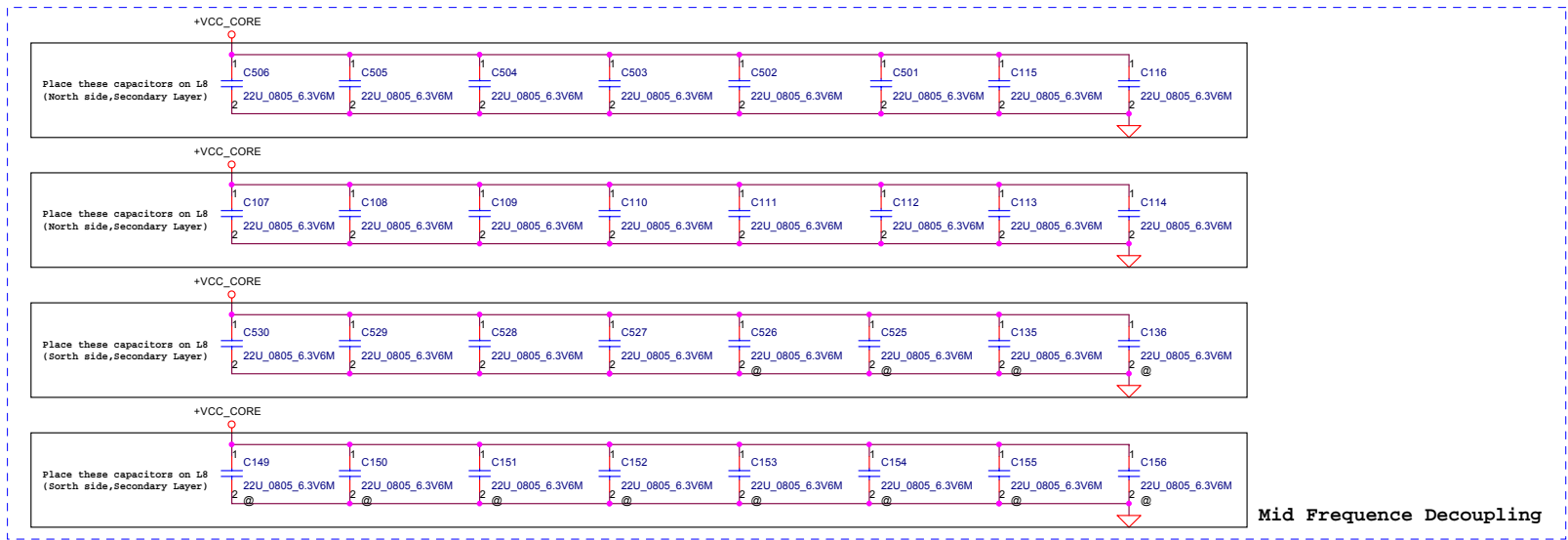
FOX\_PZ47903-2741-42\_YONAH



YONAH

POWER, GROUND

FOX\_PZ47903-2741-42\_YONAH

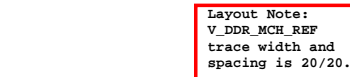


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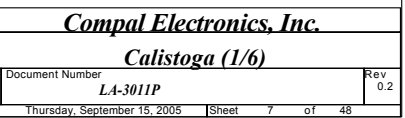


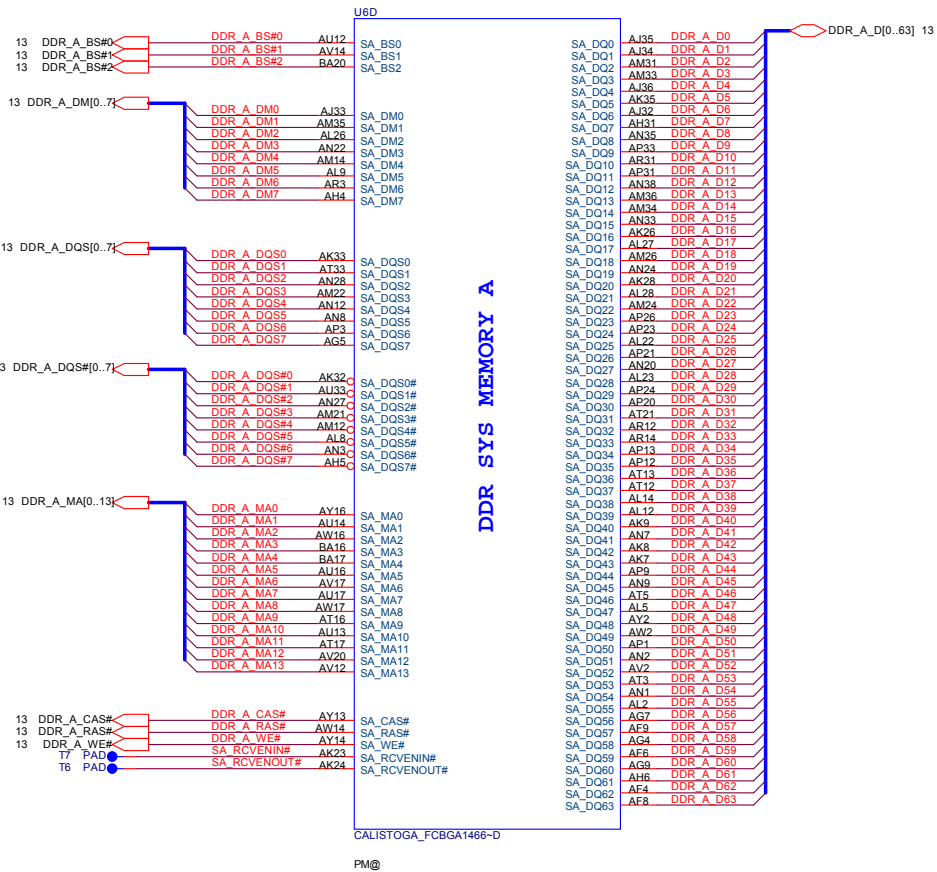
The figure shows three circuit diagrams illustrating different ways to connect a load resistor ( $R_{load}$ ) to a voltage divider. All diagrams share the same components: a voltage divider with resistors  $R1$  and  $R2$ , and a load resistor  $R_{load}$ . The input voltage is  $+VCCP$  and the output voltage is  $VREF$ .

- Diagram 1 (Left):** The load resistor  $R_{load}$  is connected in parallel with the load resistor  $R2$ . The output voltage  $VREF$  is taken across  $R2$  and  $R_{load}$ .
- Diagram 2 (Middle):** The load resistor  $R_{load}$  is connected in parallel with the load resistor  $R2$ . A switch  $SWNG0$  is connected in series with  $R_{load}$  to allow it to be disconnected from the circuit.
- Diagram 3 (Right):** The load resistor  $R_{load}$  is connected in parallel with the load resistor  $R2$ . A switch  $SWNG1$  is connected in series with  $R_{load}$  to allow it to be disconnected from the circuit.



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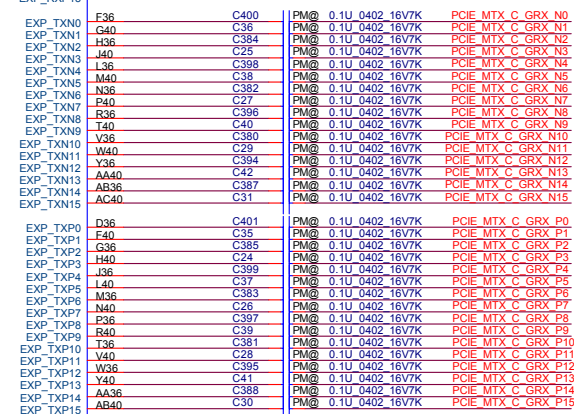
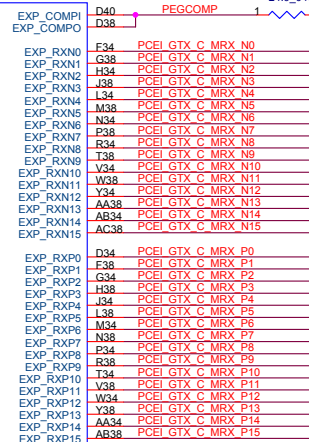
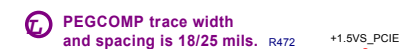
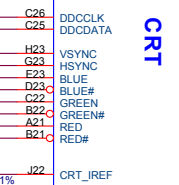
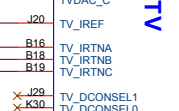
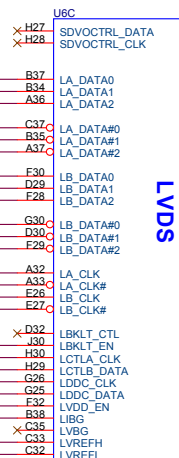
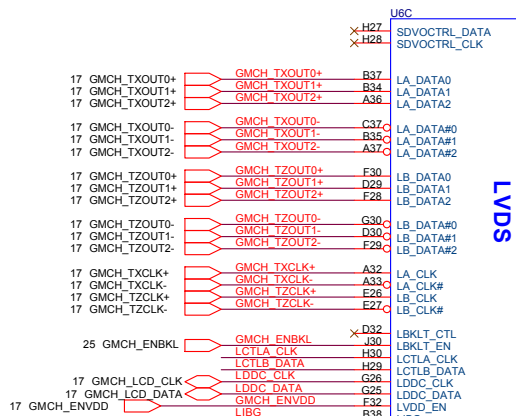
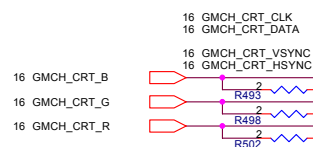
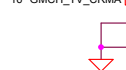
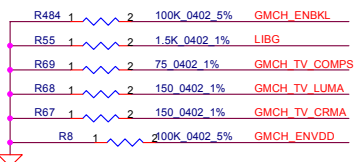
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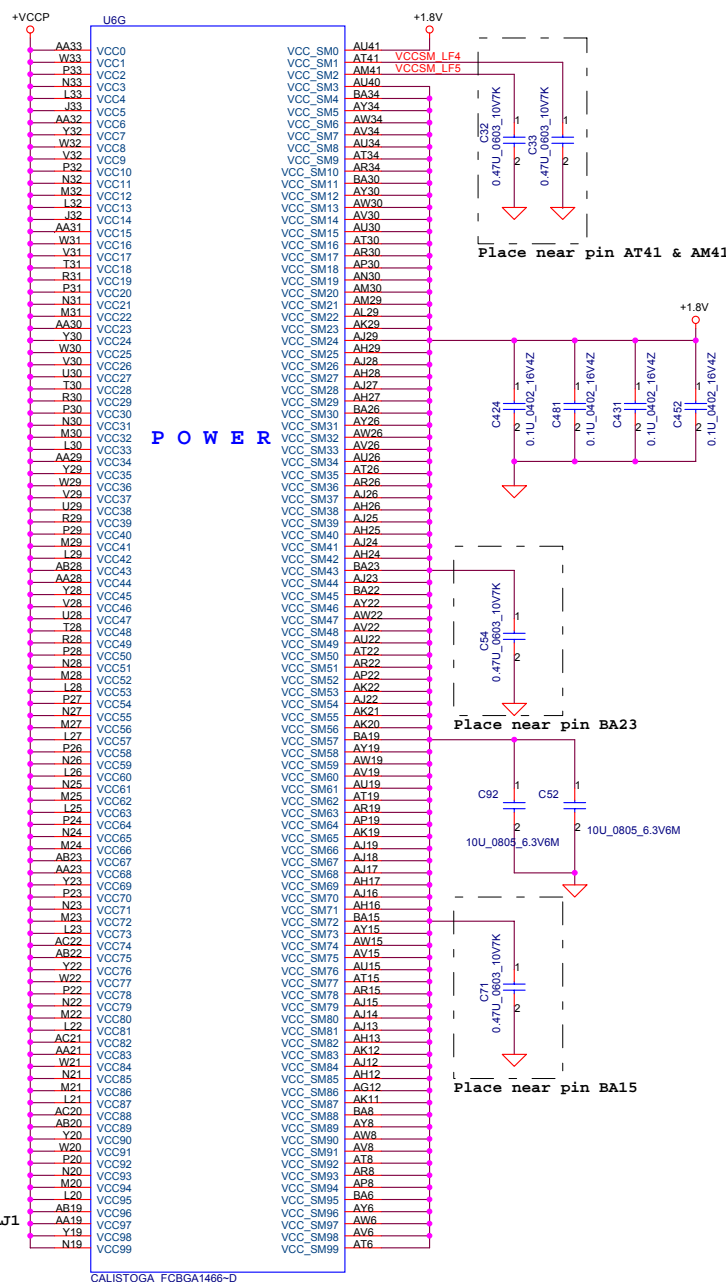
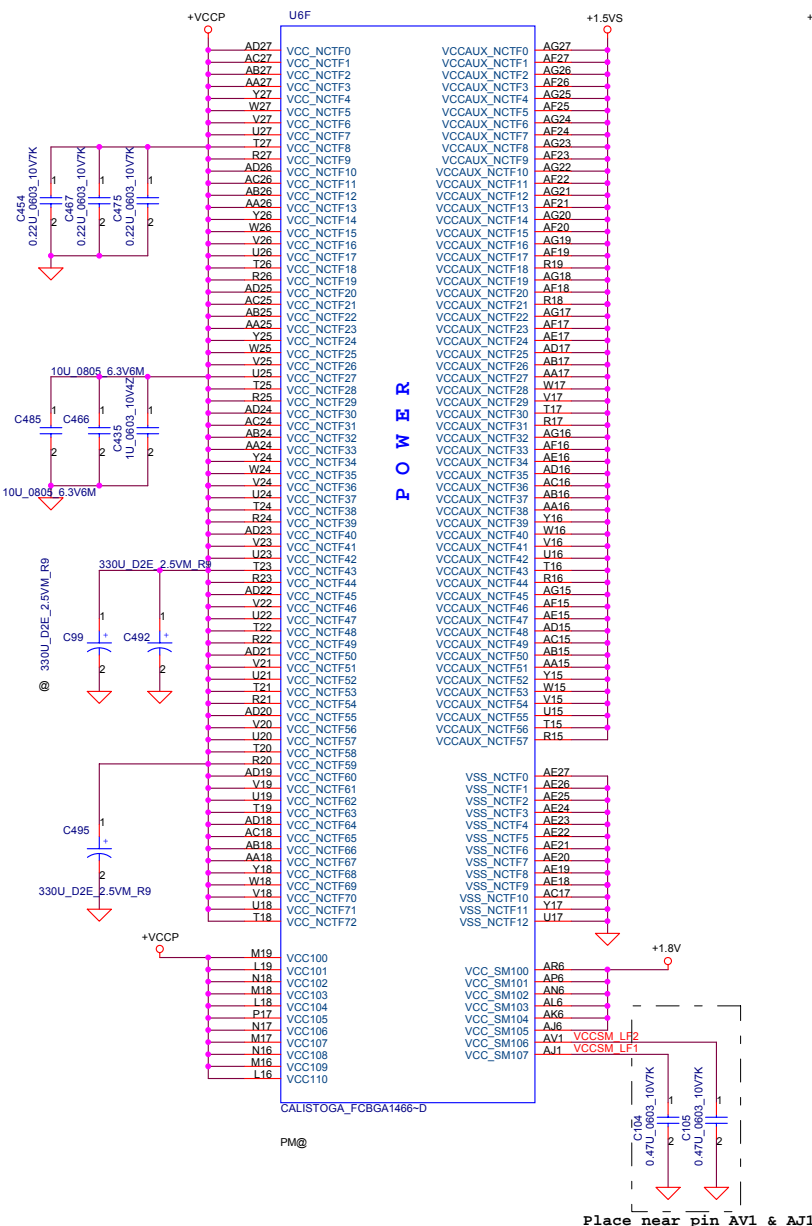
# Strap Pin Table

CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default) *
CFG11	0 = Calistoga * (According to Intel Napa Schematic Checklist & CRB Rev1.301 document 2.2Kohm pull-downs resistor request) 1 = Reserved
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.05V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.

7	CFG5	R513	1	2	@ 2.2K 0402 5%
7	CFG7	R507	1	2	@ 2.2K 0402 5%
7	CFG9	R509	1	2	@ 2.2K 0402 5%
7	CFG11	R514	1	2	@ 2.2K 0402 5%
7	CFG12	R512	1	2	@ 2.2K 0402 5%
7	CFG13	R510	1	2	@ 2.2K 0402 5%
7	CFG16	R506	1	2	@ 2.2K 0402 5%
7	CFG18	R479	1	2	@ 1K 0402 5%
7	CFG19	R482	1	2	@ 1K 0402 5%
7	CFG20	R490	1	2	@ 1K 0402 5%

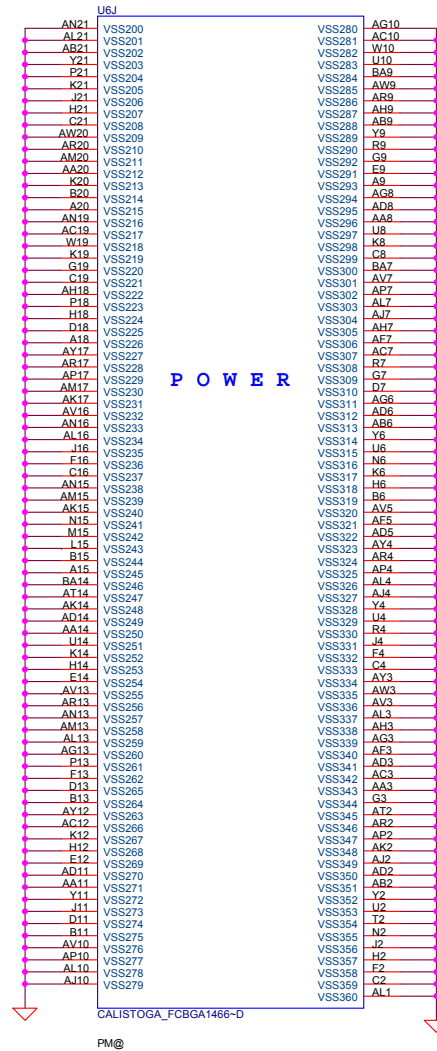
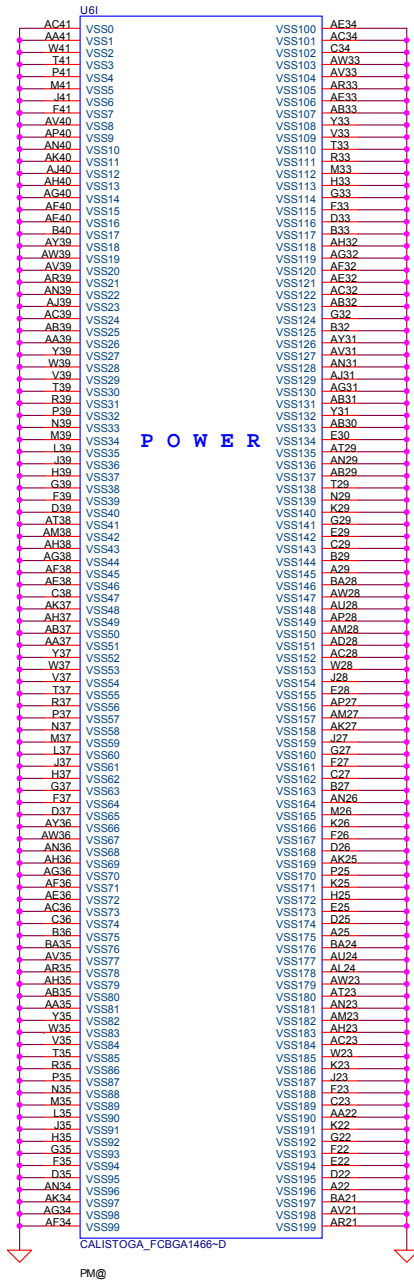


POWER

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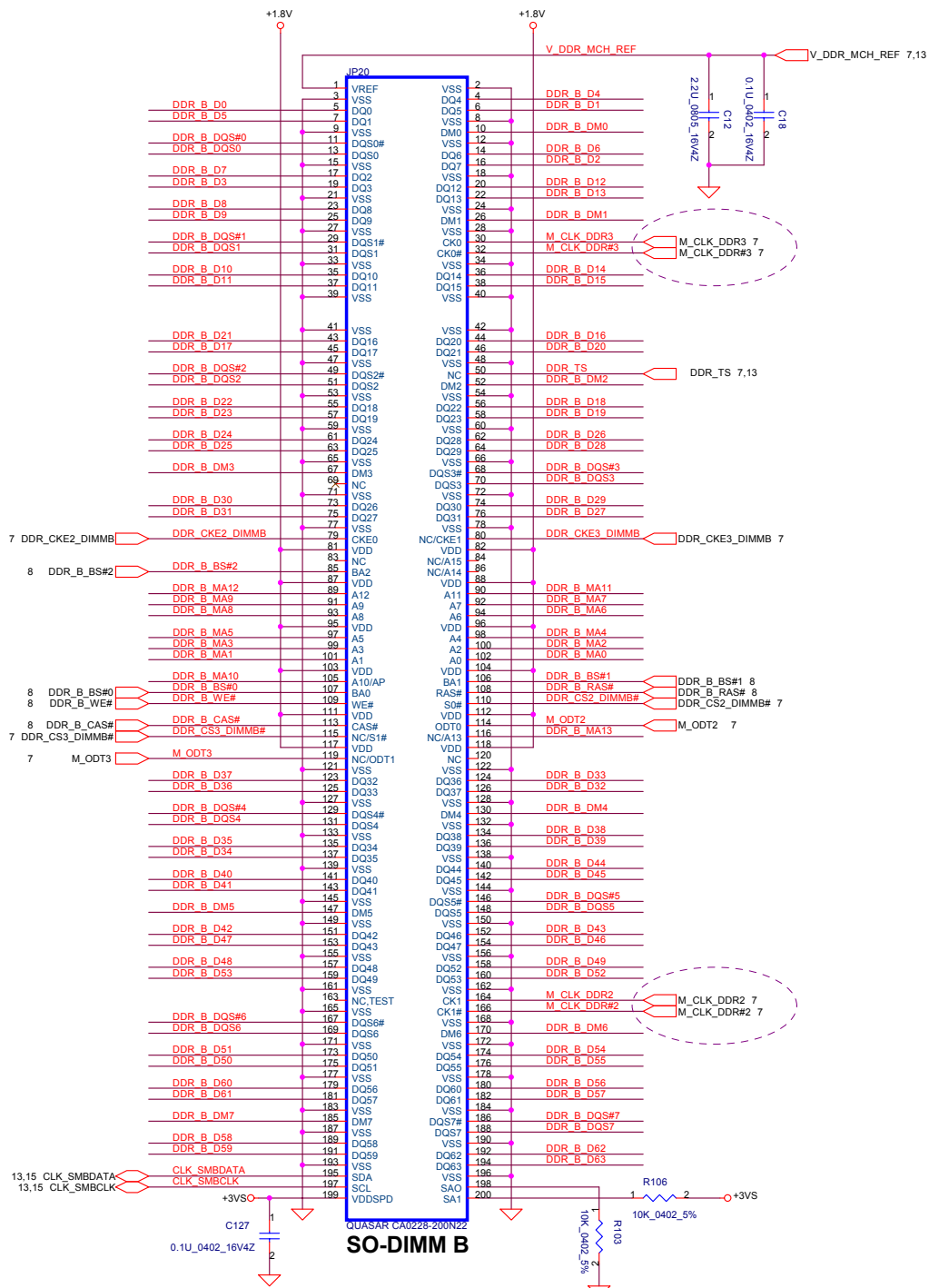
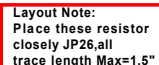
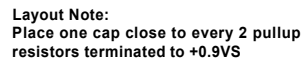
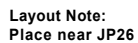
PM@

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					LA-3011P	0.2
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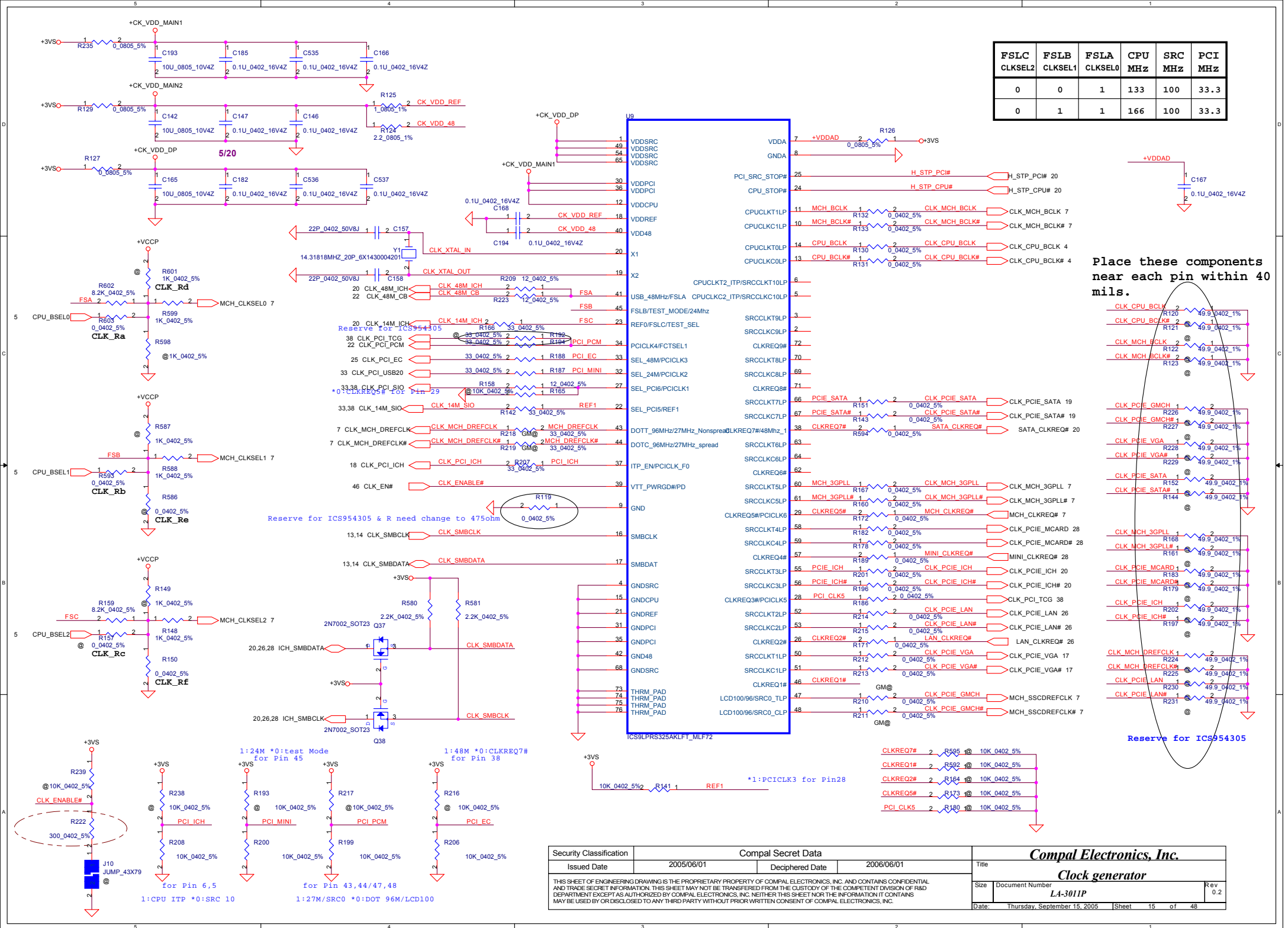
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				Size		Document Number				Rev	
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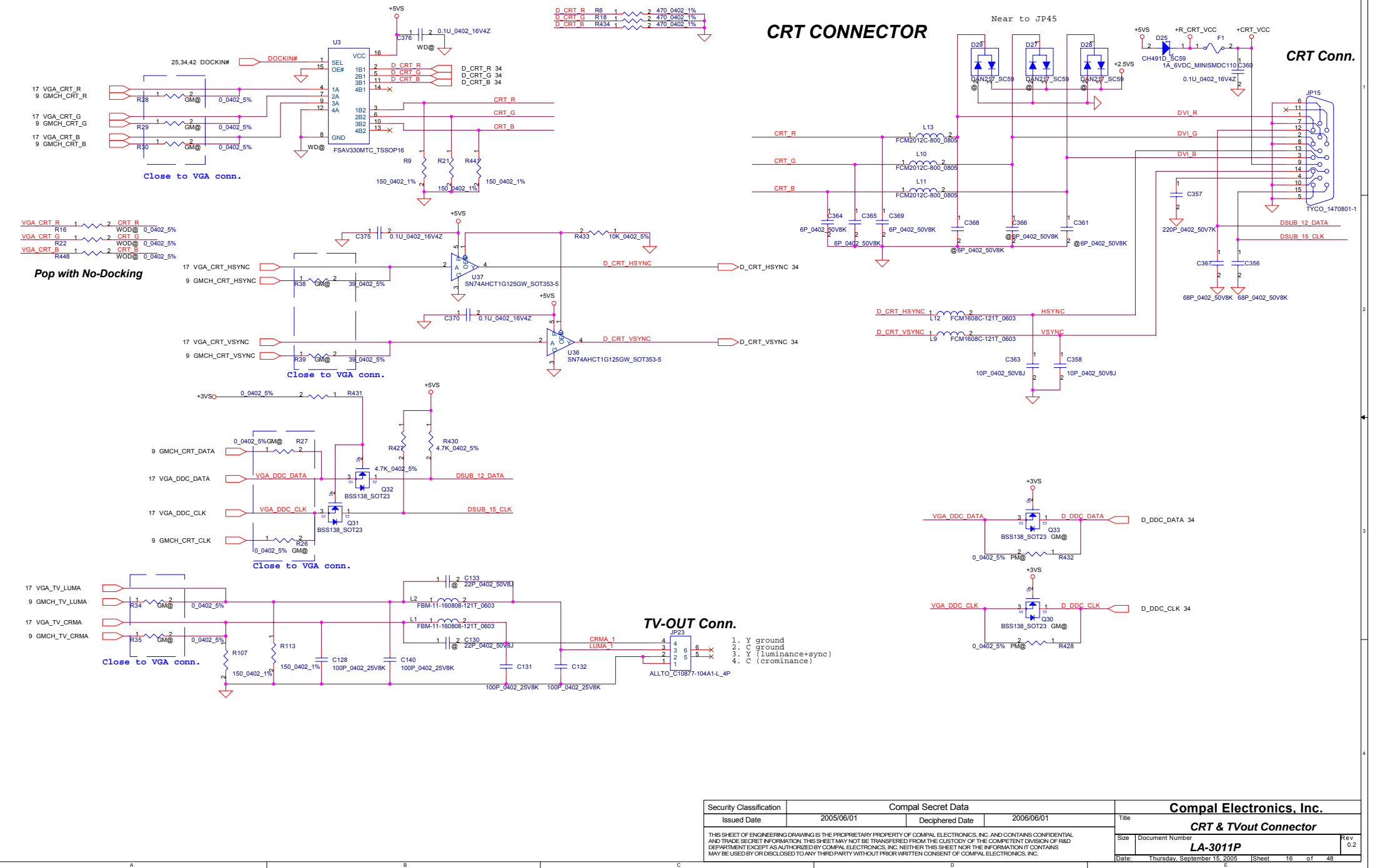


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Size		Document Number		Date		Thursday, September 15, 2005 Sheet 14 of 48	





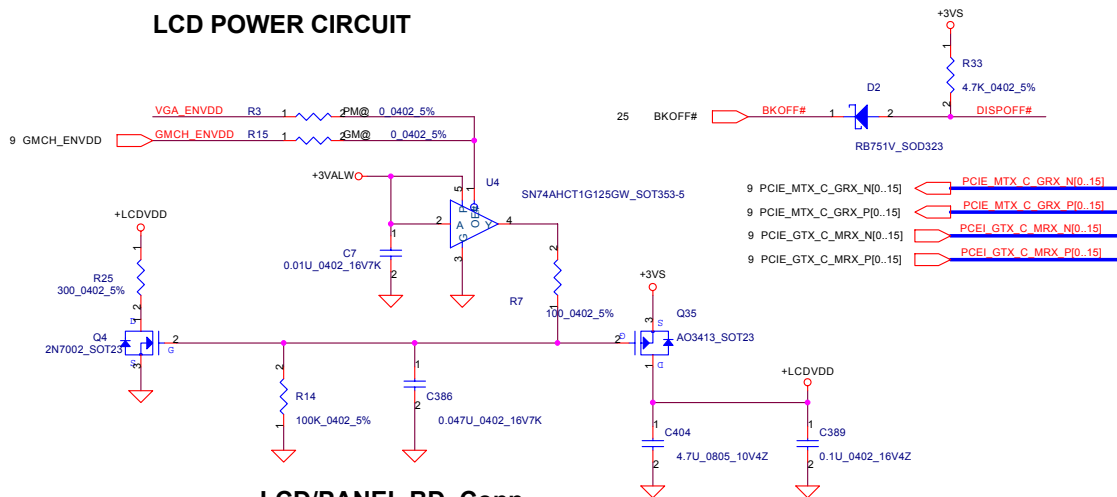
CRT Connector



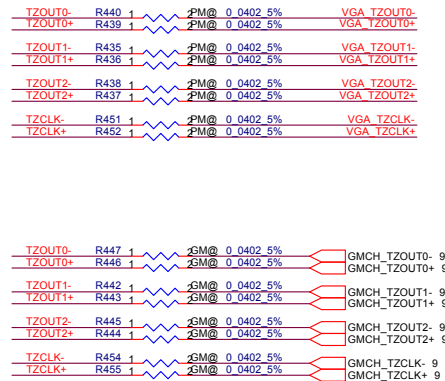
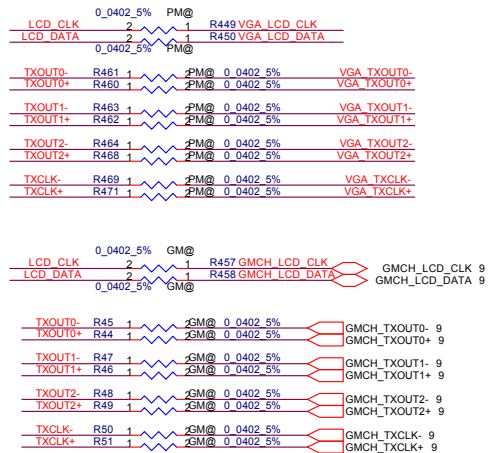
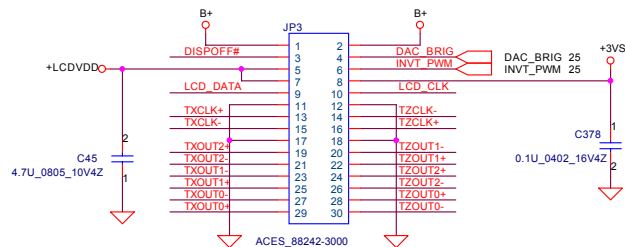
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				Size	Document Number	Rev
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				Date:	Thursday, September 15, 2005	Sheet 16 of 48



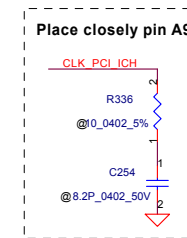
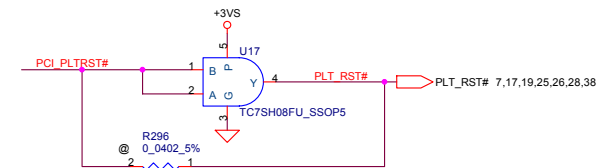
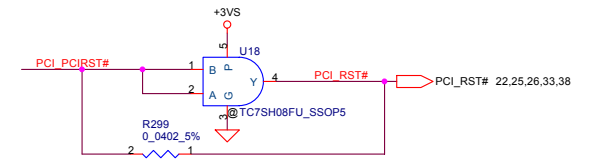
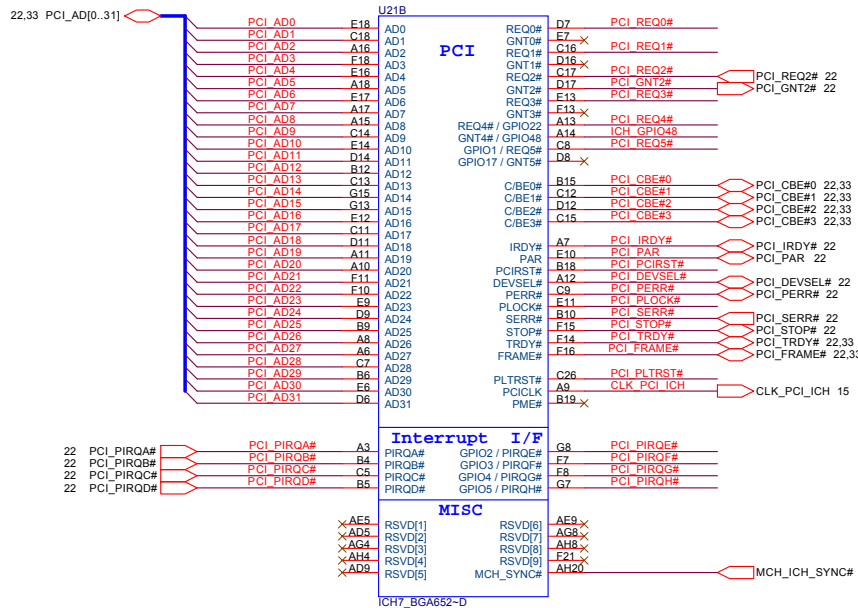
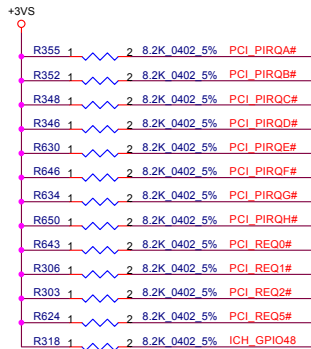
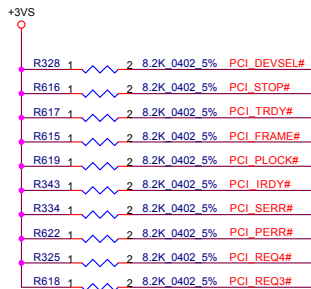
## LCD POWER CIRCUIT



**LCD/PANEL BD. Conn.**

**VGA BOARD Conn.**

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Issued Date	2005/06/01	Deciphered Date	2006/06/01	Title <b>VGA / LCD CONN.</b>	
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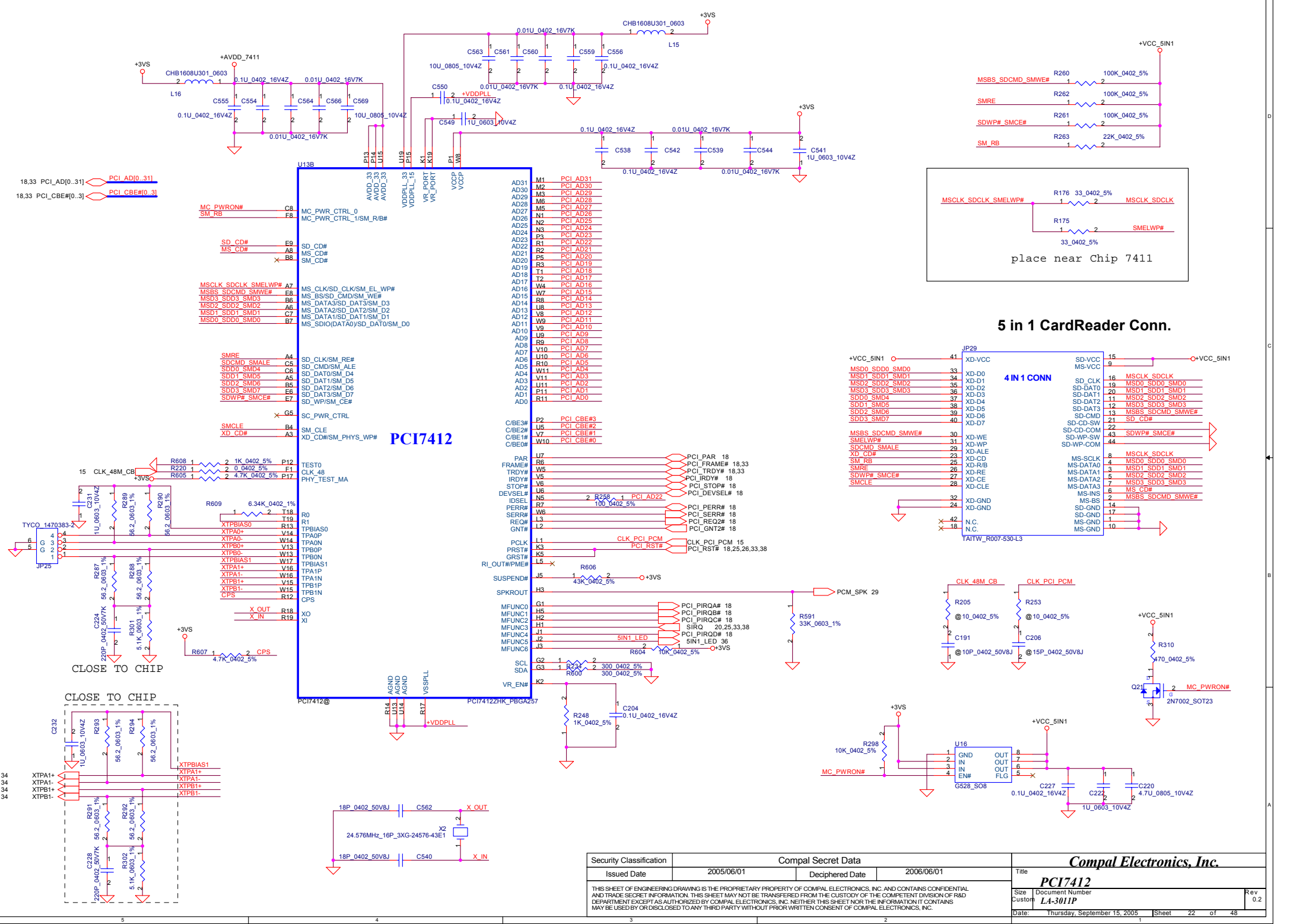


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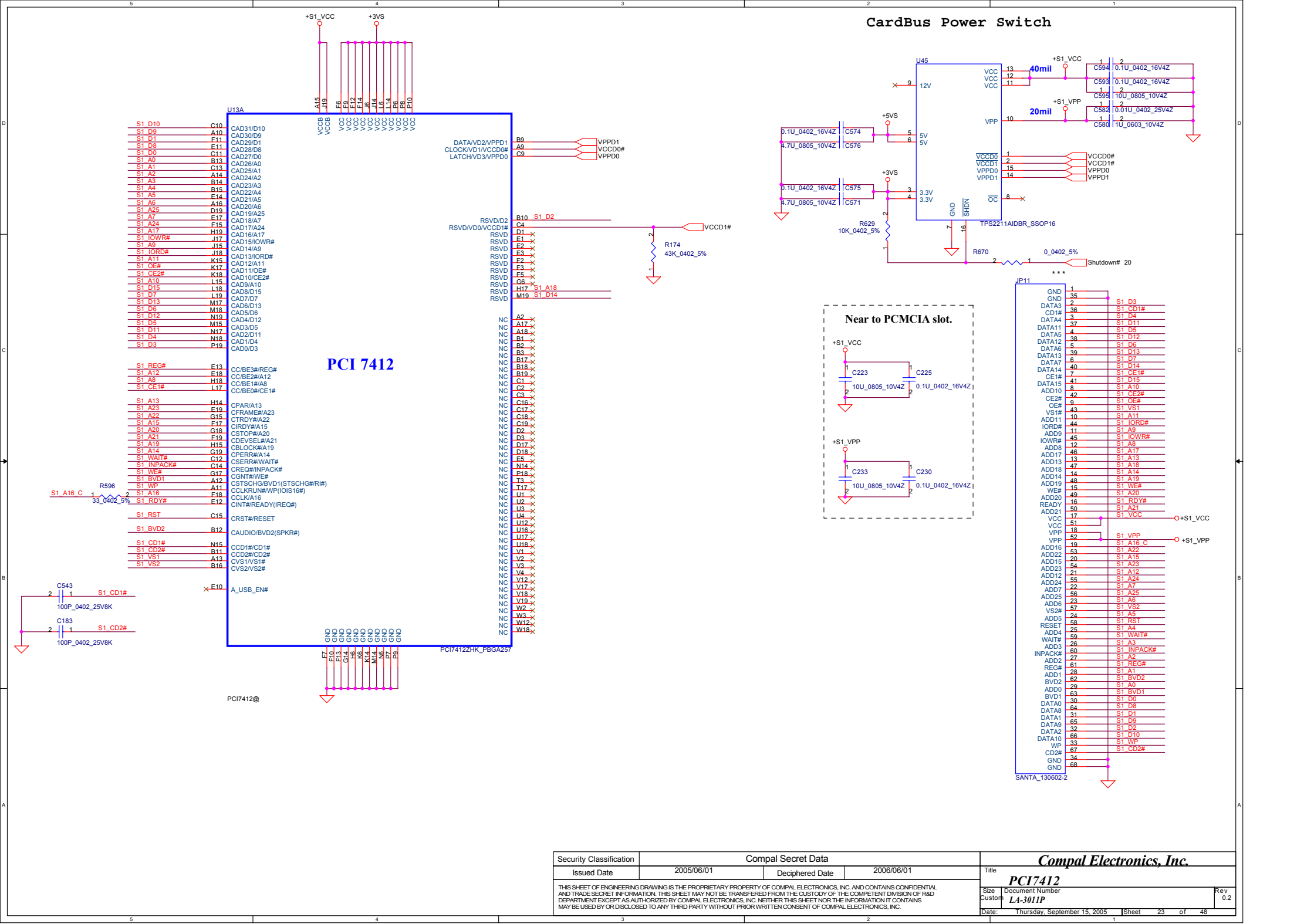




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				Size	Document Number	Rev
				Custom	LA-3011P	0.2
				Date:	Thursday, September 15, 2005	Sheet 22 of 48

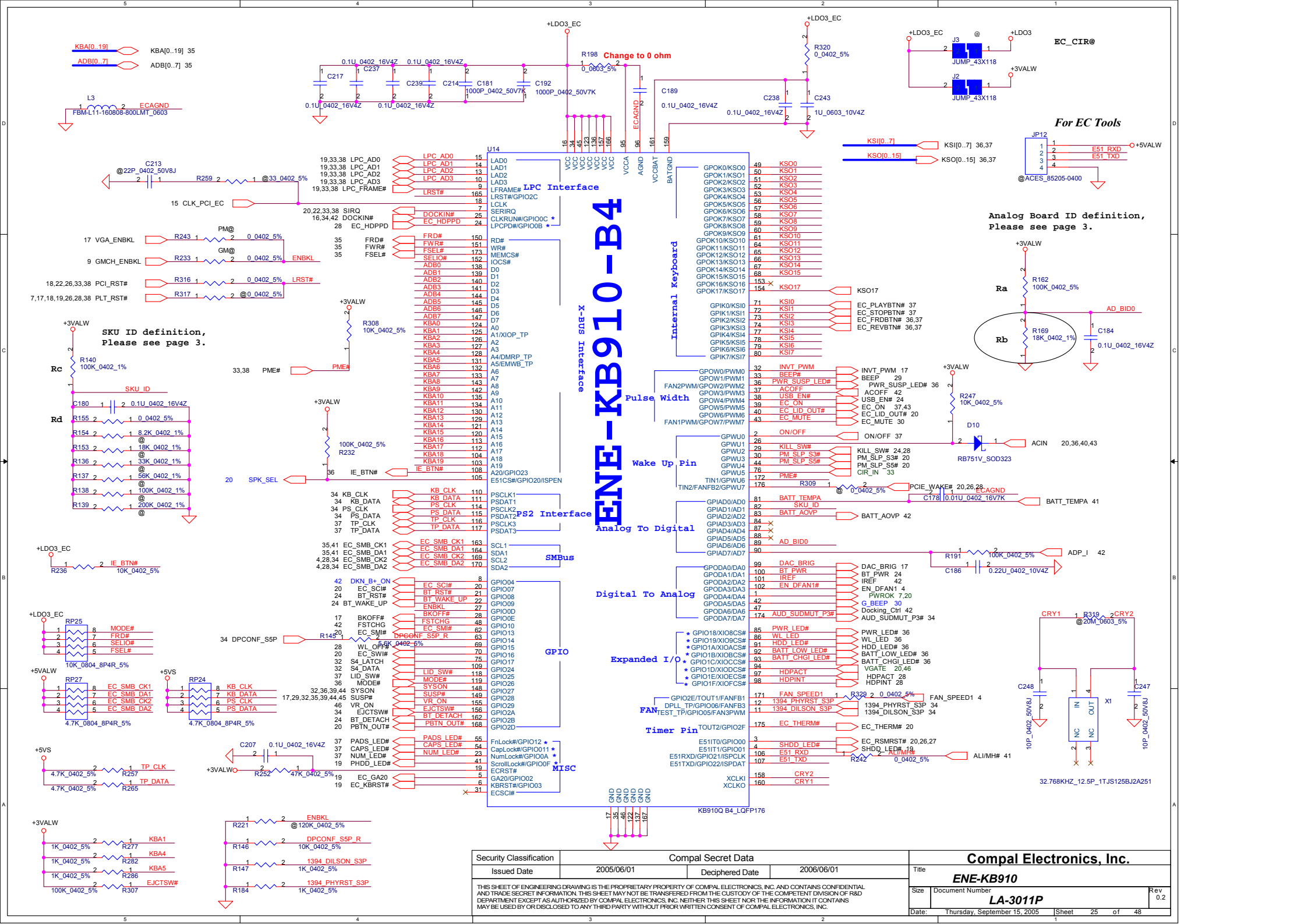


## CardBus Power Switch

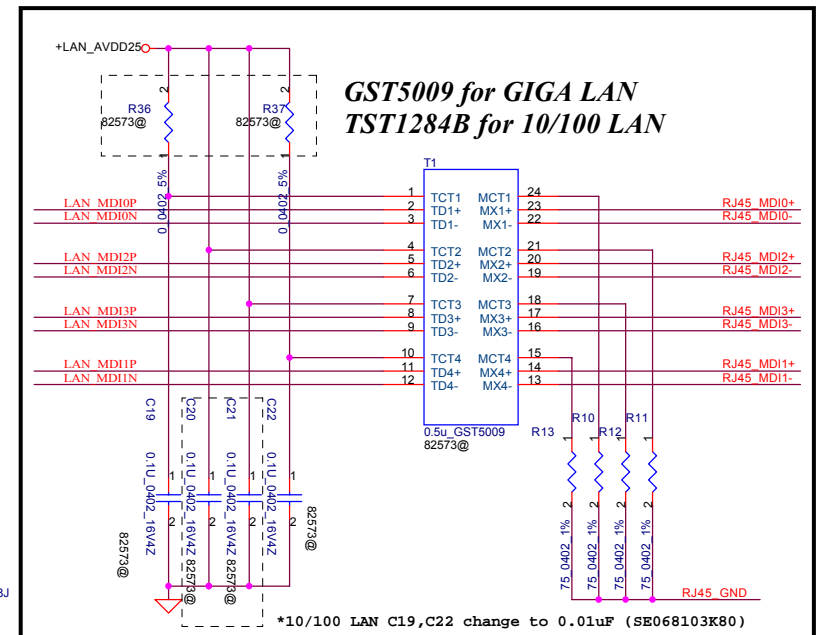
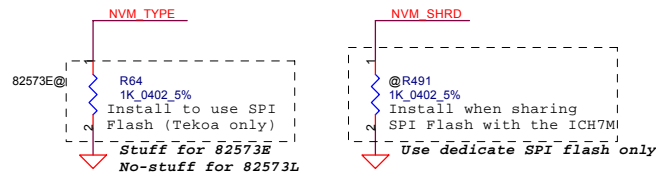
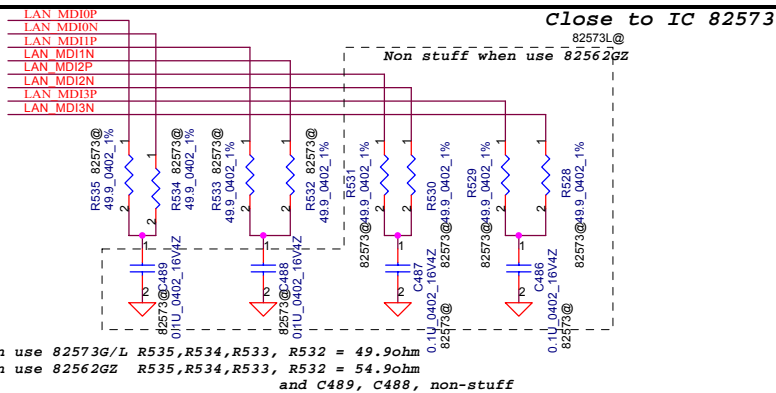
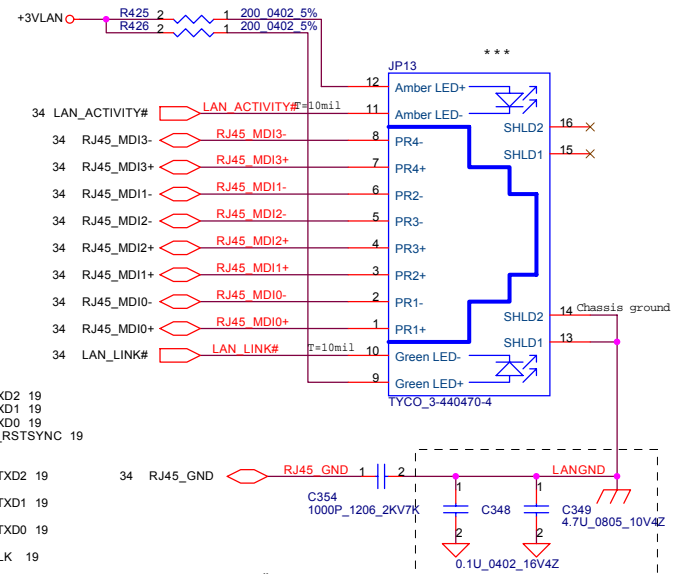
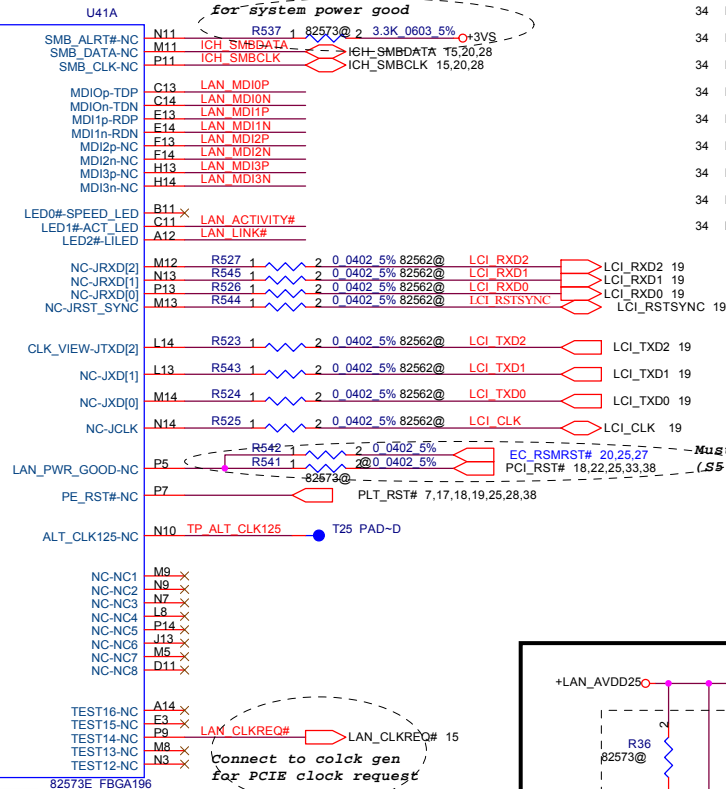
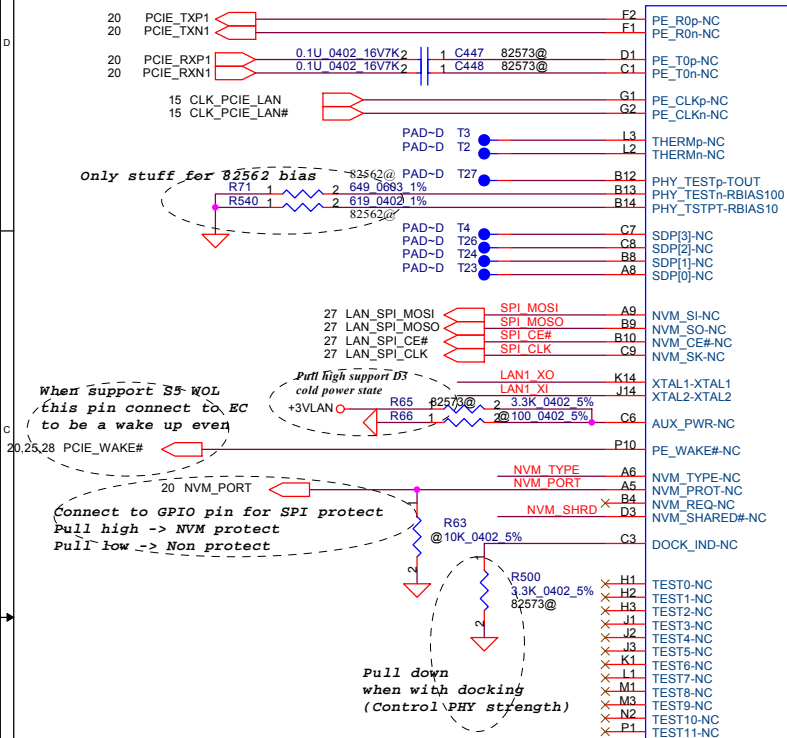


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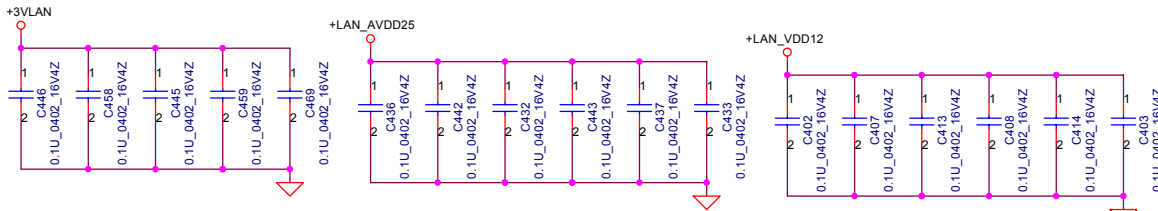




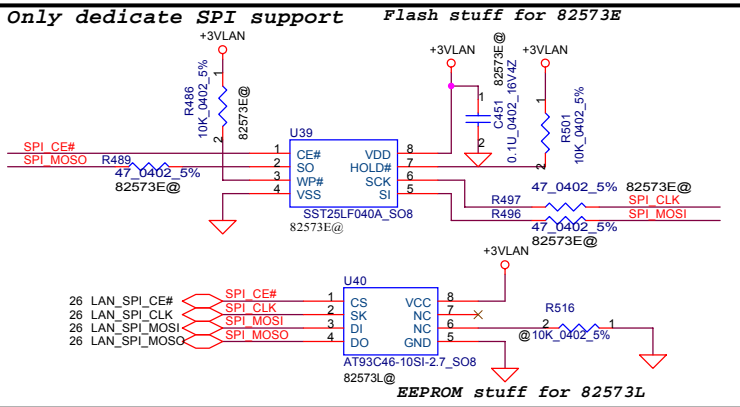
```
Tekoa 82573E -> IAMT support only (WoL Support)
Vidalia 82573L -> No management
82562GZ -> 10/100 support
```



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```
*For 82562GZ stuff 1Kbits EEPROM at ICH7*
```



```
Size:
IAMT support:
At last 4Mbits SPI flash
ASF2.0 Support:
64Kbits EEPROM or SPI flash
No magagement:
1Kbits EEPROM
```



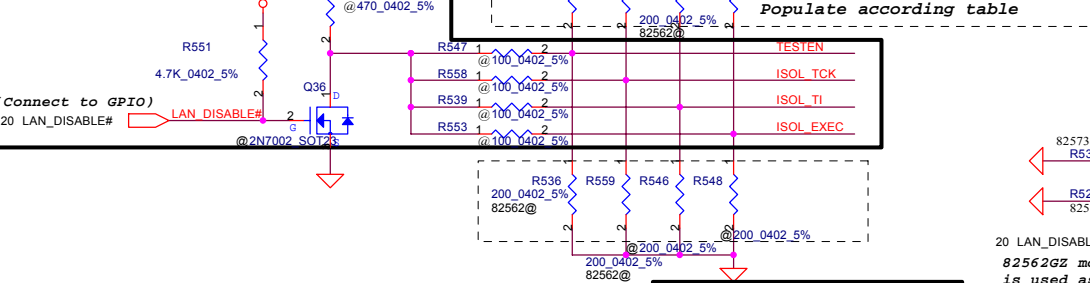
Only 82562GZ mode0 stuff

if use model,2 no-stuff and

only connect LAN\_DISABLE#

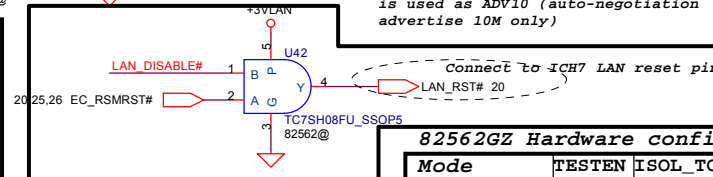
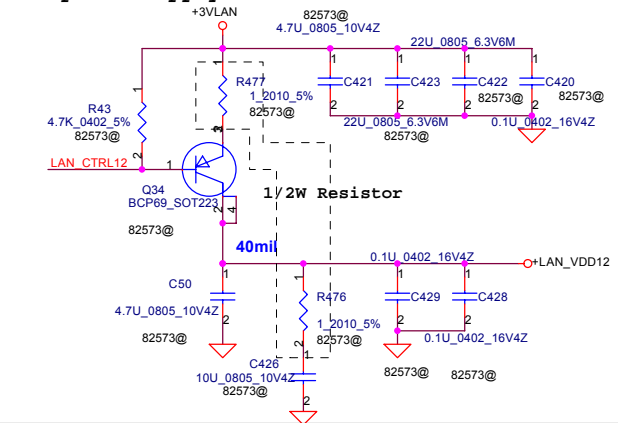
signal to Ball L7

+3VL



---

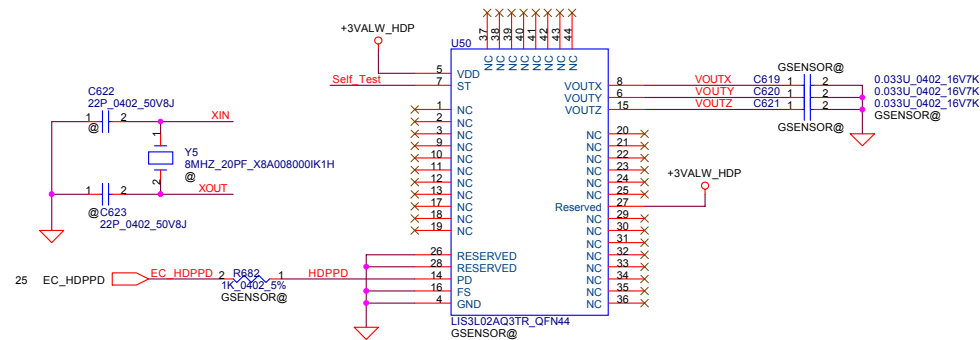
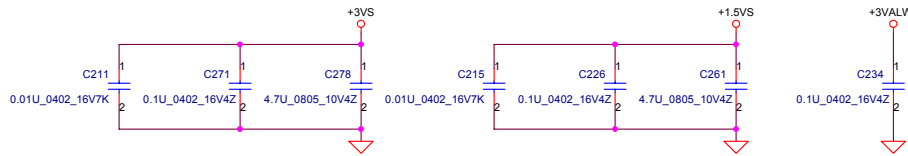
1.2V power supply



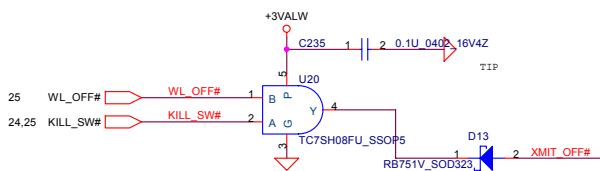
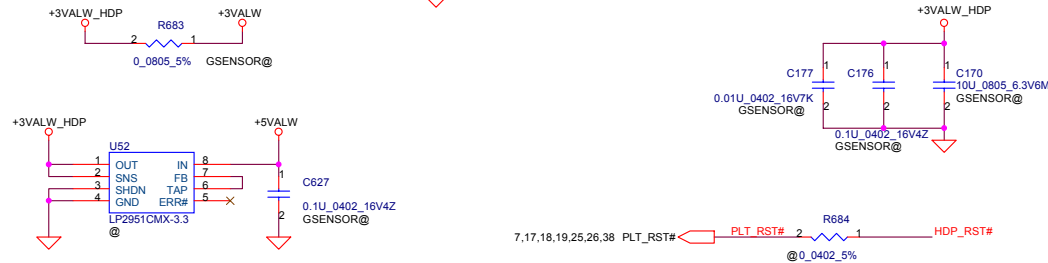
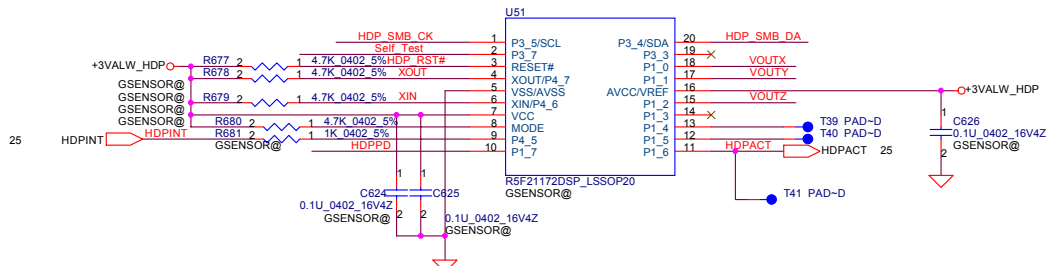
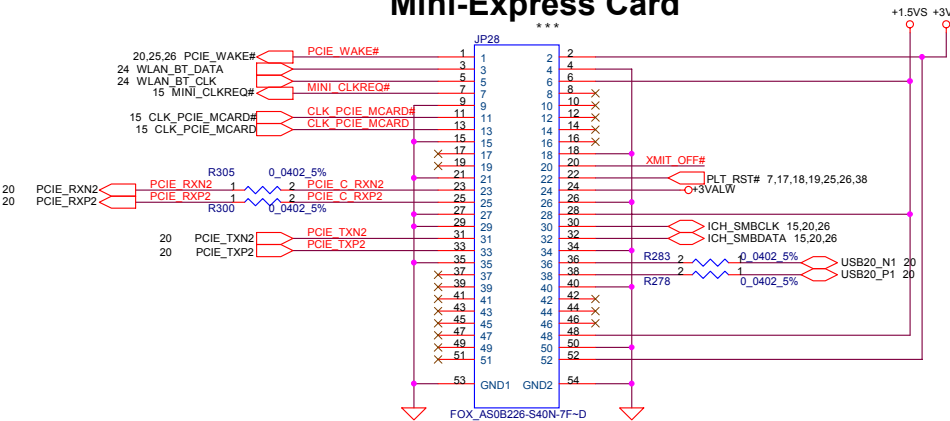
```
82562GZ Hardware configuration table (Default Mode 1)
```

<i>Mode</i>	TESTEN	ISOL_TCK	ISOL_TI	ISOL_EXEC	<i>Mode</i>	TESTEN	ISOL_TCK	ISOL_TI	ISOL_EXEC
Mode0	0	0	0	0	XOR tree	1	0	0	0
Model	0	0	1	1	Mode2	1	0	0	1
Test Mode	1	0	1	0	Mode3	1	0	1	1
Isolate	0	1	1	1	Mode4	1	1	0	0
Power down	1	1	1	1	Reserved	1	1	0	1
					Testing	1	1	1	0

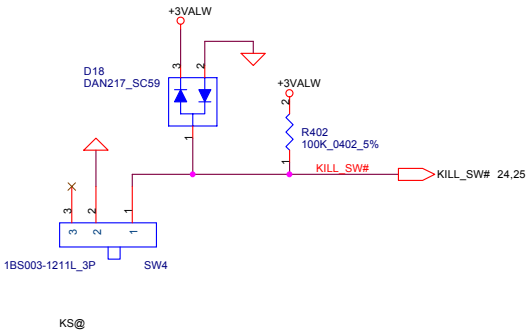
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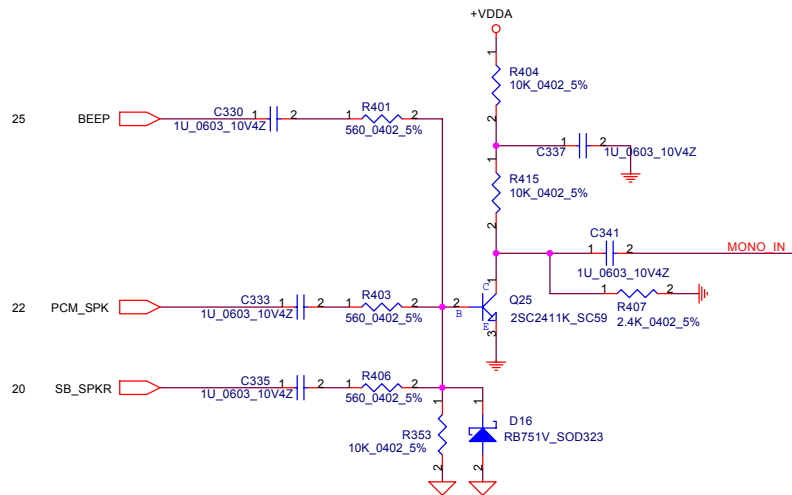
## Mini-Express Card



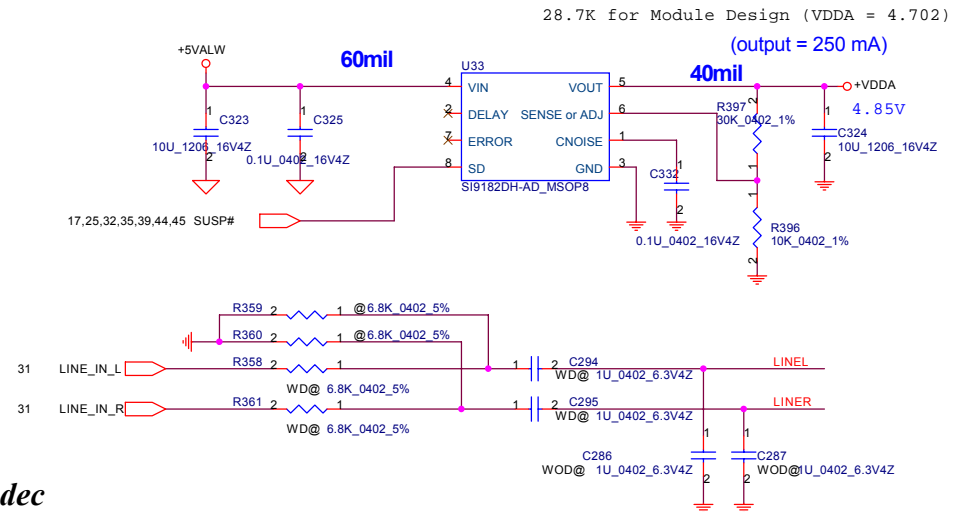
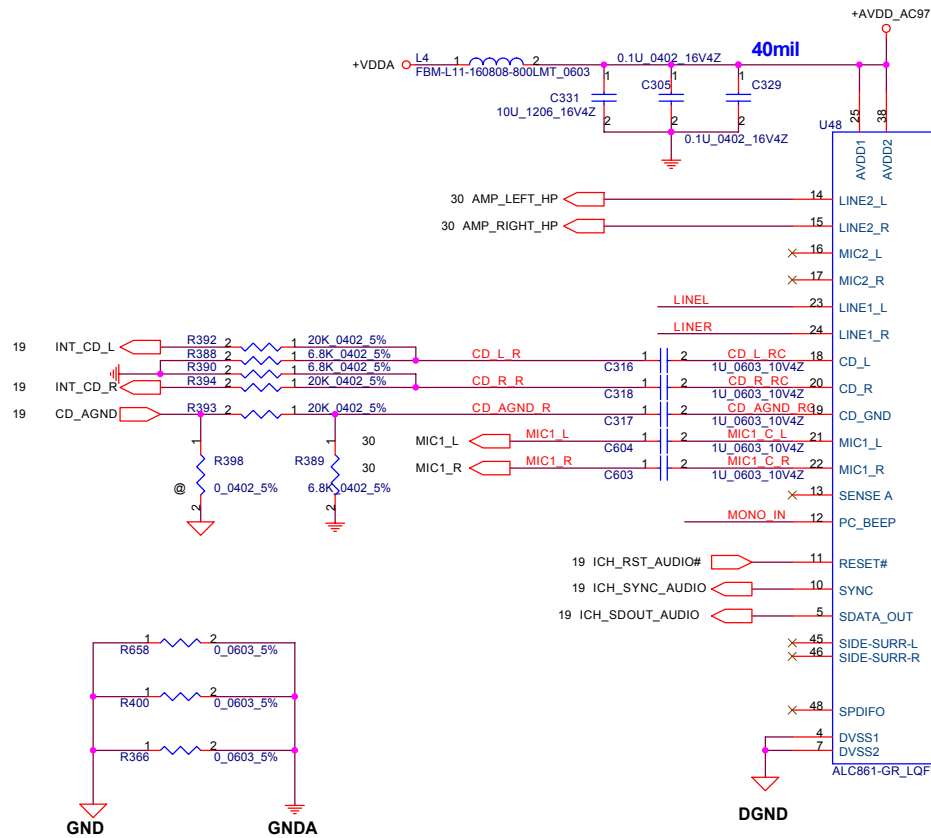
## Kill SWITCH



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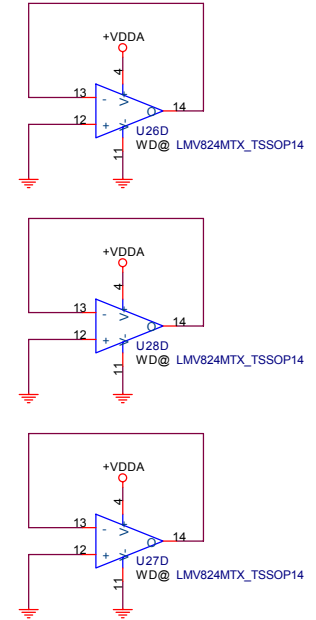
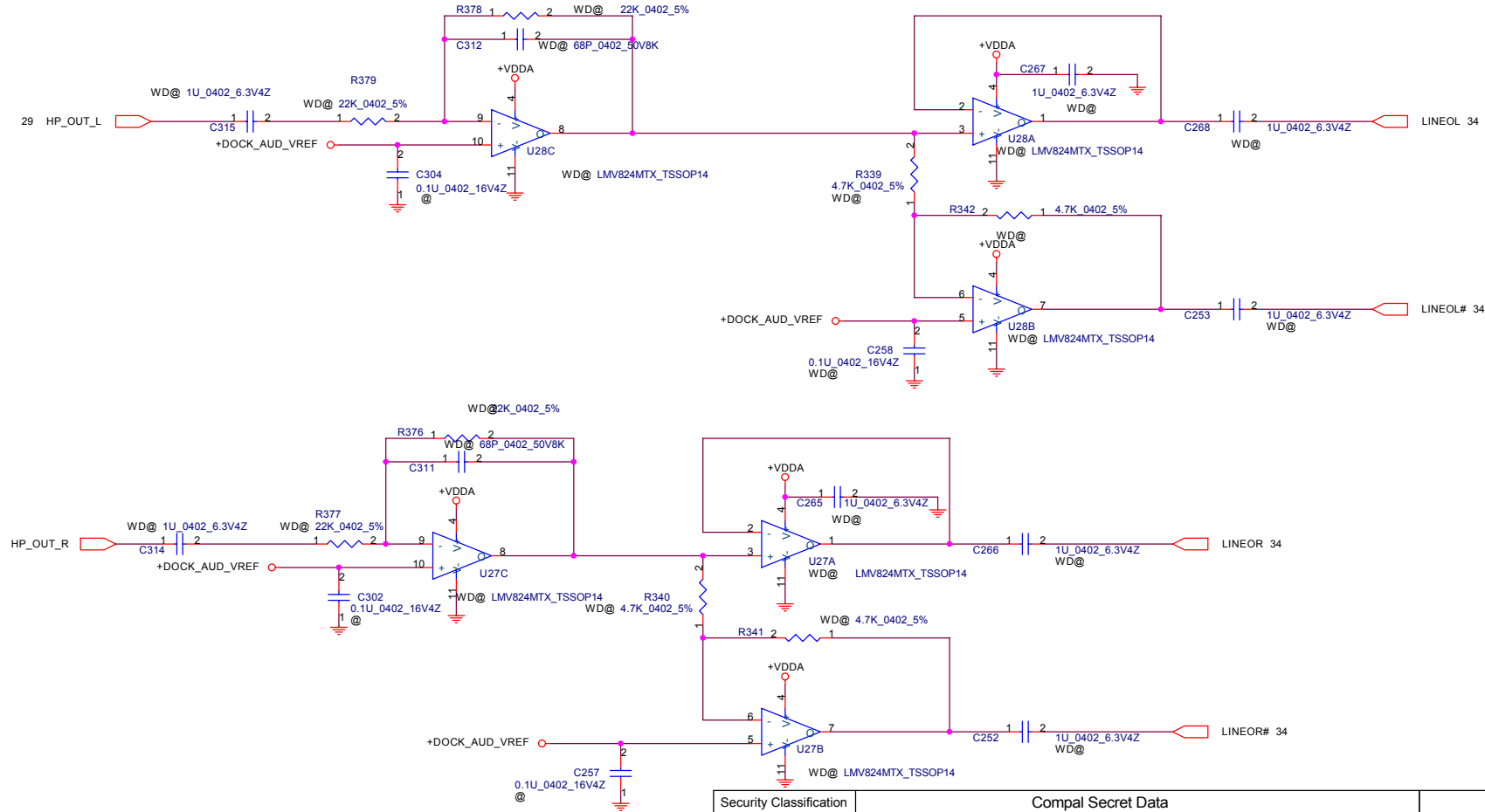
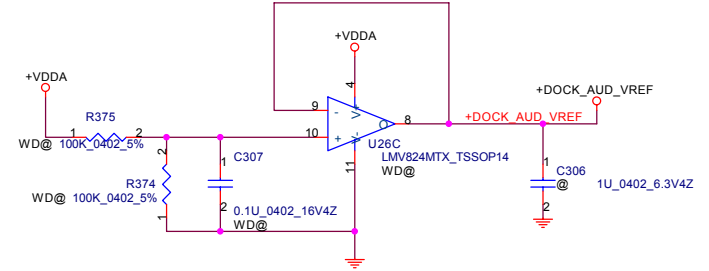
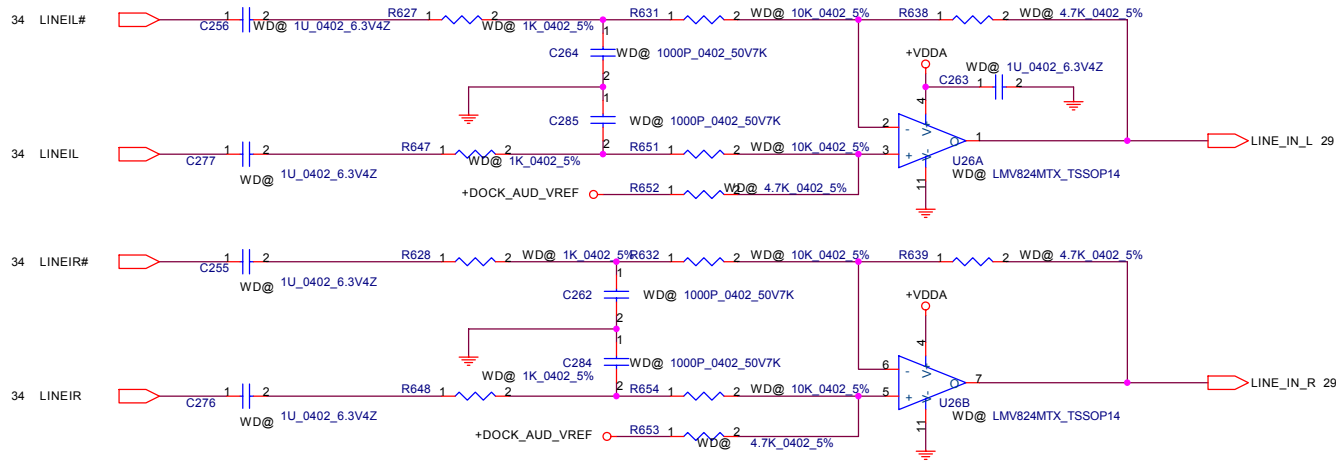
## HD Audio Codec



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Size	Document Number	Rev		0.2	
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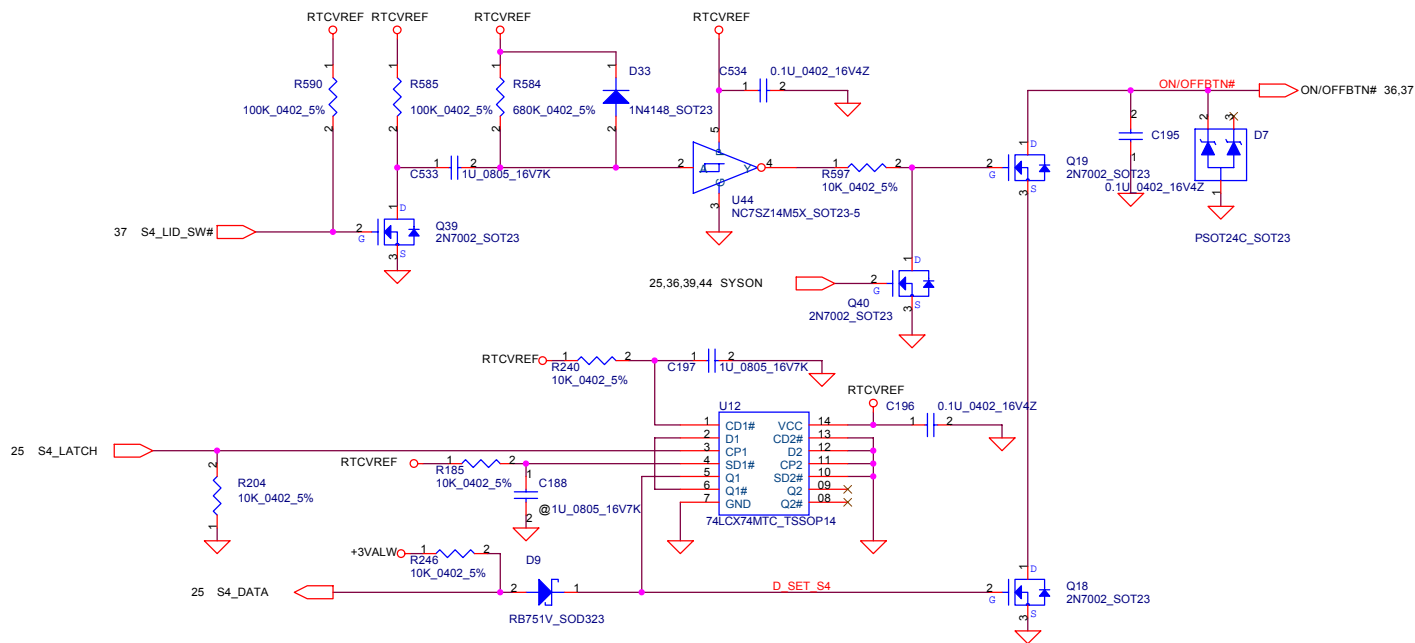




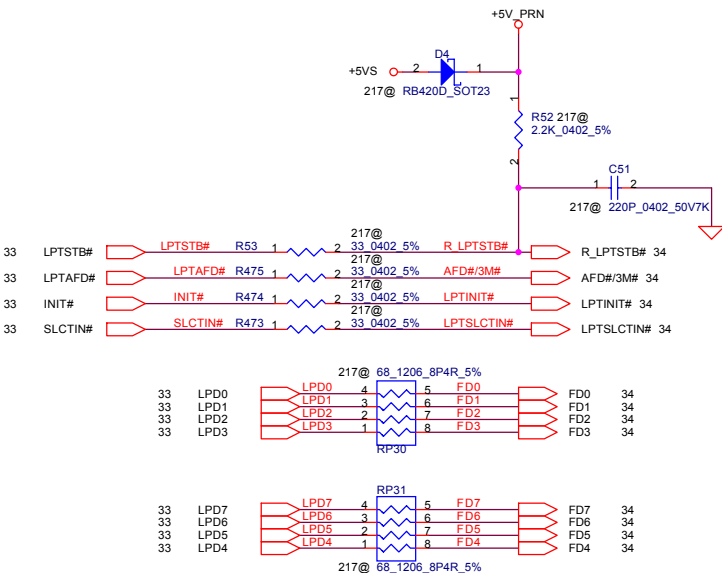


PROPRIETARY NOTE

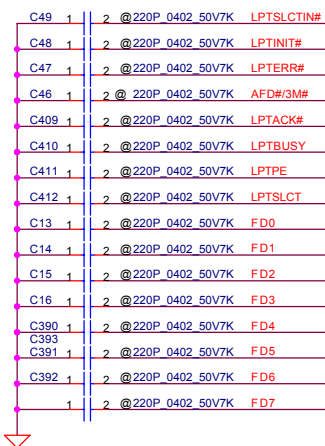
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Issued Date	2005/04/25	Deciphered Date	2006/06/01	Title	<b>Docking Audio</b>
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				<b>LA-3011P</b>	
				Date:	Thursday, September 15, 2005
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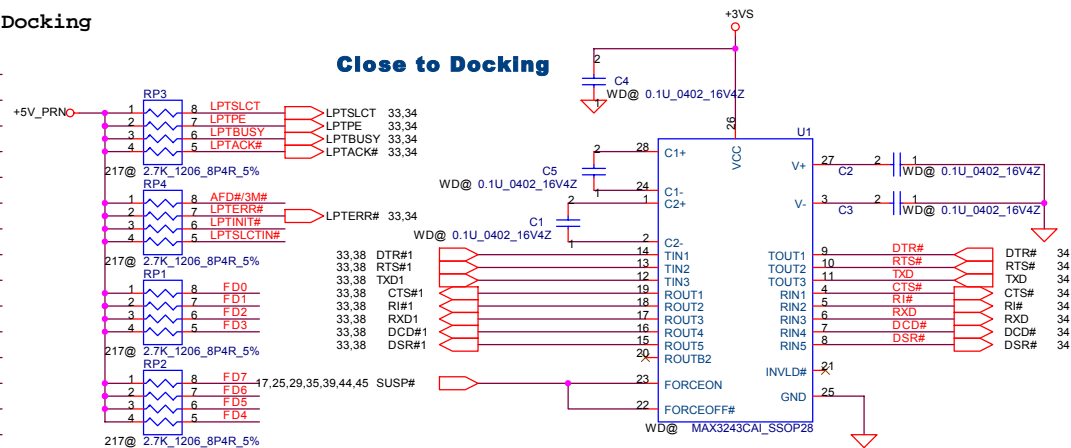
## Docking Parallel Port



## Close to Docking



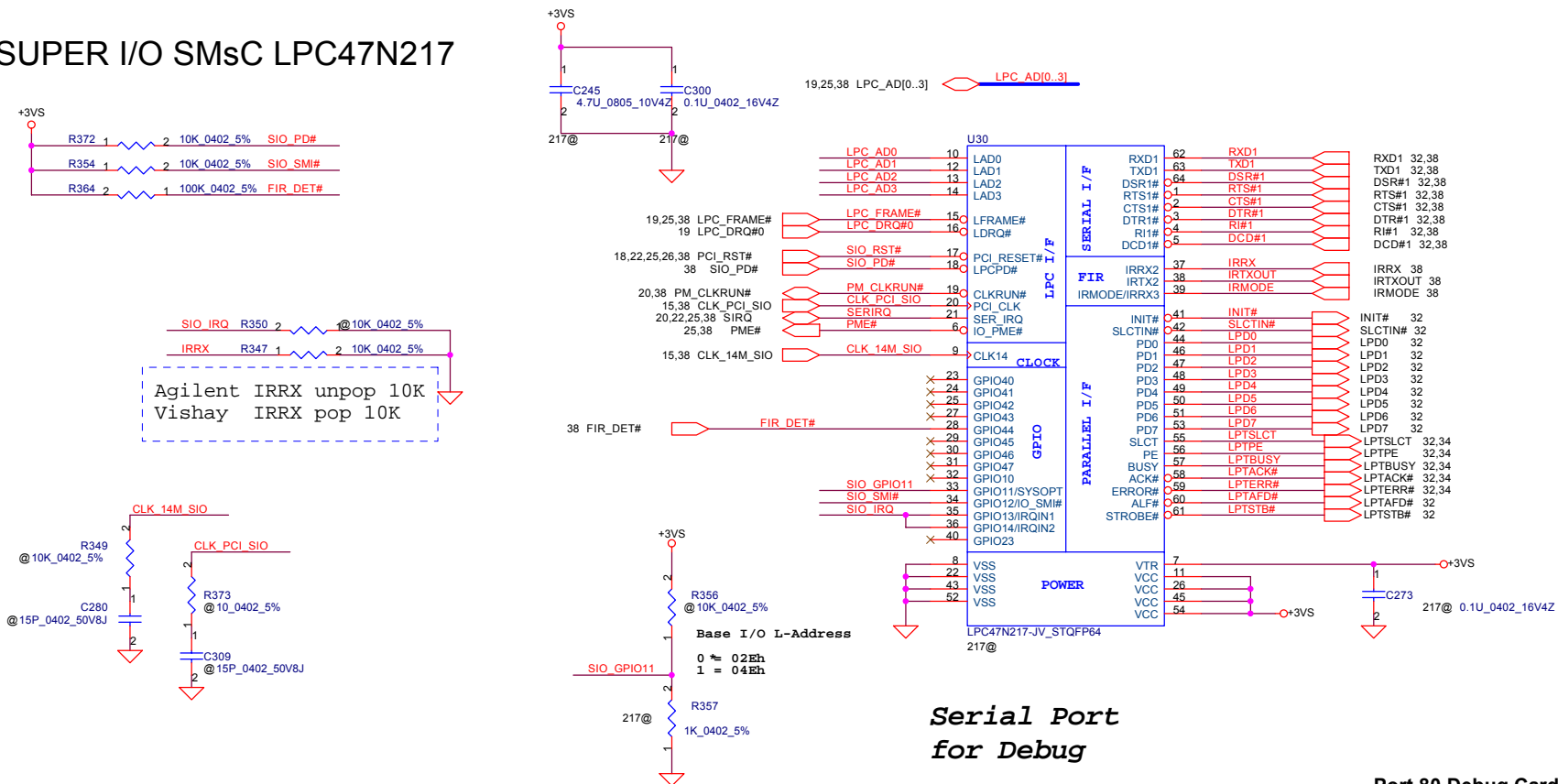
## Close to Docking



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Size		Document Number		Rev	
Date		Thursday, September 15, 2005		Sheet 32 of 48	
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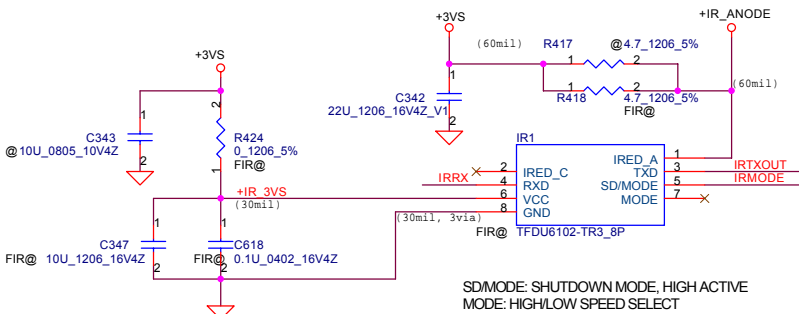
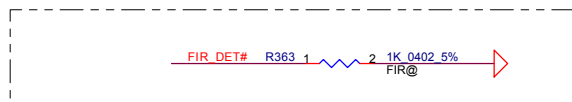


# SUPER I/O SMsC LPC47N217

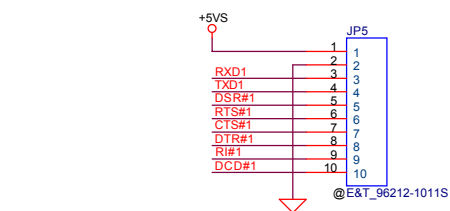
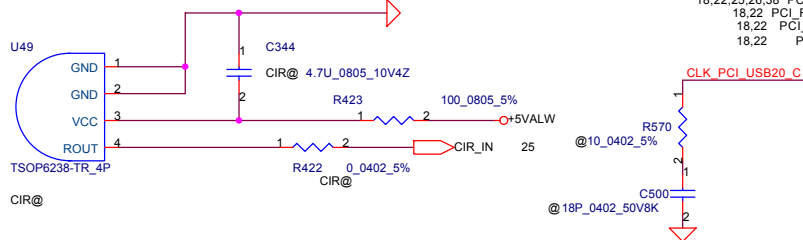


## FIR Module

```
L: R POP; FIR Enable
H: R De-POP/FIR Disable
```

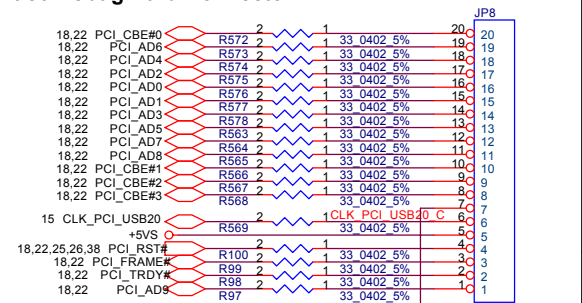


## Serial Port for Debug

**CIR**

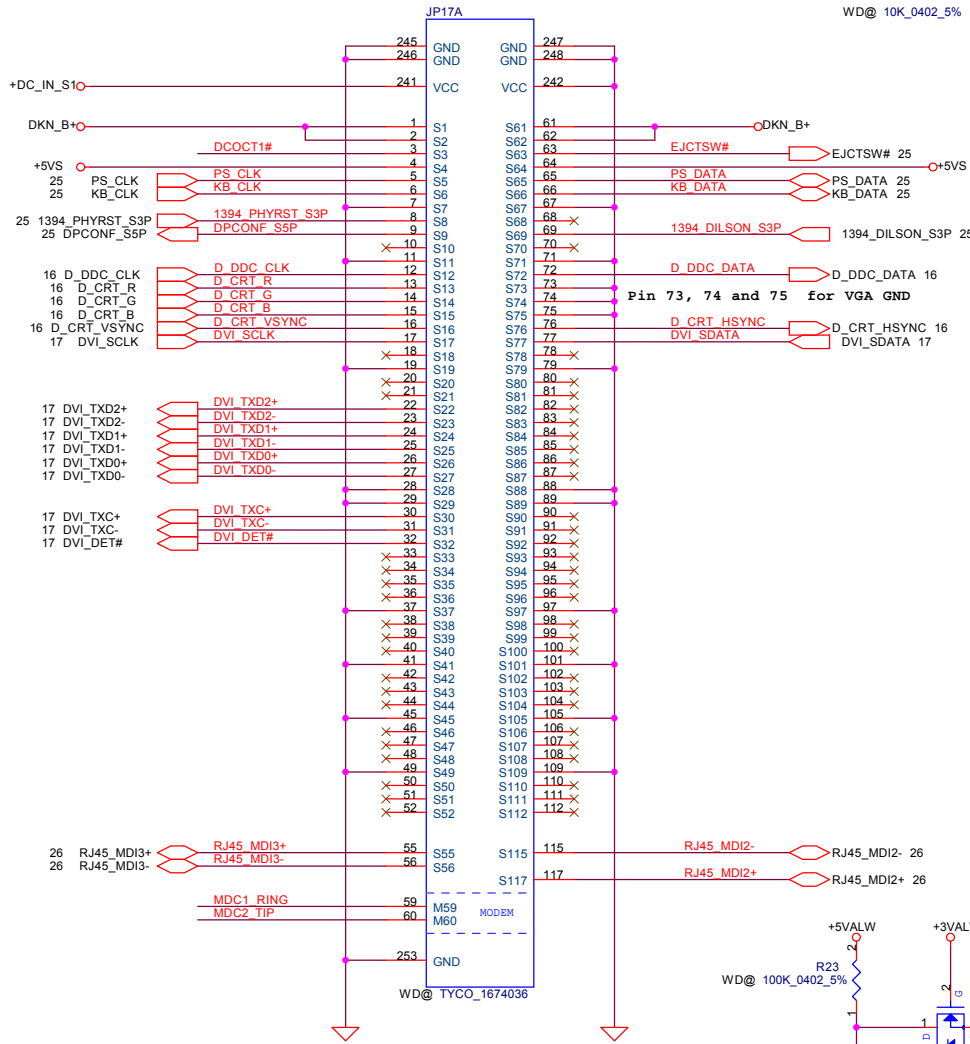
### Port 80 Debug Card Connector

**\*\***

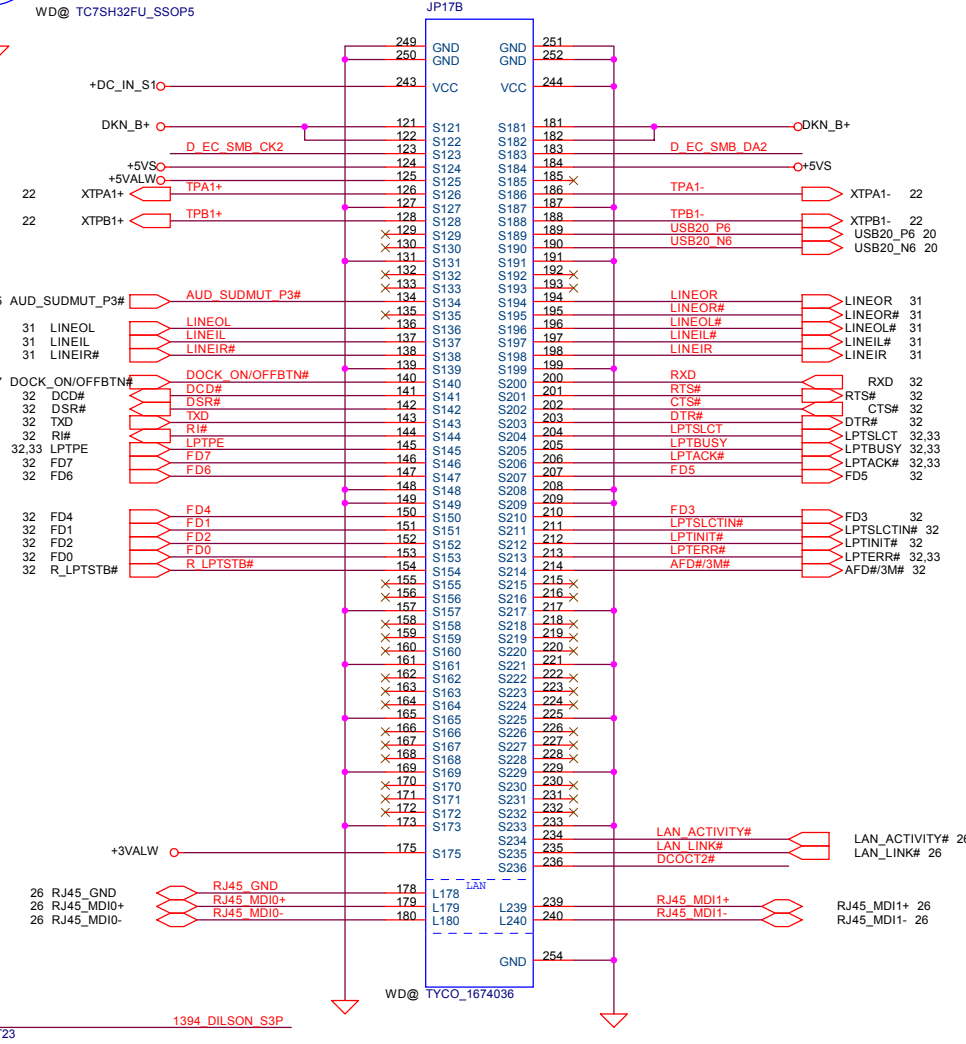
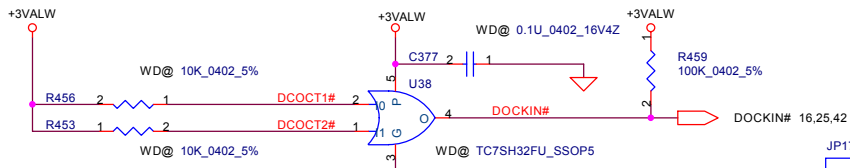
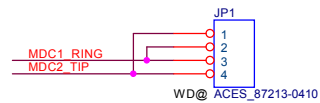


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				Date:	Thursday, September 15, 2005	Sheet 33 of 48

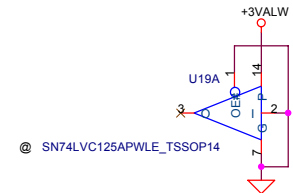
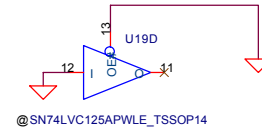
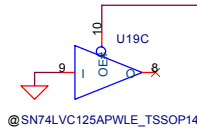
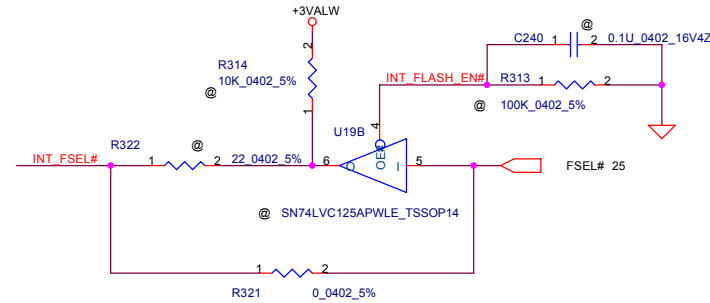
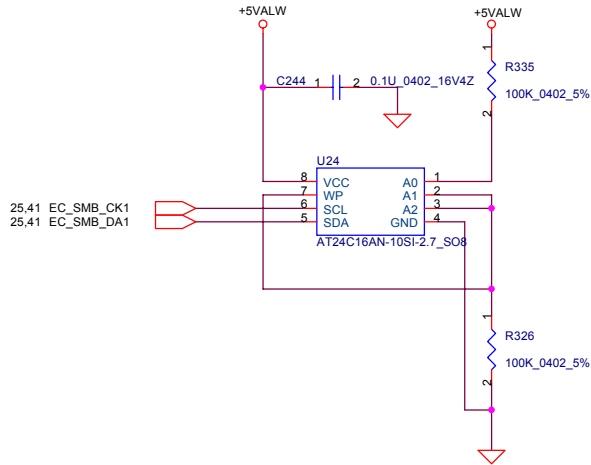
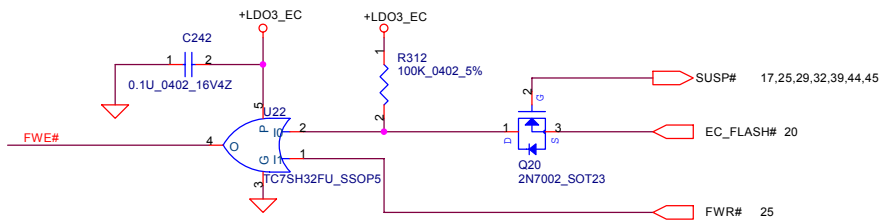
## Docking Conn.



## MDC to Docking Conn.



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								Size		Document Number		Rev	
										LA-3011P		0.2	
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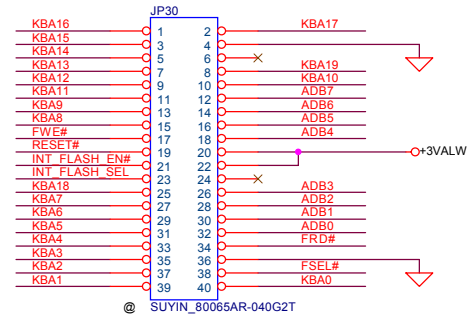
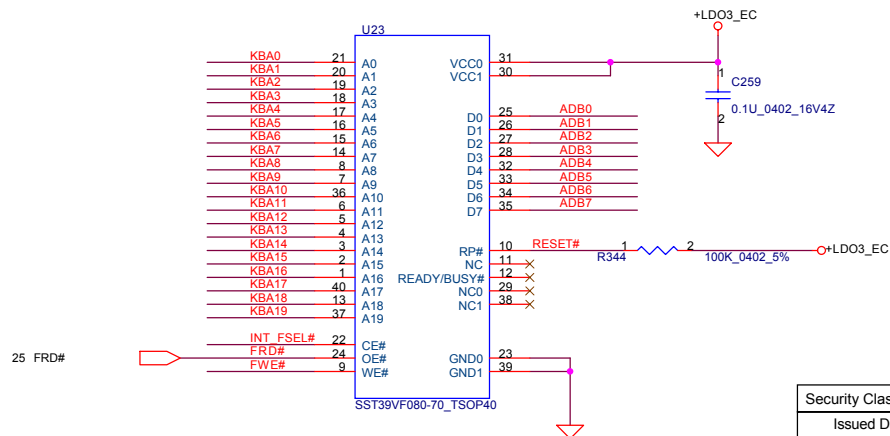


25 KBA[0..19] KBA[0..19]

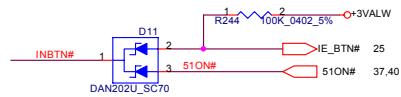
25 ADB[0..7] ADB[0..7]

## 1MB ROM Socket

## 1MB Flash ROM

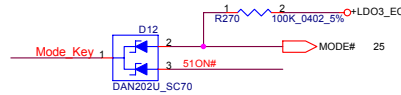


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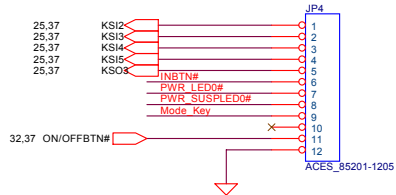


10C/10GC:Green:SC591UYG000  
10/10C:Blue:SC5191NB000

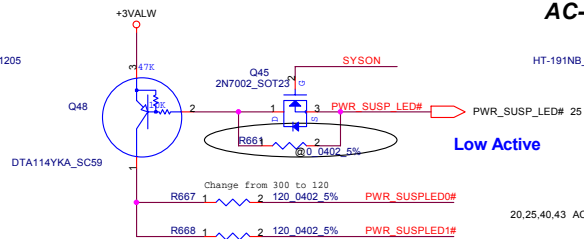
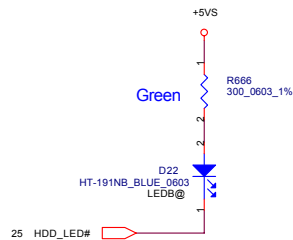
### Vivace(SW-DJ) Button



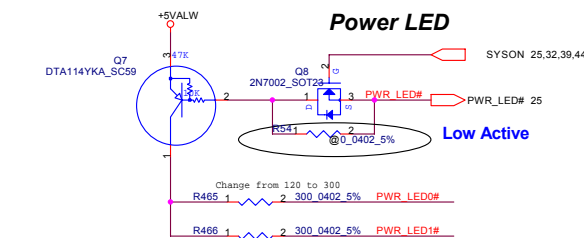
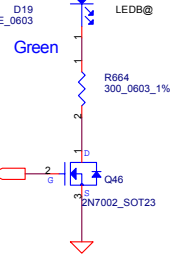
### PWR BTN/B



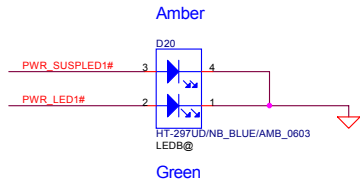
### HDD LED



### AC-IN LED



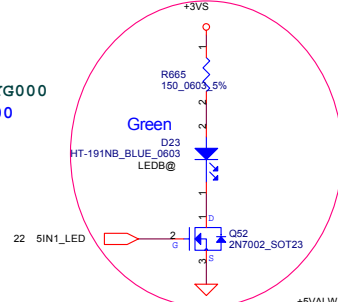
### Power LED



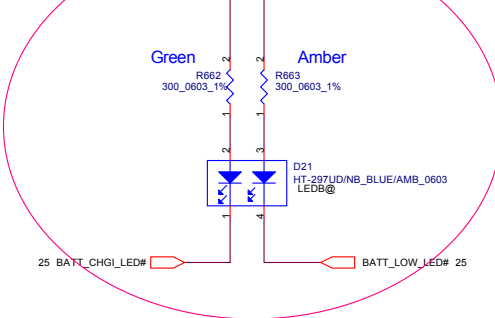
Amber

Green

### 5 In 1 Card LED (Close to Socket)

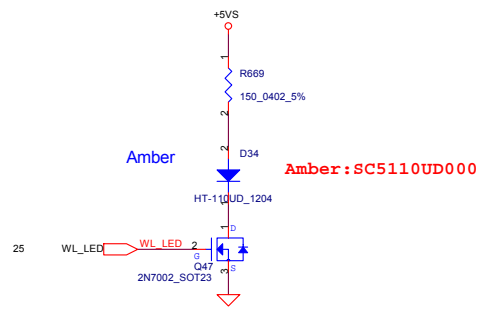


### Battery LED



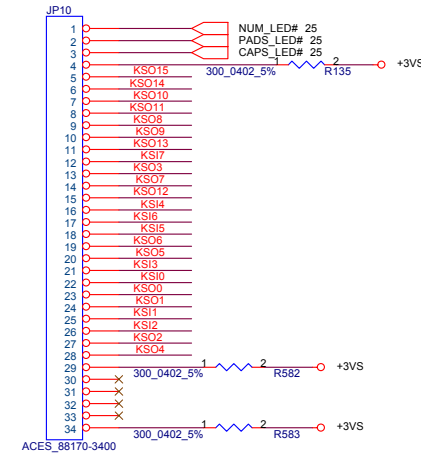
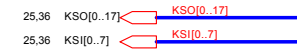
10/10C:Blue/Amber:SC597UDB000  
10C/10GC:Green/Amber:SC500001900

### Wireless Lan LED

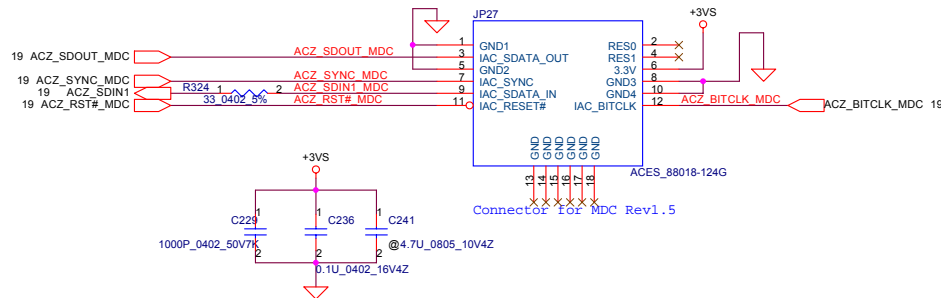


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# INT\_KBD CONN.



## MDC 1.5 Conn.



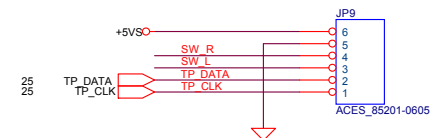
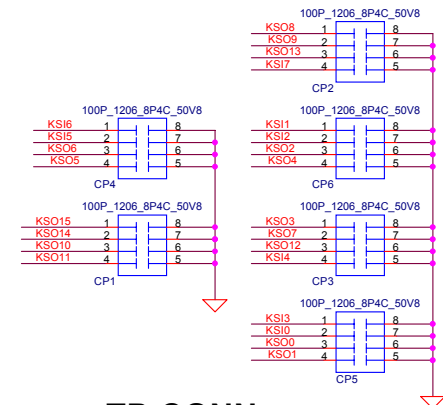
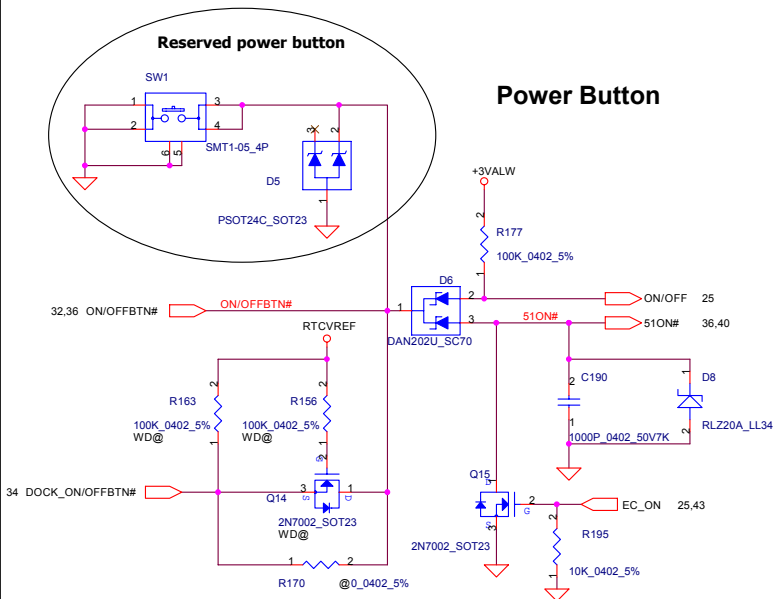
### Reserved power button

### Power Button

### Lid Switch

### TP CONN.

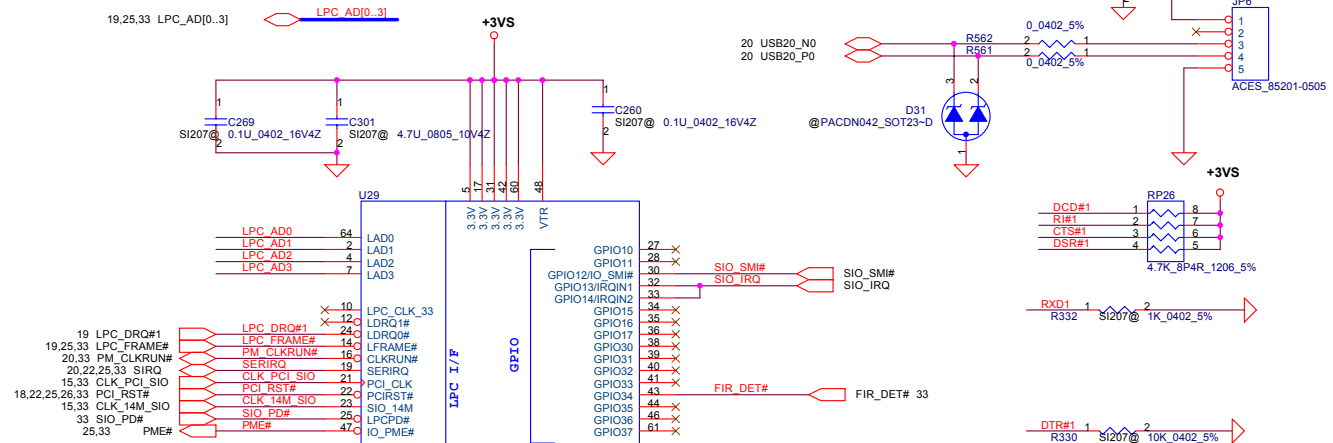
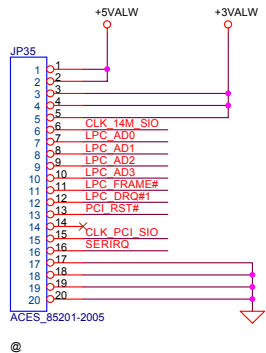
### TP Button



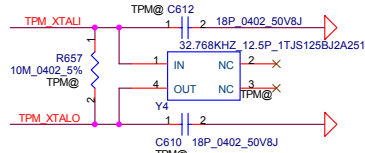
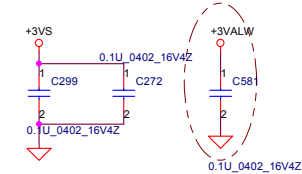
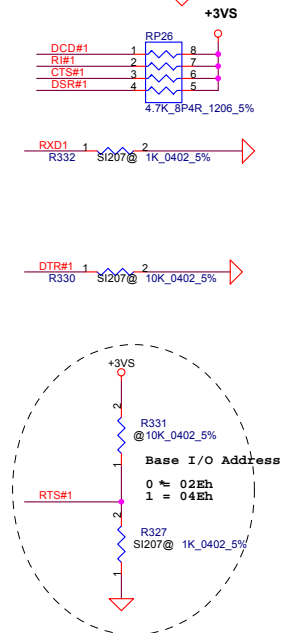
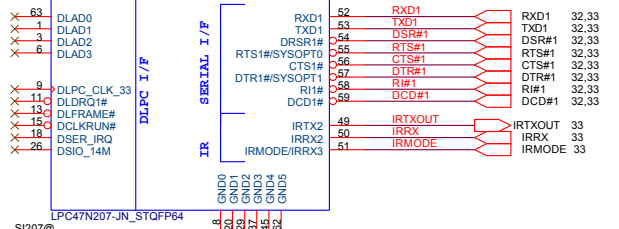
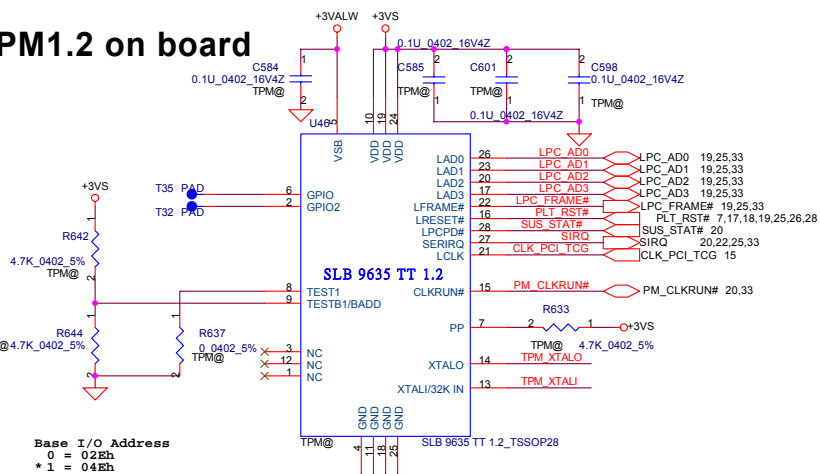
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## Finger printer

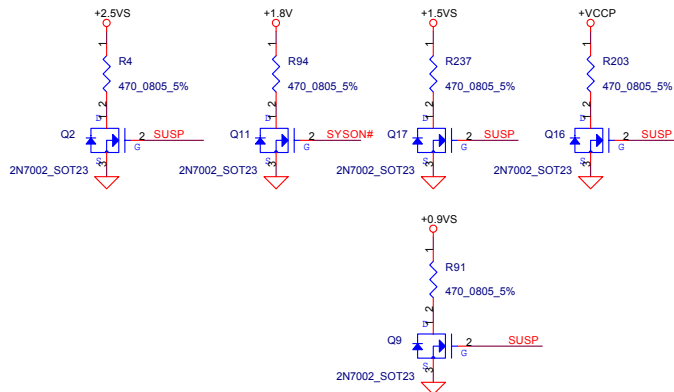
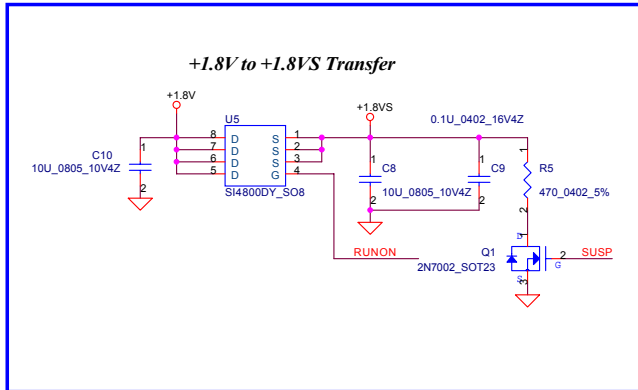
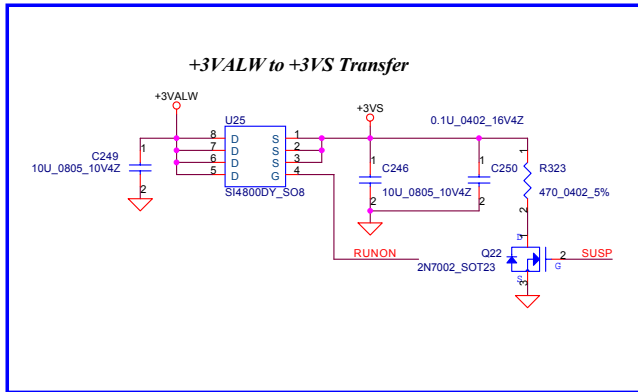
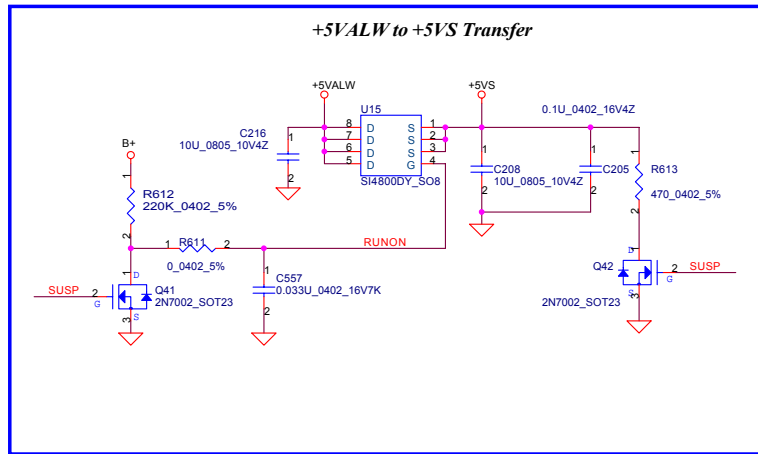
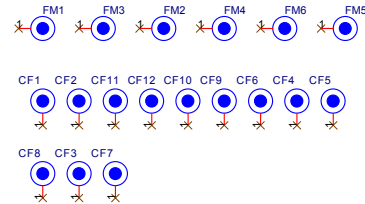
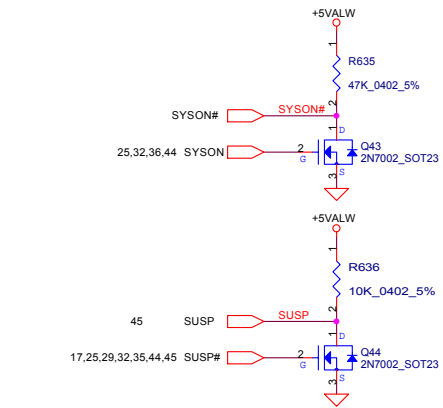
## LPC Debug Port



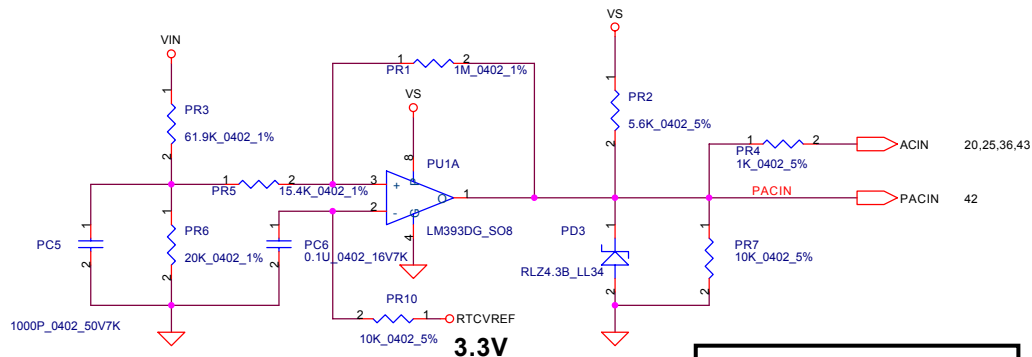
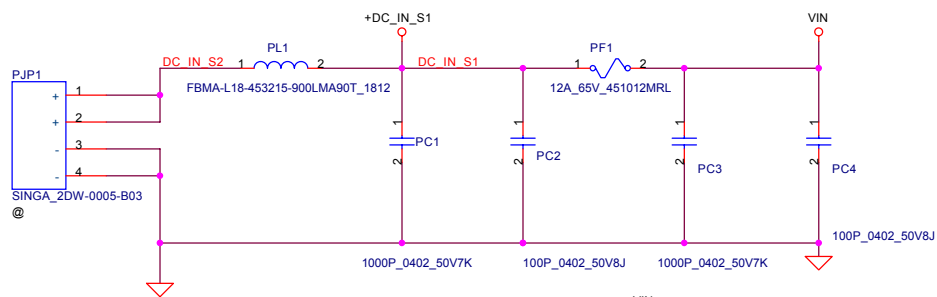
## TPM1.2 on board



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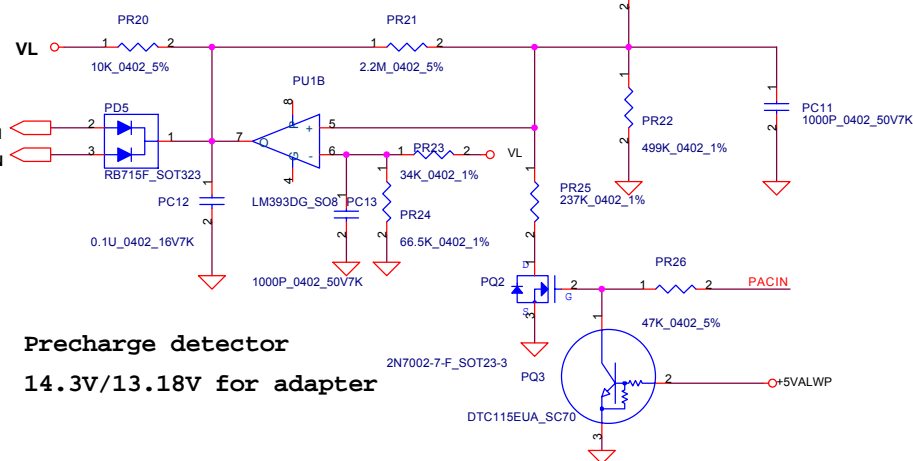
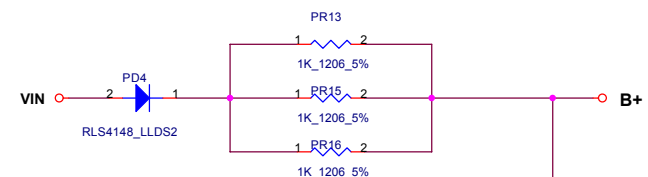
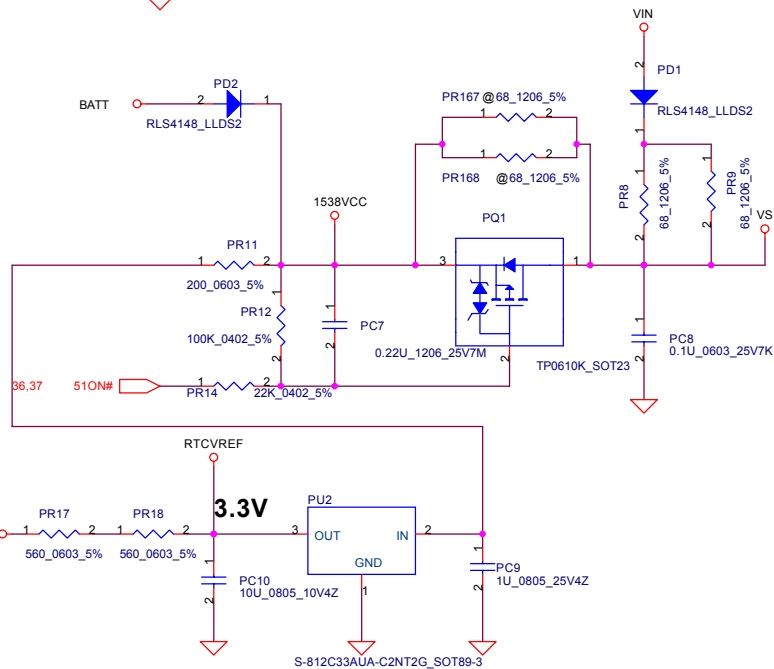


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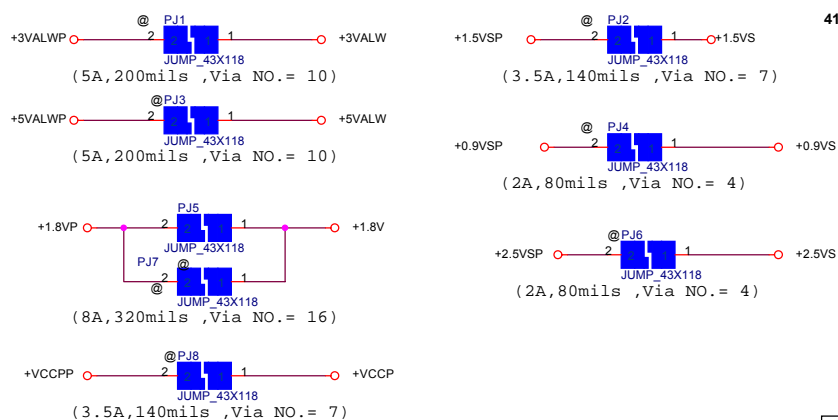


### Vin Detector

High 14.57 14.01 13.46  
Low 14.06 13.51 12.98



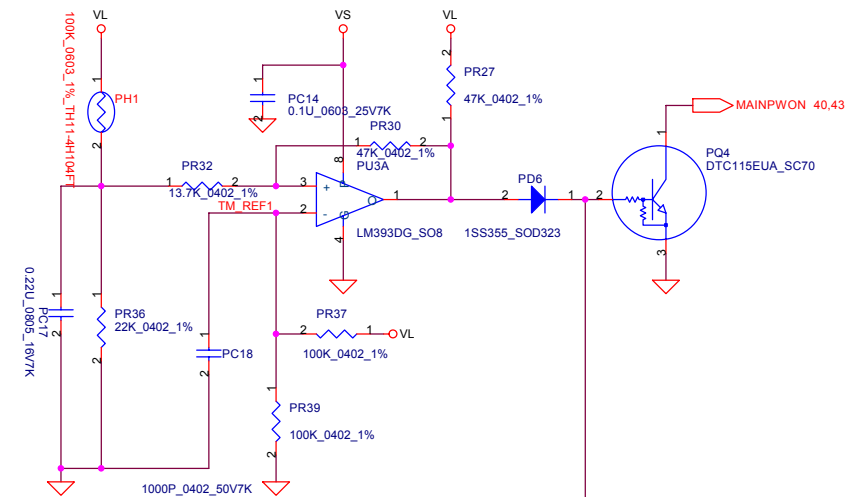
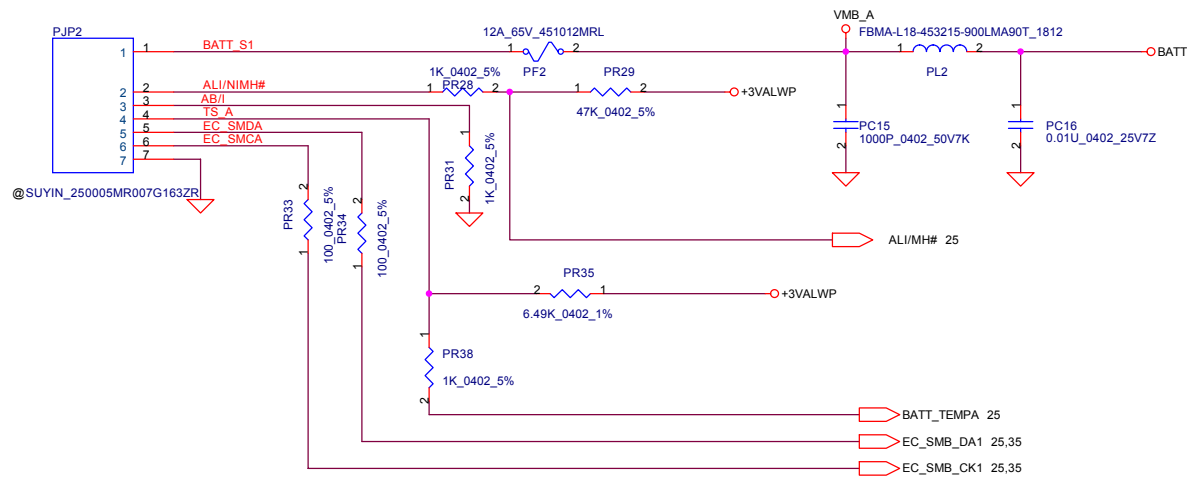
### Precharge detector 14.3V/13.18V for adapter



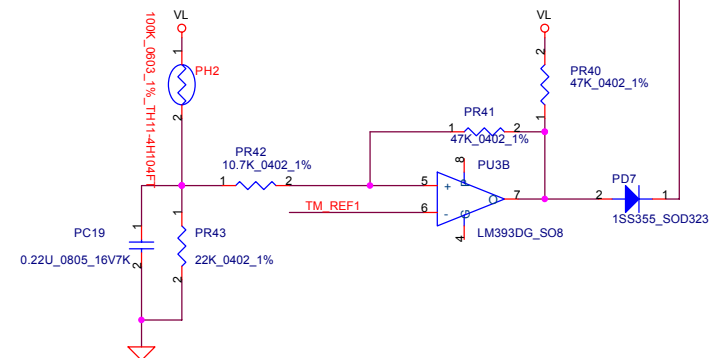
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Issued Date	2005/06/23	Deciphered Date	2006/06/23	Title DCIN & DETECTOR	
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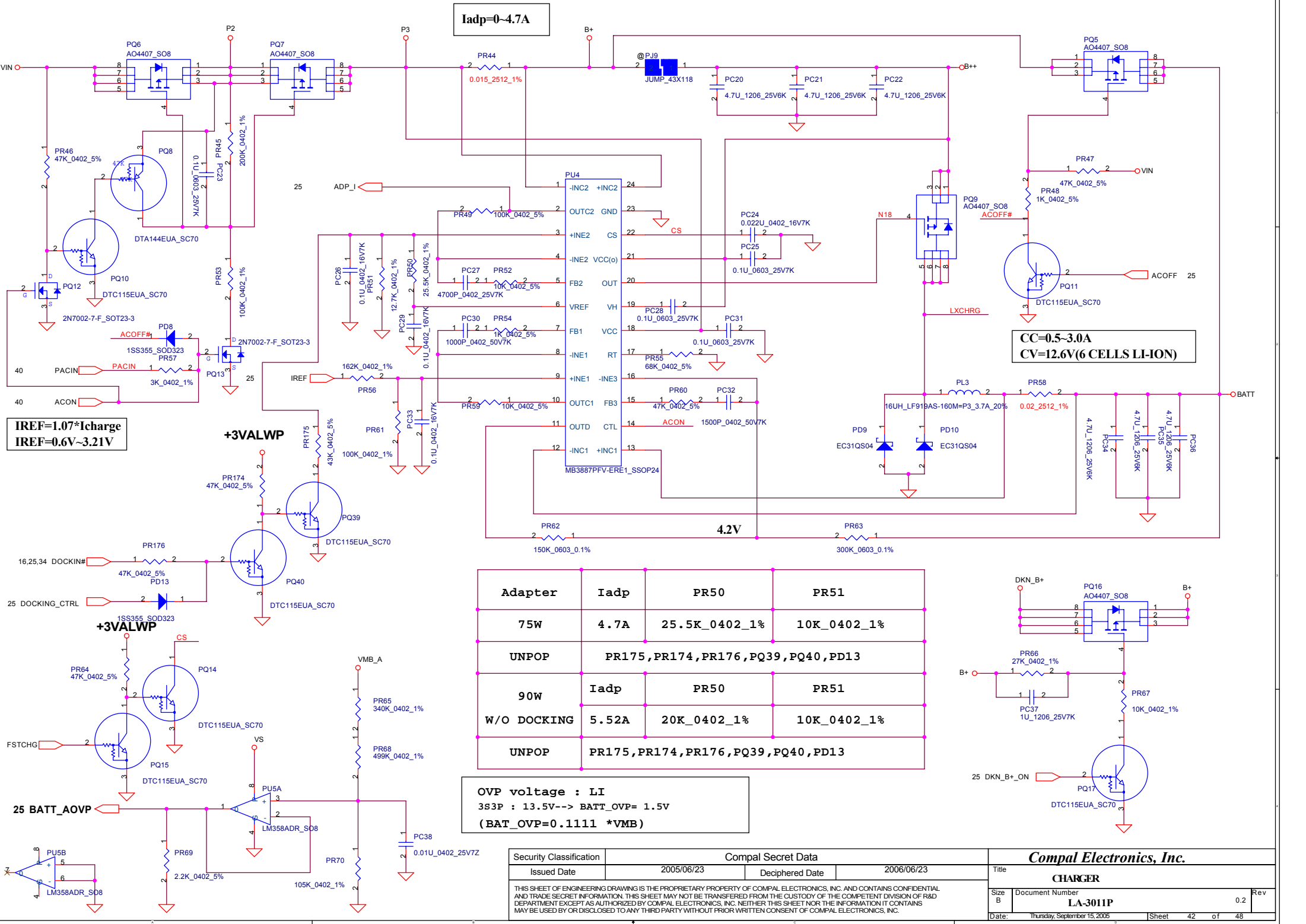
**PH1 under CPU botten side :**  
 CPU thermal protection at 84 degree C  
 Recovery at 45 degree C



**PH2 near main Battery CONN :**  
 BAT. thermal protection at 79 degree C  
 Recovery at 45 degree C



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Iadp=0-4.7A

CC=0.5-3.0A  
CV=12.6V(6 CELLS LI-ION)

IREF=1.07\*Icharge  
IREF=0.6V~3.21V

+3VALWP

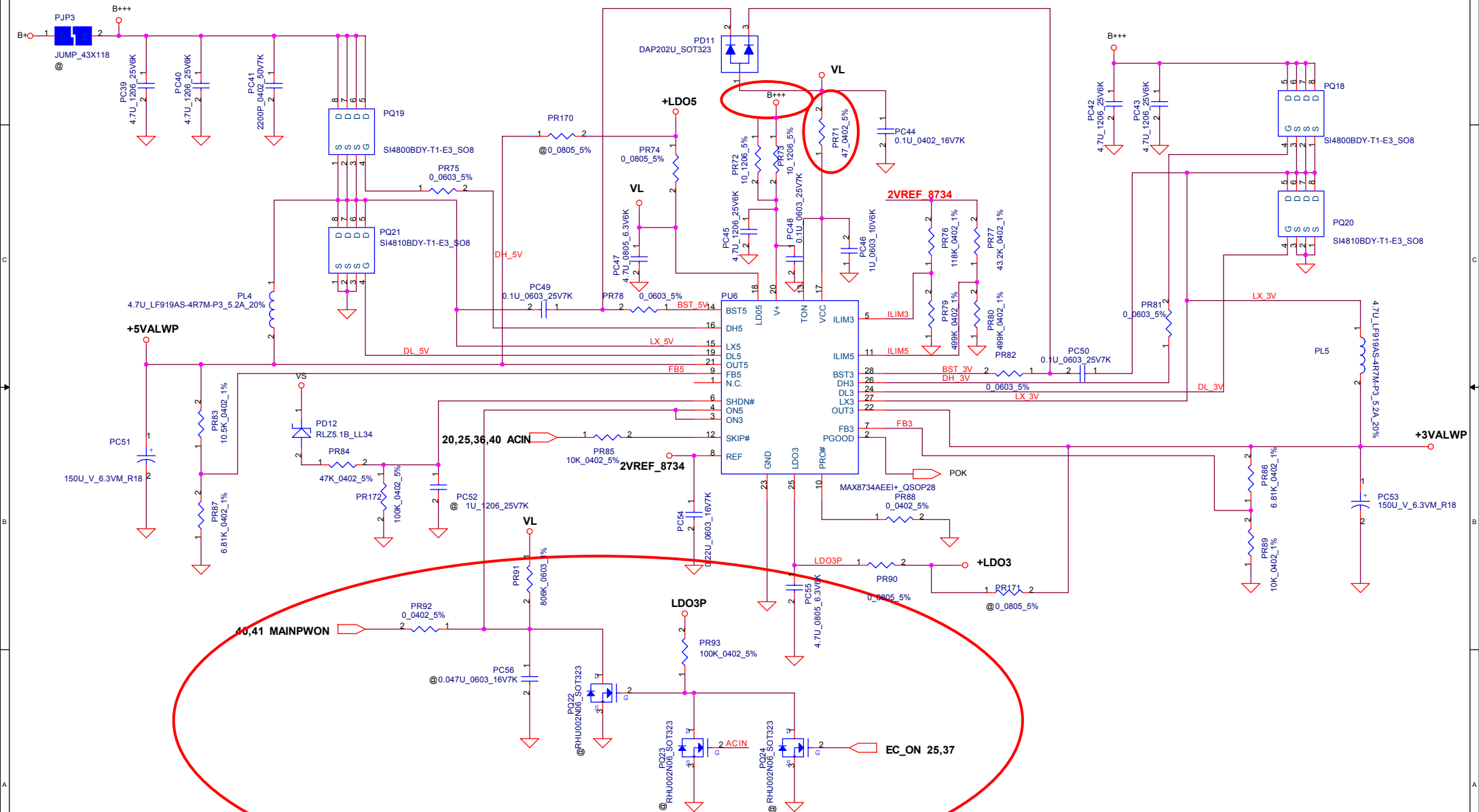
+3VALWP

Adapter	Iadp	PR50	PR51
75W	4.7A	25.5K_0402_1%	10K_0402_1%
UNPOP		PR175, PR174, PR176, PQ39, PQ40, PD13	
90W	Iadp	PR50	PR51
W/O DOCKING	5.52A	20K_0402_1%	10K_0402_1%
UNPOP		PR175, PR174, PR176, PQ39, PQ40, PD13	

OVP voltage : LI  
3S3P : 13.5V--> BATT\_OVP= 1.5V  
(BAT\_OVP=0.1111 \*VMB)

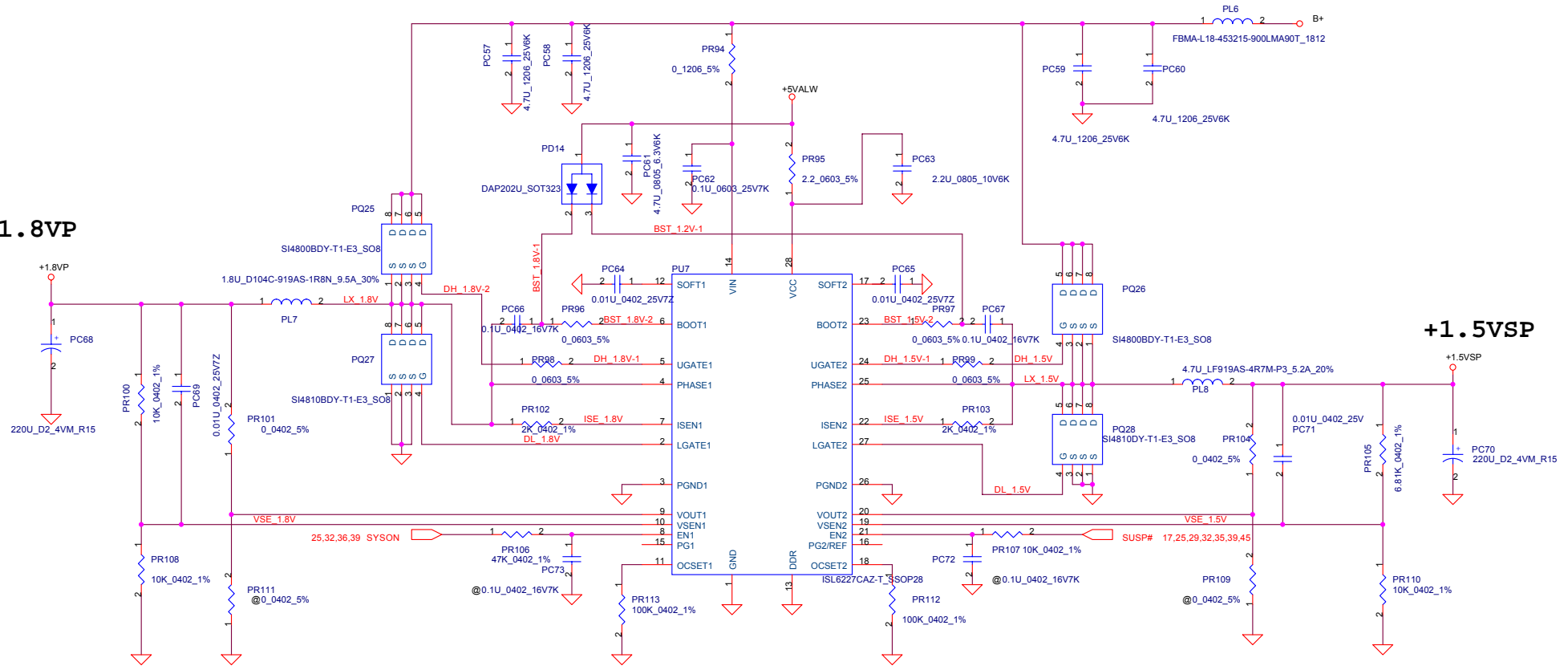
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# +3.3VALWP/+5VALWP



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Size	Document Number	0.2		Rev	
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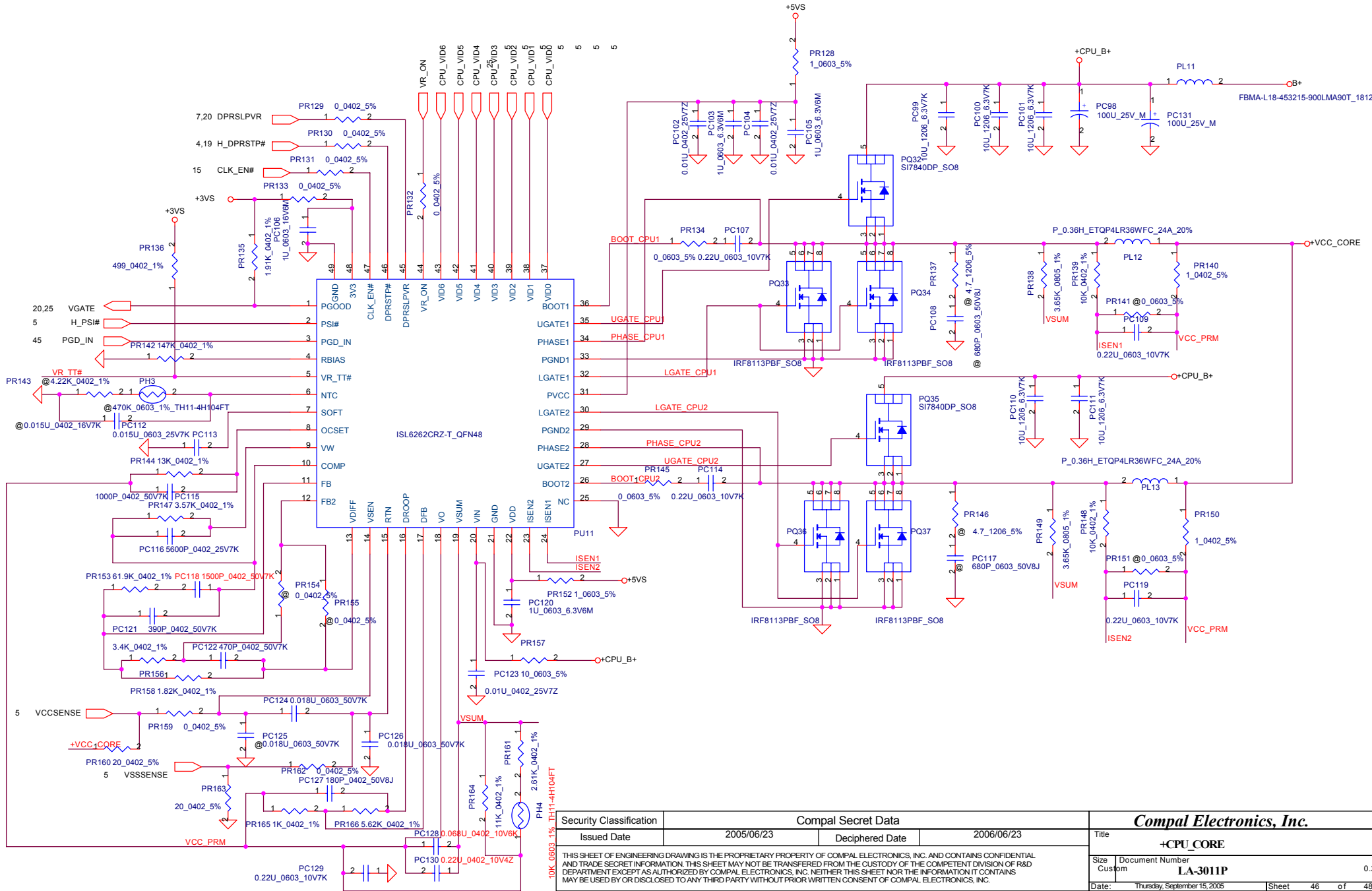
+1.8VP



+1.5VSP

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								Size		Document Number		Rev	
								Custom		LA-3011P		0.2	
								Date:		Thursday, September 15, 2006		Sheet 44 of 48	





10K\_0603 1% TH11-4H104FT

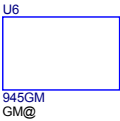
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2005/06/23	Deciphered Date	2006/06/23	Title
				+CPU_CORE	
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
8/8		P.15	Delete R589,R181,R190	No reserve those resistors
8/10		P.30	Add D35,R671	for G_beep function
8/10		P.25	Swap EC pin8 and Pin42	for G_beep function
8/11		P.30	Del R659,C613& Add D36	for G_beep function
8/16		P.7	unmount R503, R519	Intel Request
8/16		P.9	unmount R480, R478	Intel Request
8/16		P.11	unmount R514	Intel Request
8/16		P.20	Mount R249, Add R672,R673,R674	Intel Request
8/19		P.35	Add R675	For BIOS debug port
8/19		P.39	Modify R611, C557	For RUNON timing sequence
8/22		P.7	Add R676	Reserve for TS on SODIMM
8/22		P.28	Del U10,R128,R134,C162,C164,C169,C174,C175	Change G-sensor
8/23		P.28	Add C619,C620,C621,C622,C623,C624,C625,C626,C627	
8/23		P.28	Add R677,R678,R679,R680,R681,R682,R683,R684,R685,R686	
8/23		P.28	Del x_sensor, y_sensor, z_sensor connection to EC	G-sensor circuit modification
8/23		P.28	Add Q49,Q50,U50,U51,U52,Y5	For New G-sensor solution
8/24		P.17	Change JP18.40 to +5VALW	
8/24		P.29	Change U33.8 to SUSP#	
8/24		P.29	Change U33.8 to SUSP#	
8/25		P.16	Change D27,D28,D29 pin 3 to +2.5VS	for Intel's suggestion
8/25		P.37	Change JP9 connector to 6pin	To meet ME's definition
8/25		P.15	J10 change to Jump 43*79	for DFX request
8/25		P.19	CMOS_CLR1 change to Jump 43*79	for DFX request
8/30		P.39	Modify Screw holw location	
8/30		P.22	To correct MSBS_SDCMD_SMWE#/SDWP#_SMCE# signals	
8/30		P.39	Change R612=220K,C557=0.033uF,R611=0ohm	for power on sequence
9/2		P.29	Add EC_HDPPD to U14.24 and R682	G-sensor circuit modification
9/5		P.09	Swap CRT_R & CRT_B To fix CRT issue of GM	
9/8		P.20	Change LAN_Disable from GPIO15 to GPIO28	
9/9		P.26	Swap RX /TX signals	
9/9		P.25	Swap EC pin8 & Pin42	for follow EVT pin definition
9/9		P.29/30	To separate Line out and HP signals	
9/12		P.30	D35/D36 change to Diode 4148	
9/12		P.30	Add R687 ,Q51	
9/12		P.29	Add R688,C628	
9/12		P.24	Change JP34 connector to ACES_87213-1000	
9/12		P.29	Delete R395	
9/12		P.16	Change F1 to SP04301P000	
9/13		P.38	Reserve SIO_SMI#/SIO_IRQ signals	
9/13		P.38	Reserve JP35 for BIOS debug	
9/14		P.22	Add Q52 for 5in1 LED	

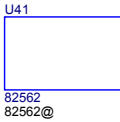
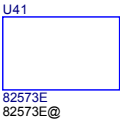
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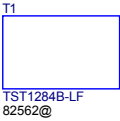
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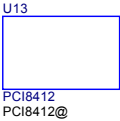
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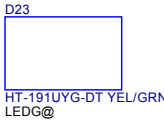
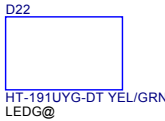
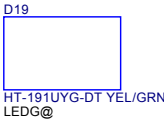
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