

Beyonce UMA Schematics Document


uFCPGA Mobile Merom

Intel Crestline-GM + ICH8M

2008-02-21

REV : -2 (DELL:A00)

DBS

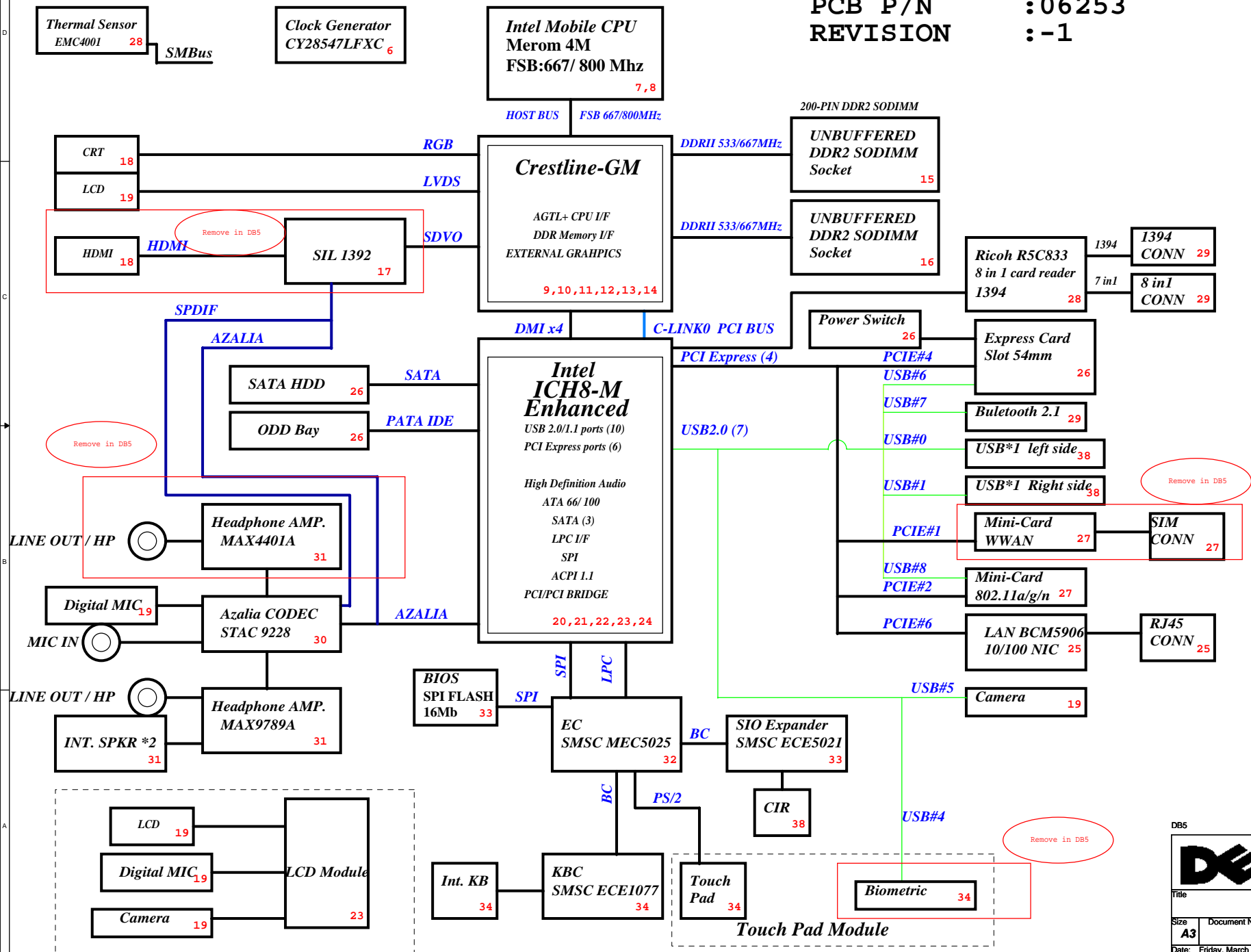
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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Beyonce UMA Block Diagram

Project code:91.4C301.001

PCB P/N : 06253

REVISION : -1



System DC/DC		41
TPS51120		
INPUTS	OUTPUTS	
+PWR_SRC	+5V_ALW +5V_SUS +3.3V_SUS +3.3V_RTC_LDO	
System DC/DC		42
TPS51124		
+PWR_SRC	+1.05V_VCCP +1.5V_RUN	
DDR2 DC/DC		43
TPS51117		
+PWR_SRC	+1.8V_SUS	
LDO		43
TPS51100		
+1.8V_SUS	+0.9V_DDR_VTT V_DDR_MCH_REF	
LDO		44
SC339SKTRT		
+PWR_SRC	+1.25V_RUN	

Battery Charger MAX8731		38
<i>INPUTS</i>	<i>OUTPUTS</i>	
+PWR_SRC	+VCHGR	

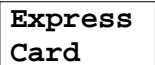
CPU DC/DC ISL6260C		39,40
INPUTS	OUTPUTS	
+PWR_SRC	+VCC_CORE	

PCB LAYER
L1:TOP
L2:GND
L3:Signal
L4:Signal
L5:VCC
L6:Signal
L7:GND
L8:BOT

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Beyonce UMA			
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ICH8-M

[illegible]

SMBus address:D2

Capacity Button Board

SMBus address:86

SIO
MEC5025

Battery Conn.

SMBus address:16

Charger

SMBus address:12

Thermal

```
SMBus address:5E
```

INVERTER

LVDS

SMBus address:72

sil 1932

HDMI CONN

CLOCK GEN CY28547

27M_SS/LCD96_100M SELECTION TABLE

BYTE 10

bits S1	Bit4 S0	Spread Spectrum S(110)
0	0	-0.5%(Default)
0	1	-1.0%
1	0	-1.5%
1	1	-2.0%

Bit2 IO_VOUT2	Bit1 IO_VOUT1	Bit0 IO_VOUT0	IO_VOUT[2,1,0]
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V(Default)
1	1	0	0.9V
1	1	1	1.0V

PIN34 FCTSEL1	0 UMA	1 DISC.
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSusi1_05 VccSusi1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSusi1_05,VccSusi1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

INTEL CRESTLINE STRAP PIN

* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation*	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation*

PCIE Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	No use
LANE4	Express Card
LANE5	No use
LANE6	10/100 LOM

ICH USB TABLE

USB0	USB1
USB1	USB2
USB2	
USB3	
USB4	Biometric
USB5	Camera
USB6	Express Card
USB7	BT
USB8	
USB9	MINI Card WWAN

PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD17	C D	1	1

INTEL ICH8-M INTEGRATED
PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

XOR Chain Entrance Strap		
ICH_RSVDtp3	AZ_DOUT ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable	
	high = default	
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	DCT
1	1	LPC(Default)

Integrated VccSusi1_05,VccSusi1_5,VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

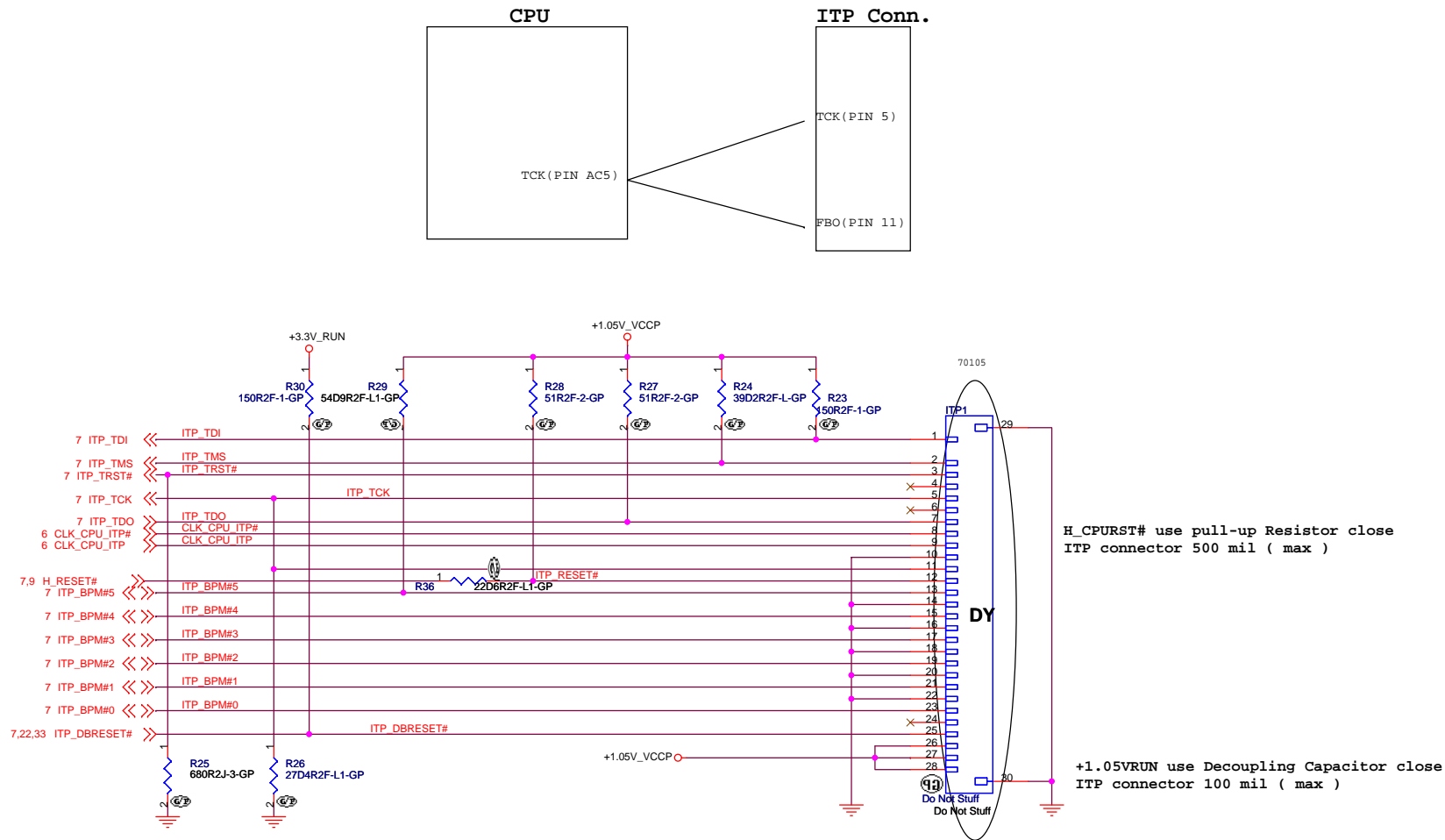
DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

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Beyonce UMA		
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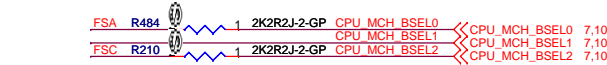
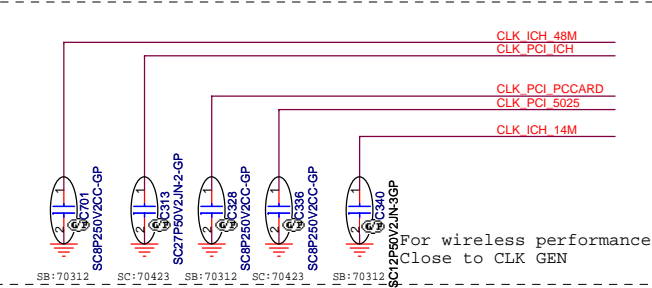
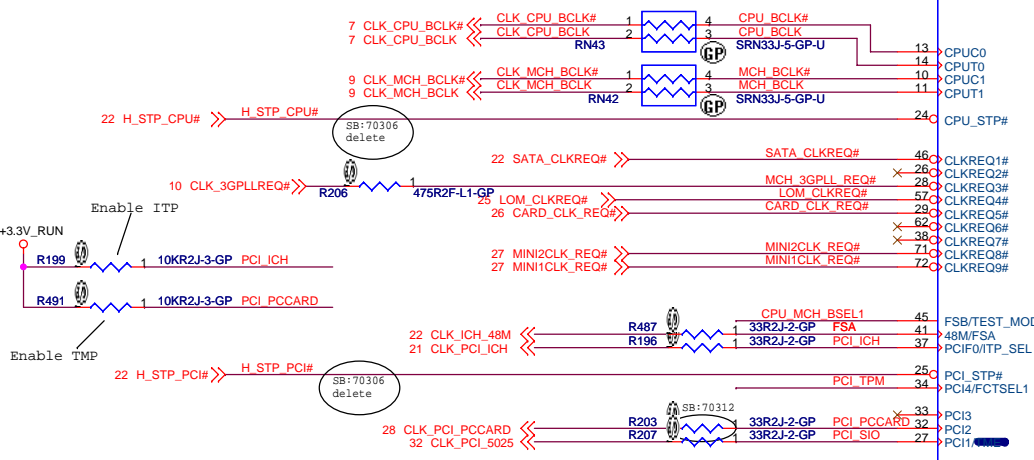
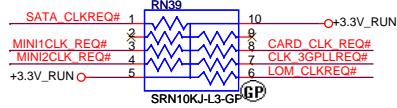
ITP Debug Conn.

DB5

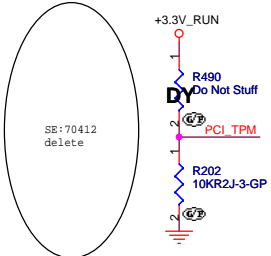


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CLKREQ PULL HIGH



SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M



ICS: 71.09333.A03 ICS9LPR333CKLFT
SB: 70216

PIN34	0 UMA	1 DISC.
FCTSEL1		
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

PIN9	PIN39
PGMODE	DISCRIPTION
0	VTT_PWRGD#/PD
1	CKPWRGD/PD# (DEFAULT)

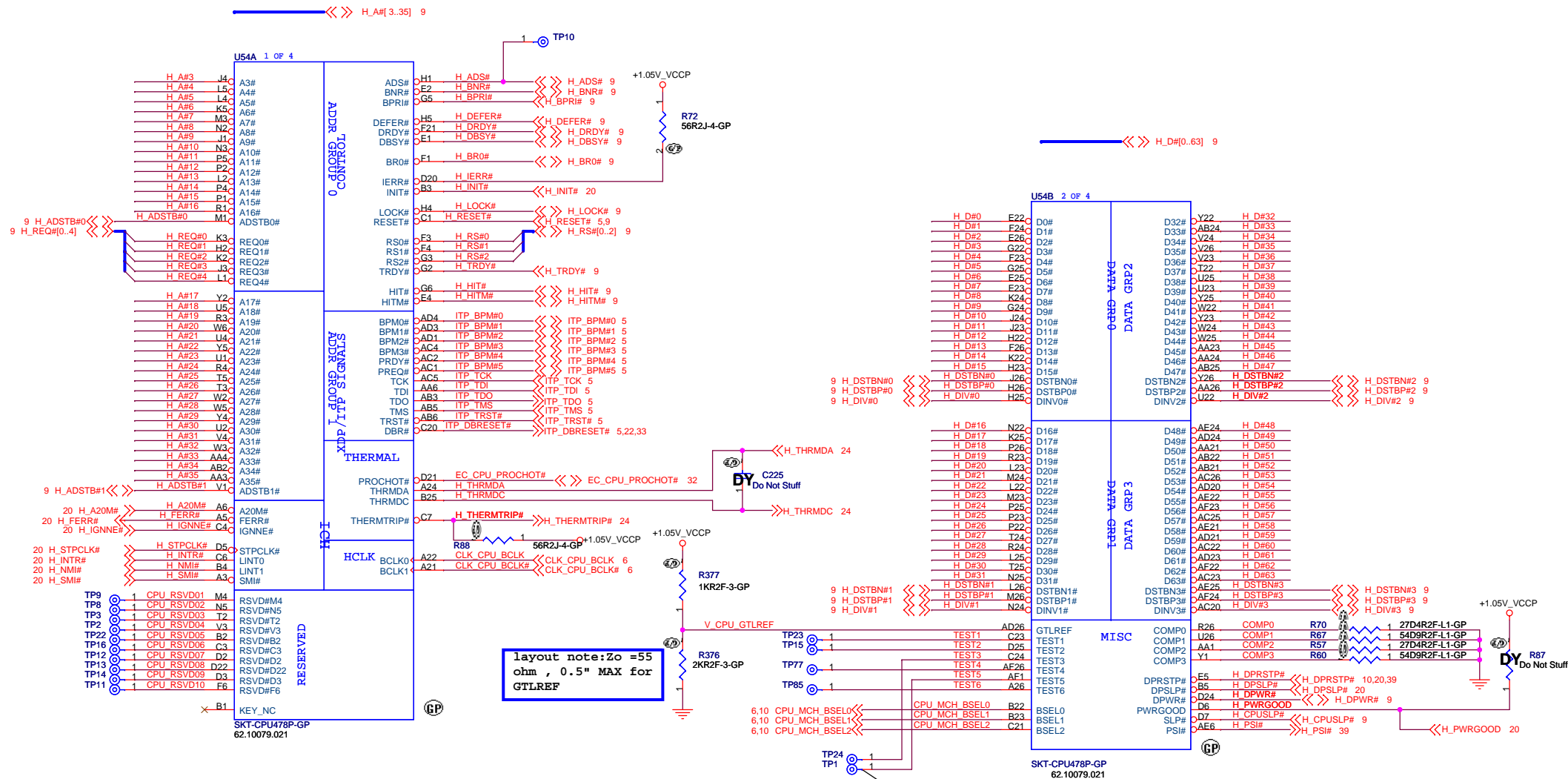
D85

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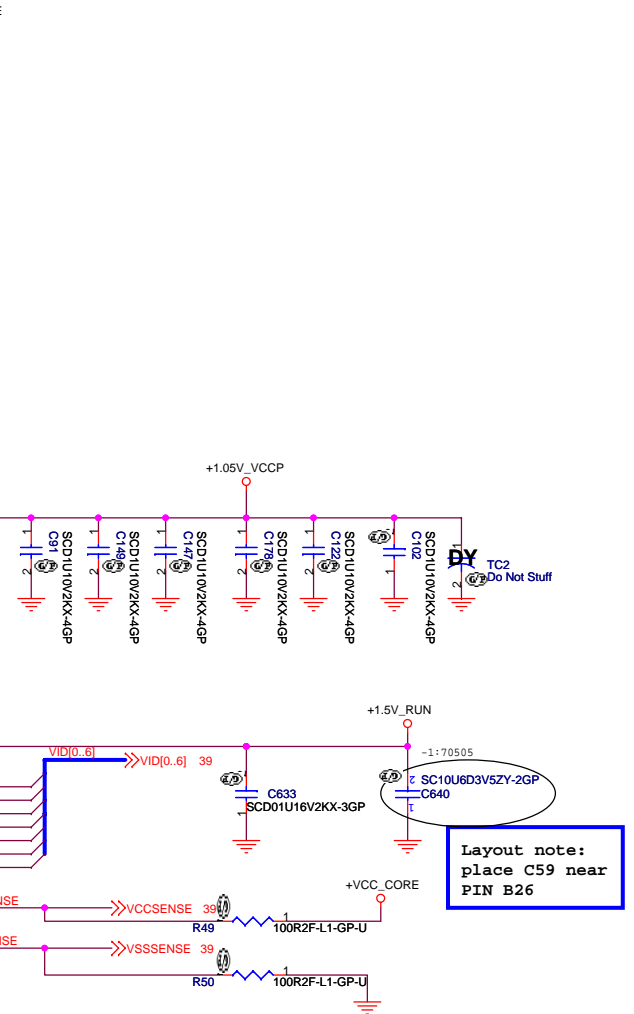
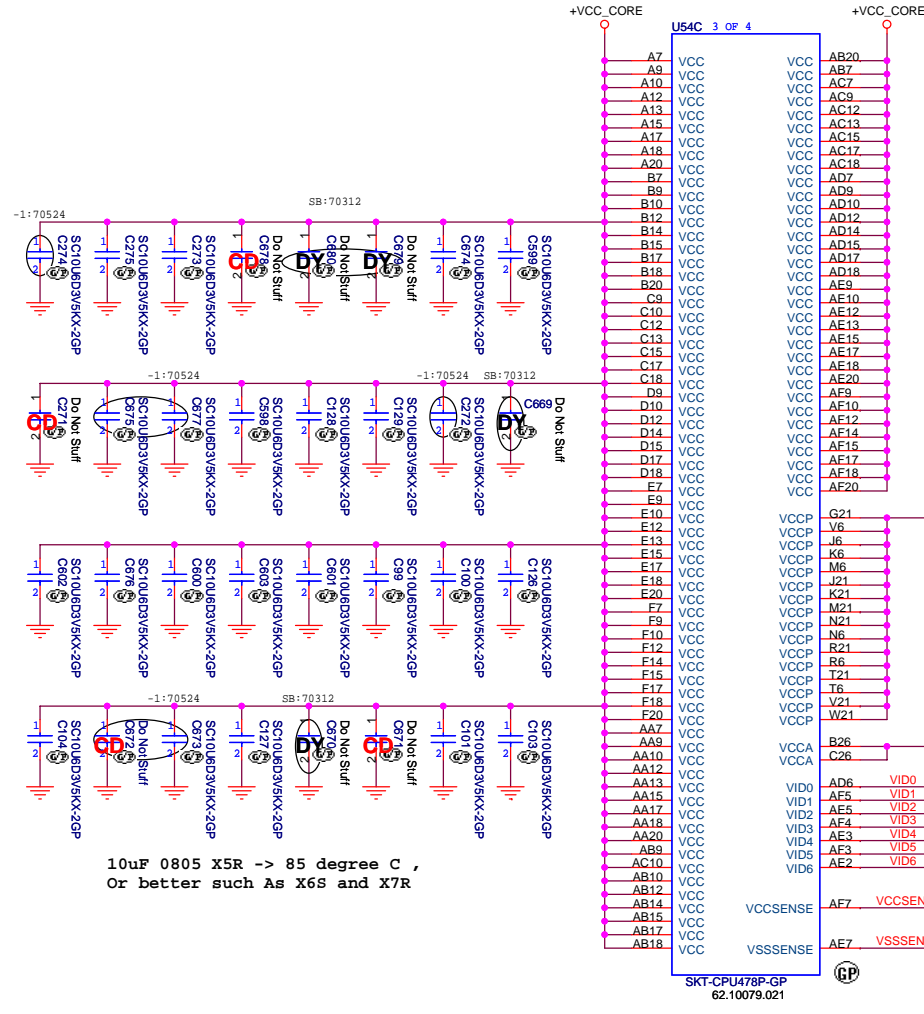
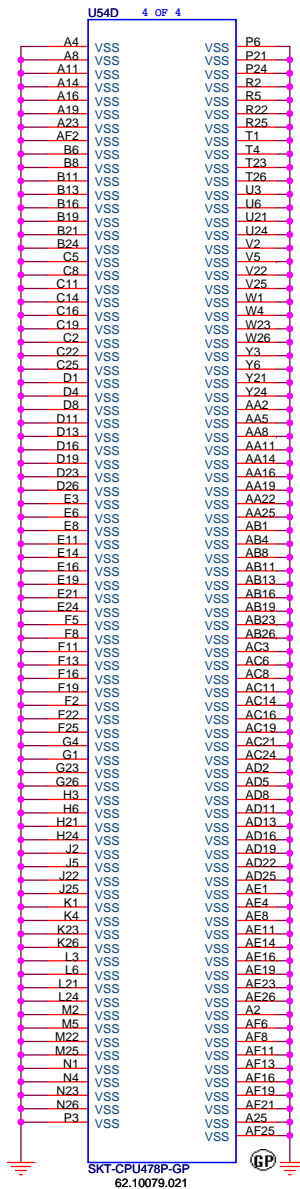
Title: **Beyonce UMA**

Size: **A3** Document Number: **CLK_GEN CY28547** Rev: **-3**

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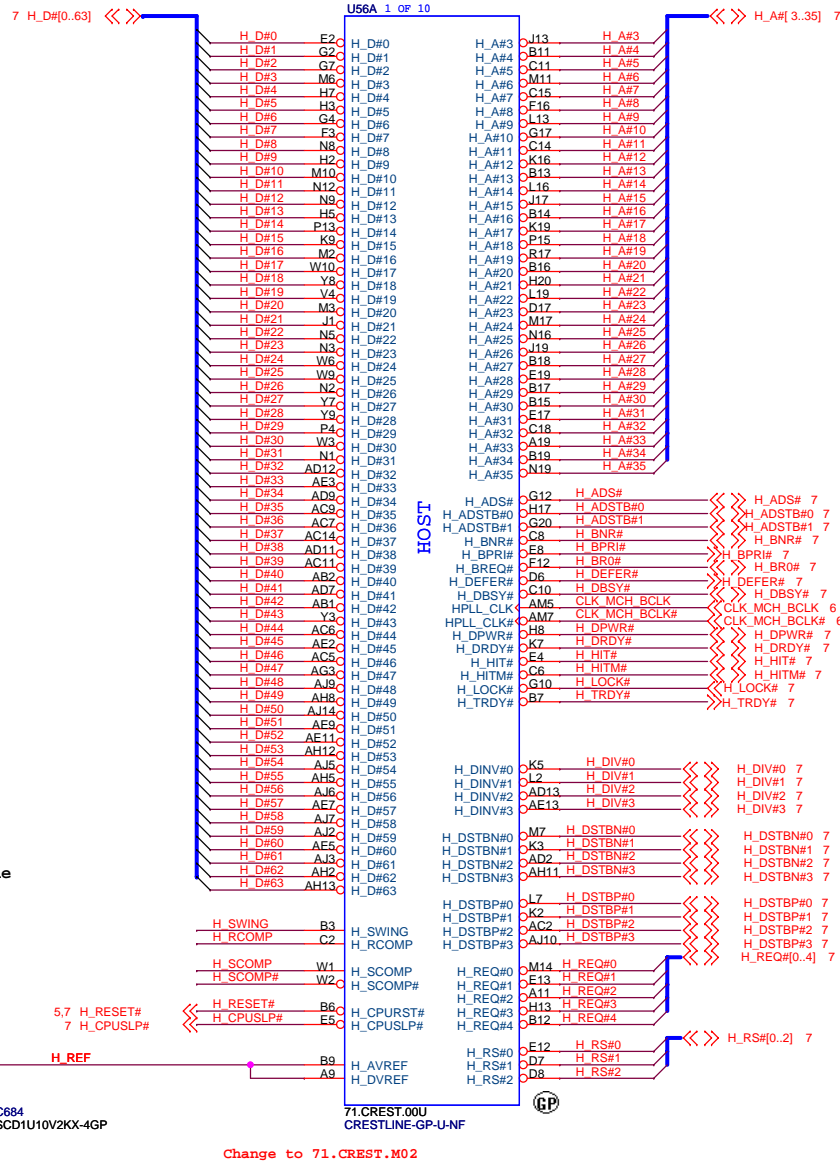
Use old Symbol replace New P/N
original value:SKT-CPU478P-GP



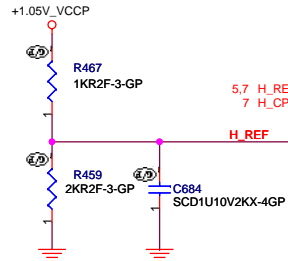
10uF 0805 X5R -> 85 degree C ,
Or better such As X6S and X7R

Layout note:
Place R53 and R54 within 1" of CPU.
Routing VCC_SENSE and VSS_SENSE at
27.4 ohms with 50 mils spacing.

Layout note:
place C59 near
PIN B26



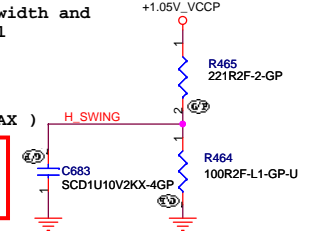
H_REF Decoupling Crestline
close Crestline 100 mil



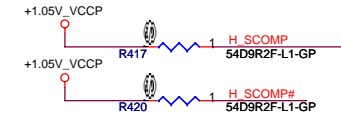
H_SWING routing Trace width and
Spacing use 10 / 20 mil

H_SWING Resistors and
Capacitors close
Caliistoga 500 mil (MAX)

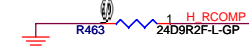
From Schematic Design
Checklit v.1201
221 1% pull high 100
1% pull low



H_SCOMP and H_SCOMP# Resistors
and Capacitors close Caliistoga
500 mil (MAX)
Zo=55ohms



H_RCOMP routing Trace width and
Spacing use 10 / 20 mil



D85

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Title

Beyonce UMA

Size

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GMCH-FSB LIBC (1/6)

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Wednesday, February 27, 2008

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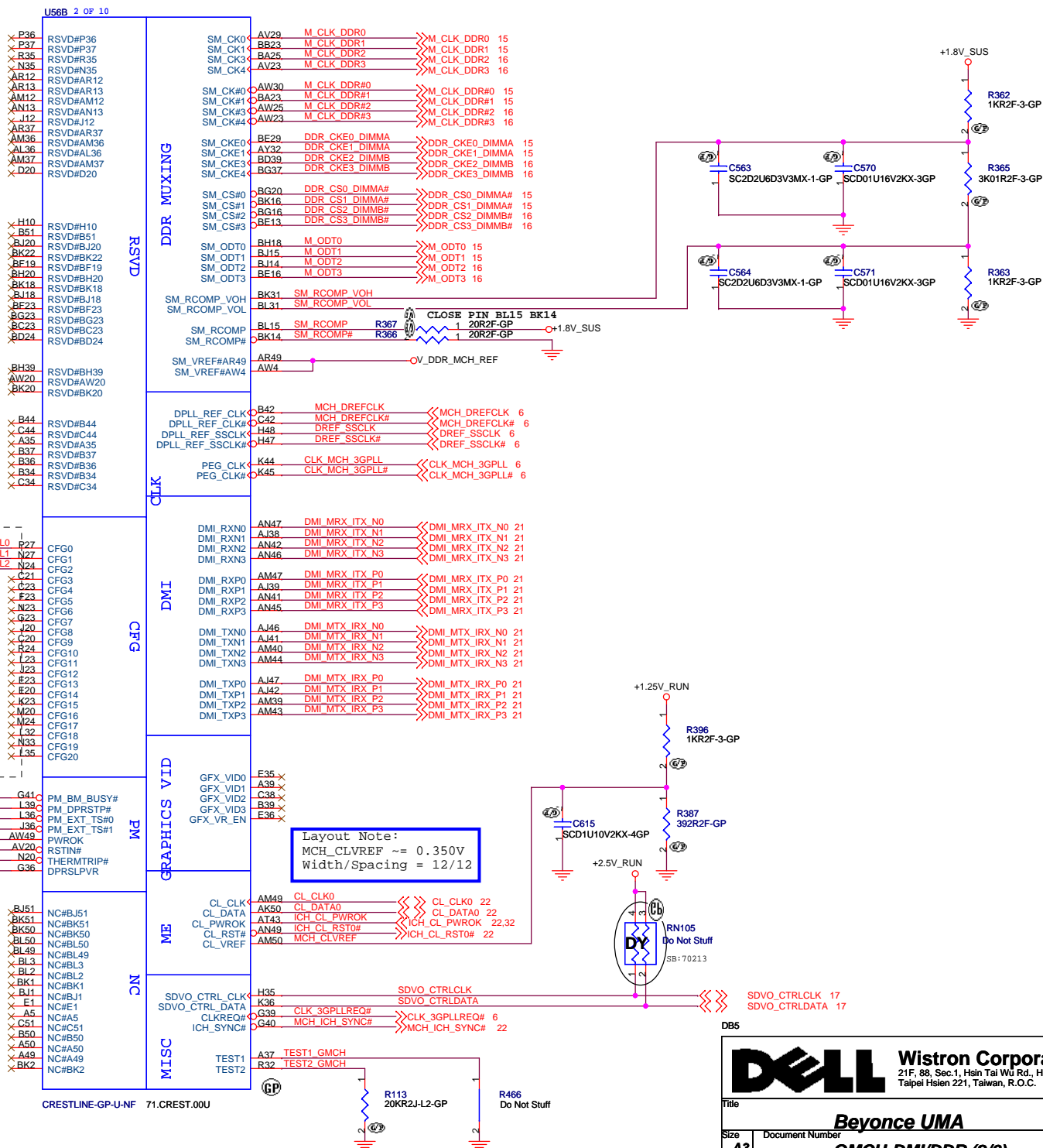
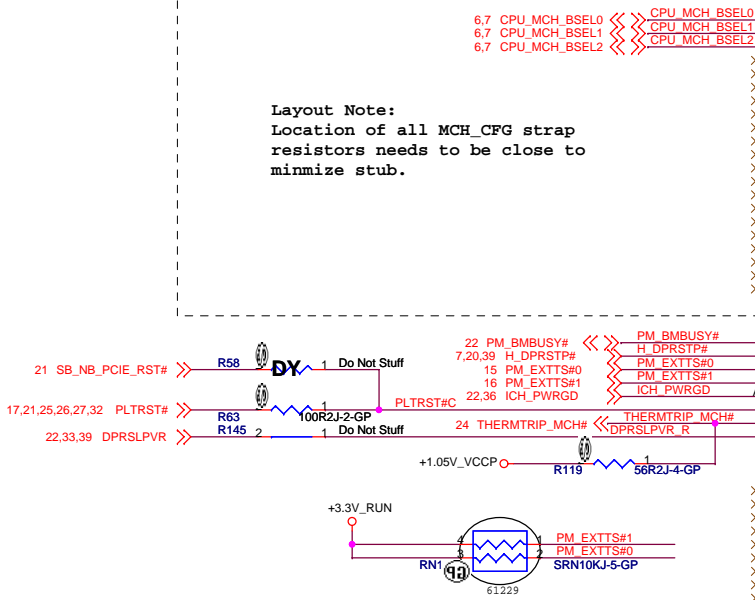
-3

* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation *	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation*
	CFG[2..0] FSB Select
LHL	FSB 800
LHH	FSB 667
Other	Reserved

Layout Note:
Location of all MCH_CFG strap
resistors needs to be close to
minimize stub.



15 DDR_A_D[0.63] <<>> DDR_A D[0.63]

DDR A D0	AR43
DDR A D1	AW44
DDR A D2	BA45
DDR A D3	AY46
DDR A D4	AR41
DDR A D5	AR45
DDR A D6	AT42
DDR A D7	AW47
DDR A D8	BA45
DDR A D9	BF48
DDR A D10	BG47
DDR A D11	BJ45
DDR A D12	BB47
DDR A D13	BG50
DDR A D14	BH49
DDR A D15	BE45
DDR A D16	AW43
DDR A D17	BE44
DDR A D18	BG42
DDR A D19	BE40
DDR A D20	BE44
DDR A D21	BH45
DDR A D22	BG40
DDR A D23	BF40
DDR A D24	AR40
DDR A D25	AW40
DDR A D26	AT39
DDR A D27	AW36
DDR A D28	AW41
DDR A D29	AY41
DDR A D30	AV38
DDR A D31	AT38
DDR A D32	AV13
DDR A D33	AT13
DDR A D34	AW11
DDR A D35	AV11
DDR A D36	AU15
DDR A D37	AT11
DDR A D38	BA13
DDR A D39	BA11
DDR A D40	BE10
DDR A D41	BD10
DDR A D42	BD8
DDR A D43	AY9
DDR A D44	BG10
DDR A D45	AW9
DDR A D46	BD7
DDR A D47	BB9
DDR A D48	BB5
DDR A D49	AY7
DDR A D50	AT5
DDR A D51	AT7
DDR A D52	AY6
DDR A D53	BB7
DDR A D54	AR5
DDR A D55	AR8
DDR A D56	AR9
DDR A D57	AN3
DDR A D58	AN8
DDR A D59	AN10
DDR A D60	AT9
DDR A D61	AN9
DDR A D62	AM9
DDR A D63	AN11

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DDR SYSTEM MEMORY A

SA_DQ0	SA_BS0
SA_DQ1	SA_BS1
SA_DQ2	SA_BS2
SA_DQ3	
SA_CAS#	
SA_DM0	
SA_DM1	
SA_DM2	
SA_DM3	
SA_DM4	
SA_DM5	
SA_DM6	
SA_DM7	
SA_DQS0	
SA_DQS1	
SA_DQS2	
SA_DQS3	
SA_DQS4	
SA_DQS5	
SA_DQS6	
SA_DQS7	
SA_DQS#0	
SA_DQS#1	
SA_DQS#2	
SA_DQS#3	
SA_DQS#4	
SA_DQS#5	
SA_DQS#6	
SA_DQS#7	
SA_MA0	
SA_MA1	
SA_MA2	
SA_MA3	
SA_MA4	
SA_MA5	
SA_MA6	
SA_MA7	
SA_MA8	
SA_MA9	
SA_MA10	
SA_MA11	
SA_MA12	
SA_MA13	
SA_MA14	
SA_RAS#	
SA_RCVEN#	
SA_WE#	

BB19	DDR A BS0
BK19	DDR A BS1
BF29	DDR A BS2
BL17	DDR A CAS#
AT45	DDR A DM0
BD44	DDR A DM1
BD42	DDR A DM2
AW38	DDR A DM3
AW13	DDR A DM4
BG8	DDR A DM5
AY8	DDR A DM6
AN6	DDR A DM7
AT46	DDR A DQS0
BE48	DDR A DQS1
BB43	DDR A DQS2
BC37	DDR A DQS3
BB16	DDR A DQS4
BH6	DDR A DQS5
B2	DDR A DQS6
AP3	DDR A DQS7
AT47	DDR A DQS#0
BD47	DDR A DQS#1
BC41	DDR A DQS#2
BA37	DDR A DQS#3
BA16	DDR A DQS#4
BH7	DDR A DQS#5
BC1	DDR A DQS#6
AP2	DDR A DQS#7
B119	DDR A MA0
BD20	DDR A MA1
BK27	DDR A MA2
BH28	DDR A MA3
BL24	DDR A MA4
BK28	DDR A MA5
BJ27	DDR A MA6
BJ25	DDR A MA7
BL28	DDR A MA8
BA28	DDR A MA9
BC19	DDR A MA10
BE28	DDR A MA11
BG30	DDR A MA12
BJ16	DDR A MA13
BJ29	DDR A MA14

BE18	DDR A RAS#	>>>DDR_A_RAS# 15
AY20	M A RCVEN#	TP6
BA19	DDR A WE#	>>>DDR_A_WE# 15



CRESTLINE-GP-U-WW.CREST.00U

DDR A BS[0.2] <<>> DDR_A_BS[0.2] 15

16 DDR_B_D[0.63] <<>> DDR_B D[0.63]

DDR A CAS# <<>> DDR_A_CAS# 15

DDR A DM[0.7] <<>> DDR_A_DM[0.7] 15

DDR A DQS[0.7] <<>> DDR_A_DQS[0.7] 15

DDR A DQS#[0.7] <<>> DDR_A_DQS#[0.7] 15

DDR A MA[0.14] <<>> DDR_A_MA[0.14] 15

DDR B D[0.63] <<>> DDR_B D[0.63]

DDR B D0	AP49
DDR B D1	AR51
DDR B D2	AW50
DDR B D3	AW51
DDR B D4	AN51
DDR B D5	AN50
DDR B D6	AV50
DDR B D7	AV49
DDR B D8	BA50
DDR B D9	BB50
DDR B D10	BA49
DDR B D11	BE50
DDR B D12	BA51
DDR B D13	AY49
DDR B D14	BE50
DDR B D15	BE49
DDR B D16	BJ50
DDR B D17	BJ44
DDR B D18	BJ43
DDR B D19	BL43
DDR B D20	BK47
DDR B D21	BK49
DDR B D22	BK43
DDR B D23	BK42
DDR B D24	BJ41
DDR B D25	BL41
DDR B D26	BJ37
DDR B D27	BJ36
DDR B D28	BK41
DDR B D29	BJ40
DDR B D30	BL35
DDR B D31	BK37
DDR B D32	BK13
DDR B D33	BE11
DDR B D34	BK11
DDR B D35	BC11
DDR B D36	BC13
DDR B D37	BE12
DDR B D38	BC12
DDR B D39	BG12
DDR B D40	BJ10
DDR B D41	BL9
DDR B D42	BK5
DDR B D43	BL5
DDR B D44	BK9
DDR B D45	BK10
DDR B D46	BJ8
DDR B D47	BJ6
DDR B D48	BF4
DDR B D49	BH5
DDR B D50	BG1
DDR B D51	BC2
DDR B D52	BK3
DDR B D53	BE4
DDR B D54	BD3
DDR B D55	BJ2
DDR B D56	BA3
DDR B D57	BB3
DDR B D58	AR1
DDR B D59	AT3
DDR B D60	AY2
DDR B D61	AY3
DDR B D62	AU2
DDR B D63	AT2

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DDR SYSTEM MEMORY B

SB_DQ0	SB_BS0
SB_DQ1	SB_BS1
SB_DQ2	SB_BS2
SB_DQ3	
SB_CAS#	
SB_DM0	
SB_DM1	
SB_DM2	
SB_DM3	
SB_DM4	
SB_DM5	
SB_DM6	
SB_DM7	
SB_DQS0	
SB_DQS1	
SB_DQS2	
SB_DQS3	
SB_DQS4	
SB_DQS5	
SB_DQS6	
SB_DQS7	
SB_DQS#0	
SB_DQS#1	
SB_DQS#2	
SB_DQS#3	
SB_DQS#4	
SB_DQS#5	
SB_DQS#6	
SB_DQS#7	
SB_MA0	
SB_MA1	
SB_MA2	
SB_MA3	
SB_MA4	
SB_MA5	
SB_MA6	
SB_MA7	
SB_MA8	
SB_MA9	
SB_MA10	
SB_MA11	
SB_MA12	
SB_MA13	
SB_MA14	
SB_RAS#	
SB_RCVEN#	
SB_WE#	

DDR B BS[0.2] <<>> DDR_B_BS[0.2] 16

16 DDR_B_D[0.63] <<>> DDR_B D[0.63]

DDR B CAS# <<>> DDR_B_CAS# 16

DDR B DM[0.7] <<>> DDR_B_DM[0.7] 16

DDR B DQS[0.7] <<>> DDR_B_DQS[0.7] 16

DDR B DQS#[0.7] <<>> DDR_B_DQS#[0.7] 16

DDR B MA[0.14] <<>> DDR_B_MA[0.14] 16

DDR B RAS# <<>> DDR_B_RAS# 16

TP5

DDR B WE# <<>> DDR_B_WE# 16

TP6

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D85



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Title

Beyonce UMA

Size

A3

Document Number

GMCH-DDR (3/6)

Rev

-3

Date:

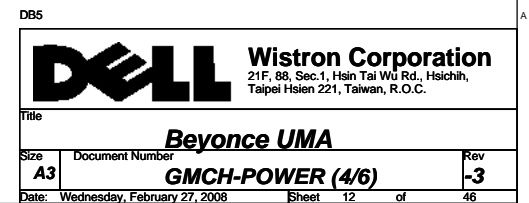
Wednesday, February 27, 2008

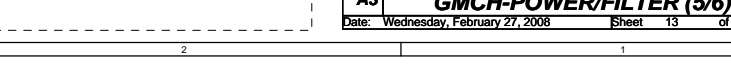
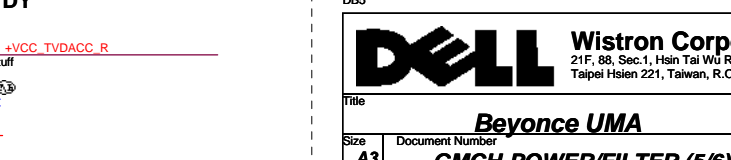
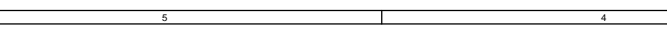
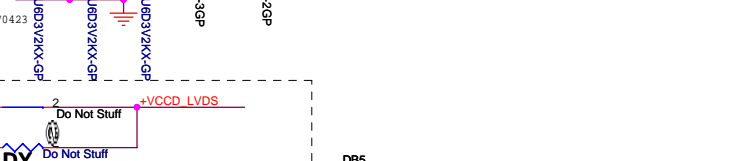
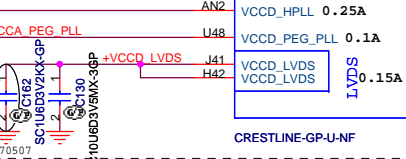
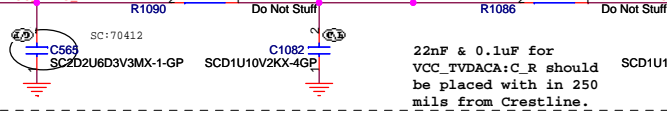
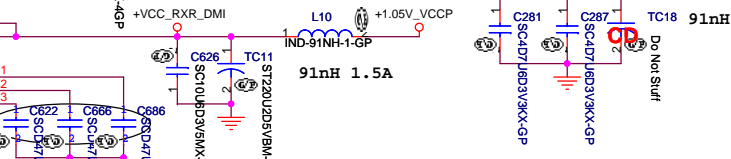
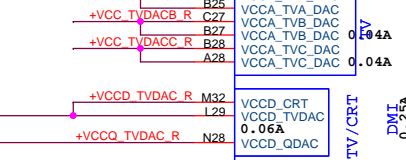
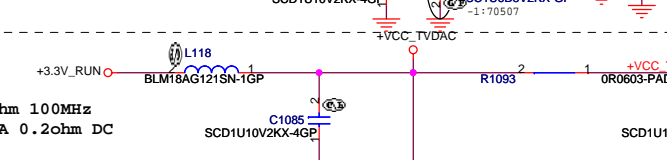
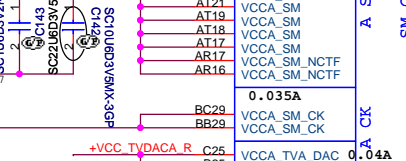
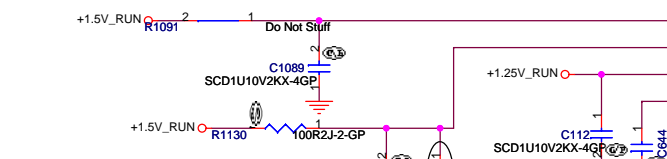
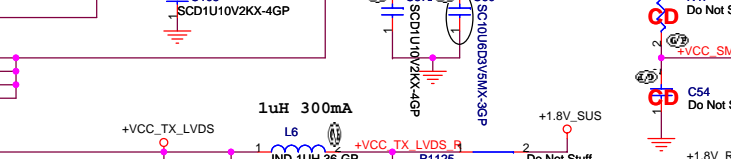
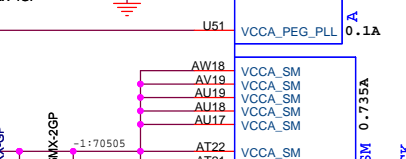
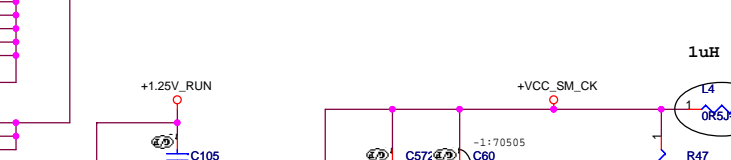
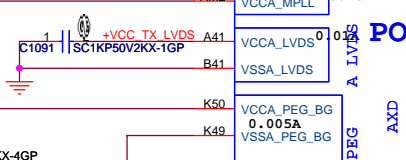
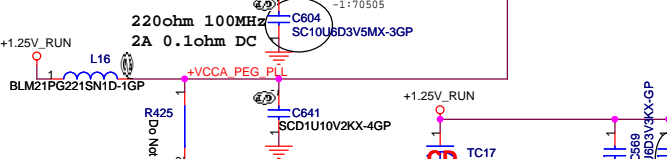
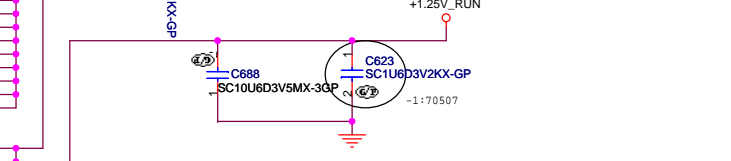
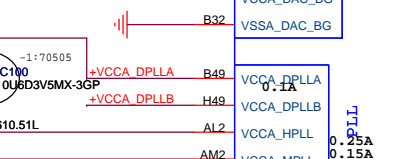
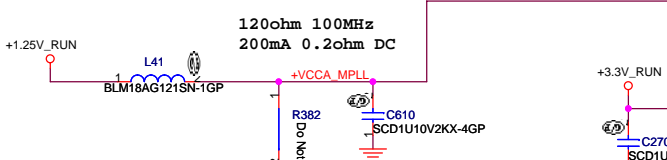
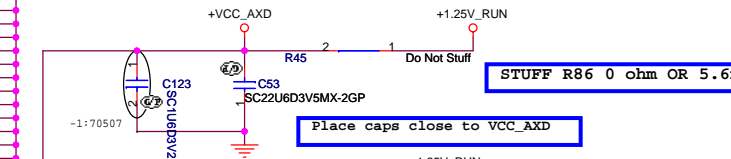
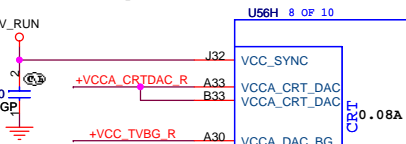
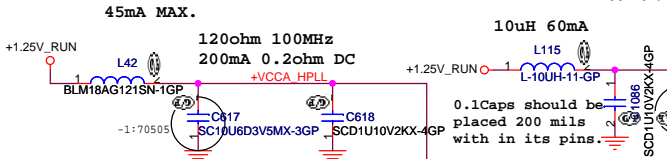
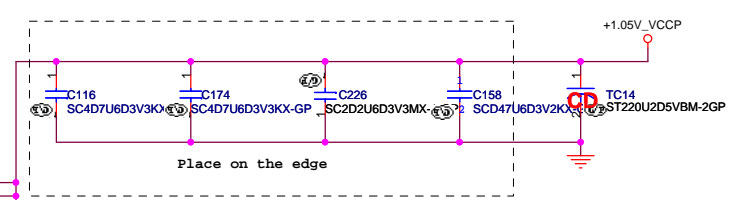
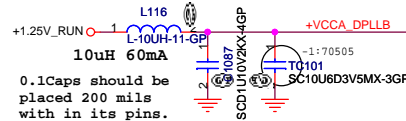
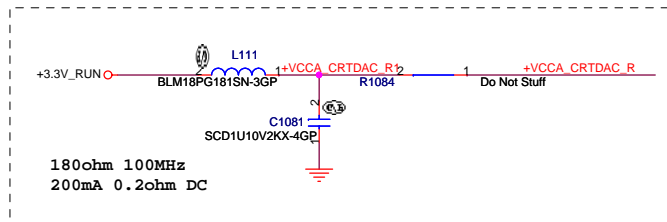
Sheet

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of

46





POWER

CRESTLINE-GP-U-NF

71.CREST.00U

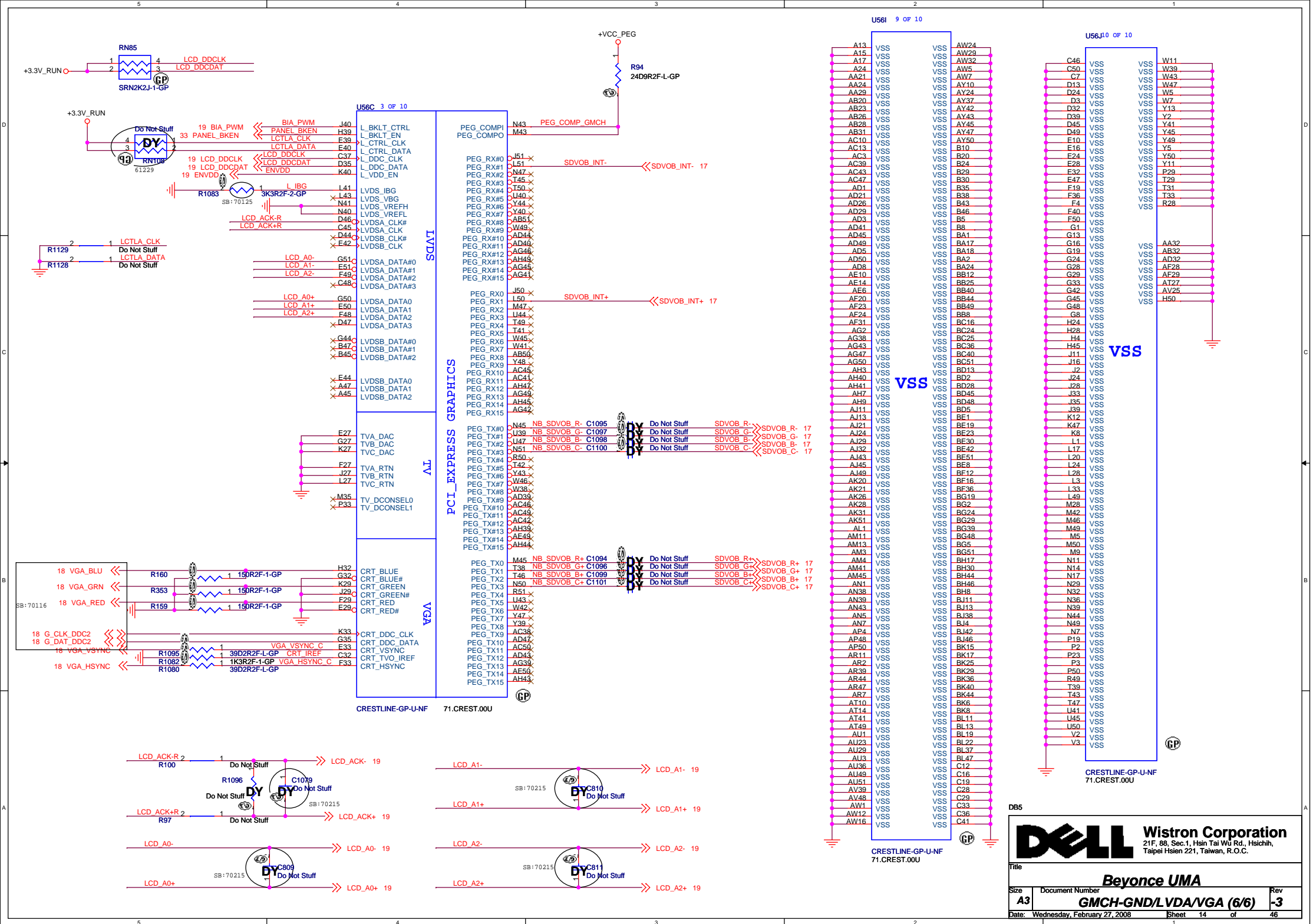
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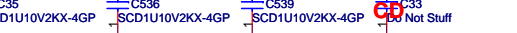
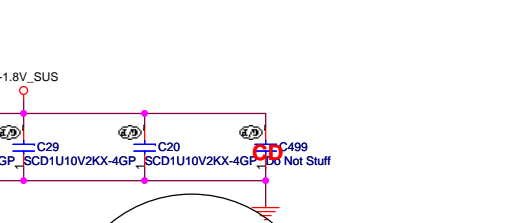
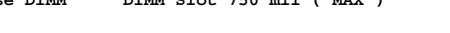
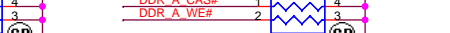
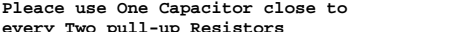
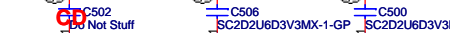
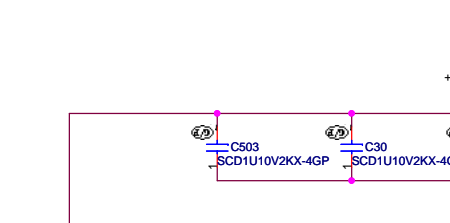
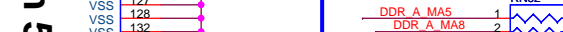
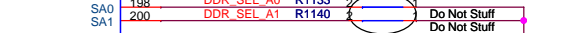
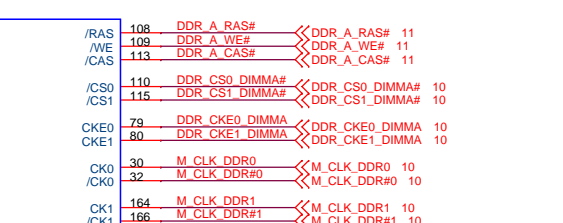
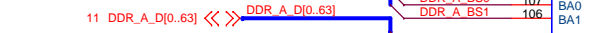
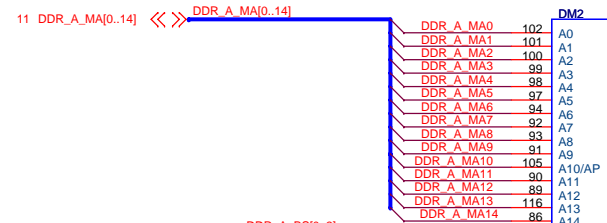
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Title

Beyonce UMA

Size	Document Number	Rev
A3	GMCH-POWER/FILTER (5/6)	-3
Date: Wednesday, February 27, 2008	Sheet 13 of 46	



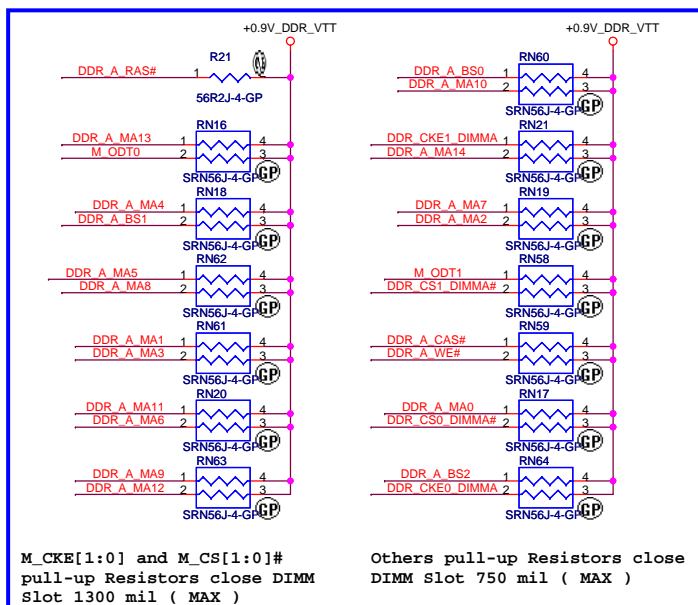


REVERSE TYPE
High 5.2 mm

Please close to the DIMM Slot

071004 modify del TC6

Please use One Capacitor close to every Two pull-up Resistors

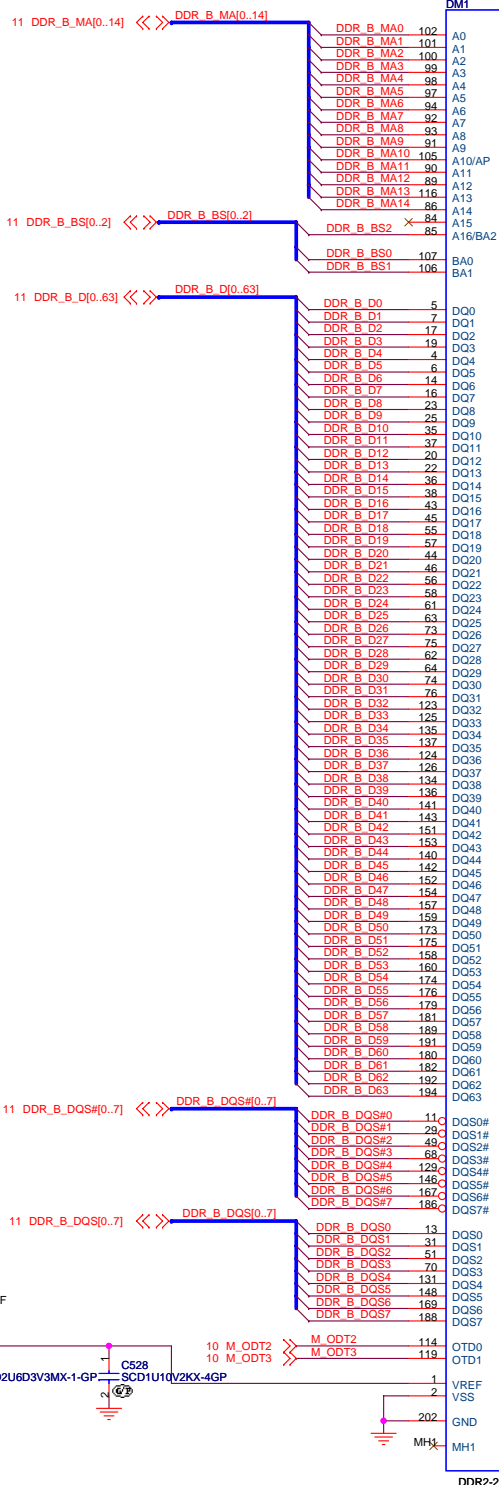


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Taipei Hsien 221, Taiwan, R.O.C.

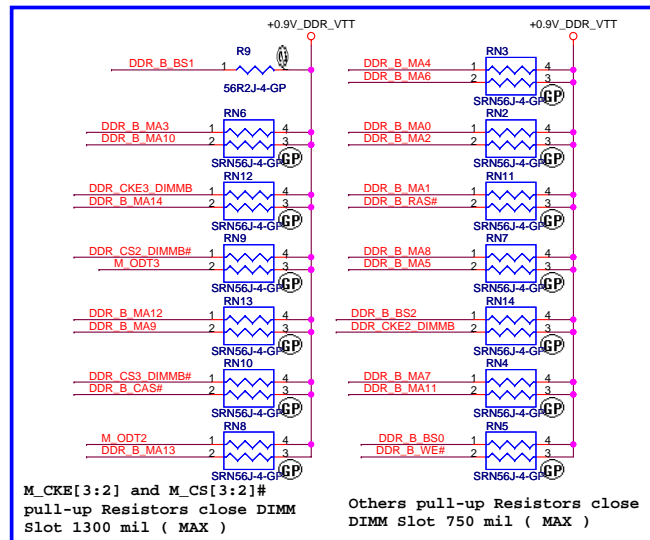
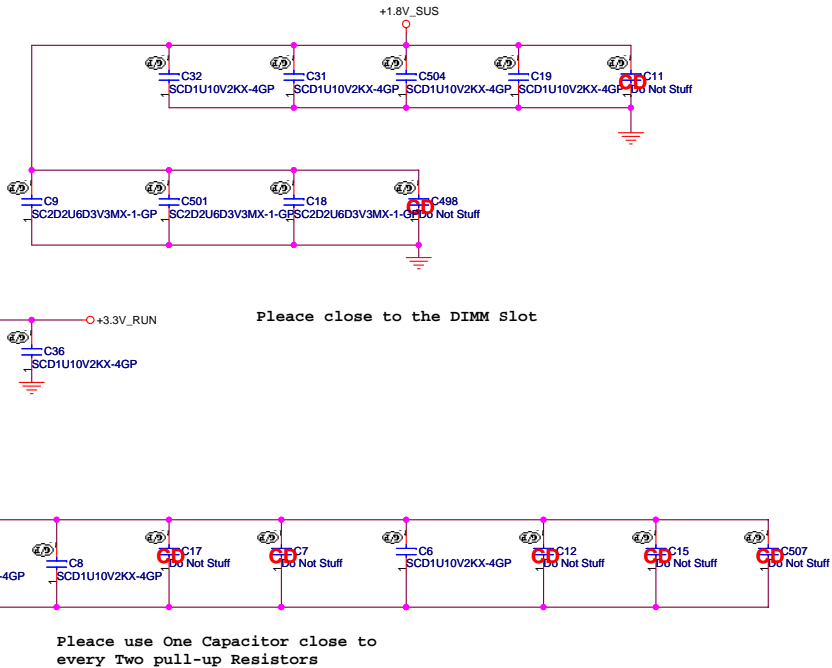
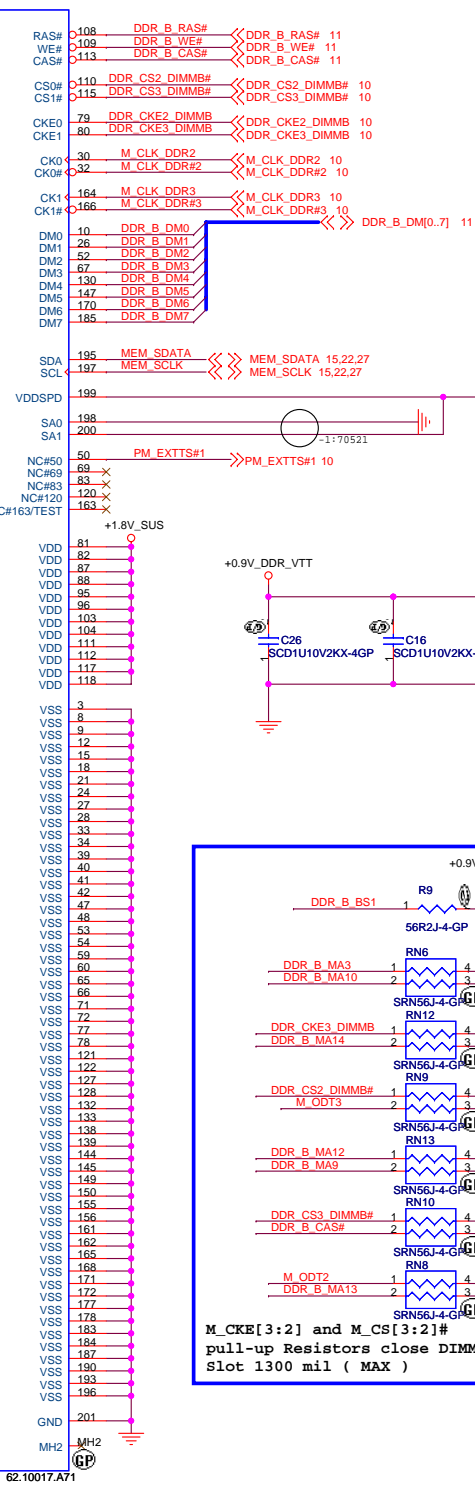
Beyonce UMA

Size A3 Document Number DDR2-SODIMM1 Rev -3

Date: Wednesday, February 27, 2008 Sheet 15 of 46



REVERSE TYPE High 9.2 mm



DB5

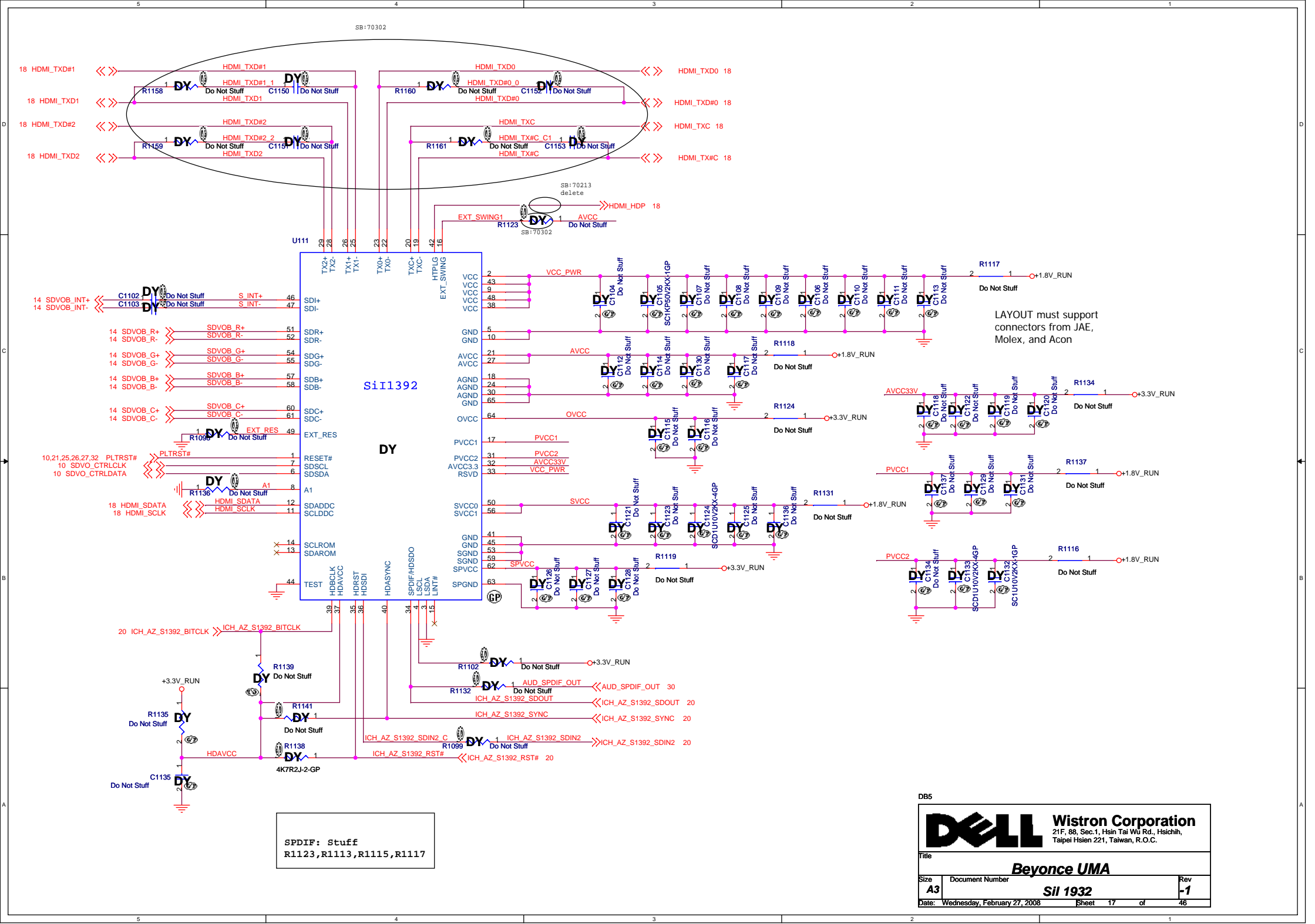


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Title: **Beyonce UMA**

Size: Custom Document Number: **DDR2-SODIMM2** Rev: **-3**

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Setting R,G,B trace impedance to 50 ohm.

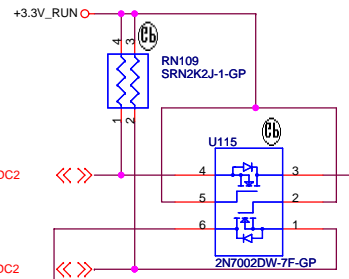
14 VGA_RED
14 VGA_GRN
14 VGA_BLU

14 VGA_HSYNC

14 VGA_VSYNC

14 G_DAT_DDC2

14 G_CLK_DDC2



+5V_RUN

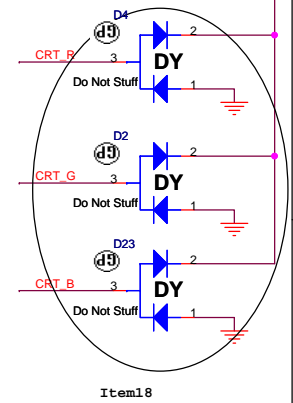
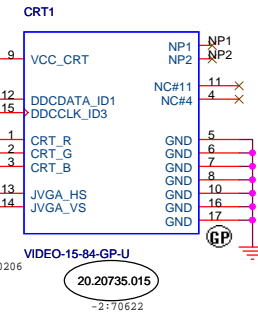
-1:70517

+CRT_VCC

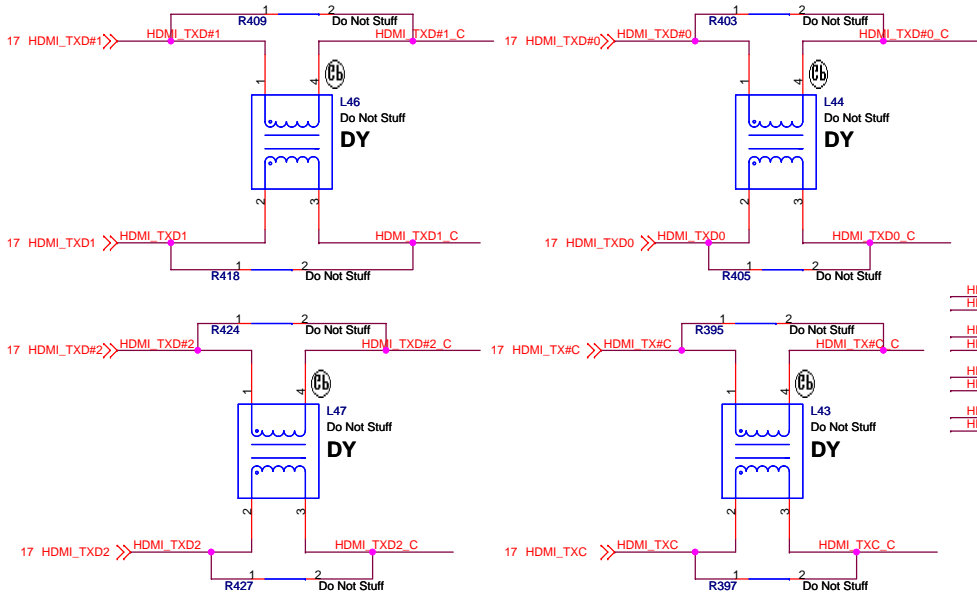
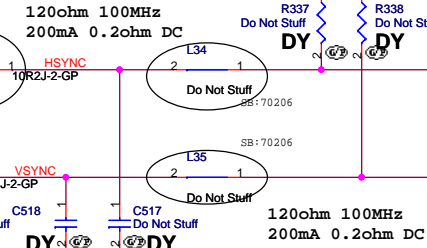
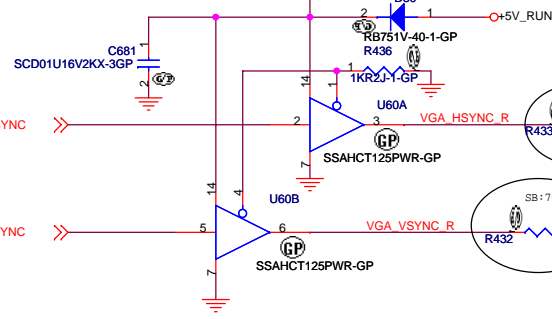
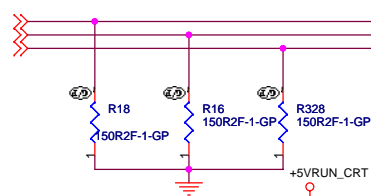
DAT_DDC2

CLK_DDC2

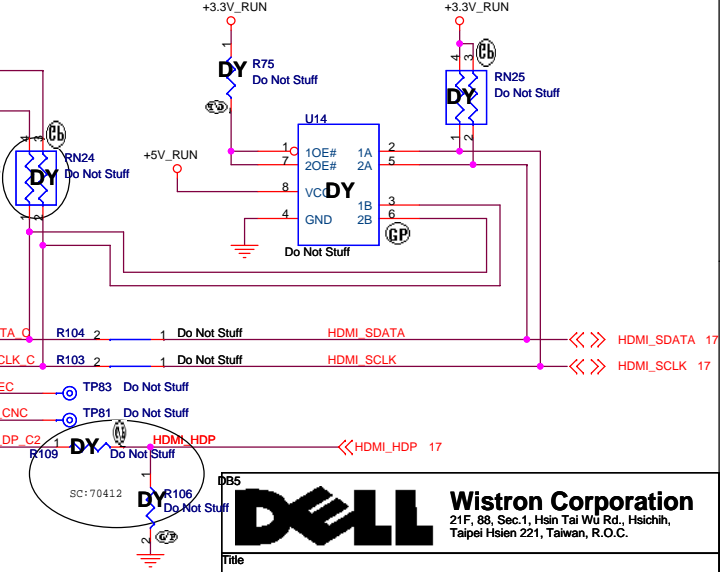
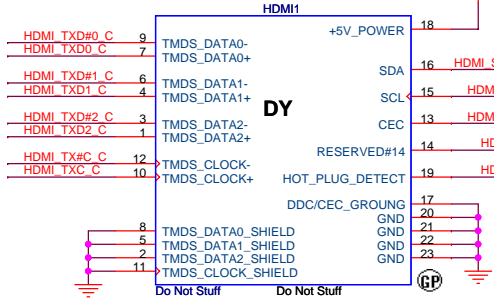
CRT conn.

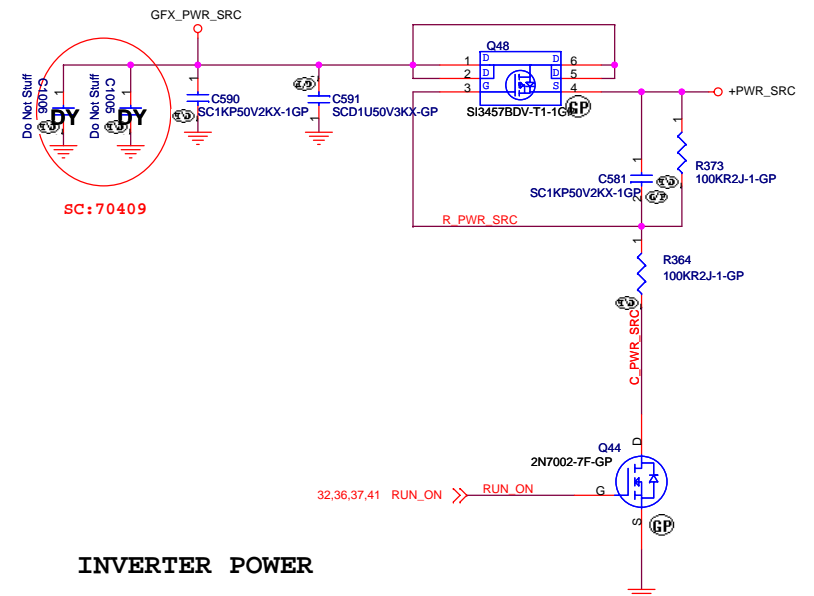
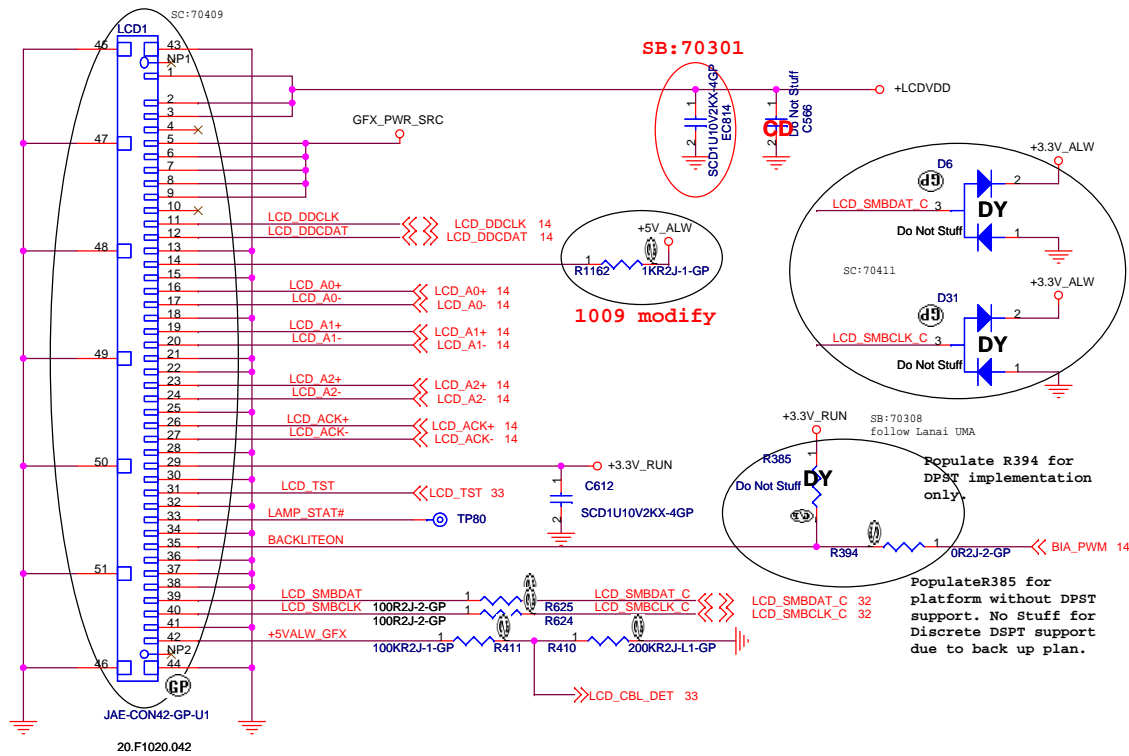


Item18



HDMI CONN

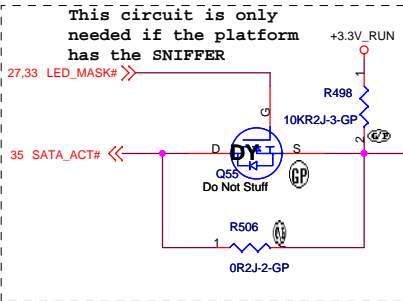




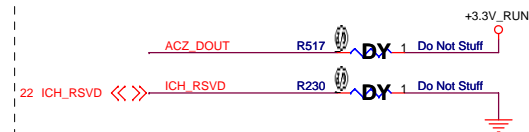
We would like to change X5 to 82.10026.021 and X3 to 82.30001.691.

ICH8-Strap PIN

integrated VccSus1_05,VccSus1_5,VccCL1_5		
ICH_INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
ICH_LAN100_SLP	High=Enable	Low=Disable



ICH8-Strap PIN

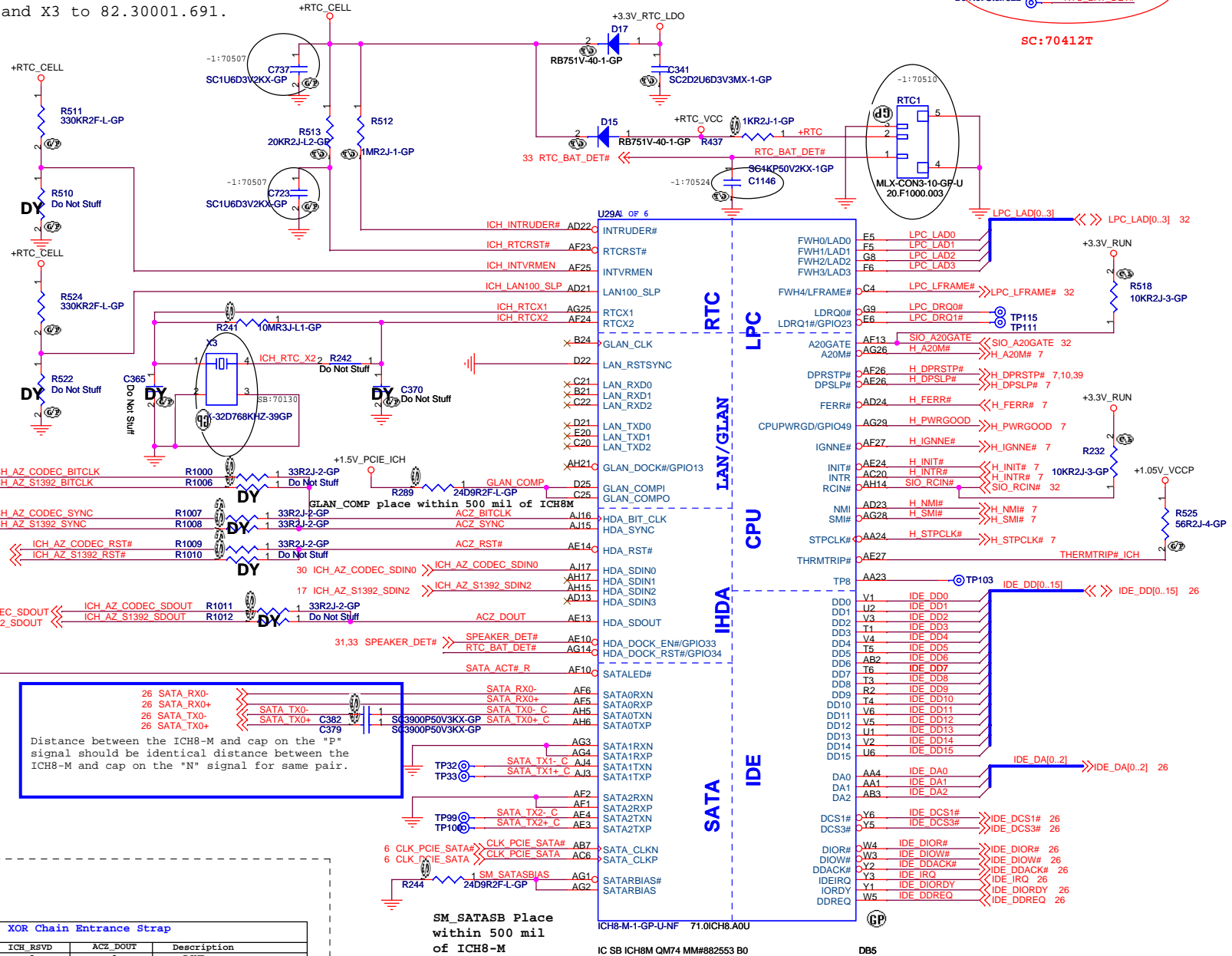


XOR Chain Entrance Strap		
ICH_RSVD	ACZ_DOUT	Description
0	0	RSVD
1	0	Enter XOR Chain
1	1	Normal Operation(default)
1	1	Set PCIE port cofig bit1

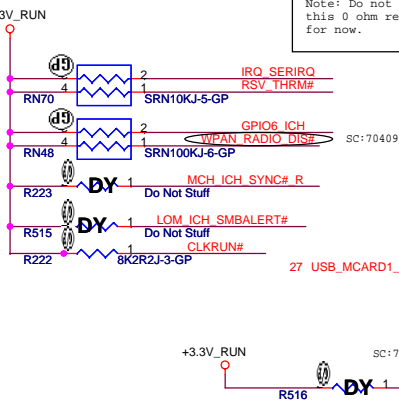
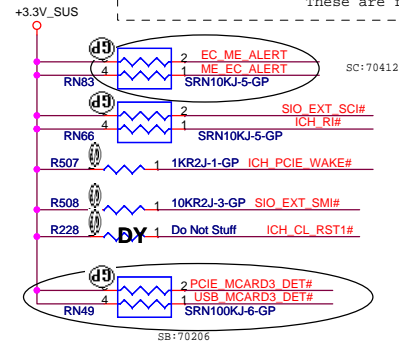
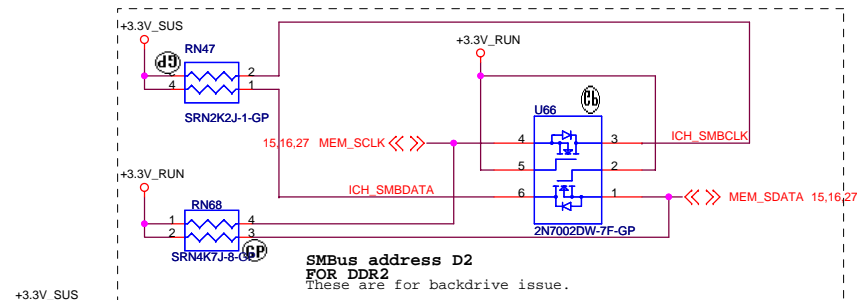
RTC circuitry

Do Not Stuff 521 +RTC
Do Not Stuff 522 RTC_BAT_DET#

SC:70412T



PCI_GNT#0 (R166)	SPI_CS#1 (R167)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC
A16 swap override strap		
PCI_GNT#3 (R168)	low = A16 swap override enable high = default	

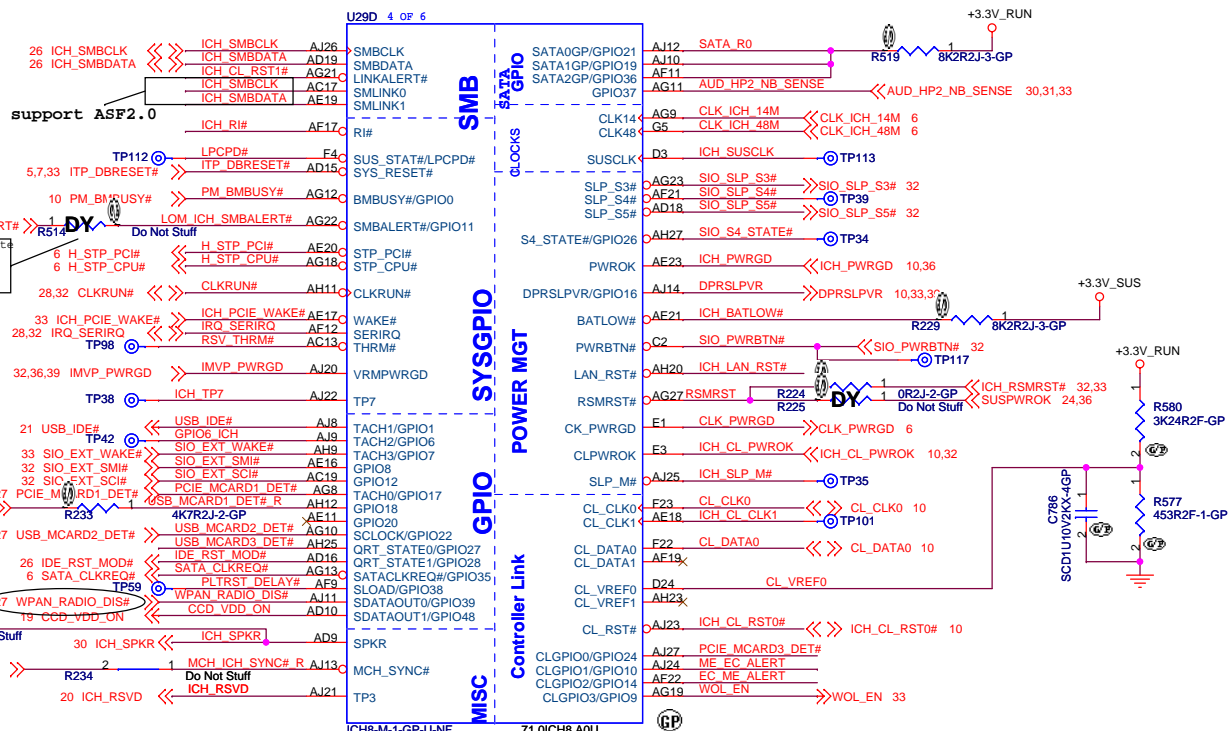
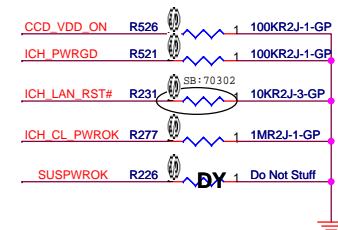
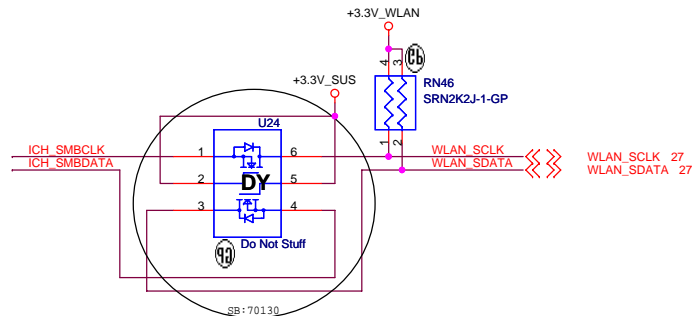
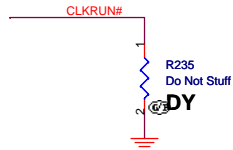


ICH8-Strap PIN

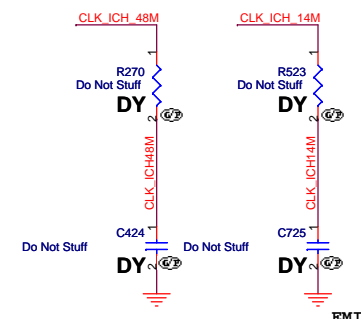
No Reboot Strap

ICH_SPKR LOW = Default

High=No Reboot



CLK_ICH_48M and CLK_ICH_14M EMI Mode Place close to ICH8-M



D85

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Title

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Size

Document Number

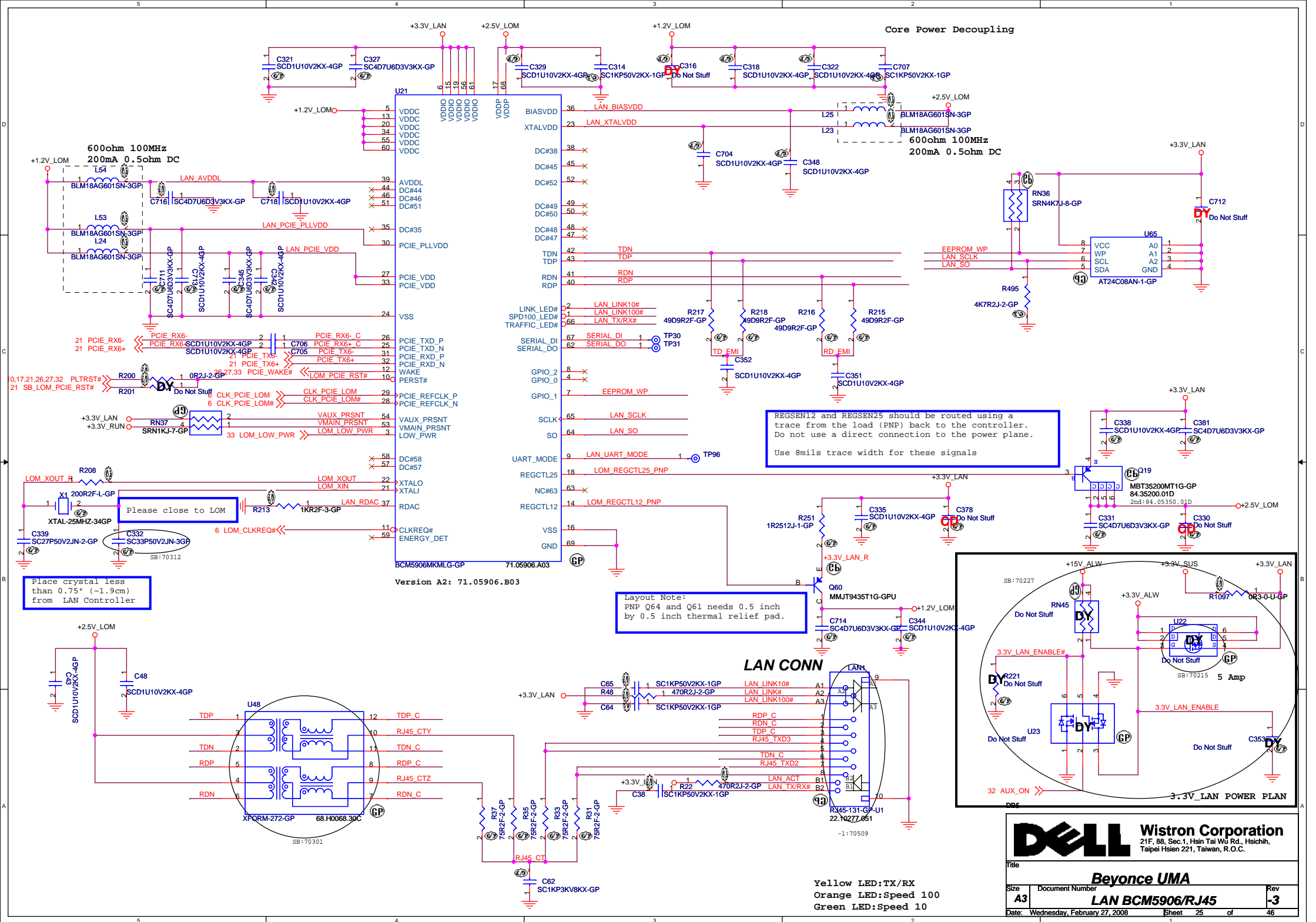
ICH8M-CL/PM/GPIO (3/4)

Rev

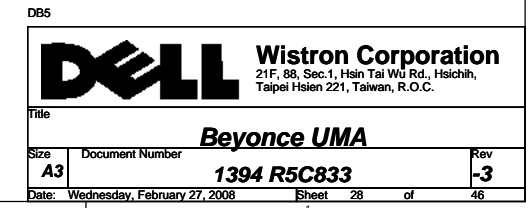
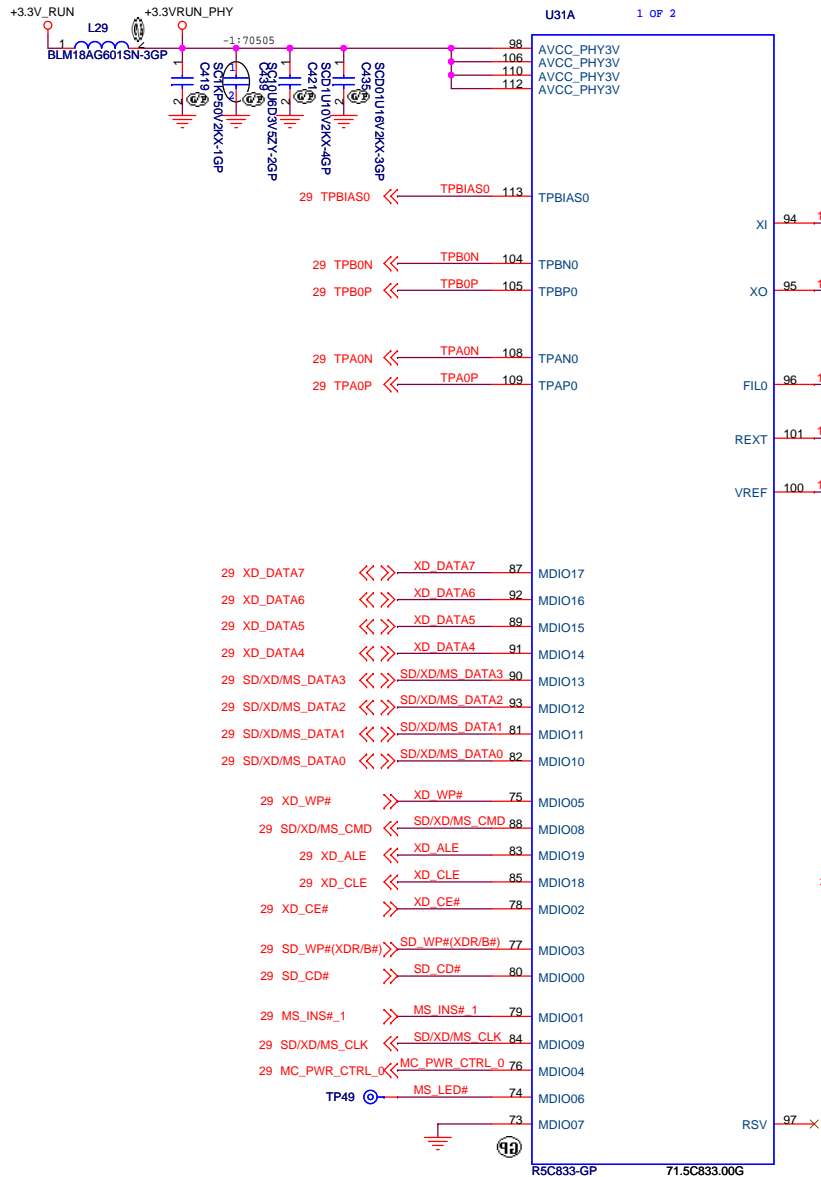
-3

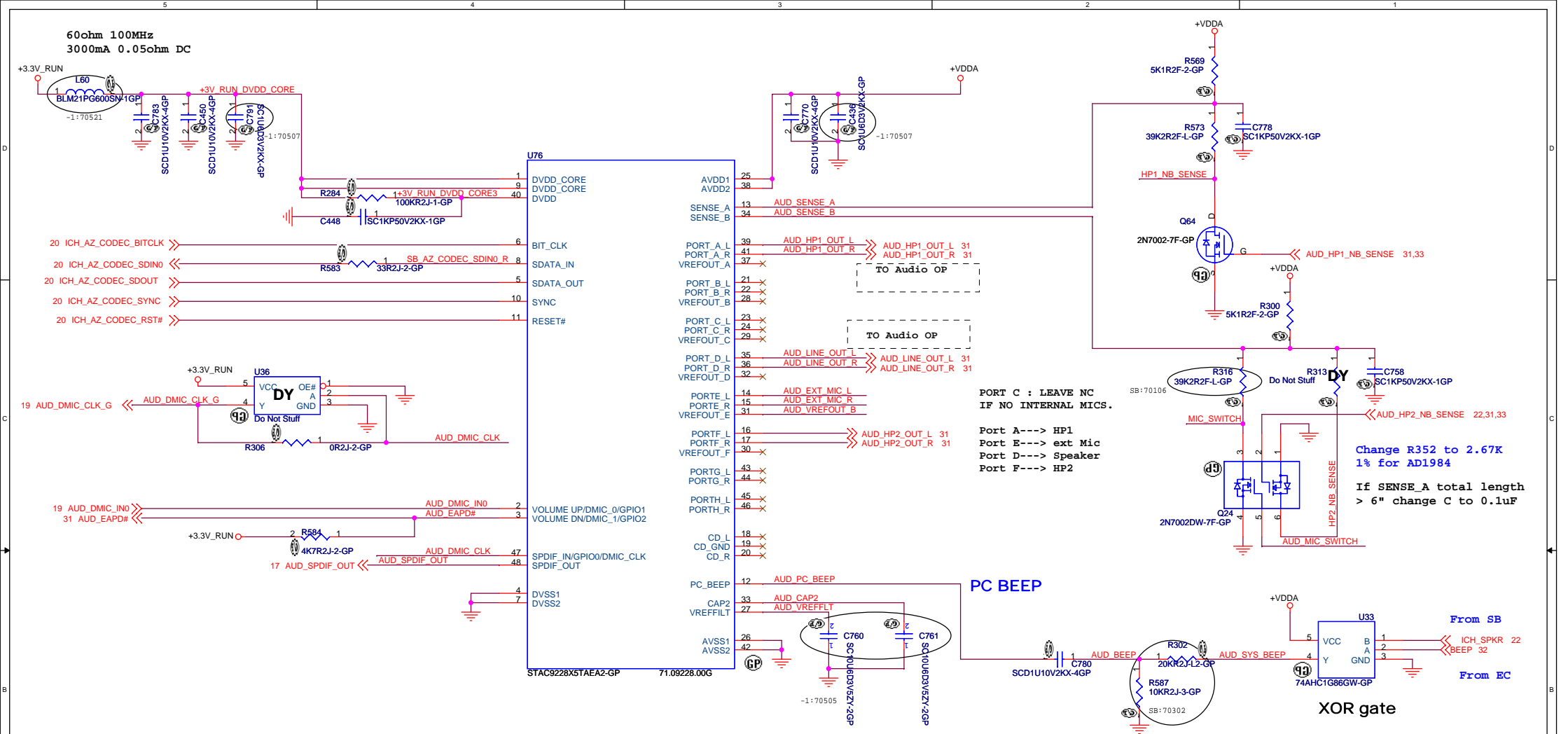
Date: Wednesday, February 27, 2008

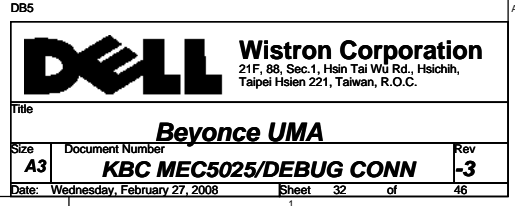
Sheet 22 of 46

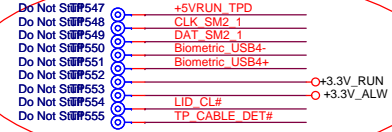
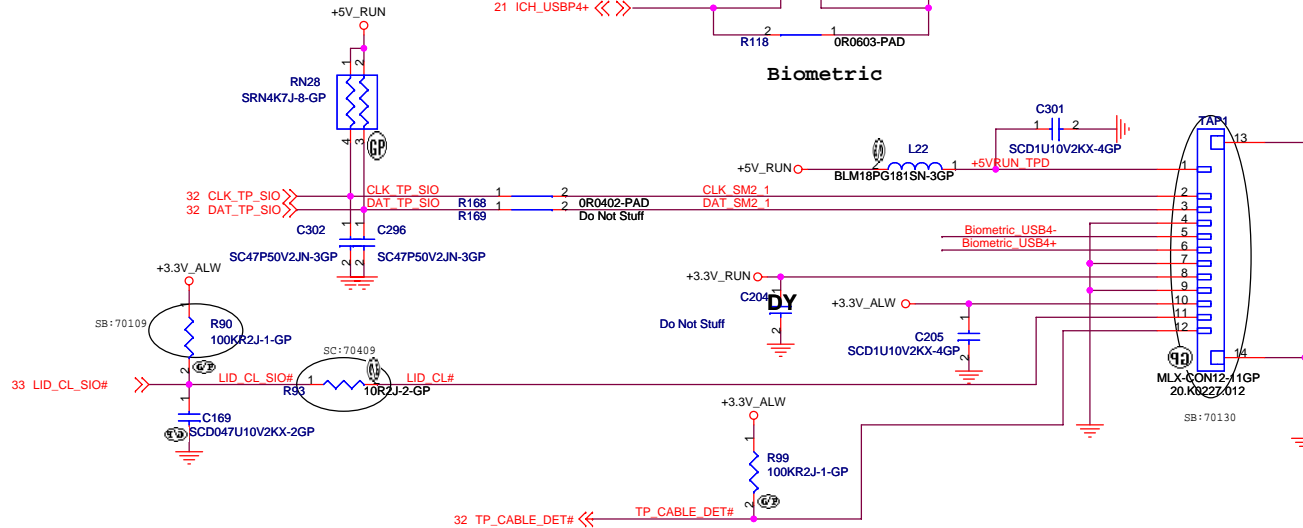
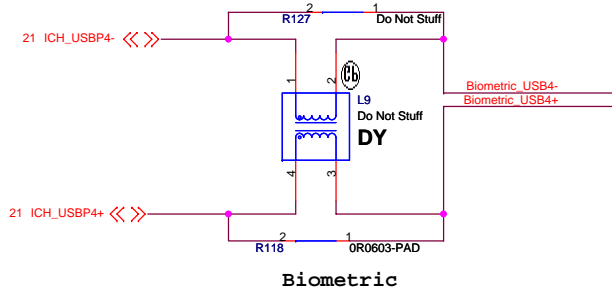
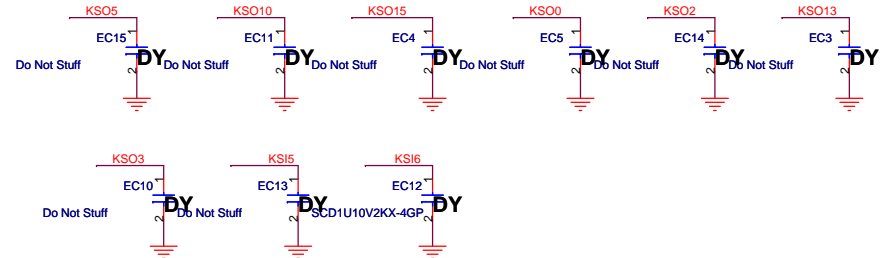
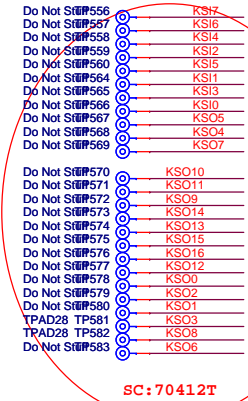
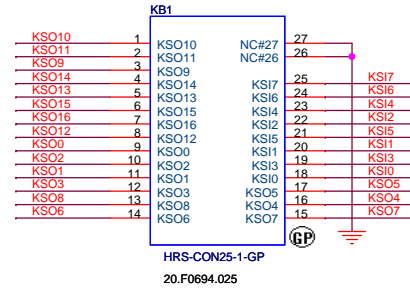
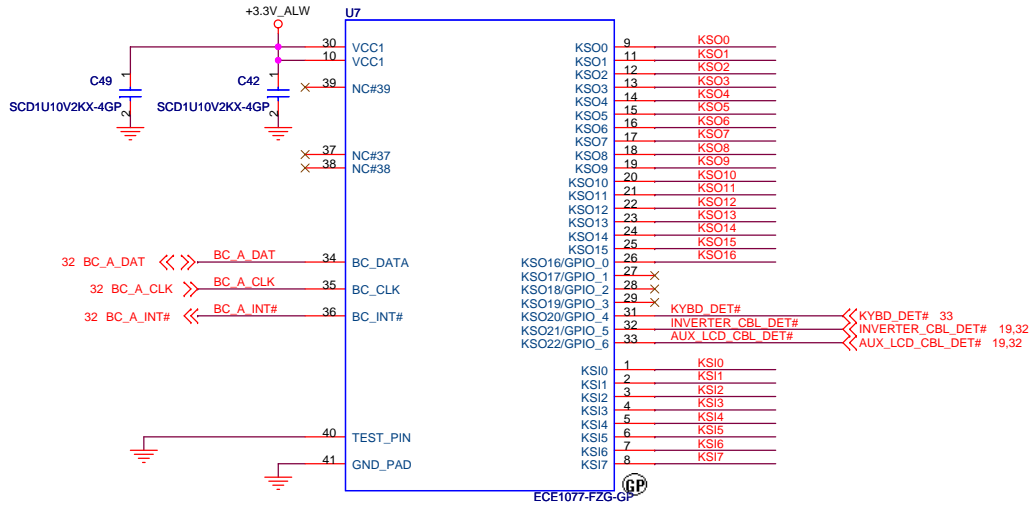


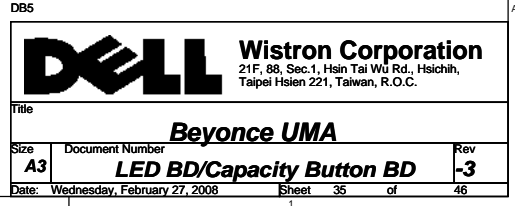
SSID = 1394

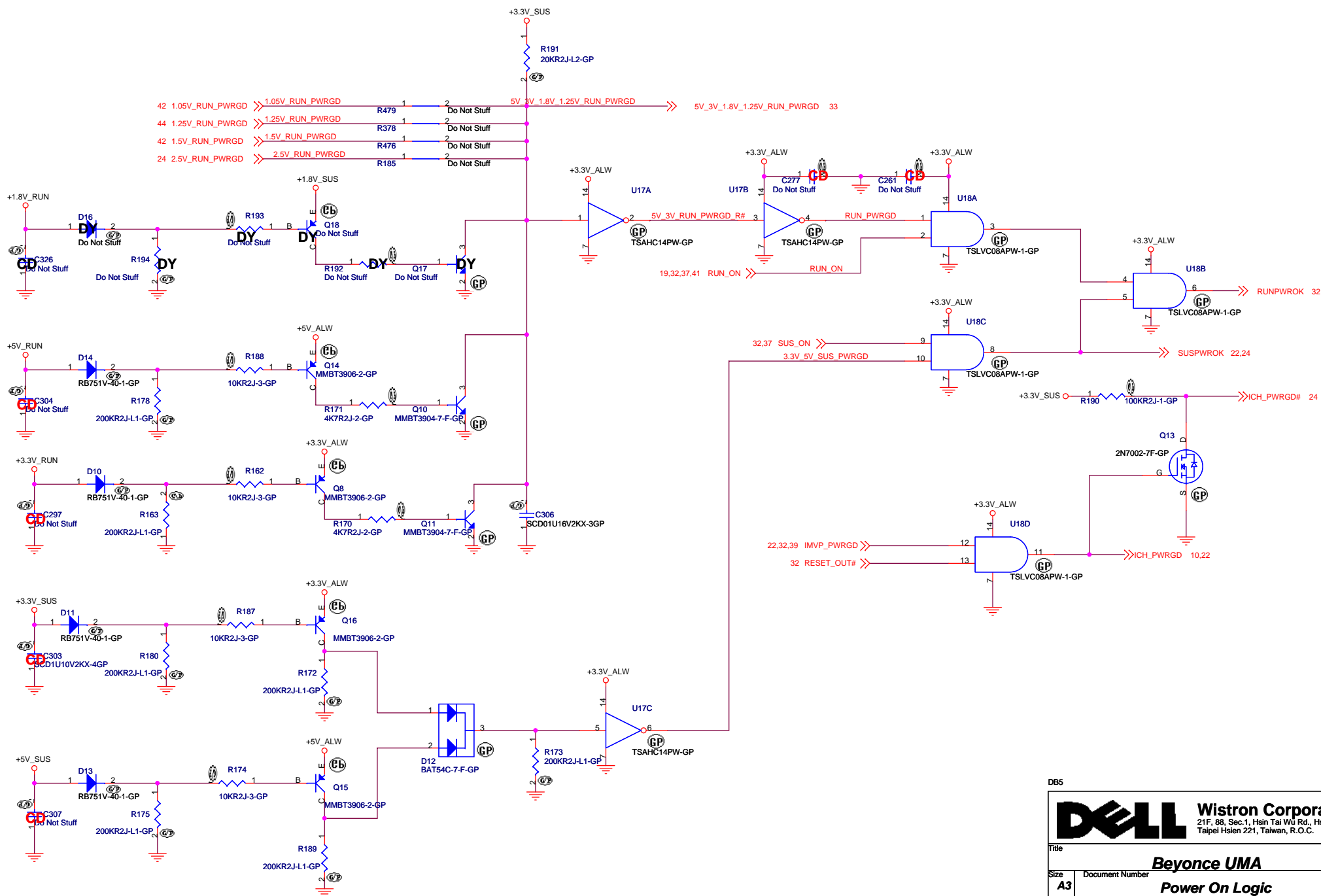












DB5



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Title

Beyonce UMA

Size

Document Number

Rev

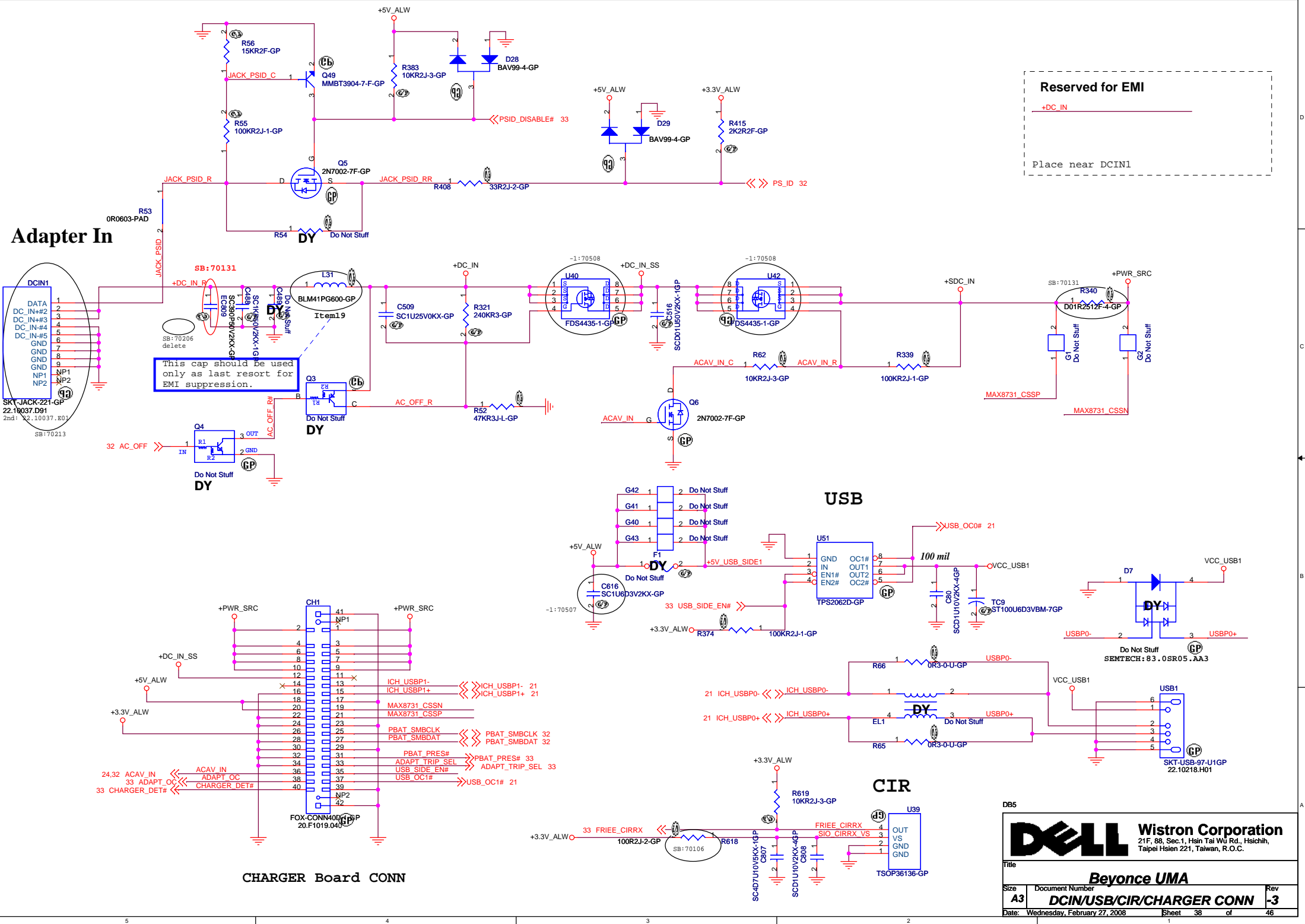
A3

Power On Logic

-3

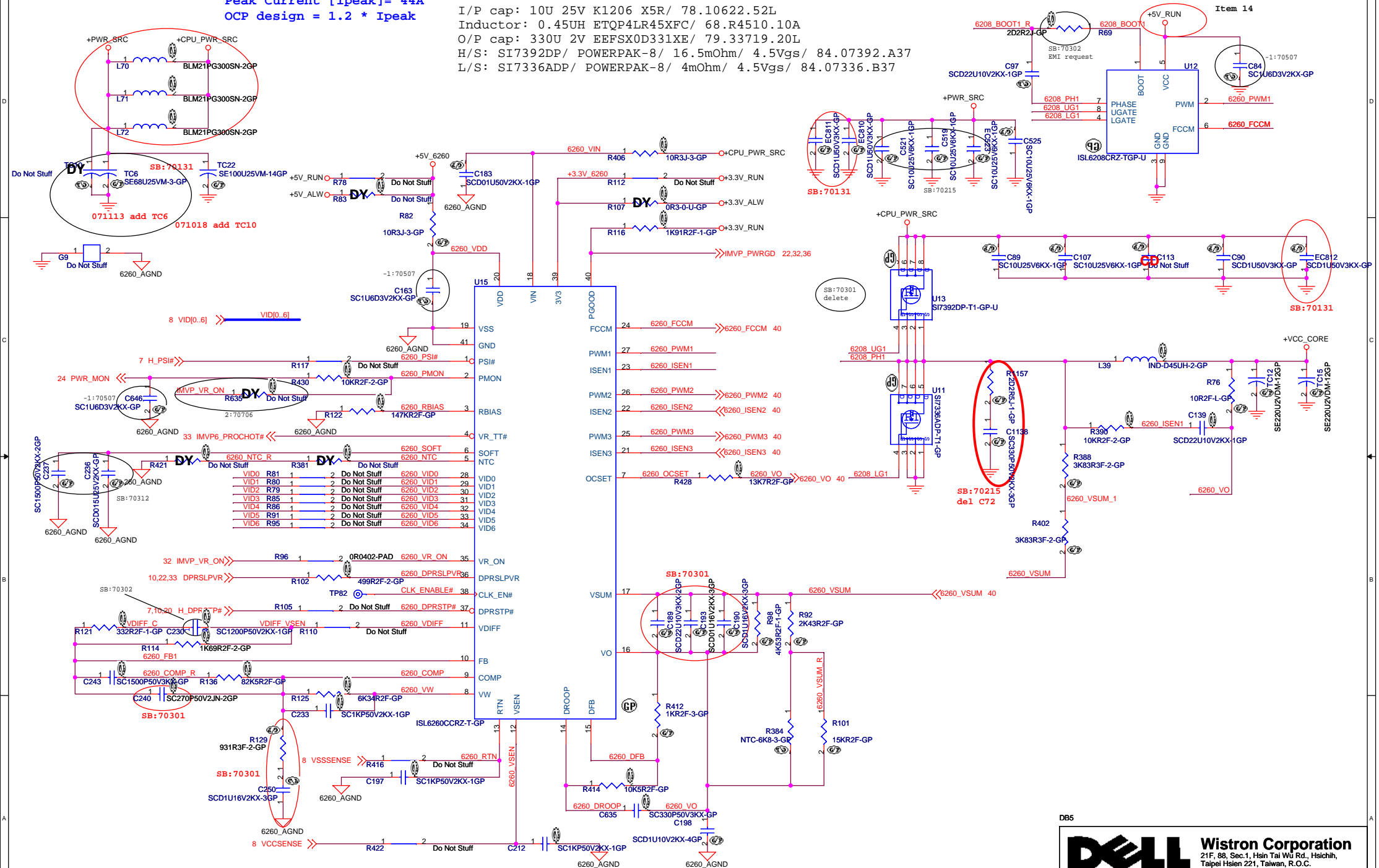
Date: Wednesday, February 27, 2008

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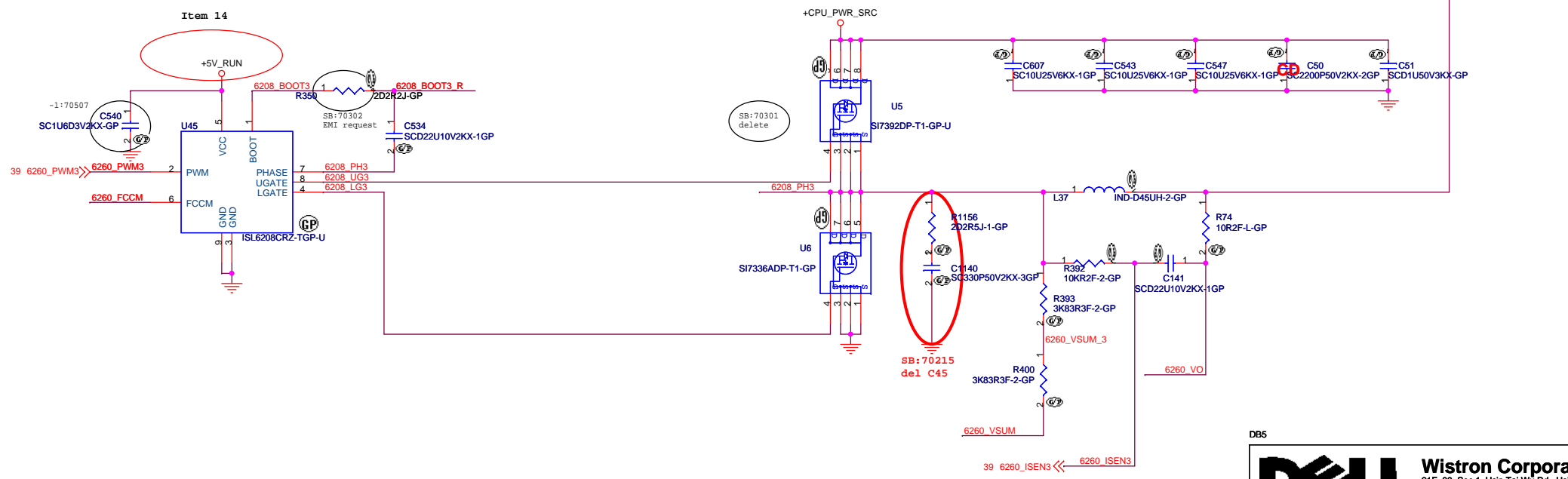
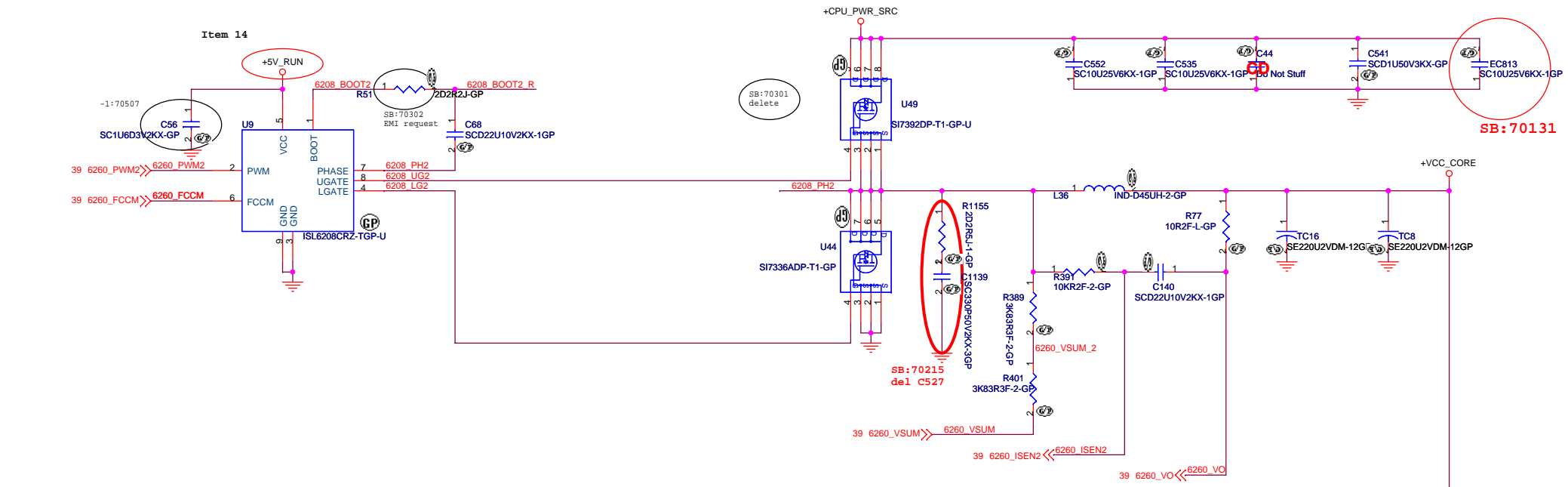
Thermal Design = 35.2A
Peak Current [Ipeak] = 44A
OCP design = 1.2 * Ipeak

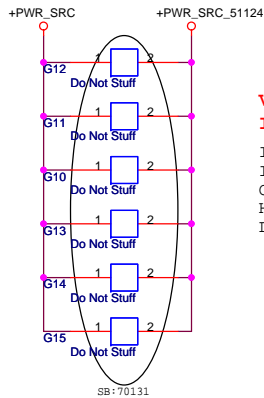
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.45UH ETQP4LR45XFC/ 68.R4510.10A
O/P cap: 330U 2V EEF5X0D331XE/ 79.33719.20L
H/S: SI7392DP/ POWERPAK-8/ 16.5mOhm/ 4.5Vgs/ 84.07392.A37
L/S: SI7336ADP/ POWERPAK-8/ 4mOhm/ 4.5Vgs/ 84.07336.B37



D85

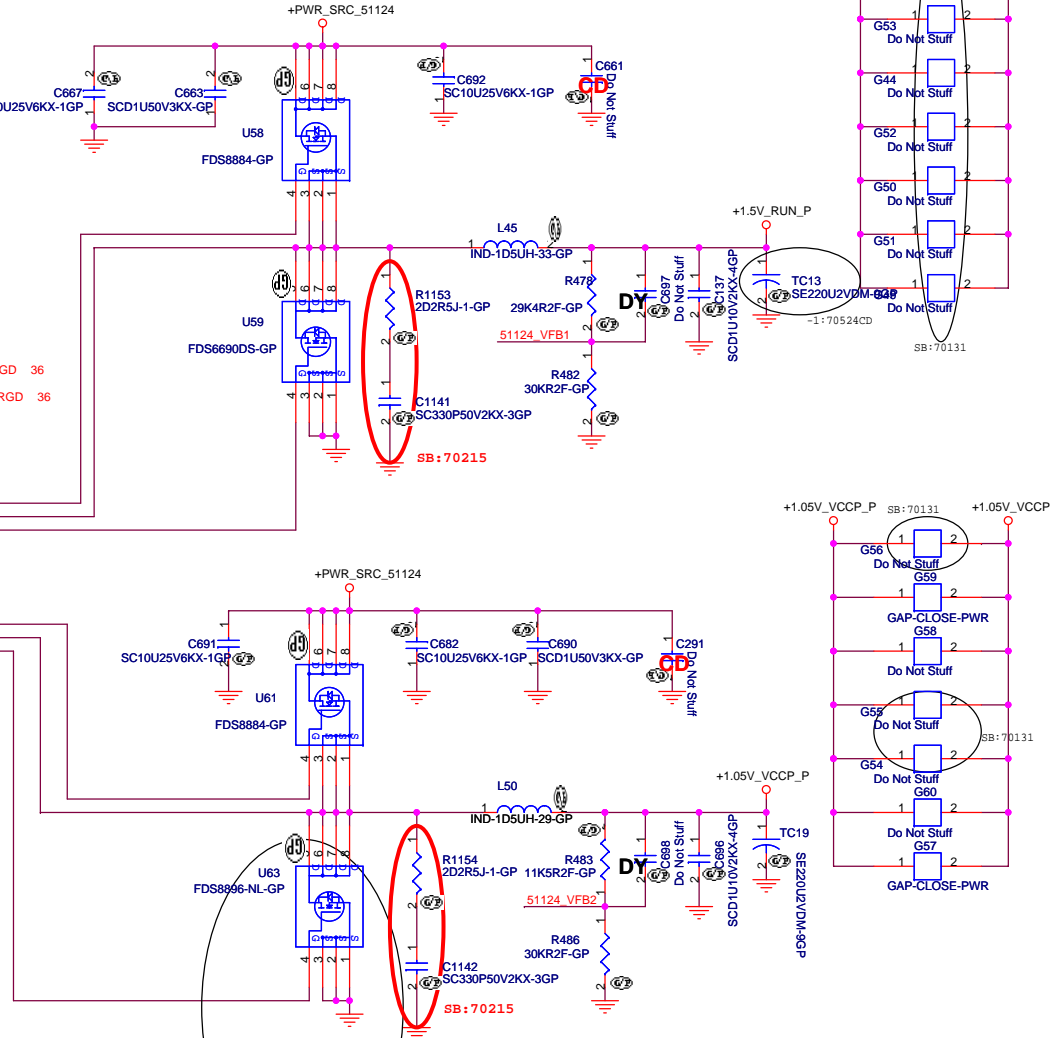
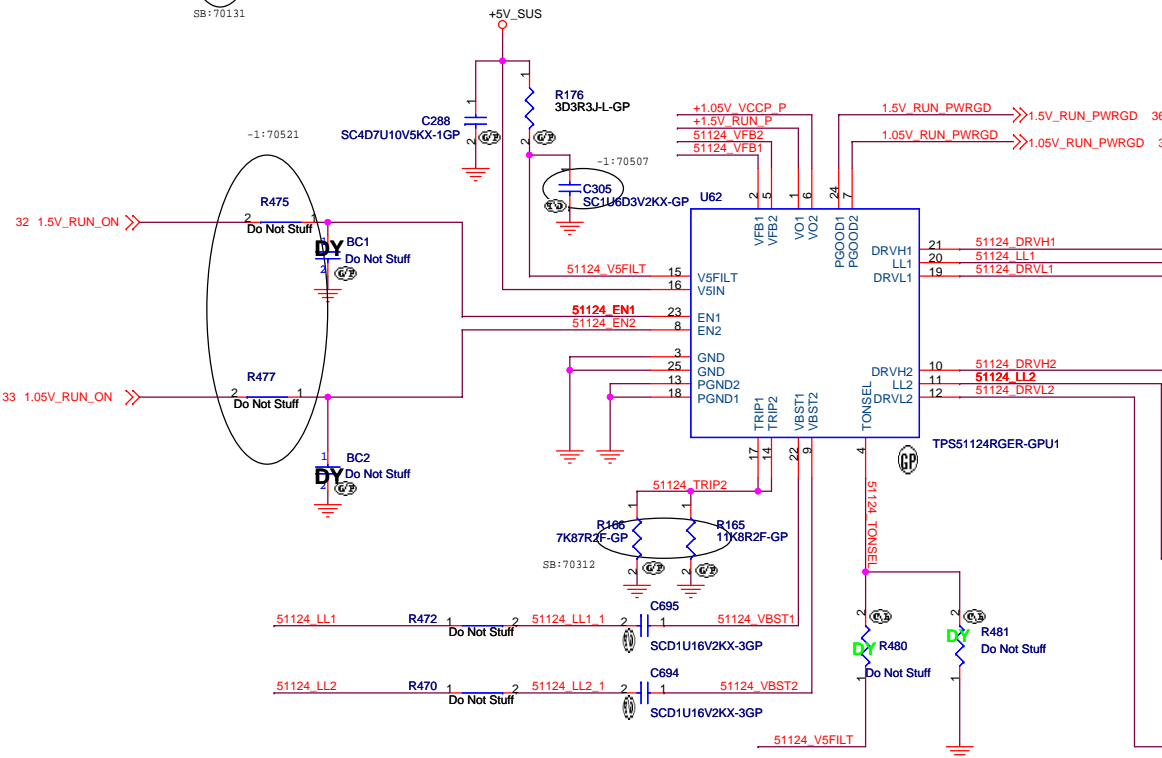
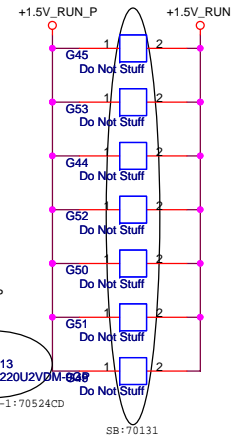






$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out})/V_{in}))$
 I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
 O/P cap: 220U 2V EEFSX0D221ER 9mOhm 3Arms Panasonic/ 79.22719.2PL
 H/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
 L/S: FDS6690AS SO-8/ 15mOhm/ 4.5Vgs/ 84.06690.E37

Design Current = 6.0A
 OCP design > 6.8A
 Included 1.25V LDO(3.02A)



Design Current= 12.2A
 OCP design > 15A

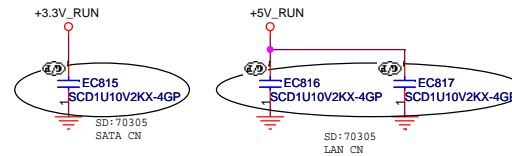
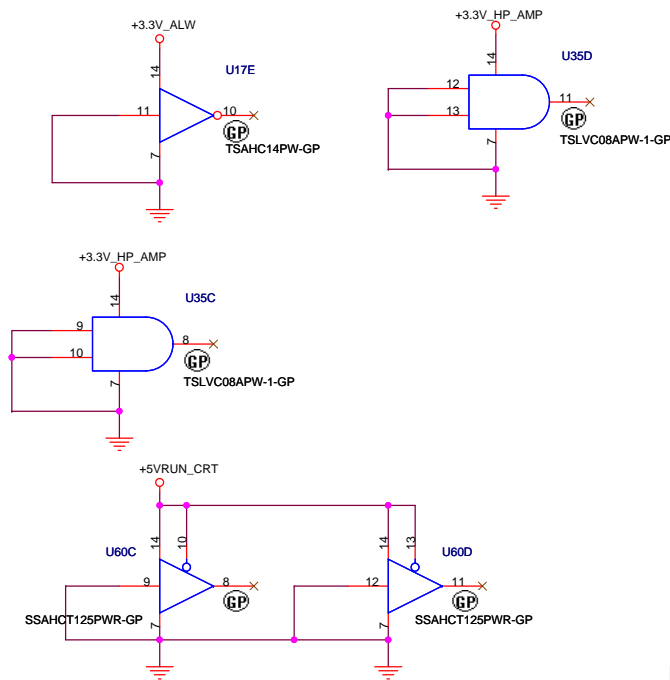
	GND	OPEN	V5FILT
TONSEL	240k/CH1	300k/CH1	360k/CH1
	300k/CH2	360k/CH2	420k/CH2

$V_{out} = 0.758V * (R1+R2)/R2$ --> PWM mode
 $V_{out} = 0.764V * (R1+R2)/R2$ --> Skip Mode

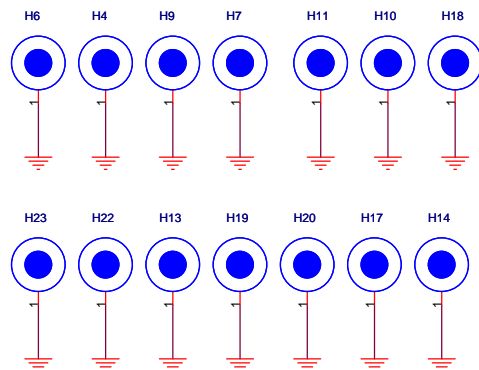
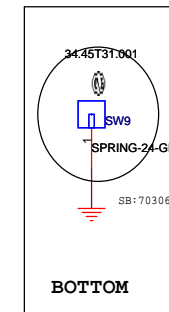
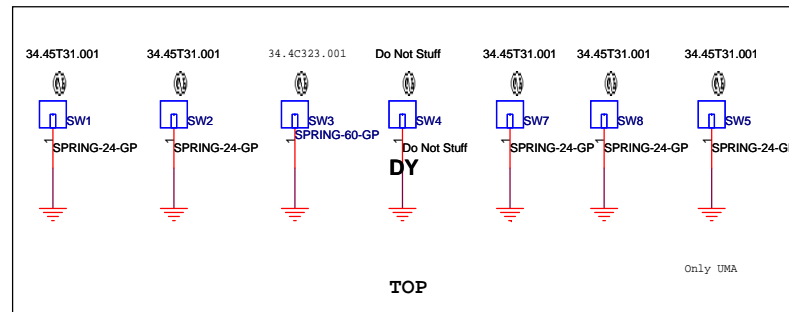
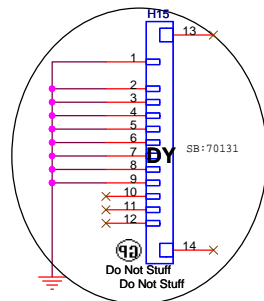
DB5



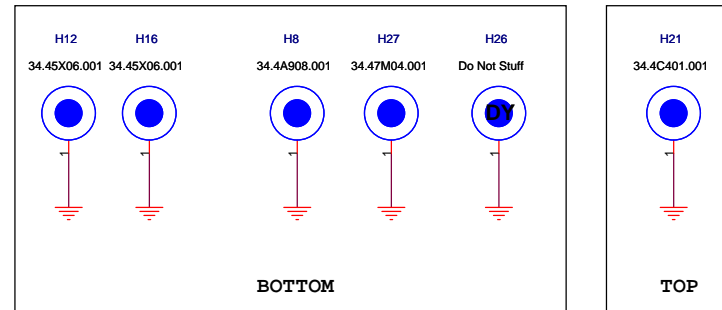




SW3 - 34.43E25.001
 SW9 - 34.49Q02.001
 SW5 - 34.34T31.001 (Only for UMA)
 others-34.45T31.001



H12, H16: 34.45X06.001
 H8: 34.4A908.001
 H27: 34.47M04.001
 H26: 34.4G901.001
 H21: 34.4C401.001



DB5

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 Size: **A3** Document Number: **EMI&MISC** Rev: **-3**
 Date: Wednesday, February 27, 2008 Sheet 45 of 46

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