

Compal Confidential

IFTxx Schematics Document

Intel Merom Processor with Crestline + DDRII + ICH8M
(With nVIDIA MXM/B)

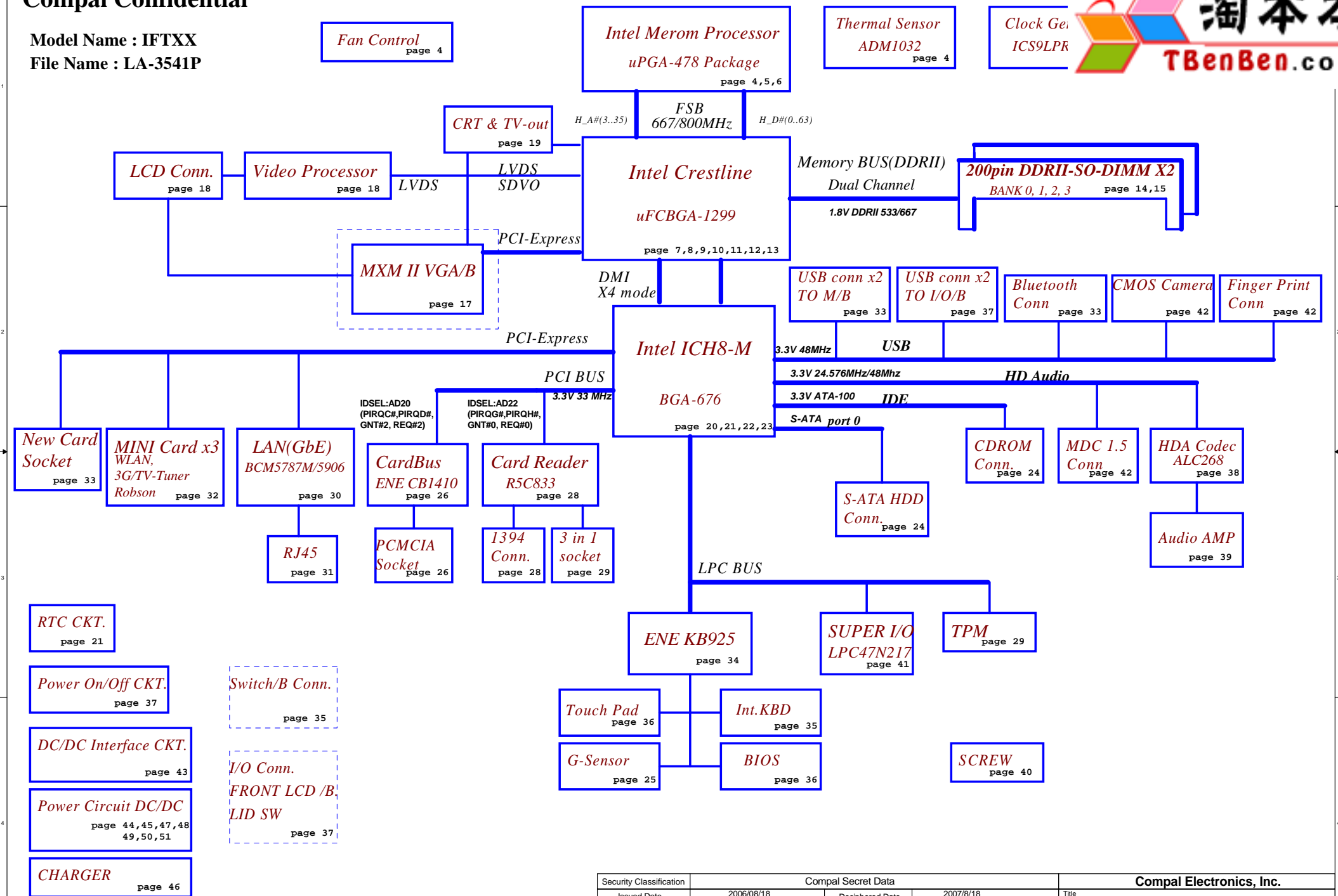
2006-11-01

REV: 0.1

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Model Name : IFTXX
File Name : LA-3541P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
CARD BUS CB1410	AD20	2	C,D
1394+Cardreader	AD22	0	G,H

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

EC SM Bus2 address

Device	Address
ADI ADM1032	1001 100X b
NVIDIA NB8X	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

ID1	ID0	TEST
0(R744)	0(R745)	A-TEST
0(R744)	1(R742)	B-TEST
1(R741)	0(R745)	C-TEST

PANEL ID Table

R	Size
Ra (R743)	15W
Rb (R740)	14W

ICH8M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

Close to CPU pin AD26
within 500mils.

Width=20 mil

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

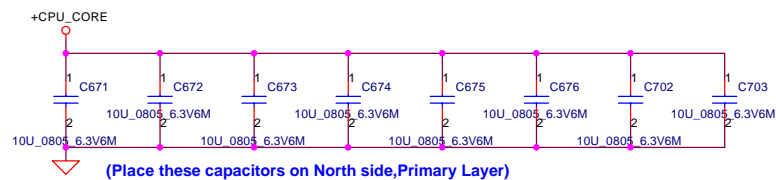
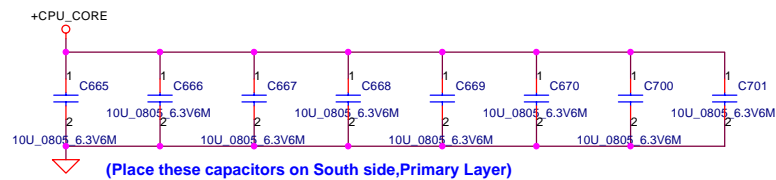
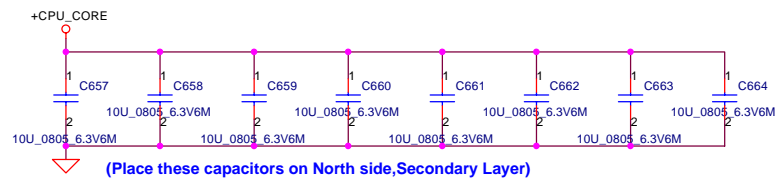
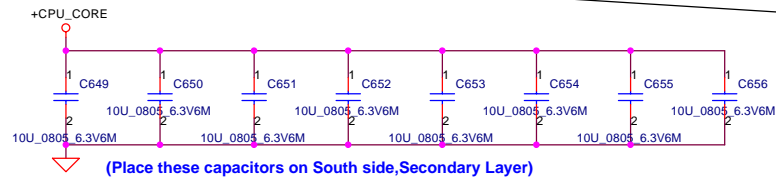
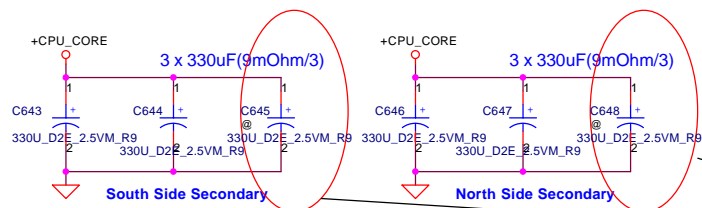
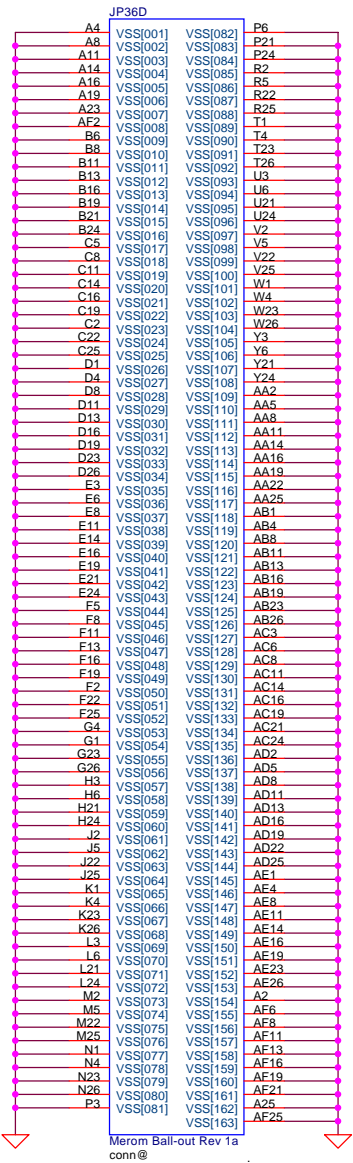
Resistor placed within
0.5" of CPU pin. Trace
should be at least 25
mils away from any other
toggling signal.
COMP[0,2] trace width is
18 mils. COMP[1,3] trace
width is 4 mils.

Length match within 25 mils.
The trace width/space/other is
20/7/25.

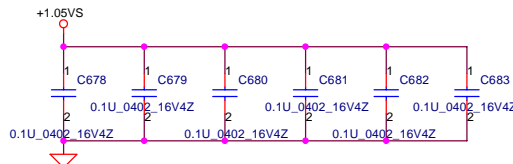
Close to CPU pin
within 500mils.

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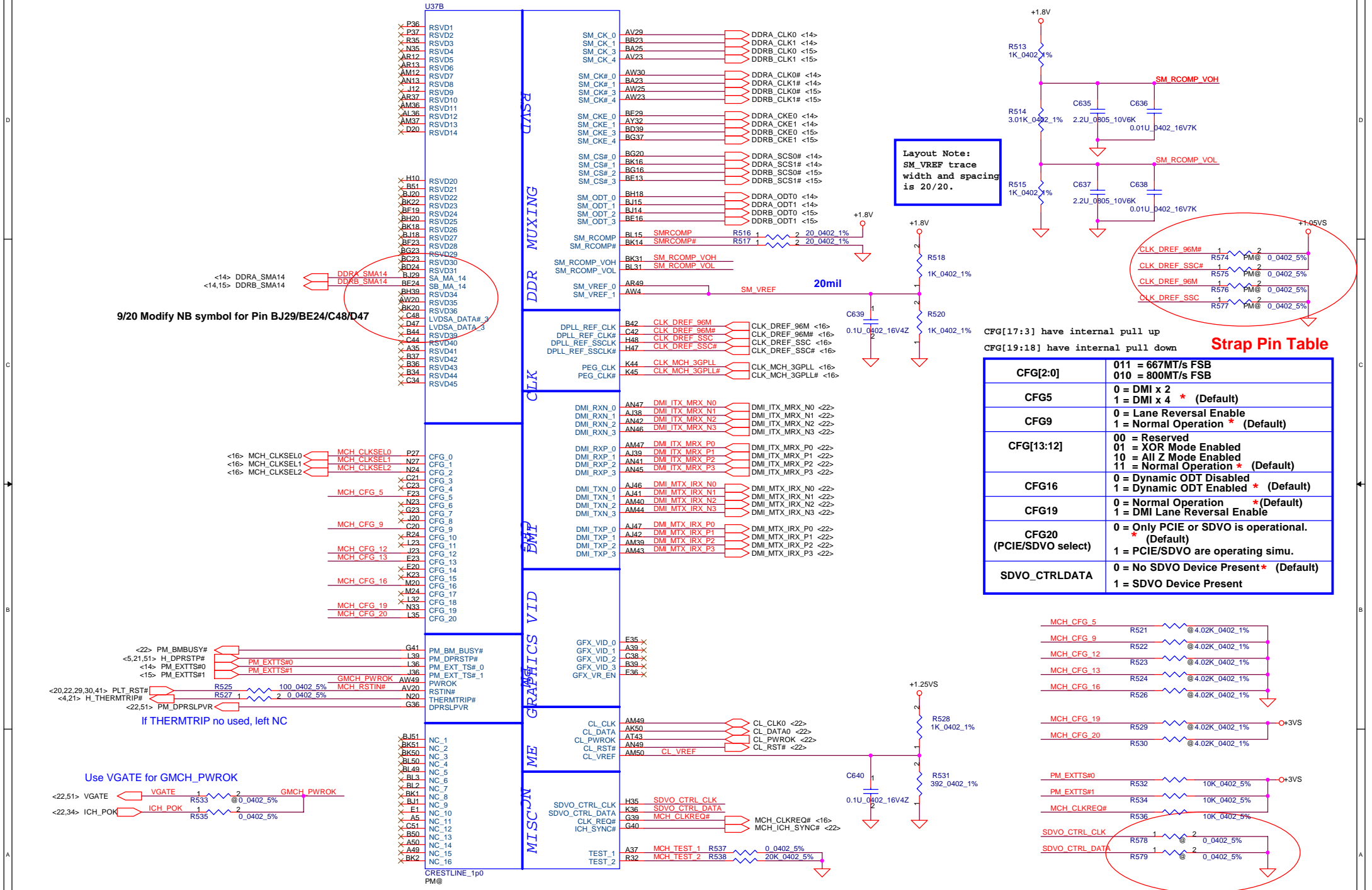
+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



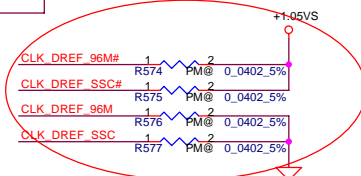
CRB no stuff. Reserved!

9/25 10U checked. OK for use!

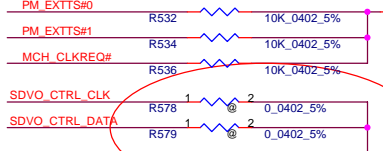
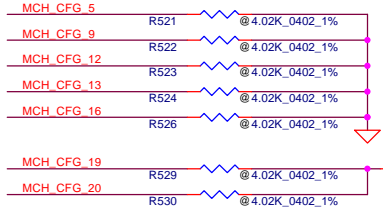
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Layout Note:
SM_VREF trace
width and spacing
is 20/20.



Strap Pin Table	
CFG[2:0]	011 = 667MT/s FSB 010 = 800MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. (Default) 1 = PCIe/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present



<14> DDRA_SDQ[0..63] <--> DDRA_SDQ[0..63]
<14> DDRA_SDM[0..7] <--> DDRA_SDM[0..7]
<14> DDRA_SMA[0..13] <--> DDRA_SMA[0..13]

<15> DDRB_SDQ[0..63] <--> DDRB_SDQ[0..63]
<15> DDRB_SDM[0..7] <--> DDRB_SDM[0..7]
<15> DDRB_SMA[0..13] <--> DDRB_SMA[0..13]

U37D
DDRA_SDQ0 AR43 SA_DQ_0
DDRA_SDQ1 AW44 SA_DQ_1
DDRA_SDQ2 BA45 SA_DQ_2
DDRA_SDQ3 AY46 SA_DQ_3
DDRA_SDQ4 AR41 SA_DQ_4
DDRA_SDQ5 AR45 SA_DQ_5
DDRA_SDQ6 AT42 SA_DQ_6
DDRA_SDQ7 AW47 SA_DQ_7
DDRA_SDQ8 BB45 SA_DQ_8
DDRA_SDQ9 BF48 SA_DQ_9
DDRA_SDQ10 BG47 SA_DQ_10
DDRA_SDQ11 BA45 SA_DQ_11
DDRA_SDQ12 BB47 SA_DQ_12
DDRA_SDQ13 BG50 SA_DQ_13
DDRA_SDQ14 BH49 SA_DQ_14
DDRA_SDQ15 BE45 SA_DQ_15
DDRA_SDQ16 AW44 SA_DQ_16
DDRA_SDQ17 BA45 SA_DQ_17
DDRA_SDQ18 BG42 SA_DQ_18
DDRA_SDQ19 BE40 SA_DQ_19
DDRA_SDQ20 BF44 SA_DQ_20
DDRA_SDQ21 BH45 SA_DQ_21
DDRA_SDQ22 BG40 SA_DQ_22
DDRA_SDQ23 BE40 SA_DQ_23
DDRA_SDQ24 AR40 SA_DQ_24
DDRA_SDQ25 AW40 SA_DQ_25
DDRA_SDQ26 AT39 SA_DQ_26
DDRA_SDQ27 AW36 SA_DQ_27
DDRA_SDQ28 AW41 SA_DQ_28
DDRA_SDQ29 AY41 SA_DQ_29
DDRA_SDQ30 AV38 SA_DQ_30
DDRA_SDQ31 AT38 SA_DQ_31
DDRA_SDQ32 AV13 SA_DQ_32
DDRA_SDQ33 AT13 SA_DQ_33
DDRA_SDQ34 AW11 SA_DQ_34
DDRA_SDQ35 AY11 SA_DQ_35
DDRA_SDQ36 AU15 SA_DQ_36
DDRA_SDQ37 AT11 SA_DQ_37
DDRA_SDQ38 BA13 SA_DQ_38
DDRA_SDQ39 BA11 SA_DQ_39
DDRA_SDQ40 BE10 SA_DQ_40
DDRA_SDQ41 BD10 SA_DQ_41
DDRA_SDQ42 BD8 SA_DQ_42
DDRA_SDQ43 AY9 SA_DQ_43
DDRA_SDQ44 BG10 SA_DQ_44
DDRA_SDQ45 AW9 SA_DQ_45
DDRA_SDQ46 BD7 SA_DQ_46
DDRA_SDQ47 BB9 SA_DQ_47
DDRA_SDQ48 BB5 SA_DQ_48
DDRA_SDQ49 AY7 SA_DQ_49
DDRA_SDQ50 AT5 SA_DQ_50
DDRA_SDQ51 AT7 SA_DQ_51
DDRA_SDQ52 AY6 SA_DQ_52
DDRA_SDQ53 BB7 SA_DQ_53
DDRA_SDQ54 AR5 SA_DQ_54
DDRA_SDQ55 AR8 SA_DQ_55
DDRA_SDQ56 AR9 SA_DQ_56
DDRA_SDQ57 AN3 SA_DQ_57
DDRA_SDQ58 AN8 SA_DQ_58
DDRA_SDQ59 AN10 SA_DQ_59
DDRA_SDQ60 AT9 SA_DQ_60
DDRA_SDQ61 AN9 SA_DQ_61
DDRA_SDQ62 AM9 SA_DQ_62
DDRA_SDQ63 AN11 SA_DQ_63

CRESTLINE_1p0
PM@

DDR SYSTEM MEMORY A

SA_BS_0 BB19 <--> DDRA_SBS0 <14>
SA_BS_1 BK19 <--> DDRA_SBS1 <14>
SA_BS_2 BF29 <--> DDRA_SBS2 <14>
SA_CAS# BL17 <--> DDRA_SCAS# <14>
SA_DM_0 AT45 <--> DDRA_SDM0
SA_DM_1 BD44 <--> DDRA_SDM1
SA_DM_2 BD42 <--> DDRA_SDM2
SA_DM_3 AW38 <--> DDRA_SDM3
SA_DM_4 AW13 <--> DDRA_SDM4
SA_DM_5 BG8 <--> DDRA_SDM5
SA_DM_6 AV5 <--> DDRA_SDM6
SA_DM_7 AN6 <--> DDRA_SDM7
SA_DQS_0 AT46 <--> DDRA_SDQS0 <14>
SA_DQS_1 BE48 <--> DDRA_SDQS1 <14>
SA_DQS_2 BB43 <--> DDRA_SDQS2 <14>
SA_DQS_3 BC37 <--> DDRA_SDQS3 <14>
SA_DQS_4 BB16 <--> DDRA_SDQS4 <14>
SA_DQS_5 BH6 <--> DDRA_SDQS5 <14>
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SA_MA_1 BD20 <--> DDRA_SMA1
SA_MA_2 BK27 <--> DDRA_SMA2
SA_MA_3 BH28 <--> DDRA_SMA3
SA_MA_4 BL24 <--> DDRA_SMA4
SA_MA_5 BK28 <--> DDRA_SMA5
SA_MA_6 BJ27 <--> DDRA_SMA6
SA_MA_7 BJ25 <--> DDRA_SMA7
SA_MA_8 BL28 <--> DDRA_SMA8
SA_MA_9 BA28 <--> DDRA_SMA9
SA_MA_10 BC19 <--> DDRA_SMA10
SA_MA_11 BE28 <--> DDRA_SMA11
SA_MA_12 BG30 <--> DDRA_SMA12
SA_MA_13 BJ16 <--> DDRA_SMA13
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SA_WE# BA19 <--> DDRA_SWE# <14>

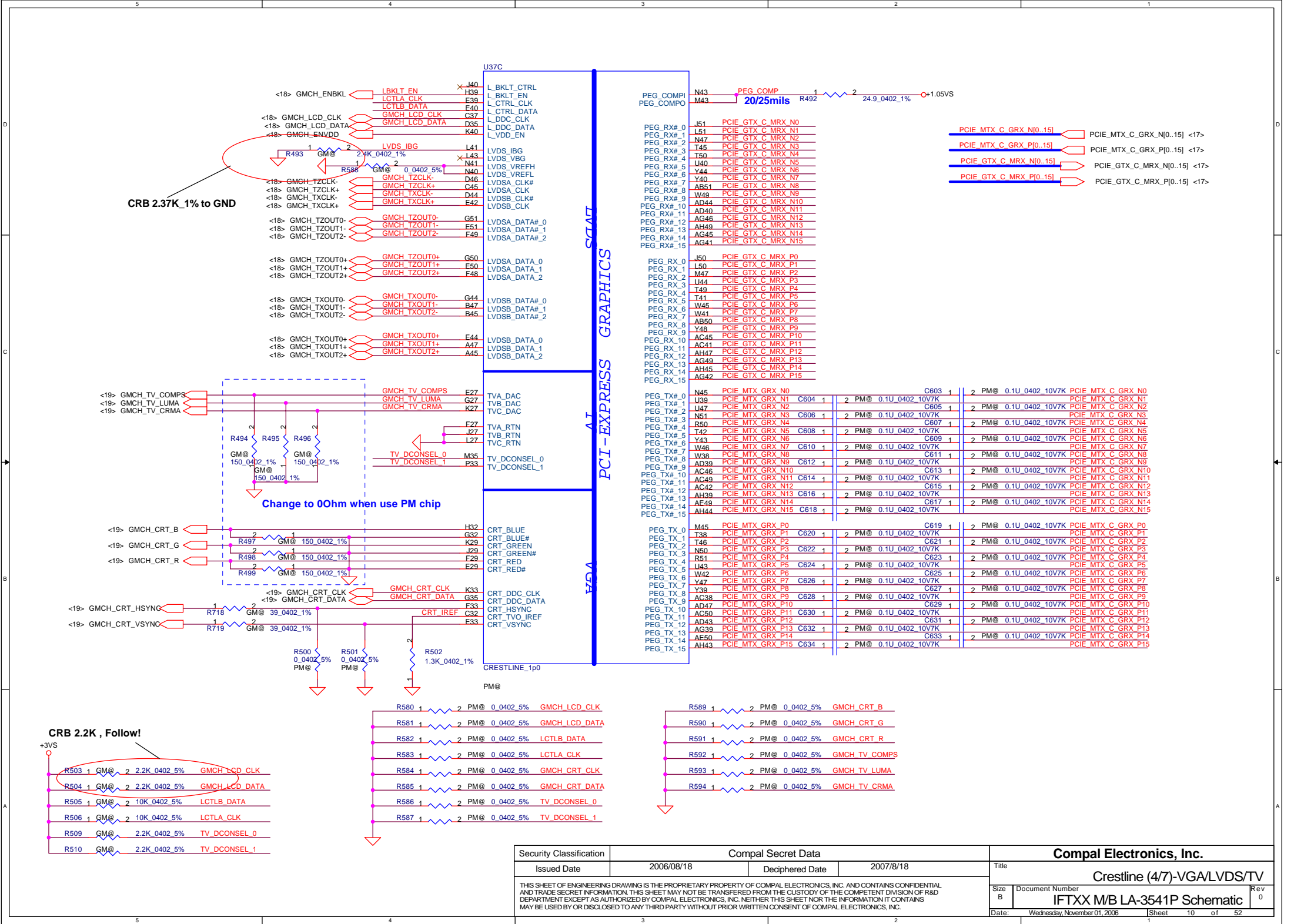
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DDRB_SDQ4 AN51 SB_DQ_4
DDRB_SDQ5 AN50 SB_DQ_5
DDRB_SDQ6 AV50 SB_DQ_6
DDRB_SDQ7 AV49 SB_DQ_7
DDRB_SDQ8 BA50 SB_DQ_8
DDRB_SDQ9 BB50 SB_DQ_9
DDRB_SDQ10 BA49 SB_DQ_10
DDRB_SDQ11 BE50 SB_DQ_11
DDRB_SDQ12 BA51 SB_DQ_12
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DDRB_SDQ14 BF50 SB_DQ_14
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DDRB_SDQ48 BF4 SB_DQ_48
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DDRB_SDQ50 BG1 SB_DQ_50
DDRB_SDQ51 BC2 SB_DQ_51
DDRB_SDQ52 BK3 SB_DQ_52
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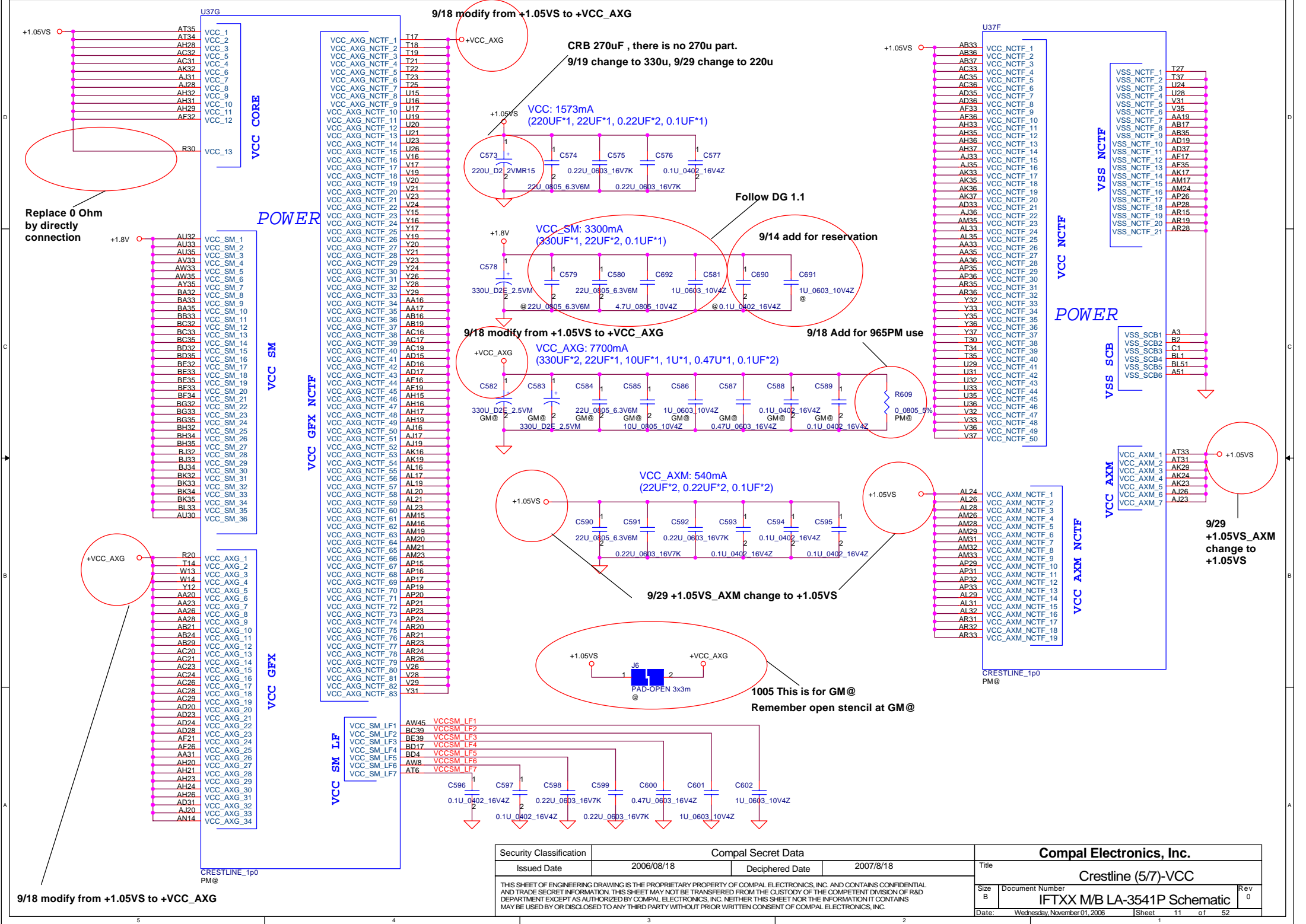
DDR SYSTEM MEMORY B

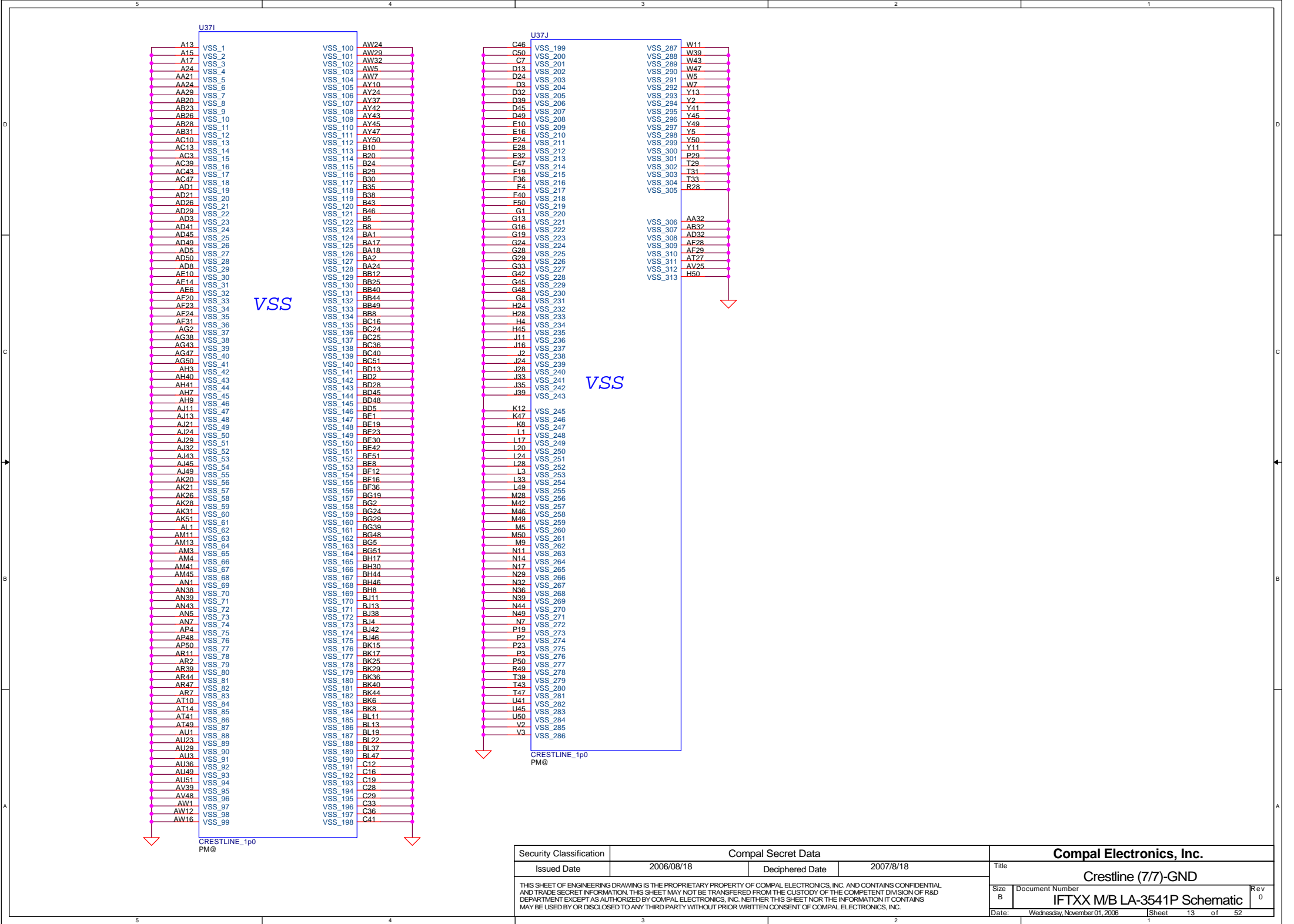
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SB_DM_2 BK45 <--> DDRB_SDM2
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SB_DM_4 BH12 <--> DDRB_SDM4
SB_DM_5 BJ7 <--> DDRB_SDM5
SB_DM_6 BF3 <--> DDRB_SDM6
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SB_MA_6 BA29 <--> DDRB_SMA6
SB_MA_7 BC28 <--> DDRB_SMA7
SB_MA_8 AY28 <--> DDRB_SMA8
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SB_MA_10 BG17 <--> DDRB_SMA10
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												IFTXX M/B LA-3541P Schematic					
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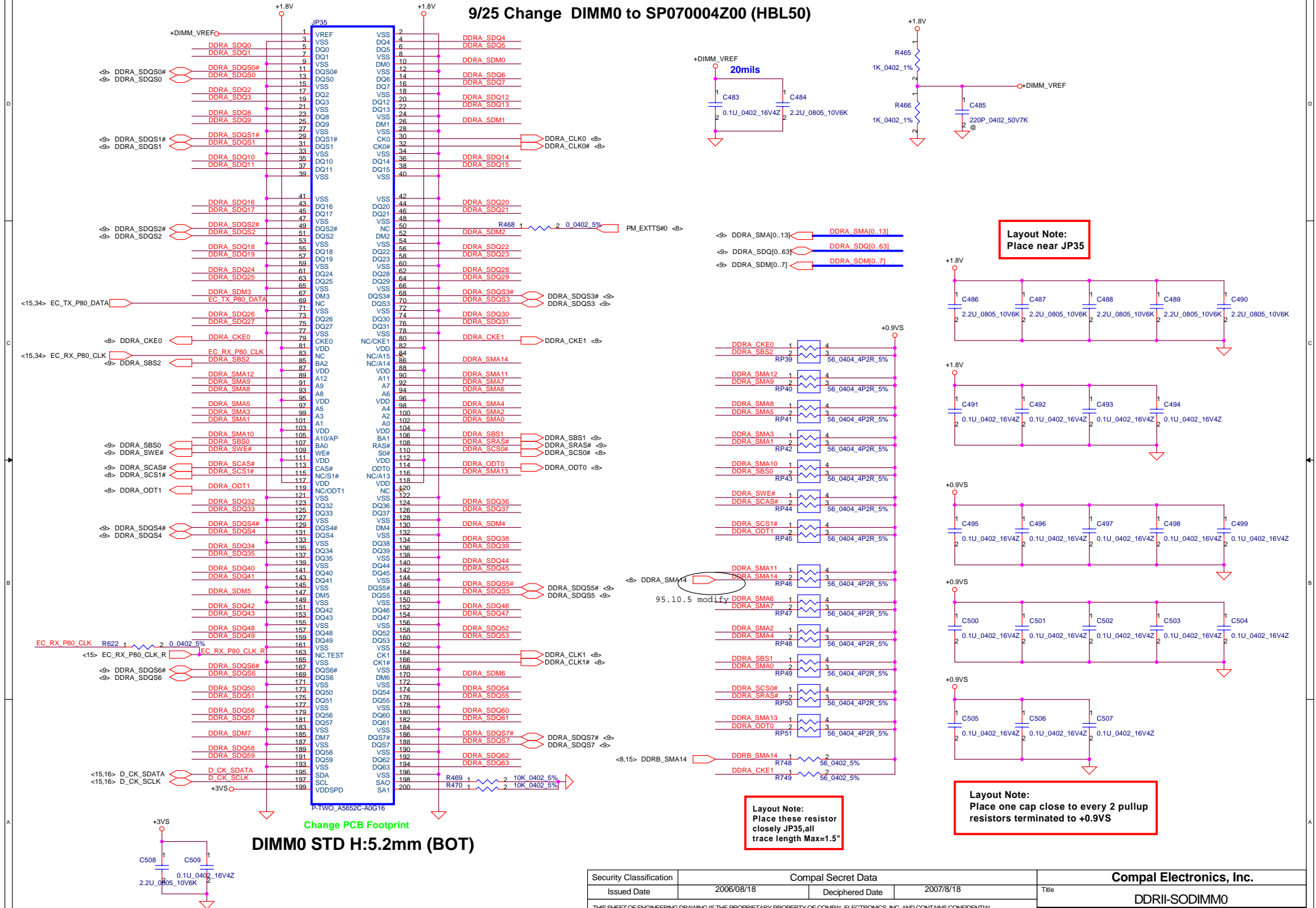






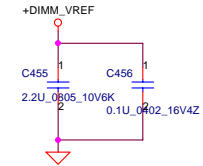
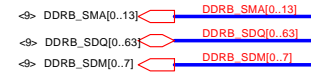
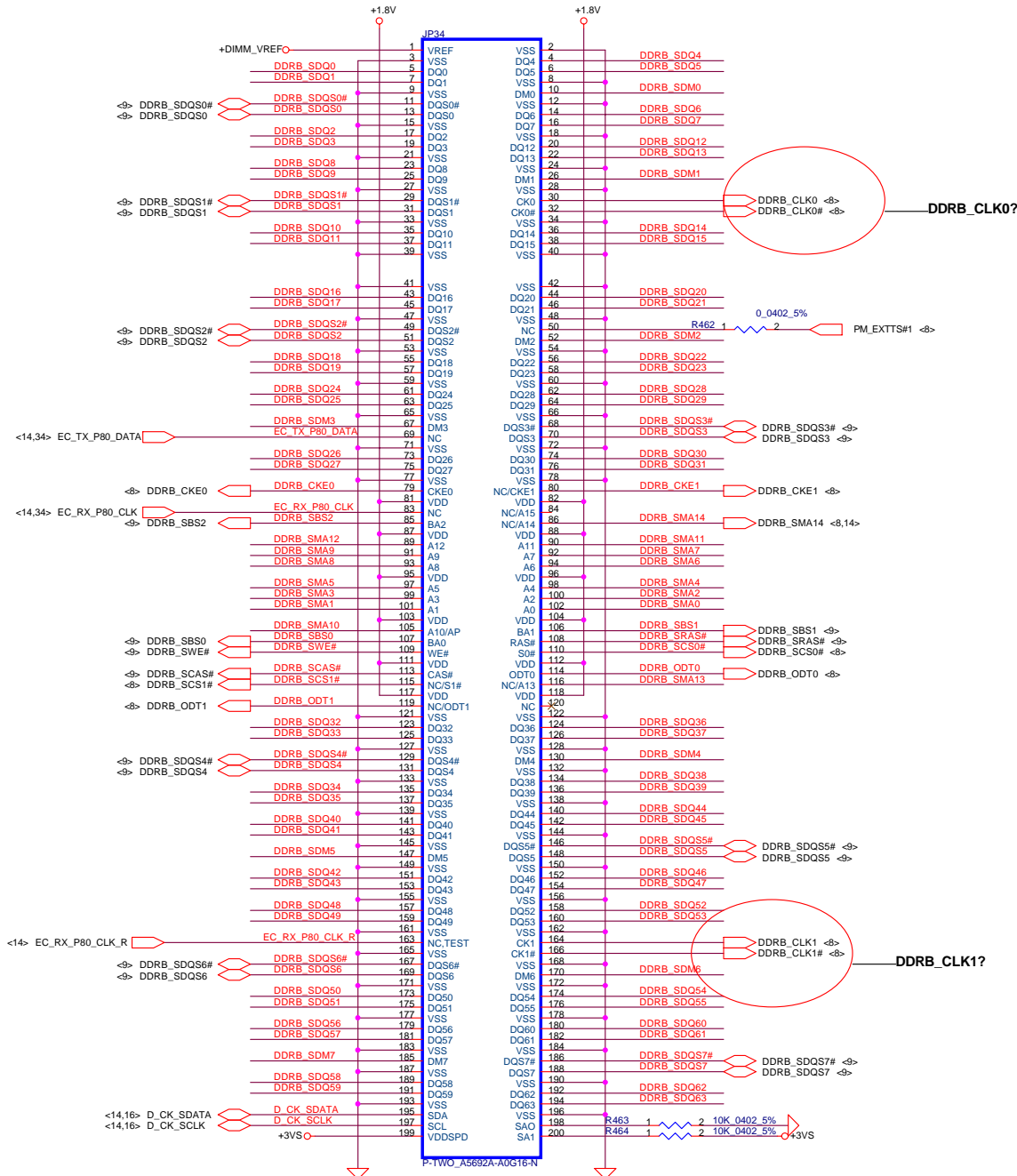
Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Crestline (7/7)-GND	
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				Date: Wednesday, November 01, 2006	Sheet 13 of 52

+1.8V

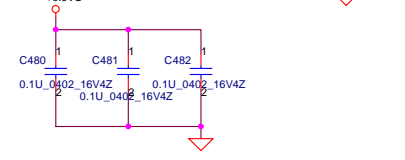
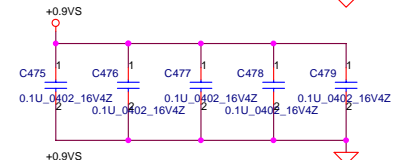
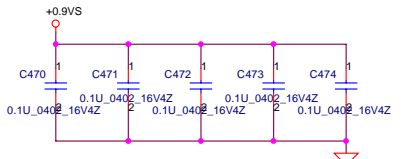
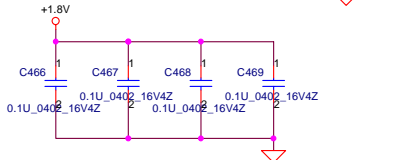
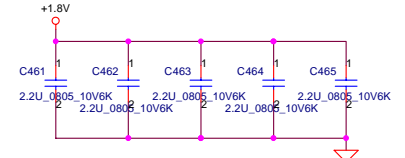


Security Classification		Compal Secret Data		Compal Electronics, Inc.				
Issued Date		2006/08/18		Deciphered Date		2007/8/18		
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				DDRII-SODIMMO				
				Size B	Document Number			Rev 0
				IFTXX M/B LA-3541P Schematic				
				Date:	Wednesday, November 01, 2006		Sheet 14 of 52	

9/25 Change DIMM1 to SP070006F00



Layout Note:
Place near JP34



Layout Note:
Place these resistor closely JP35, all trace length Max=1.5"

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

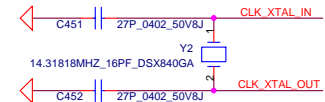
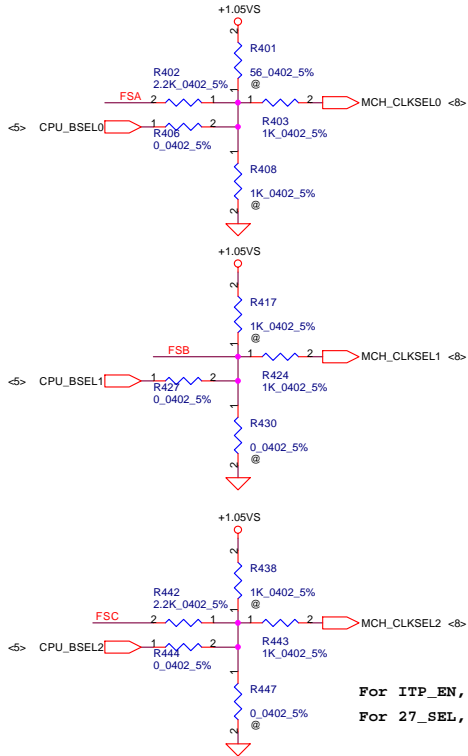
DIMM1 STD H:9.2mm (BOT)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size B	Document Number	IFTXX M/B LA-3541P Schematic		Rev 0	
Date:	Wednesday, November 01, 2006	Sheet	15	of	52

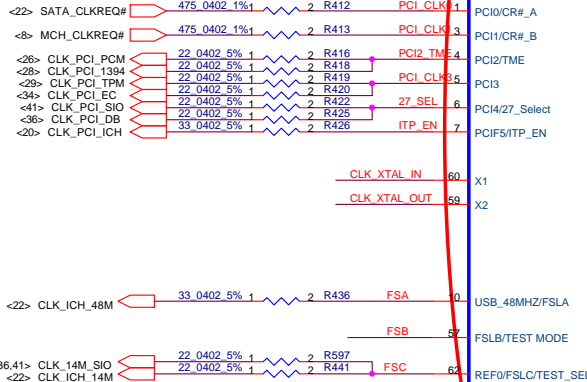
FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Set:

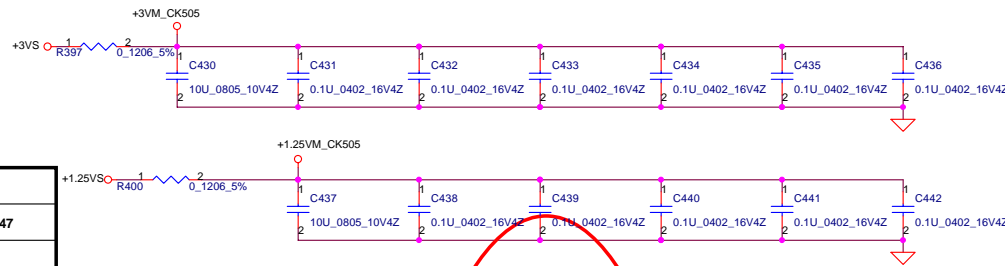
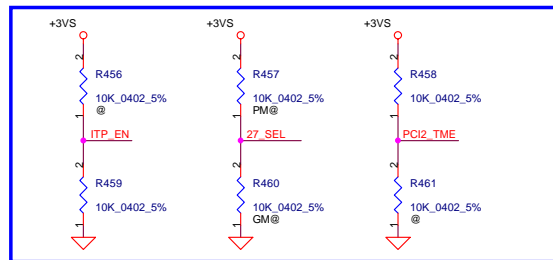
CPU Driven	Stuff	R401	R408	R417	R430	R438	R447
★ (Default)	No Stuff	R401	R408	R417	R430	R438	R447
667MHz	Stuff	R401	R417	R447			
	No Stuff	R408	R430	R438			
800MHz	Stuff	R408	R417	R447			
	No Stuff	R401	R430	R438			



Routing the trace at least 10mil

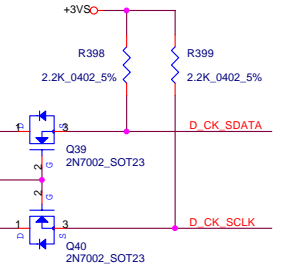
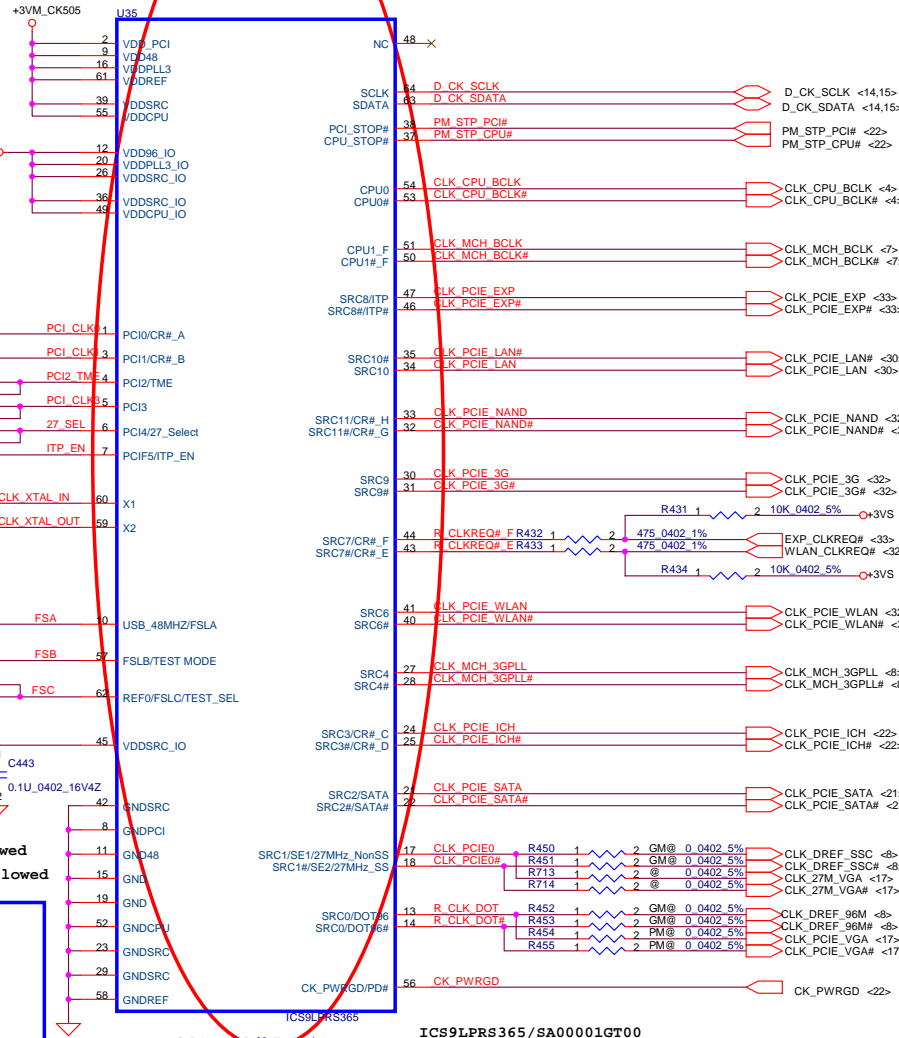


For ITP_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1 = Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed



10/17 : Change P/N from SA0001GT00 to SA00001GT10

Need to update Symbol







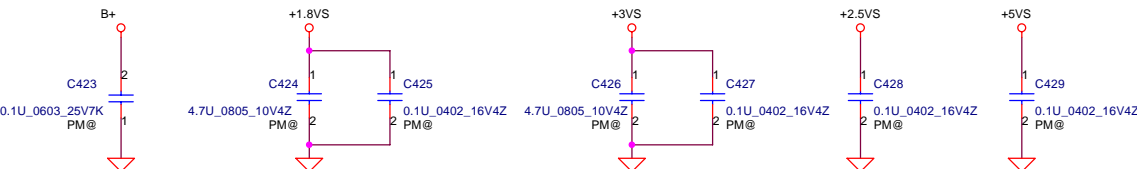
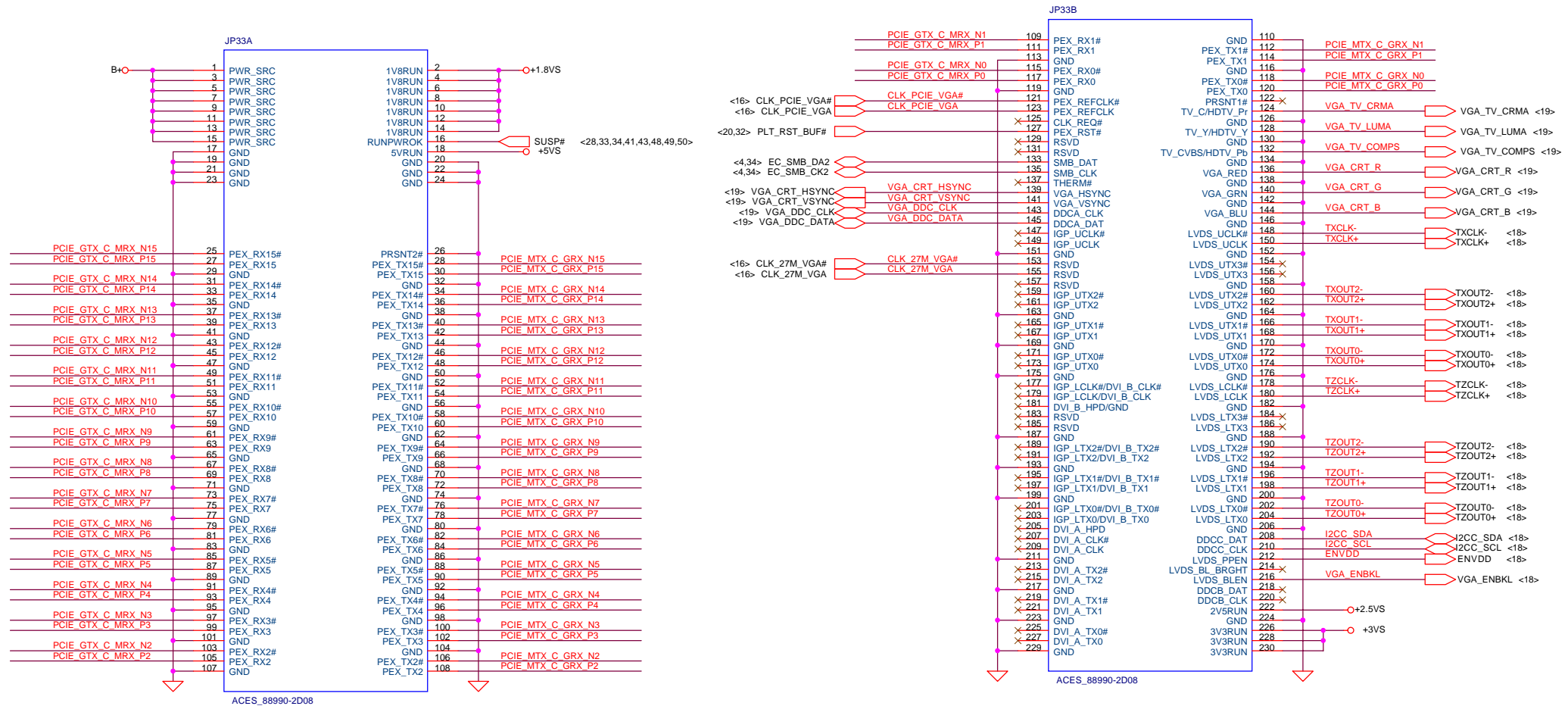
C444	2	1	CLK_ICH_48M
C445	2	1	CLK_ICH_14M
C446	2	1	CLK_PCIE_ICH
C447	2	1	CLK_14M_SIO
C448	2	1	CLK_PCIE_PCM
C449	2	1	CLK_PCIE_EC
C450	2	1	CLK_PCIE_SIO

Place close to U35

Security Classification	Compal Secret Data	Title	
Issued Date	2006/08/04	Deciphered Date	2006/10/06
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Date: Wednesday, November 01, 2006		Sheet 16 of 52	Rev 0.1

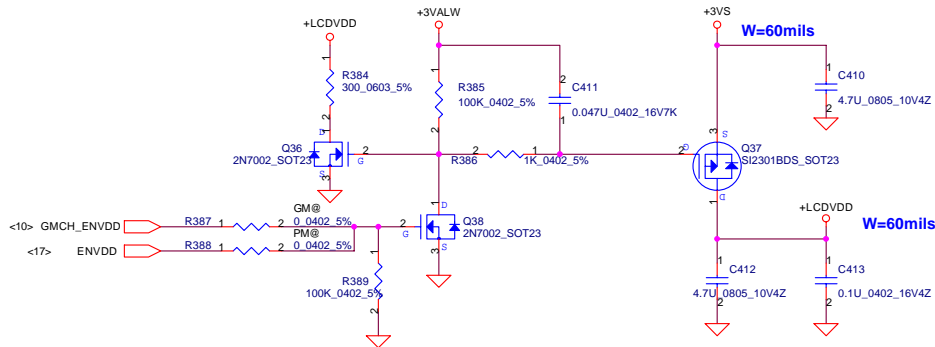
9/13 modify this footprint from ACES_88990-2D08_230P to ACES_88990-2D28_230P

<10> PCIE_MTX_C_GRX_N[0..15]  PCIE_MTX_C_GRX_N[0..15]
 <10> PCIE_MTX_C_GRX_P[0..15]  PCIE_MTX_C_GRX_P[0..15]
 <10> PCIE_GTX_C_MRX_N[0..15]  PCIE_GTX_C_MRX_N[0..15]
 <10> PCIE_GTX_C_MRX_P[0..15]  PCIE_GTX_C_MRX_P[0..15]

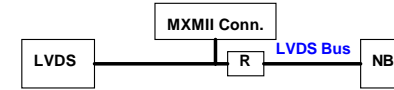


Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2006/08/18		Deciphered Date		2007/8/18		Title			
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						Size		Document Number		Rev	
						Custom		IFTXX M/B LA-3541P Schematic		0	
						Date:		Wednesday, November 01, 2006		Sheet 17 of 52	

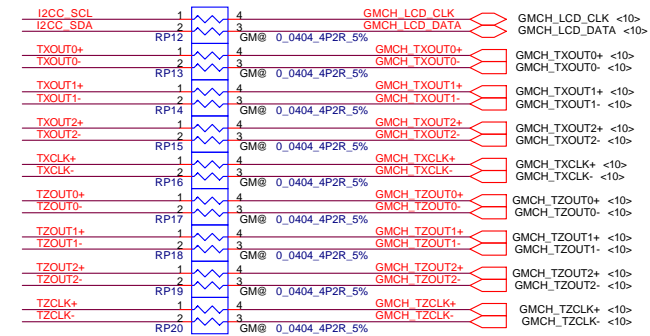
LCD POWER CIRCUIT



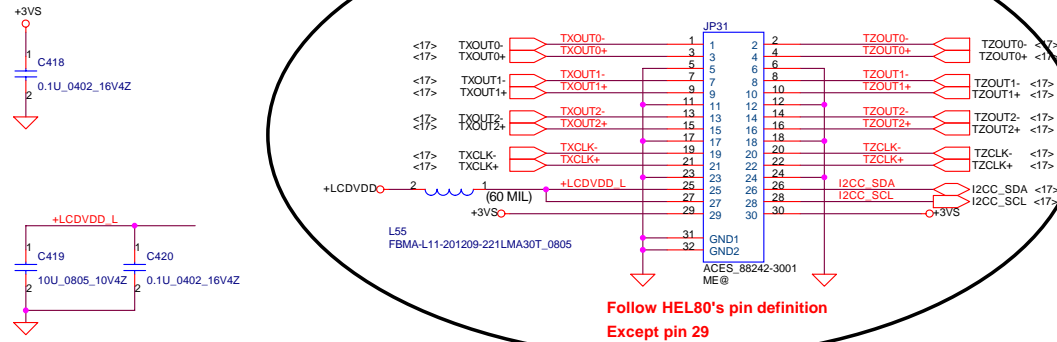
Routing Diagram



Use Daisy chain to route

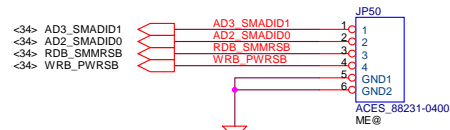


LCD/PANEL BD. Conn.

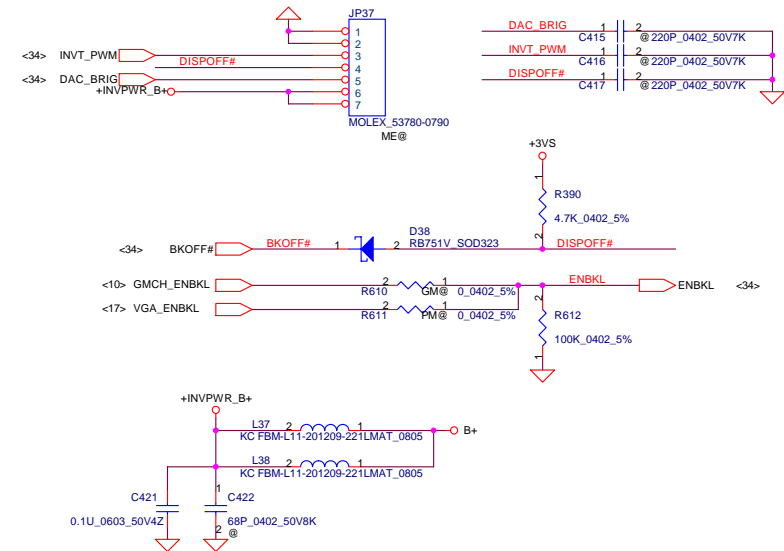


Follow HEL80's pin definition
Except pin 29

JEPICO Conn.

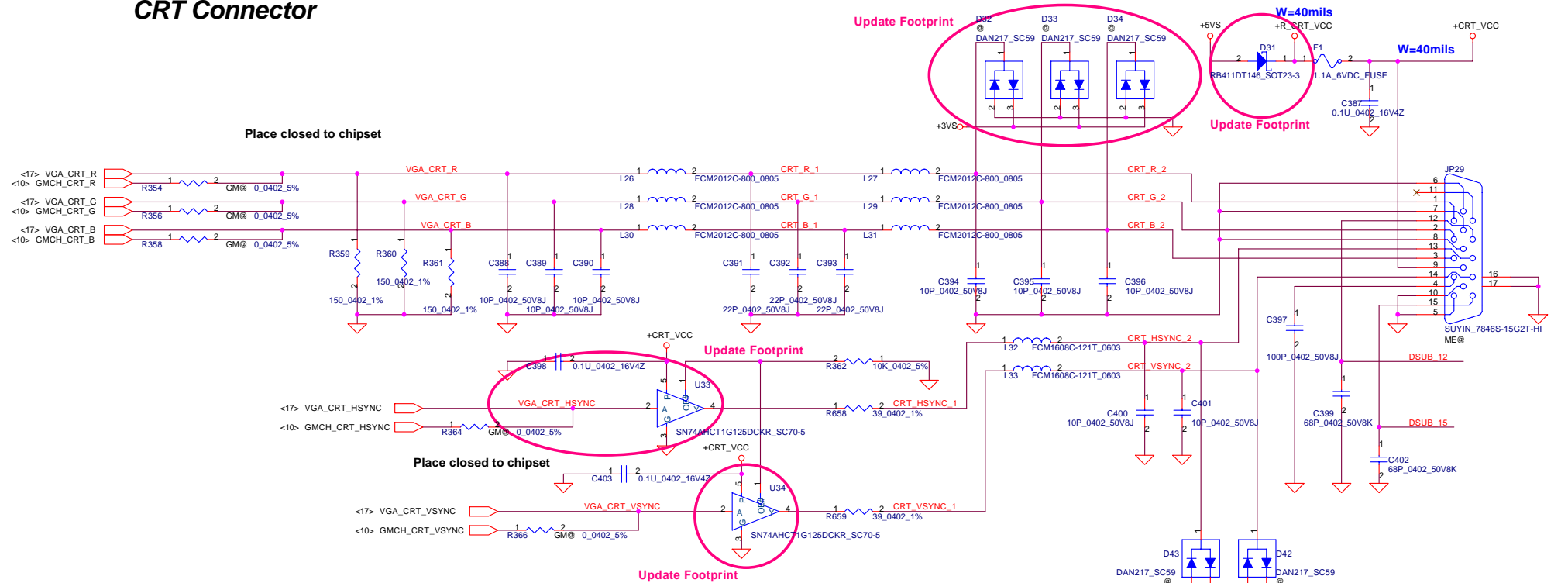
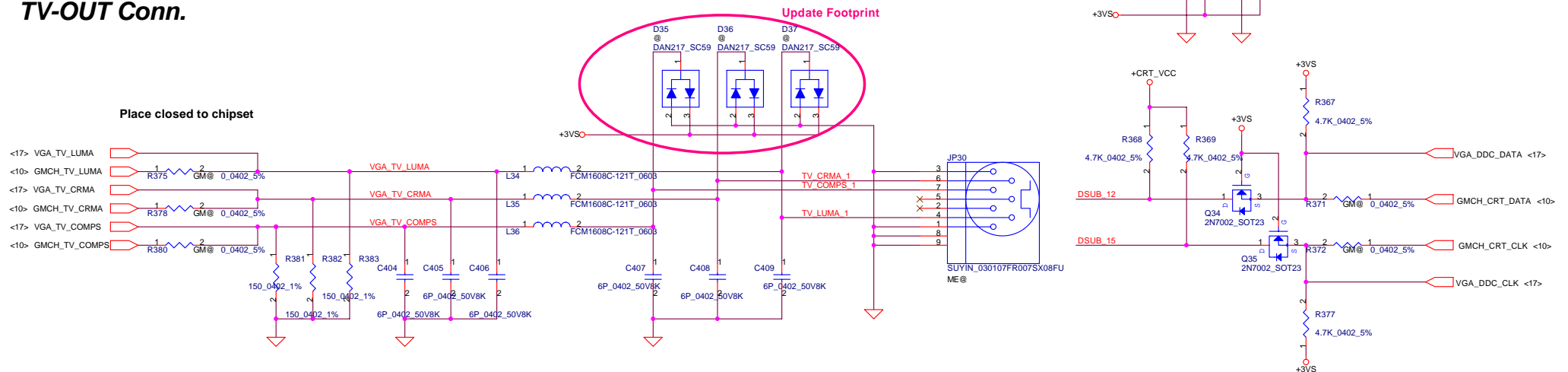


INVERTER Conn.

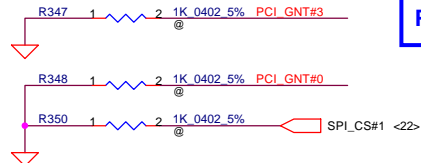
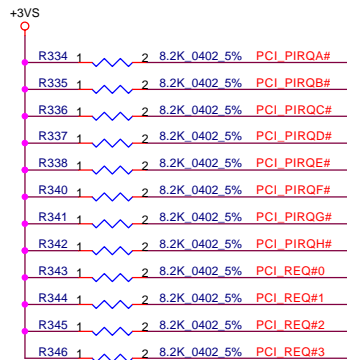
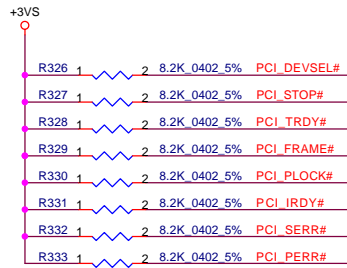


Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	LVDS & DVI Connector	
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				ITFX MB LA-3541P Schematic	
				Date: Wednesday, November 01, 2006	Sheet 18 of 52

CRT Connector

**TV-OUT Conn.**

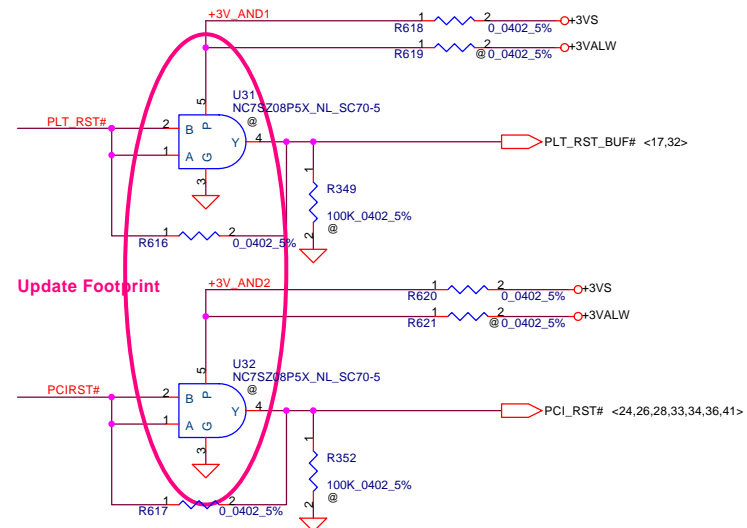
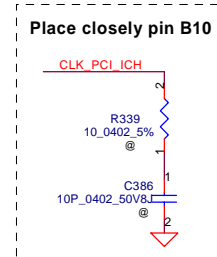
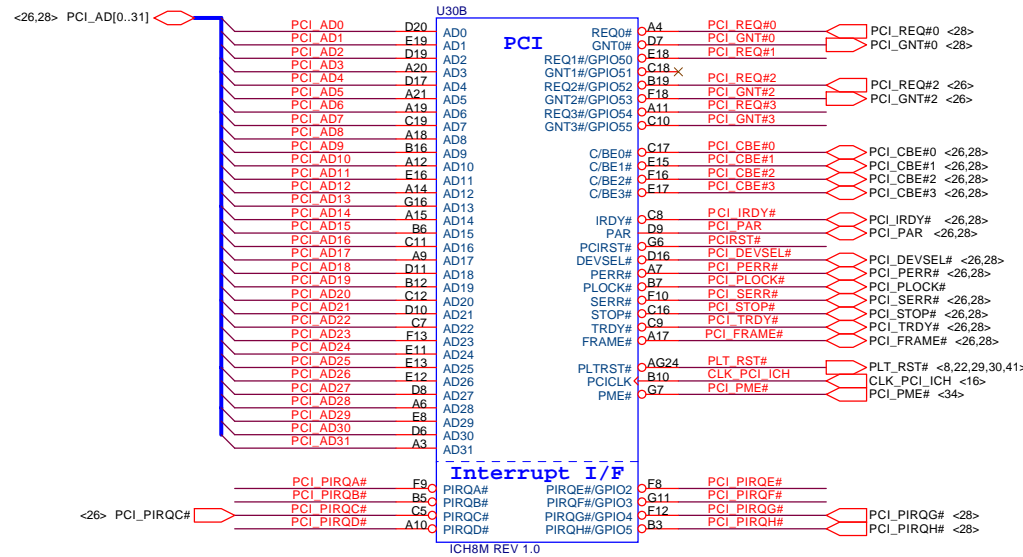
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	CRT & TV-OUT Connector		
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				IFTXX M/B LA-3541P Schematic			
				Date:	Wednesday, November 01, 2006	Sheet	19 of 52

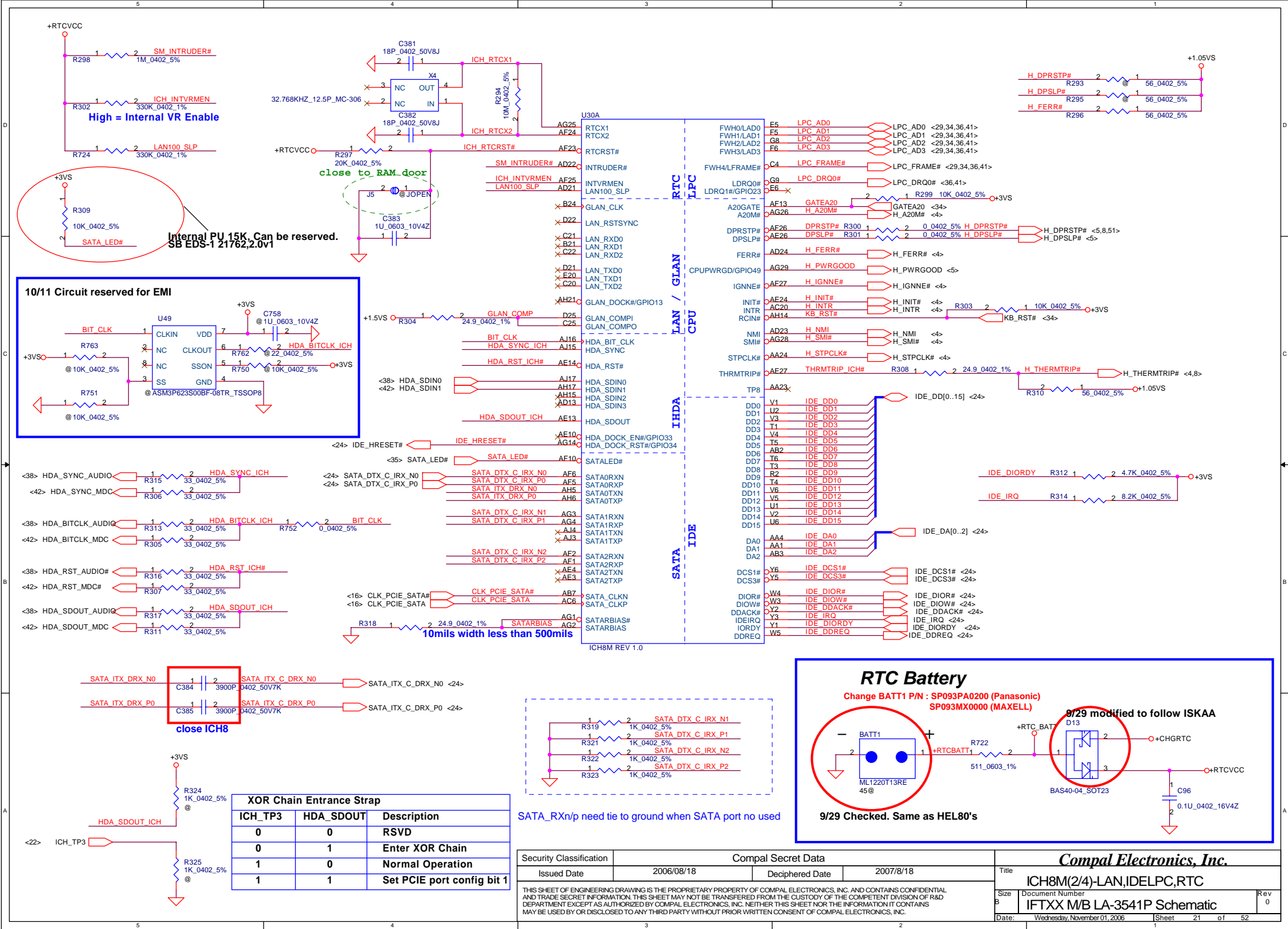


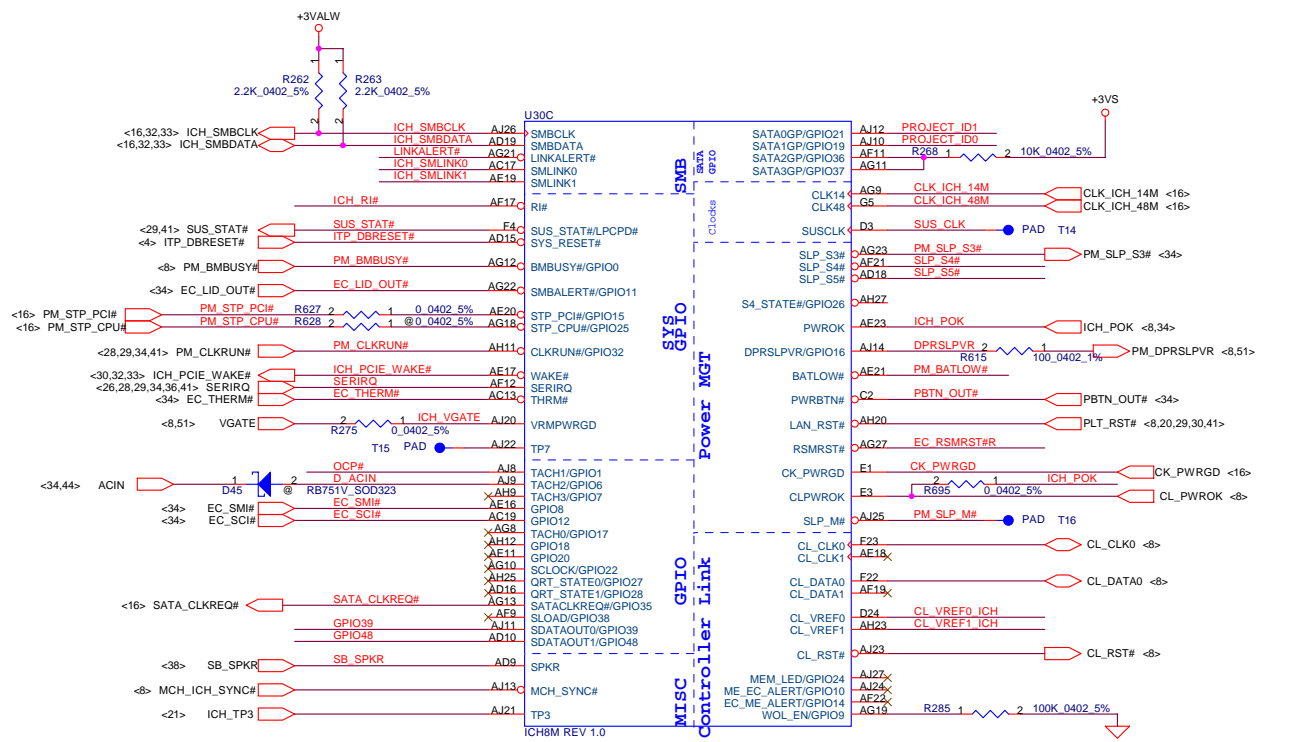
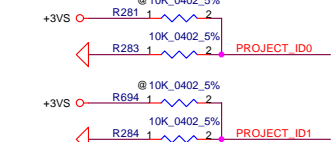
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

10/17 : Change P/N from SA000010G00 to SA00001JU10
 10/17 : FootPrint : SA000010G00
 BOM : SA00001JU10







LAN

NEW Card

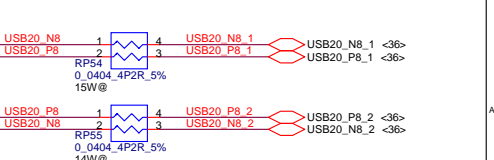
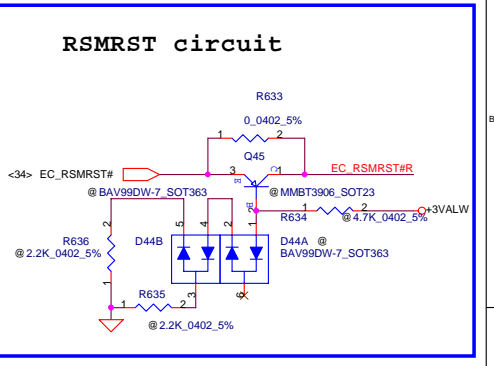
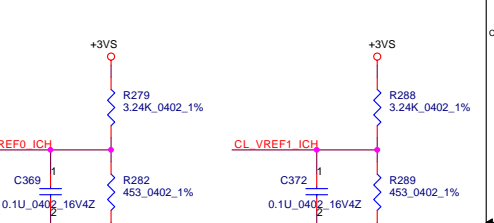
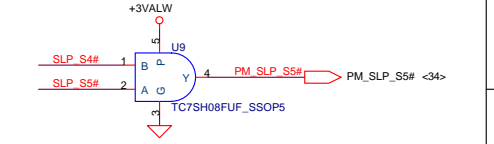
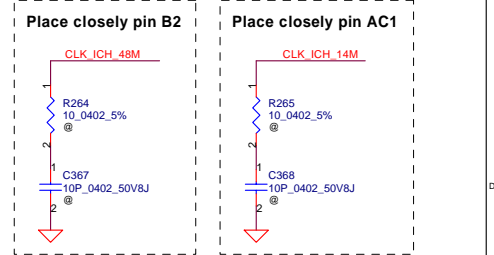
Robson

3G

WLAN

Need to define PROJECT ID

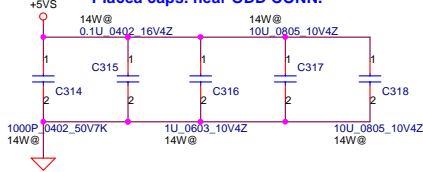
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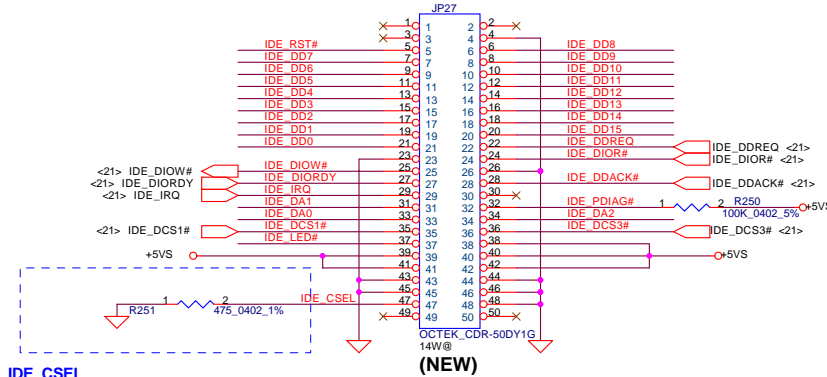
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i>		
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	ICH8M(34)-USB,GPIO,PCIE	
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				Customer	M/B LA-3541P Schematic	0
				Date:	Wednesday, November 01, 2006	Sheet 22 of 52

14W ODD Conn.

Place caps. near ODD CONN.



<21> IDE_DD[0..15] IDE DD[0..15]
<21> IDE_DA[0..2] IDE DA[0..2]



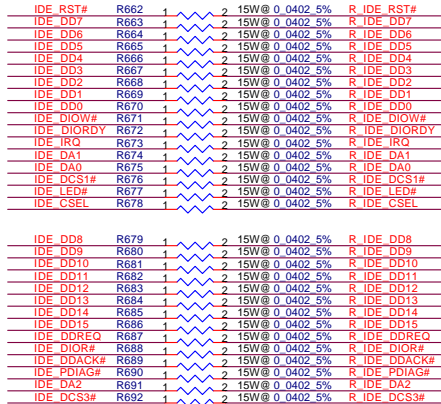
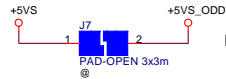
IDE_CSEL
Grounding for Master (When use SATA HDD)
Open or High for Slaver (Normal)

(NEW)

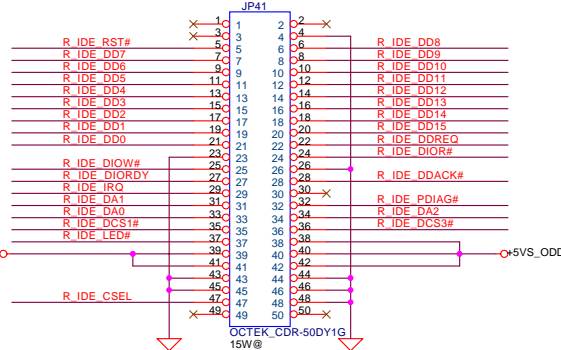
+5VS R252 100K_0402_5%

15W ODD Conn.

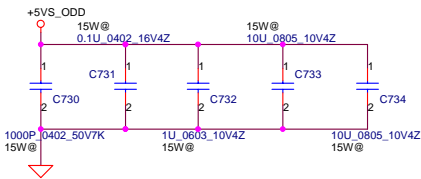
Remember Short at 15W@



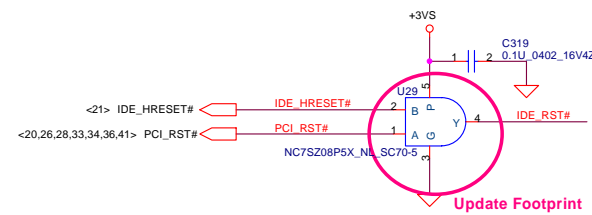
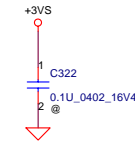
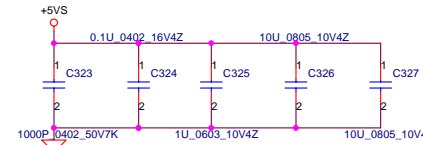
+5VS_ODD



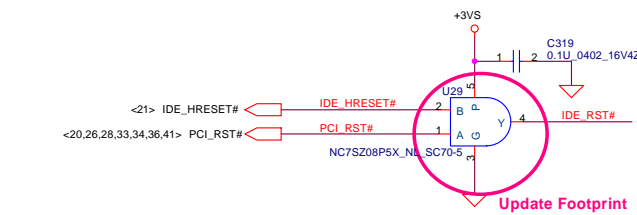
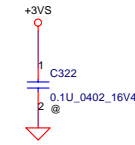
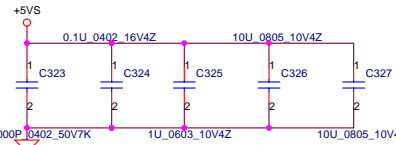
OCTEK_CDR-50DY1G
15W@



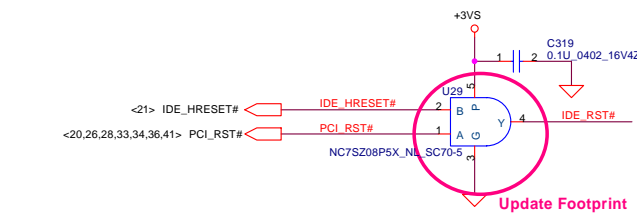
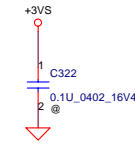
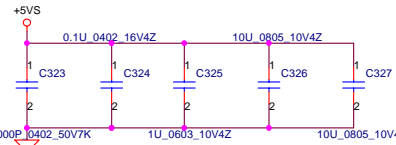
SATA HDD Conn.



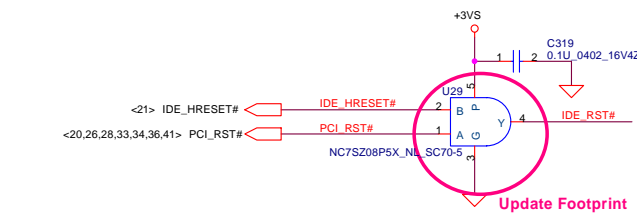
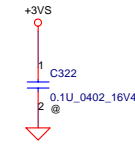
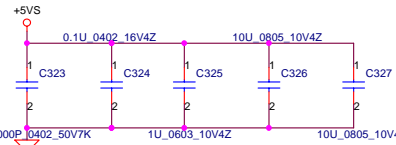
Update Footprint



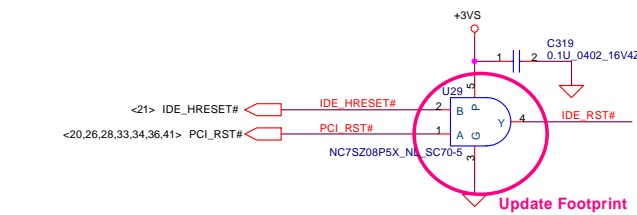
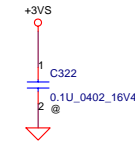
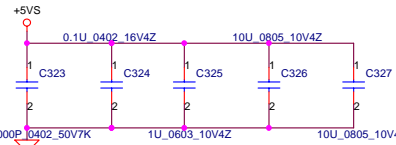
Update Footprint



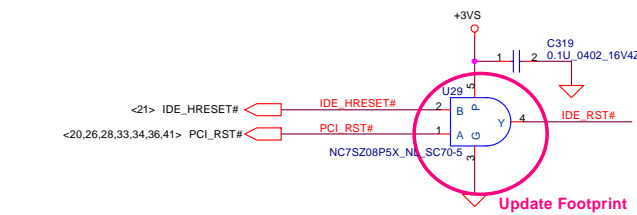
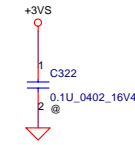
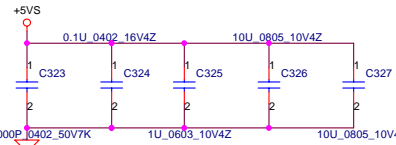
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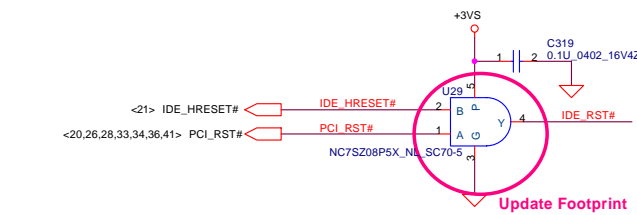
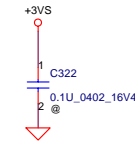
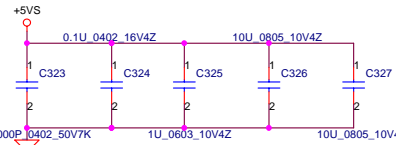
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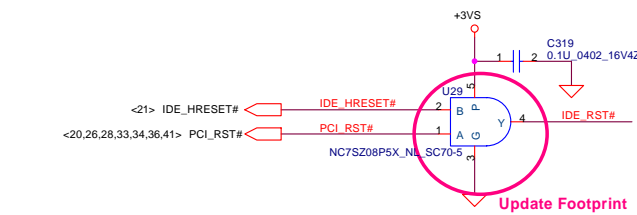
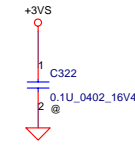
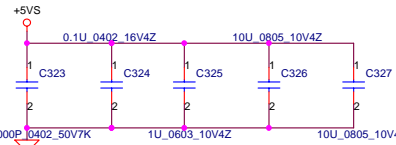
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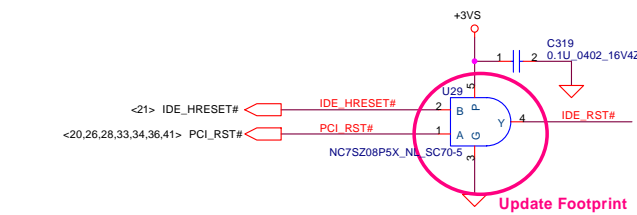
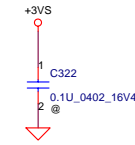
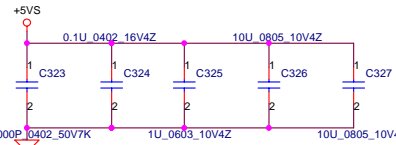
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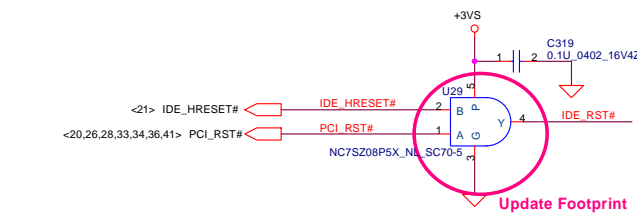
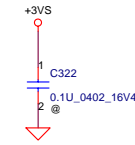
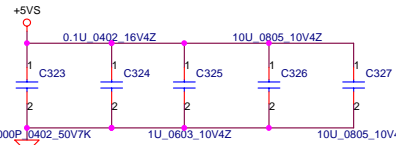
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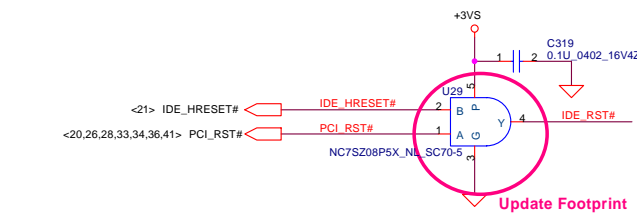
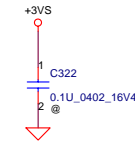
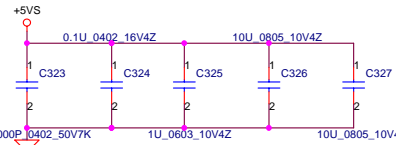
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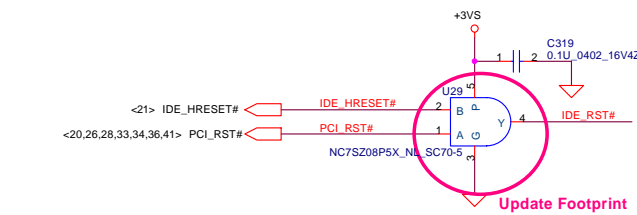
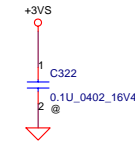
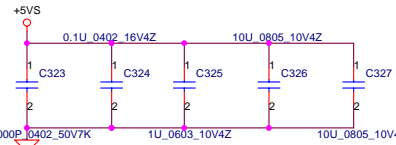
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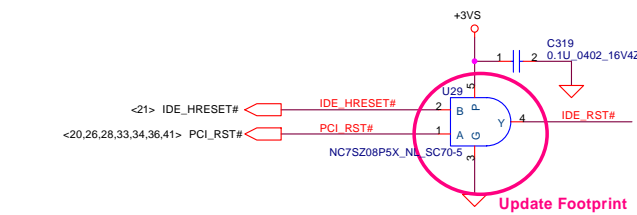
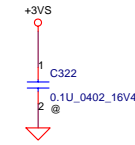
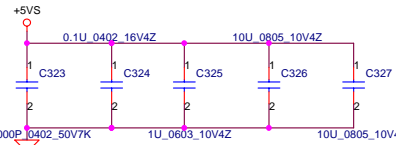
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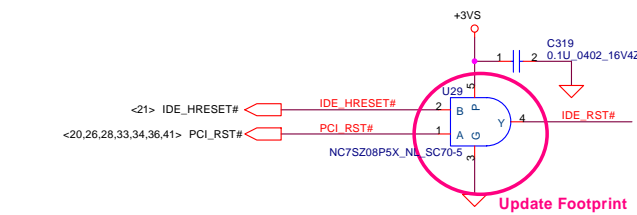
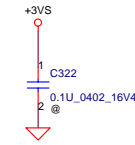
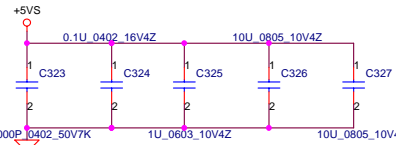
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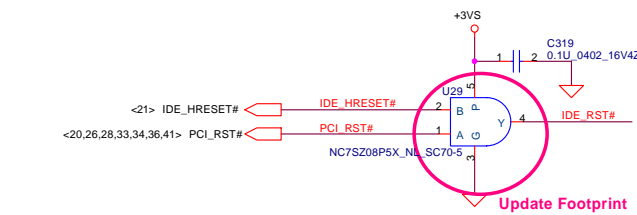
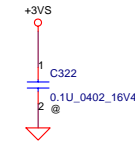
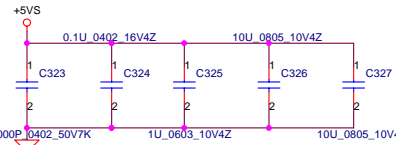
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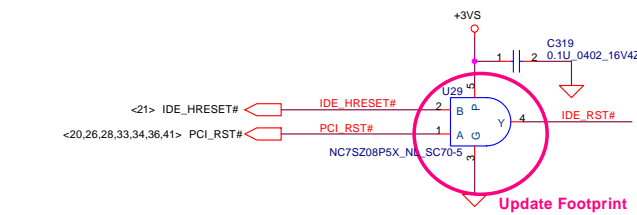
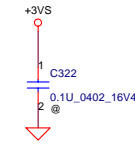
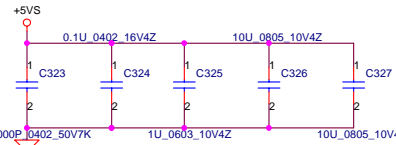
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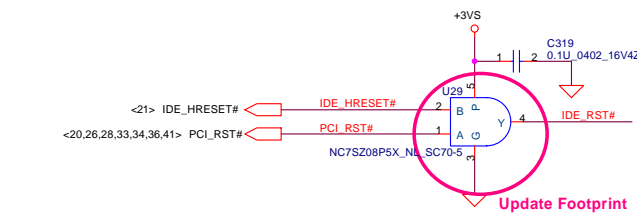
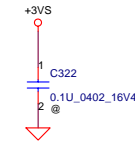
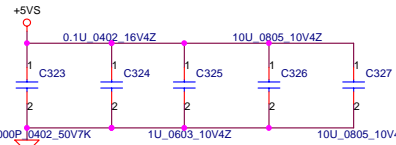
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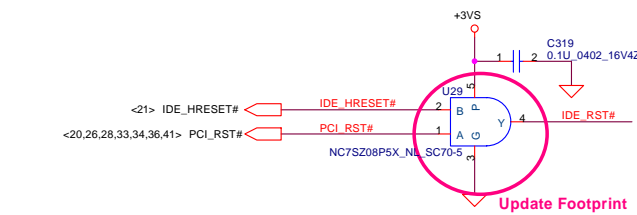
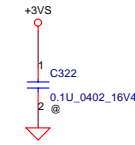
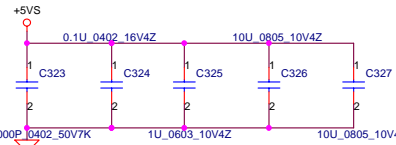
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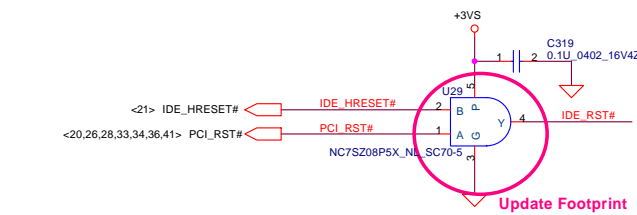
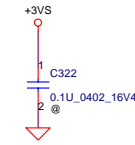
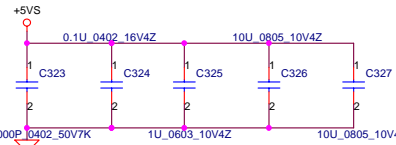
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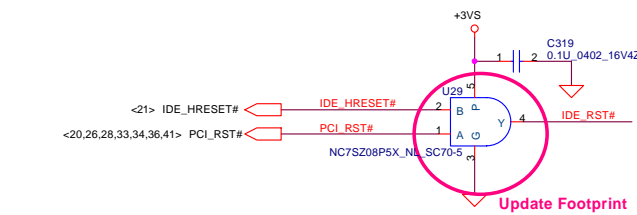
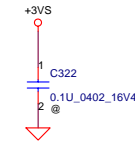
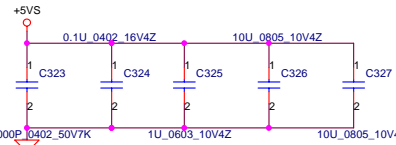
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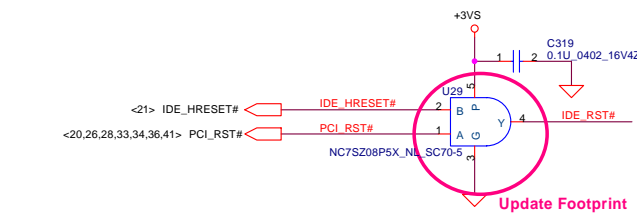
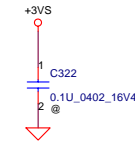
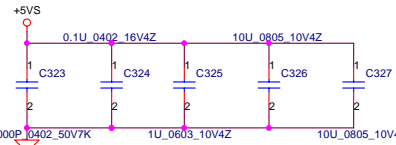
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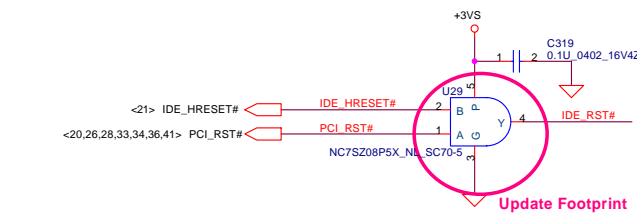
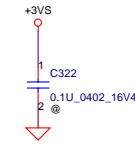
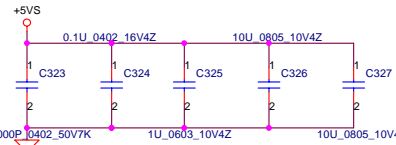
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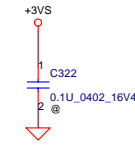
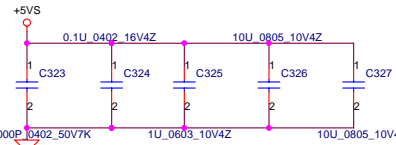
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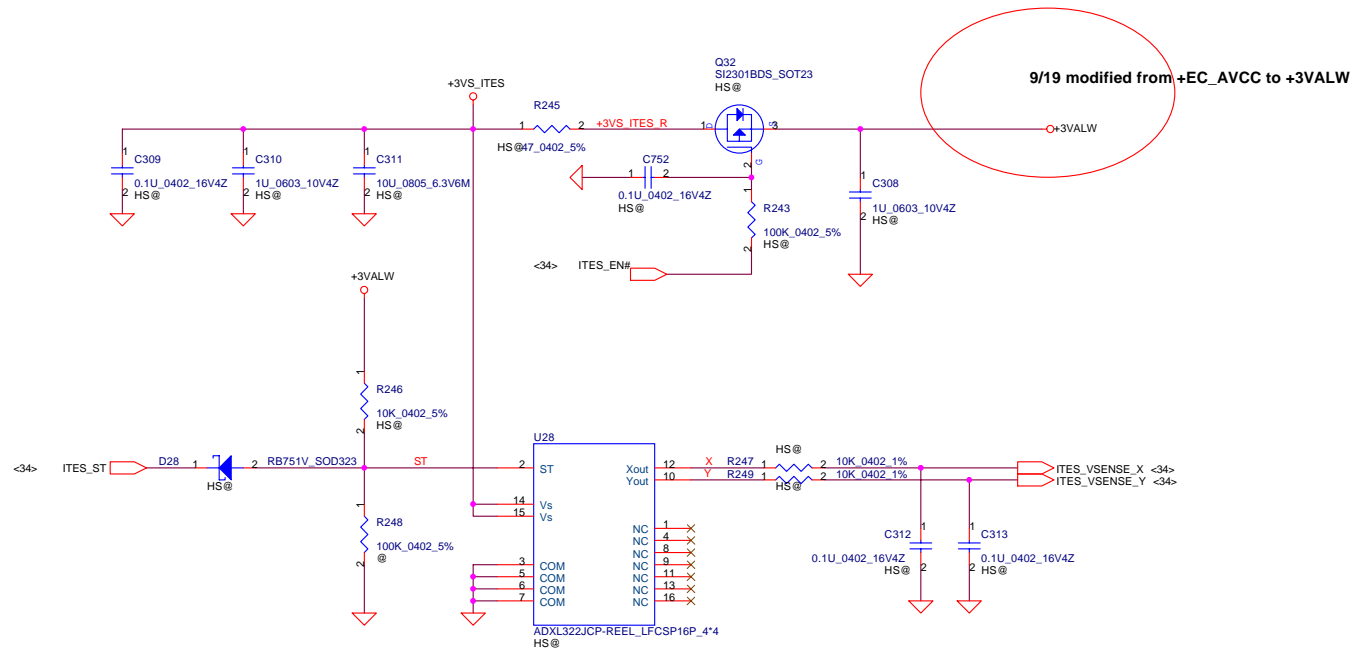
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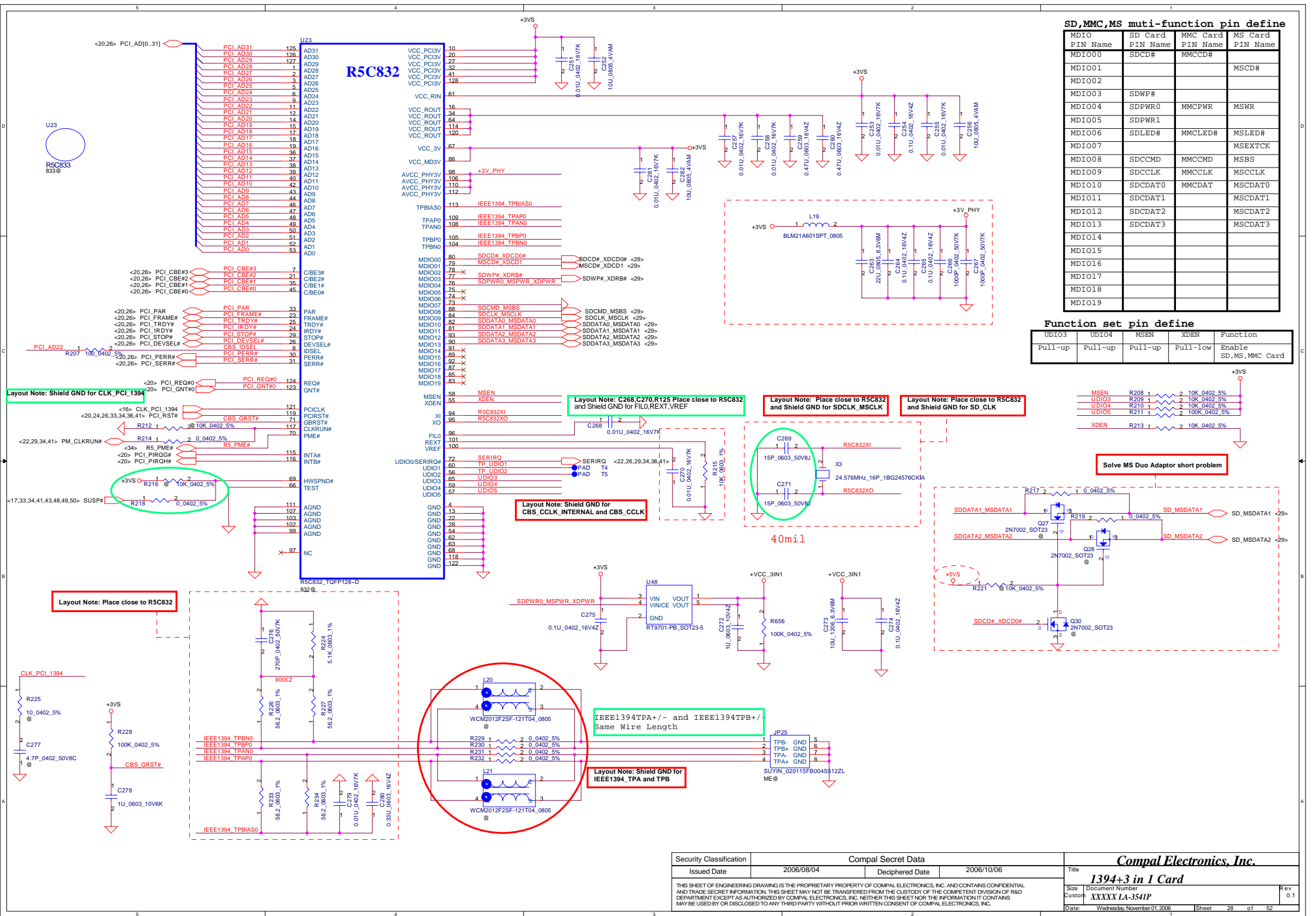
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Note : BOM structure HS@ is for Heng shan IFT10/11 this model

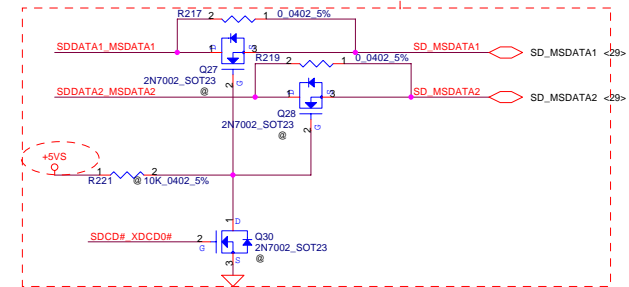
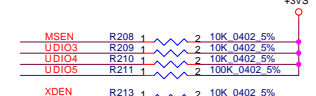


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				Date: Wednesday, November 01, 2006	Rev 0.1
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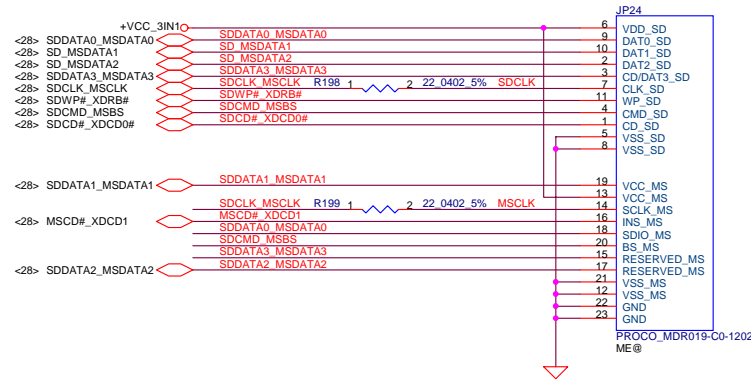


SD,MMC,MS multi-function pin define			
MDIO	SD Card	MMC Card	MS Card
PIN Name	PIN Name	PIN Name	PIN Name
MDIO00	SDCD#	MMCCD#	
MDIO01			MSCD#
MDIO02			
MDIO03	SDWP#		
MDIO04	SDPWR0	MMCPWR	MSWR
MDIO05	SDPWR1		
MDIO06	SDLED#	MMCLED#	MSLED#
MDIO07			MSEXTCK
MDIO08	SDCCMD	MMCCMD	MSBS
MDIO09	SDCLK	MMCLK	MSCCLK
MDIO10	SDCDAT0	MMC DAT	MSCDAT0
MDIO11	SDCDAT1		MSCDAT1
MDIO12	SDCDAT2		MSCDAT2
MDIO13	SDCDAT3		MSCDAT3
MDIO14			
MDIO15			
MDIO16			
MDIO17			
MDIO18			
MDIO19			

Function set pin define			
UDIO3	UDIO4	MSEN	XDEN
Pull-up	Pull-up	Pull-up	Pull-low
			Enable
			SD, MS, MMC Card

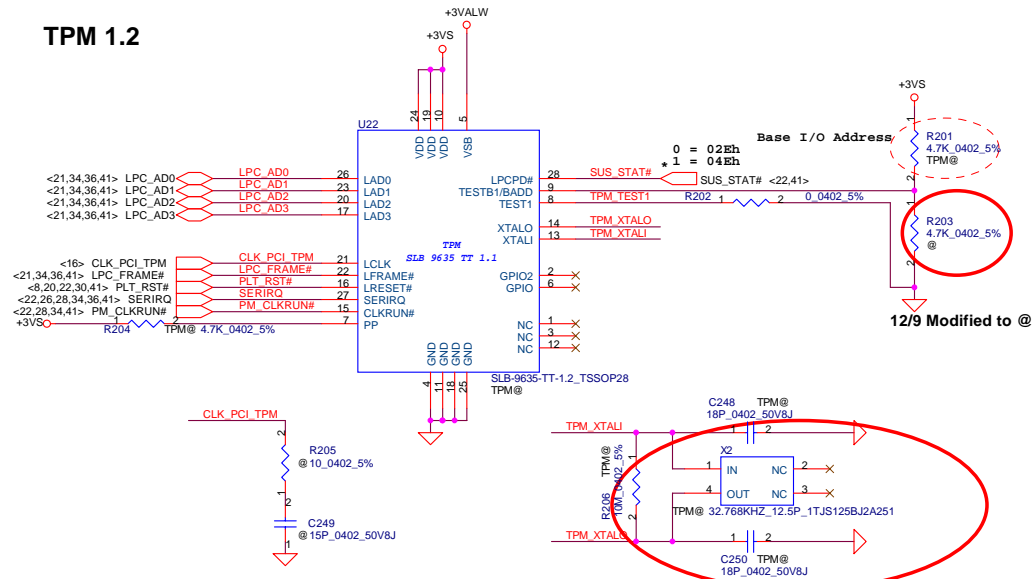


3 in 1 Card Reader

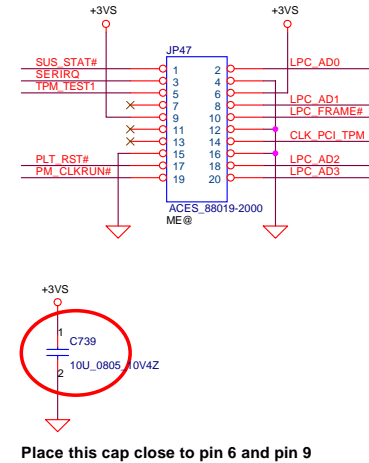


For A30

TPM 1.2



TPM Conn. For C38



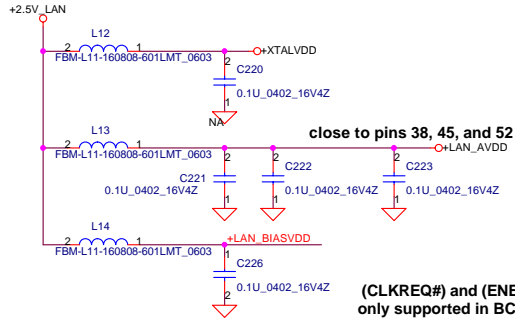
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Issued Date	2006/08/04	Deciphered Date	2006/10/06
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		Sheet	29 of 52

Compal Electronics, Inc.

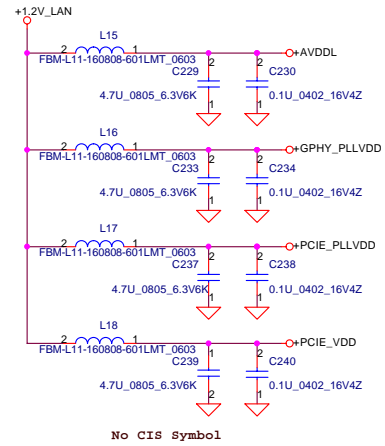
INDICATE LED

Rev 0.1

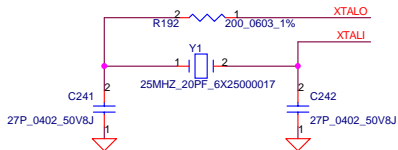
Layout Notice : Filter place as close chip as possible.



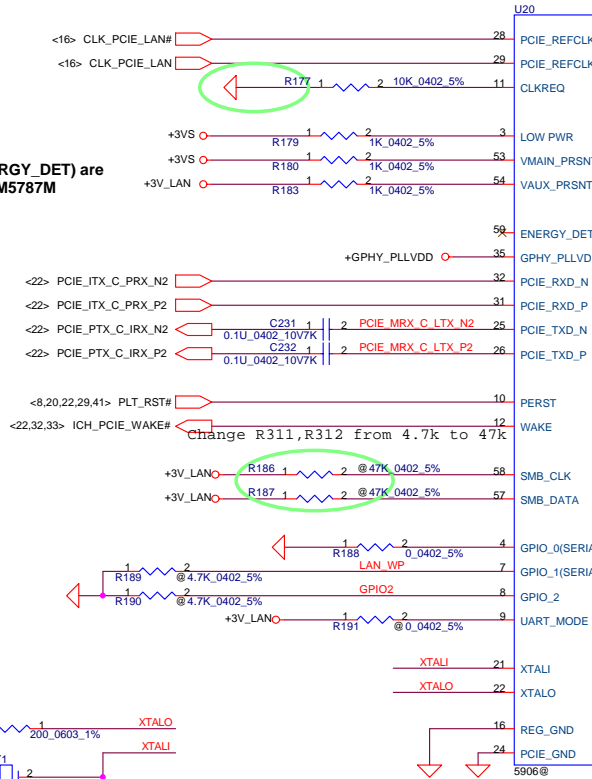
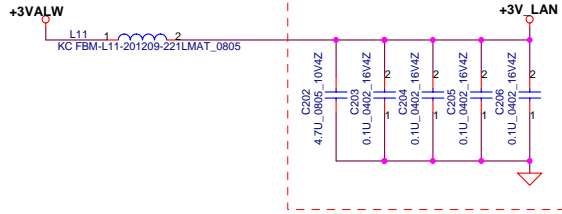
(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M



No CIS Symbol



Layout Notice : Place as close chip as possible.



Change R311, R312 from 4.7k to 47k

LAN_WP

GPIO2

UART_MODE

XTALI

XTALO

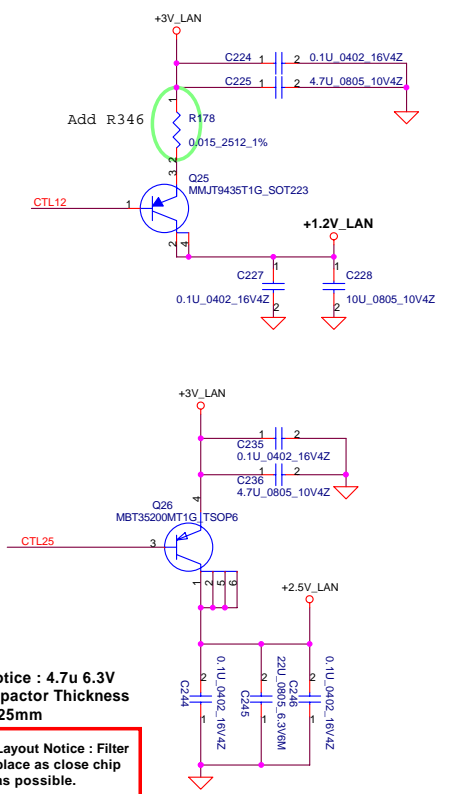
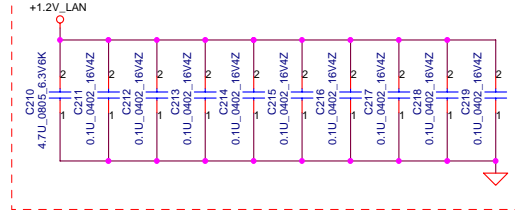
REG_GND

PCIE_GND

5906@

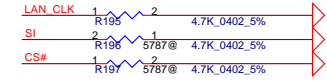
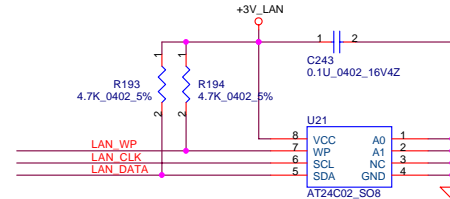


Layout Notice : 1.2V filter. Place as close chip as possible.

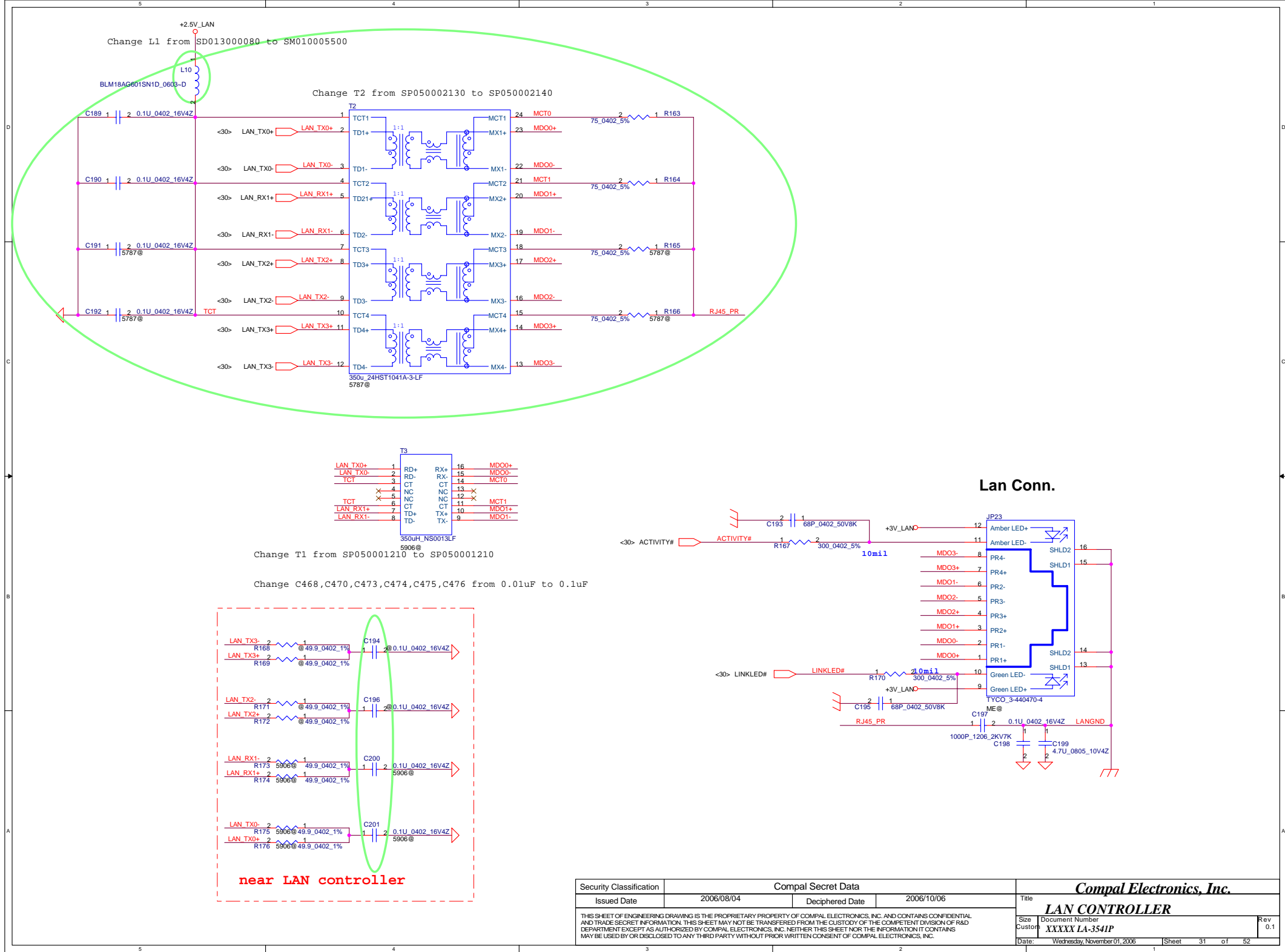


Notice : 4.7u 6.3V capacitor Thickness 1.25mm

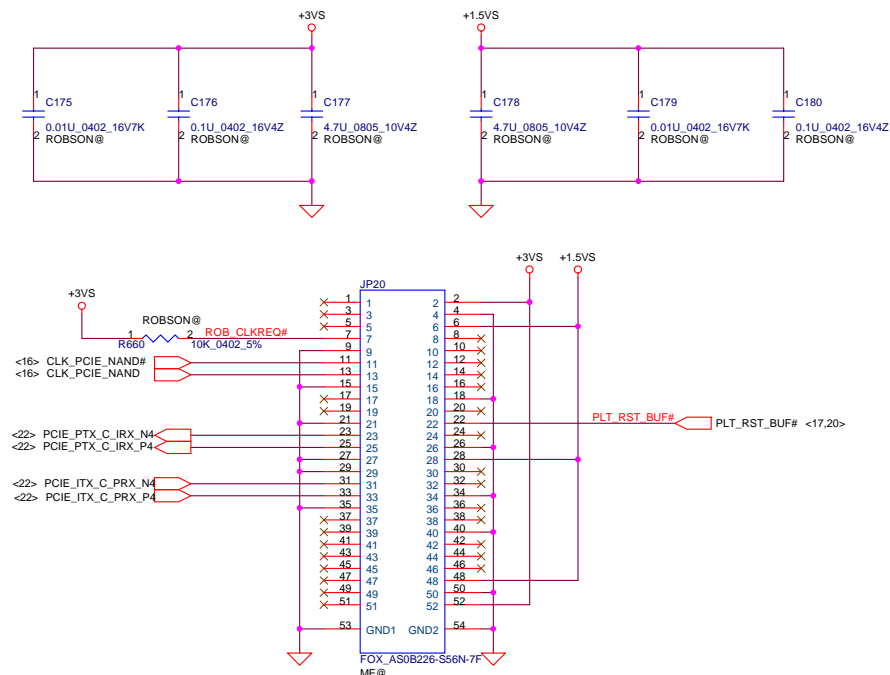
Layout Notice : Filter place as close chip as possible.



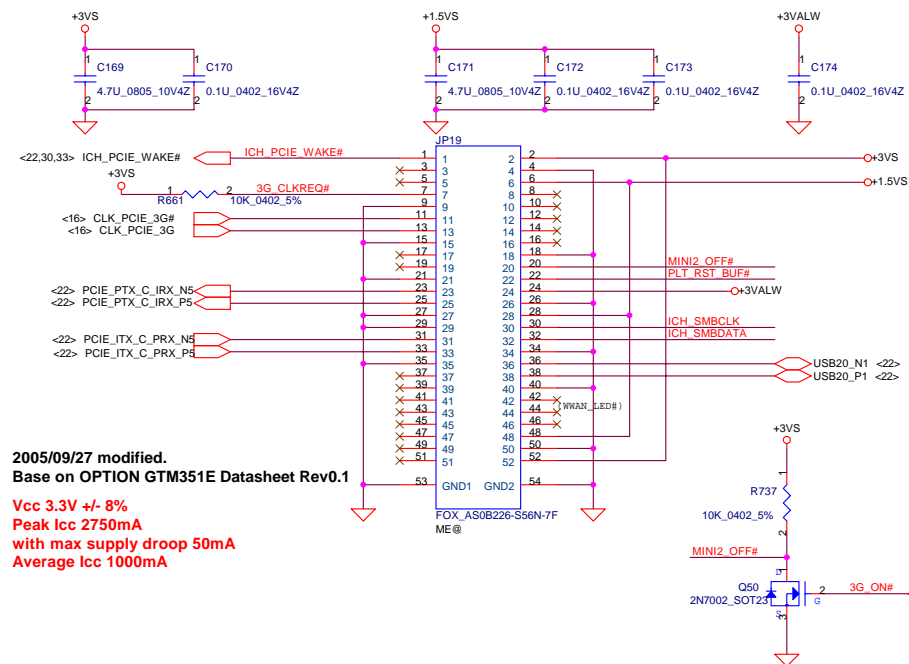
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Size				Document Number				XXXXX LA-3541P			
Date:				Wednesday, November 01, 2006				Sheet 30 of 52			
								Rev 0.1			



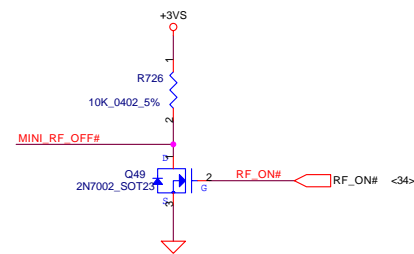
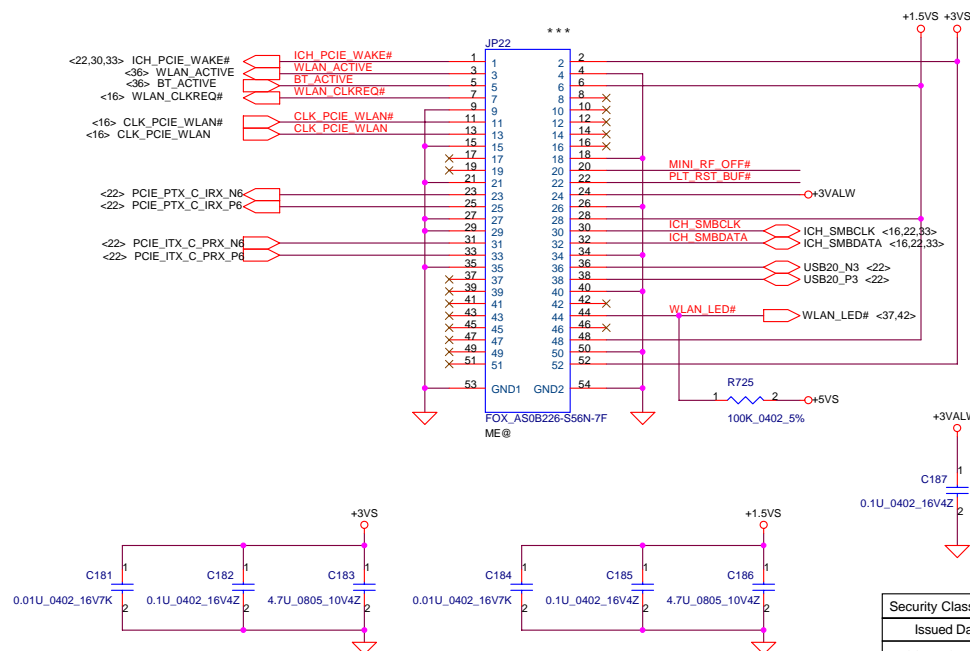
NAND mini Card(Robson support)



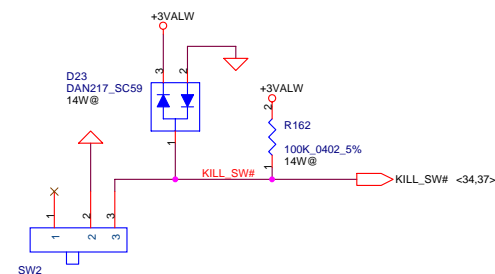
Mini-Express Card for 3G Or TV Tuner



Mini-Express Card for WLAN

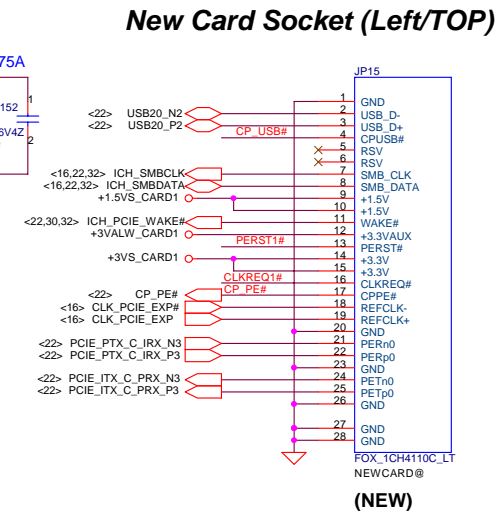
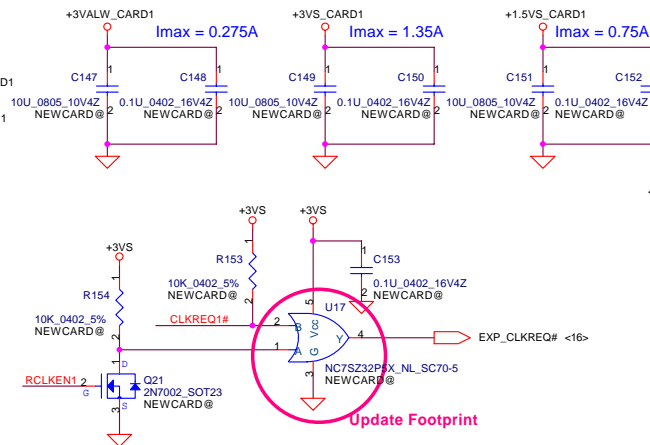
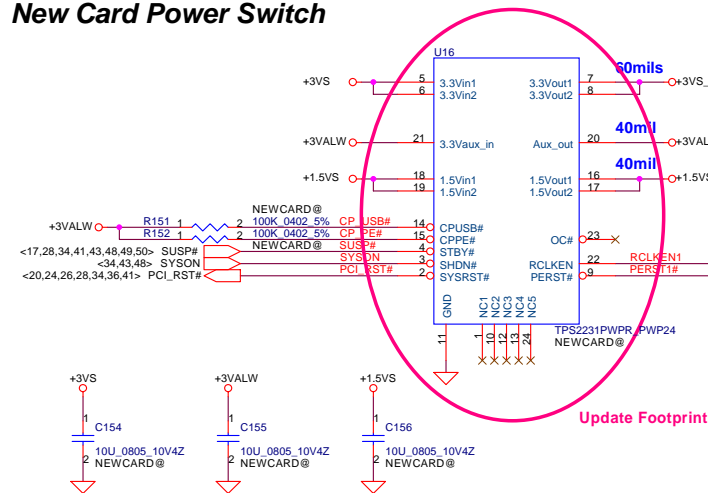
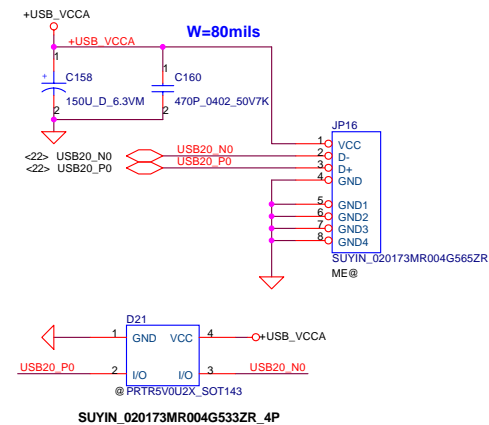


Kill SWITCH

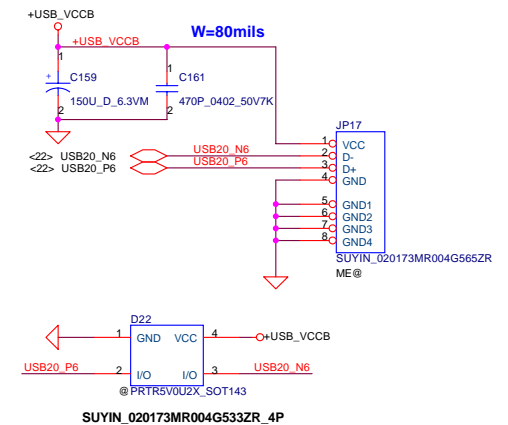


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New Card Power Switch

**USB CONN. 1**

USB CONN. 2

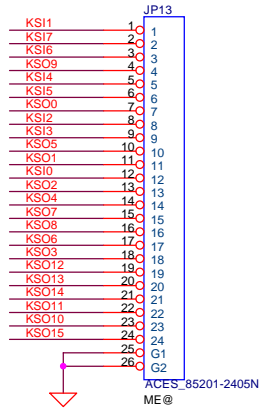


9/17 modified this block

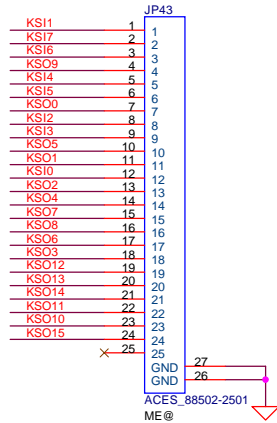
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				NEW CARD & USB Connector				
				Size B	Document Number		Rev 0	
				ITFTX M/B LA-3541P Schematic				
Date:				Wednesday, November 01, 2006		Sheet 33 of 52		

INT_KBD Conn.

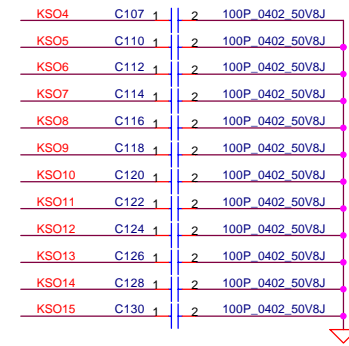
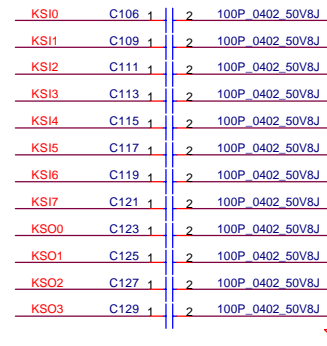
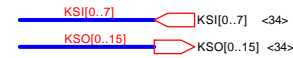
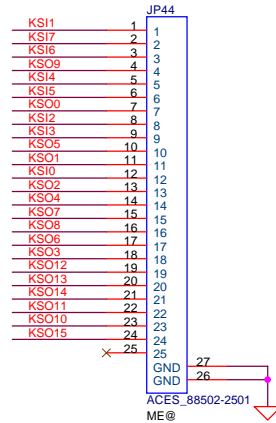
For IFT10



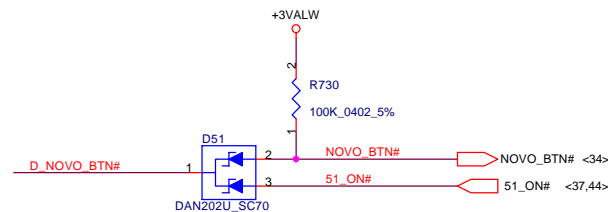
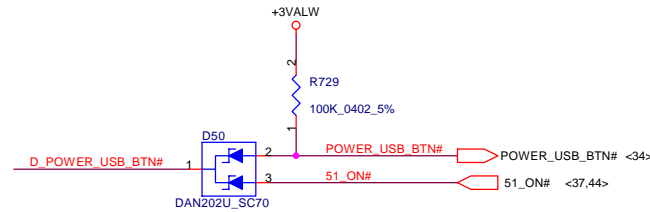
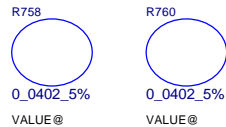
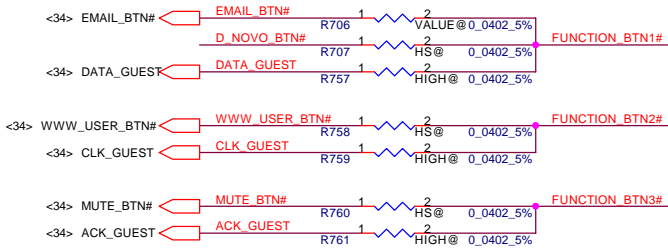
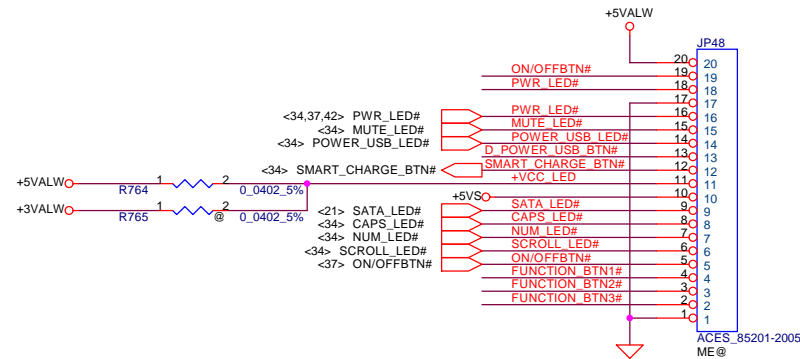
For IFL90



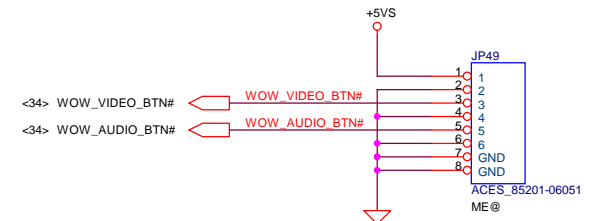
For IFT00



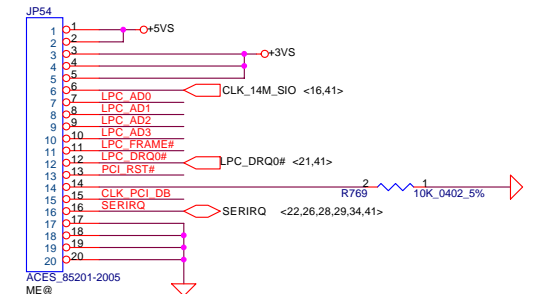
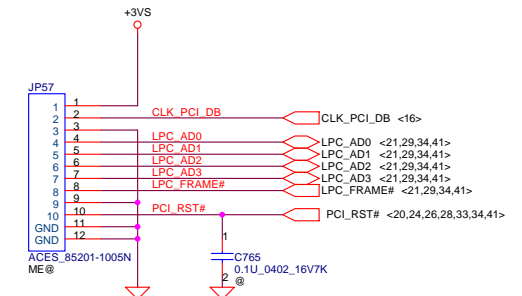
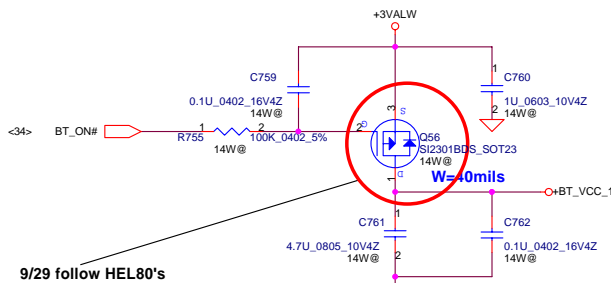
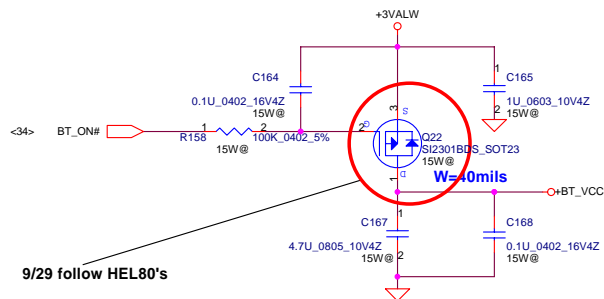
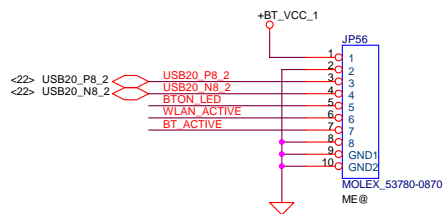
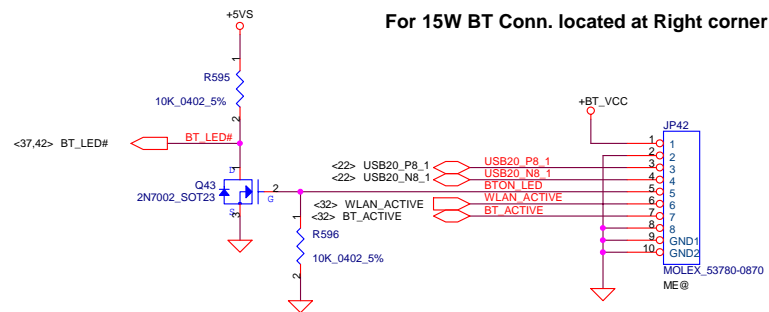
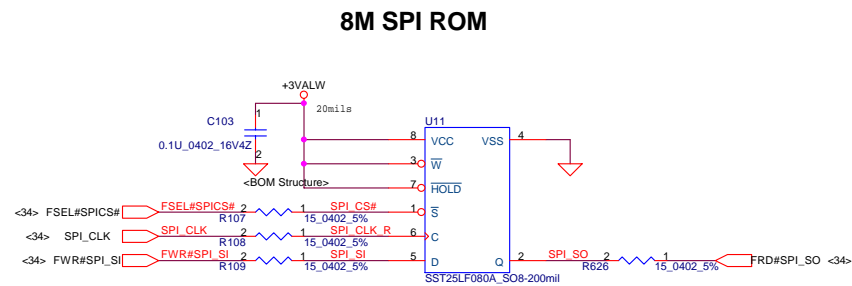
Switch Board Conn.



Video Switch Board Conn.

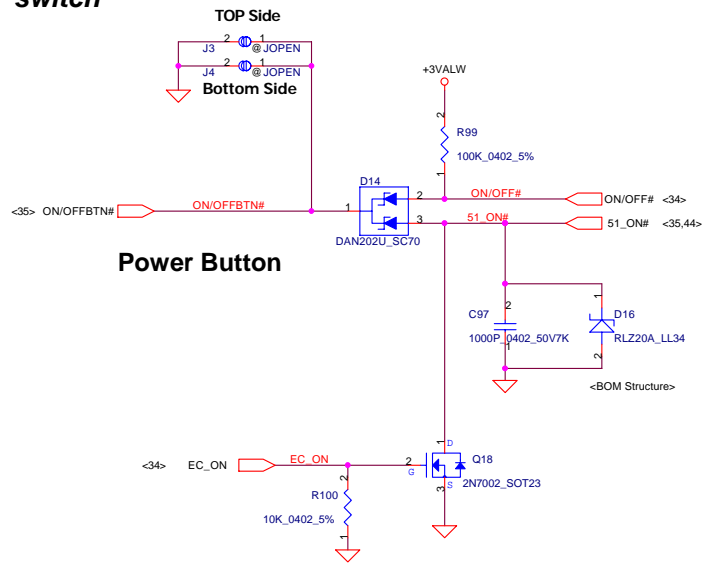


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Size	Document Number	IFTXX M/B LA-3541P Schematic		Rev	0
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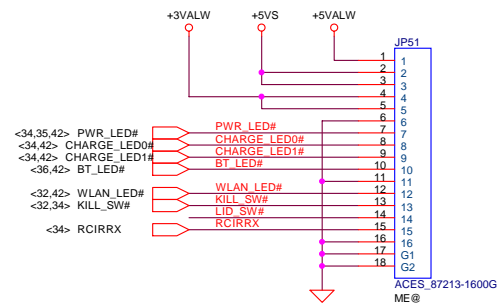
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	BIOS, I/O Port & K/B Connector	
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ON/OFF switch

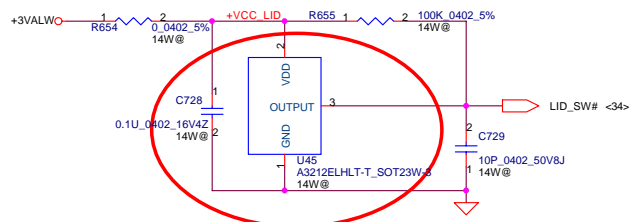


Power Button

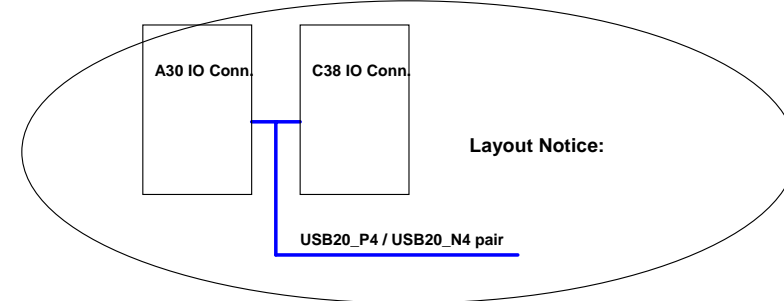
Front LED Board



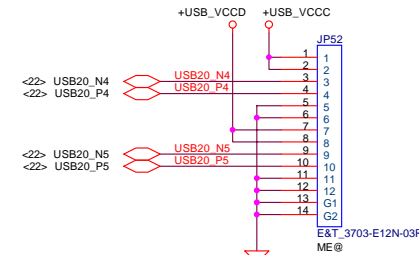
Lid Switch



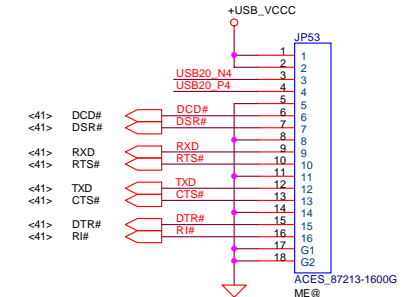
12/9 Change to SA032120010



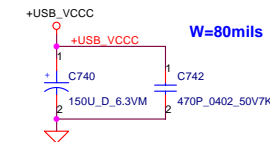
For A30 IO Conn.



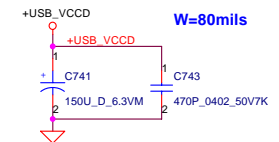
For C38 IO Conn.



To USB CONN. 3

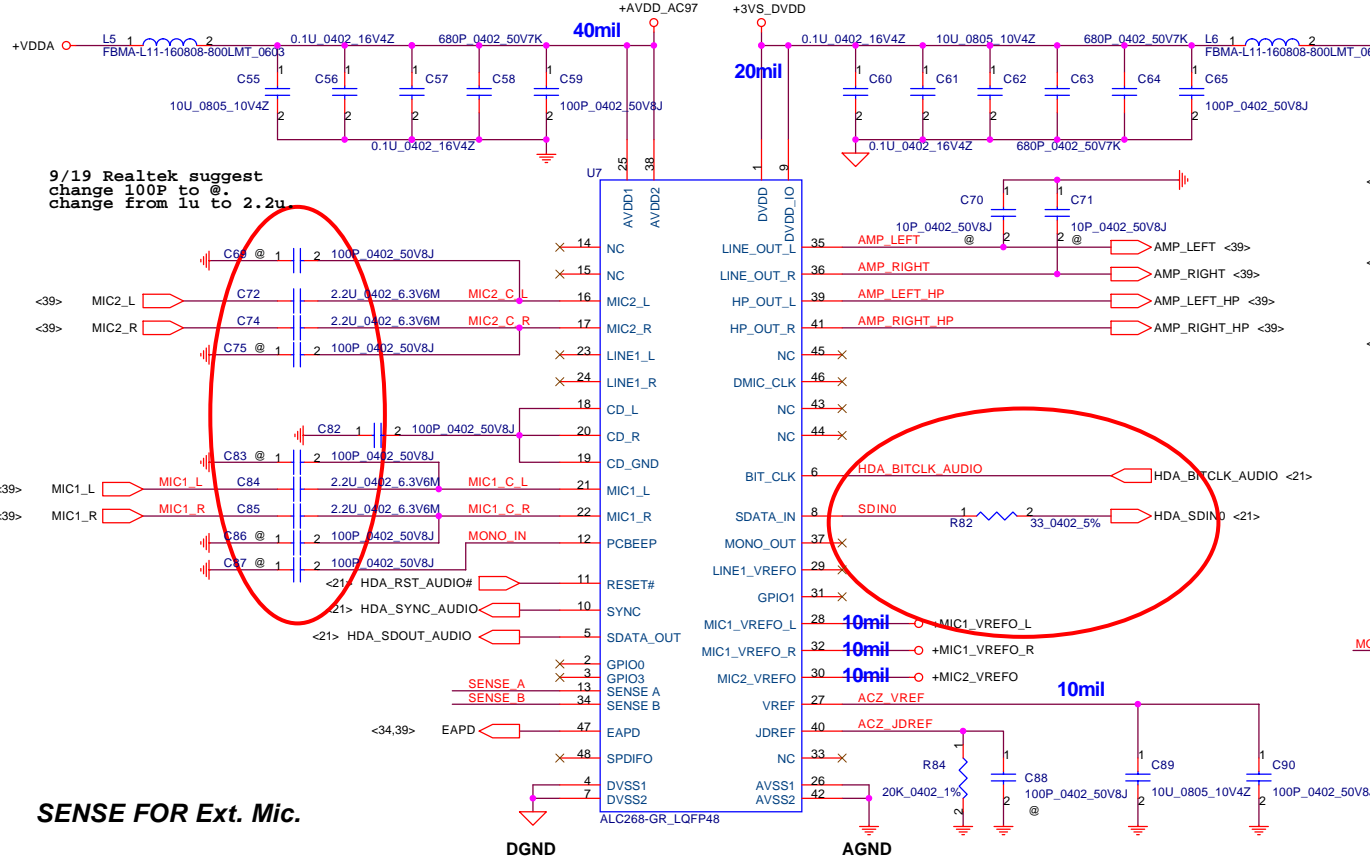


To USB CONN. 4



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Size	B	Document Number	IFTXX MB LA-3541P Schematic		Rev
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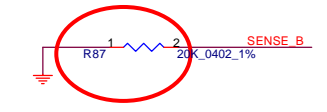
HD Audio Codec



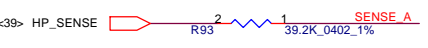
9/19 Realtek suggest
change 100P to @.
change from 1u to 2.2u

SENSE FOR Ext. Mic.

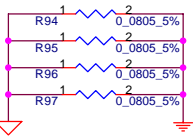
SENSE FOR Solo Int. Mic.



SENSE FOR HP



Moat Bridge

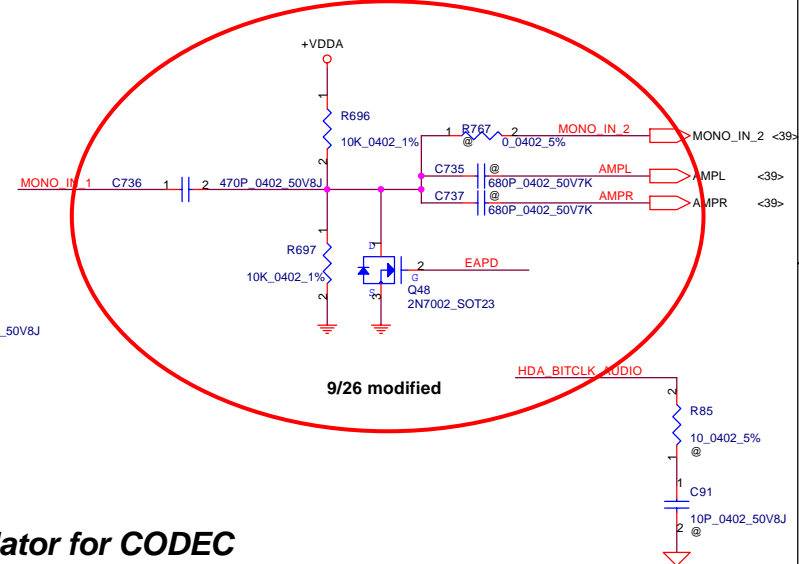
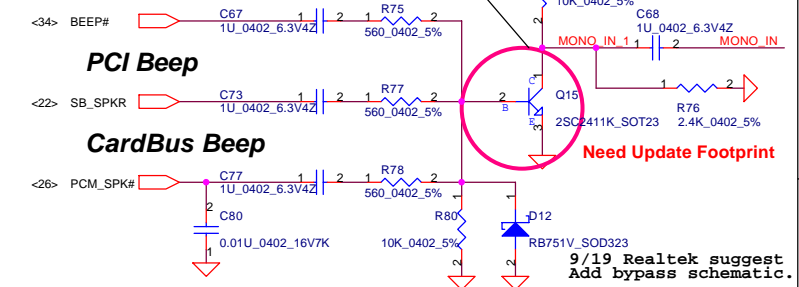


Sense Pin	Impedance	Codec Signals	Funnnction
SENSE A / B	39.2K	PORT-A (PIN 39, 41)	HP
	20K	PORT-B (PIN 21, 22)	MIC
	10K	PORT-C (PIN 23, 24)	LINE IN
	5.1K	PORT-D (PIN 35, 36)	LINE Out
SENSE B	39.2K	PORT-E (PIN 14, 15)	HP
	20K	PORT-F (PIN 16, 17)	MIC
	10K	PORT-G (PIN 43, 44)	LINE IN
	5.1K	PORT-H (PIN 45, 46)	LINE Out

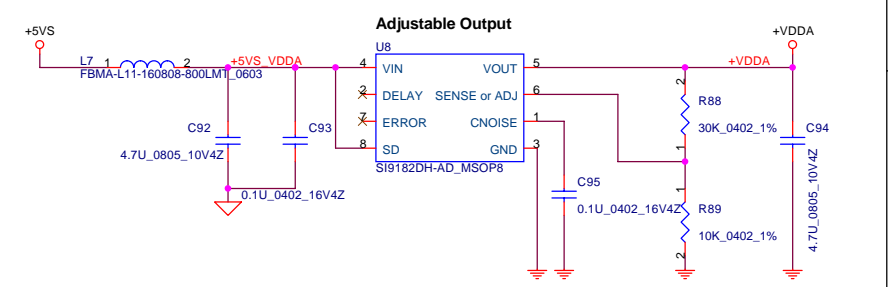
EC Beep

PCI Beep

CardBus Beep

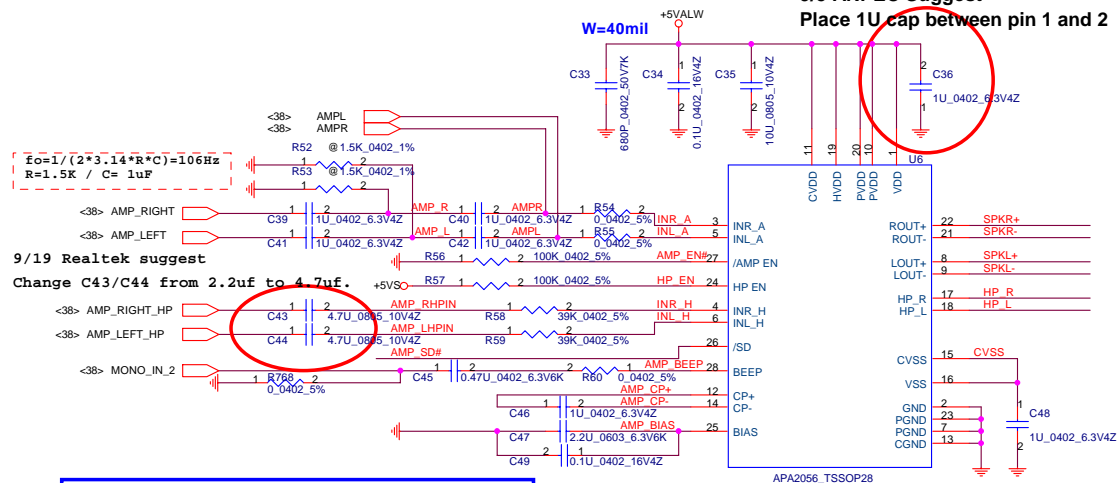


Regulator for CODEC



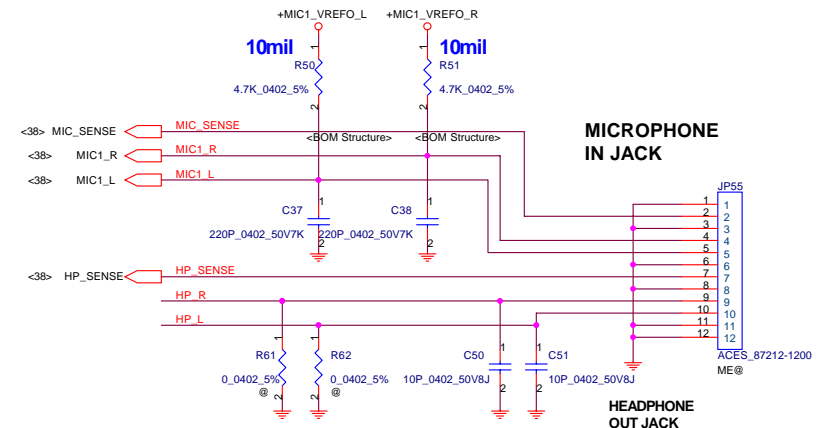
APA2056 SPK/HP Amplifier

9/5 ANPEC Suggest
Place 1U cap between pin 1 and 2

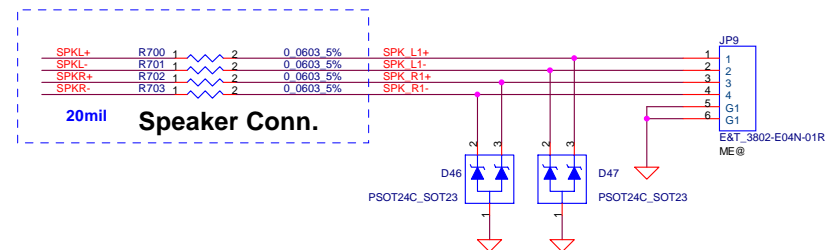
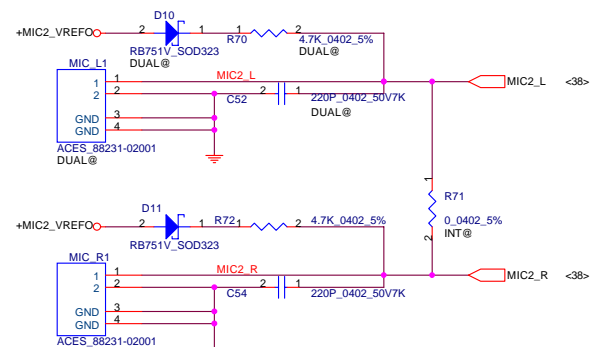


9/5 If implement AMP BEEP, Swap C155 and R79.
R79 change from 0 Ohm to 47K

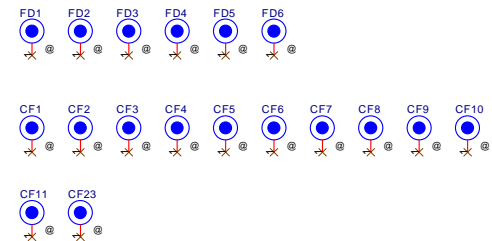
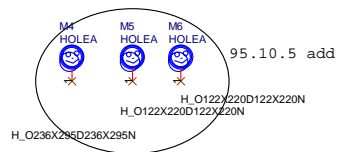
IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)



SINGLE INT MIC/DUAL INT MIC

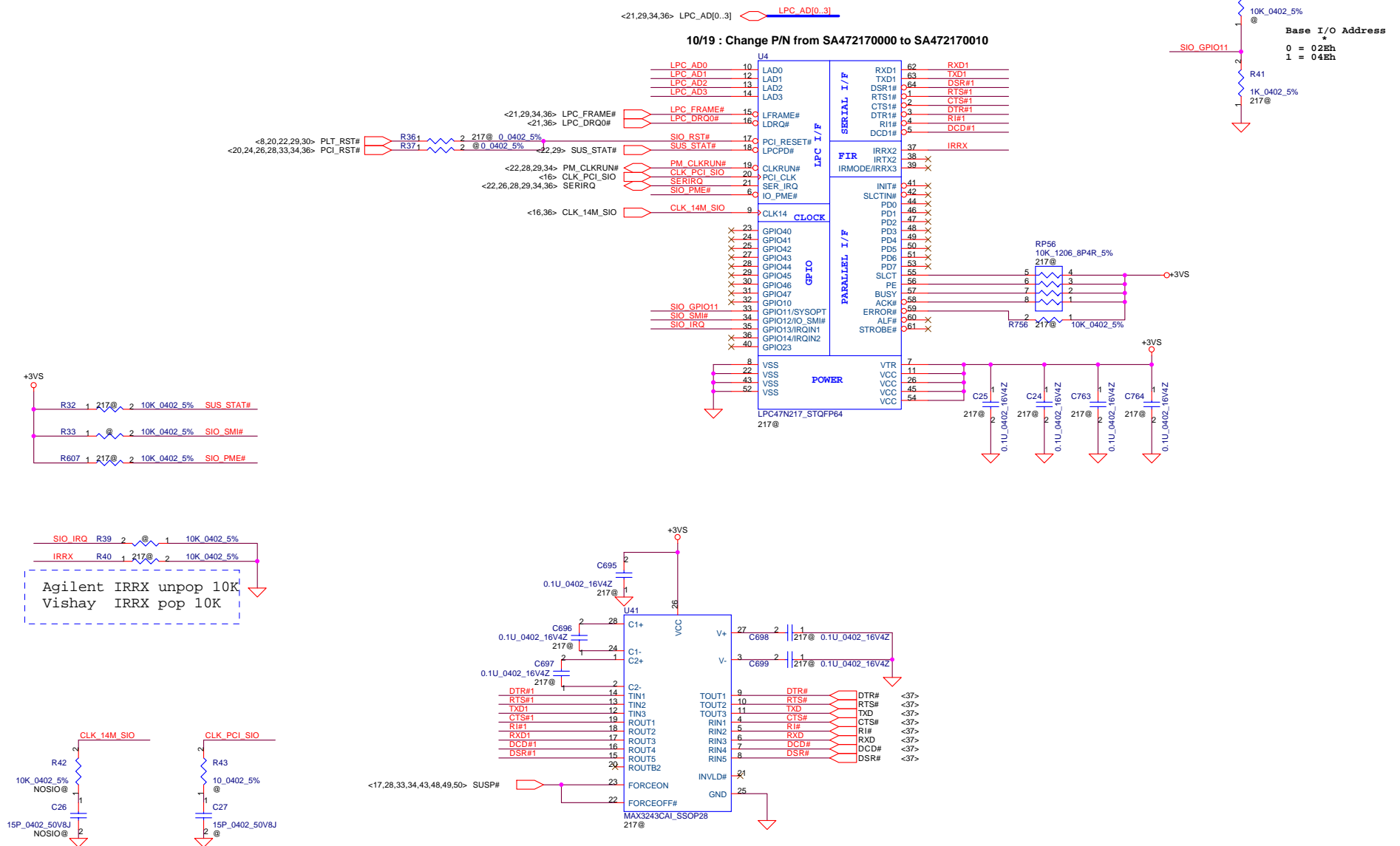


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Size	Document Number	Customer	Rev	
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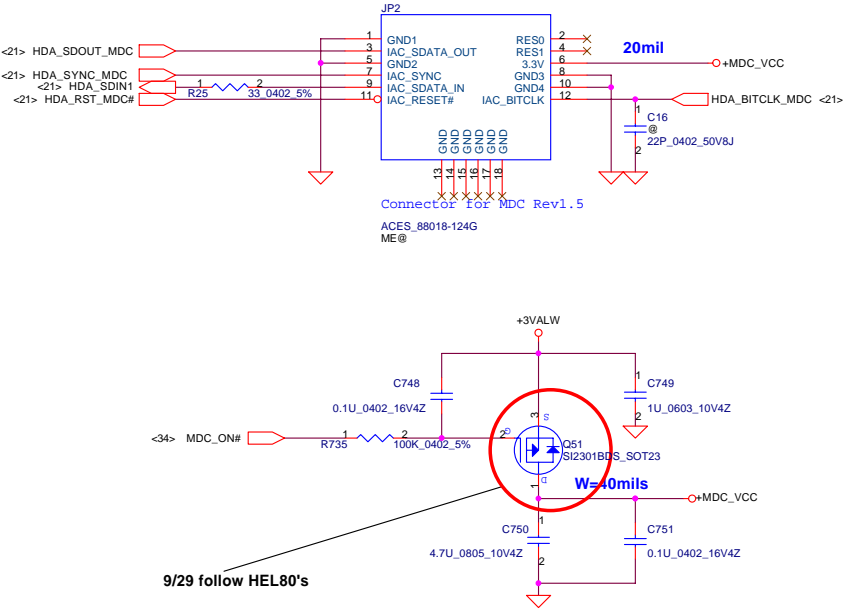


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Size	B	Document Number	IFTXX MB LA-3541P Schematic		Rev
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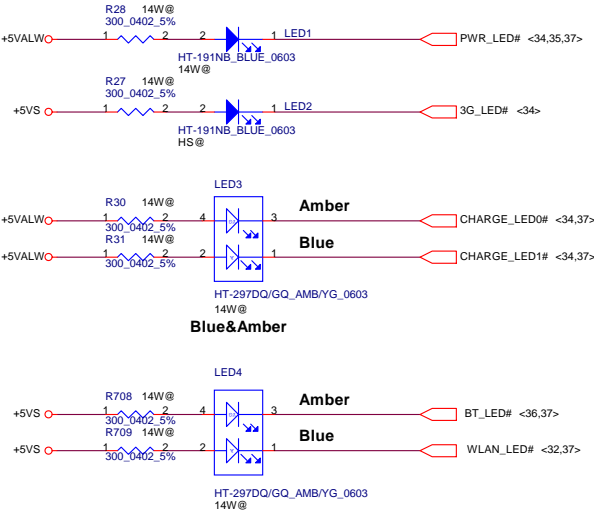
SUPER I/O SMsC LPC47N217



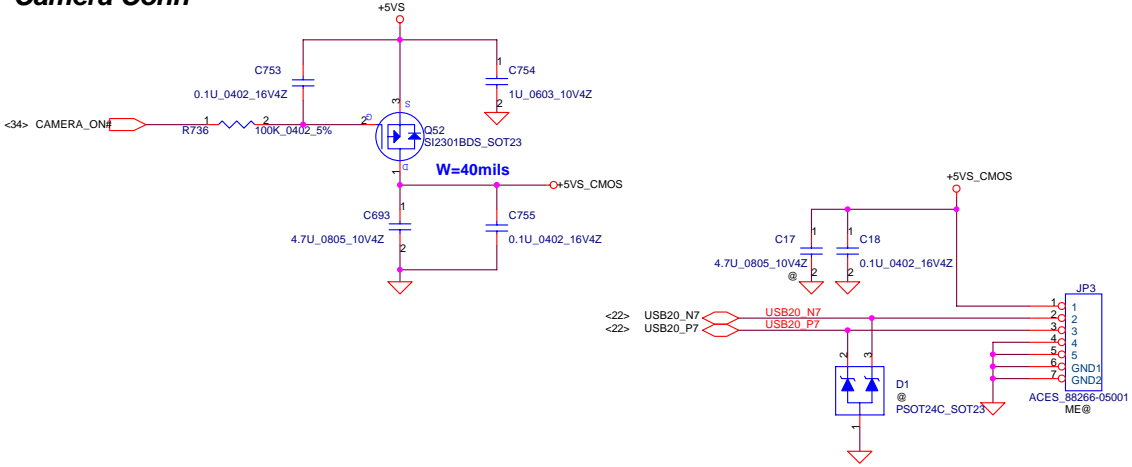
MDC Conn.



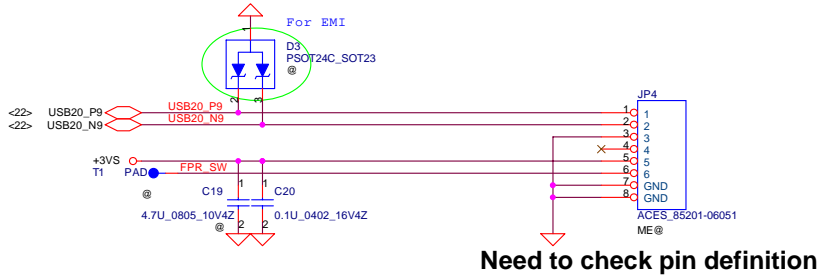
LED



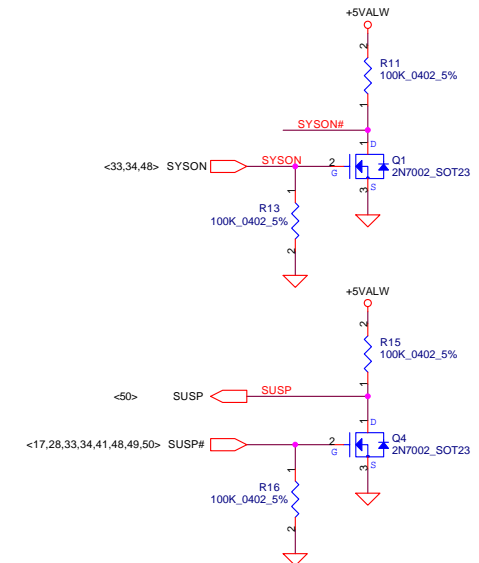
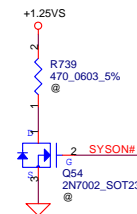
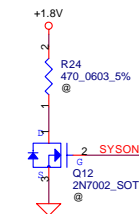
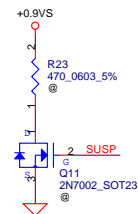
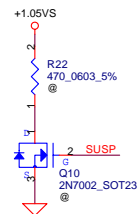
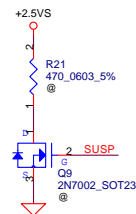
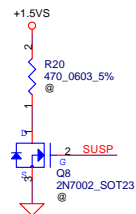
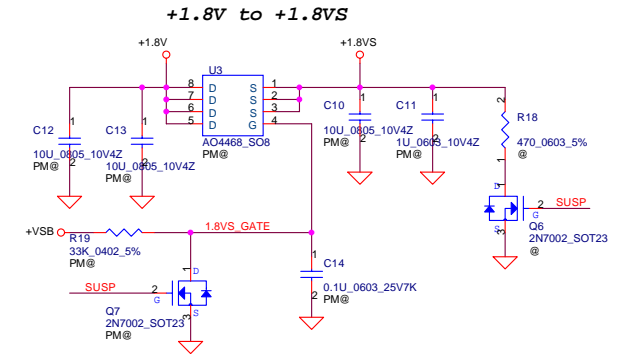
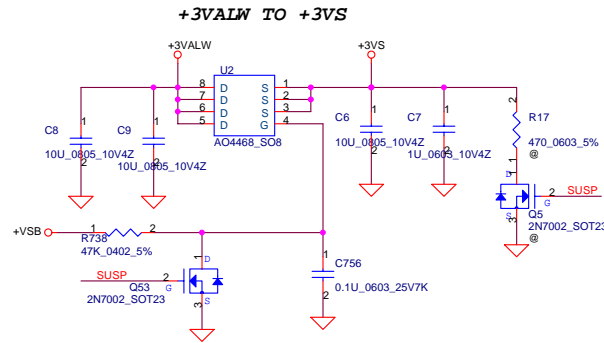
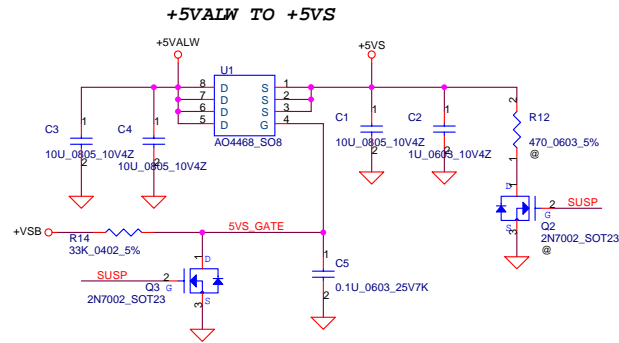
Camera Conn



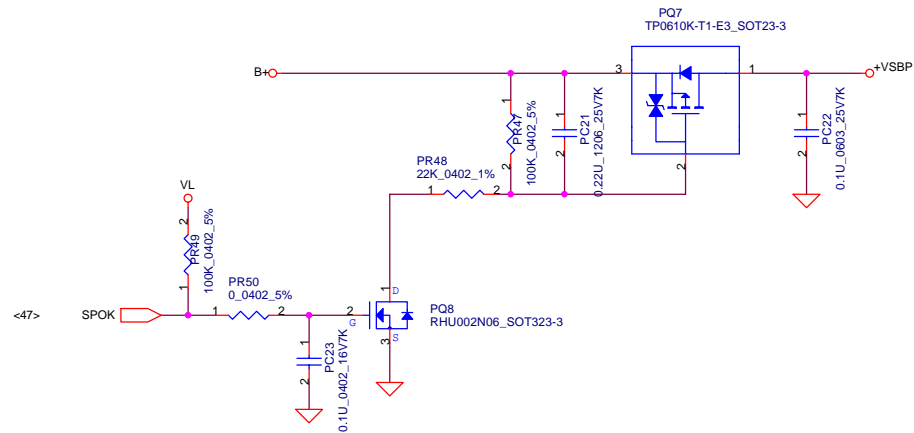
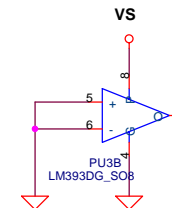
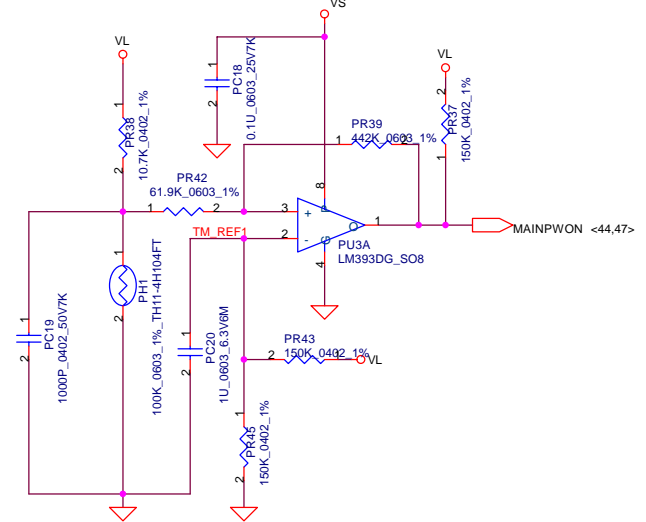
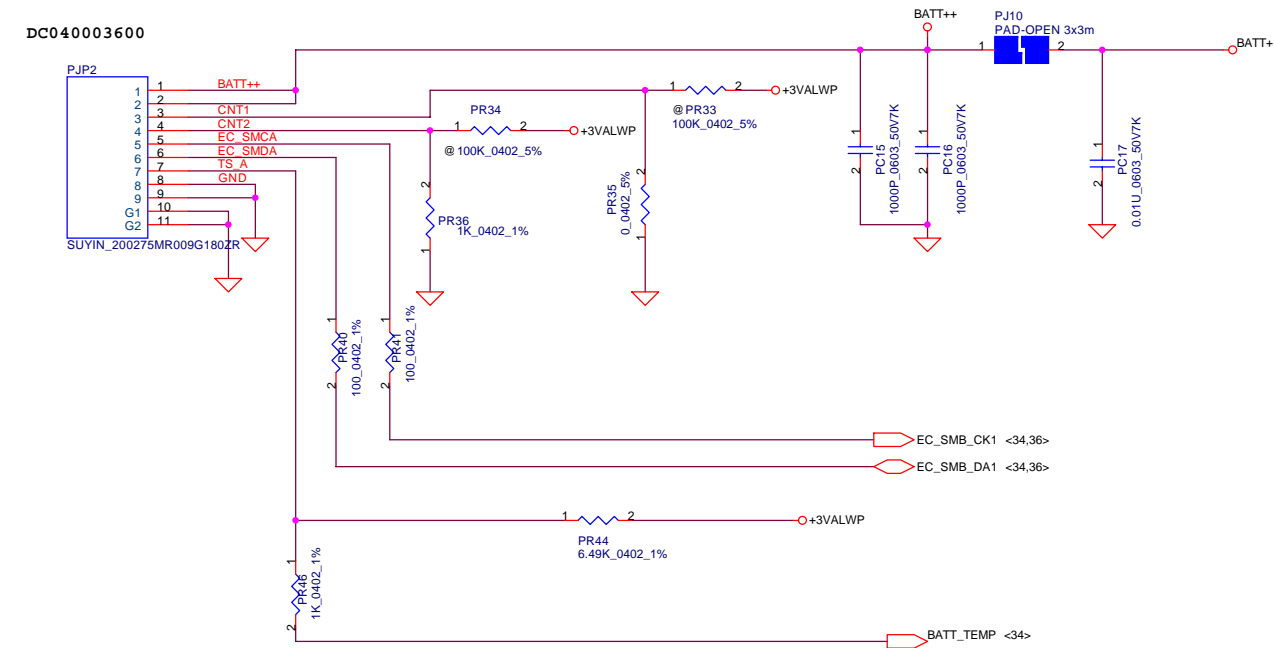
Finger Print board



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								MDC/CIR & LED			
								Size		Document Number	
								B		IFTXX M/B LA-3541P Schematic	
								Date:		Wednesday, November 01, 2006	
								Sheet		42 of 52	

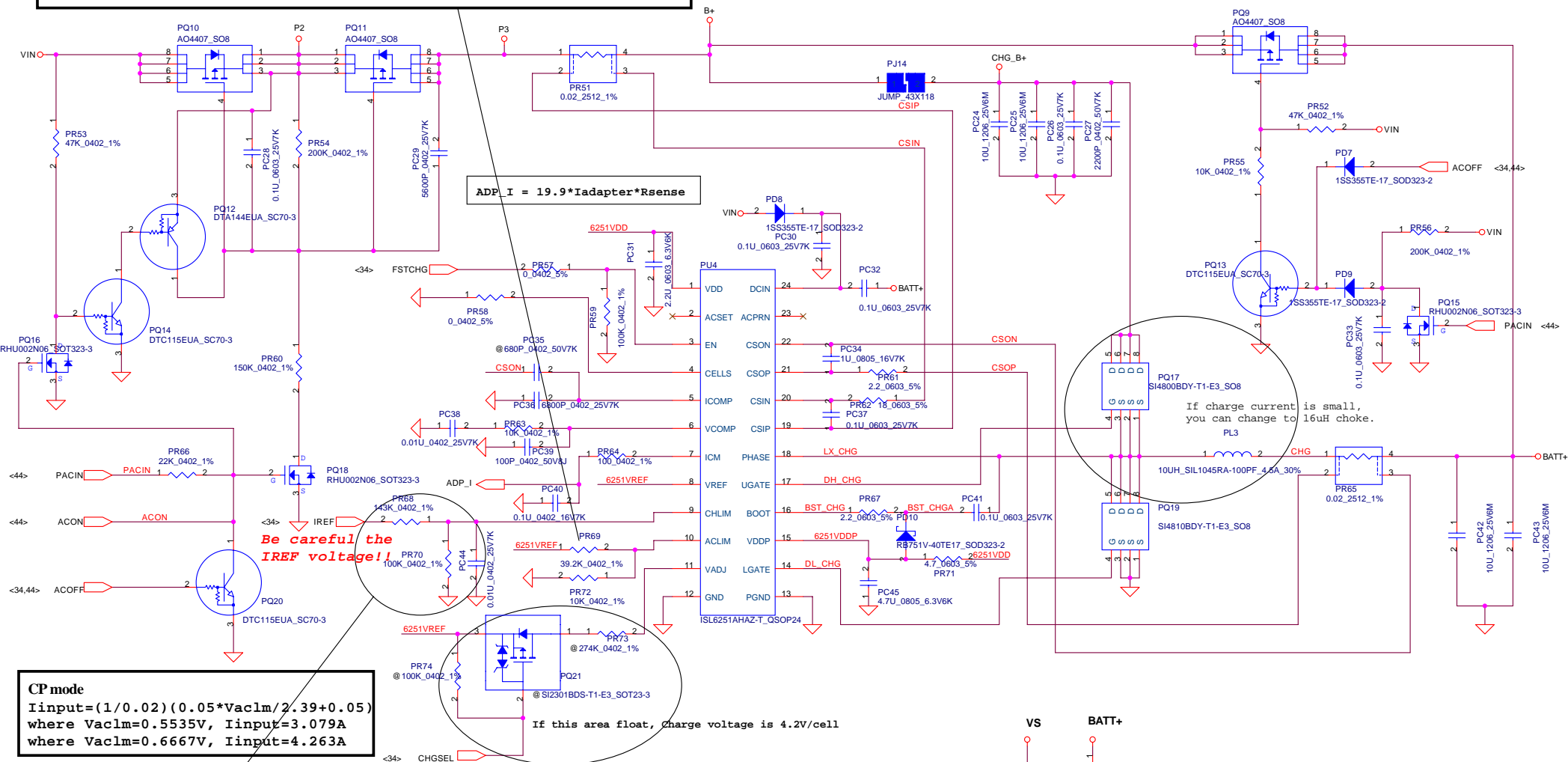


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Size B	Document Number	Date: Wednesday, November 01, 2006		Sheet 45 of 52	Rev 0.1

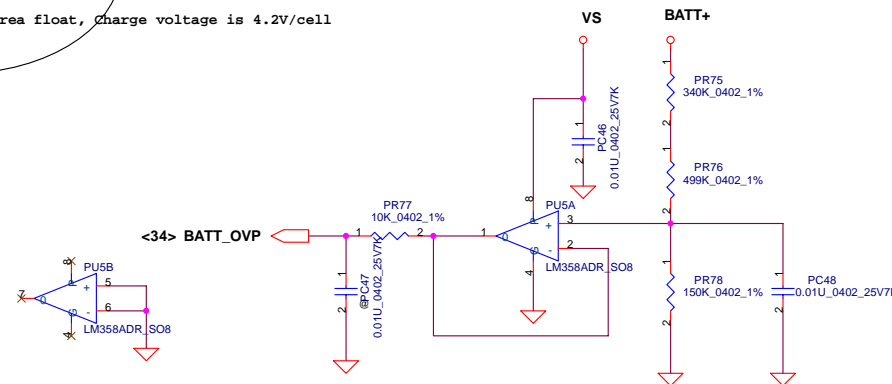
65W, Iadapter=0~3.42A, Current sense=0.02ohm, PR69=39.2K, CP=3.079A
90W, Iadapter=0~4.74A, Current Sense=0.015ohm, PR69=28.7K, CP=4.263A



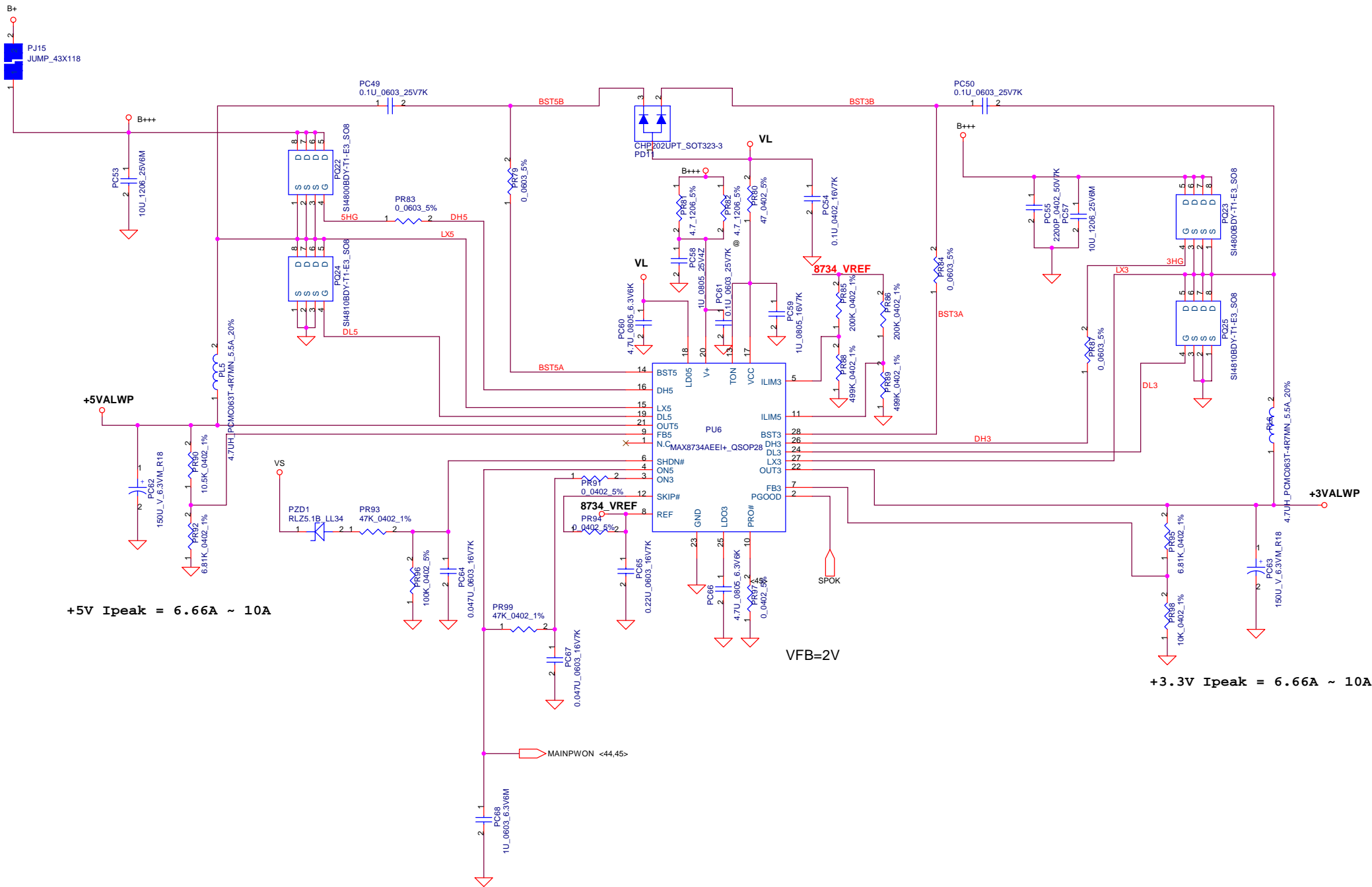
CP mode
 $I_{input} = (1/0.02)(0.05 \cdot V_{ac1m}/2.39 + 0.05)$
 where $V_{ac1m} = 0.5535V$, $I_{input} = 3.079A$
 where $V_{ac1m} = 0.6667V$, $I_{input} = 4.263A$

CC=0.6~3.4A
 $V_{CHLM} = 0.24V \sim 1.36V$
 $I_{REF} = 0.972 \cdot I_{charge}$
 $I_{REF} = 0.5832V \sim 3.3V$

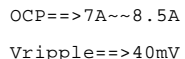
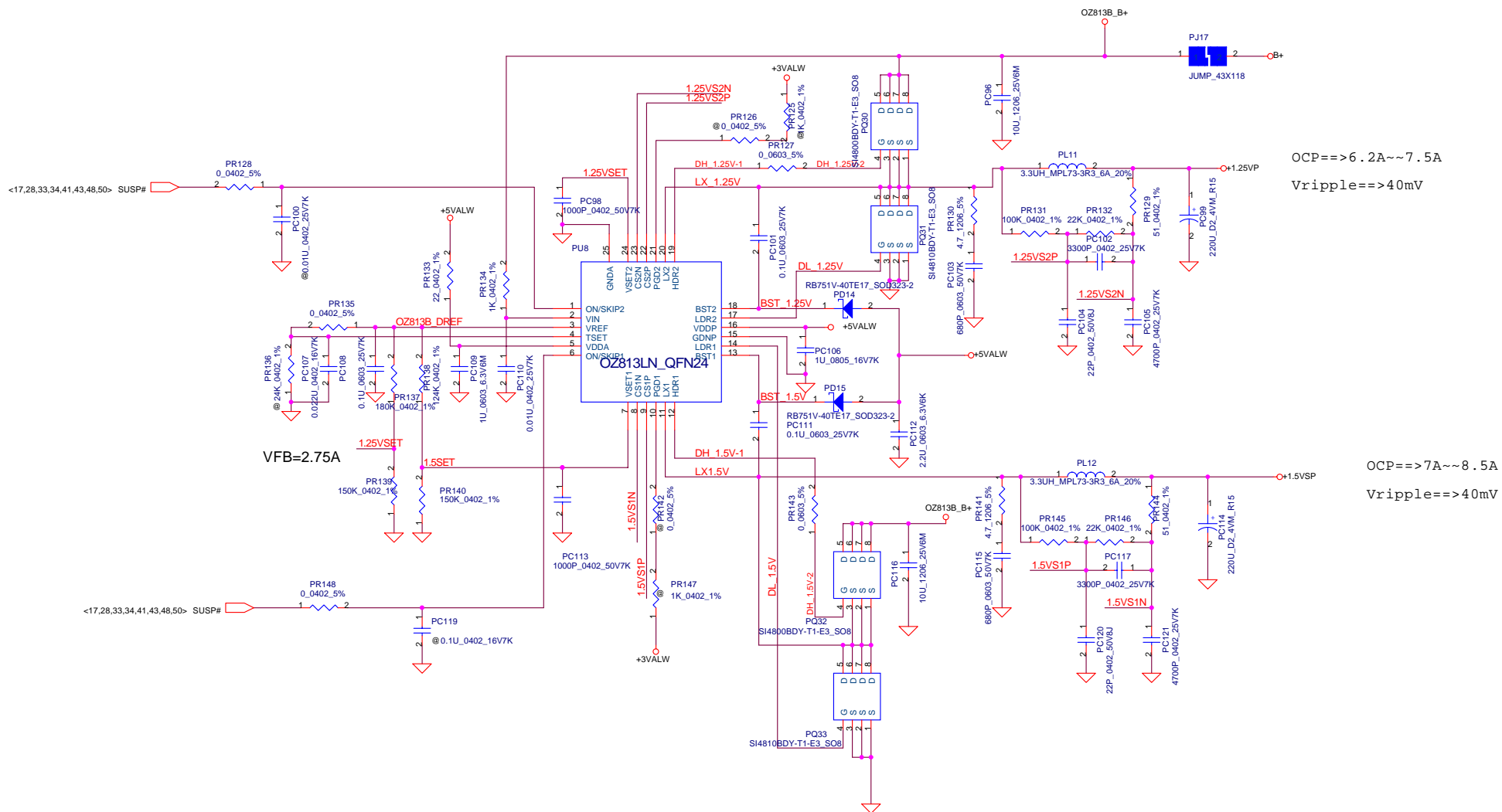
BATT Type	Charging Voltage (0x15)	CHGSEL	CV mode
2800mAH 3S pack	13050mV	LOW	12.90V
Normal 3S LI-ON Cells	12600mV	HIGH	12.60V



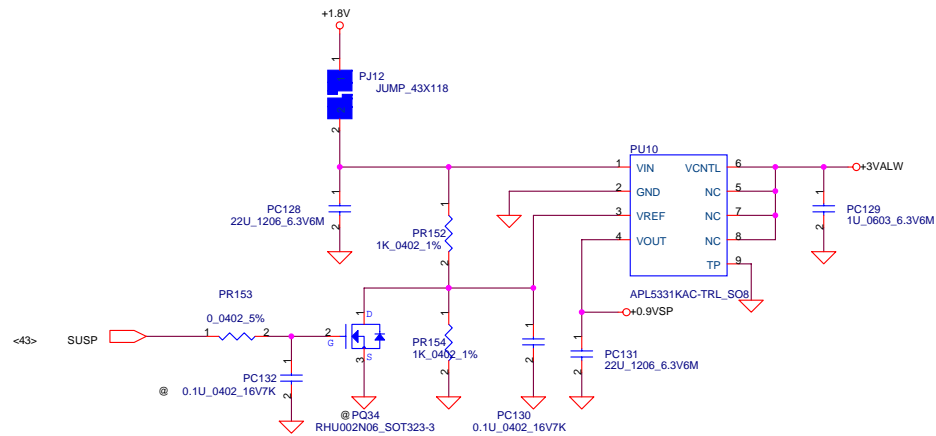
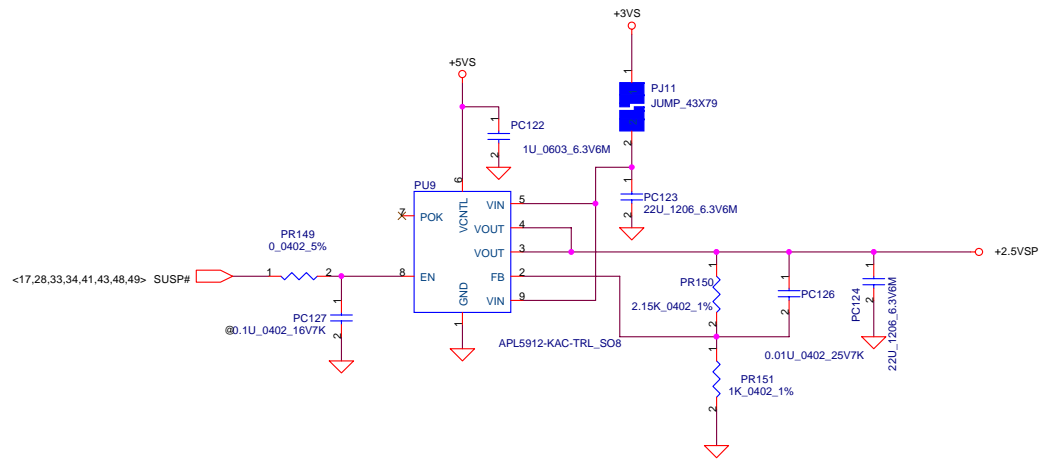
OVP voltage :
 $LI-3S : 13.50V \sim BATT-OVP = 1.5V$
 $BATT-OVP = 0.111 \cdot BATT+$



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