Model Name : VILE1 & VILE2
File Name : NM-A043, NM-A044
BOM P/N:

VILE1:

VILE2:

M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

GPU nVIDIA N14M-GL / N14P-GV2

2012-11-07

REV:0.1

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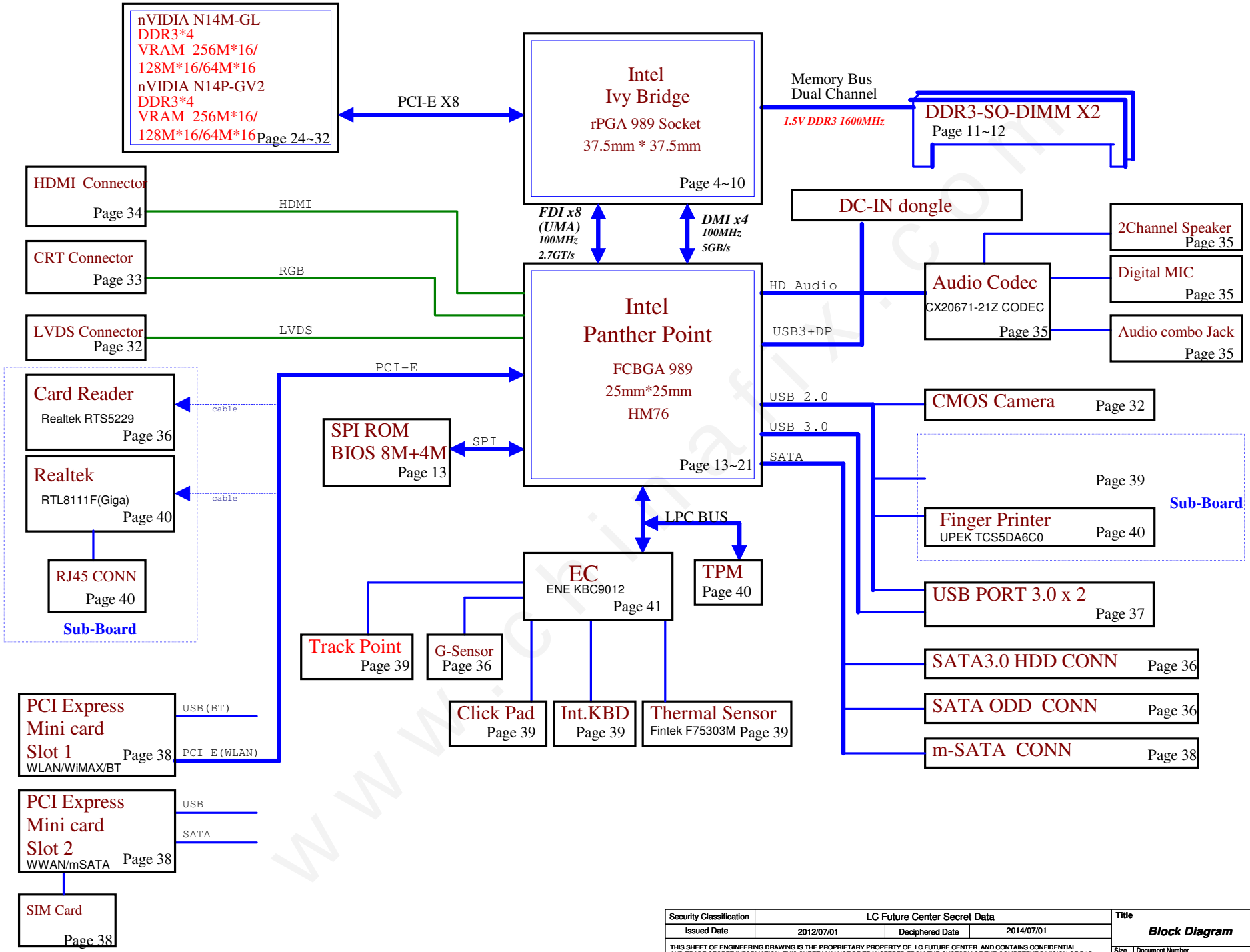

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Title: **Block Diagram**

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Voltage Rails

State \ power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS	+3VM +1.05VM
S0	O	O	O	O	O M3 Supported
S3	O	O	O	X	O M3 Supported
S5 S4/AC	O	O	X	X	O M3 Supported
S5 S4/ Battery only	X	X	X	X	
S5 S4/AC & Battery don't exist	X	X	X	X	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor Fintek F75303M	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	USB 3.0 Port (Left Side)
		1	
	UHCI1	2	USB 3.0 Port (Left Side)
		3	USB 3.0 Port
	UHCI2	4	Touch Panel
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	USB Port (Right Side)
	UHCI5	10	Mini Card(WLAN/BT)
		11	FPR
	UHCI6	12	Mini Card(WWAN)
		13	Camera

BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
45 LEVEL	45@
Unpop	@
NVidia	DIS@
PCH AUX Power	+3V_PCH@
Intel UMA	UMA@
VRAM Option	X76@
Intel SBA	SBA@
Intel AOAC	AOAC@
TPM	TPM@
GPU N14M-GL	N14MGL@
GPU N14P-GV2	N14PGV2@
SIM Card Slot	3G@
Touch Panel	Touch@
Finger Print Board	FP@
SSD	SSD@

SMBUS Control Table

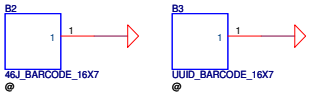
	SOURCE	VGA	BATT	KE9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

ZZZ5

DA PCB

DA80000TG00

NM-A043



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Title: Notes List

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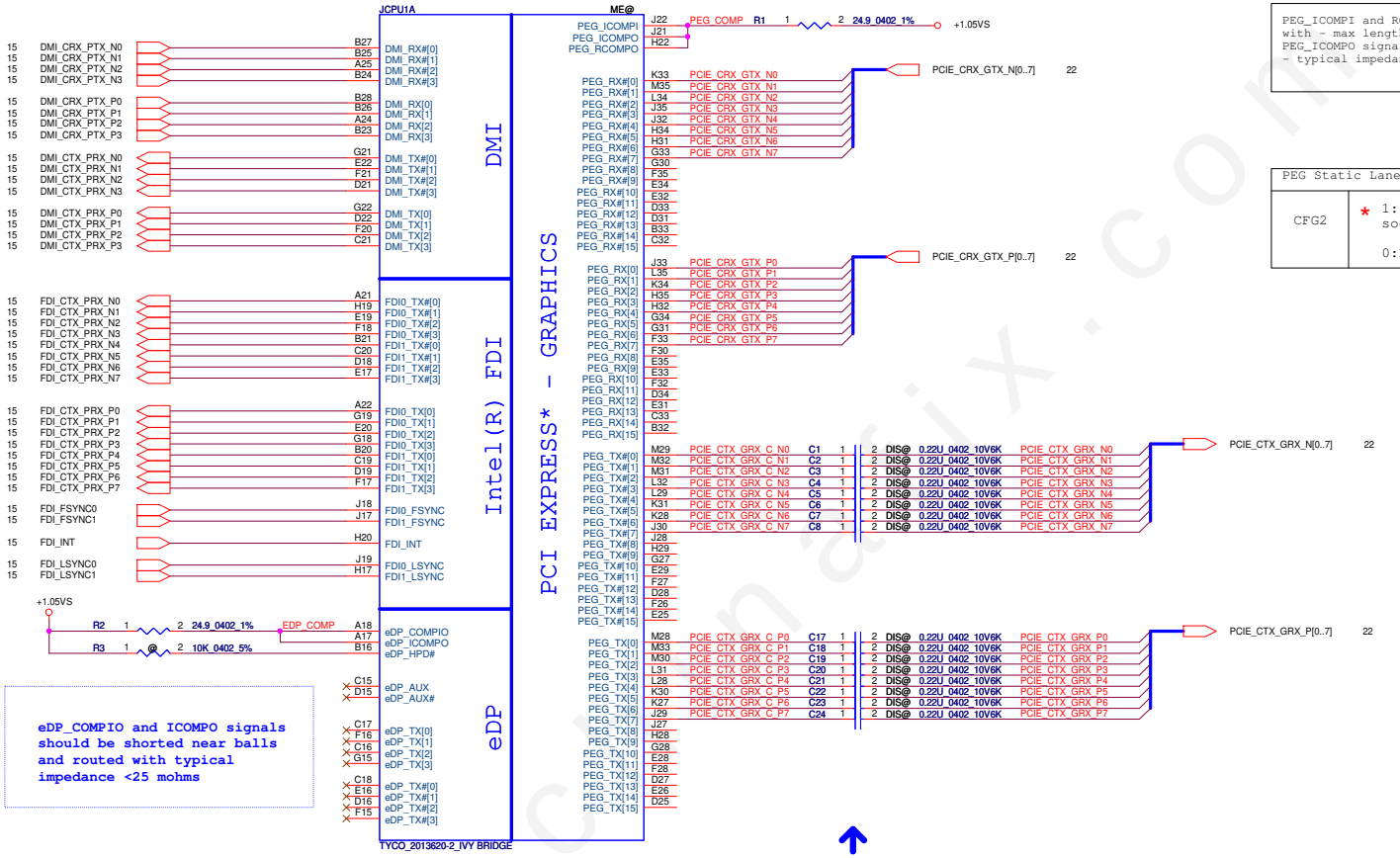

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

Nvidia support PCIE Gen2

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Title: PROCESSOR(1/7) DMI,FDI,PEG

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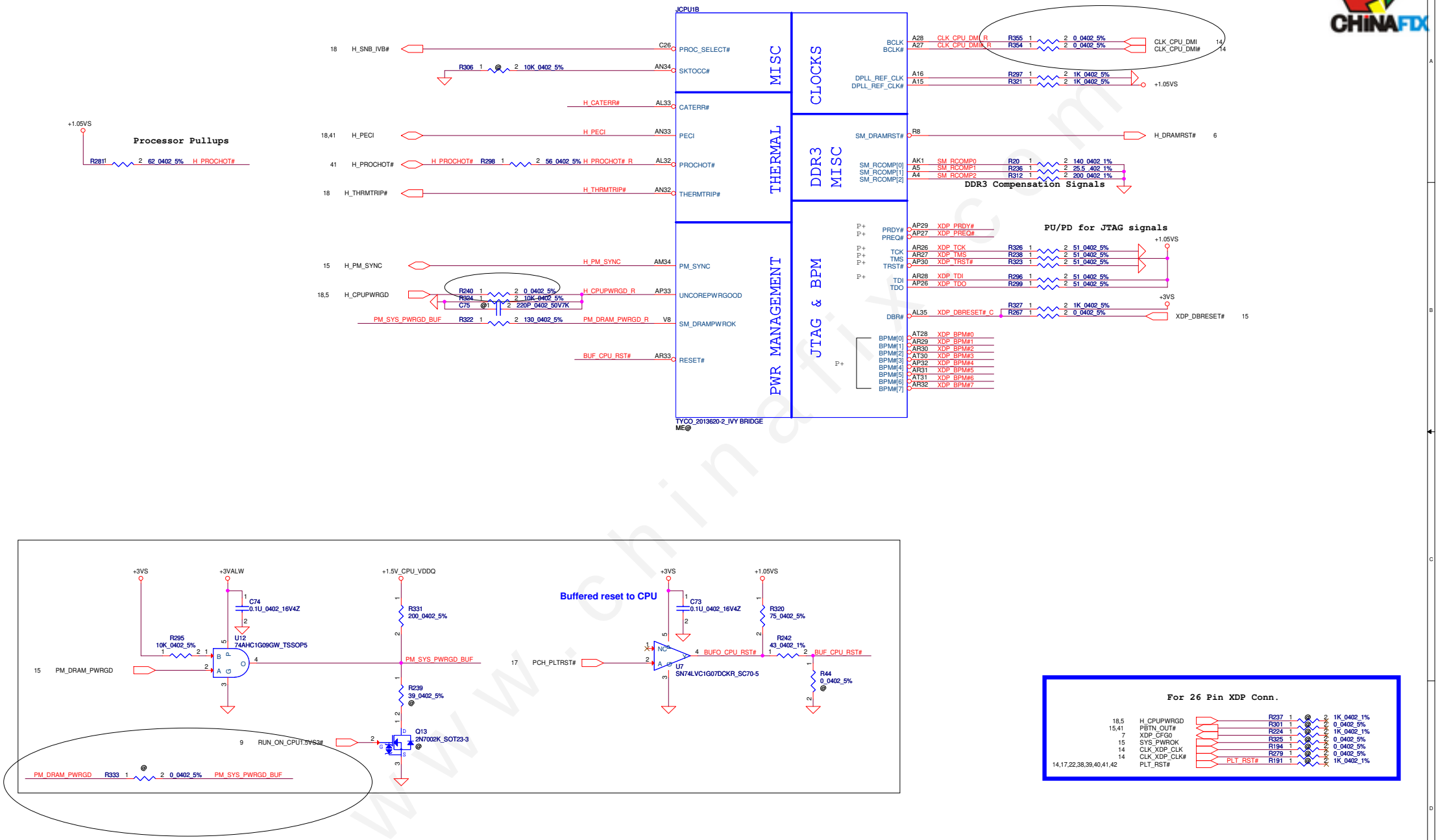

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Title: PROCESSOR(2/7) PM,XDP,CLK

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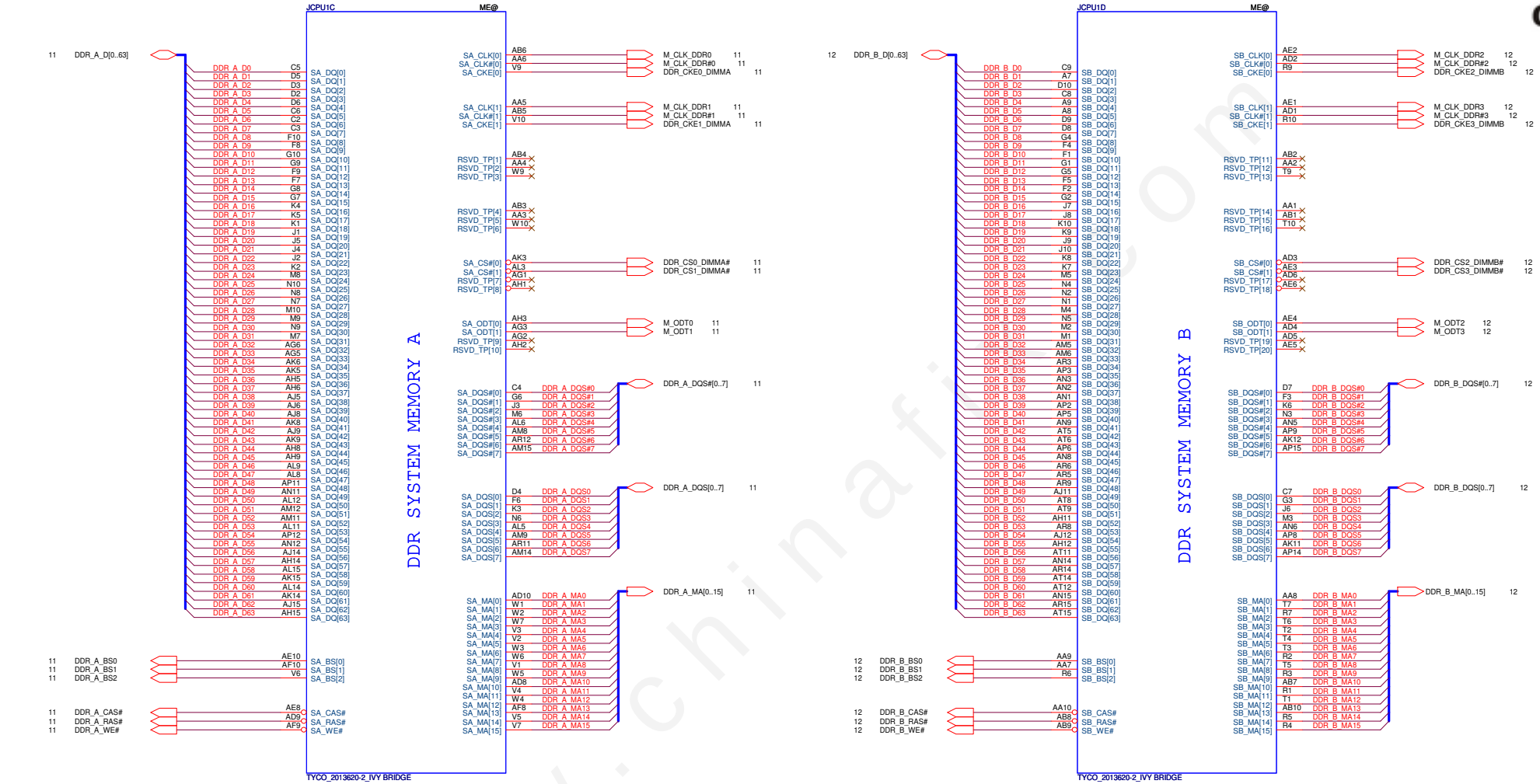

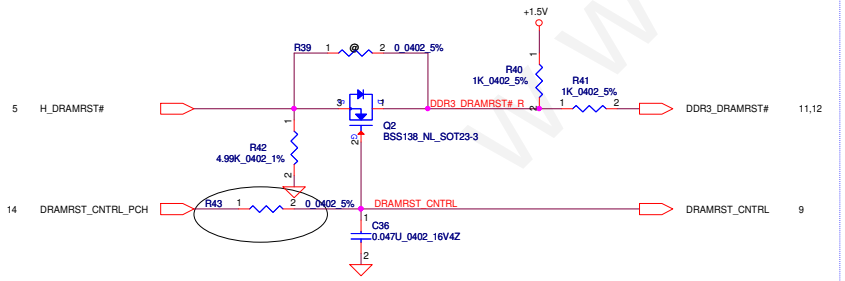

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Title: PROCESSOR(3/7) DDRIII

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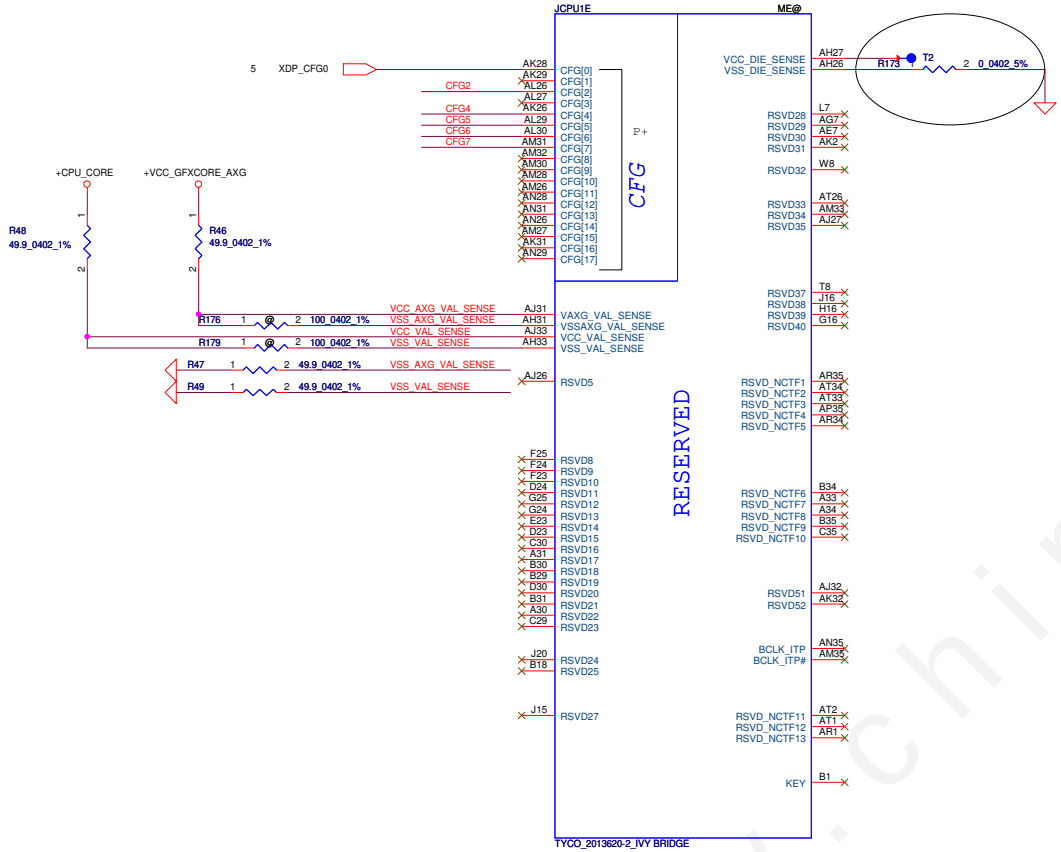
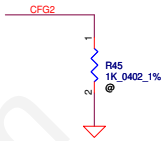
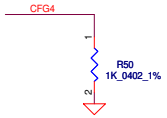


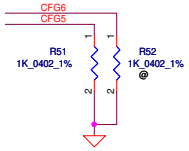
CFG Straps for Processor



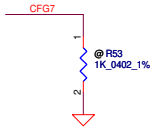
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled *10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG

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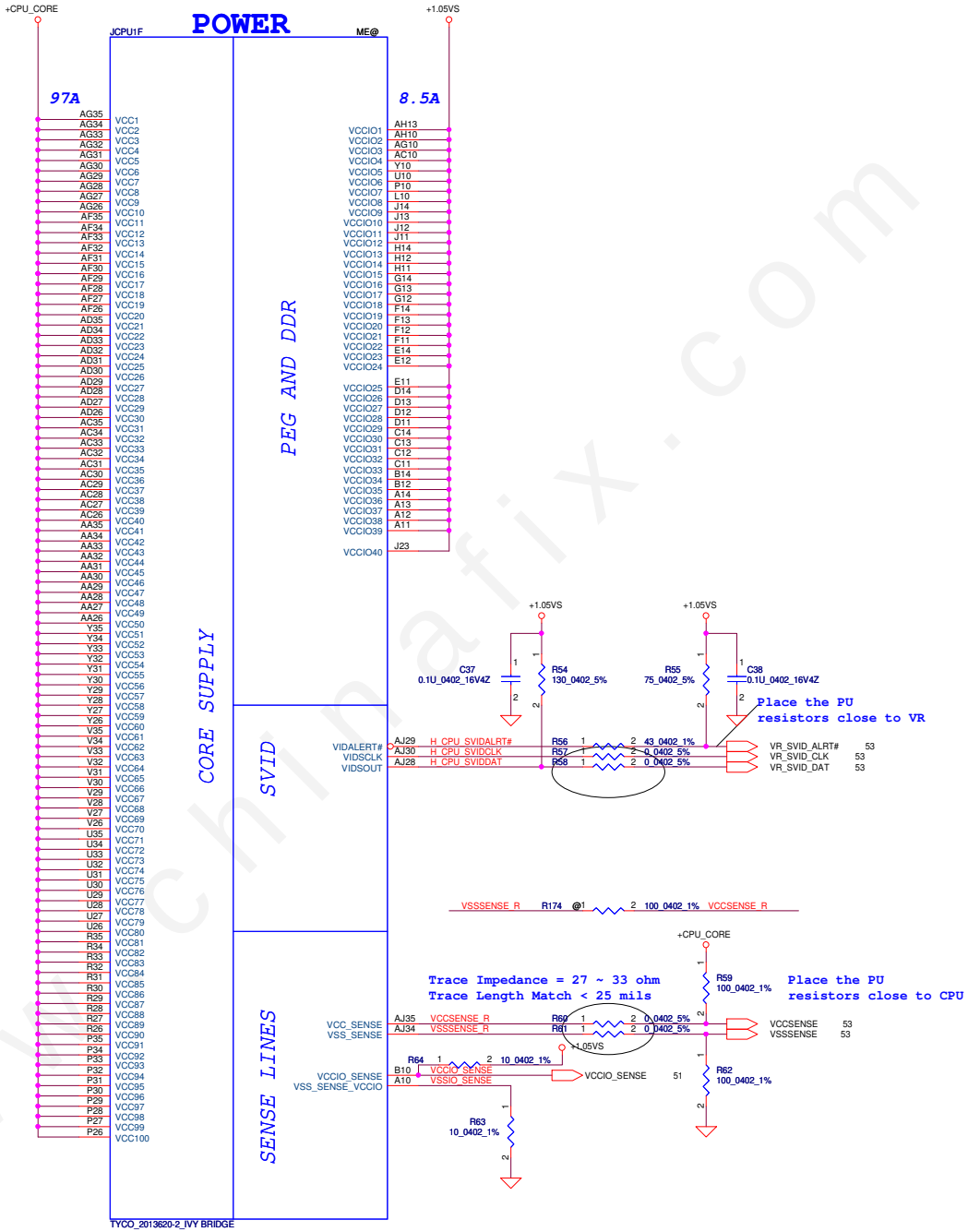

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Title: PROCESSOR(5/7) PWR,BYPASS

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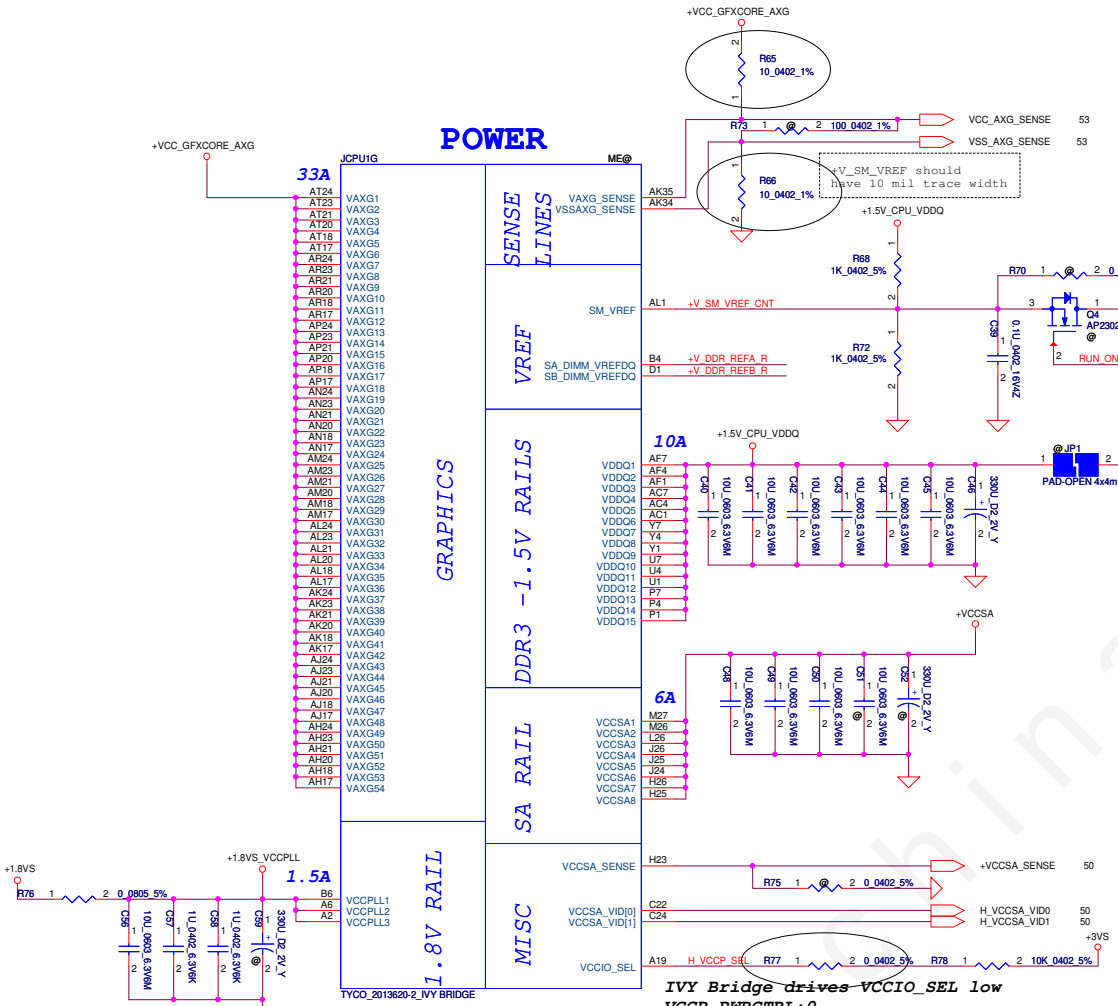
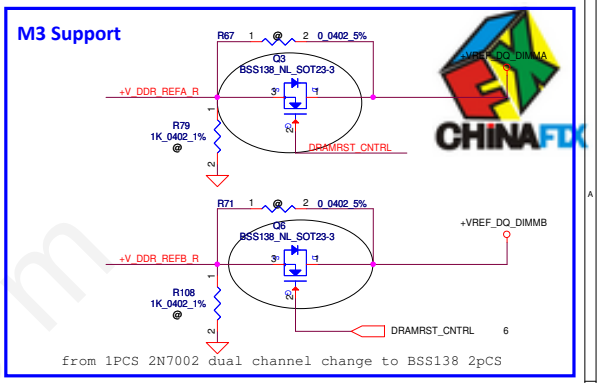
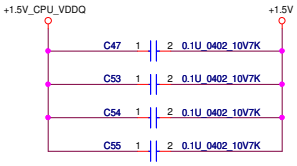


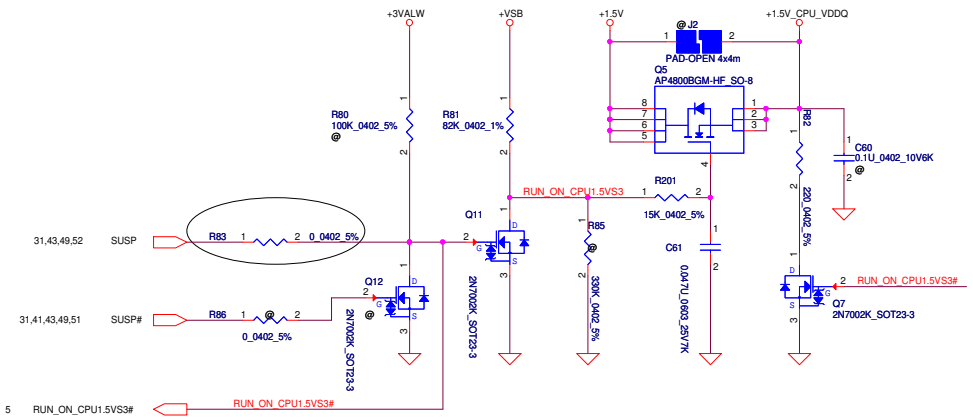
IVY Bridge drives VCCIO_SEL low
VCCP_PWRCTRL:0

Sandy Bridge is NC for A19
VCCP_PWRCTRL:1





+1.5V_CPU_VDDQ Source



Vaxg

- **Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,**
- **VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed**

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Title: ***PROCESSOR(6/7) PWR***

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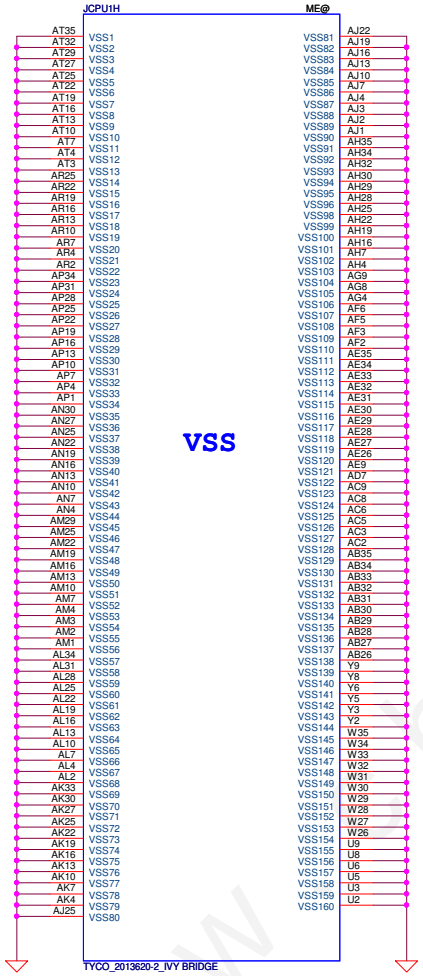

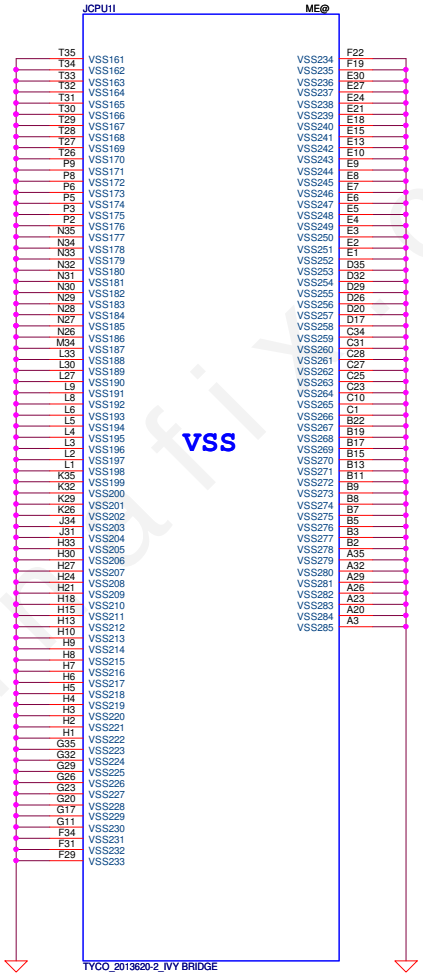

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Title: PROCESSOR(7/7) VSS

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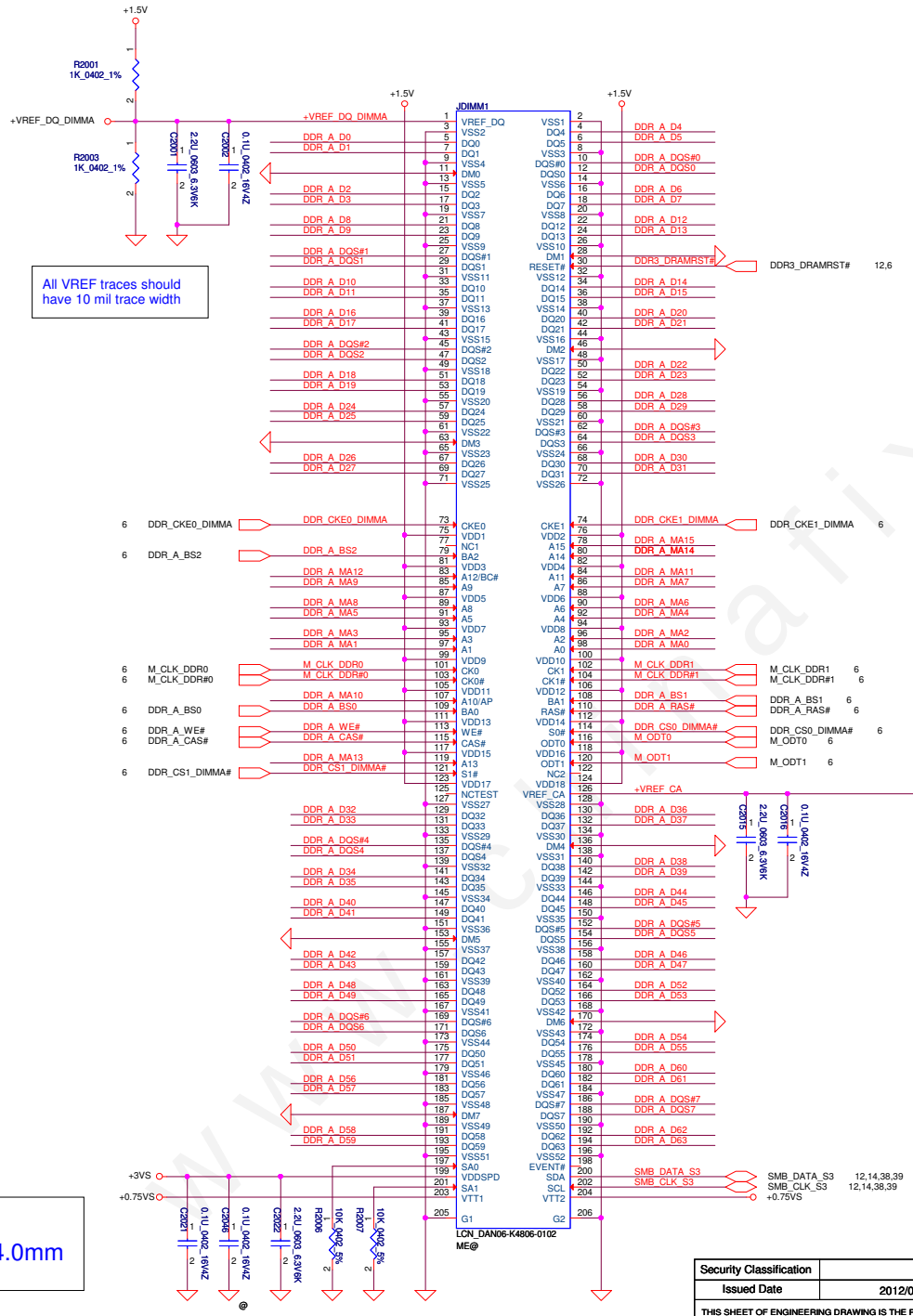

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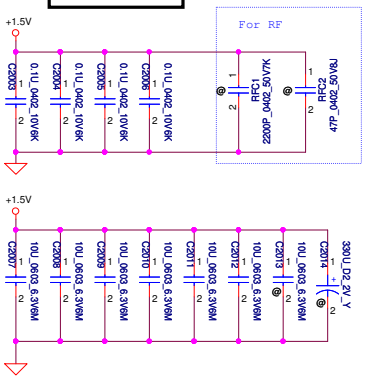

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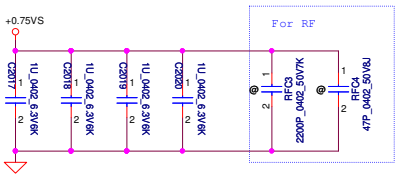

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Title: DDRIII DIMMA

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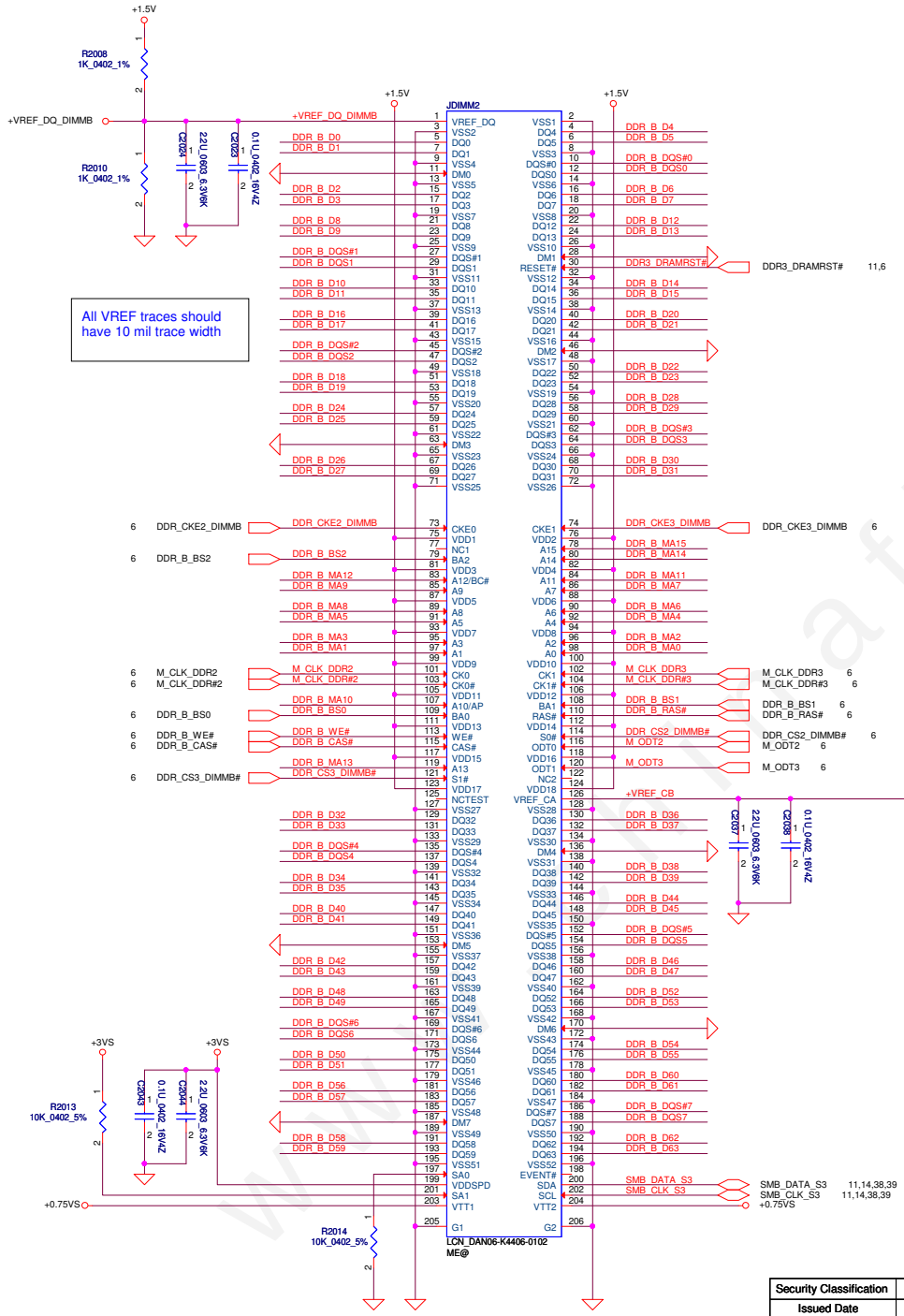

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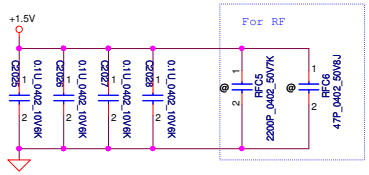

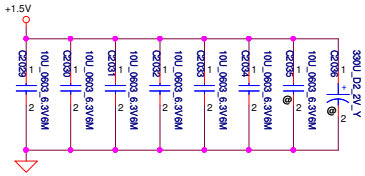

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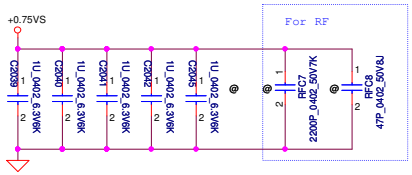

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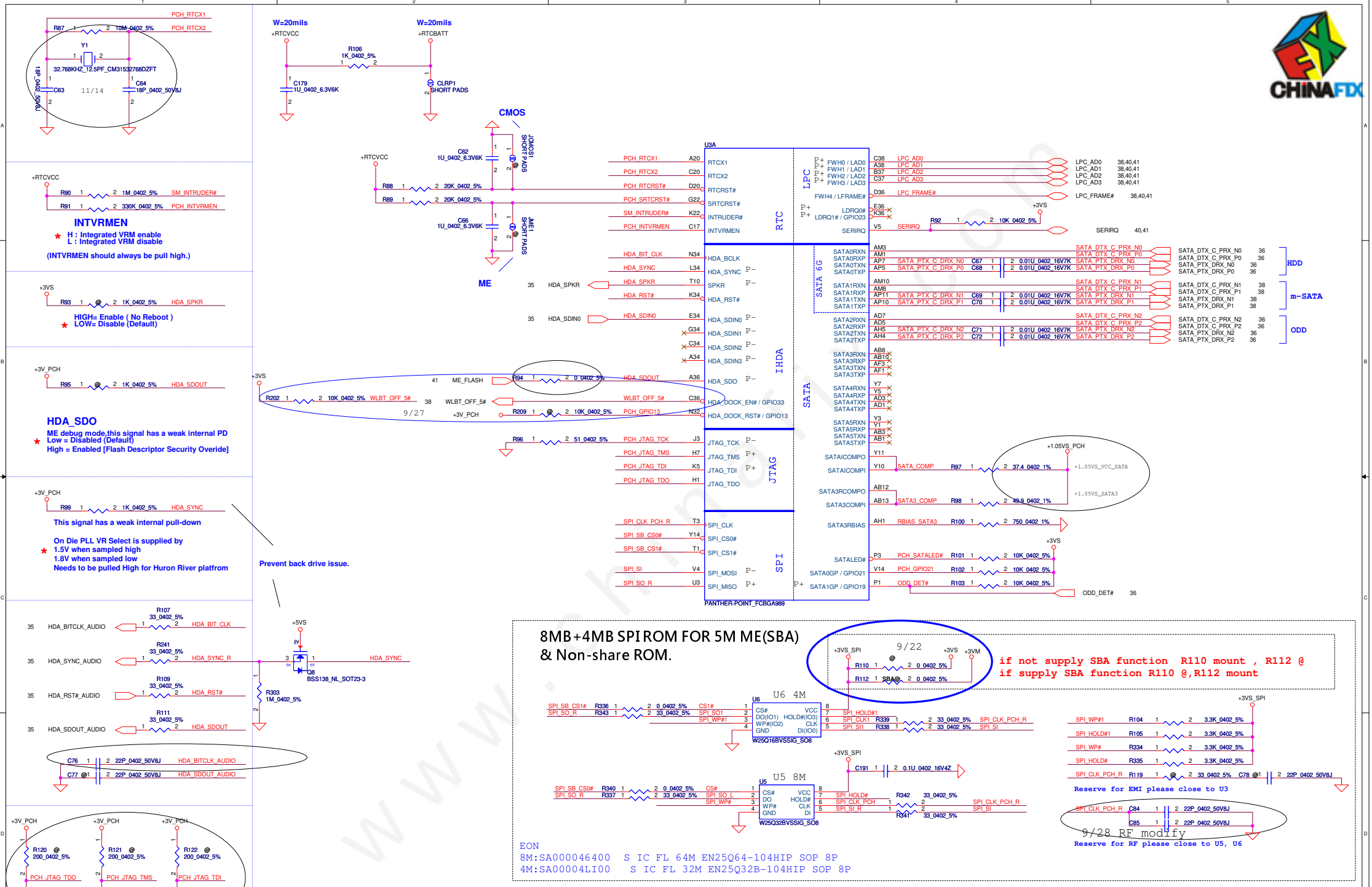

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Title: PCH (1/9) SATA,HDA,SPI, LPC

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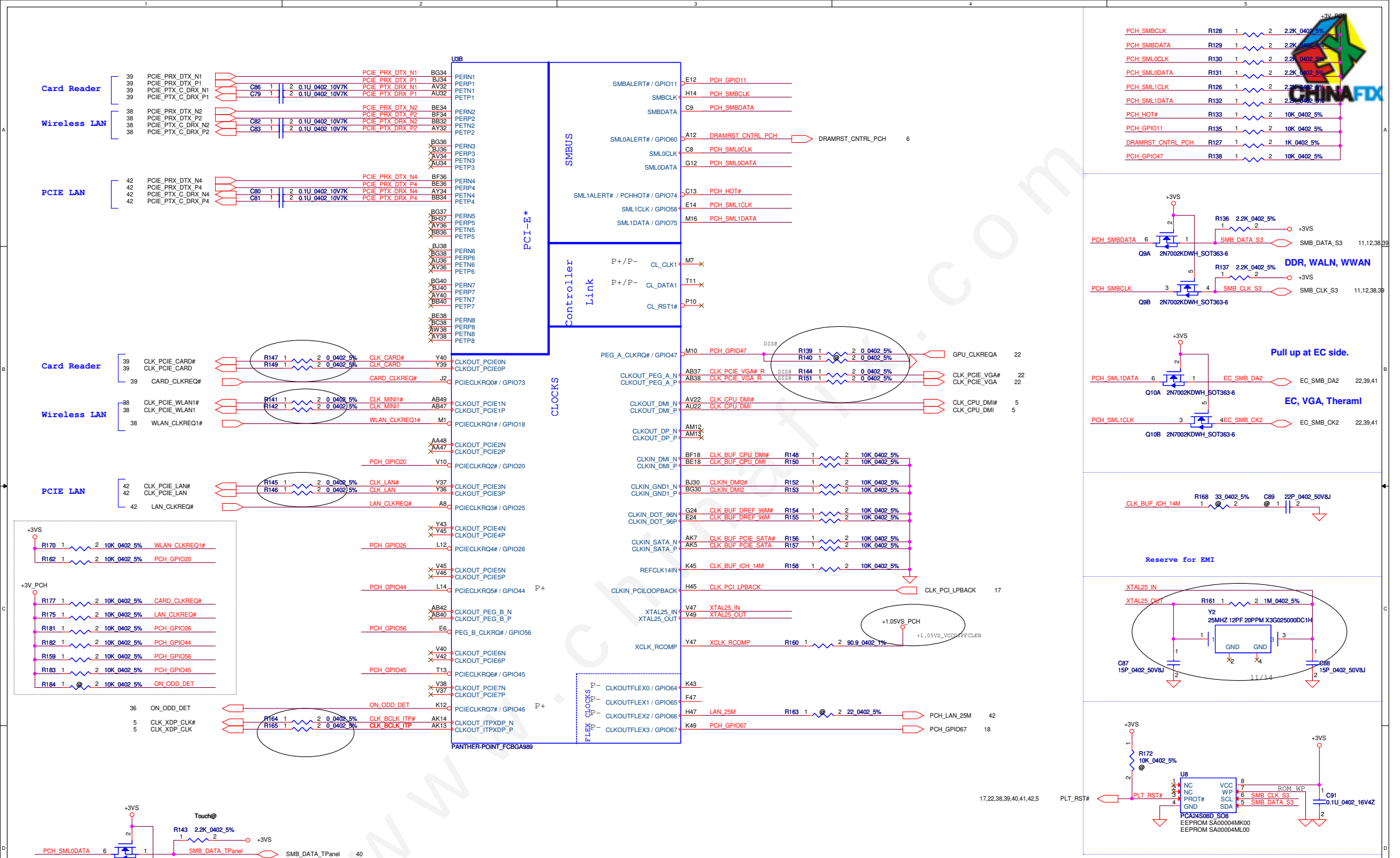
Date: Saturday, November 03, 2012 | Sheet 13 of 59


U3B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
PANTHER-POINT_FCBGA989
Card Reader
Wireless LAN
PCIE LAN
PCIE_PRX_DTX_N1
PCIE_PRX_DTX_P1
PCIE_PTX_C_DRX_N1
PCIE_PTX_C_DRX_P1
PCIE_PRX_DTX_N2
PCIE_PRX_DTX_P2
PCIE_PTX_C_DRX_N2
PCIE_PTX_C_DRX_P2
PCIE_PRX_DTX_N4
PCIE_PRX_DTX_P4
PCIE_PTX_C_DRX_N4
PCIE_PTX_C_DRX_P4
C86 0.1U_0402_10V7K
C79 0.1U_0402_10V7K
C82 0.1U_0402_10V7K
C83 0.1U_0402_10V7K
C80 0.1U_0402_10V7K
C81 0.1U_0402_10V7K
SMBALERT# / GPIO11
SMBCLK
SMBDATA
SML0ALERT# / GPIO60
SML0CLK
SML0DATA
SML1ALERT# / PCHHOT# / GPIO74
SML1CLK / GPIO58
SML1DATA / GPIO75
PCH_GPIO11
PCH_SMBCLK
PCH_SMBDATA
DRAMRST_CNTRL_PCH
PCH_SML0CLK
PCH_SML0DATA
PCH_HOT#
PCH_SML1CLK
PCH_SML1DATA
CL_CLK1
CL_DATA1
CL_RST1#
PEG_A_CLKRQ# / GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_GND1_N
CLKIN_GND1_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
CLKOUTFLEX0 / GPIO64
CLKOUTFLEX1 / GPIO65
CLKOUTFLEX2 / GPIO66
CLKOUTFLEX3 / GPIO67
GPU_CLKREQA
CLK_PCIE_VGA# R
CLK_PCIE_VGA# R
CLK_PCIE_VGA
CLK_CPU_DMI#
CLK_CPU_DMI
CLK_BUF_CPU_DMI#
CLK_BUF_CPU_DMI
CLKIN_DMI2#
CLKIN_DMI2
CLK_BUF_DREF_96M#
CLK_BUF_DREF_96M
CLK_BUF_PCIE_SATA#
CLK_BUF_PCIE_SATA
CLK_BUF_ICH_14M
CLK_PCI_LPBACK
90.9_0402_1%
+1.05VS_PCH
+1.05VS_VCCDIFFCLKN
LAN_25M
PCH_LAN_25M
PCH_GPIO67
CLK_CARD#
CLK_CARD
CARD_CLKREQ#
CLK_MINI1#
CLK_MINI1
WLAN_CLKREQ1#
CLK_LAN#
CLK_LAN
LAN_CLKREQ#
PCH_GPIO20
PCH_GPIO26
PCH_GPIO44
PCH_GPIO56
PCH_GPIO45
ON_ODD_DET
CLK_BCLK_ITP#
CLK_BCLK_ITP
CLK_XDP_CLK#
CLK_XDP_CLK
CLKOUT_PCIE0N
CLKOUT_PCIE0P
PCIECLKRQ0# / GPIO73
CLKOUT_PCIE1N
CLKOUT_PCIE1P
PCIECLKRQ1# / GPIO18
CLKOUT_PCIE2N
CLKOUT_PCIE2P
PCIECLKRQ2# / GPIO20
CLKOUT_PCIE3N
CLKOUT_PCIE3P
PCIECLKRQ3# / GPIO25
CLKOUT_PCIE4N
CLKOUT_PCIE4P
PCIECLKRQ4# / GPIO26
CLKOUT_PCIE5N
CLKOUT_PCIE5P
PCIECLKRQ5# / GPIO44
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
PEG_B_CLKRQ# / GPIO56
CLKOUT_PCIE6N
CLKOUT_PCIE6P
PCIECLKRQ6# / GPIO45
CLKOUT_PCIE7N
CLKOUT_PCIE7P
PCIECLKRQ7# / GPIO46
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
+3VS
R170 10K_0402_5% WLAN_CLKREQ1#
R162 10K_0402_5% PCH_GPIO20
+3V_PCH
R177 10K_0402_5% CARD_CLKREQ#
R175 10K_0402_5% LAN_CLKREQ#
R181 10K_0402_5% PCH_GPIO26
R182 10K_0402_5% PCH_GPIO44
R159 10K_0402_5% PCH_GPIO56
R183 10K_0402_5% PCH_GPIO45
R184 10K_0402_5% ON_ODD_DET
Touch@
R143 2.2K_0402_5%
SMB_DATA_TPanel
SMB_DATA_TPanel 40
Q2417A 2N7002KDWH_SOT363-6
R167 2.2K_0402_5%
SMB_CLK_TPanel
SMB_CLK_TPanel 40
Q2417B 2N7002KDWH_SOT363-6
Touch Panel
R128 2.2K_0402_5%
R129 2.2K_0402_5%
R130 2.2K_0402_5%
R131 2.2K_0402_5%
R126 2.2K_0402_5%
R132 2.2K_0402_5%
R133 10K_0402_5%
R135 10K_0402_5%
R127 1K_0402_5%
R138 10K_0402_5%
R136 2.2K_0402_5%
R137 2.2K_0402_5%
Q9A 2N7002KDWH_SOT363-6
Q9B 2N7002KDWH_SOT363-6
DDR, WALN, WWAN
Pull up at EC side.
Q10A 2N7002KDWH_SOT363-6
Q10B 2N7002KDWH_SOT363-6
EC, VGA, Theraml
R168 33_0402_5%
C89 22P_0402_50V8J
Reserve for EMI
XTAL25_IN
XTAL25_OUT
R161 1M_0402_5%
Y2
25MHZ 12PF 20PPM X3G025000DC1H
C87 15P_0402_50V8J
C88 15P_0402_50V8J
R172 10K_0402_5%
U8
PCA24S08D_SO8
EEPROM SA00004MK00
EEPROM SA00004ML00
C91 0.1U_0402_16V4Z
PLT_RST#
17,22,38,39,40,41,42,5
Security Classification
LC Future Center Secret Data
Issued Date
2012/07/01
Deciphered Date
2014/07/01
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Title
PCH (2/9) PCIE, SMBUS, CLK
Size Custom
Document Number
NM-A041
Rev 1.A
Date: Saturday, November 03, 2012
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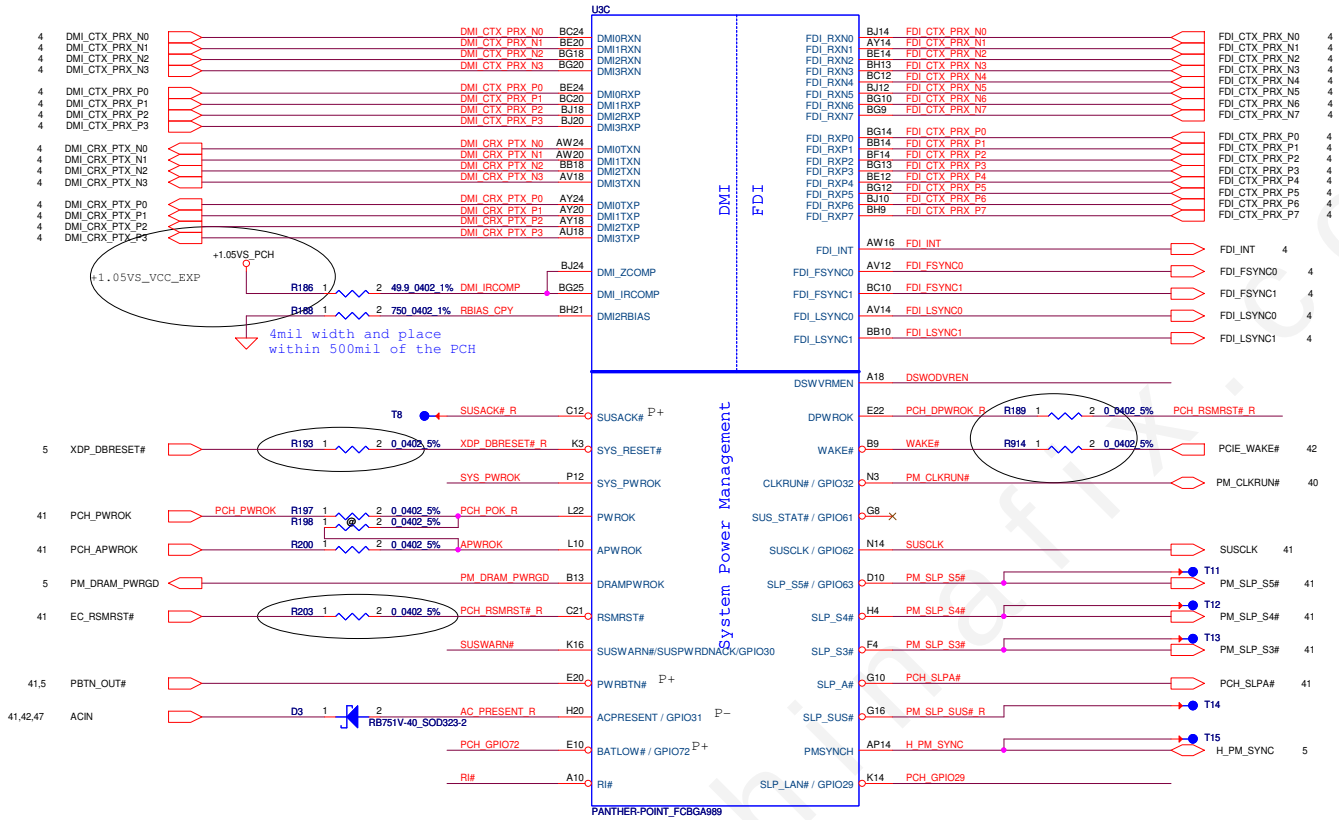
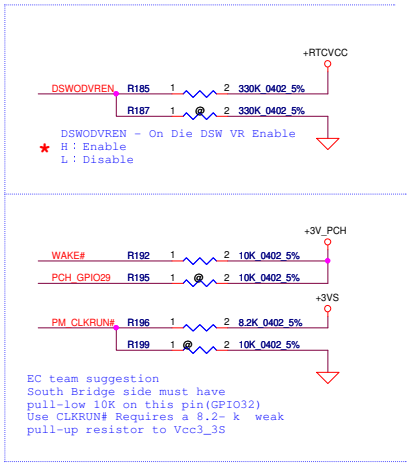
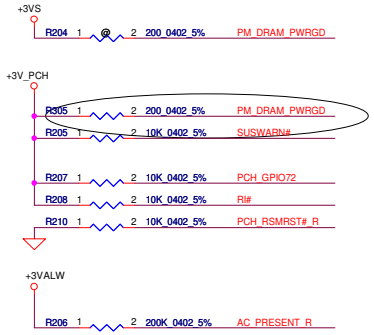
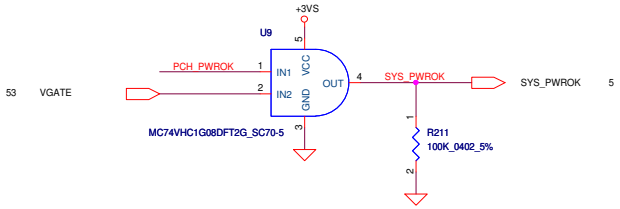




Can be left NC when
IAMT is not support on
the platfrom





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Title: PCH (3/9) DMI,FDI,PM

Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Saturday, November 03, 2012 | Sheet 15 of 59

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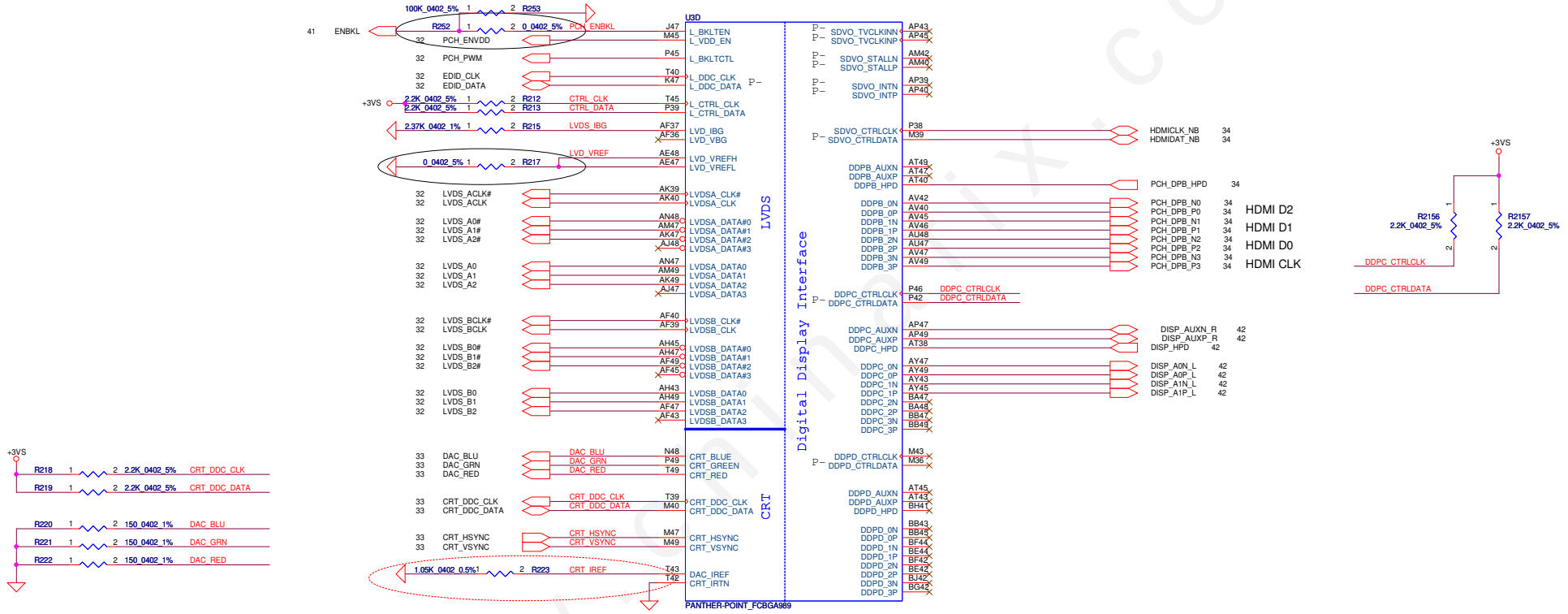

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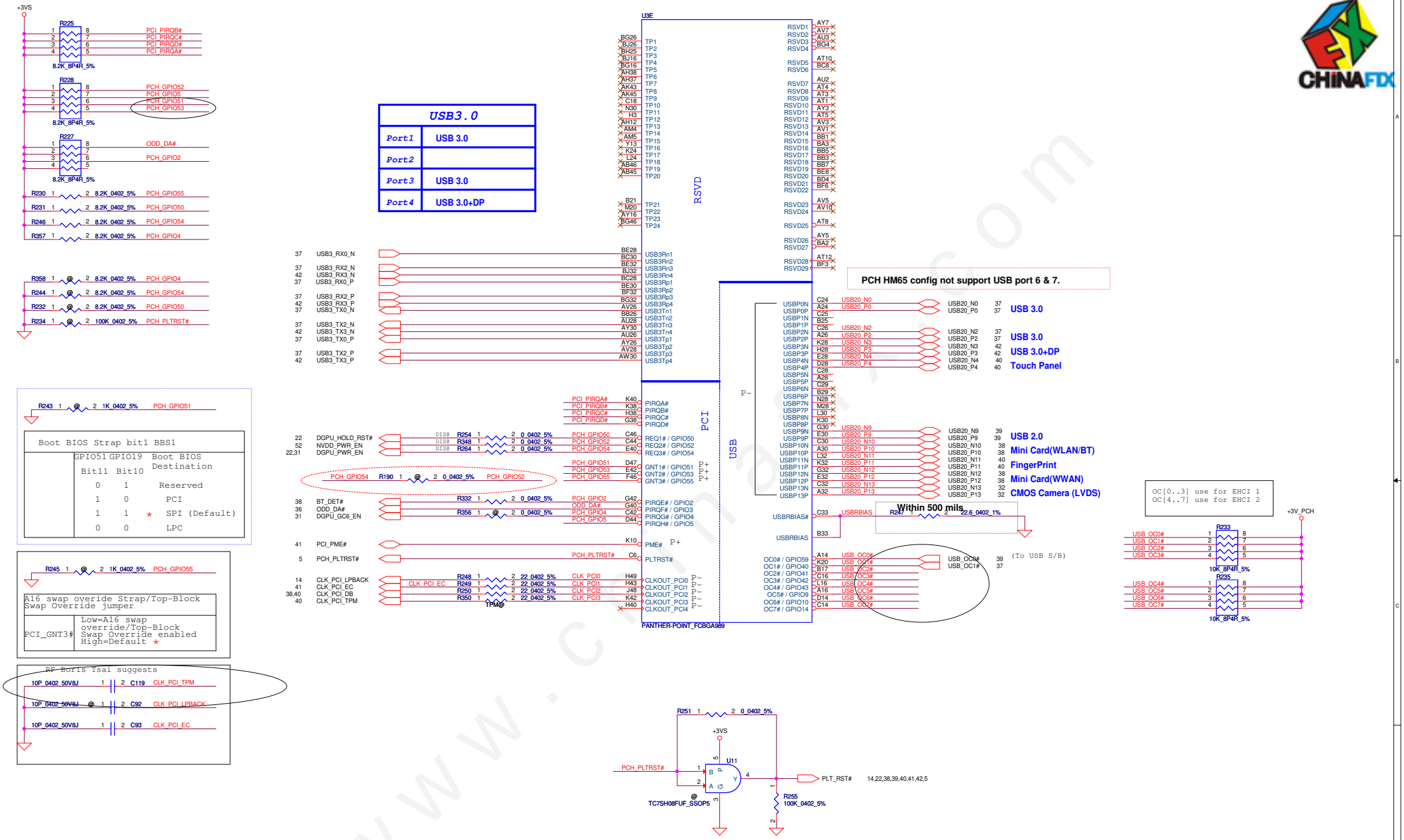
Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Saturday, November 03, 2012 | Sheet 16 of 59



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Title: PCH (5/9) PCI, USB, NVRAM

Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Saturday, November 03, 2012 | Sheet 17 of 59

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

R265 1 @ 2 1K_0402_5% PCH_GPIO28

R274 1 @ 2 1K_0402_5% EC_SMI#

+3VS
R280 1 2 10K_0402_5%
R282 1 @ 2 10K_0402_5% WLBT_OFF_51#

For GC6

+3V_PCH
R288 1 2 10K_0402_5%
R290 1 @ 2 10K_0402_5% PCH_GPIO24

+3VS
R285 1 @ 2 10K_0402_5%
R284 1 2 10K_0402_5% PCH_GPIO37

+3VS
R269 1 2 10K_0402_5% PCH_GPIO0
R270 1 2 10K_0402_5% PCH_GPIO1
R266 1 2 10K_0402_5% PCH_GPIO6
R344 1 2 10K_0402_5% EC_SCI#
R275 1 2 10K_0402_5% PCH_GPIO16
R268 1 2 10K_0402_5% DGPU_PWROK
R277 1 2 10K_0402_5% PCH_GPIO22
R346 1 2 10K_0402_5% PCH_GPIO34 GPIO34
R283 1 2 10K_0402_5% 3G_DET#
R287 1 2 10K_0402_5% 3G_OFF#
R289 1 2 10K_0402_5% GPS_OFF#
R291 1 2 10K_0402_5% PCH_GPIO49

+3V_PCH
R345 1 2 10K_0402_5% EC_SMI#
R271 1 2 10K_0402_5% PCH_GPIO12
R273 1 2 1K_0402_5% PCH_GPIO15
R347 1 2 10K_0402_5% PCH_GPIO28
R292 1 @ 2 10K_0402_5% PCH_GPIO57
R352 1 2 10K_0402_5% PCH_GPIO27

U3F

			PCH_GPIO0	T7	BMBUSY# / GPIO0	P+	TACH4 / GPIO68	C40	ODD_EN# → ODD_EN# 36
39	FN_LED#	R359 1 2 0_0402_5%	PCH_GPIO1	A42	TACH1 / GPIO1	P+	TACH5 / GPIO69	B41	PCH_GPIO69
39	F1_LED#	R360 1 2 0_0402_5%	PCH_GPIO6	H36	TACH2 / GPIO6	P+	TACH6 / GPIO70	C41	PCH_GPIO70
41	EC_SCI#		EC_SCI#	E38	TACH3 / GPIO7	P+	TACH7 / GPIO71	A40	CMOS_ON# → CMOS_ON# 32
41	EC_SMI#		EC_SMI#	C10	GPIO8	P+			
			PCH_GPIO12	C4	LAN_PHY_PWR_CTRL / GPIO12				
41	EC_WAKE#	R178 1 2 0_0402_5%	PCH_GPIO15	G2	GPIO15	P−			
			PCH_GPIO16	U2	SATA4GP / GPIO16				
31,52	DGPU_PWROK		DGPU_PWROK	D40	TACH0 / GPIO17				
39	F4_LED#	R361 1 2 0_0402_5%	PCH_GPIO22	T5	SCLOCK / GPIO22				
			PCH_GPIO24	E8	GPIO24				
38	mSATA_PCH	R293 1 2 0_0402_5%	PCH_GPIO27	E16	GPIO27	P+			
			PCH_GPIO28	P8	GPIO28	P+			
			PCH_GPIO34	K1	STP_PCI# / GPIO34				
38	3G_DET#		3G_DET#	K4	GPIO35				
38	WLBT_OFF_51#		WLBT_OFF_51#	V8	SATA2GP / GPIO36	P−			
			PCH_GPIO37	M5	SATA3GP / GPIO37	P−			
			PCH_GPIO38	N2	SLOAD / GPIO38				
38	3G_OFF#		3G_OFF#	M3	SDATAOUT0 / GPIO39				
38	GPS_OFF#		GPS_OFF#	V13	SDATAOUT1 / GPIO48				
			PCH_GPIO49	V3	SATA5GP / GPIO49 / TEMP_ALERT#				
			PCH_GPIO57	D6	GPIO57				

GPIO

	A20GATE	P4	→ GATEA20 41
P−	PECI	AU16	PCH_PECI_R R307 1 @ 2 0_0402_5% → H_PECI 41,5
	RCIN#	P5	KB_RST# → KB_RST# 41
	PROCPWRGD	AY11	H_CPUPWRGD → H_CPUPWRGD 5
	THRMTRIP#	AY10	R278 1 2 390_0402_5% H_THRMTRIP# → H_THRMTRIP# 5, VGA_THRMTRIP# 22
P+	INIT3_3V#	T14	
P−	DF_TVS	AY1	DF_TVS
	TS_VSS1	AH8	
	TS_VSS2	AK11	
	TS_VSS3	AH10	
	TS_VSS4	AK10	
	NC_1	P37	

CPU/MISC

INIT3_3V
This signal has weak internal PU, can't pull low

Intel schematic reviwe recommand.

	VSS_NCTF_15	BG2	T18
	VSS_NCTF_16	BG48	T19
	VSS_NCTF_17	BH3	T20
	VSS_NCTF_18	BH47	T21
	VSS_NCTF_19	BJ4	T23
	VSS_NCTF_20	BJ44	T25
	VSS_NCTF_21	BJ45	T27
	VSS_NCTF_22	BJ46	T29
	VSS_NCTF_23	BJ5	T31
	VSS_NCTF_24	BJ6	T33
	VSS_NCTF_25	C2	T35
	VSS_NCTF_26	C48	T37
	VSS_NCTF_27	D1	T39
	VSS_NCTF_28	D49	T41
	VSS_NCTF_29	E1	T43
	VSS_NCTF_30	E49	T45
	VSS_NCTF_31	F1	T47
	VSS_NCTF_32	F49	T49

T22	A4	VSS_NCTF_1	
T24	A44	VSS_NCTF_2	
T26	A45	VSS_NCTF_3	
T28	A46	VSS_NCTF_4	
T30	A5	VSS_NCTF_5	
T32	A6	VSS_NCTF_6	
T34	B3	VSS_NCTF_7	
T36	B47	VSS_NCTF_8	
T38	BD1	VSS_NCTF_9	
T40	BD49	VSS_NCTF_10	
T42	BE1	VSS_NCTF_11	
T44	BE49	VSS_NCTF_12	
T46	BF1	VSS_NCTF_13	
T48	BF49	VSS_NCTF_14	

NCTF

PANTHER-POINT_FCBGA989

ODD_EN# R256 1 2 8.2K_0402_5%
R260 1 @ 2 8.2K_0402_5%

+3VS
PCH_GPIO70 R258 2 1 10K_0402_5%
R262 1 @ 2 10K_0402_5%

+3VS
CMOS_ON# R257 2 1 10K_0402_5%
R263 1 @ 2 10K_0402_5%

+3VS
GATEA20 R272 1 2 10K_0402_5%
KB_RST# R276 1 2 10K_0402_5%

+1.8VS
R226 2.2K_0402_5%
DF_TVS R229 1 2 1K_0402_5% → H_SNB_IVB# 5

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

CLOSE TO THE BRANCHING POINT

For Edge code setting

PCH_GPIO69	PCH_GPIO38	PCH_GPIO67	Function
0	0	0	Optimus
0	0	1	Reserved
0	1	0	DIS
0	1	1	UMA

+3VS
R259 10K_0402_5% @
R330 10K_0402_5% UMA@
R311 10K_0402_5% UMA@
PCH_GPIO69
PCH_GPIO38
PCH_GPIO67 → PCH_GPIO67 14
R261 10K_0402_5%
R329 10K_0402_5% DIS@
R286 10K_0402_5% DIS@

(MB_ID_2)
(MB_ID_1)
(MB_ID_0)

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Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title: PCH (6/9) GPIO, CPU, MISC

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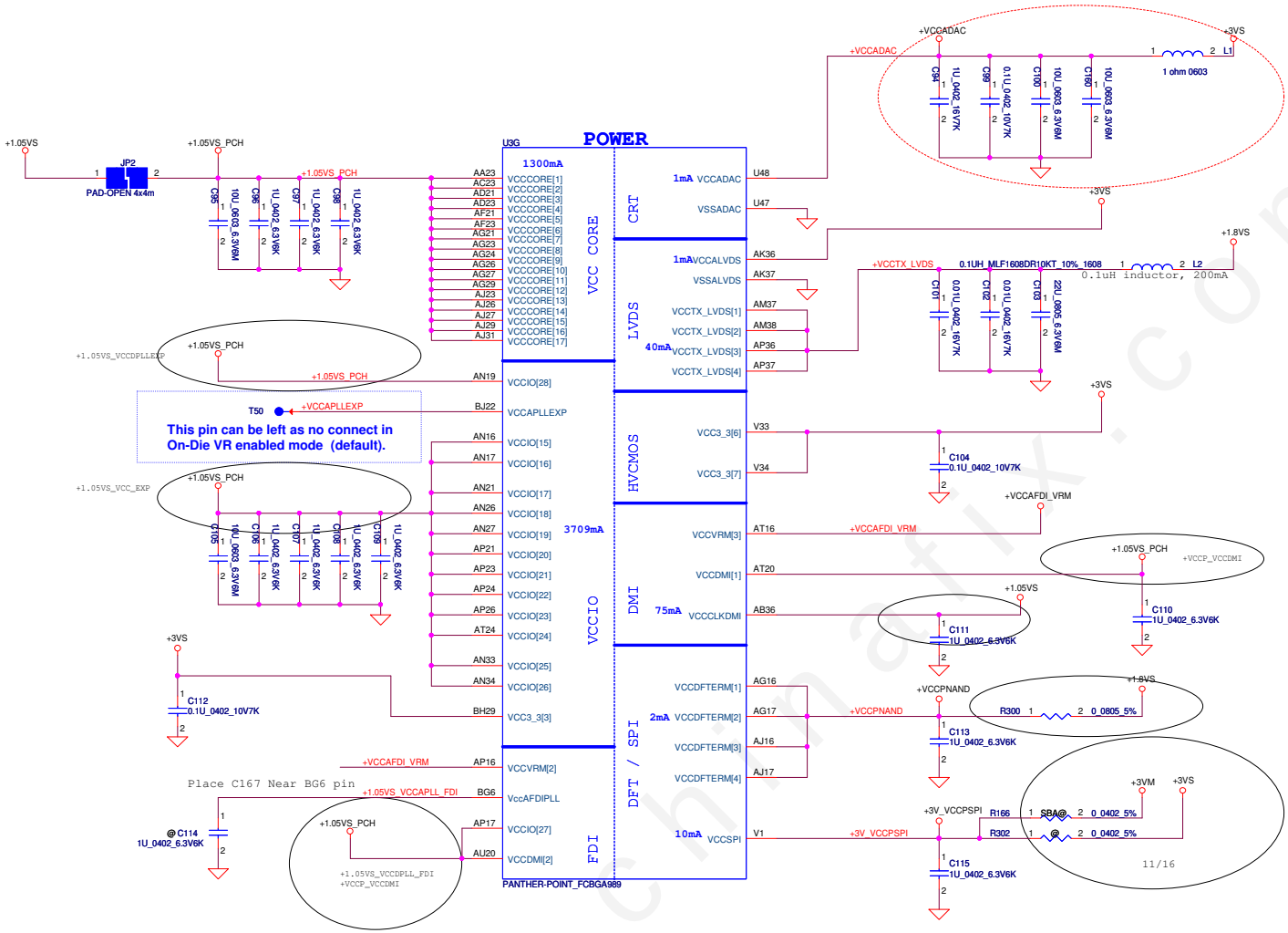

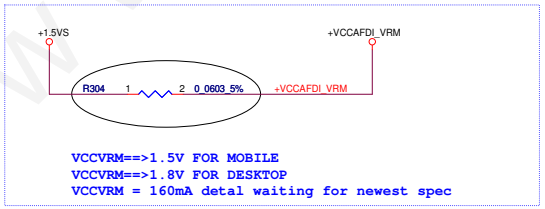

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Title: PCH (7/9) PWR

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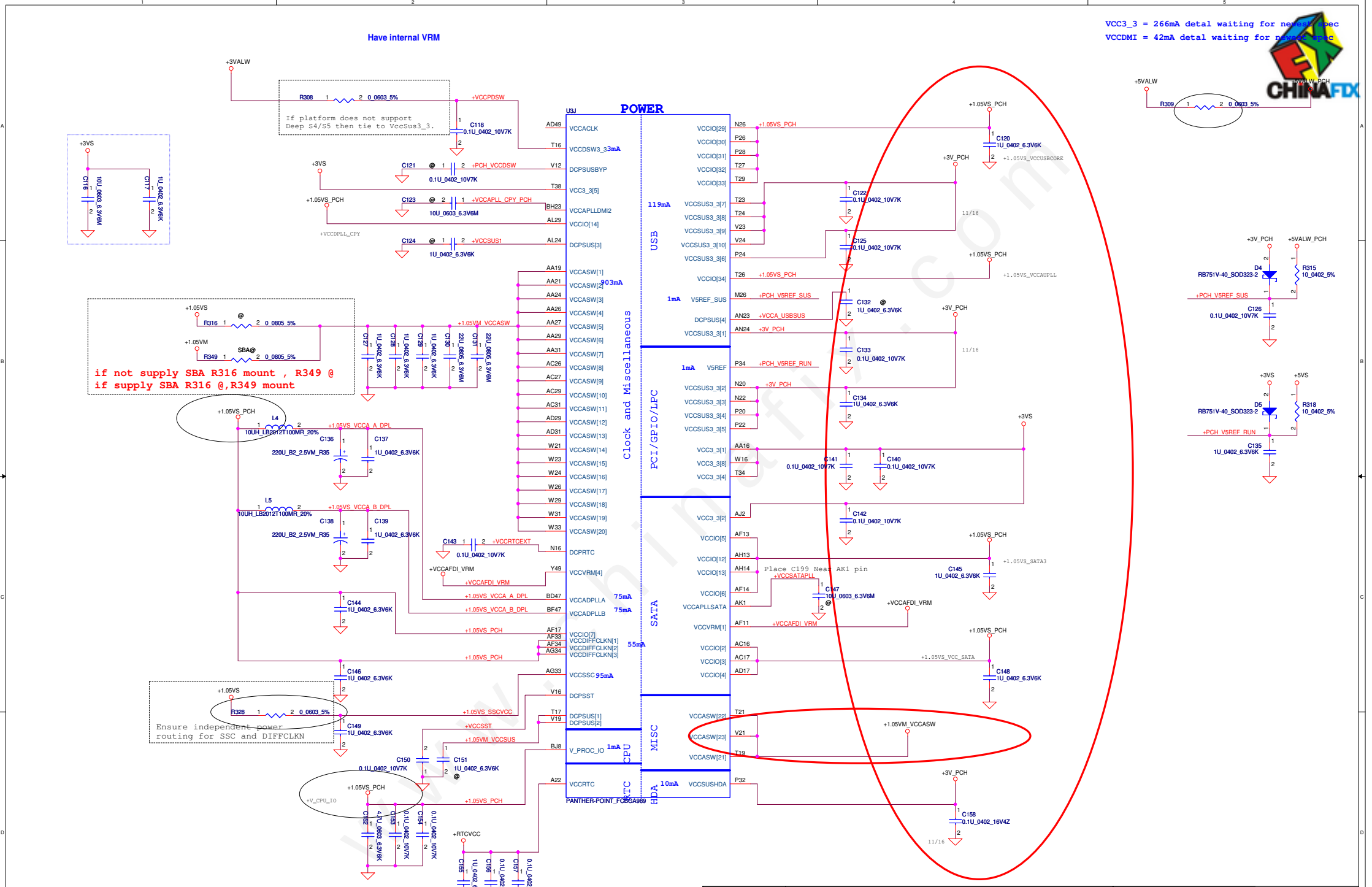

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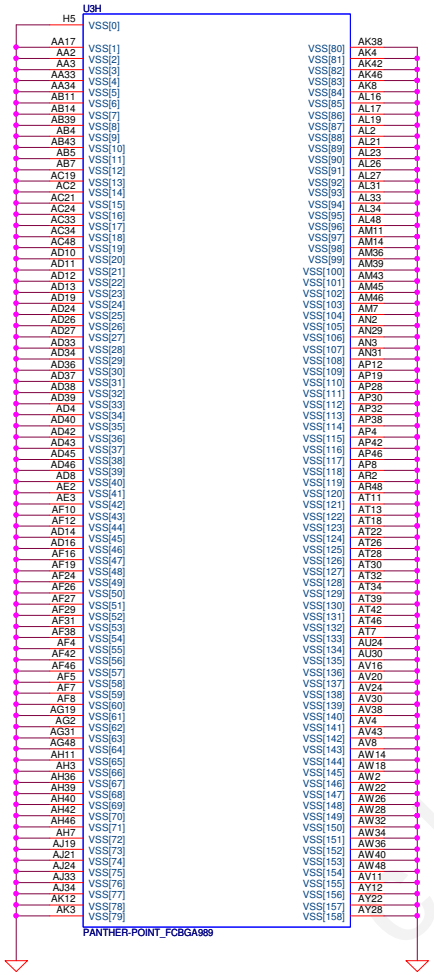
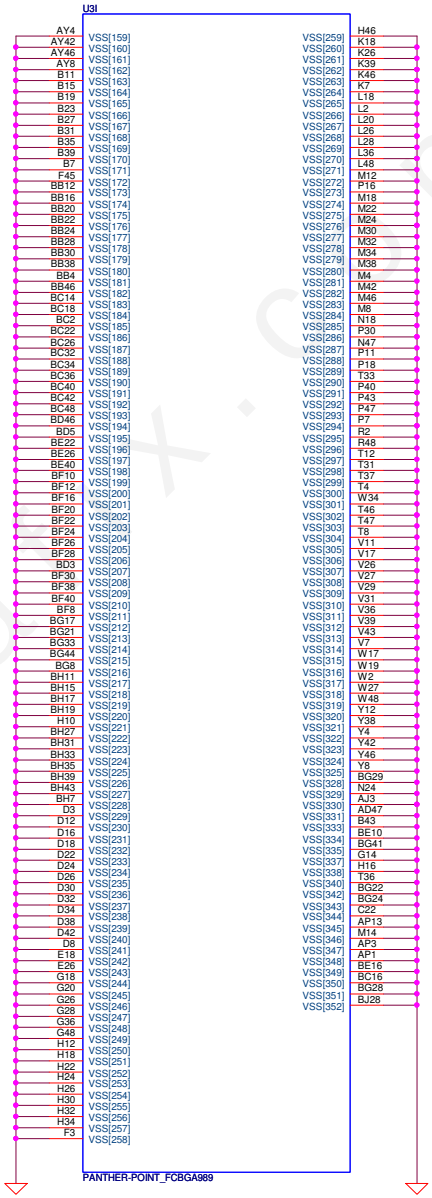
Title: PCH (8/9) PWR

Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Saturday, November 03, 2012 | Sheet 20 of 59





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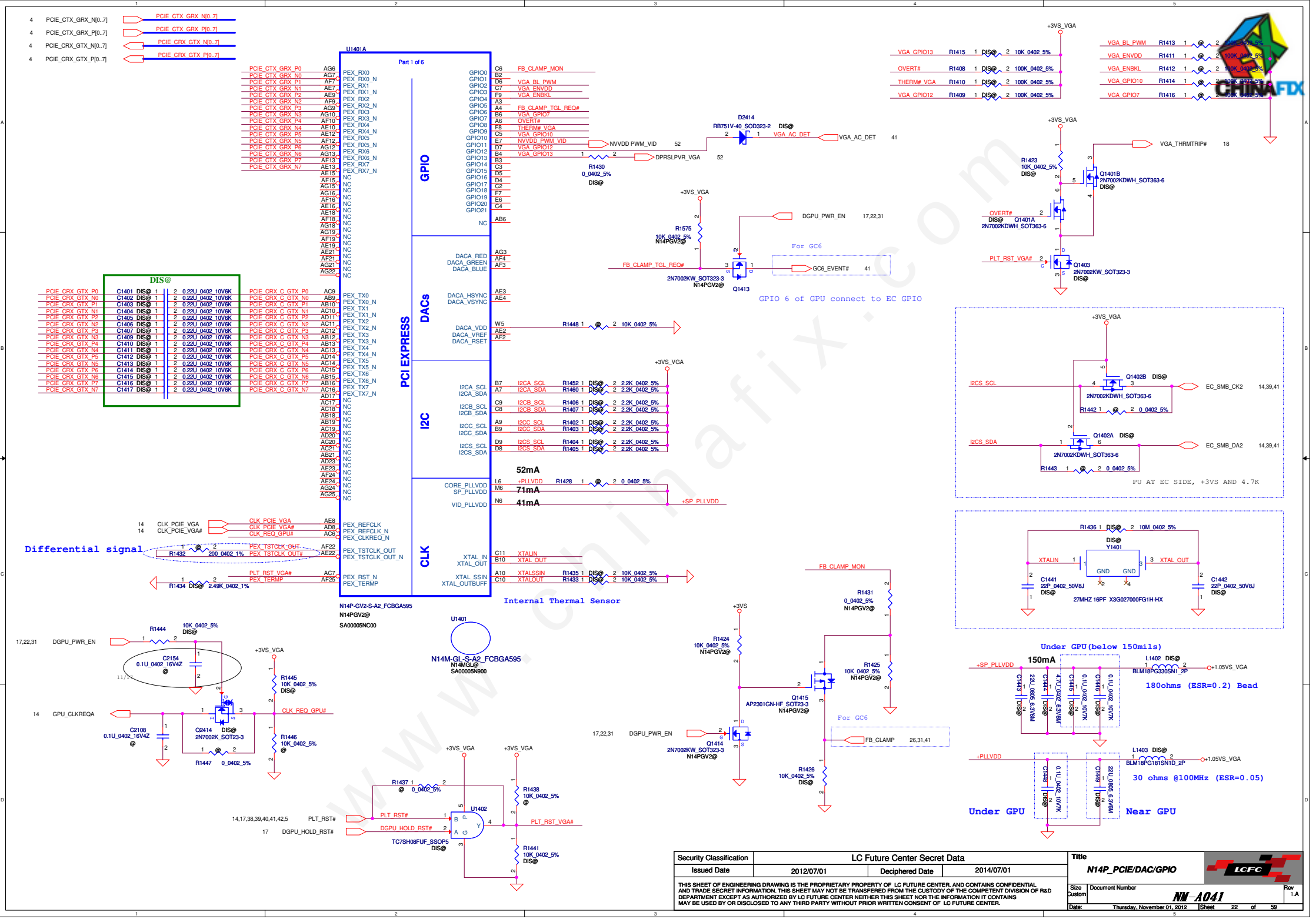
Title: PCH (9/9) VSS

Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Saturday, November 03, 2012 | Sheet 21 of 59



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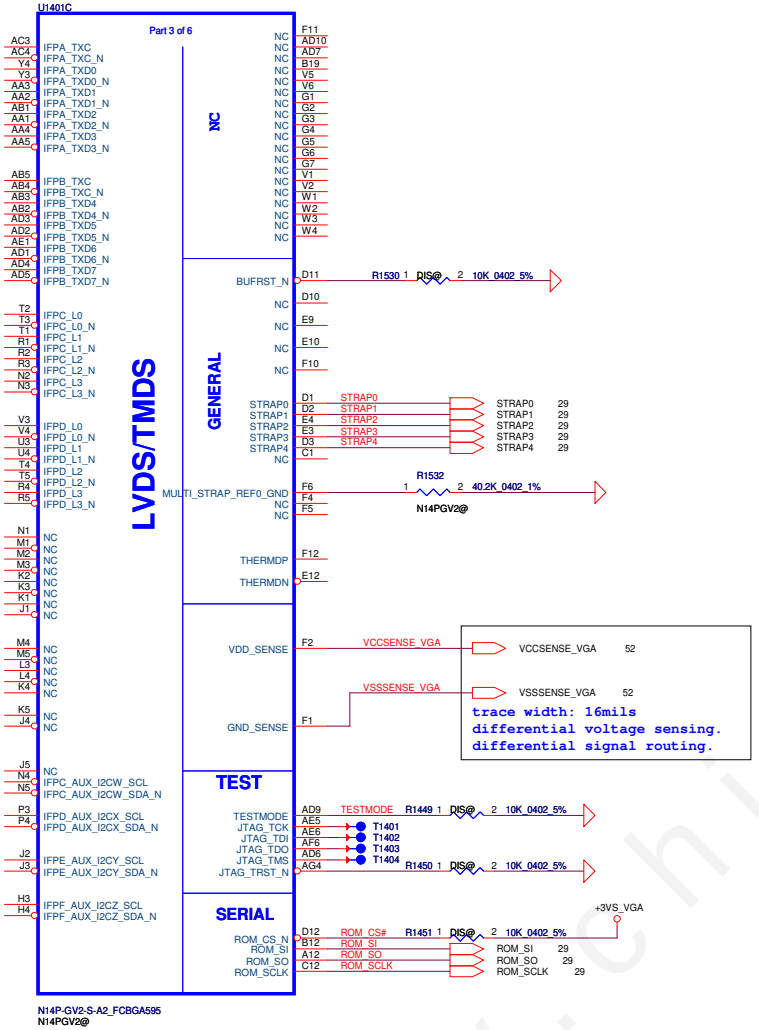
Title: N14P_PCIE/DAC/GPIO

Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Thursday, November 01, 2012 | Sheet 22 of 59



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Title: N14P_LVDS/HDMI/THERM

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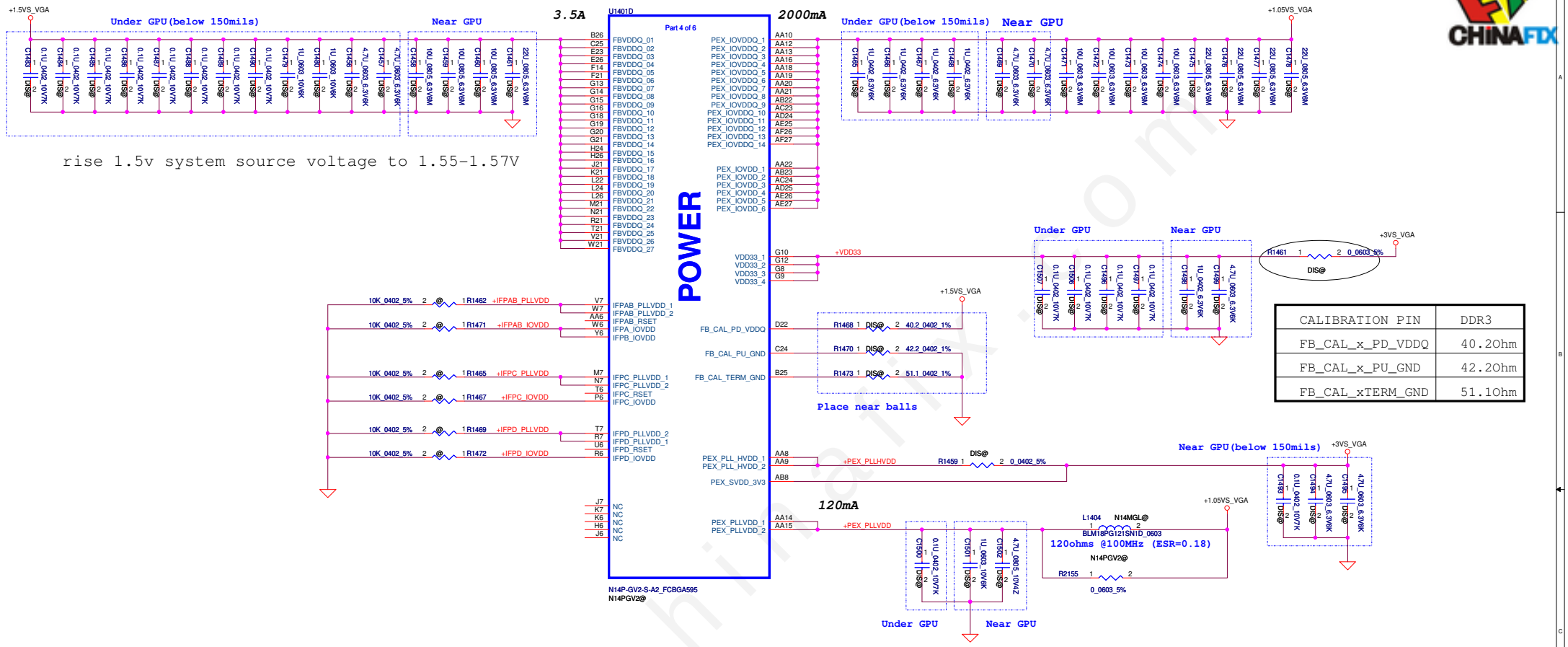

CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	42.2Ohm
FB_CAL_xTERM_GND	51.1Ohm

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Title: N14P_Power

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Date: Thursday, November 01, 2012 | Sheet 24 of 59

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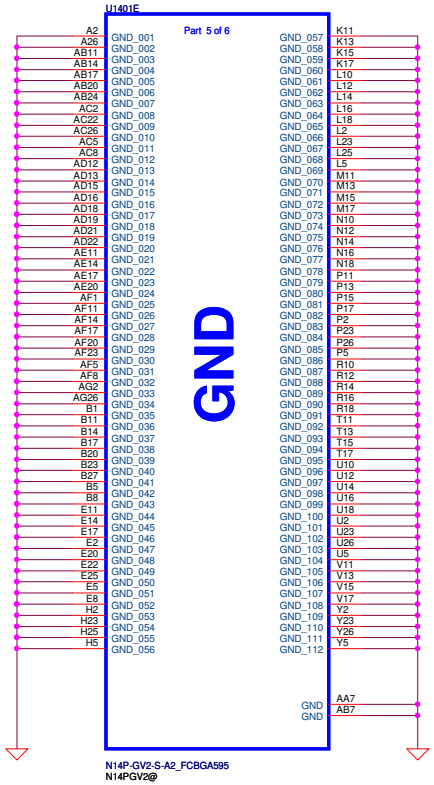

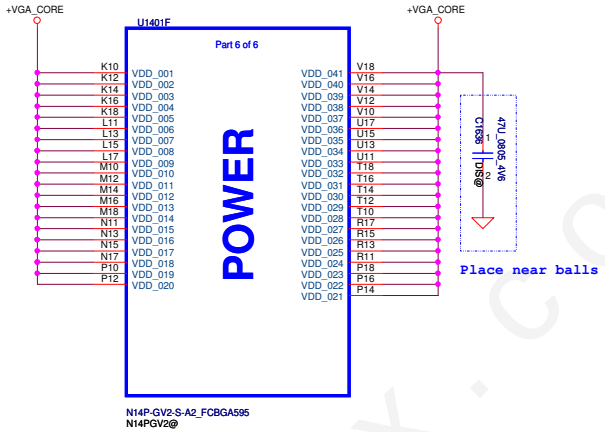

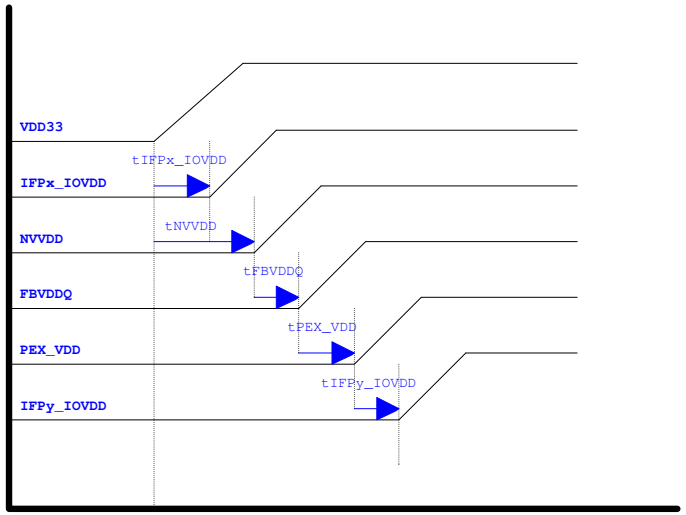

NV Recommended Power On Sequencing Order

X=A and B
Y=C,D,E and F

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Title: N14P_VGA CORE, GND

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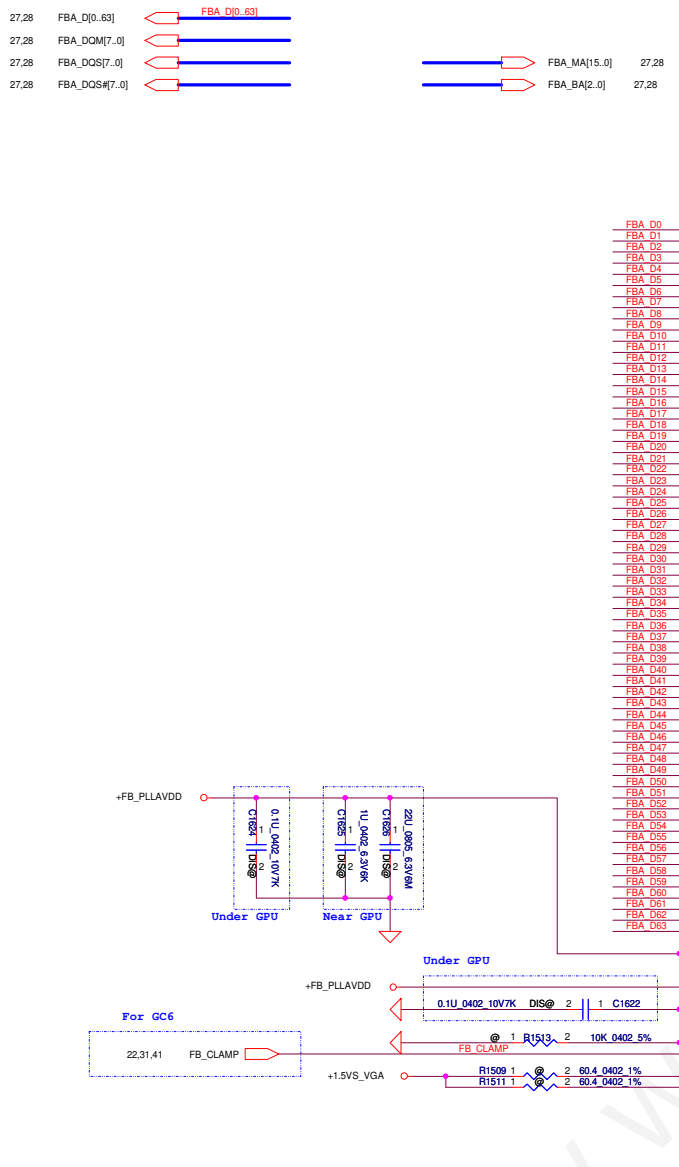

Mode D - Mirror Mode Mapping

Address	DATA Bus 0..31	DATA Bus 32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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Title: N14P_MEM Interface

Size: Custom | Document Number: NM-A041 | Rev: 1.A

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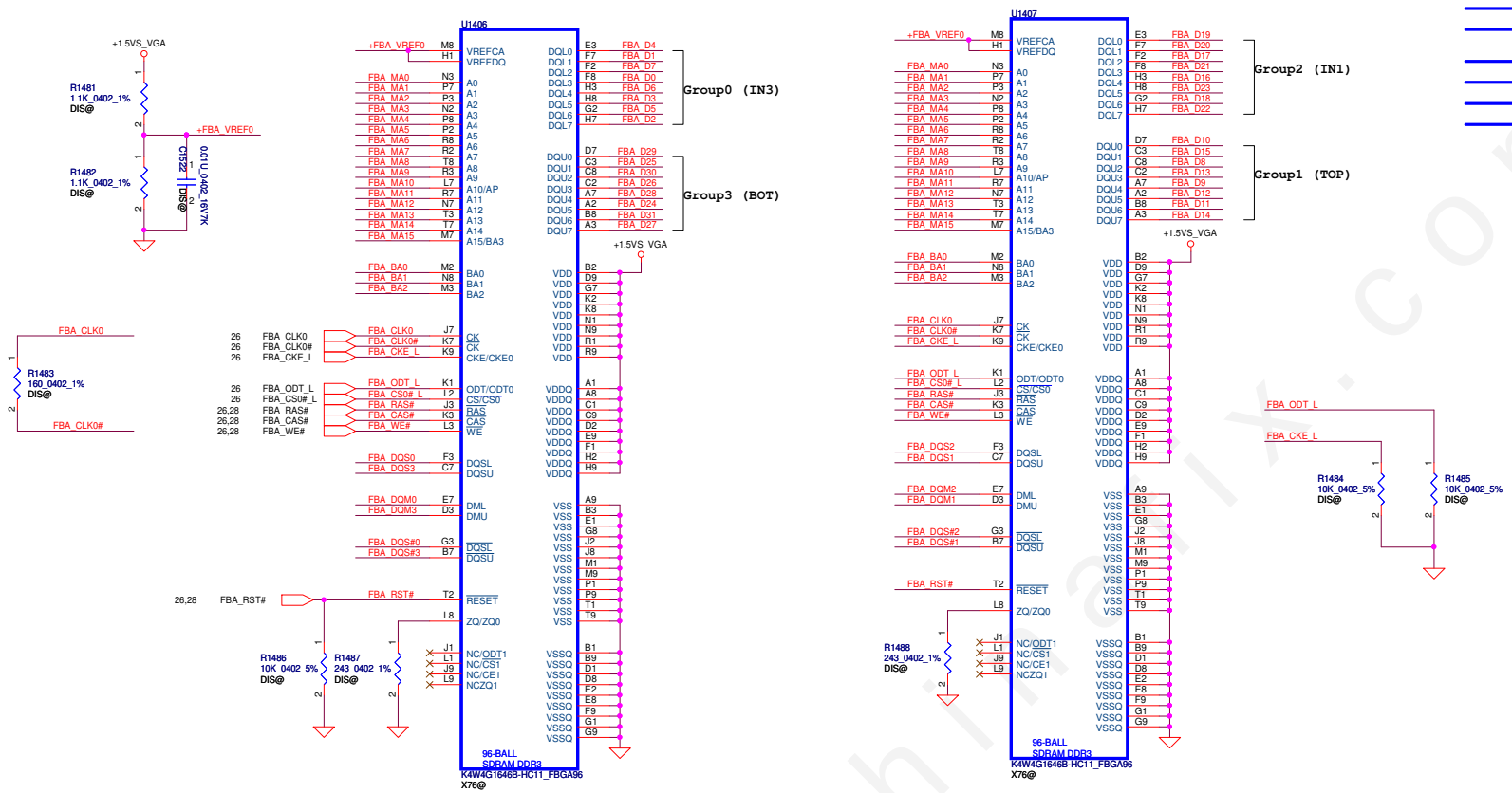
Memory Partition A - Lower 32 bits



FBA_MA[15..0] 26,28
FBA_BA[2..0] 26,28
FBA_D[0..63] 26,28
FBA_DQM[7..0] 26,28
FBA_DQS[7..0] 26,28
FBA_DQS#[7..0] 26,28

Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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Title: N14P_GDDR3_A Lower

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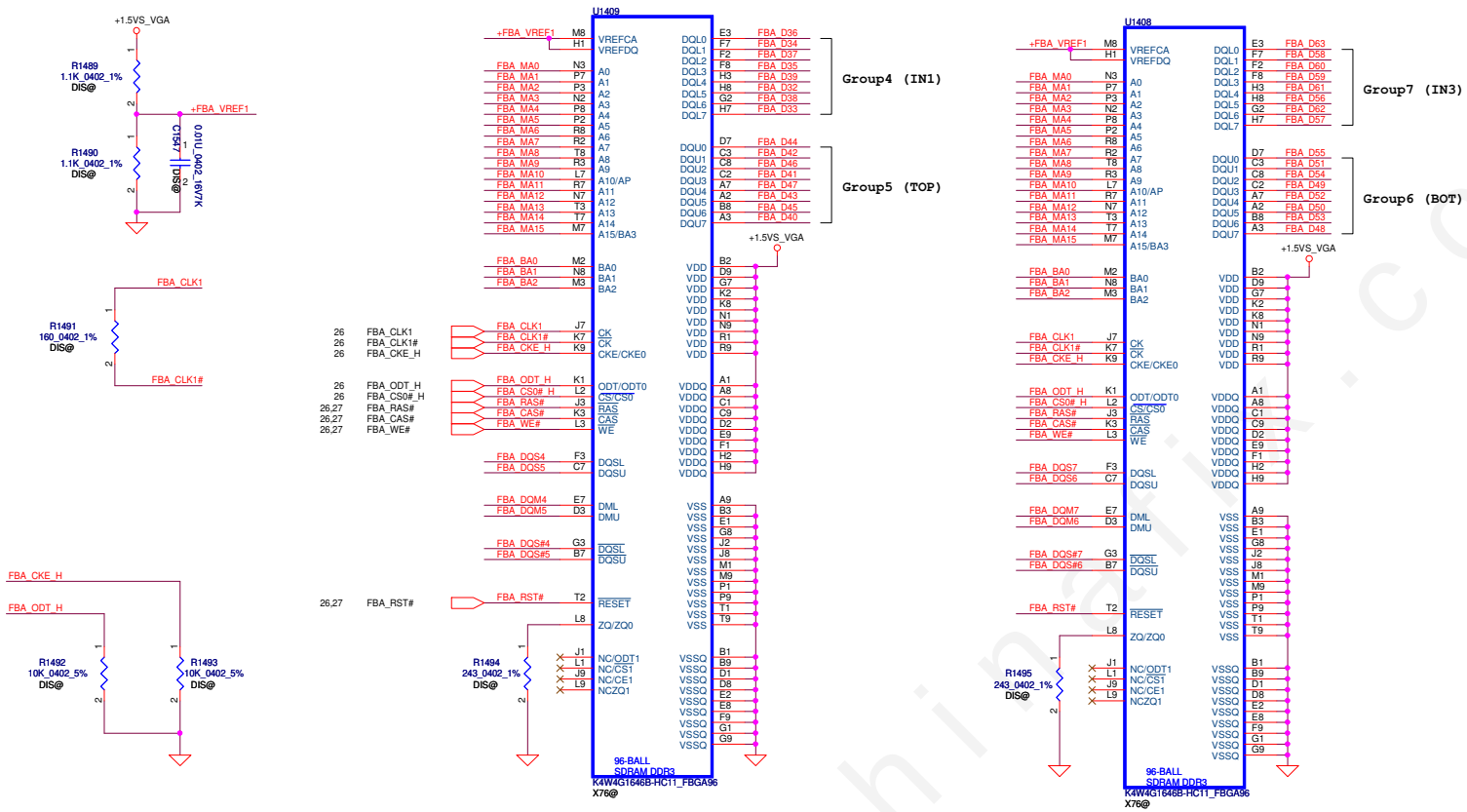
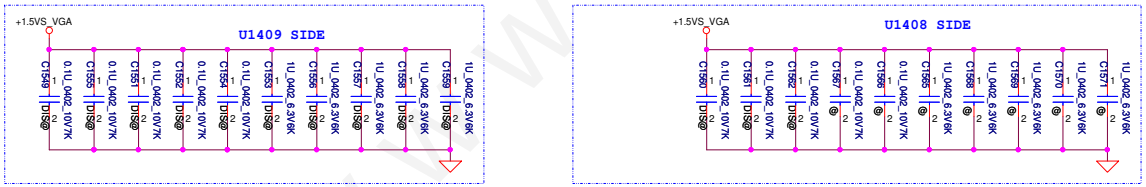
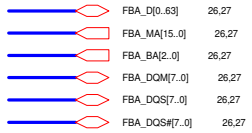
Memory Partition A - Upper 32 bits







Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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Title: N14P_GDDR3_A Upper

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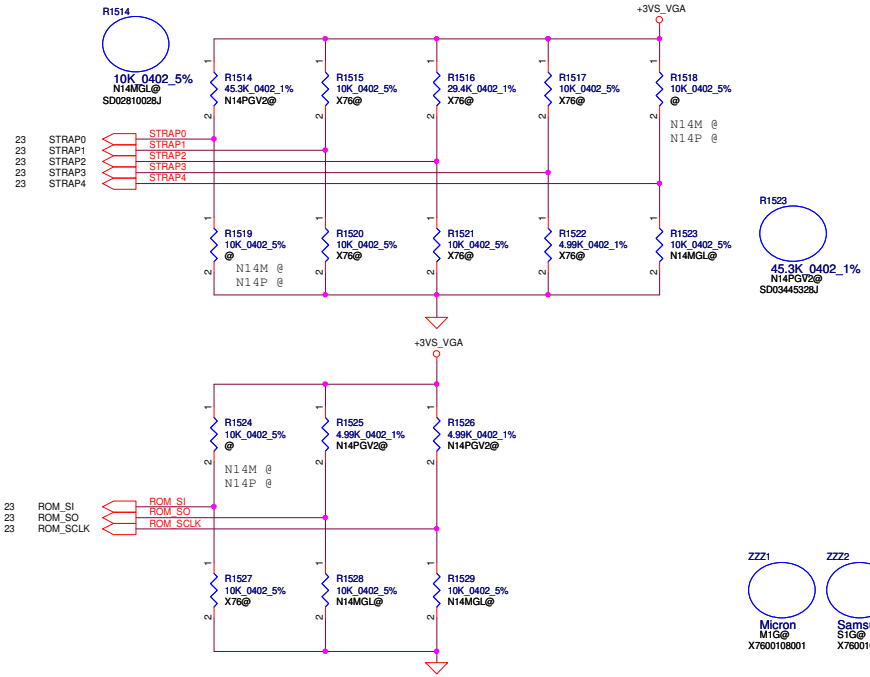
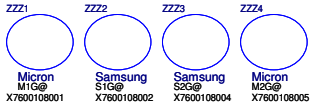




Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG[3:0]	
0110	Gen1/Gen2 support only
0000	Gen3 support

FB[1:0]	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

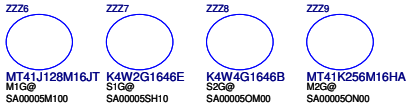
USER Straps	
User[3:0]	
1000-1100	Customer defined

PCIE_MAX_SPEED	
0	Limit booting to PCIE Gen1
1	Allow booting to PCIE Gen 2/3

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_SPEED_CHANGE_GEN3	
0	Disable PCIE Gen3 operation
1	Enable PCIE Gen3 operation

DP_PLL_VDD33V	
0	Reserved
1	Default



For N14P-GV2 QS Sample
ROM_SO change from PU 10K to PU 5K
ROM_SCLK change from PD 15K to PU 5K
STRAP1 change from PD 5K to PD 45K
STRAP2 change from PU 30K to PD 15K
STRAP4 change from PD 5K to PD 45K

GPU	FB Memory gDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N14P-GV2	Samsung 1000MHz	K4W2G1646E-BC1A 128Mx16	PU 5K	PU 5K	PD 45K	PU 45K	PD 45K	PD 15K	PD 5K	PD 45K
	Micron 1000MHz	MT41J128M16JT-093G 128Mx16	PU 5K	PU 5K	PD 30K	PU 45K	PD 45K	PD 15K	PD 5K	PD 45K
	Samsung 900MHz	K4W4G1646B-HC11 256Mx16	PU 5K	PU 5K	PD 20K	PU 45K	PD 45K	PD 15K	PD 5K	PD 45K
	Micron 900MHz	MT41K256M16HA-107G 256Mx16	PU 5K	PU 5K	PD 10K	PU 45K	PD 45K	PD 15K	PD 5K	PD 45K

GPU	FB Memory gDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N14M-GL	Samsung 1000MHz	K4W2G1646E-BC1A 128Mx16	PD 10K	PD 10K	PD 10K	PU 10K	PD 10K	PU 10K	PD 10K	PD 10K
	Hynix 1000MHz	H5TQ2G63DFR-N0C 128Mx16	PD 10K	PD 10K	PD 10K	PD 10K	PU 10K	PU 10K	PD 10K	PD 10K
	Micron 1000MHz	MT41J128M16JT-093G 128Mx16	PD 10K	PD 10K	PD 10K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K
	Samsung 900MHz	K4W4G1646B-HC11 256Mx16	PD 10K	PD 10K	PD 10K	PU 10K	PU 10K	PD 10K	PU 10K	PD 10K
	Hynix 900MHz	H5TQ4G63MFR-11C 256Mx16	PD 10K	PD 10K	PD 10K	PU 10K	PU 10K	PD 10K	PD 10K	PD 10K
	Micron 900MHz	MT41K256M16HA-107G 256Mx16	PD 10K	PD 10K	PD 10K	PU 10K	PD 10K	PU 10K	PU 10K	PD 10K

X76 X76

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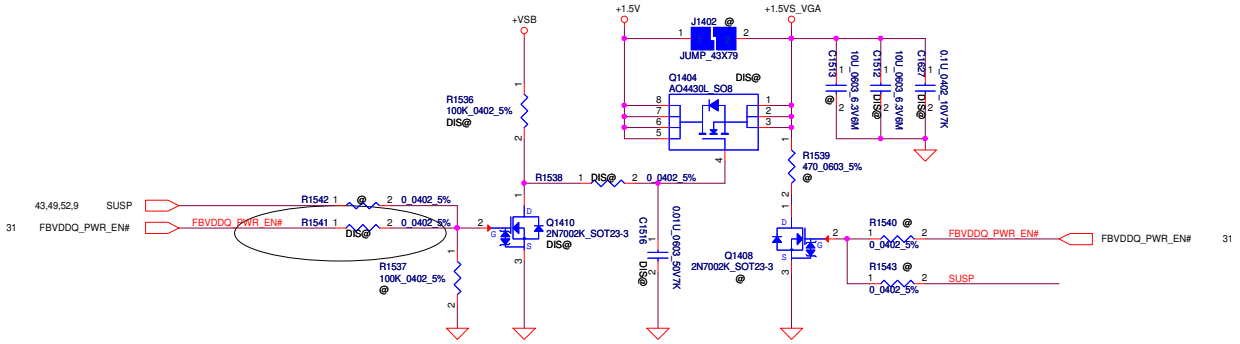
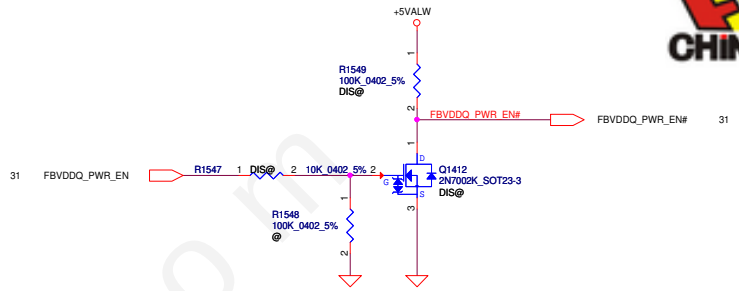
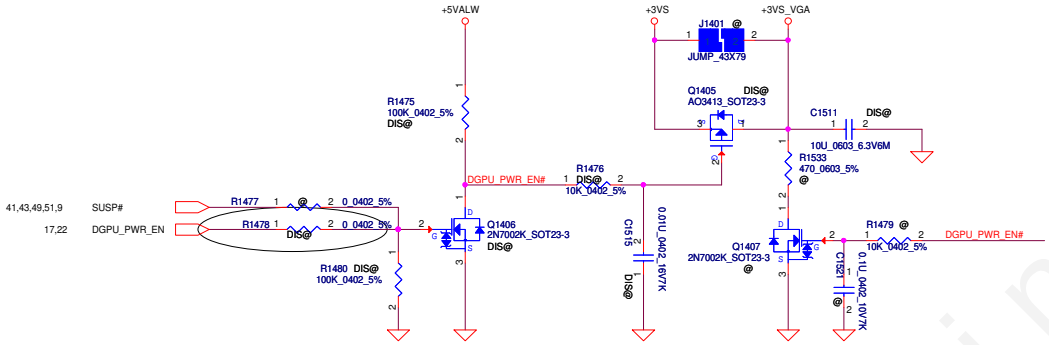
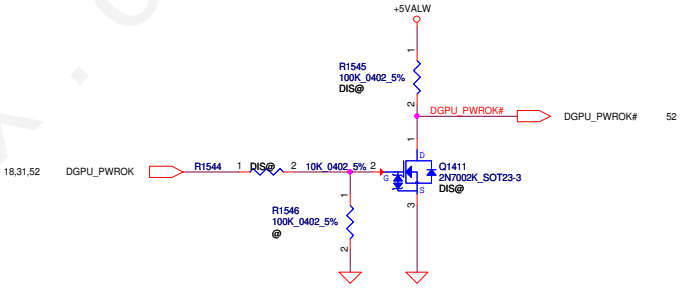
+1.5V to +1.5VS_VGA

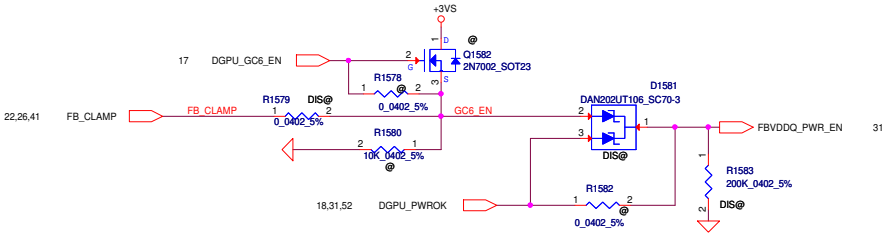




+3VS to +3VS_VGA







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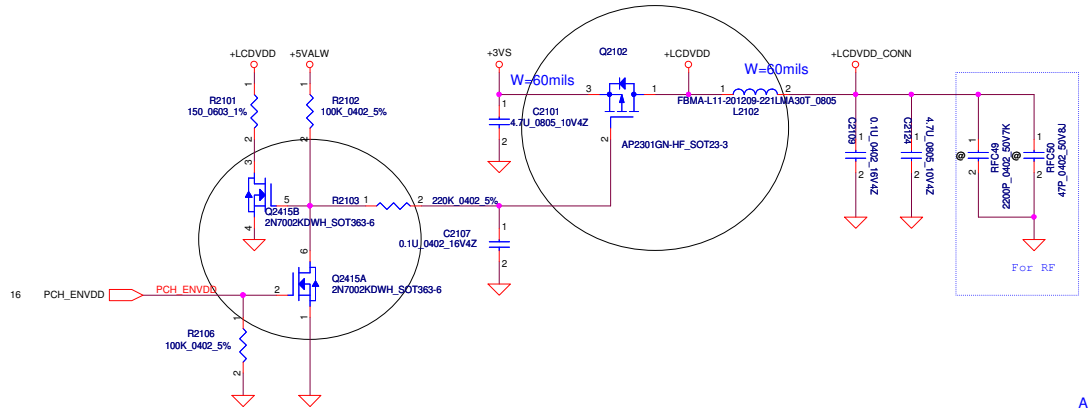
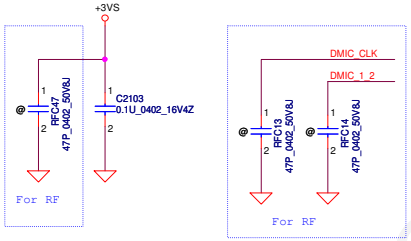
LCD POWER CIRCUIT

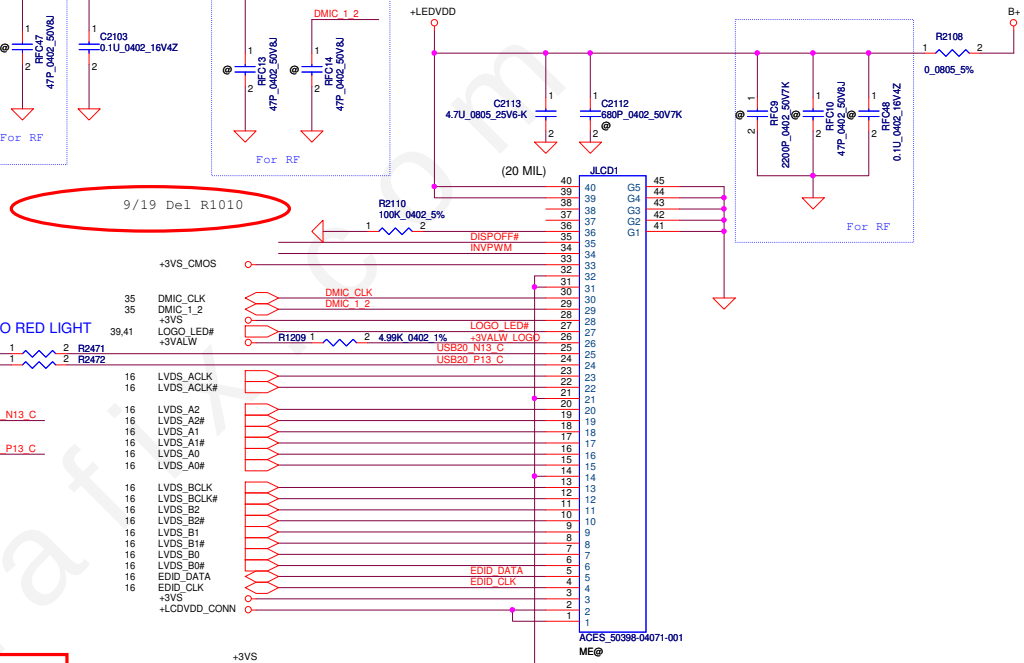


Place closed to JLVDS1



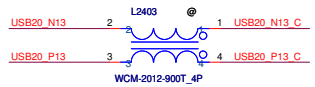
LCD/LED PANEL Conn.

PN:SP01000XE00



A LOGO RED LIGHT

CMOS



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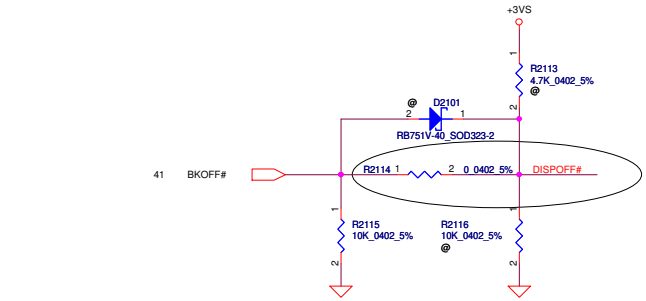
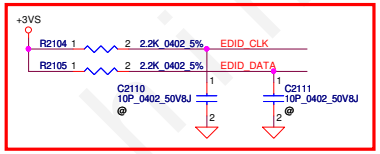
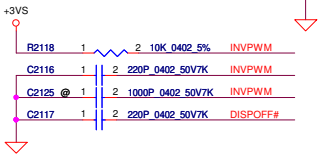
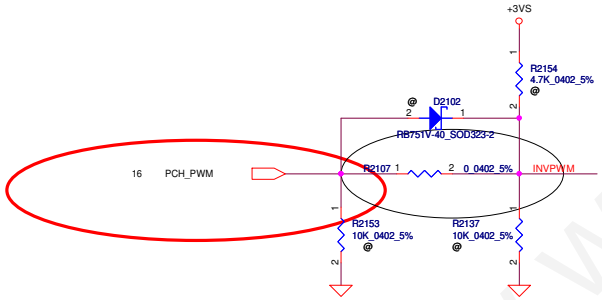
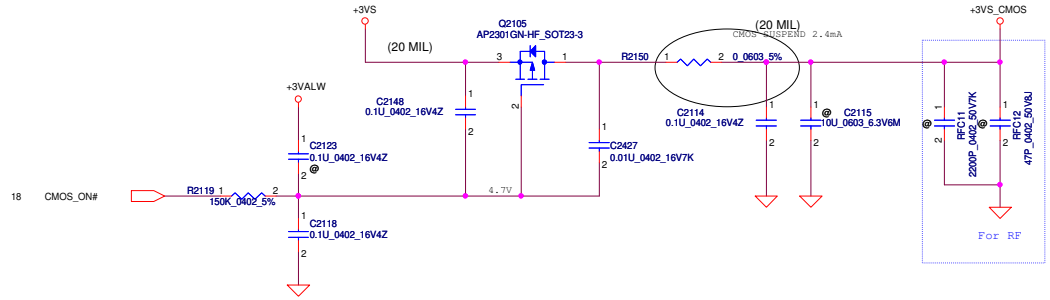








CMOS Camera Conn



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Title: LVDS CONN.

Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Saturday, November 03, 2012 | Sheet 32 of 59

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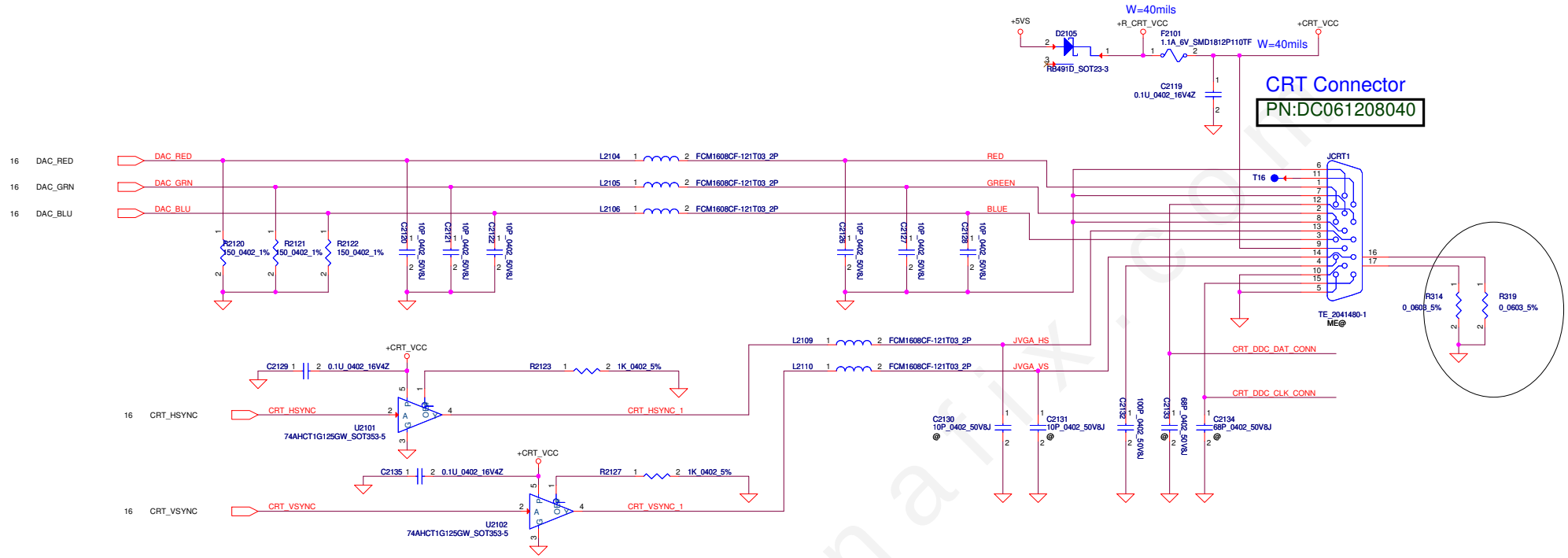

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Title: CRT CONN.

Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Thursday, November 01, 2012 | Sheet 33 of 59

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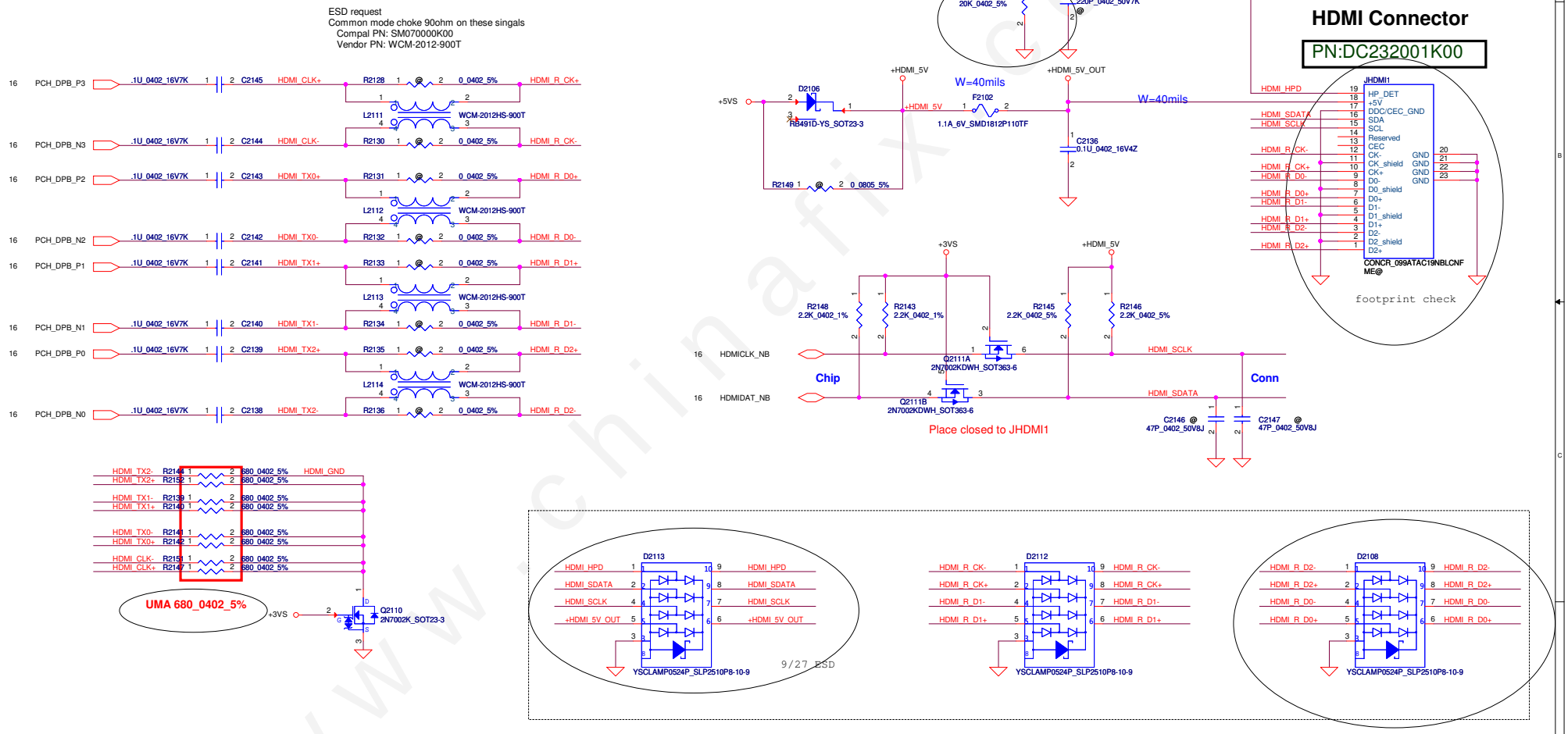

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Title: HDMI CONN.

Size: Custom | Document Number: NM-A041 | Rev: 1.A

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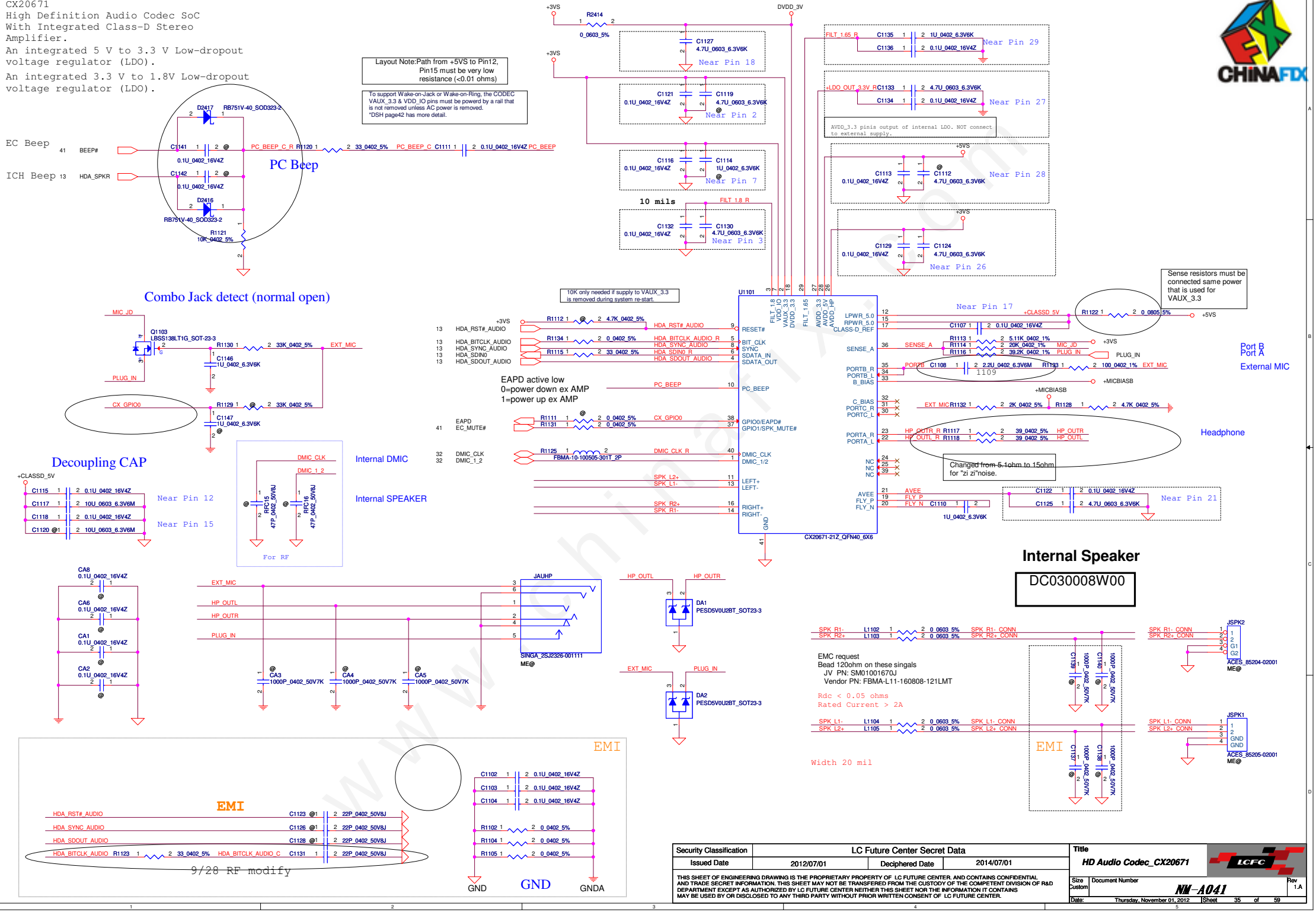
CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

Layout Note:Path from +5VS to Pin12, Pin15 must be very low resistance (<0.01 ohms)

To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 & VDD_IO pins must be powerd by a rail that is not removed unless AC power is removed.
*DSH page42 has more detail.



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Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title: HD Audio Codec_CX20671

Size: Custom | Document Number: NM-A041 | Rev: 1.A

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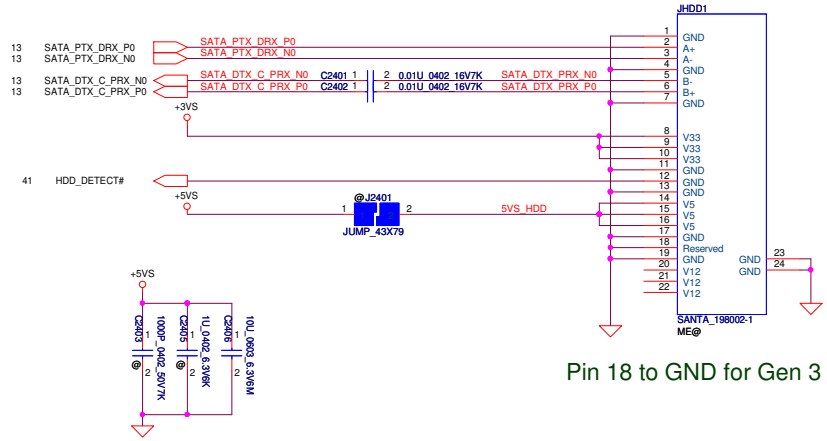
SATA HDD CONN.

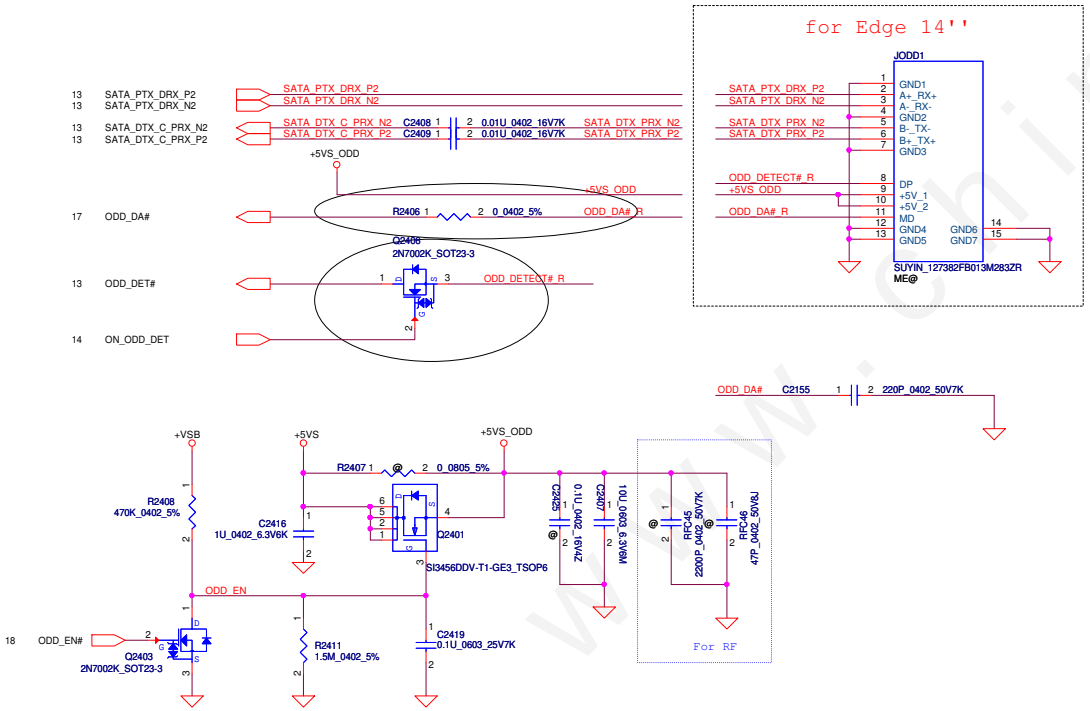
PN:SP01001HE00



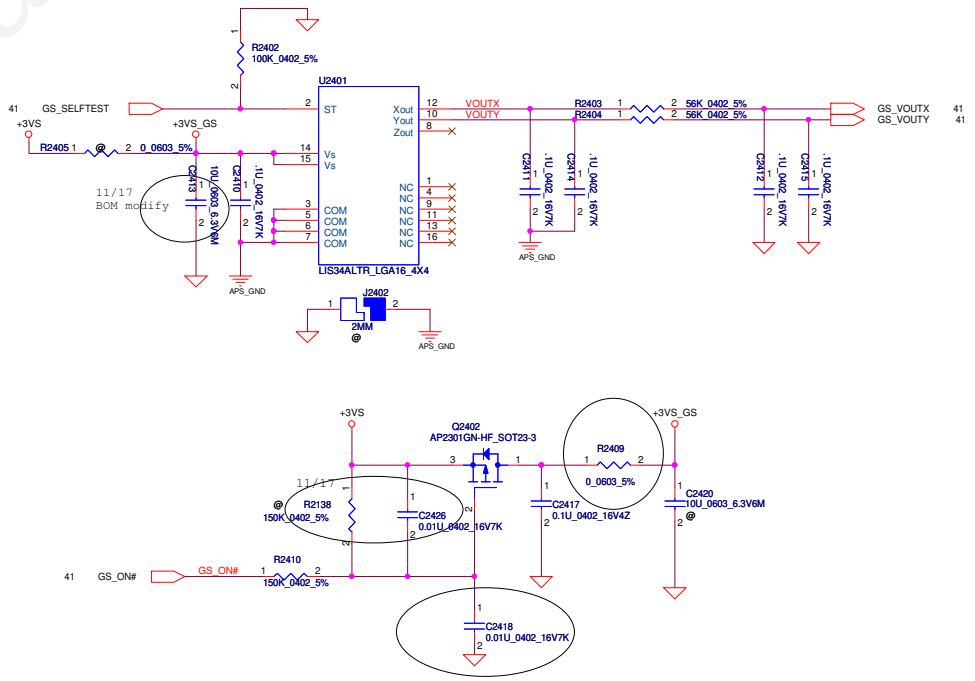
Pin 18 to GND for Gen 3

SATA ODD CONN.

PN:SP01000TU10



APS G-Sensor



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Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title: HDD/ODD/Card reader/G-Sen

Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Thursday, November 01, 2012 | Sheet 36 of 59

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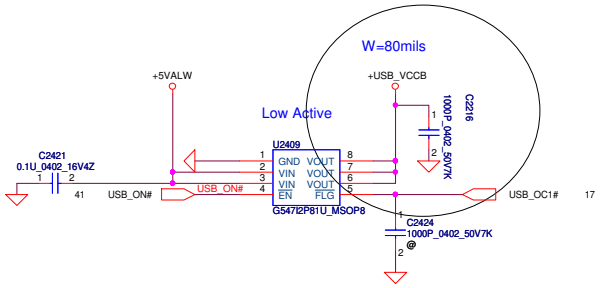
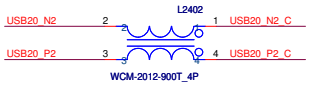
USB 3.0 Conn.





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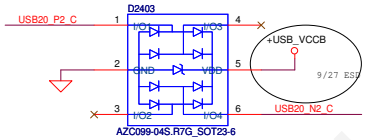
PN: SM070001S00 x 2



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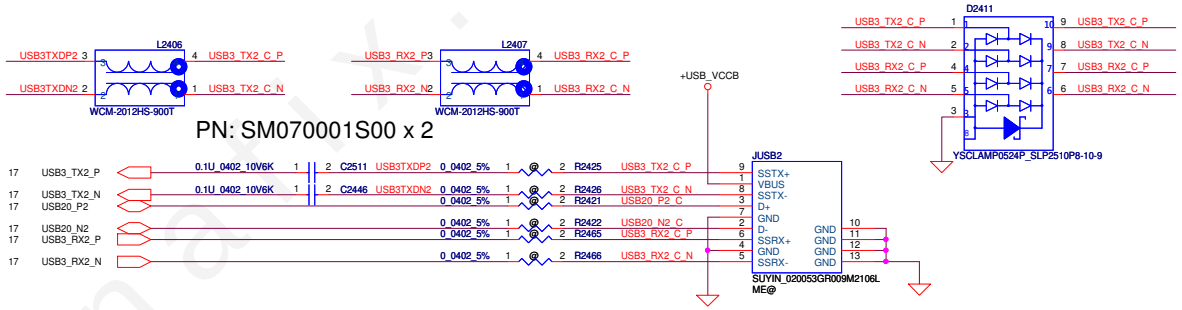

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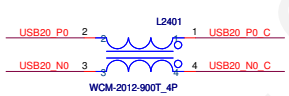

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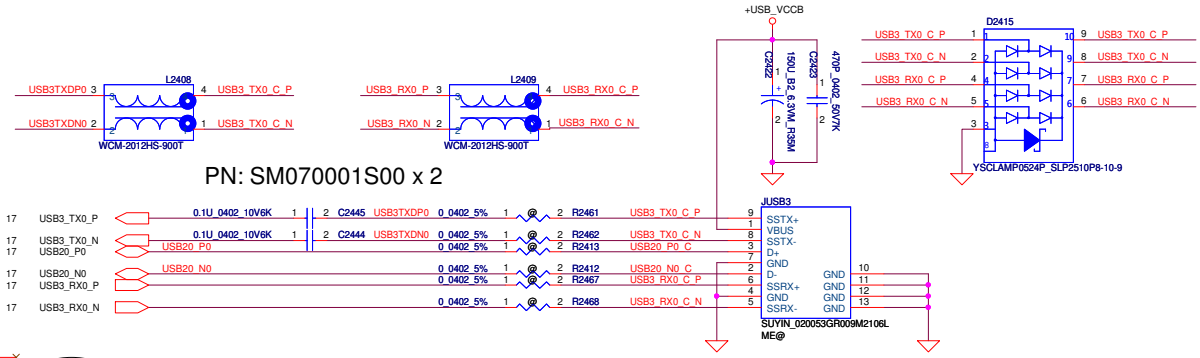
PN: SM070001S00 x 2



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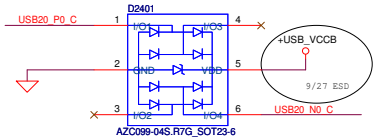

PN: SC300001G00

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Title: USB 3.0 CONN.

Size: Custom | Document Number: NM-A041 | Rev: 1.A

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Mini-Express Card for WLAN(Half)

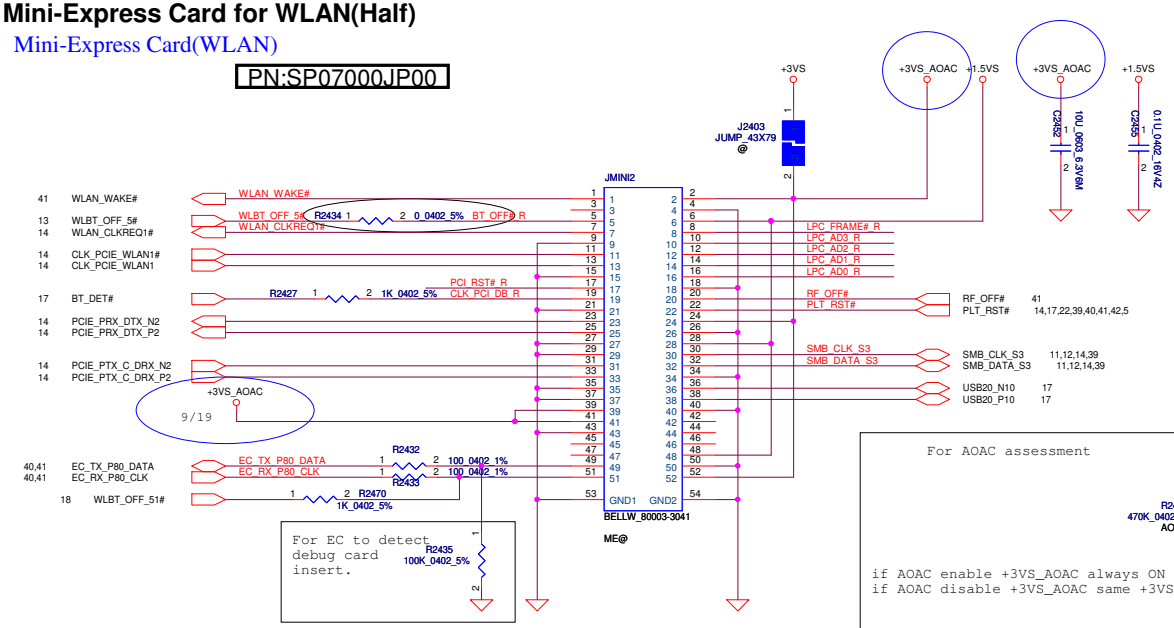
Mini-Express Card(WLAN)

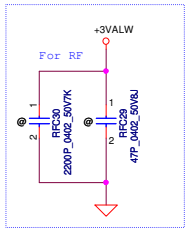
PN:SP07000JP00

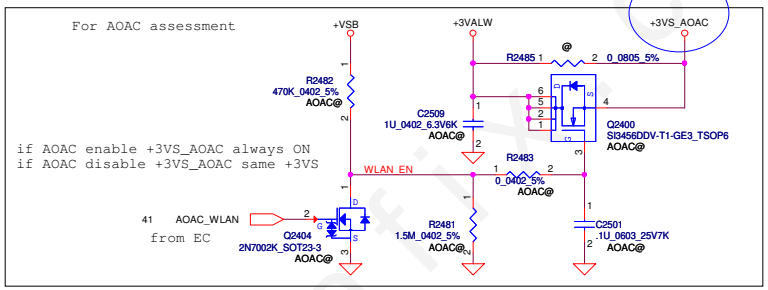
BT Connector

Mini Card Power Rating

Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



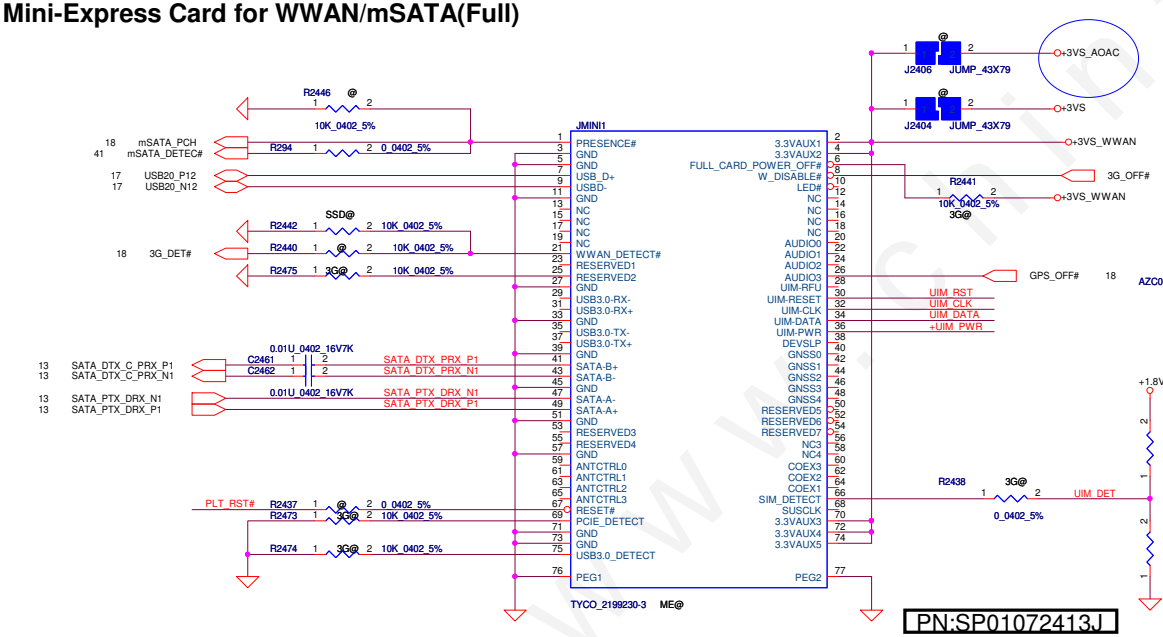




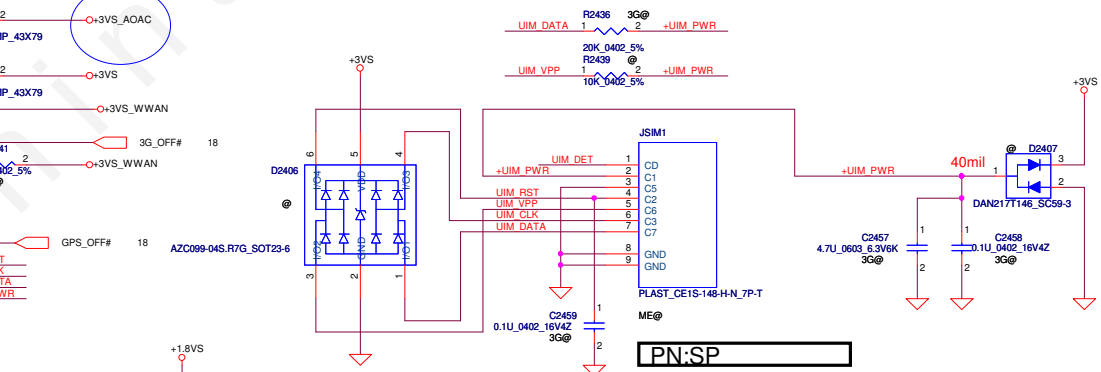
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R2449	0_0402_5%	LPC_FRAME#	LPC_FRAME#	13,40,41
LPC_AD3 R	R2455	0_0402_5%	LPC_AD3	LPC_AD3	13,40,41
LPC_AD2 R	R2456	0_0402_5%	LPC_AD2	LPC_AD2	13,40,41
LPC_AD1 R	R2457	0_0402_5%	LPC_AD1	LPC_AD1	13,40,41
LPC_AD0 R	R2458	0_0402_5%	LPC_AD0	LPC_AD0	13,40,41
PCI_RST# R	R2459	0_0402_5%	PLT_RST#		
CLK_PCI_DB_R	R2428	0_0402_5%	CLK_PCI_DB	CLK_PCI_DB	17,40

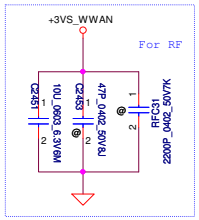
Mini-Express Card for WWAN/mSATA(Full)



PN:SP01072413J



PN:SP



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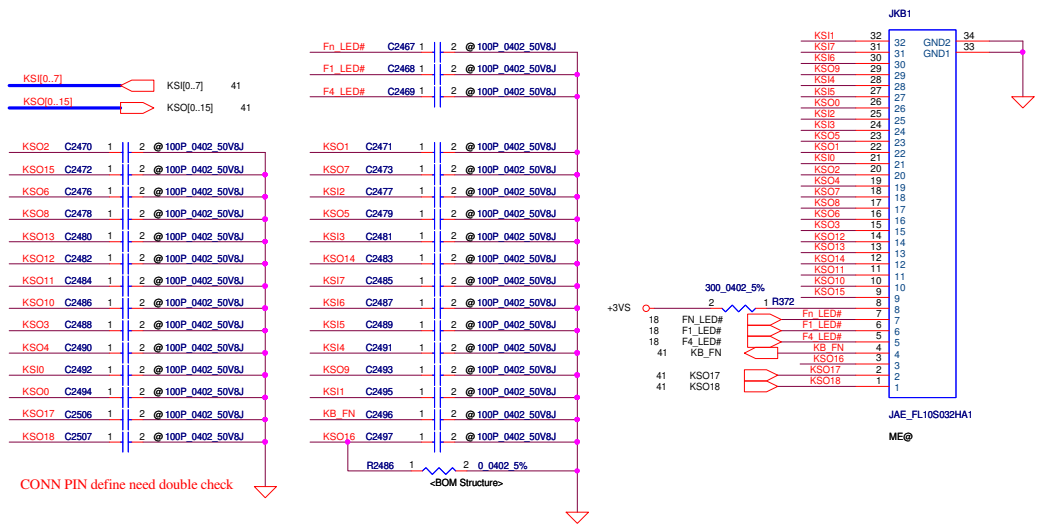
Title: PCIe-WLAN and WWAN_mSATA

Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Thursday, November 01, 2012 | Sheet 38 of 59

INT_KBD Conn.

PN:SP011208010



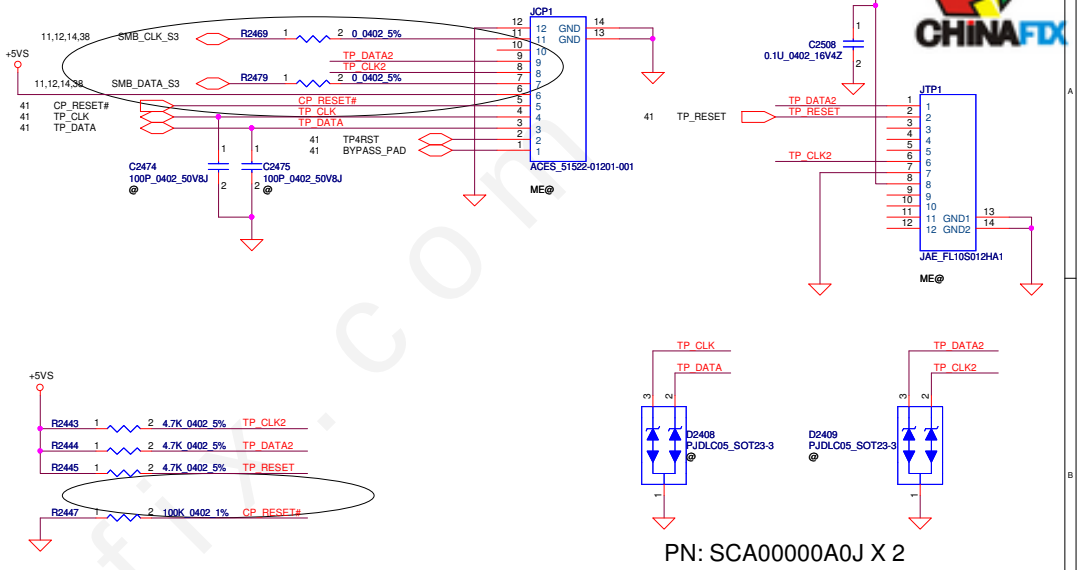
CONN PIN define need double check

Click pad

PN:SP01001BX00

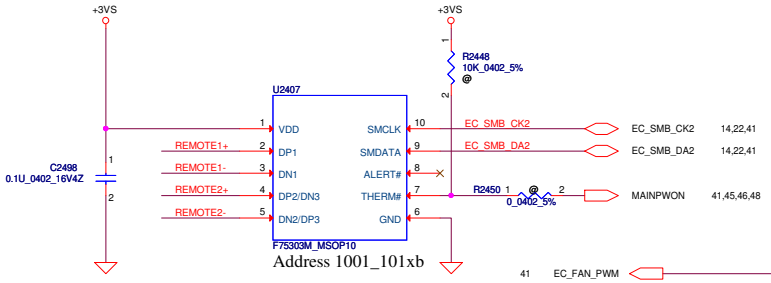
Track point

PN:SP01120802K



PN: SCA00000A0J X 2

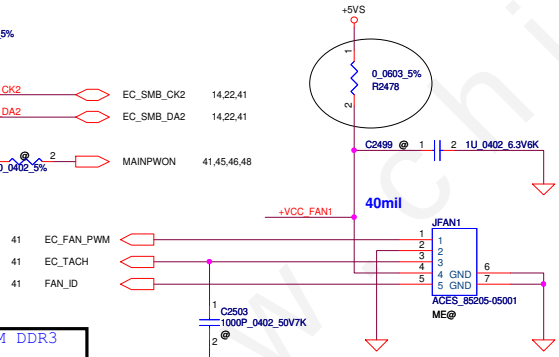
Fintek thermal sensor placed near by TOP DDR3



Address 1001_101xb

2nd source
SA000029210-->EMC1403-2-AIZL-TR

FAN CONN.



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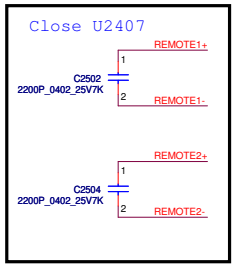
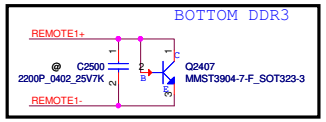
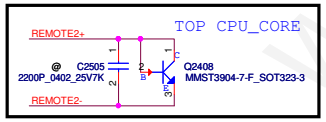
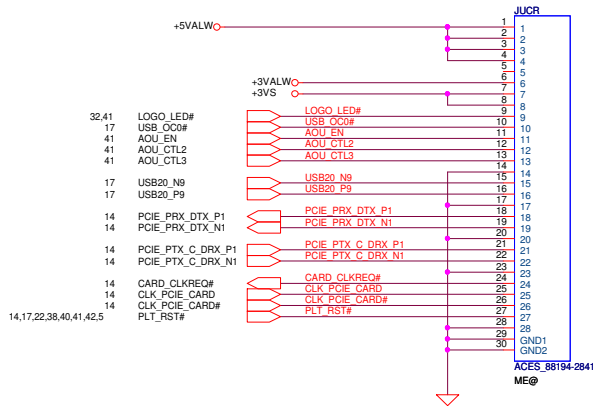






REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

Audio+CR Board



need change to 28 Pin

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Title: KB/TP/Thermal Sensor/Audio

Size: Custom | Document Number: NM-A041 | Rev: 1.A

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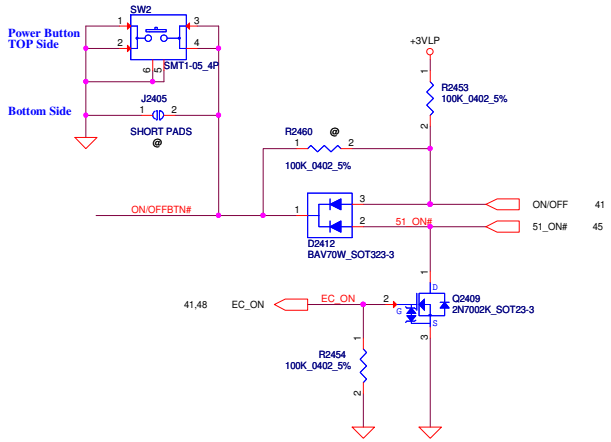
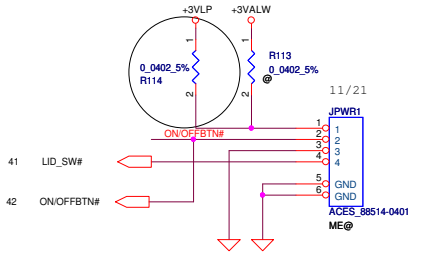
Power Button

ON/OFF switch



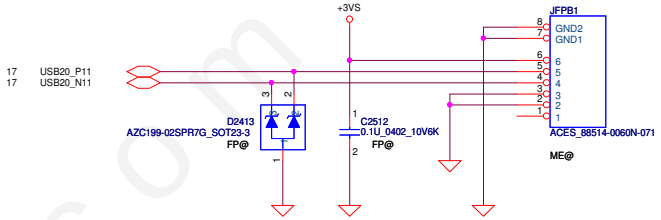
Power Button CONN.

PN:SP01000R400

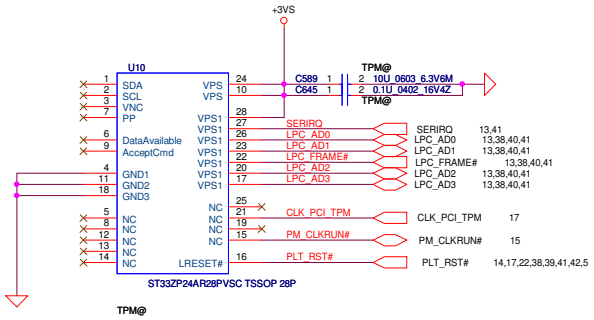


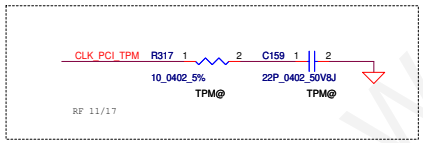
Finger Print Board

PN:SP01000R400

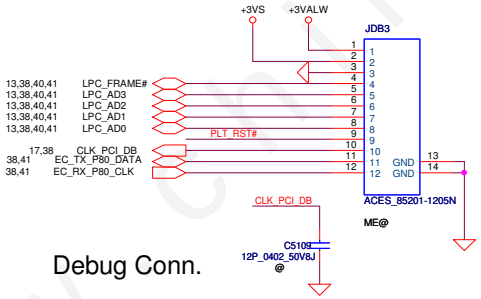


TPM

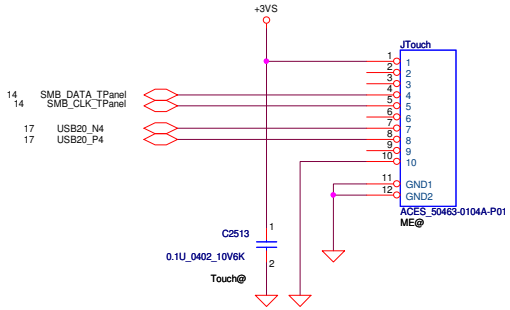




Debug Conn.



Touch Panel



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Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title: PWR S/B/LID SW/TPM/RJ45

Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Wednesday, November 07, 2012 | Sheet 40 of 59

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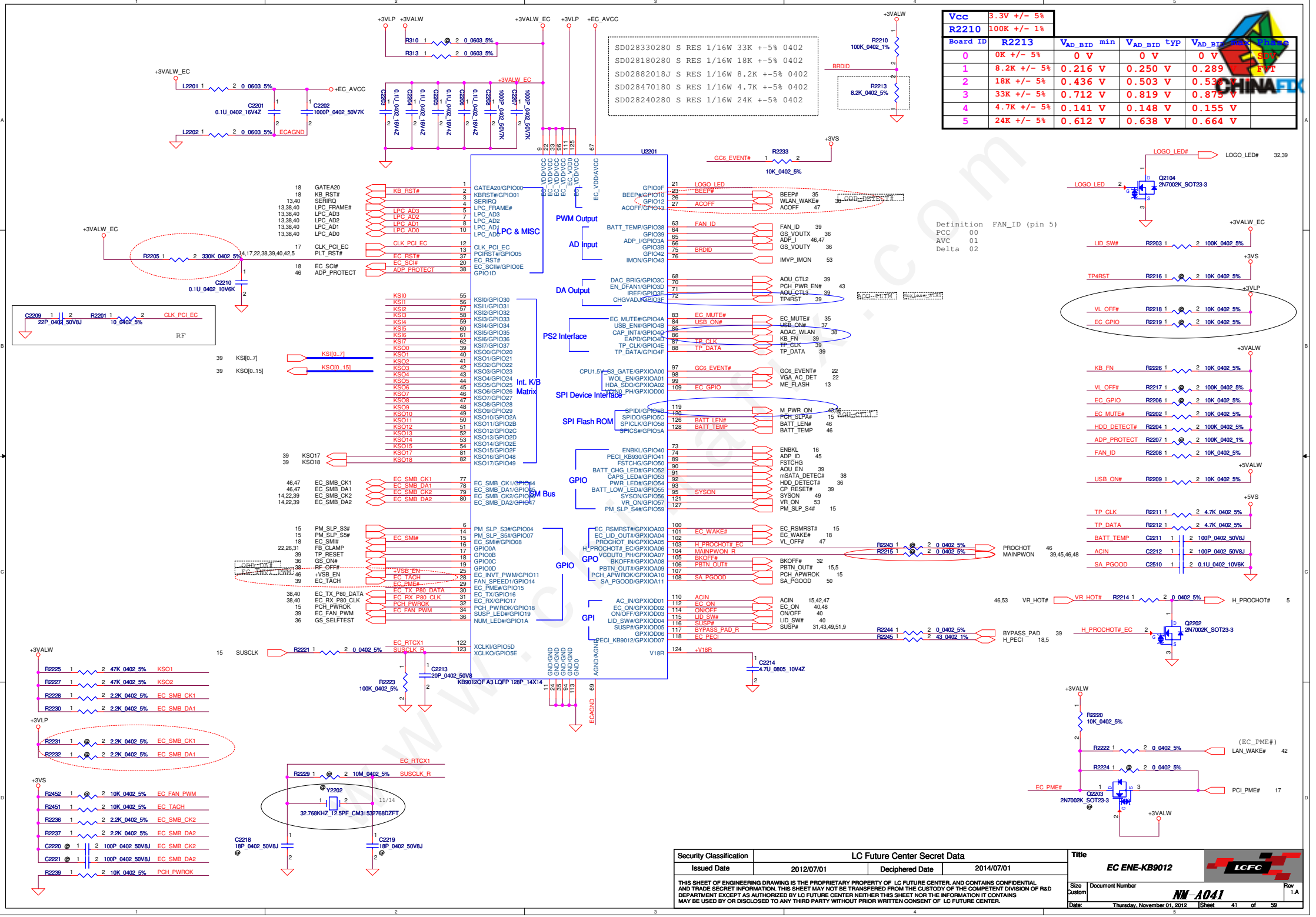

Vcc	3.3V +/- 5%				
R2210	100K +/- 1%				
Board ID	R2213	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289	FVT
2	18K +/- 5%	0.436 V	0.503 V	0.538	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	

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Issued Date	2012/07/01	Deciphered Date	2014/07/01

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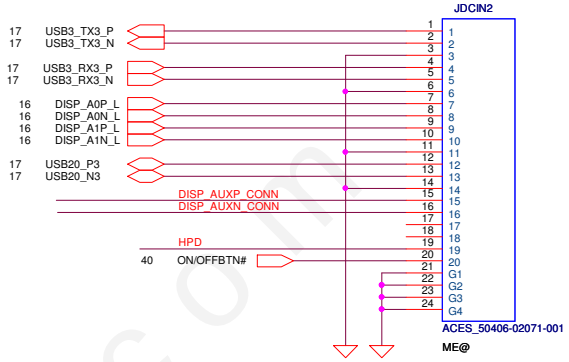
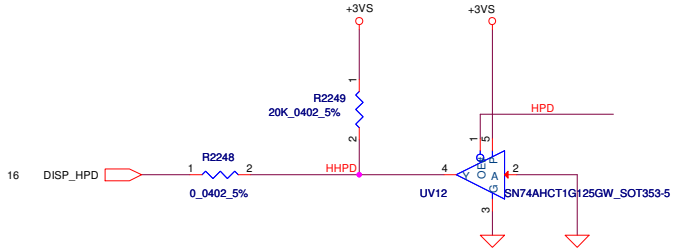
Title: EC ENE-KB9012

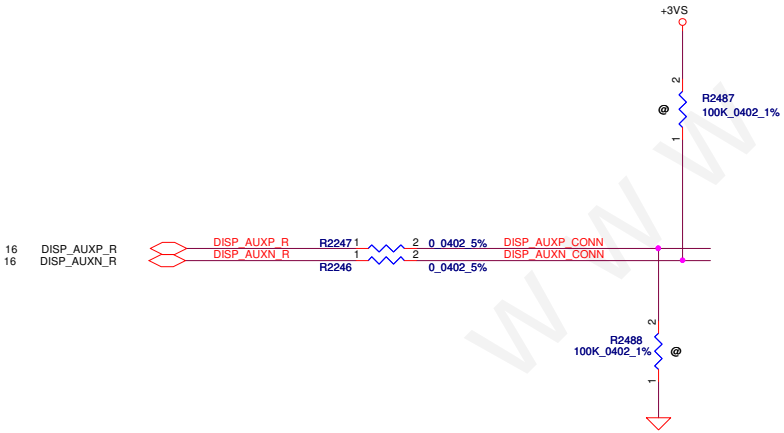
Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Thursday, November 01, 2012 | Sheet 41 of 59

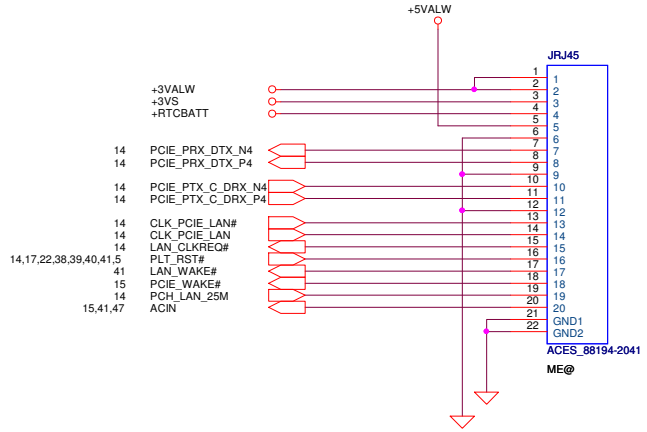




DP/TMDS Switch Circuit (1)



RJ45 Board



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Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title: DP U3 CONN.

Size: Custom | Document Number: NW-A041 | Rev: 1.A

Date: Thursday, November 01, 2012 | Sheet 42 of 59

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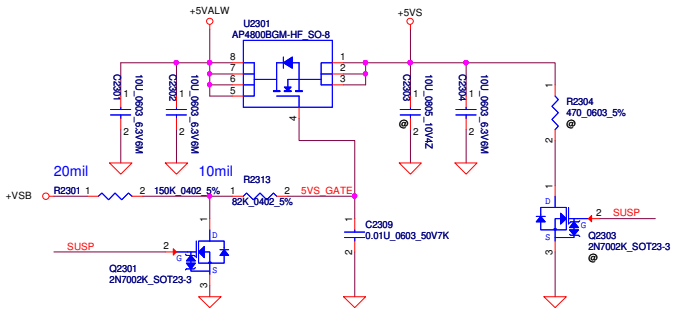
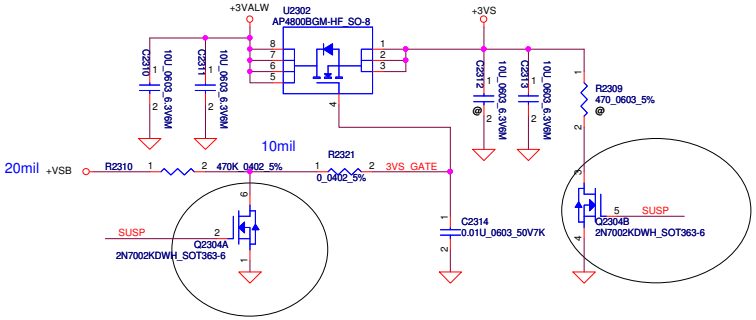
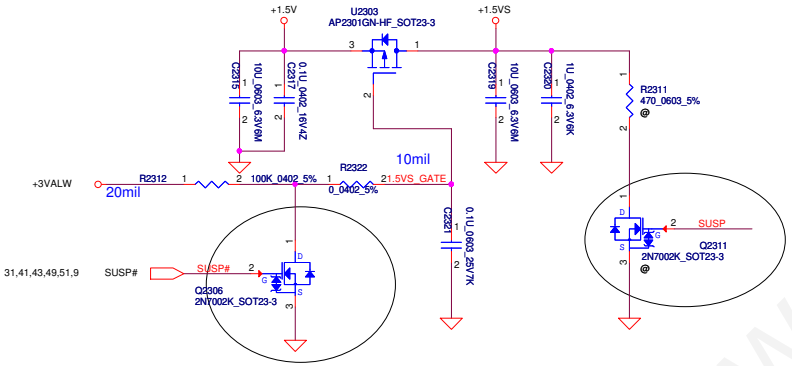
+5VALW TO +5VS

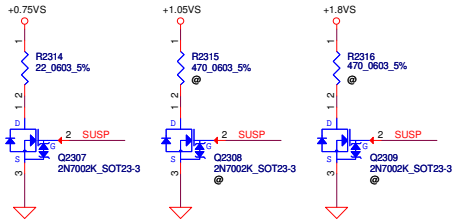


+3VALW TO +3VS



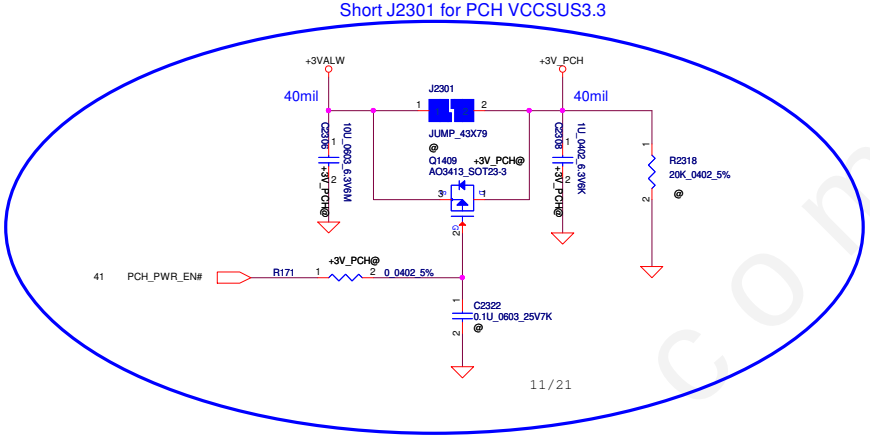
+1.5V to +1.5VS

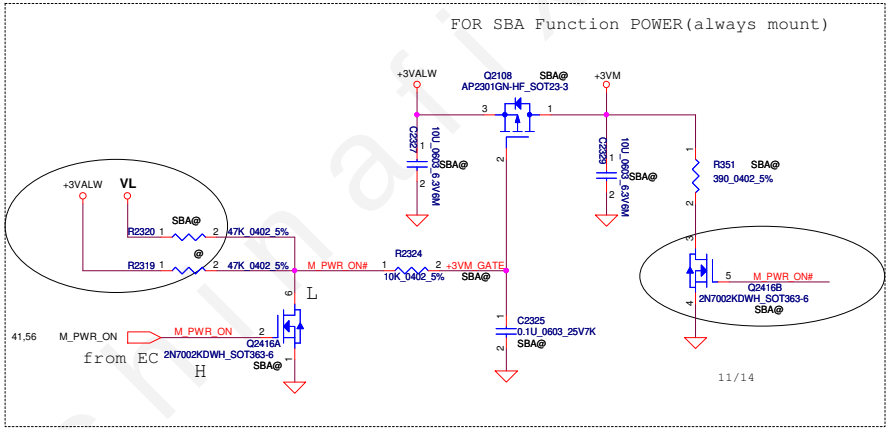


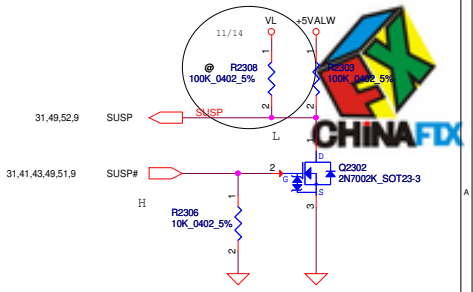


+3VALW TO +3VALW(PCH AUX Power)

Short J2301 for PCH VCCSUS3.3







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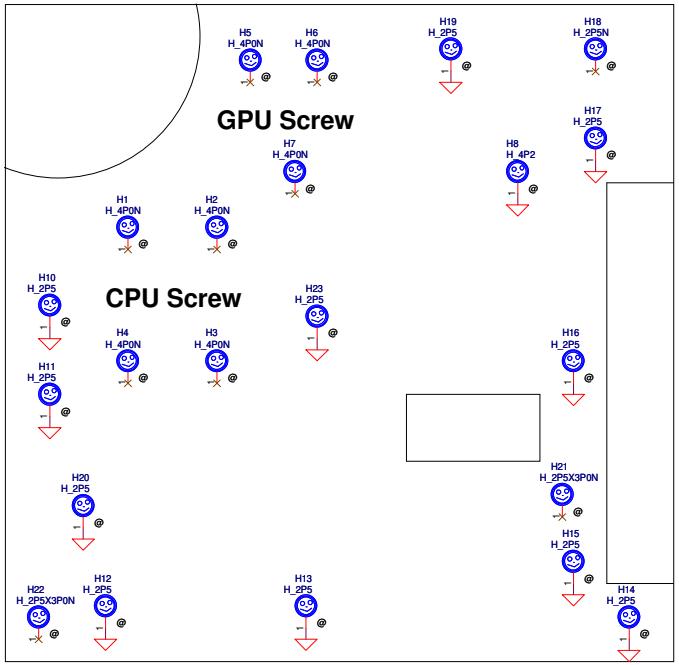
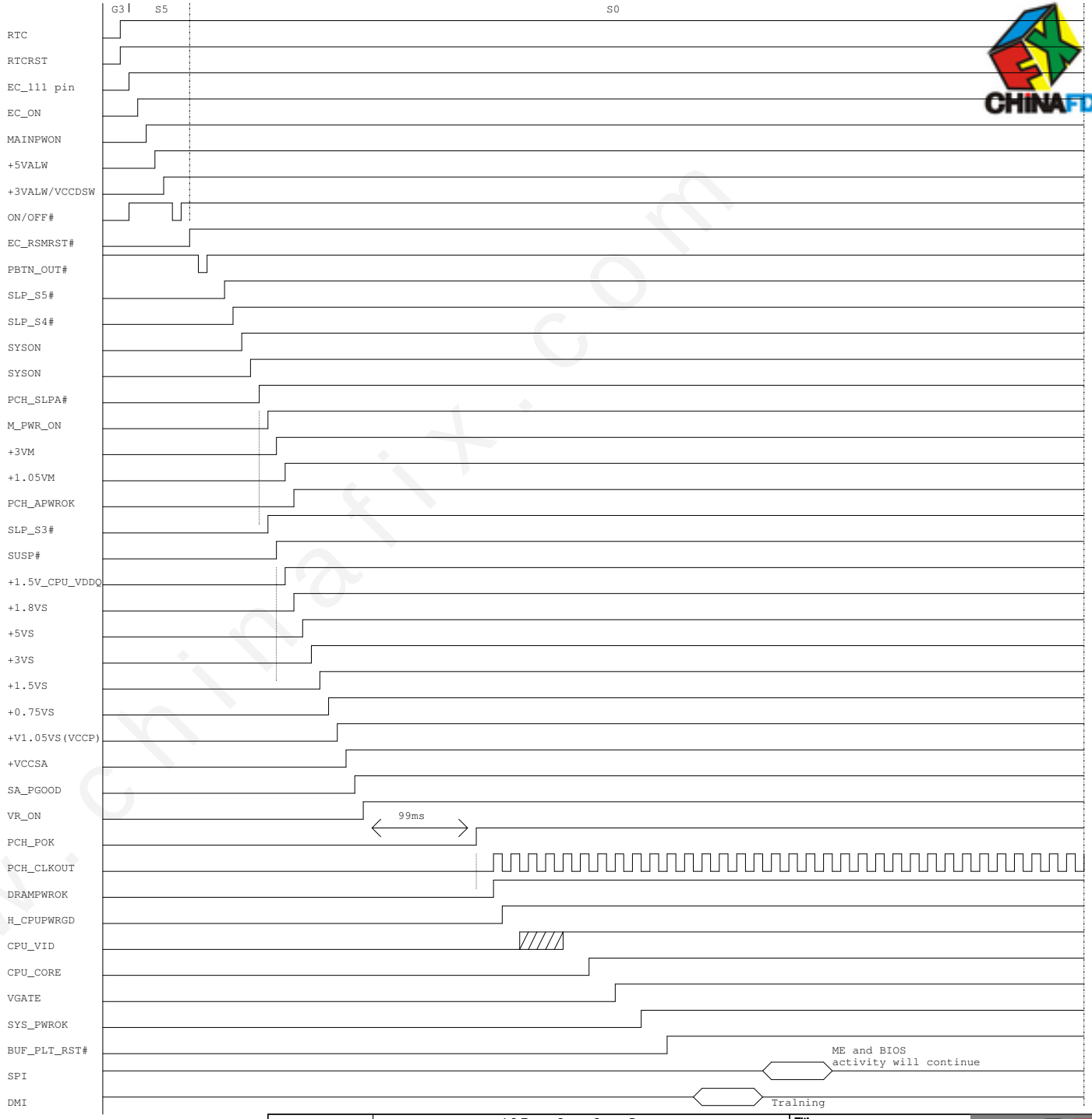
Title: DC INTERFACE

Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Thursday, November 01, 2012 | Sheet 43 of 59

Screw Hole & FD





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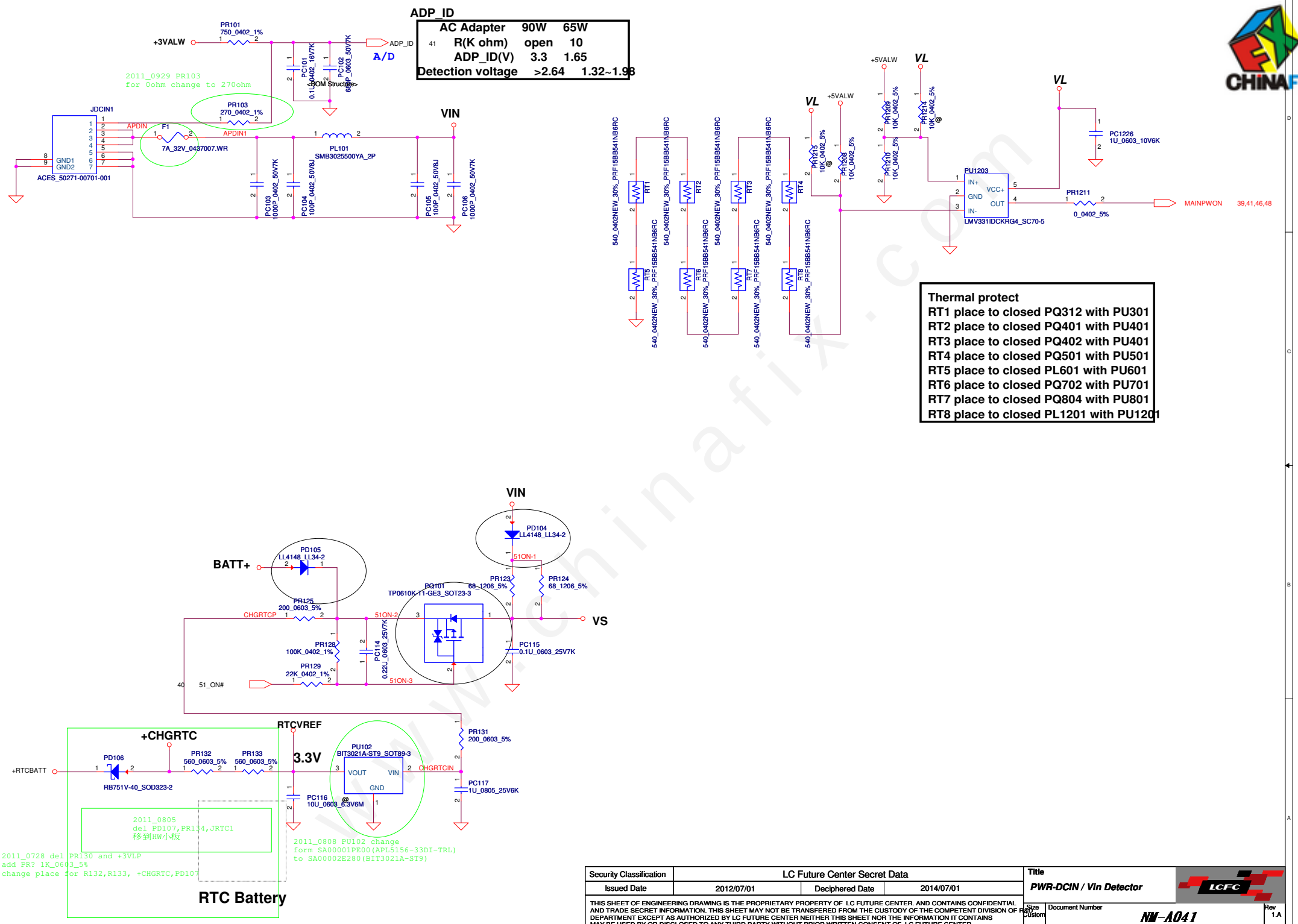
Title: Screw Hole

Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Monday, November 05, 2012 | Sheet 44 of 59



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title: PWR-DCIN / Vin Detector

Size: Custom | Document Number: NW-A041 | Rev: 1.A

Date: Thursday, November 01, 2012 | Sheet 45 of 59

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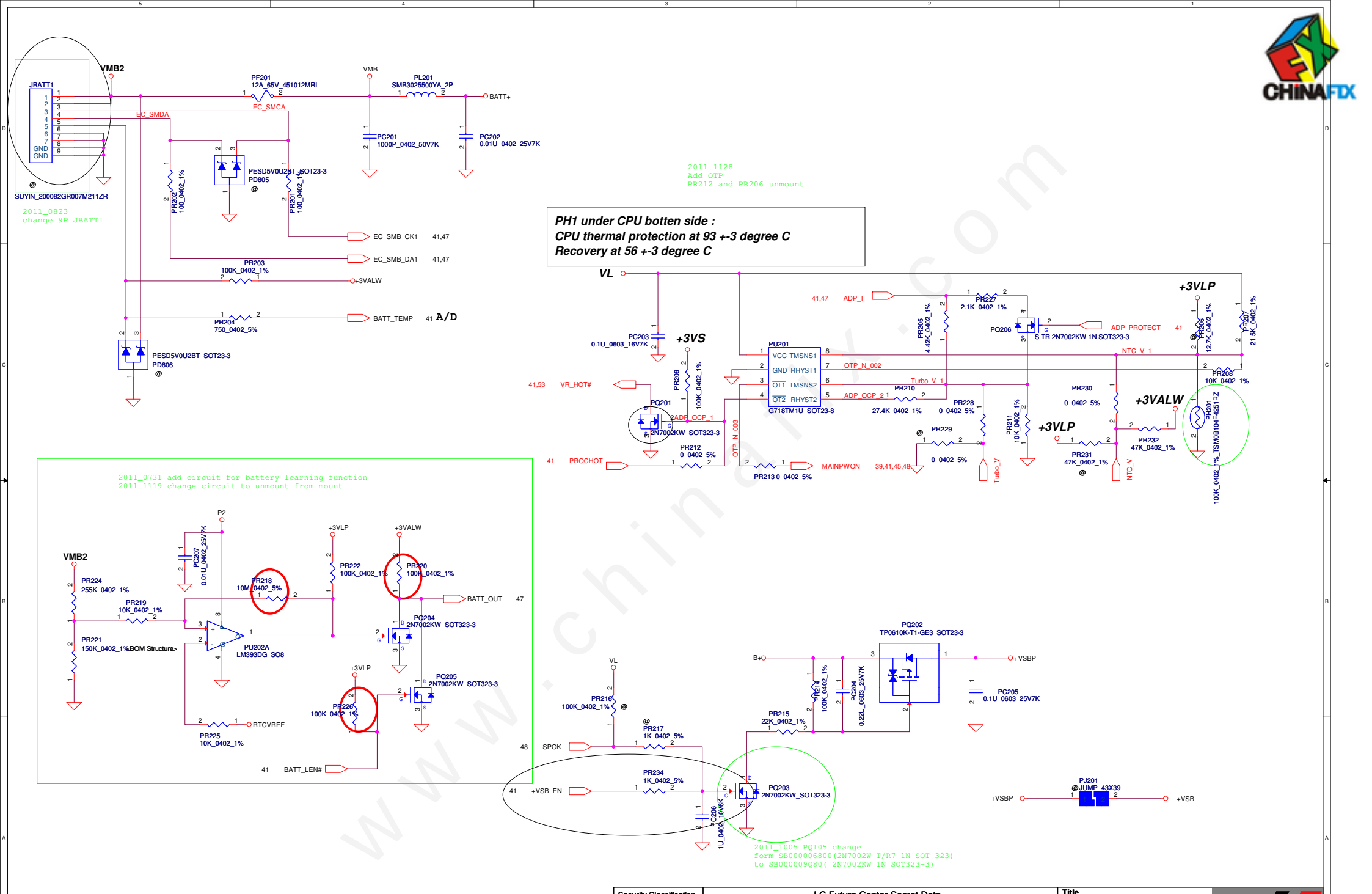

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: NW-A041 | Rev: 1.A

Date: Thursday, November 01, 2012 | Sheet 46 of 59

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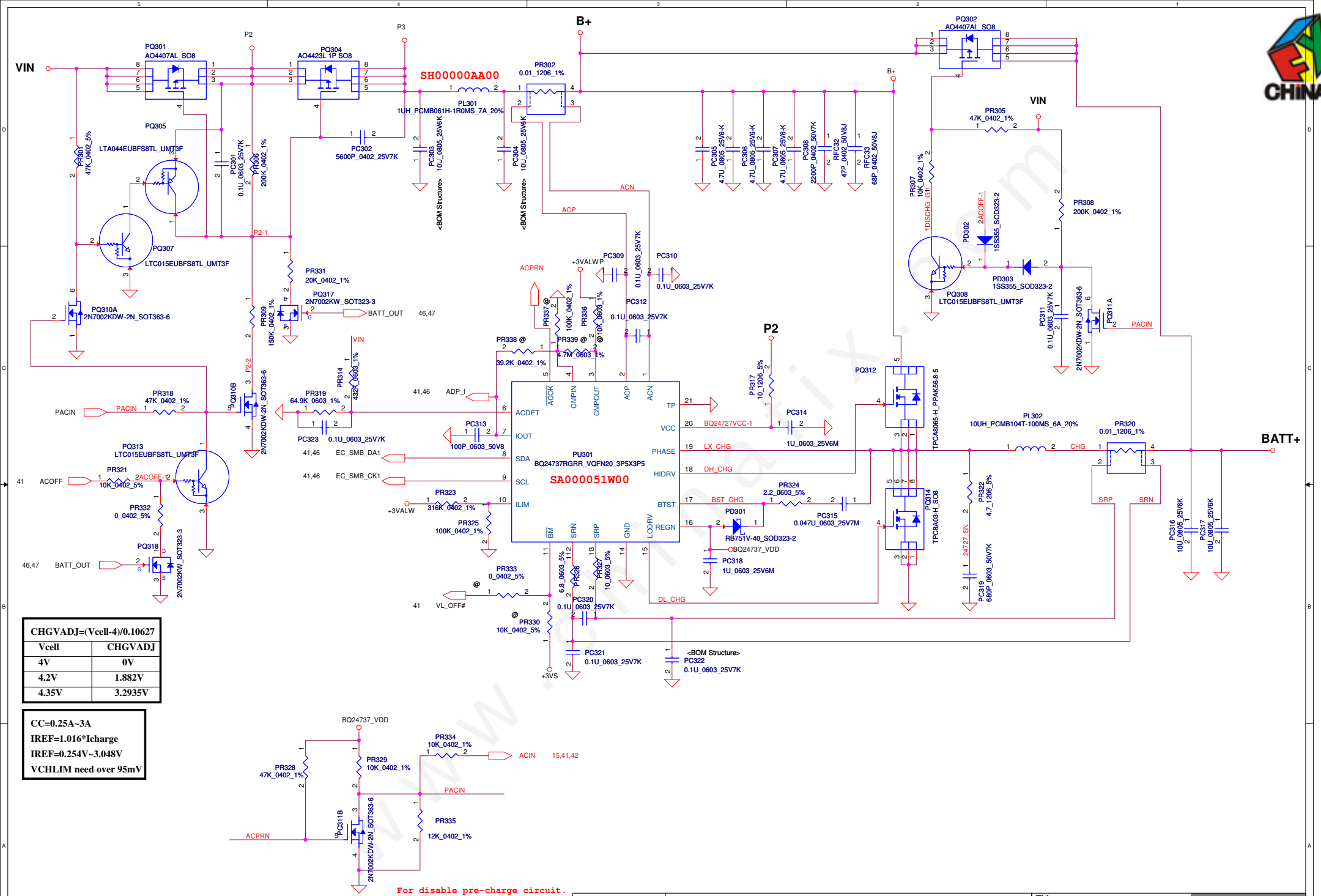

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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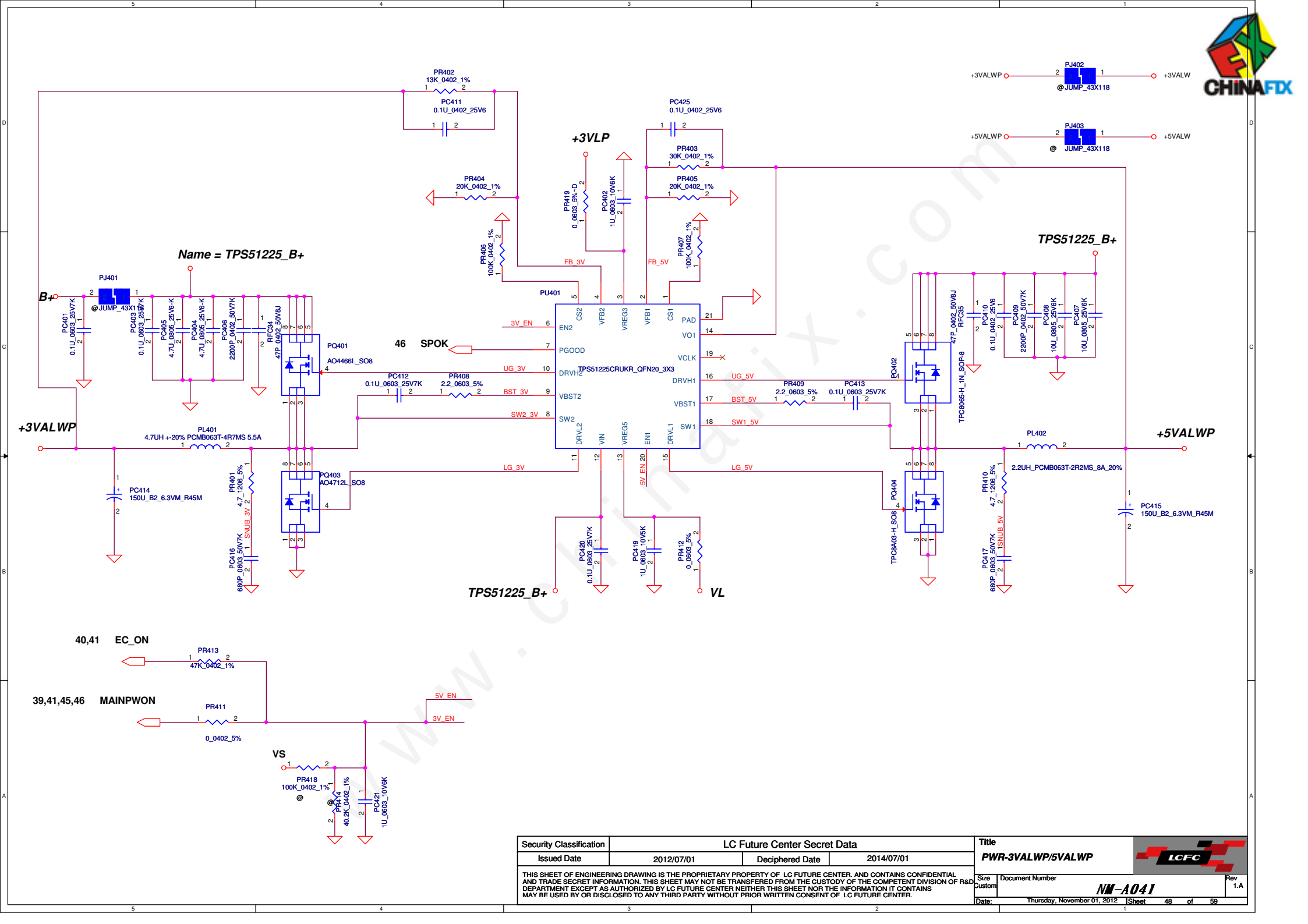
Title: PWR-CHARGER-BQ24737

Size: Custom | Document Number: NW-A041 | Rev: 1.A

Date: Thursday, November 01, 2012 | Sheet 47 of 59



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title: PWR-3VALWP/5VALWP

Size: Custom | Document Number: NM-A041 | Rev: 1.A

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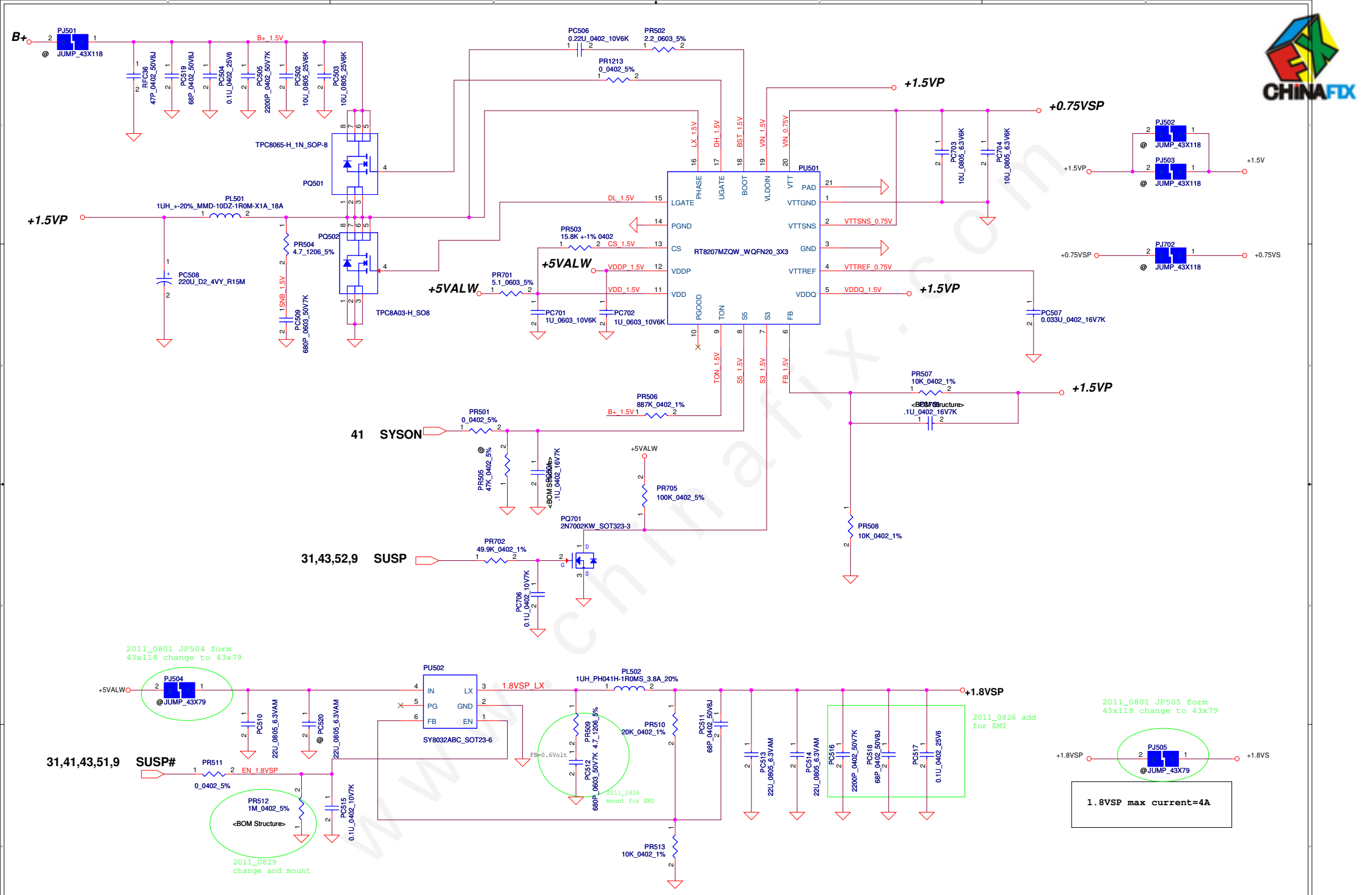
B+
PJ501
JUMP_43X118
B+_1.5V
PC506 0.22U_0402_10V6K
PR502 2.2_0603_5%
PR1213 0_0402_5%
+1.5VP
+0.75VSP
PJ502 JUMP_43X118
PJ503 JUMP_43X118
+1.5V
+0.75VS
PJ702 JUMP_43X118
TPC8065-H_1N_SOP-8
PQ501
PQ502
TPC8A03-H_SO8
PL501 1UH_+-20%_MMD-10DZ-1R0M-X1A_18A
PR504 4.7_1206_5%
PC508 220U_D2_4VY_R15M
PC509 680P_0603_50V7K
PR503 15.8K +-1% 0402
+5VALW
PR701 5.1_0603_5%
PC701 1U_0603_10V6K
PC702 1U_0603_10V6K
PU501
RT8207MZQW_WQFN20_3X3
PC703 10U_0805_6.3V6K
PC704 10U_0805_6.3V6K
PC507 0.033U_0402_16V7K
PR507 10K_0402_1%
PR506 887K_0402_1%
PR501 0_0402_5%
41 SYSON
PR505 47K_0402_5%
PR705 100K_0402_5%
PQ701 2N7002KW_SOT323-3
PR508 10K_0402_1%
PR702 49.9K_0402_1%
31,43,52,9 SUSP
PC706 0.1U_0402_10V7K
2011_0801 JP504 form 43x118 change to 43x79
PJ504 @JUMP_43X79
PU502
SY8032ABC_SOT23-6
1.8VSP_LX
PL502 1UH_PH041H-1R0MS_3.8A_20%
+1.8VSP
PR510 20K_0402_1%
PR509 4.7_1206_5%
PC512 680P_0603_50V7K
2011_0826 mount for EMI
2011_0826 add for EMI
PC510 22U_0805_6.3VAM
PC520 22U_0805_6.3VAM
PC511 68P_0402_50V8J
PC513 22U_0805_6.3VAM
PC514 22U_0805_6.3VAM
PC516 2200P_0402_50V7K
PC518 68P_0402_50V8J
PC517 0.1U_0402_25V6
31,41,43,51,9 SUSP#
PR511 0_0402_5%
EN_1.8VSP
PR512 1M_0402_5%
<BOM Structure>
PC515 0.1U_0402_10V7K
2011_0829 change and mount
PR513 10K_0402_1%
2011_0801 JP505 form 43x118 change to 43x79
PJ505 @JUMP_43X79
1.8VSP max current=4A
Security Classification
LC Future Center Secret Data
Issued Date
2012/07/01
Deciphered Date
2014/07/01
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Title
PWR-+1.5VP/+1.8VSP
Size Custom
Document Number
NM-A041
Rev 1.A
Date: Thursday, November 01, 2012
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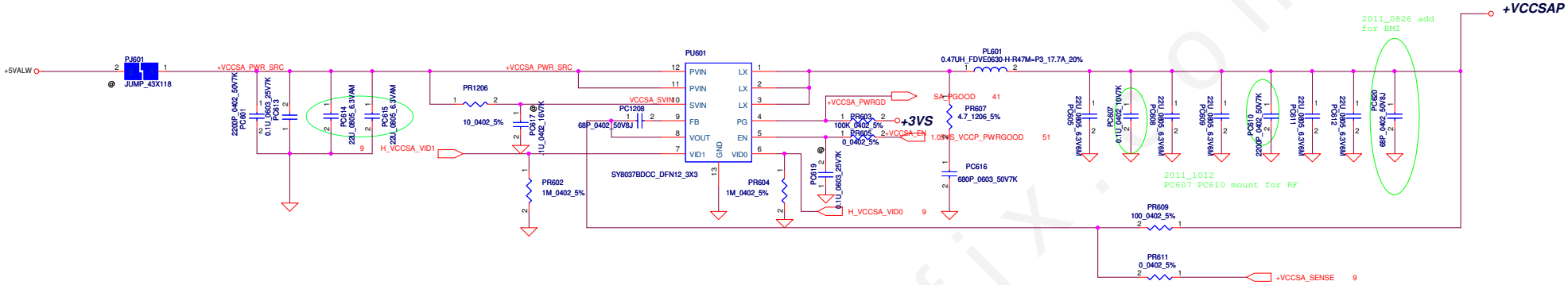
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

+VCCSAP — PJ602 JUMP_43X118 — +VCCSA

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



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Issued Date	2012/07/01	Deciphered Date	2014/07/01

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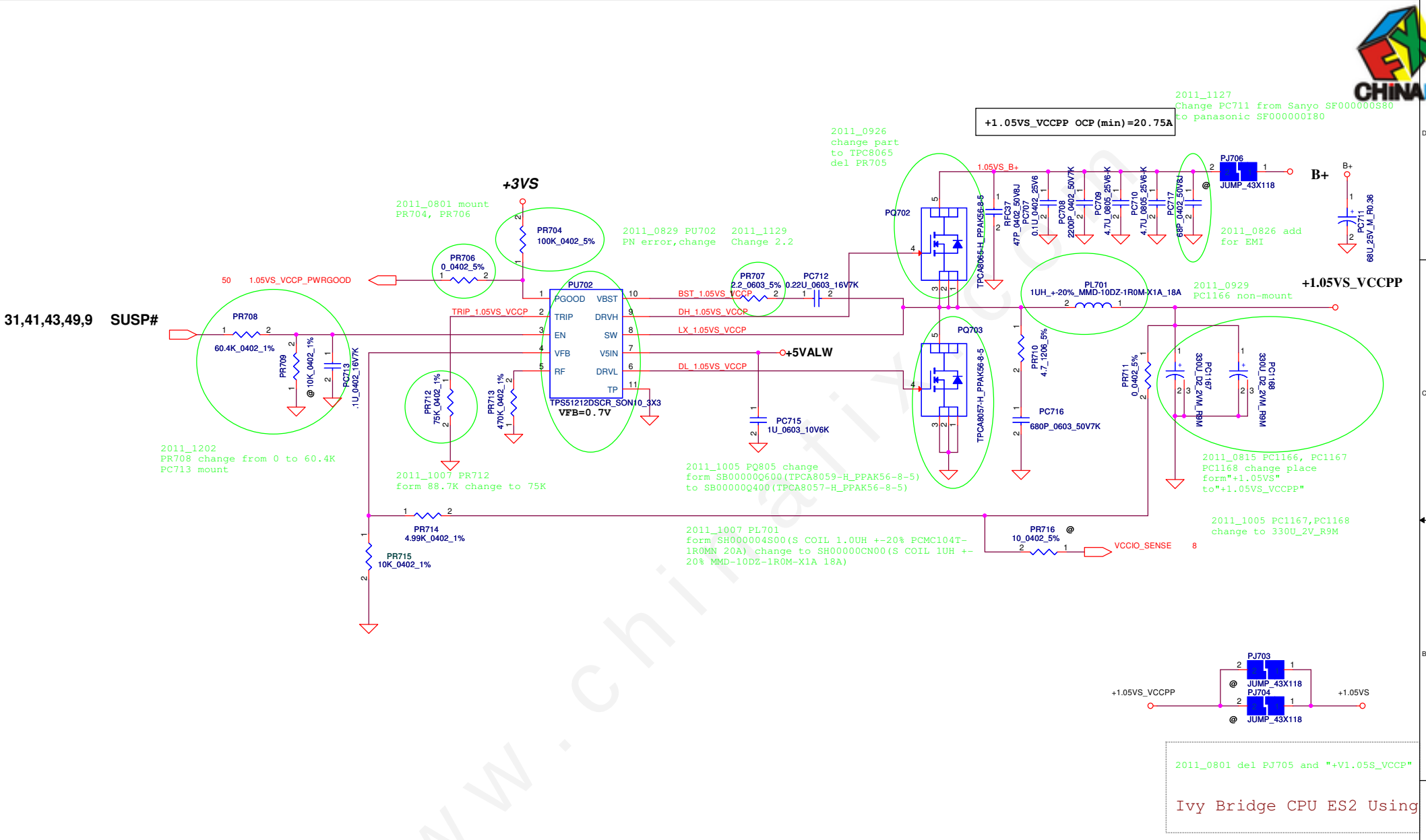
Title: PWR-VCCSAP

Size: C | Document Number: NW-A041 | Rev: 1.A

Date: Thursday, November 01, 2012 | Sheet 50 of 59



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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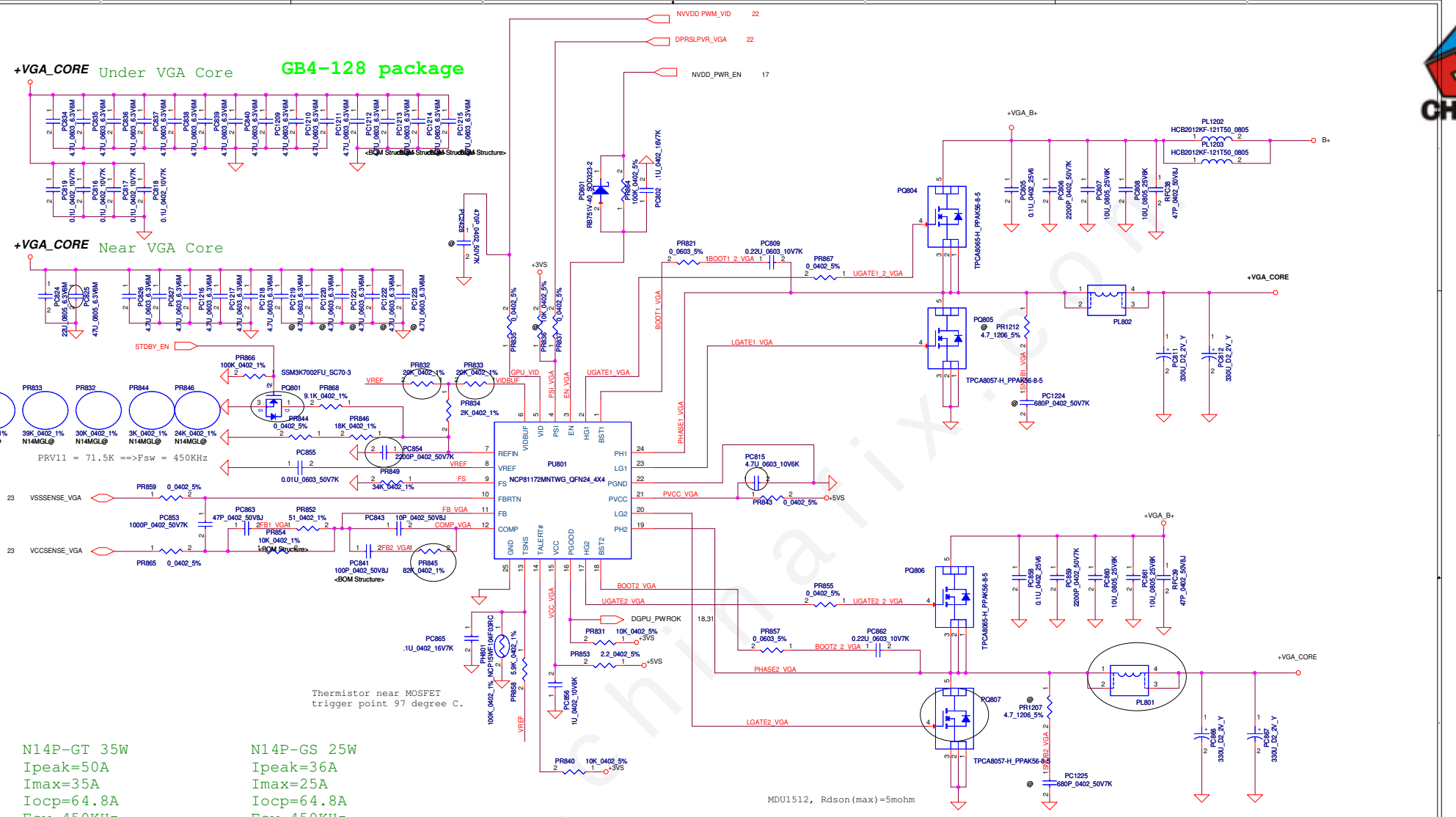
Title: PWR-+1.05VS_VCCP/+0.75VSP

Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Thursday, November 01, 2012 | Sheet 51 of 59



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Title: PWR-VGA_COREP-ISL62883

Size: C | Document Number: NW-A041 | Rev: 1.A

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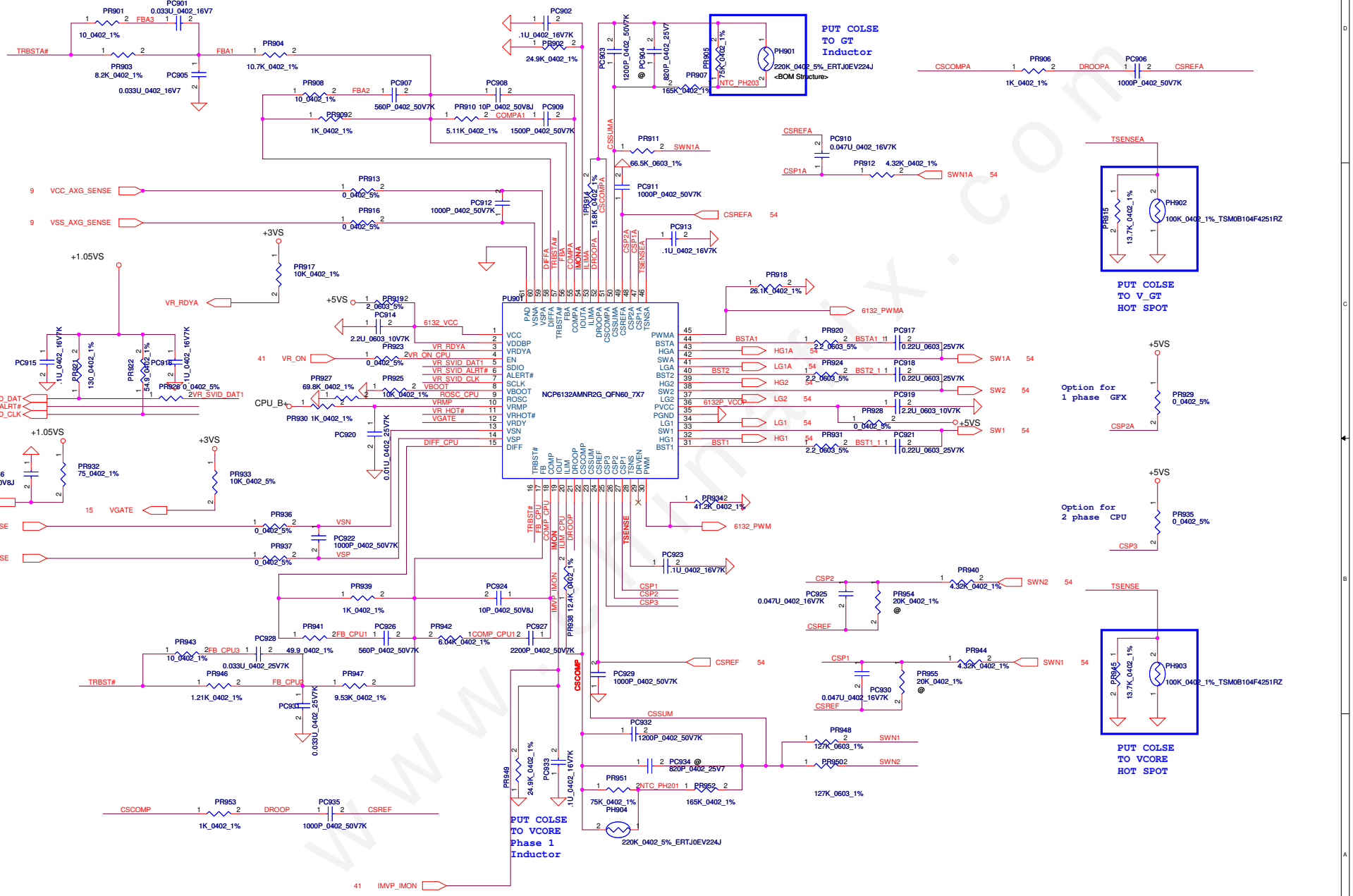

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Title: PWR-CPU_CORE1

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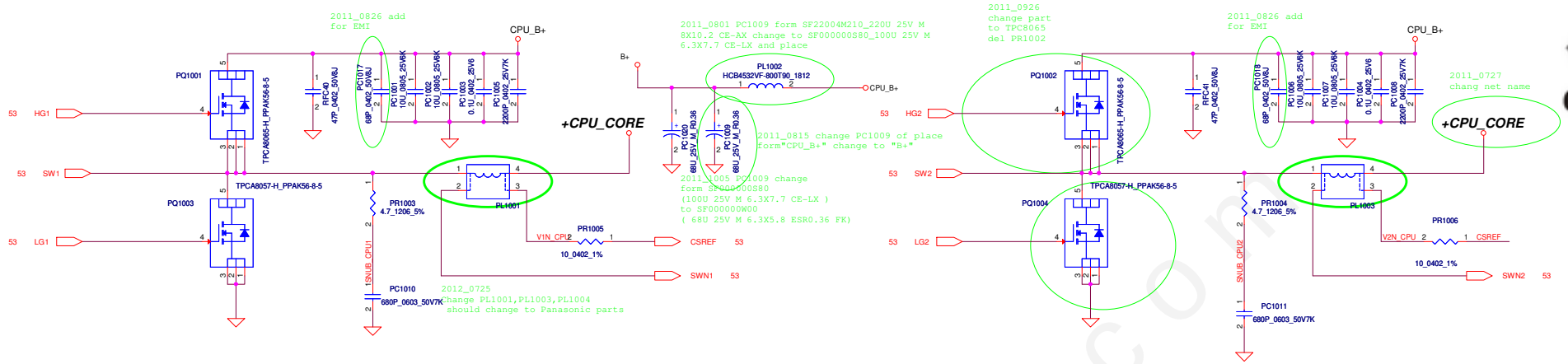
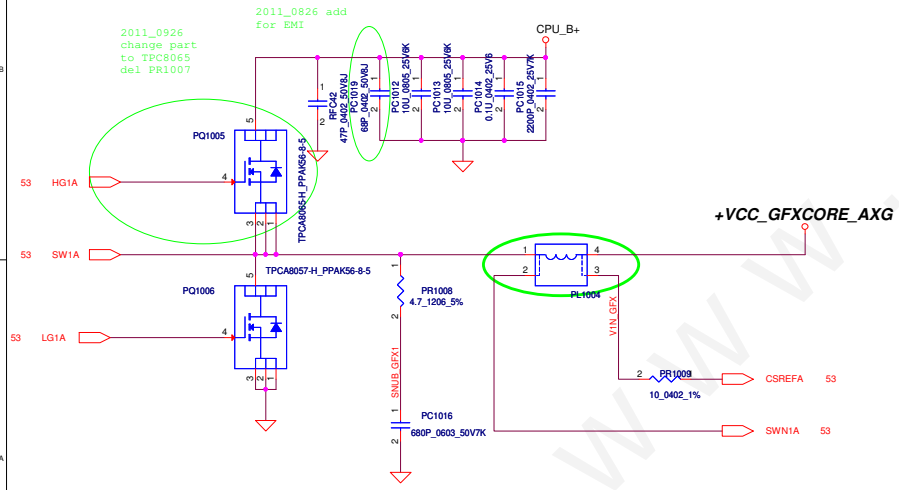


QC 45W CPU	DC 35W CPU
VID1=0.9V	VID1=1.05V
IccMax=94A	IccMax=53A
Icc_Dyn=66A	Icc_Dyn=43A
Icc_TDC=52A	Icc_TDC=36A
R_LL=1.9m ohm	R_LL=1.9m ohm
OCP~110A	OCP~65A



QC 45W GT2	DC 35W GT2
VID1=1.23V	VID1=1.23V
IccMax=46A	IccMax=33A
Icc_Dyn=37A	Icc_Dyn=20.2A
Icc_TDC=38A	Icc_TDC=21.5A
R_LL=3.9m ohm	R_LL=3.9m ohm
OCP~55A	OCP~40A

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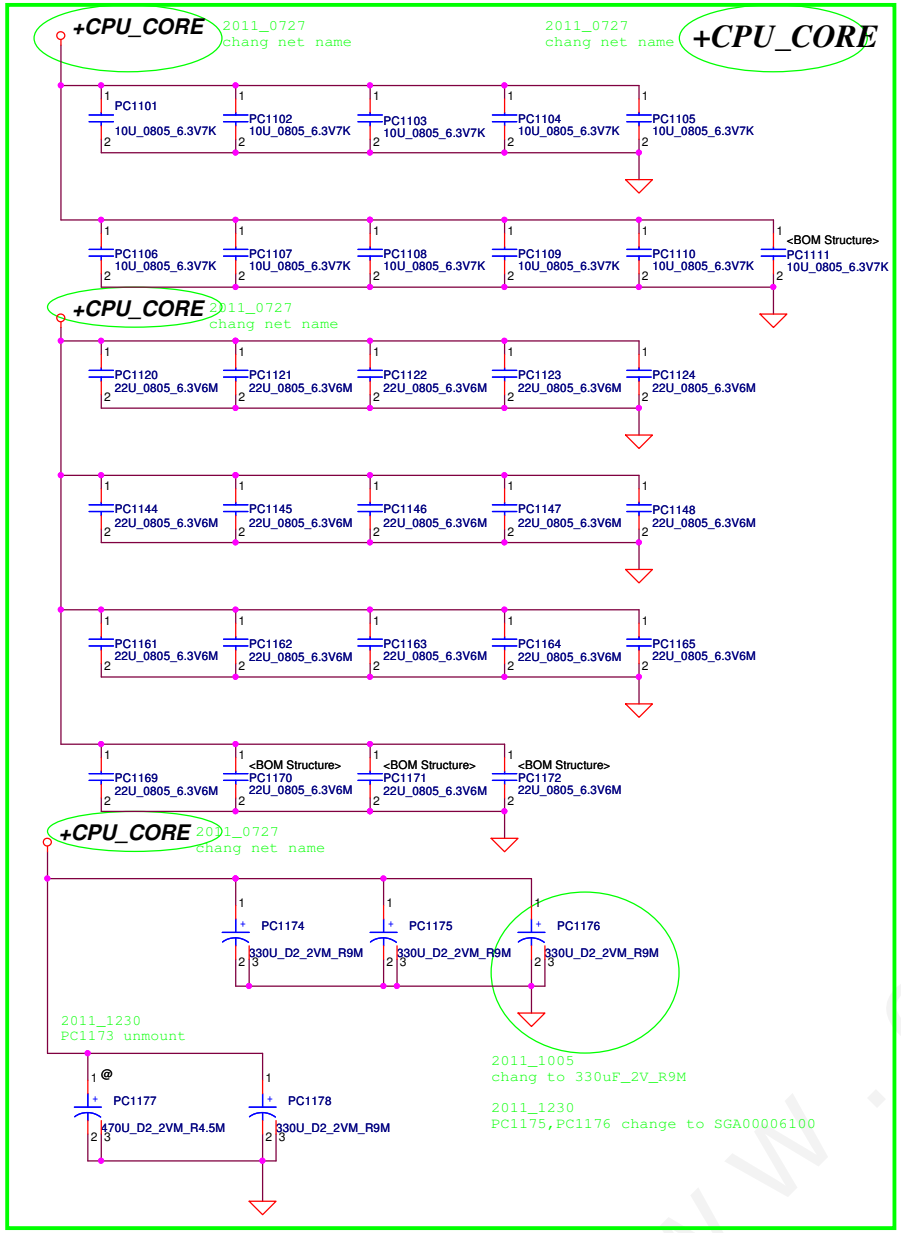
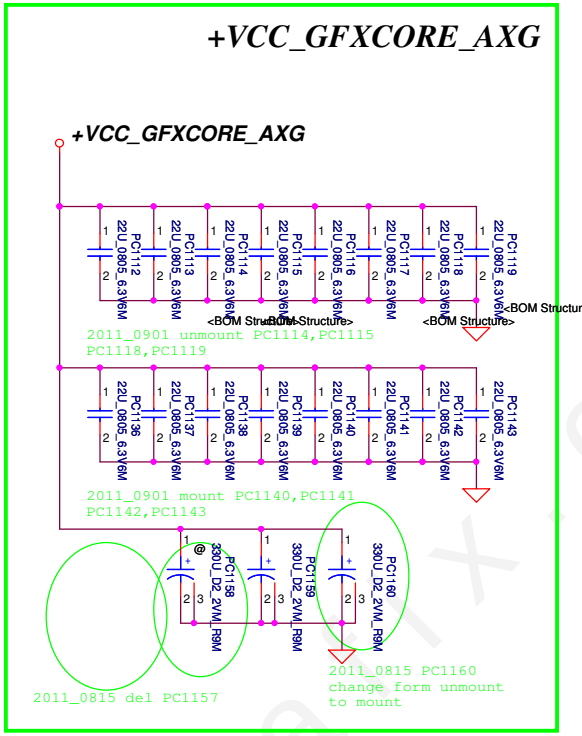
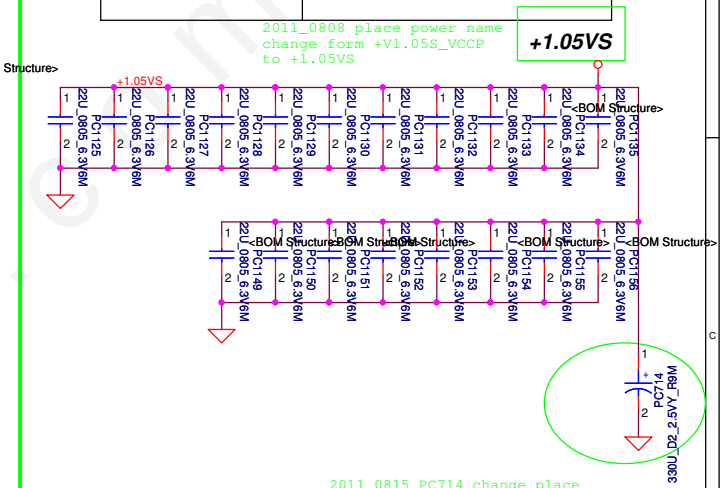




Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



2011_0815 PC714 change place
form "+1.05VS_VCCPP" to "+1.05VS"

2011_1005 PC714 change to
330uF_2V_R9M

2011_1007
PC714
form SGA00001Q802
(S POLY C 330U 2V M X LESR6M SX H1.9)
change to SGA00002680
(330U_D2_2.5VY_R9M)

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Title: PWR-PROCESSOR DECOUPLING

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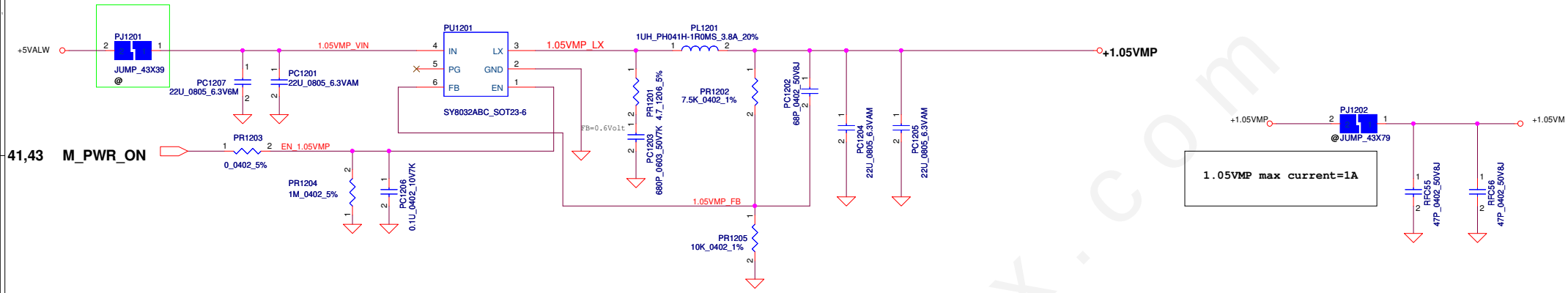
2011_0923 JUMP form 43X79 change to 43X79



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Title: PWR-+1.05VMP

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Title

PWR-Thermal Protect-NA

Size	Document Number	Rev
Custom	NW-A041	1.A

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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Title: PWR-PIR

Size: Custom | Document Number: NM-A041 | Rev: 1.A

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Version Change List (P.I.R. List)

Phase	Date	No.	BOM	Sch	Layout	Description	function
	2012/09/XX	No1	V	V	V	Add CXXX,CXXX	Add XXX function

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Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: EE P.I.R.

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