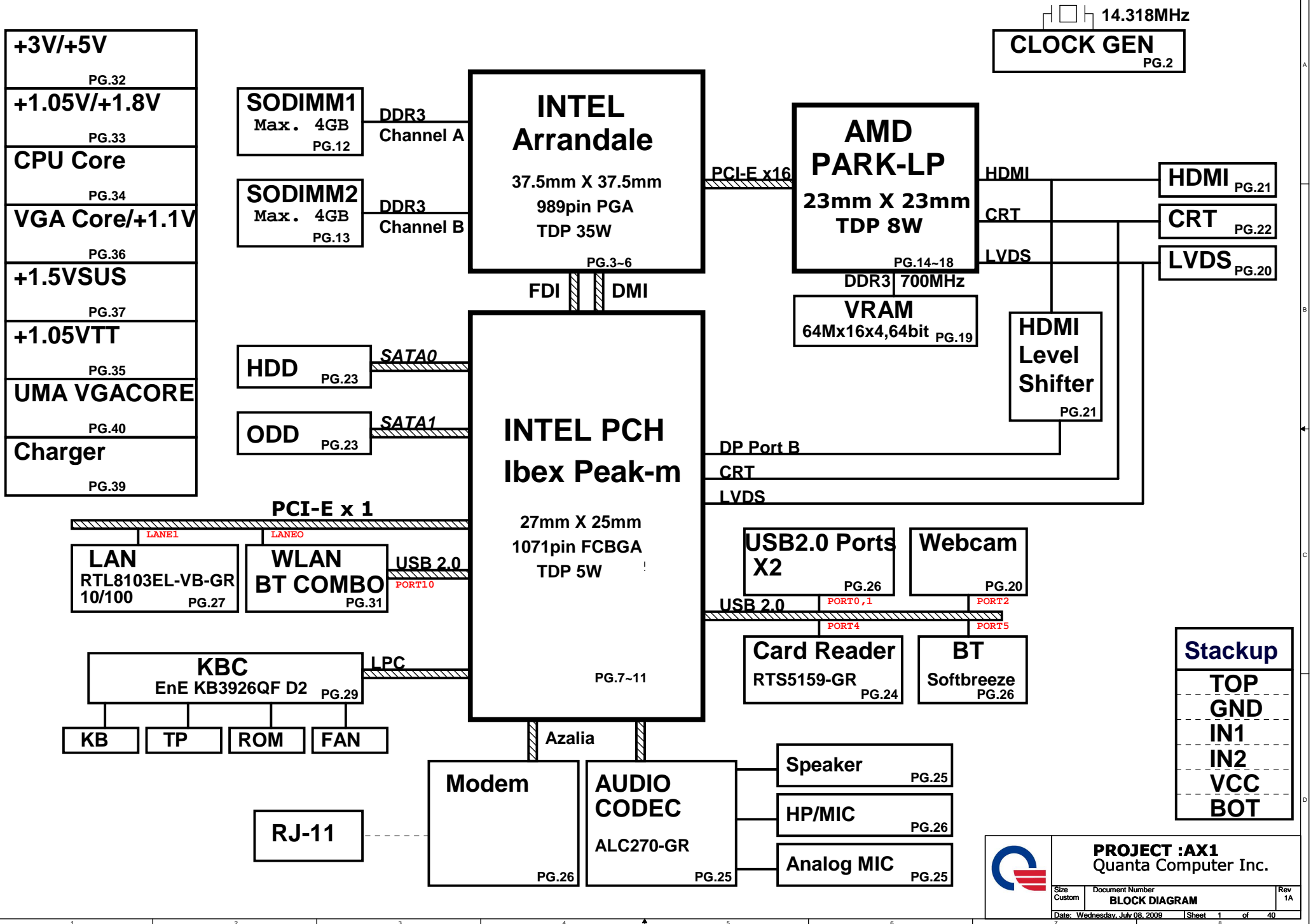
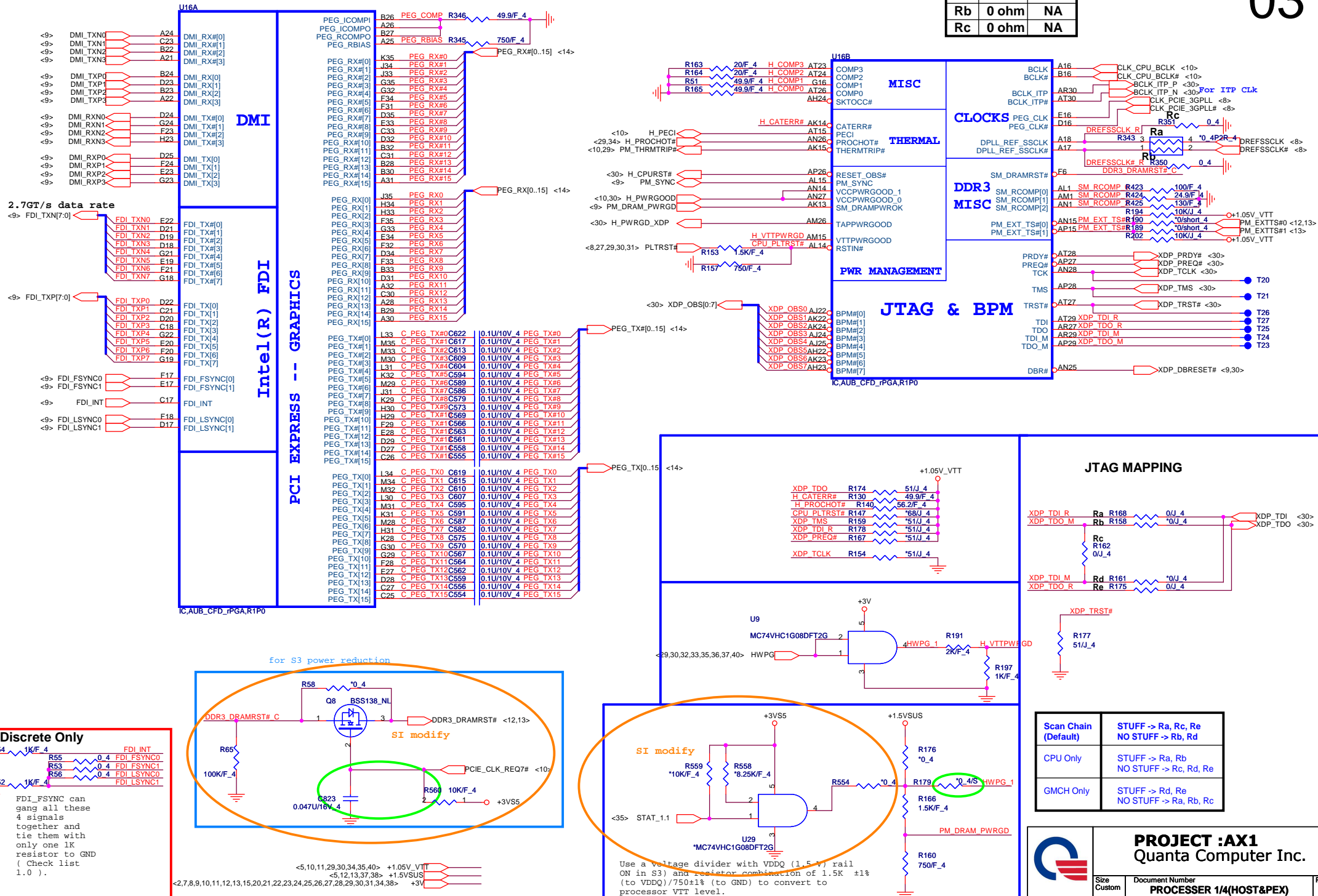


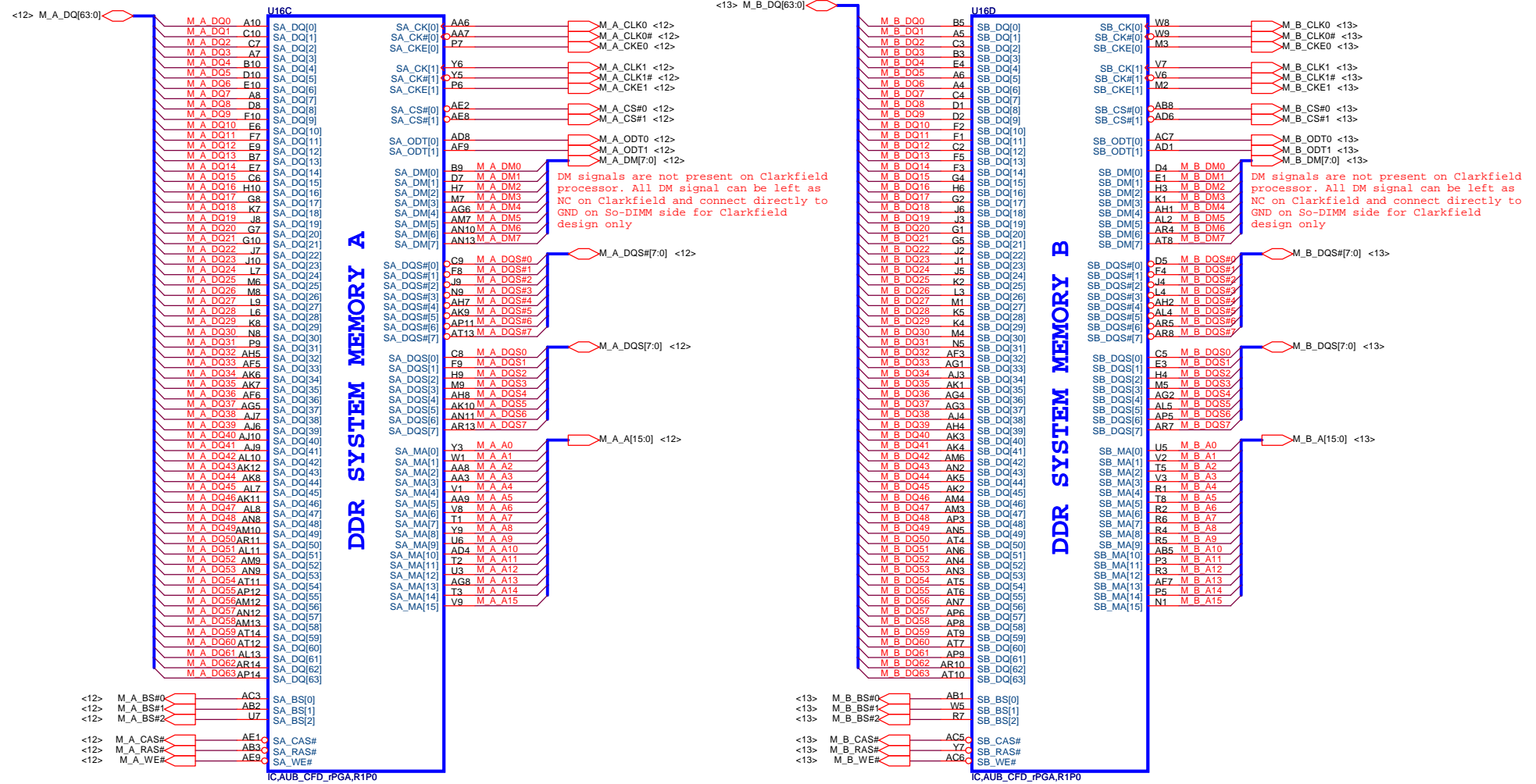
AX1 INTEL UMA/DISCRETE SYSTEM DIAGRAM

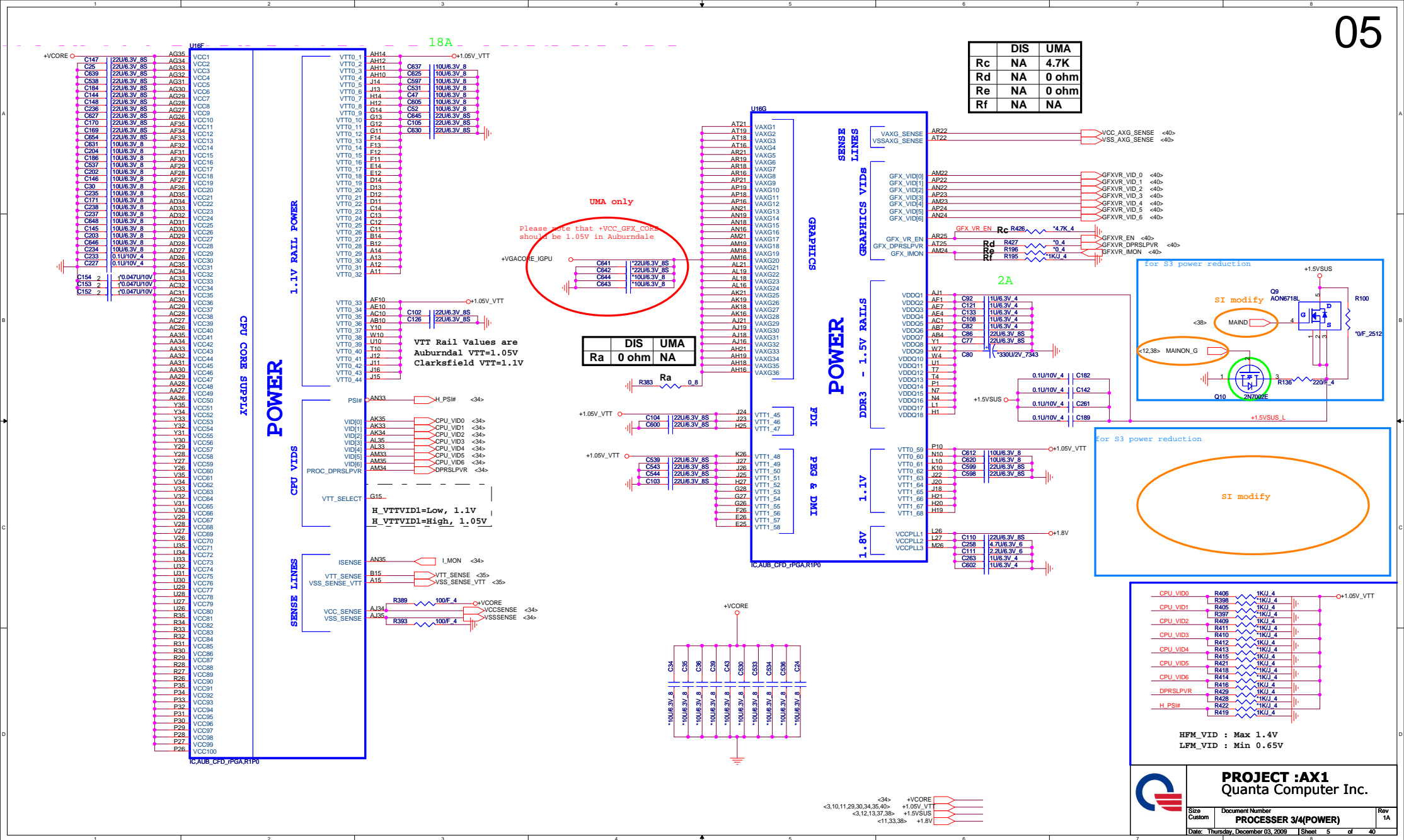


	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA



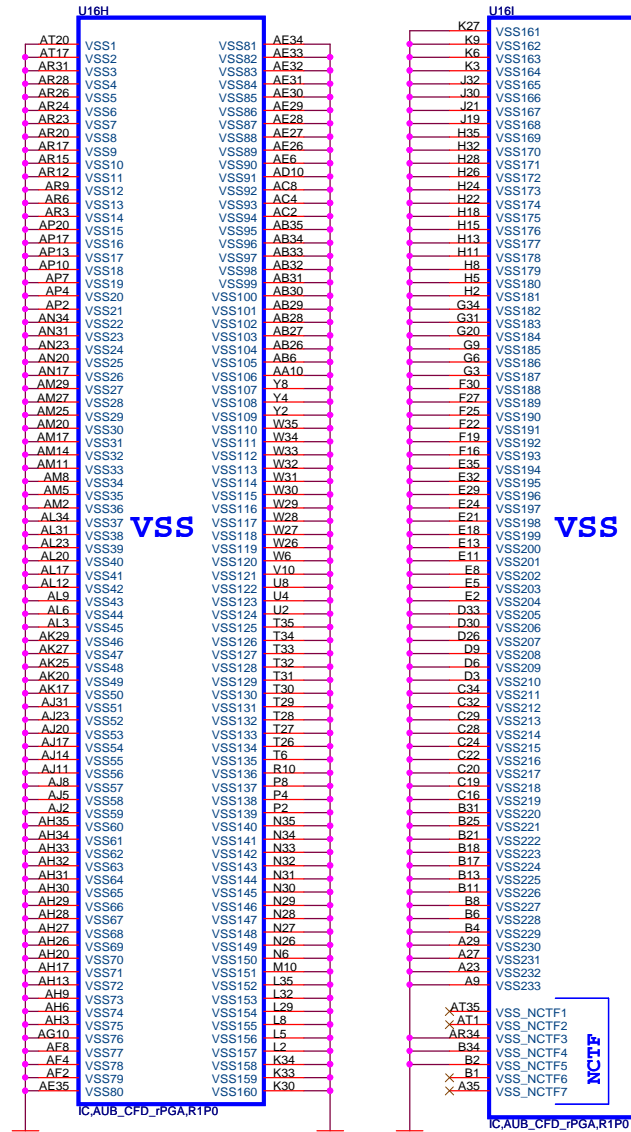
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

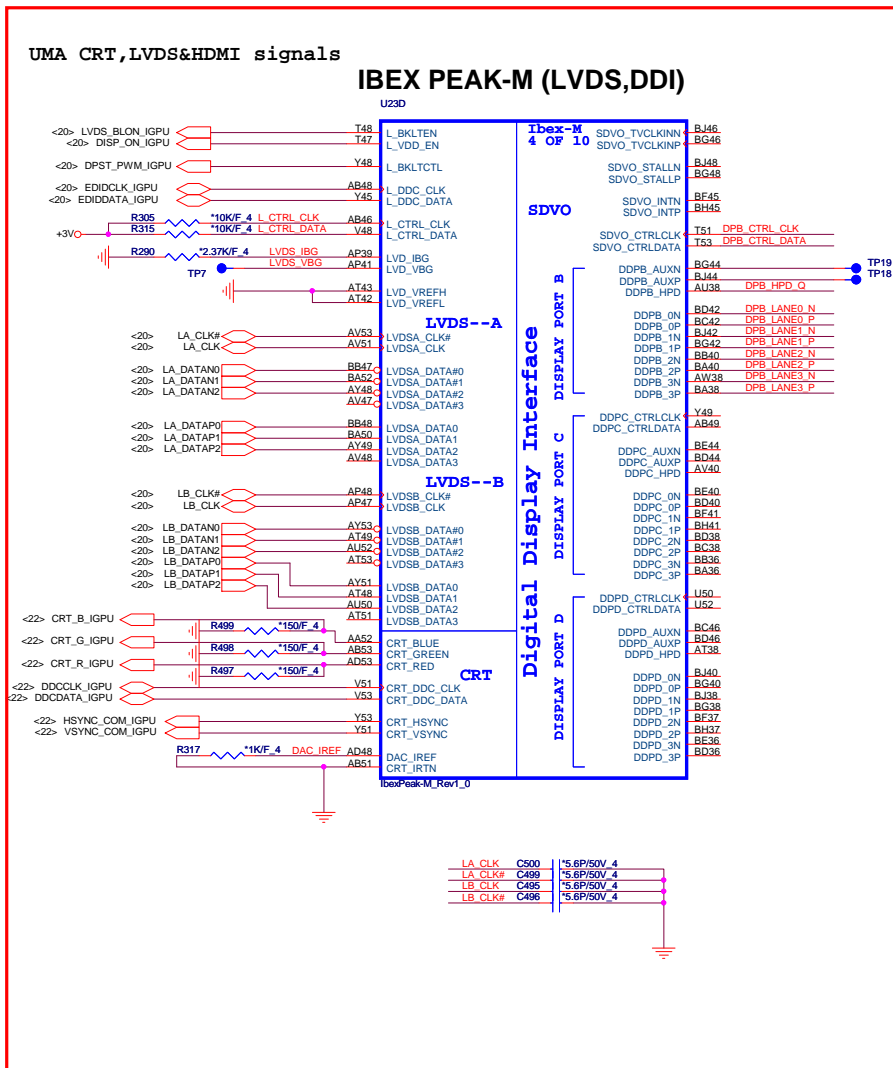




AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

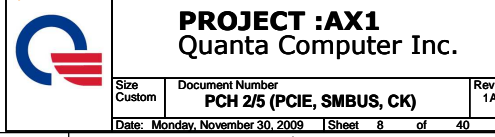
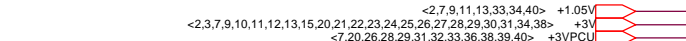
AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



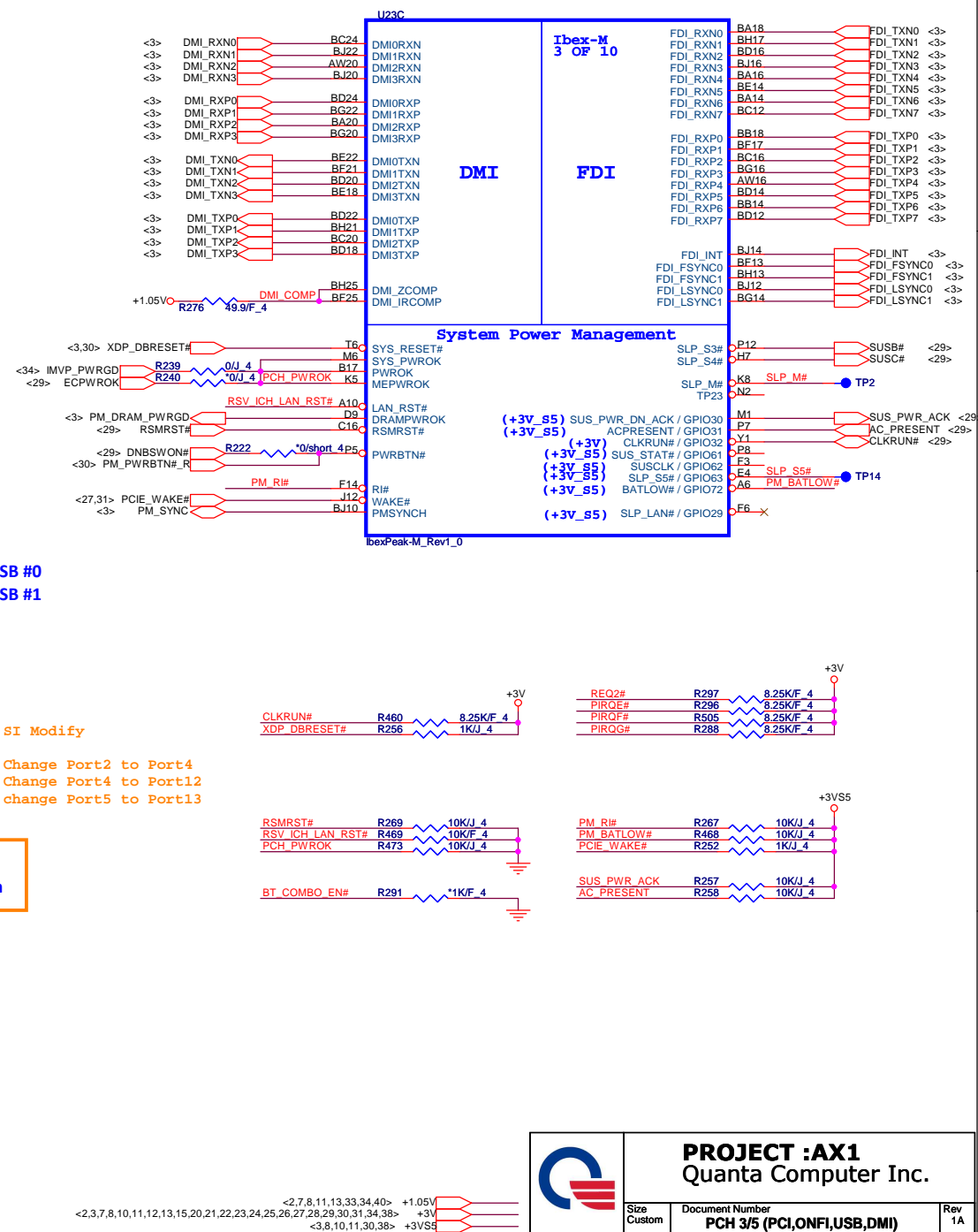
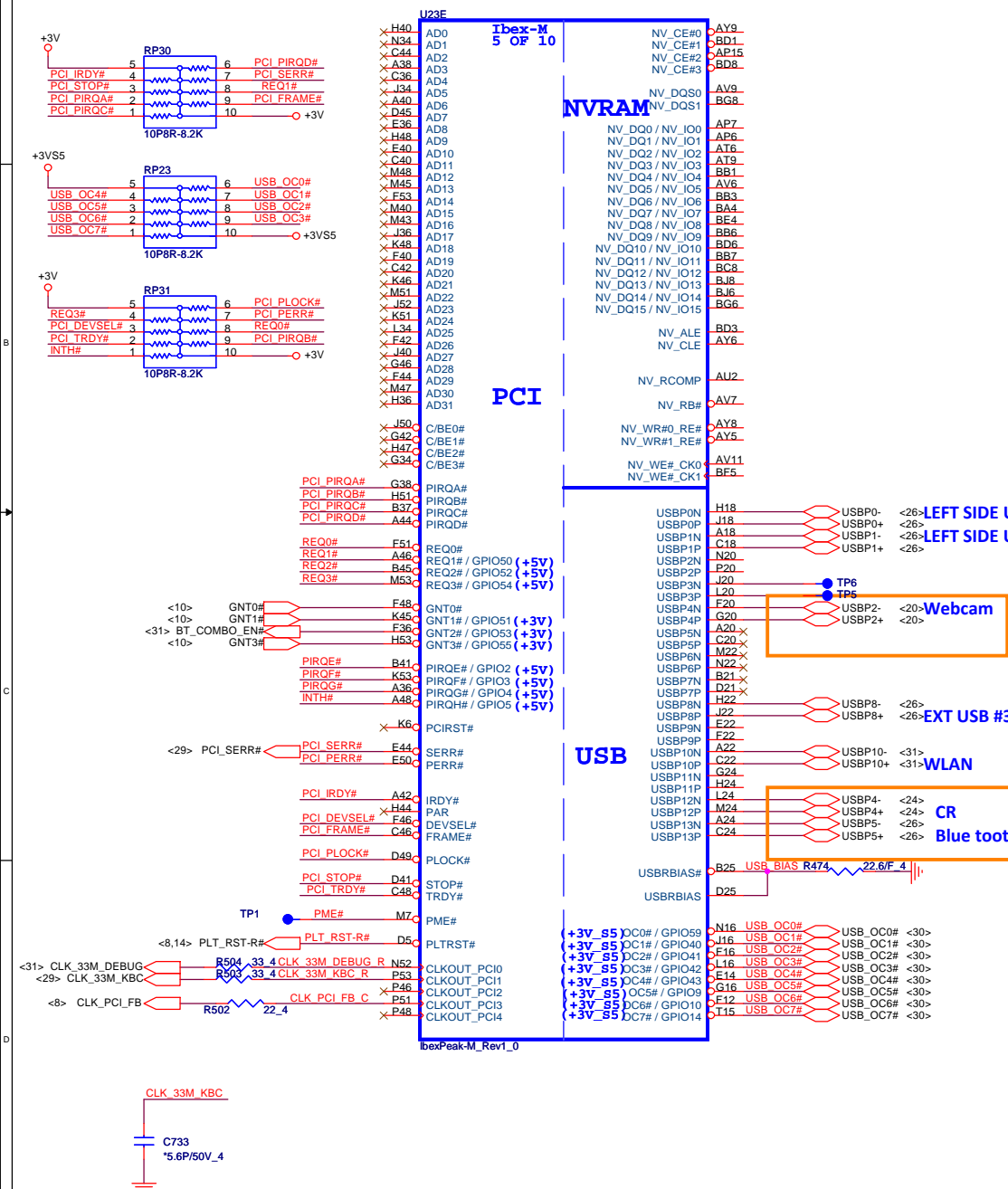


Vendor	PN
Socket	DG008000031
WINBOND	AKE39ZP0N00
MAX	AKE39FP0N00

PROJECT :AX1
Quanta Computer Inc.



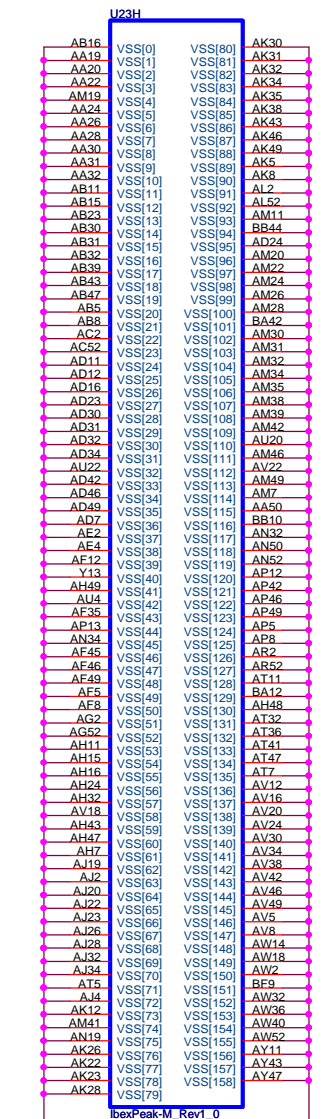
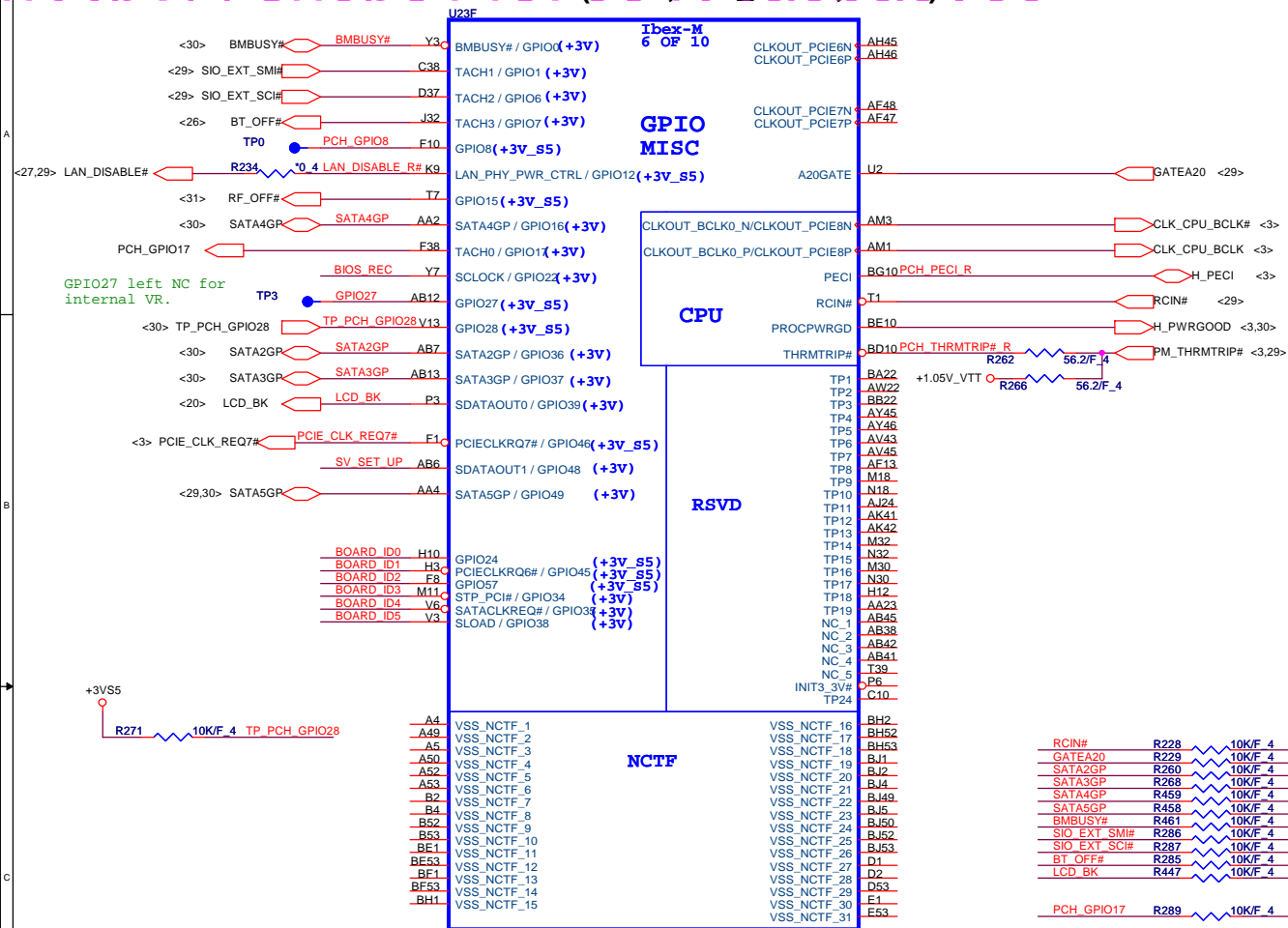
IBEX PEAK-M (PCI,USB,NVRAM)



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)

10



Al6 swap override Strap/Top-Block Swap Override jumper

GNT3#

Low = Al6 swap override/Top-Block Swap Override enabled
High = Default

SV SET UP R259

SV_SET_UP

1-X High = Strong (Default)

Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled

NV_ALE	High = Enable Low = Disable

DMI Termination Voltage

NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

No Reboot Strap

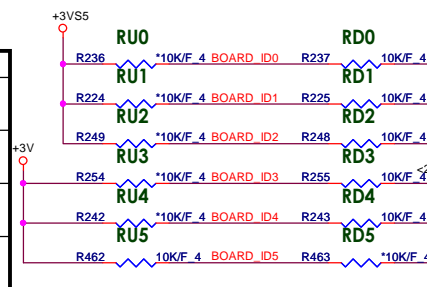
<7.25> ACZ_SPKR

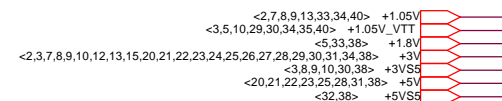
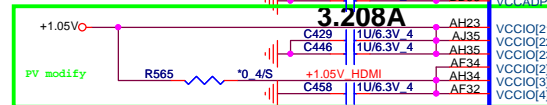
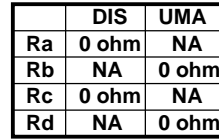
<7.29> PCH_GPIO33

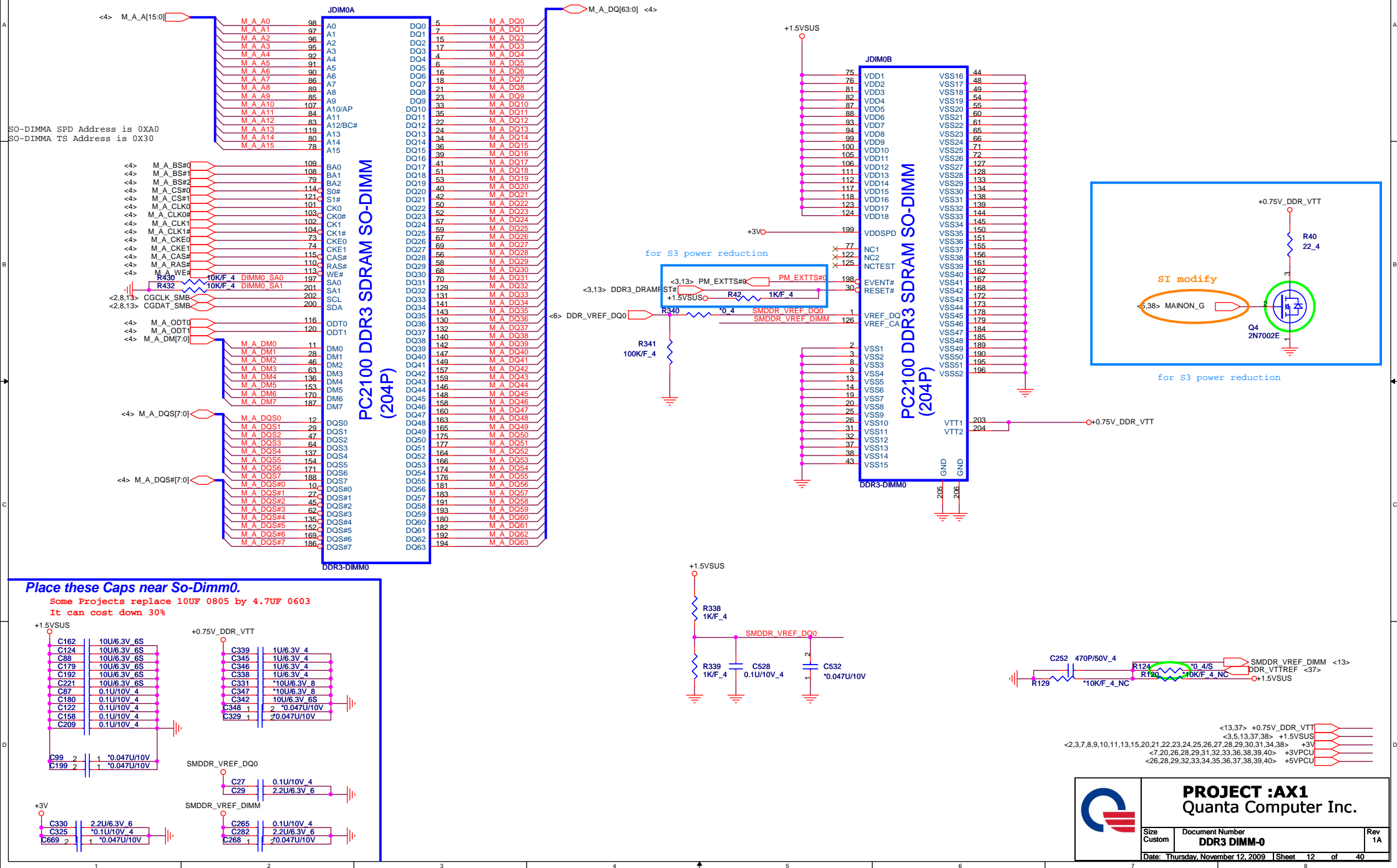
BOARD ID SETTING

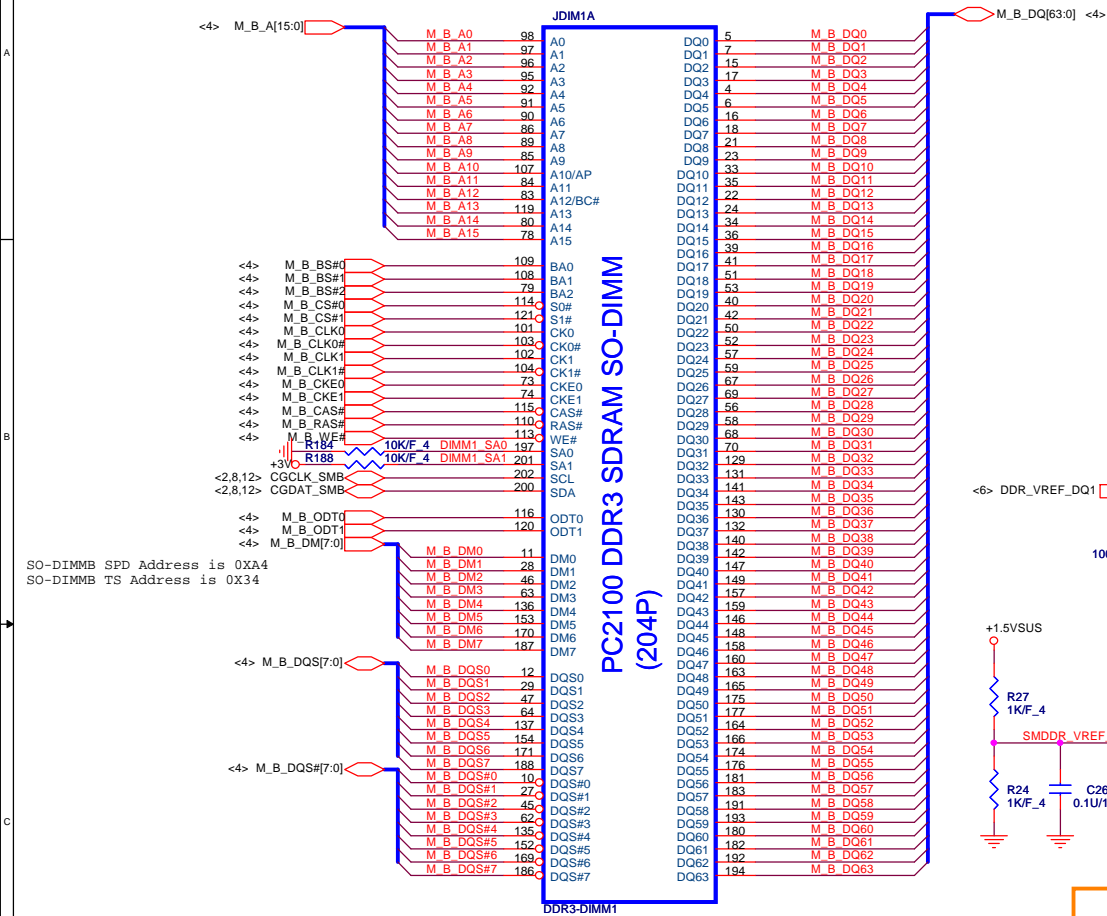
Board ID5: For identify UMA and DIS
Board ID4: For identify FF and DF
Board ID3: Reserve
Board ID2: Reserve
Board ID1: Reserve

Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UMA FF	0	0	0	0	0	0
UMA DF	0	0	0	0	1	0
DIS	0	0	0	0	0	1

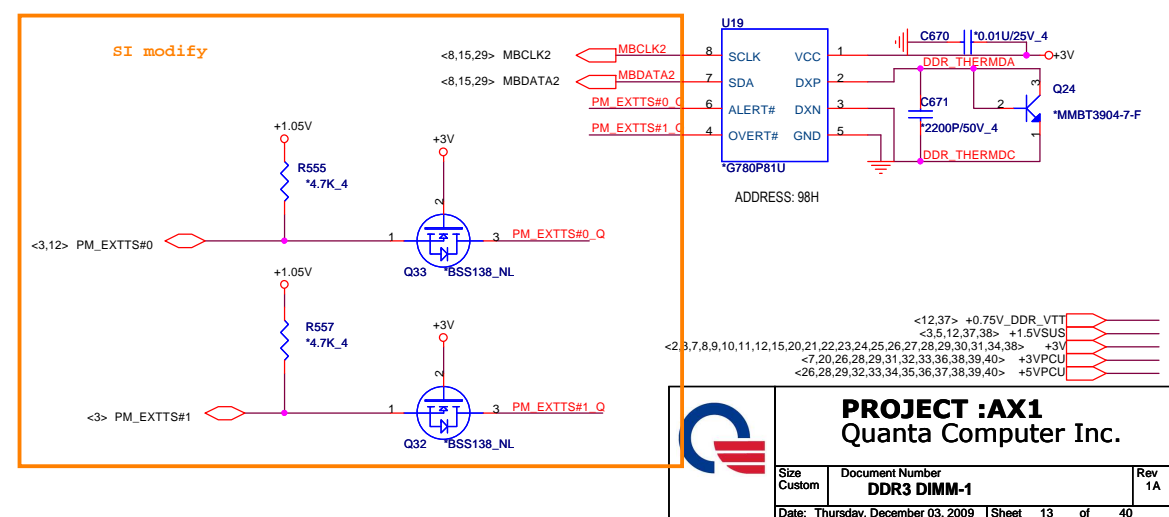
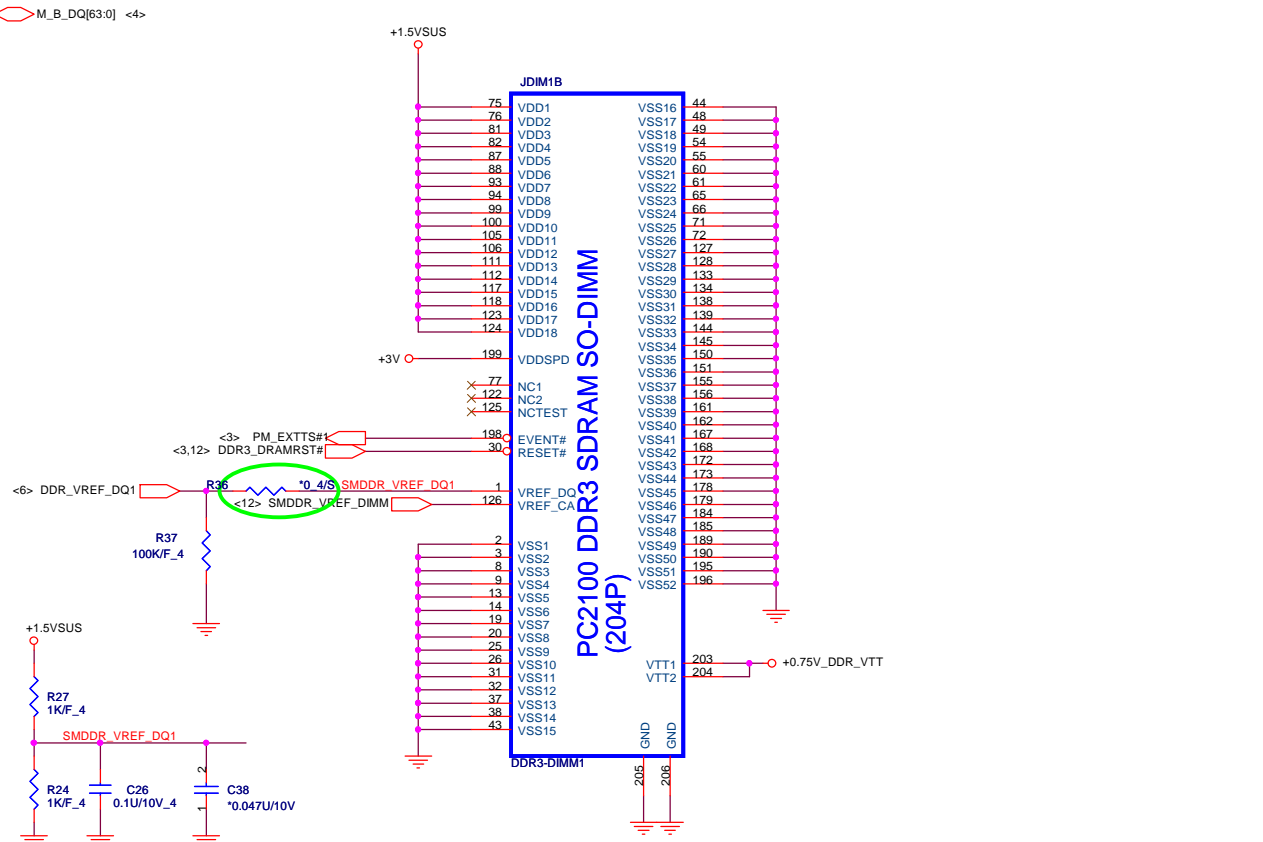
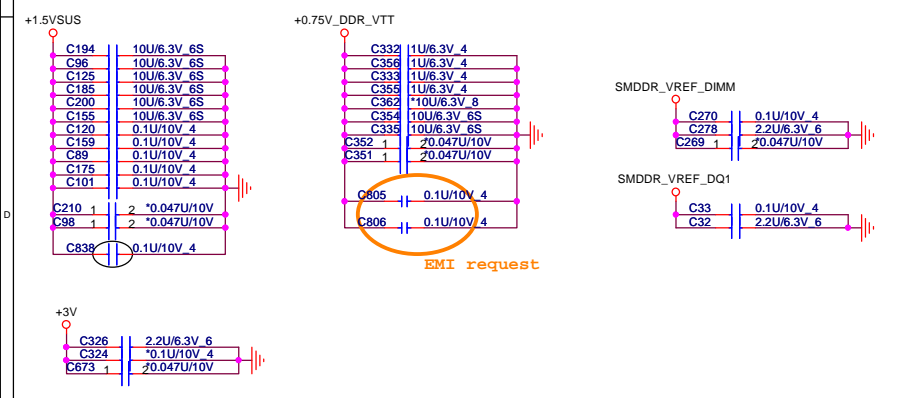




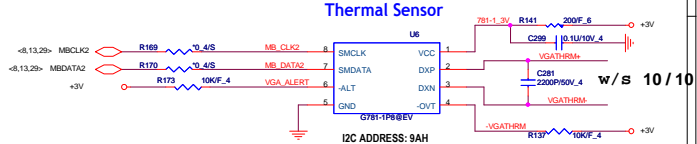
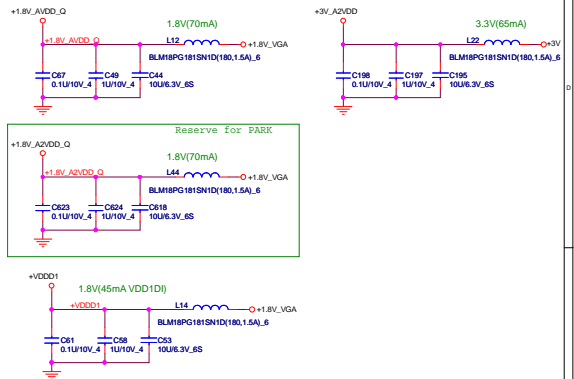


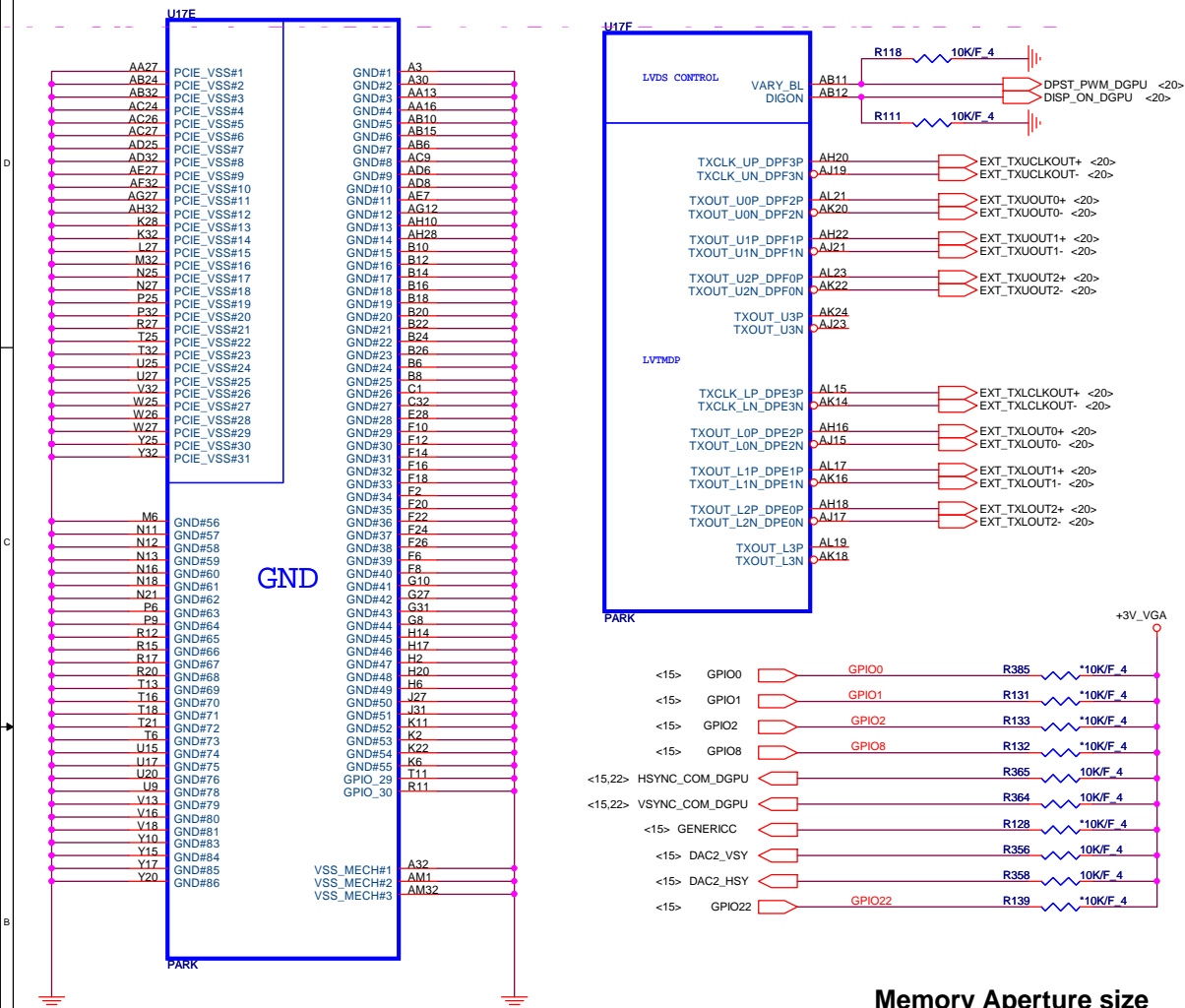


Place these Caps near So-Dimm1.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%



	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0.9V
M	0	1	0.95V
H	1	0	1.05V
TBD	1	1	NA





Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

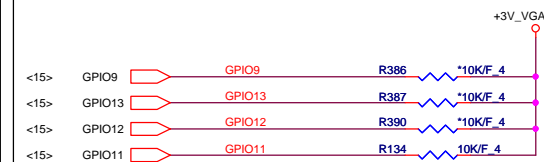
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1= INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO21_BB_EN	

PROJECT :AX1
Quanta Computer Inc.

Size Custom	Document Number M93_GND / LVDS / Straps	Rev 1A
Date: Thursday, November 12, 2009	Sheet 16 of 40	

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Size Custom	Document Number M93_Power_and_NC	Rev 1A
Date: Tuesday, November 10, 2009		Sheet 17 of 40

<19> VMA_ODT0 VMA_ODT0
<19> VMA_ODT1 VMA_ODT1
<19> VMA_RAS0# VMA_RAS0#
<19> VMA_RAS1# VMA_RAS1#
<19> VMA_CAS0# VMA_CAS0#
<19> VMA_CAS1# VMA_CAS1#
<19> VMA_WE0# VMA_WE0#
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<19> VMA_CS0# VMA_CS0#
<19> VMA_CS1# VMA_CS1#

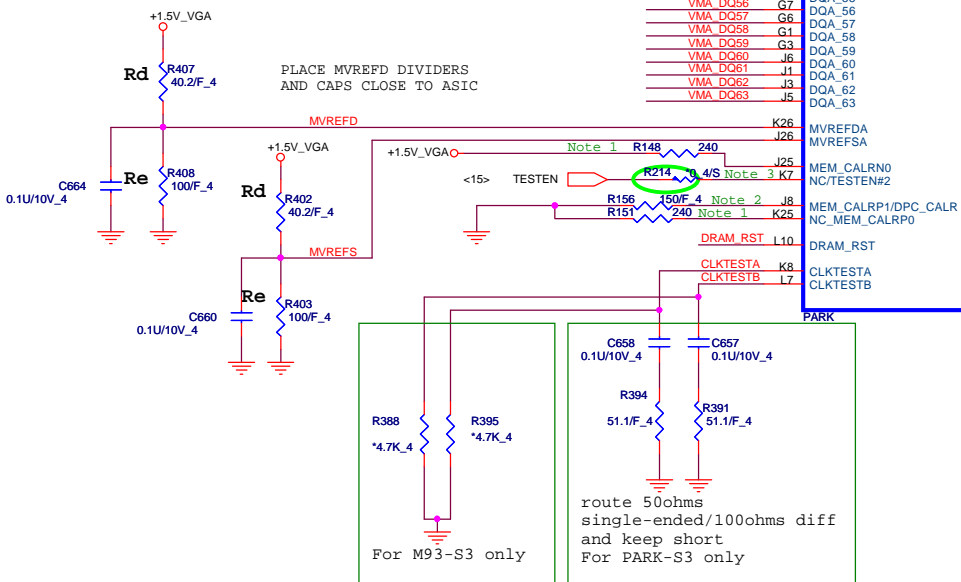
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<19> VMA_CKE1 VMA_CKE1
<19> VMA_CLK0 VMA_CLK0
<19> VMA_CLK0# VMA_CLK0#
<19> VMA_CLK1 VMA_CLK1
<19> VMA_CLK1# VMA_CLK1#

<19> VMA_WDQS[7..0] VMA_WDQS[7..0]
<19> VMA_RDQS[7..0] VMA_RDQS[7..0]
<19> VMA_DM[7..0] VMA_DM[7..0]
<19> VMA_DQ[63..0] VMA_DQ[63..0]
<19> VMA_MA[13..0] VMA_MA[13..0]

<19> VMA_BA0 VMA_BA0
<19> VMA_BA1 VMA_BA1
<19> VMA_BA2 VMA_BA2

support 1gbit
VRAM (64M X 16)

DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Rd)	40.2R	40.2R
MVREF TO GND (Re)	100R	100R



Note 1 :Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.
Note 2 :For M9X-S2/S3,J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
For Park-S3,J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR
Note 3 :For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected.
For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24

MEMORY INTERFACE

MAA_0 K17 VMA_MA0
MAA_1 J20 VMA_MA1
MAA_2 H23 VMA_MA2
MAA_3 G23 VMA_MA3
MAA_4 G24 VMA_MA4
MAA_5 H24 VMA_MA5
MAA_6 J19 VMA_MA6
MAA_7 J19 VMA_MA7
MAA_8 K14 VMA_MA8
MAA_9 K14 VMA_MA9
MAA_10 J11 VMA_MA10
MAA_11 J13 VMA_MA11
MAA_12 H11 VMA_MA12
MAA_13/BA2 G11 VMA_BA2
MAA_14/BA0 J16 VMA_BA0
MAA_15/BA1 L15 VMA_BA1

DQMA_0 E32 VMA_DM0
DQMA_1 E30 VMA_DM1
DQMA_2 A21 VMA_DM2
DQMA_3 C21 VMA_DM3
DQMA_4 E13 VMA_DM4
DQMA_5 D12 VMA_DM5
DQMA_6 E3 VMA_DM6
DQMA_7 F4 VMA_DM7

RDQSA_0 H28 VMA_RDQS0
RDQSA_1 C27 VMA_RDQS1
RDQSA_2 A23 VMA_RDQS2
RDQSA_3 E19 VMA_RDQS3
RDQSA_4 D10 VMA_RDQS4
RDQSA_5 D6 VMA_RDQS5
RDQSA_6 G5 VMA_RDQS6
RDQSA_7 G5 VMA_RDQS7

WDQSA_0 H27 VMA_WDQS0
WDQSA_1 A27 VMA_WDQS1
WDQSA_2 C23 VMA_WDQS2
WDQSA_3 C19 VMA_WDQS3
WDQSA_4 C15 VMA_WDQS4
WDQSA_5 E9 VMA_WDQS5
WDQSA_6 C5 VMA_WDQS6
WDQSA_7 H4 VMA_WDQS7

ODTA0 L18 VMA_ODT0
ODTA1 K16 VMA_ODT1

CLKA0 H26 VMA_CLK0
CLKA0B H25 VMA_CLK0#

CLKA1 G9 VMA_CLK1
CLKA1B H9 VMA_CLK1#

RASA0B G22 VMA_RAS0#
RASA1B G17 VMA_RAS1#

CASA0B G19 VMA_CAS0#
CASA1B G16 VMA_CAS1#

CSA0B_0 H22 VMA_CS0#
CSA0B_1 J22

CSA1B_0 G13 VMA_CS1#
CSA1B_1 K13

CKEA0 K20 VMA_CKE0
CKEA1 J17 VMA_CKE1

WEA0B G25 VMA_WE0#
WEA1B H10 VMA_WE1#

PX_EN AB16
RSVD#2 G14
RSVD#3 G20

MEM_CALRNO J25
NC_MEM_CALRP0 K7

DRAM_RST L10
CLKTESTA K8
CLKTESTB L7

PARK

MVREFDA K26
MVREFSA J26

TESTEN <15> R214 4/S Note 3 K7

MEM_CALRP1/DPC_CALR J8
NC_MEM_CALRP0 K25

DRAM_RST L10
CLKTESTA K8
CLKTESTB L7

PARK

MVREFDA K26
MVREFSA J26

TESTEN <15> R214 4/S Note 3 K7

MEM_CALRP1/DPC_CALR J8
NC_MEM_CALRP0 K25

DRAM_RST L10
CLKTESTA K8
CLKTESTB L7

PARK

For PARK-S3 only
For M9X-S2/S3 with
DDR3: this pin is
not in use.

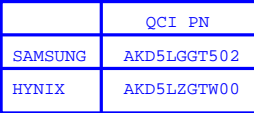
Designator	M9X-S2 and M93-S3	Park-S3
Ra	NC	10K
Rb	0R/Short	680R
Rc	2.2K	NC
Ca	2.2nF	68pF



PROJECT :AX1
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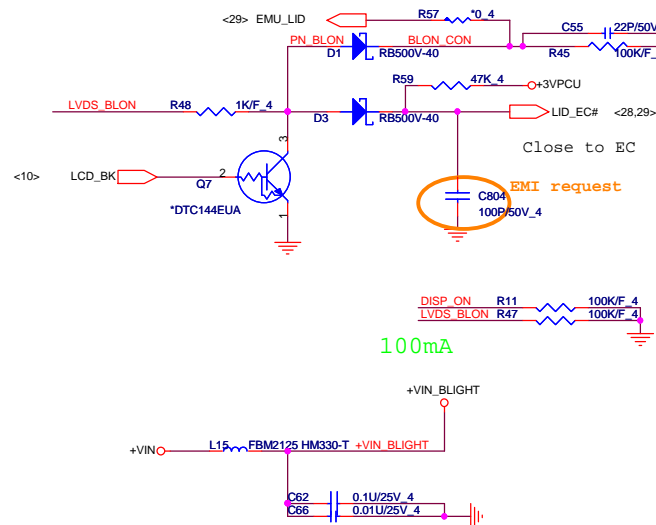
Size Custom	Document Number M93_MEM_Interface	Rev 1A
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<18> VMA_MA[13..0] VMA_MA[13..0]
 <18> VMA_DM[7..0] <18> VMA_DQ[63..0]
 <18> VMA_WDQS[7..0]
 <18> VMA_RDQS[7..0]

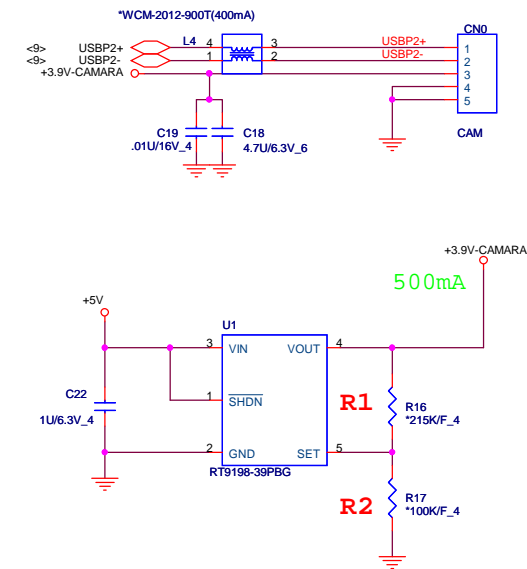


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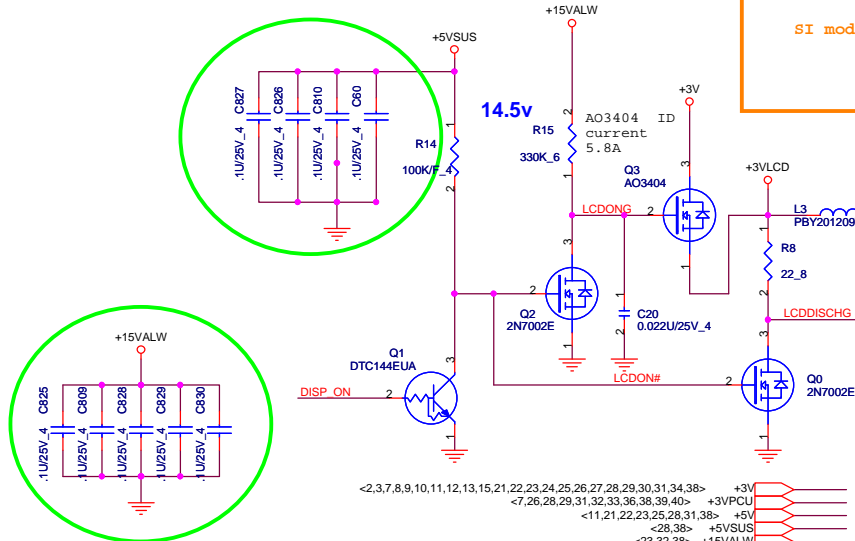
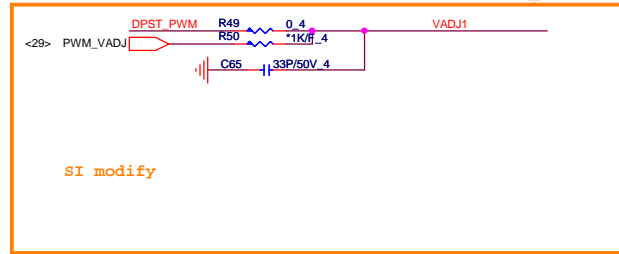
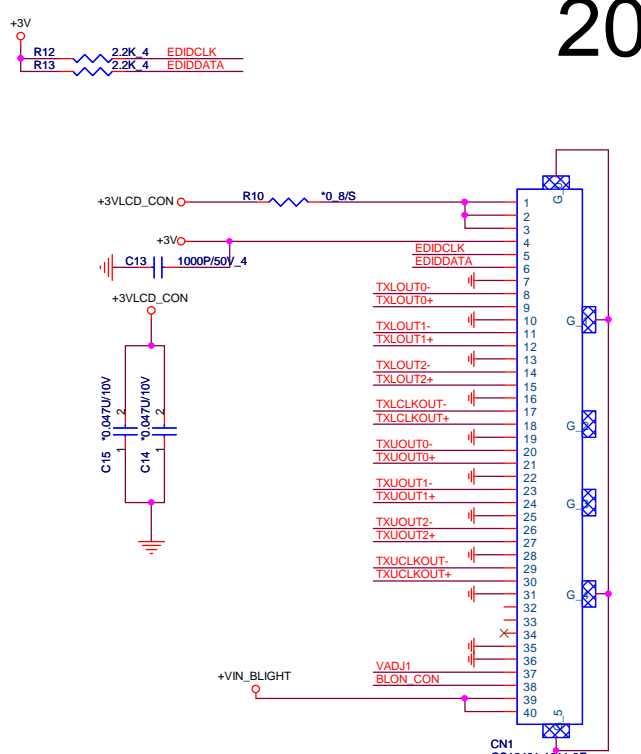
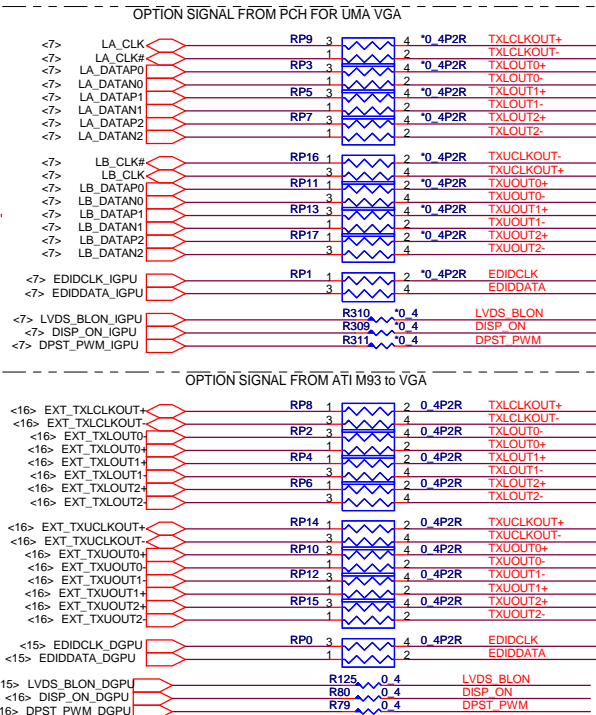
LID Switch



CAMERA

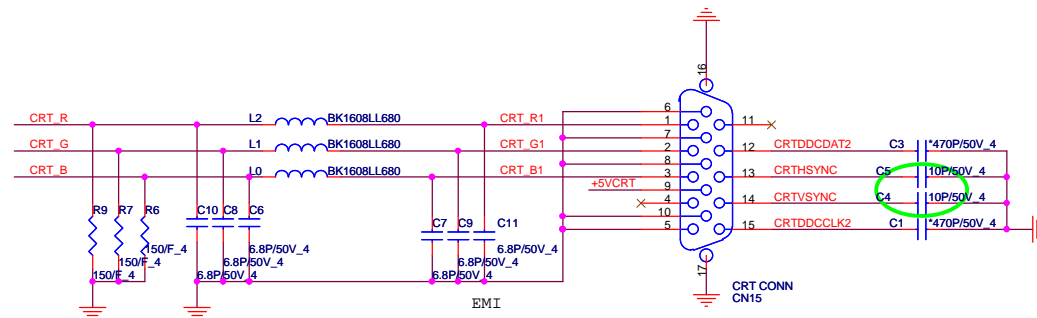
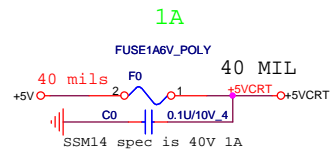


1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near PCH, then place these series Resistors near PCH

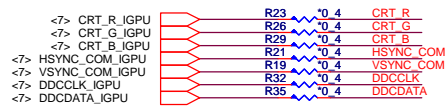


PROJECT :AX1
Quanta Computer Inc.

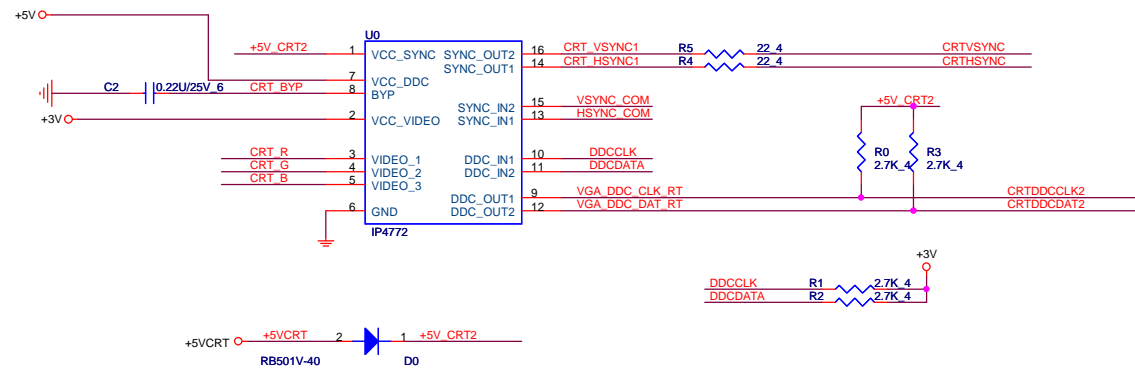
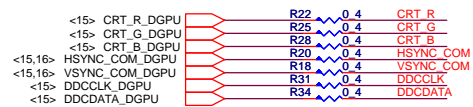
CRT PORT



FOR UMA



FOR DISCRETE



$$\text{FANPWR} = 1.6 \cdot \text{VSET}$$

Figure 1: G995 layout notes. The diagram illustrates the electrical connections for the G995 component. The component has 8 pins: 1 (VIN), 2 (VON), 3 (+5V_FAN), 4 (/FON), 5 (GND), 6 (GND), 7 (GND), and 8 (GND). A thermistor R68 (10K/F_4) is connected between +5V and pin 1. A fan is connected to +5V and pin 2. A GND symbol is shown near pin 5. Below the schematic is a 'Gnd shape' diagram showing a 4x4 grid of pins. To the right, a note says 'G995 layout notes'.

Diagram illustrating the connection of the SATA HDD(1ST) connector (CN29) to the system. The connector pins are numbered 1 through 19. The connections are as follows:

- Pins 1, 2, 3, 4, 5, 6, 7: SATA TXP0, SATA TXN0, SATA RXN0, SATA RXP0, C743, C746, and 0.01uF/16V 4.
- Pins 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19: +3V, +5V, and other signals.

The diagram also shows a green oval highlighting the connection area for the SATA HDD(1ST) connector, labeled "PV modisay".

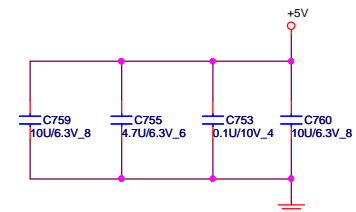
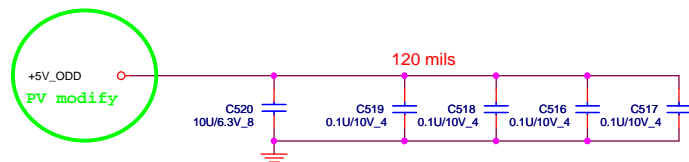


Diagram illustrating the SATA TXN1 and RXN1 connections. The SATA connector (CN13) is shown with pins 1 through 19. The connections are as follows:

- Pins 1, 3, 5, 7, 9, 11, 13, 15, 17, 19: SATA_TXP1 <7> / SATA_TXN1 <7>
- Pins 2, 4, 6, 8, 10, 12, 14, 16, 18: SATA_RXN1 <7> / SATA_RXP1 <7>
- Pin 10: +5V_ODD
- Pin 11: ODD_EJECT#
- Pin 19: SATA_ODD

A green oval highlights the "PV modify" section, showing a +5V_ODD supply connected to a resistor R452 (0.8 ohms) and then to the SATA_TXN1 pin.

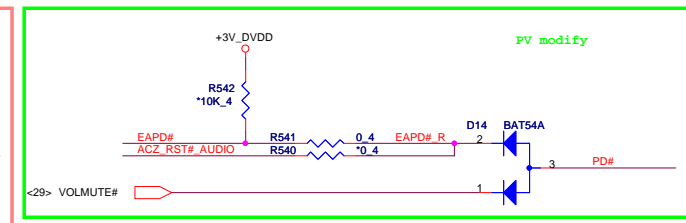
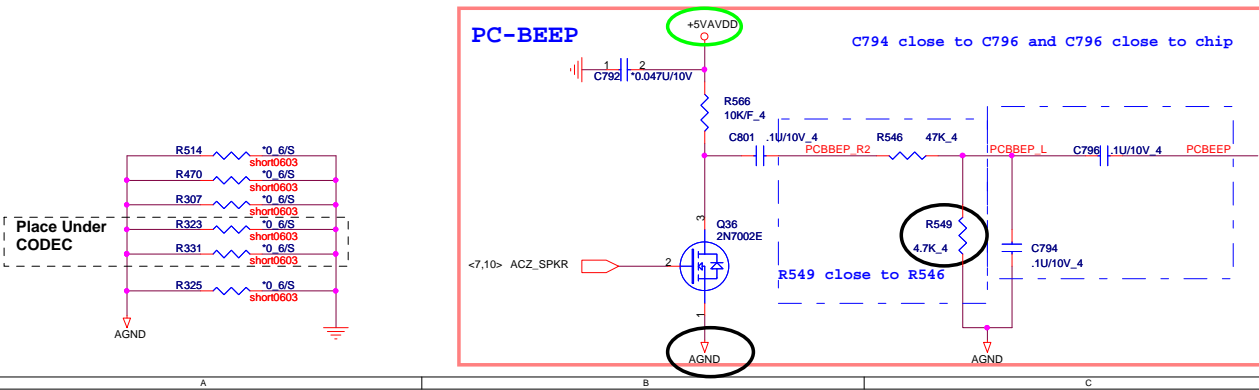
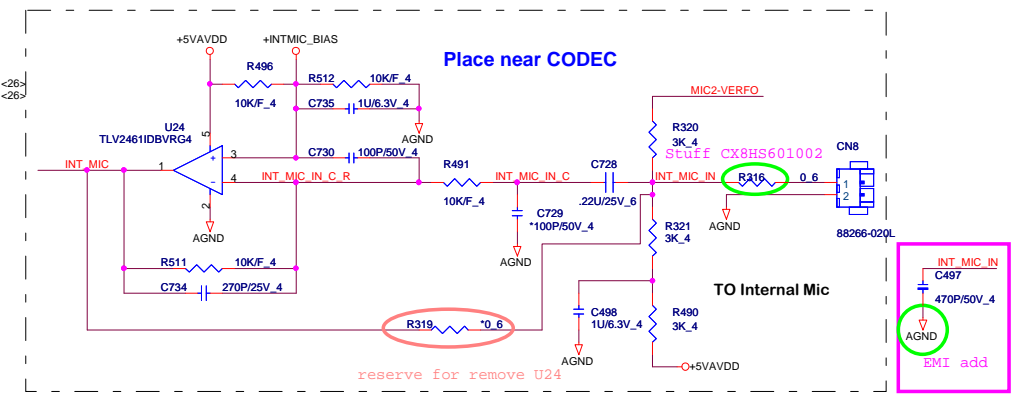
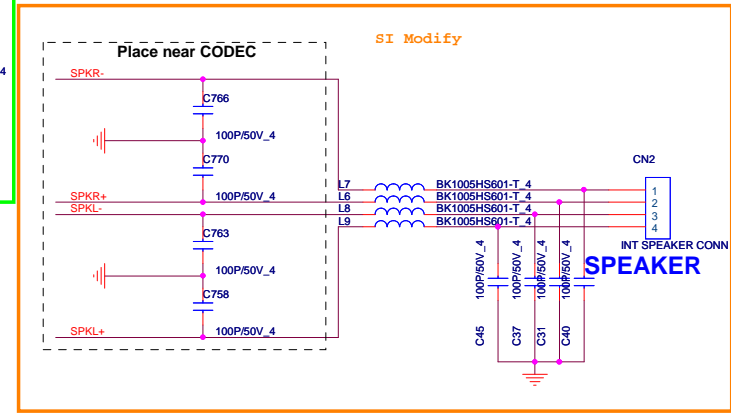
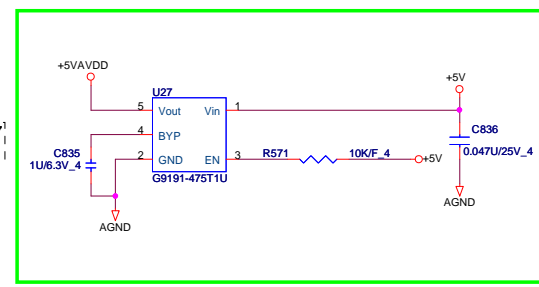
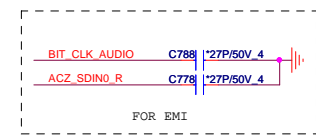


: ODD power down
 : ODD power on

<29> ODD_PD



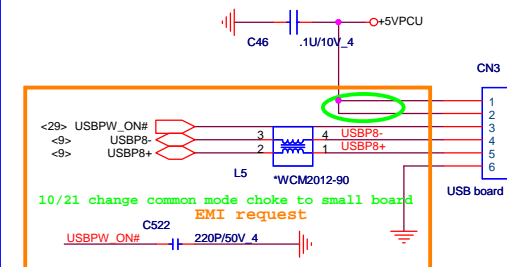
Size Custom	Document Number HDD/ODD/FAN	Rev 1A
Date: Thursday, November 12, 2009	Sheet 23 of 40	



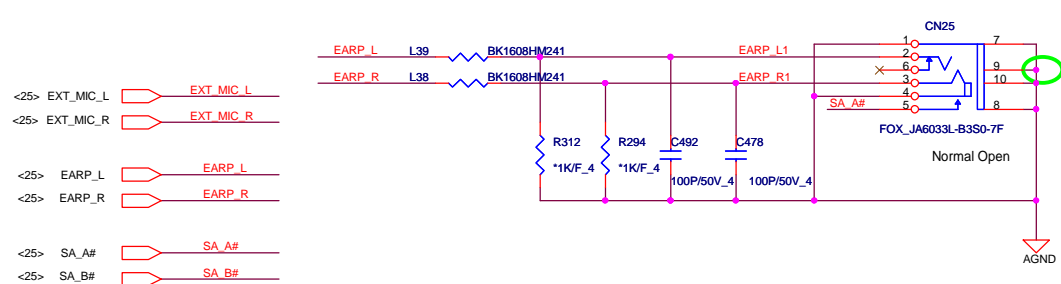
26



Right SIDE USBX1

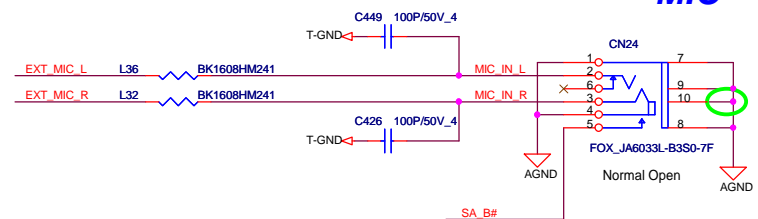


Line out



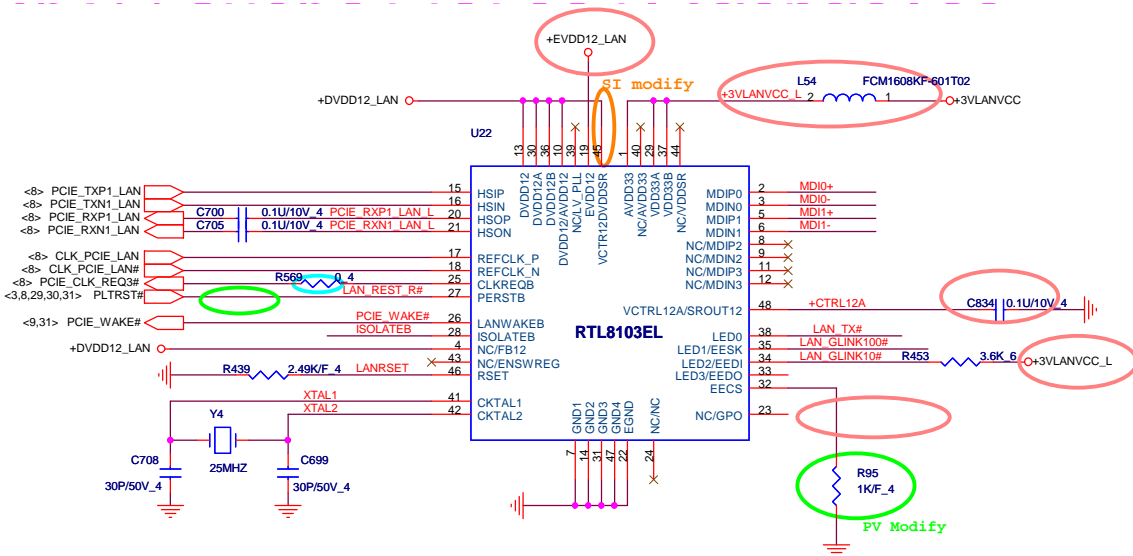
SA_A# -->EXT Ear Phone

SA_B# -->EXT MIC

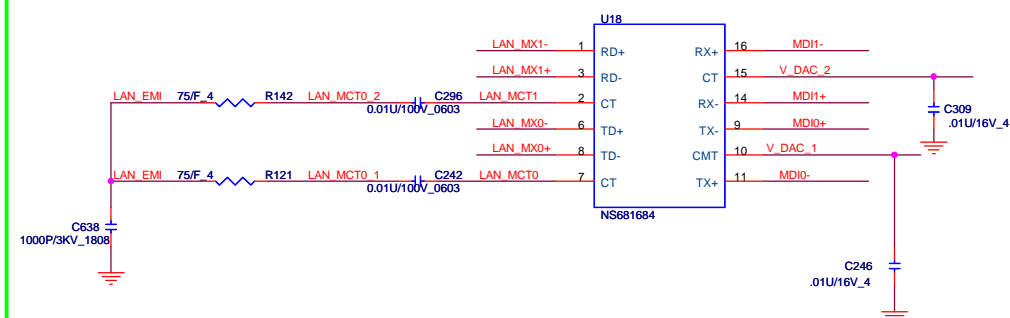
MIC

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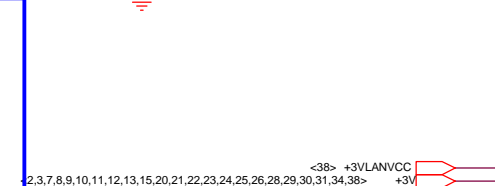
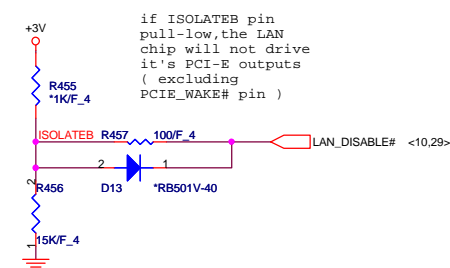
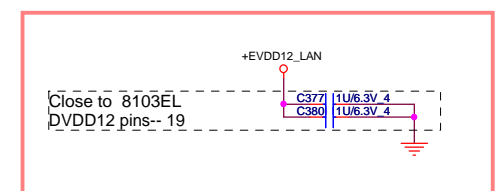
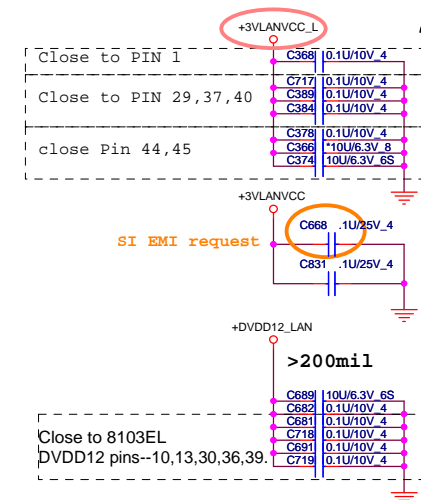
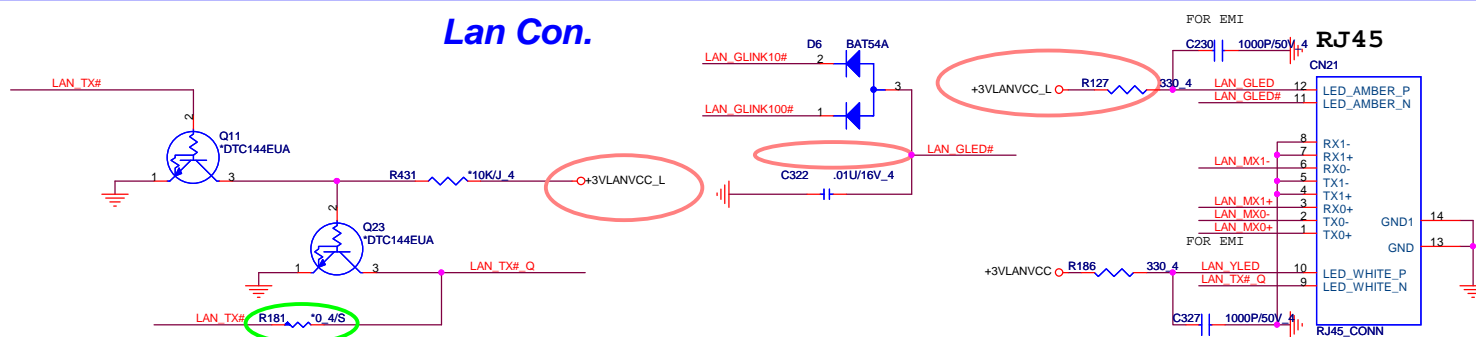
Size Custom	Document Number USB/BT/Modem/Audio Jack	Rev 1A
Date: Monday, November 30, 2009		Sheet 26 of 40



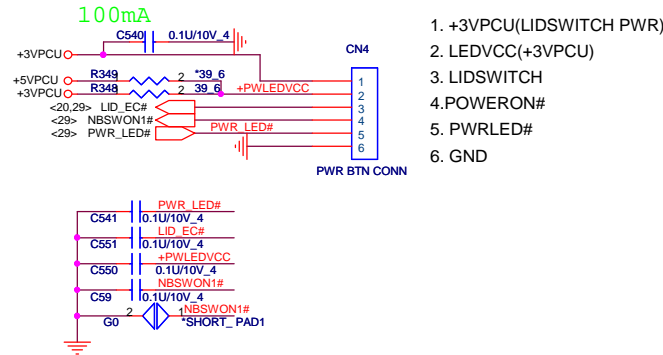
Transformer for 10/100



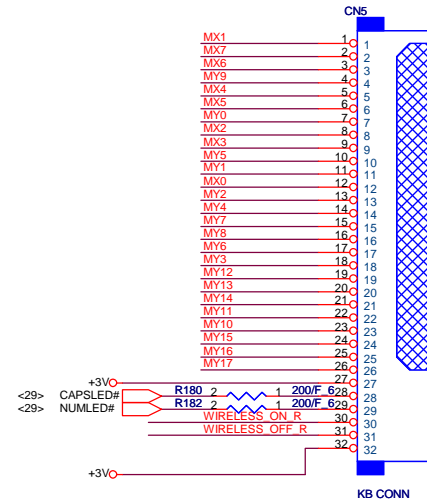
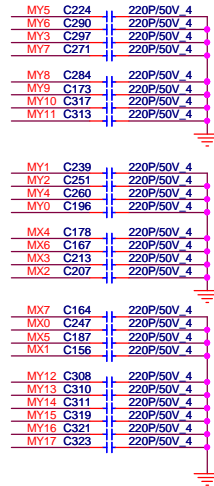
Lan Con.



POWER BUTTON CONNECT



KEYBOARD Con.

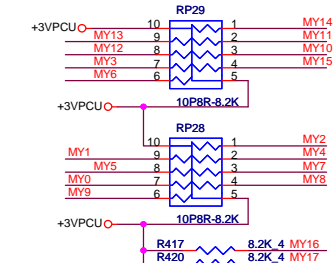


<29> MY[0..17] MY[0..17]

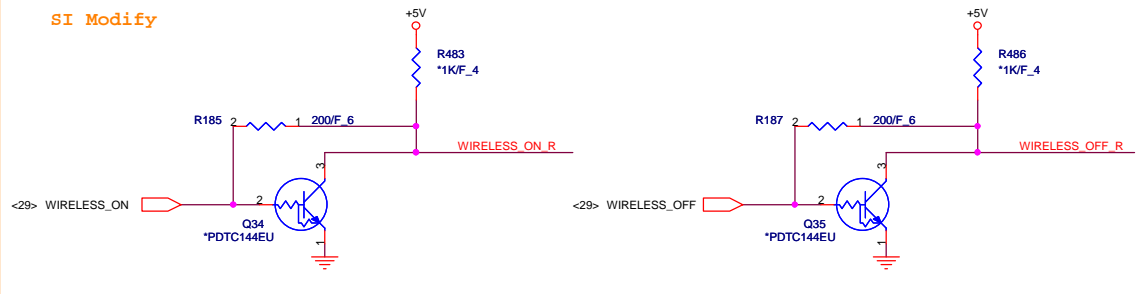
<29> MX[0..7] MX[0..7]

28

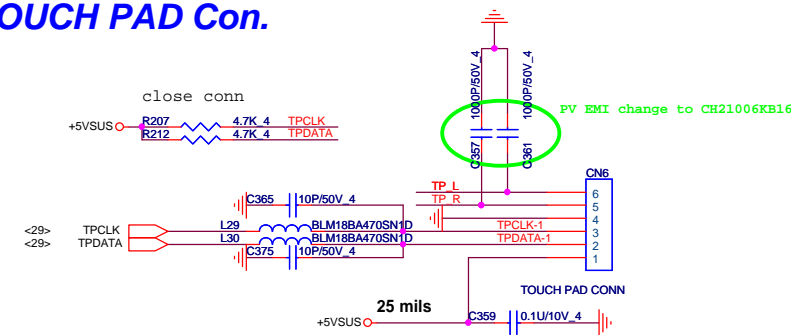
KEYBOARD PULL-UP



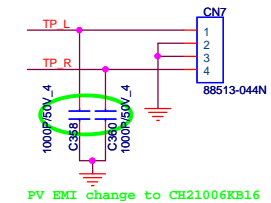
SI Modify



TOUCH PAD Con.



To TOUCH PAD SW board



PV EMI change to CH21006KB16

<7,20,26,29,31,32,33,36,38,39,40> +3VPCU

<11,20,21,22,23,25,31,38> +5V

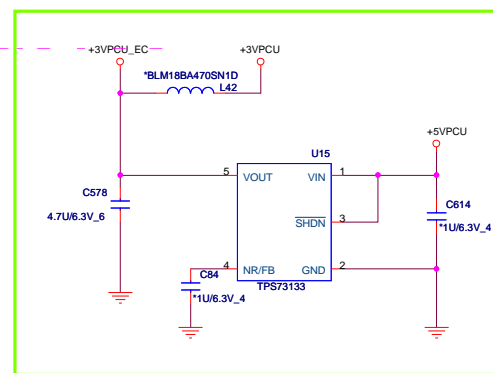
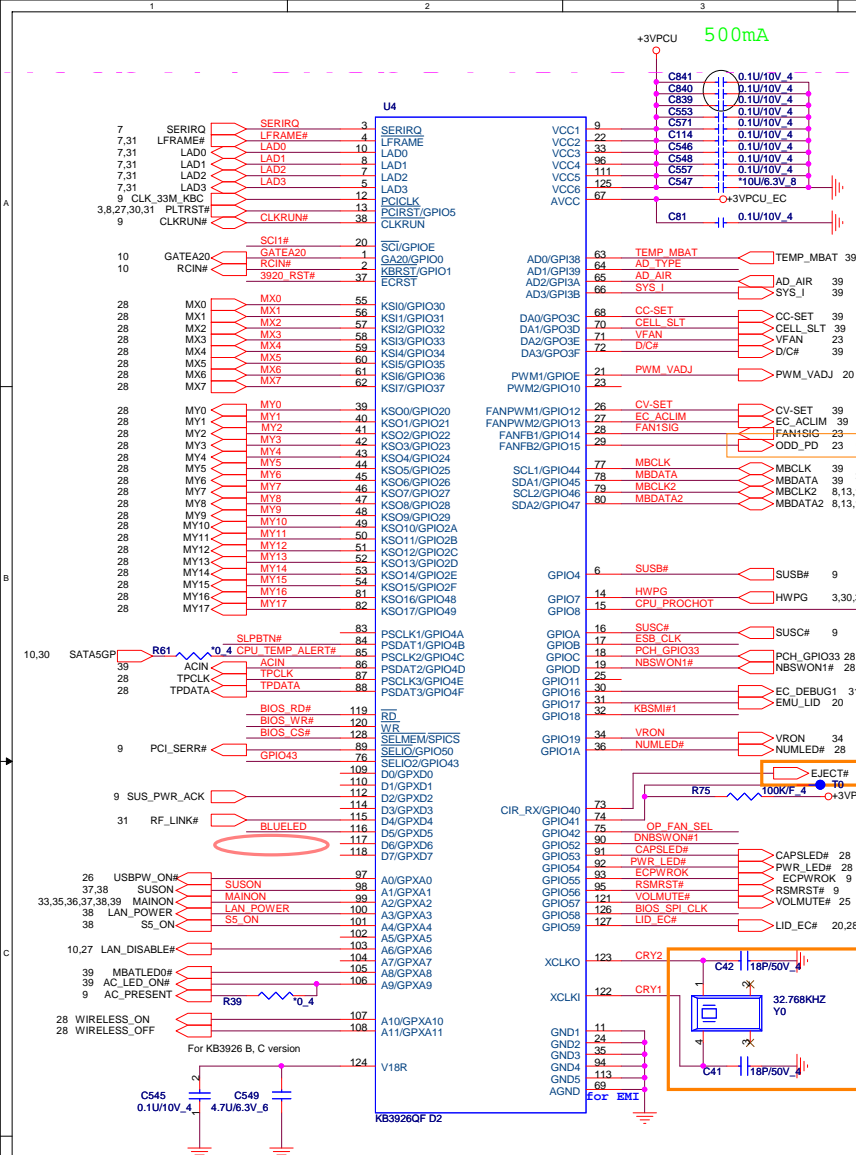
<20,38> +5VSUS

<2,3,7,8,9,10,11,12,13,15,20,21,22,23,24,25,26,27,29,30,31,34,38> +3V

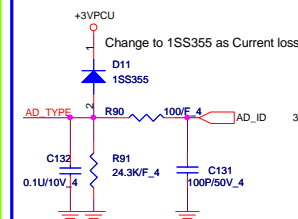


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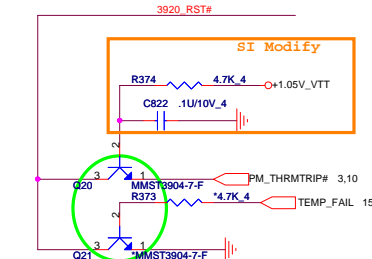
Size Custom Document Number LEB/KB/SW/TP Rev 1A
Date: Thursday, November 12, 2009 Sheet 28 of 40



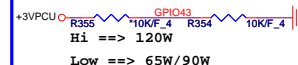
adapter Type check



thermal shutdown circuit

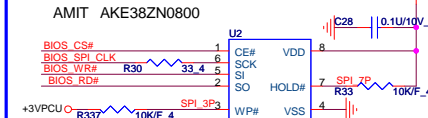


adapter select for EC



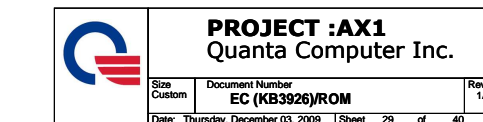
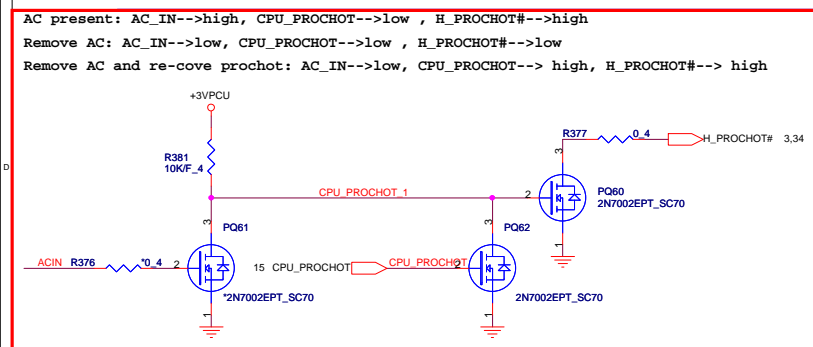
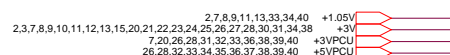
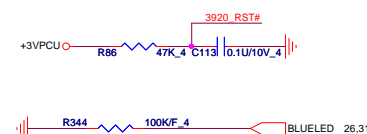
512K byte SPI EC ROM

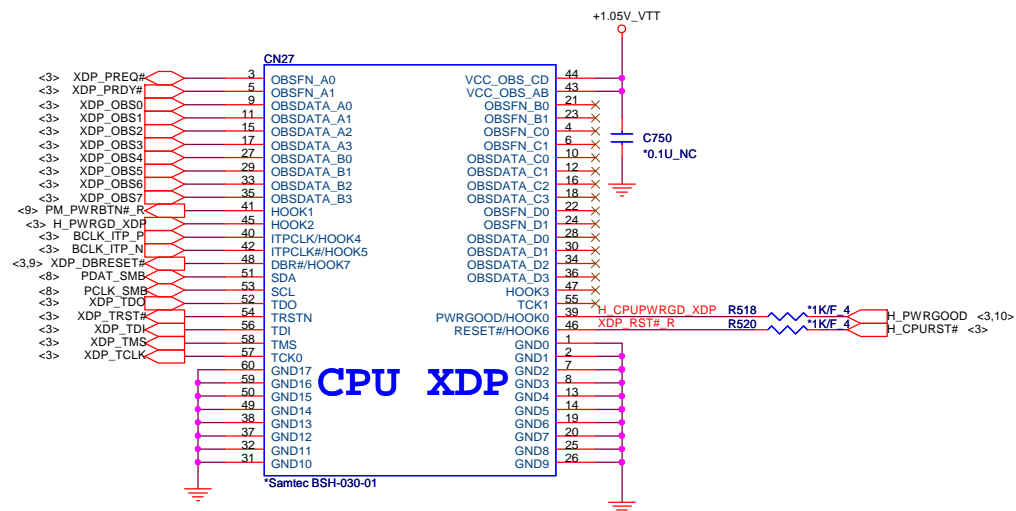
Socket: DG008000031
MXIC AKE3KZP0001
WINBOND AKE37ZN0N00
AMIT AKE38ZN0800



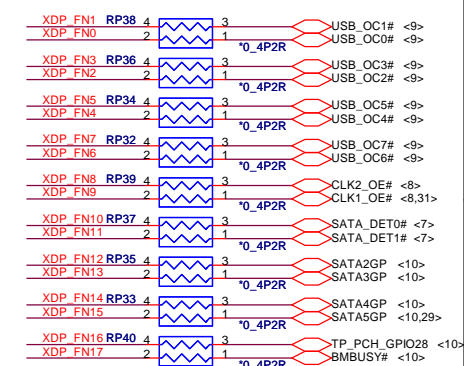
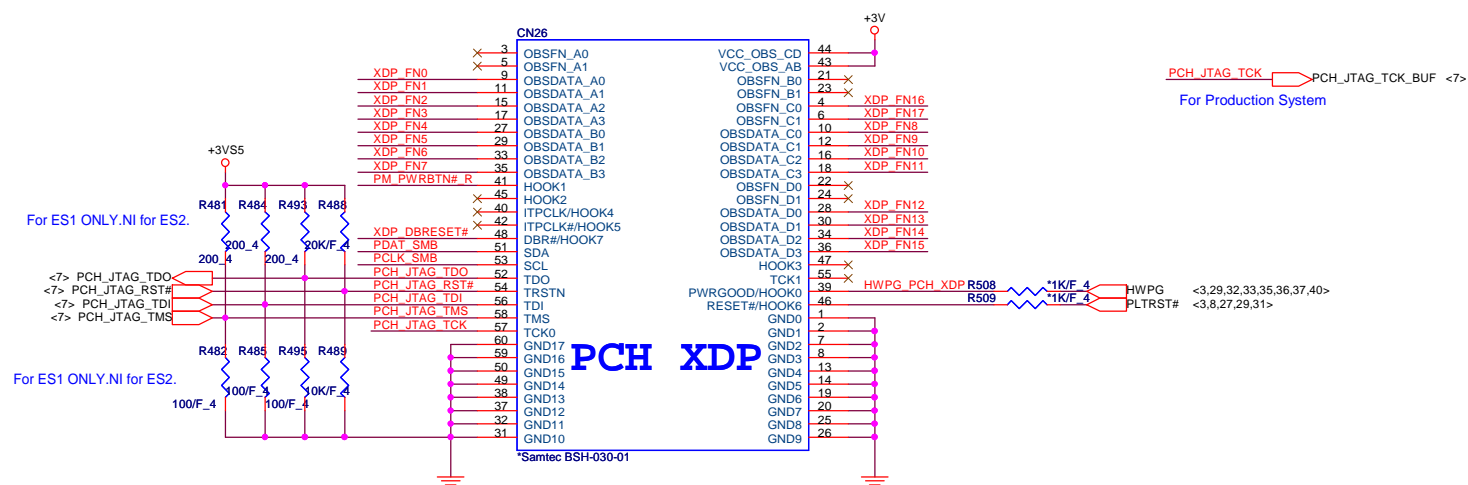
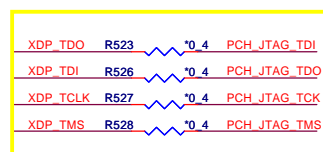
Project Model	GPI042
AX 14"	High
AX 15.6"	Low
AX 17.3"	Middle (1.5V)

GPIO42 control fan table

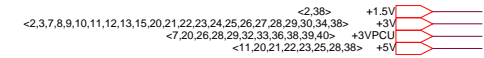
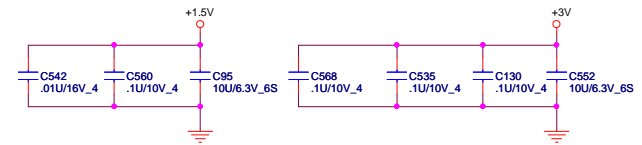




Reserve for BSDL



31



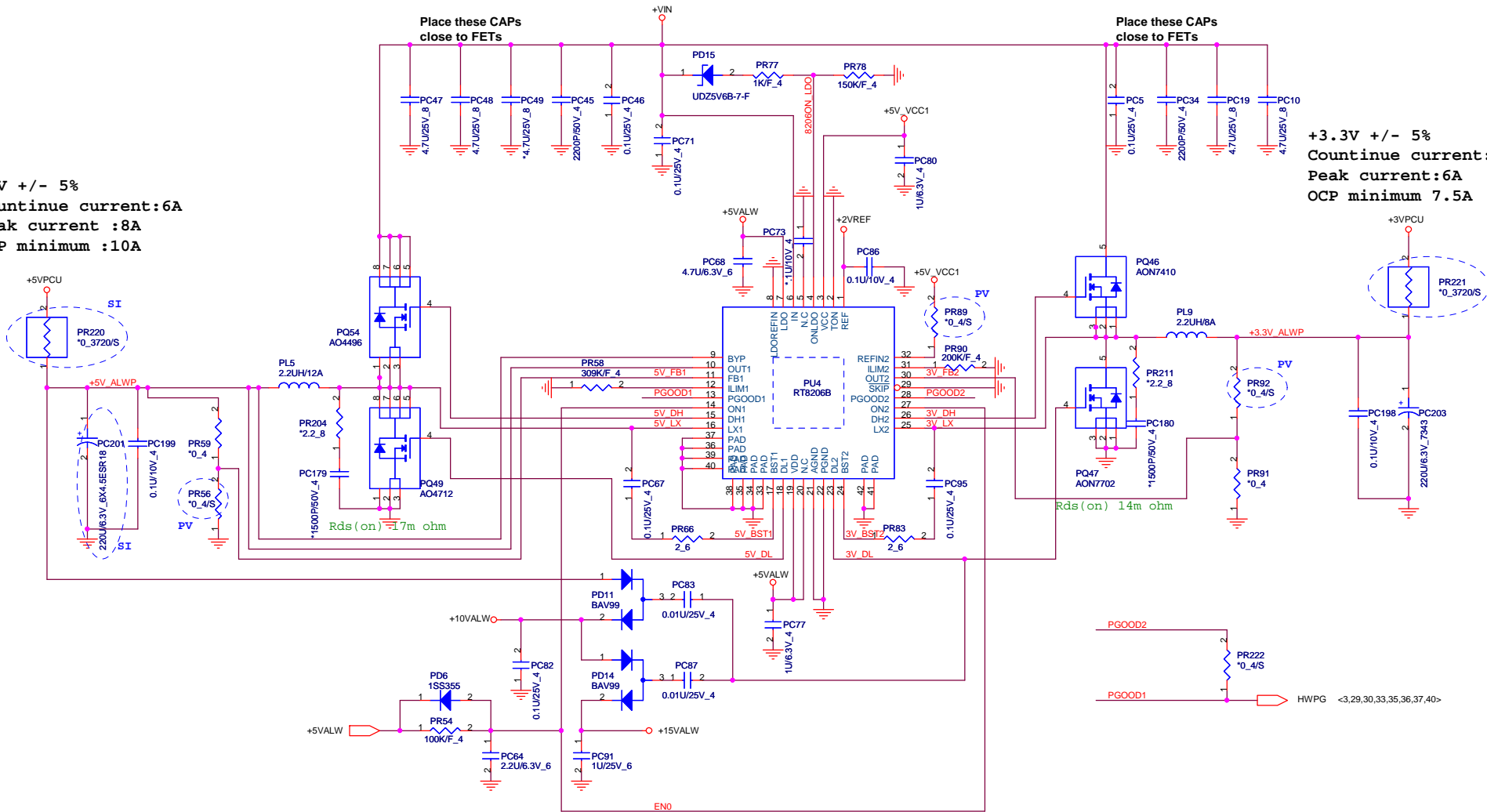
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

+5V +/- 5%
Countinue current:6A
Peak current :8A
OCP minimum :10A

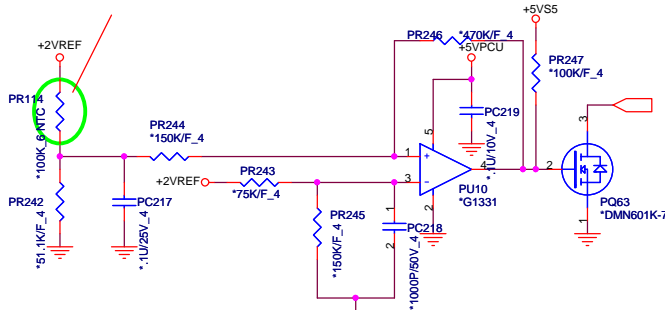
+3.3V +/- 5%
Countinue current:5A
Peak current:6A
OCP minimum 7.5A

Place these CAPs
close to FETs

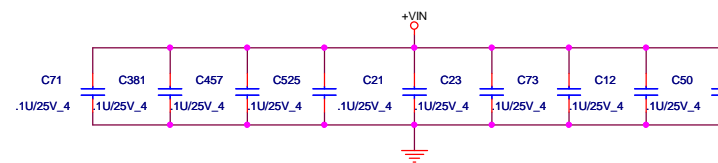
Place these CAPs
close to FETs



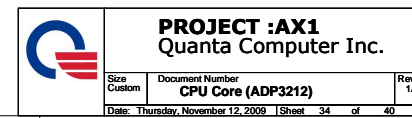
NTC need place under CPU Socket
CPU Thermal protection at 90 +/-3 degrec

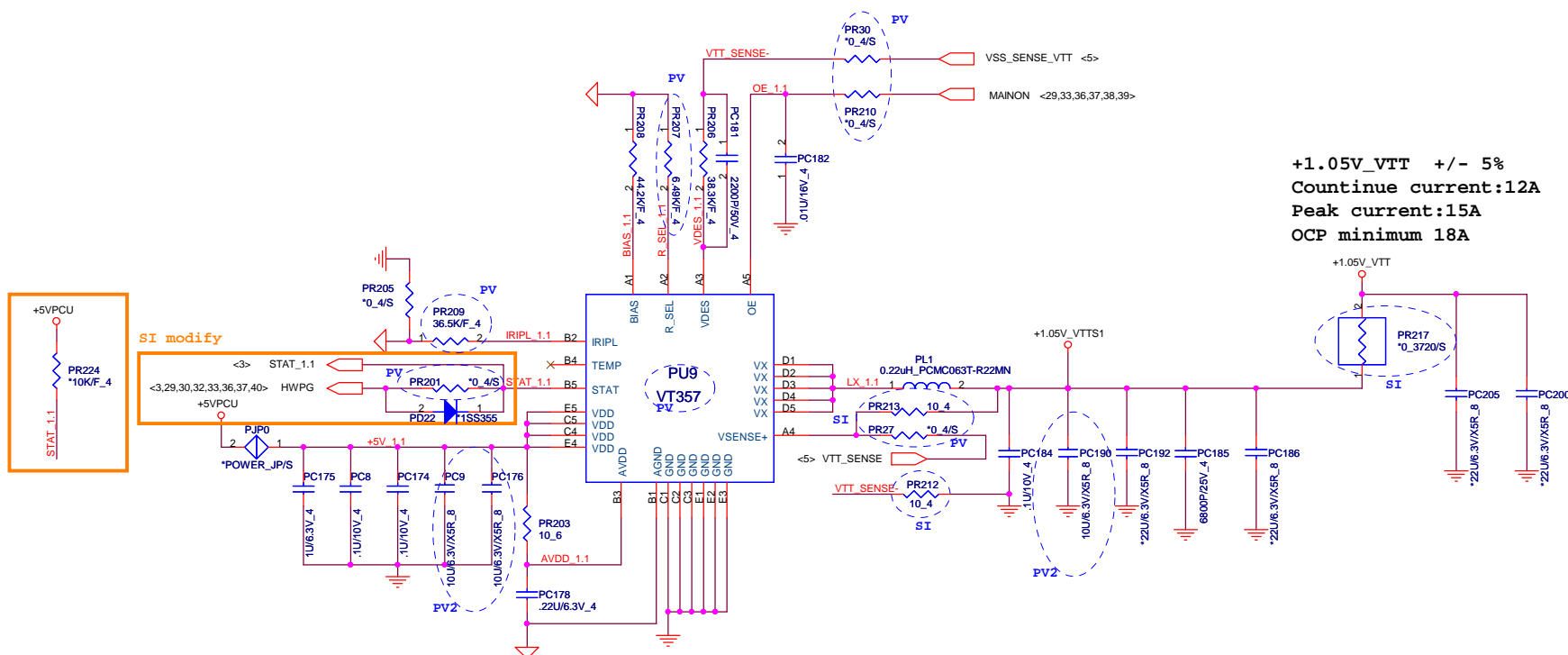


EMI request



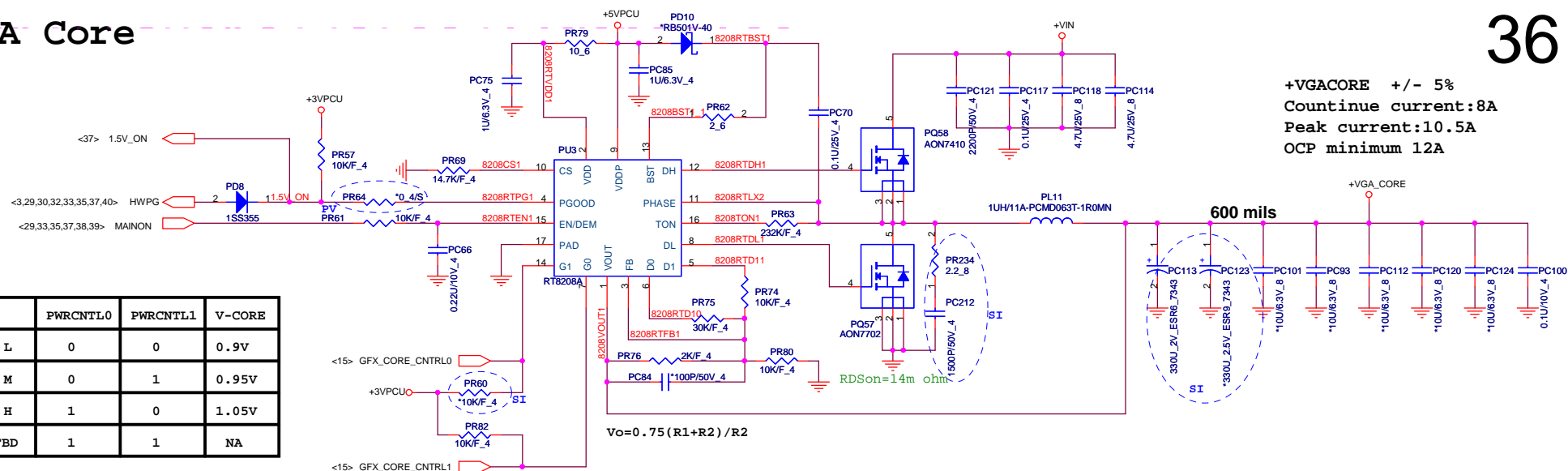






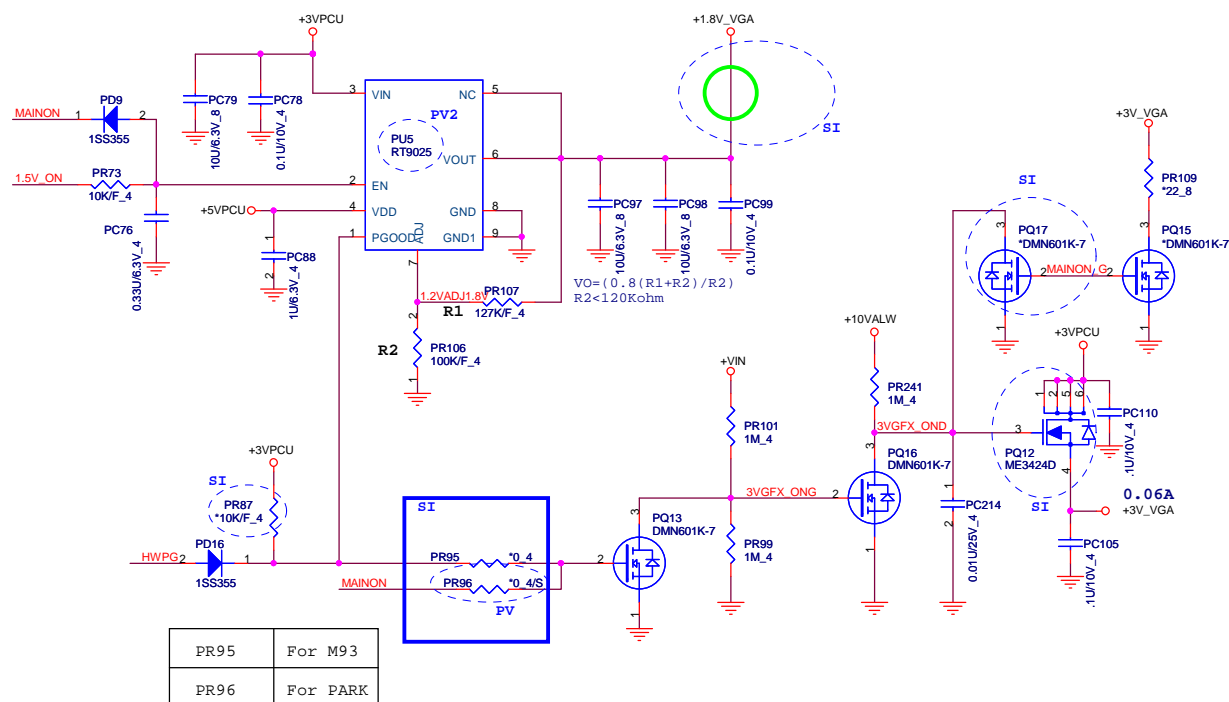
36

	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	0.95V
H	1	0	1.05V
TBD	1	1	NA



+VGACORE +/- 5%
Countinue current:8A
Peak current:10.5A
OCP minimum 12A

+1.8V +/- 5%
Continue current:1.2A
Peak current:3A



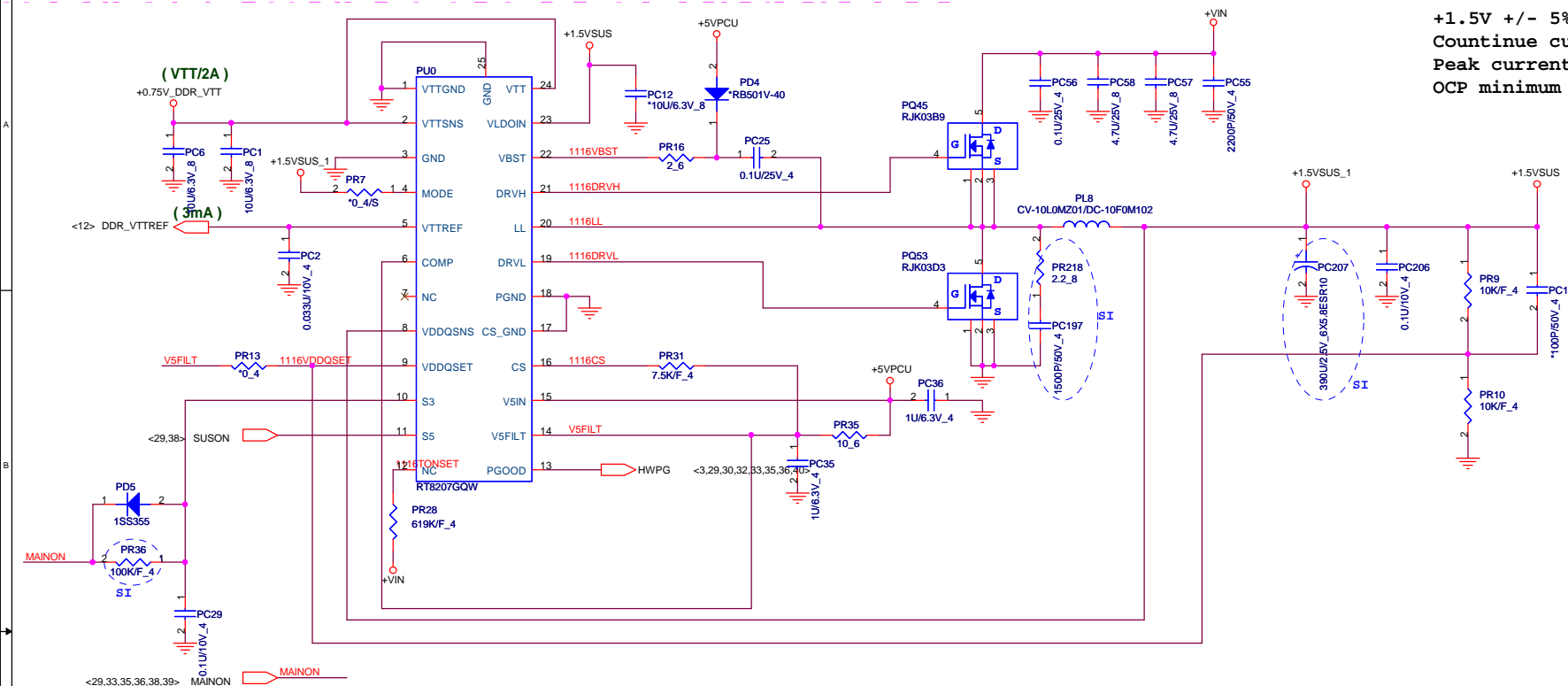
PR95	For M93
PR96	For PARK



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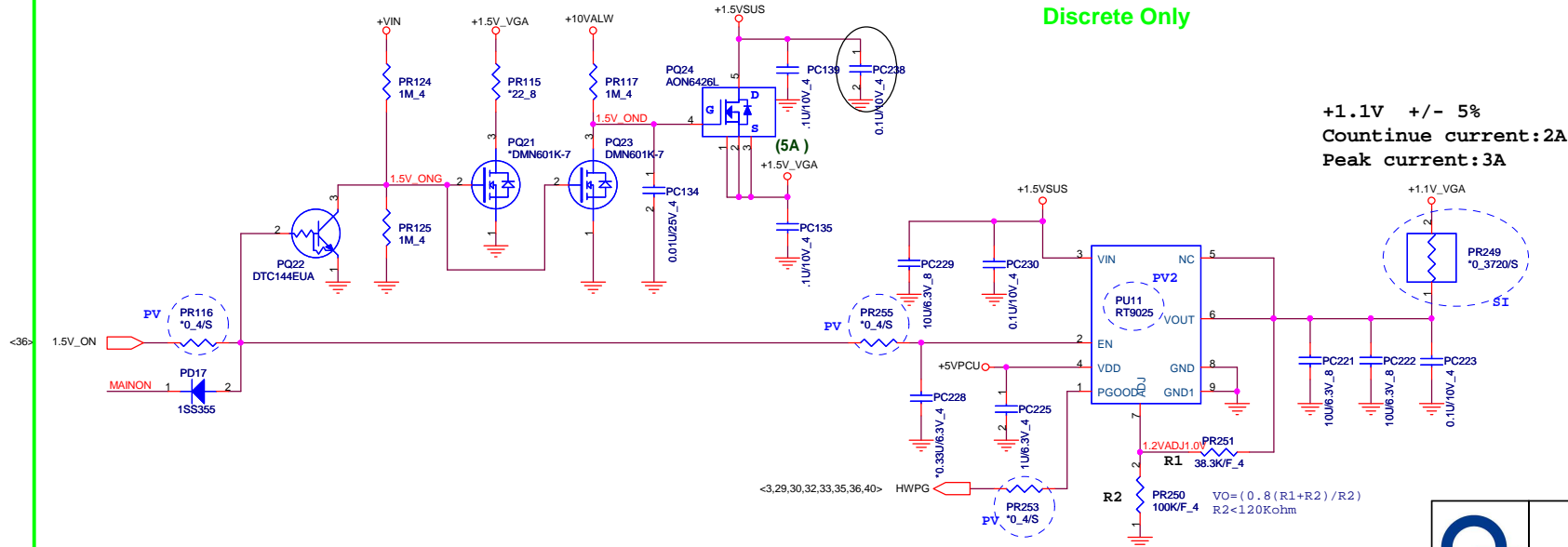
Size Custom	Document Number +VGACORE (RT8208/1.8V)	Re 1
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+1.5V +/- 5%
 Countinue current:6A
 Peak current:12A
 OCP minimum 15A



Discrete Only

+1.1V +/- 5%
 Countinue current:2A
 Peak current:3A



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