RYU2-13 CALPELLA UMA Schematics

Intel ULV CPU-Arrandale SFF

Intel Ibex Peak-M

2010-09-28

REV : A00

DY : Nopop Component

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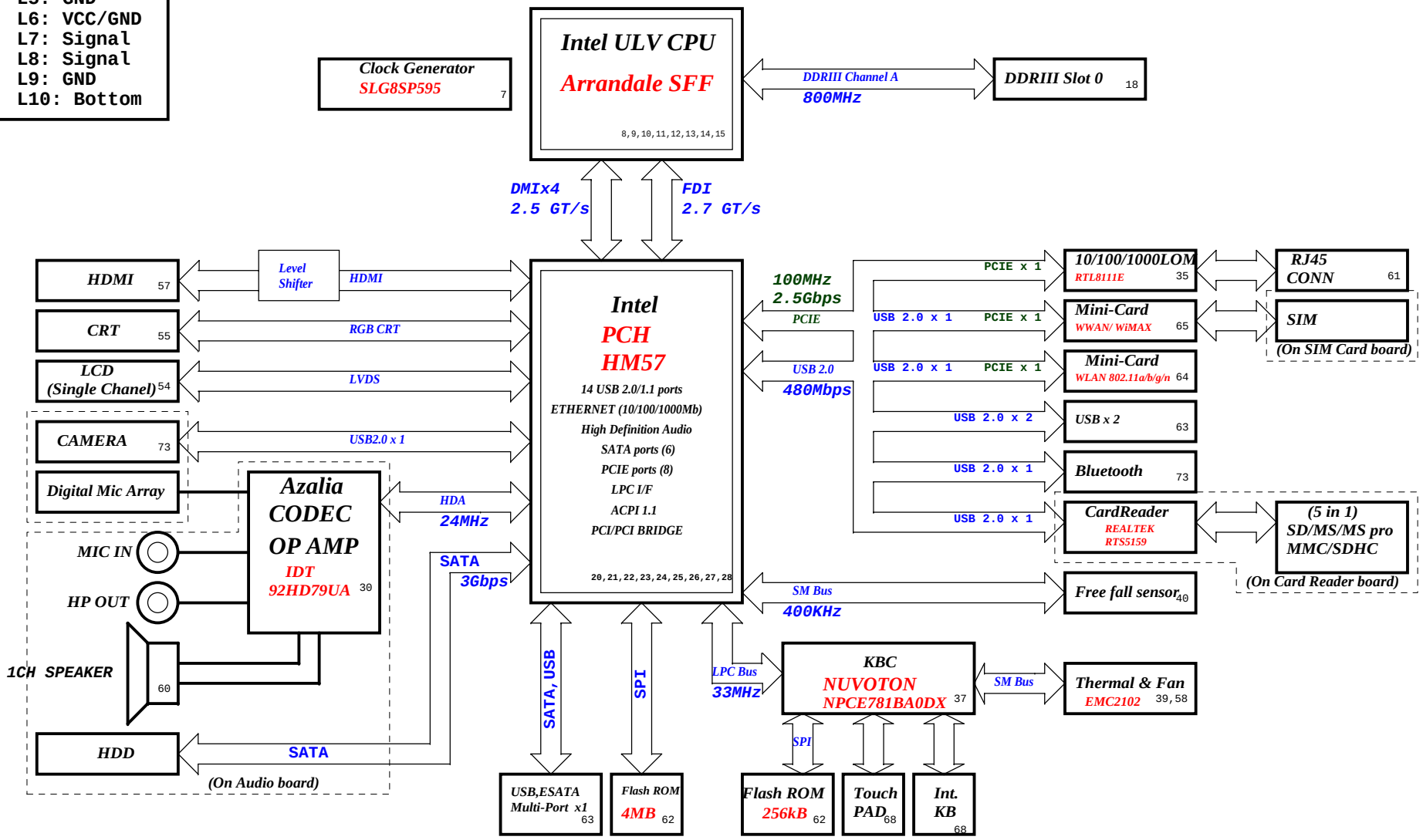
Title	***Cover Page***	
Size: Custom	Document Number: ***RYU2 13 UMA***	Rev: ***A00***
Date: Tuesday, September 28, 2010	Sheet 1 of 92	

RYU2 CALPELLA Block Diagram

Project code : 91.4M101.001
Part Number : 48.4M101.0SB
PCB P/N : 10251
Revision : SB

PCB LAYER

L1: Top
L2: GND
L3: Signal
L4: Signal
L5: GND
L6: VCC/GND
L7: Signal
L8: Signal
L9: GND
L10: Bottom



CPU DC/DC RT8152DGQW-GP 47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51123RGER 46	
INPUTS	OUTPUTS
+PWR_SRC	+15V_ALW +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

SYSTEM DC/DC RT8207LGQW-GP-U 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

SYSTEM DC/DC ADP3211 53	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFXCORE

CHARGER BQ24745 45	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

SYSTEM DC/DC RT8209PGQW 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_PCH

SYSTEM DC/DC TPS51311RGTR 51	
INPUTS	OUTPUTS
+3.3V_RUN	+1.8V_RUN

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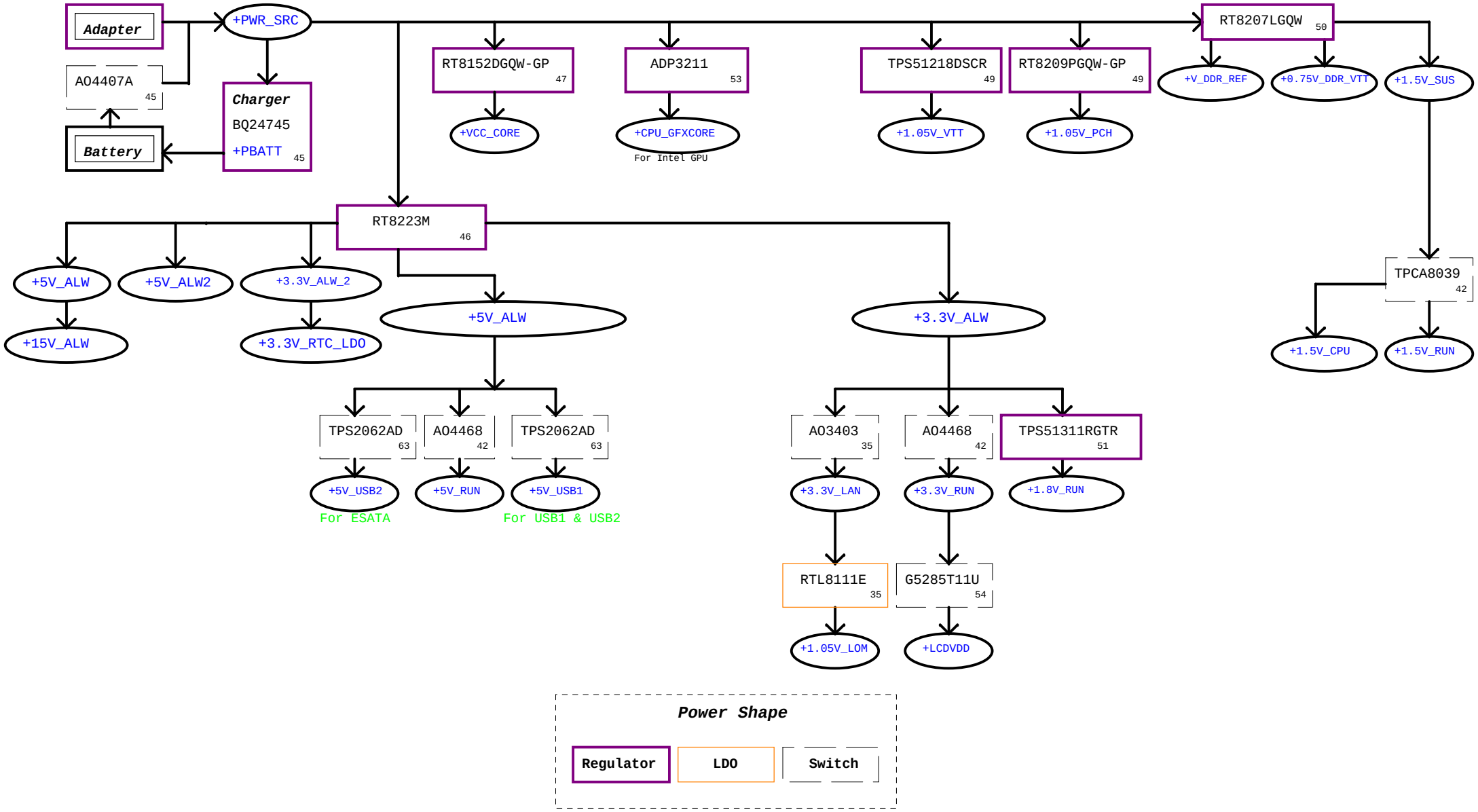
Title: Block Diagram
Size: Custom
Document Number: RYU2 13 UMA
Rev: A00
Date: Tuesday, September 28, 2010
Sheet 2 of 92



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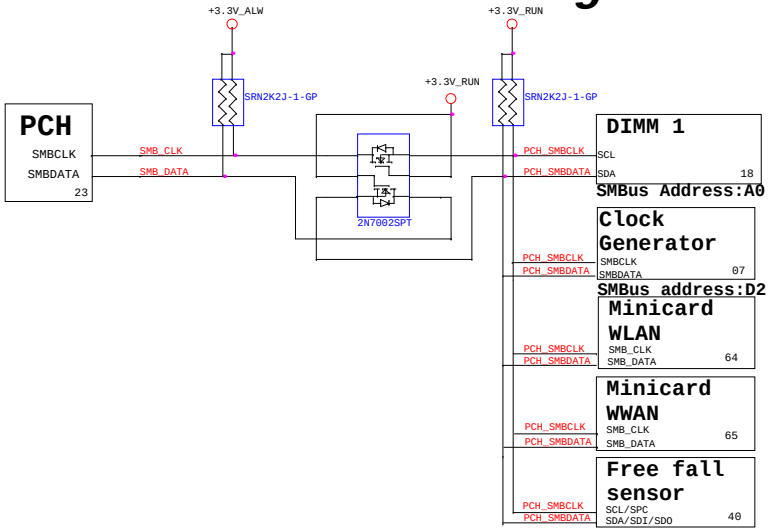
Title: **Power Block Diagram**

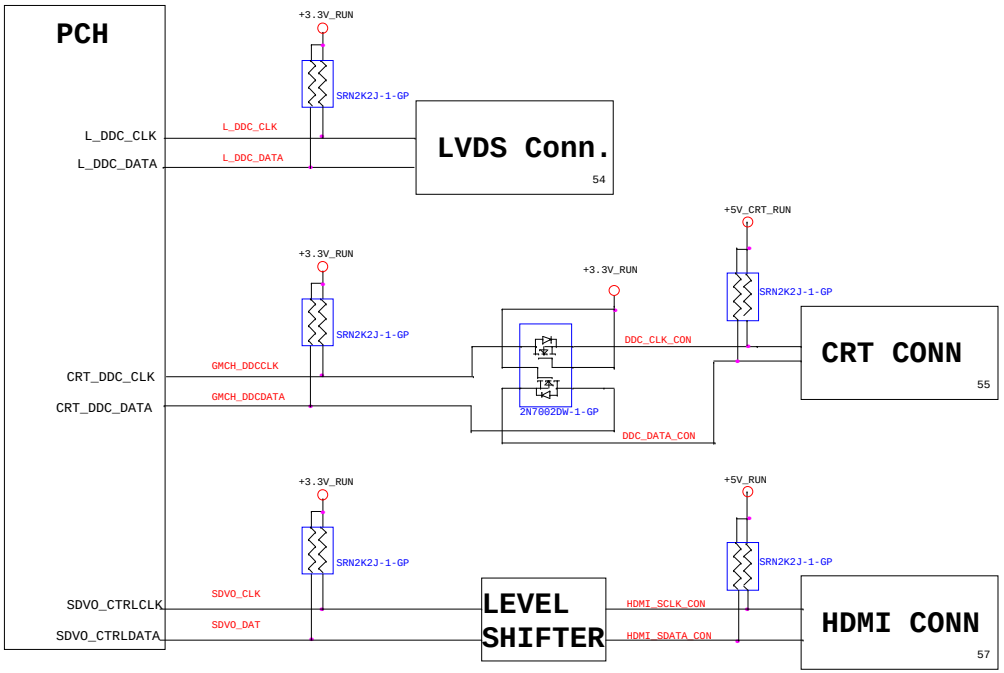
Size	Document Number	Rev
Custom	RYU2 13 UMA	A00

Date: Tuesday, September 28, 2010 Sheet 3 of 92

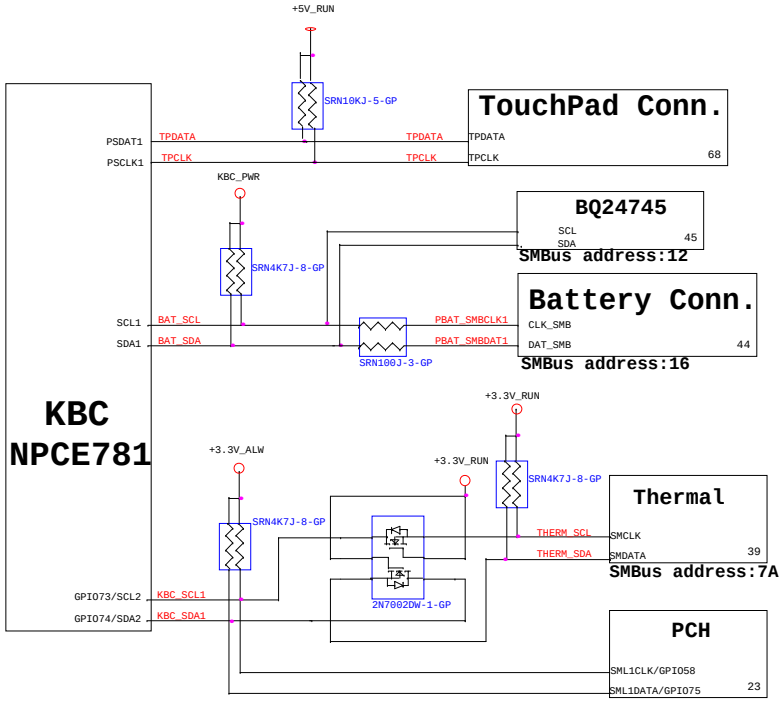
PCH SMBus Block Diagram



Graphic SMBus Block Diagram



KBC SMBus Block Diagram



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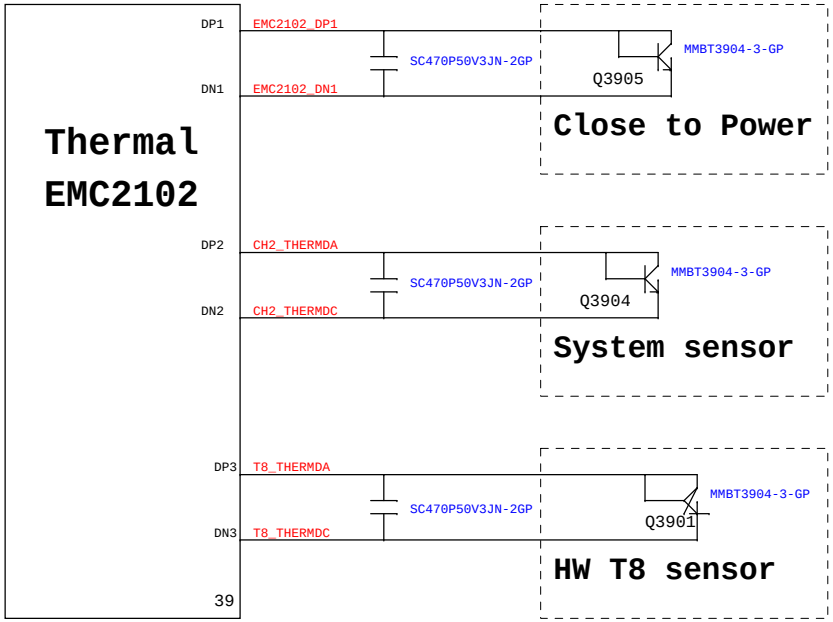
Title: SMBUS Block Diagram

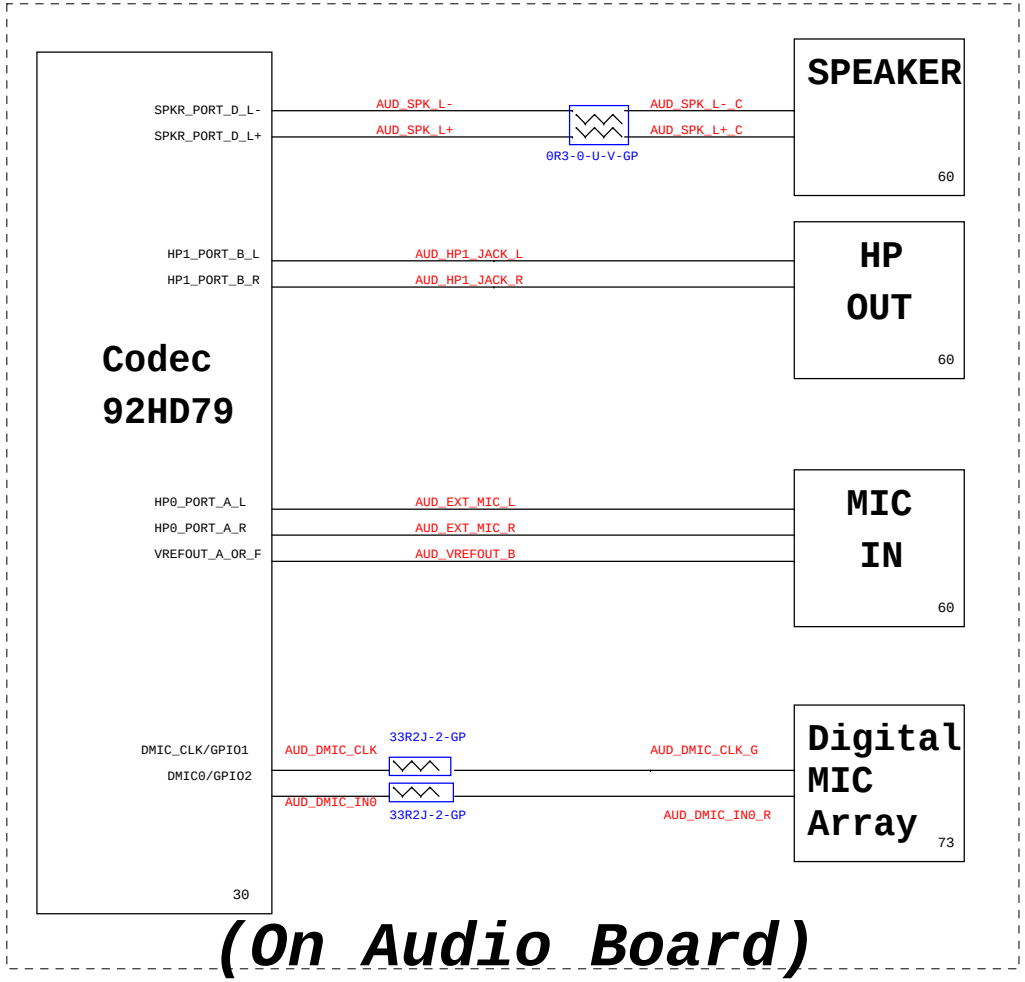
Size	Document Number	Rev
C	RYU2 13 UMA	A00

Date: Tuesday, September 28, 2010 Sheet 4 of 92

Thermal Block Diagram



Audio Block Diagram



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Title	Thermal/Audio Block Diagram	
Size: Custom	Document Number: RYU2 13 UMA	Rev: A00
Date: Tuesday, September 28, 2010	Sheet 5 of 92	

PCH Strapping Calpella Schematic Checklist Rev2.0

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor. Intel suggest 1K resistor (Fonseca)
INIT3_3V#	Internal pull-up. Leave as "No Connect"
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** Note: Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 kΩ; do not stuff resistor.
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled** **Note:** CRB uses a 330-kΩ resistor.
GNT0#, GNT1#	**Default (SPI):** Leave both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor. Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
SPI_MOSI	**Enable Intel Anti-Theft Technology:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Intel Anti-Theft Technology:** Left floating, no pull-down required.
NV_ALE	**Enable Intel Anti-Theft Technology:** Connect to +NVRAM_Vccq with 8.2-kΩ weak pull-up resistor.[CRB has it pulled up with 1-kΩ no-stuff resistor] **Disable Intel Anti-Theft Technology:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0)-** Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. **High (1)-:** Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. **Note:** CRB recommends 1-kΩ pull-down for FD Override. There is an internal pull-up of 20 kΩ for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	**Low (0)-**Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality **High (1)-:** Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality **Note:** This is an unmuxed signal. This signal has a weak internal pull-down of 20 KΩ which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kΩ pull-up on this signal to +3.3VA rail.
GPIO8	Weak internal pull-up. Do not pull low. Sampled at rising edge of RSMRST#.
GPIO27	**Default = Do not connect (floating). Internal pull-up.** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping Calpella SFF Schematic Checklist Rev2.1

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	1:Disabled - No Physical Di splay Port attached to Embedded DisplayPort 0:Enabled - An external DisplayPort device is connected to the Embedded DisplayPort	1
CFG[3]	**PCI-Express Static Lane Reversal**	1:Normal Operation 0: Lane Numbers Reversed 15 -> 0, 14 -> 1	1
CFG[0]	**PCI-Express Configuration Select**	1: Single PCI-Express Graphics 0: Bifurcation enabled	1

PCIE Routing

LANE1	RESERVE
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	MiniCard WWAN
LANE5	RESERVE

USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	USB for ESATA
3	RESERVE
4	WLAN
5	WWAN
6	RESERVED (Not available for HM55)
7	RESERVED (Not available for HM55)
8	BlUETOOTH
9	Card Reader
10	RESERVED
11	CAMERA
12	RESERVED
13	RESERVED

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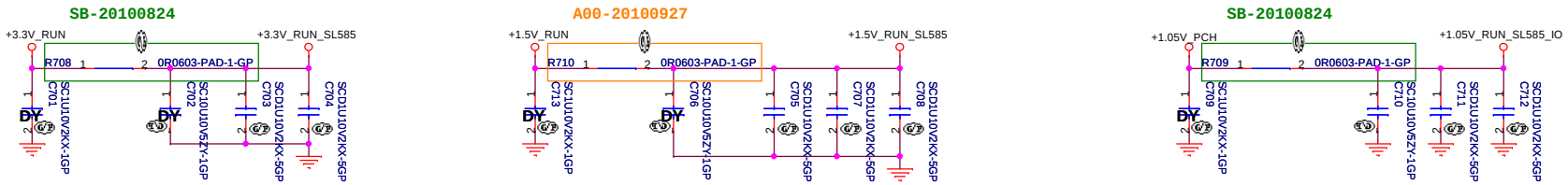
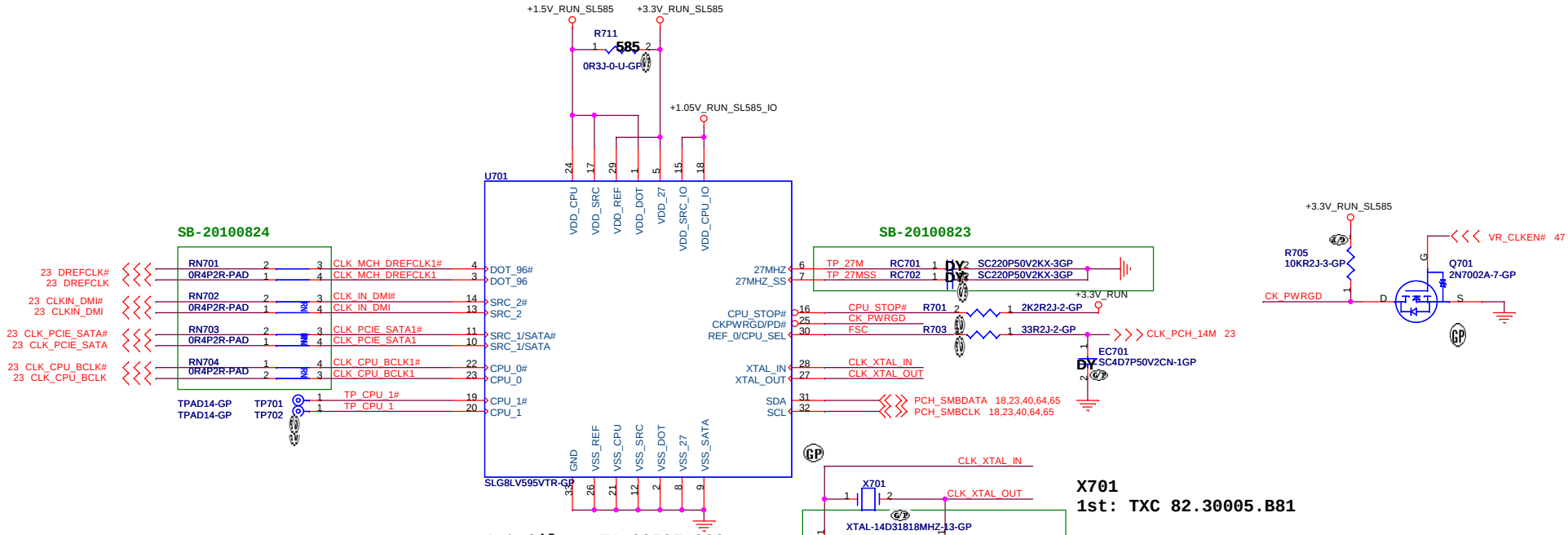
Title: Table of Content

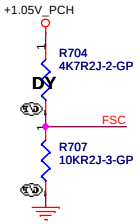
Size: Custom | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 6 of 92

SSID = Clock GEN







FSC	0	1
SPEED	133MHz (Default)	100MHz

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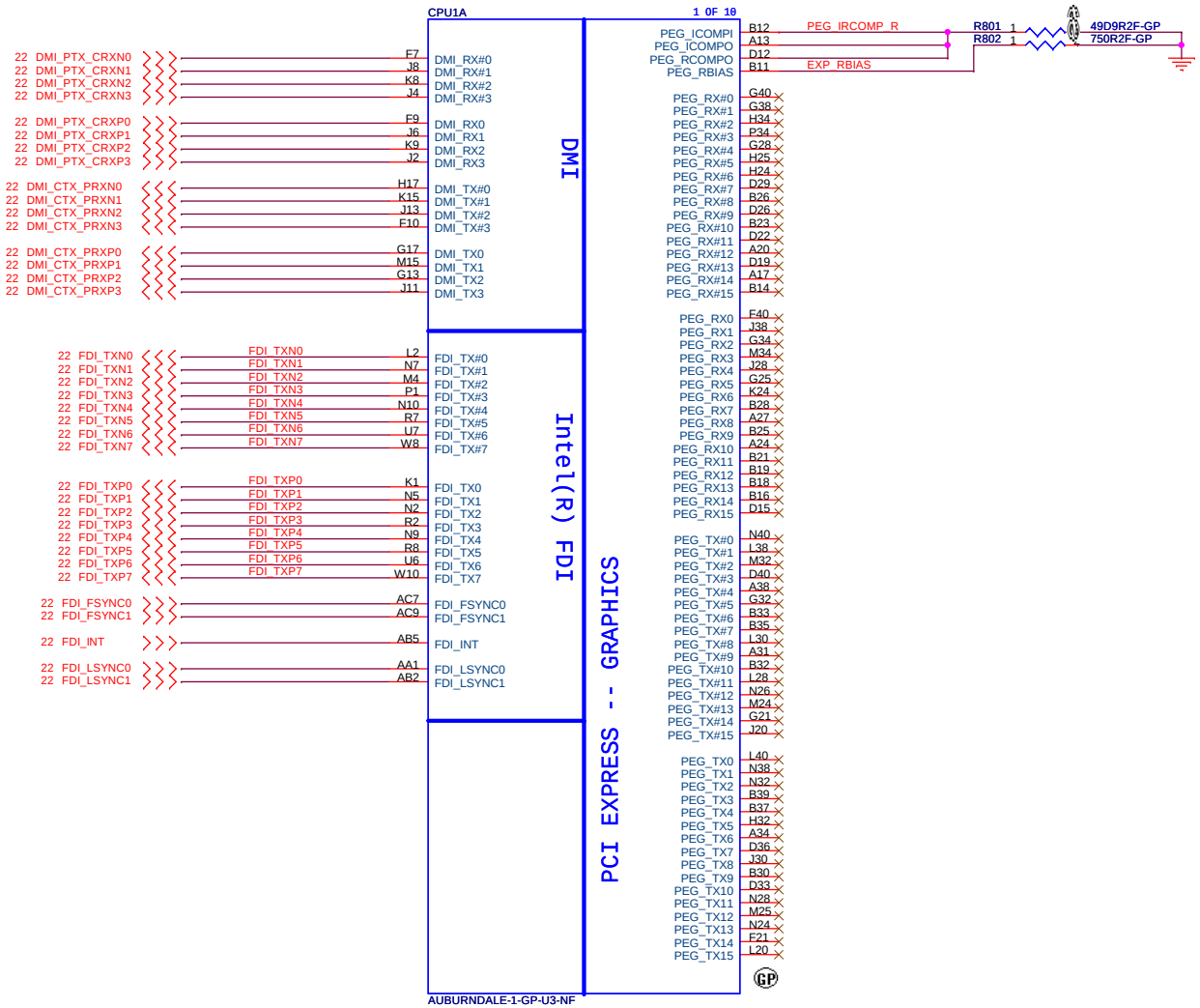
Title: Clock Generator SLG8SP585

Size | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 7 of 92

SSID = CPU



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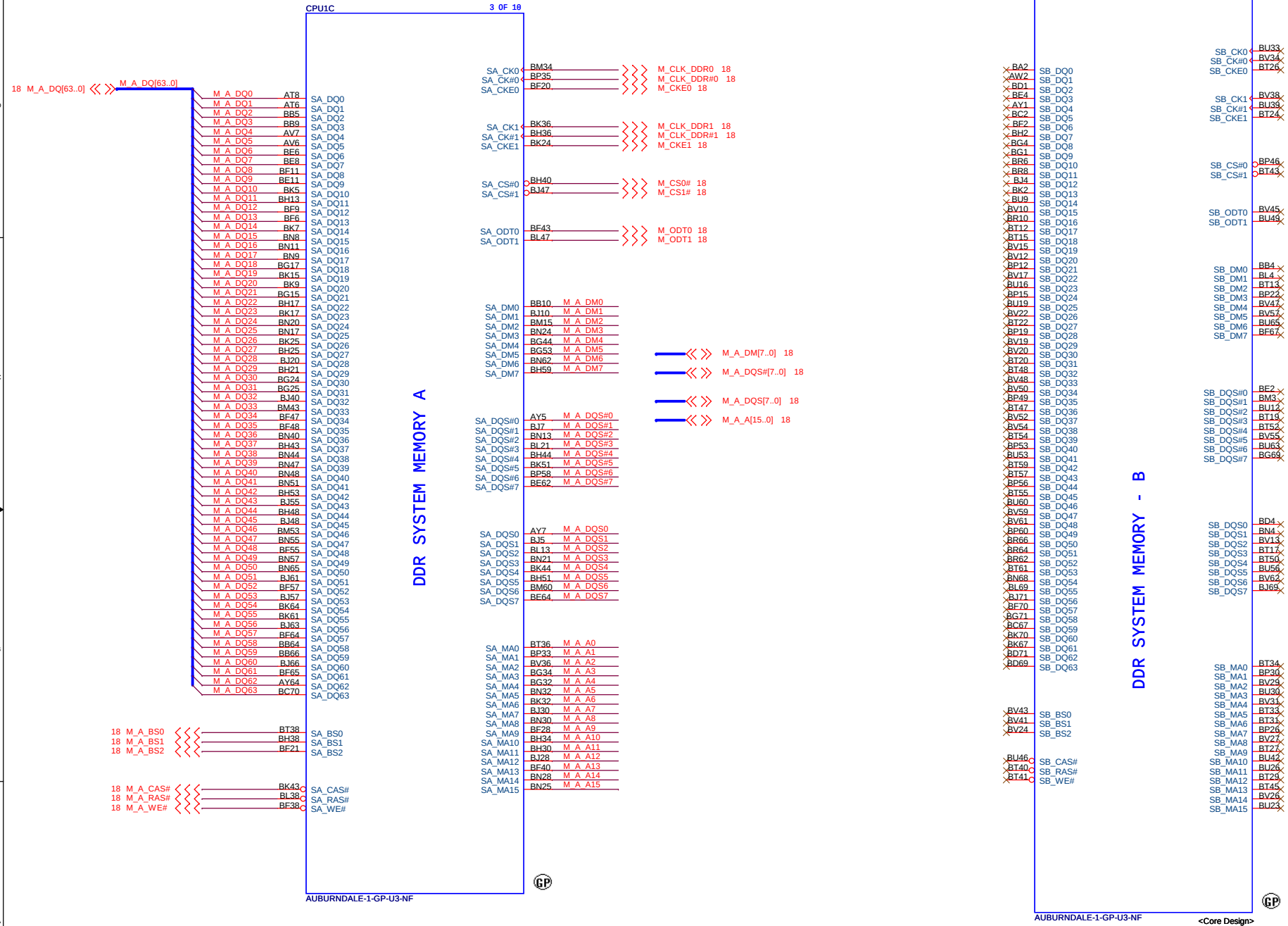
Title: CPU (PCIE/DMI/FDI)-1/8

Size	Document Number	Rev
	RYU2 13 UMA	A00

Date: Tuesday, September 28, 2010 Sheet 8 of 92

SSID = CPU



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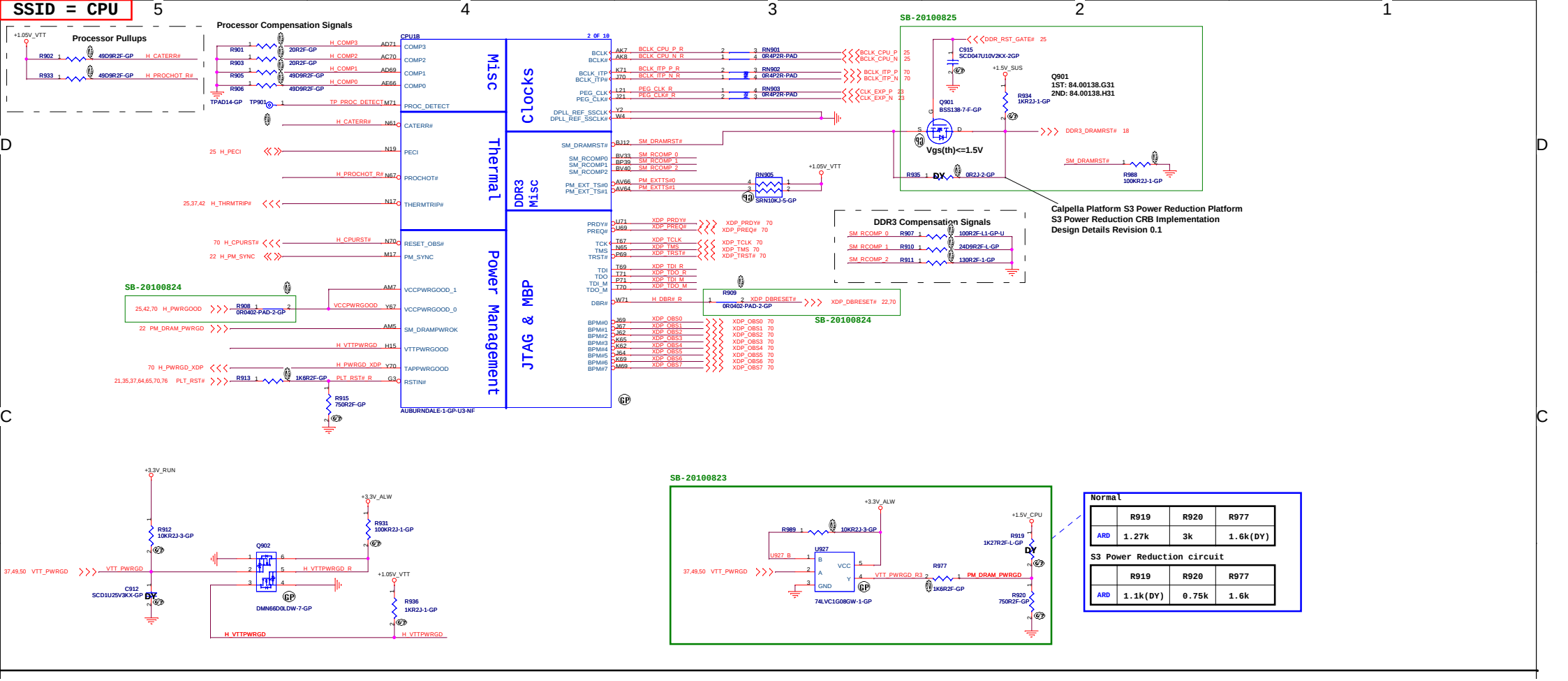
Title		
	CPU (DDR)-2/8	
Size	Document Number	Rev
	RYU2 13 UMA	A00

Date: Tuesday, September 28, 2010 Sheet 9 of 92

SSID = CPU



Normal

	R919	R920	R977
ARD	1.27k	3k	1.6k(DY)

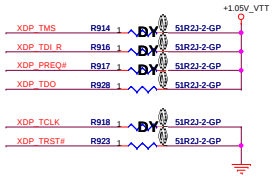
S3 Power Reduction circuit

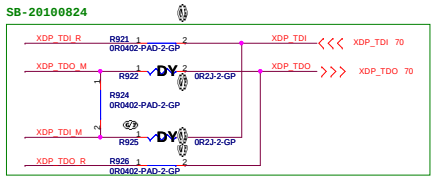
	R919	R920	R977
ARD	1.1k(DY)	0.75k	1.6k

XDP Connector

+1.05V_VCCP use Decoupling Capacitor close ITP connector 100 mil (max)

CPU	XDP_Connector
TCK(PIN AN28)	TCK(PIN 57)





Scan Chain (Default)	Stuff --> R921, R924, R926 No Stuff --> R922, R925
CPU Only	Stuff --> R921, R922 No Stuff --> R924, R926, R925
GMCH Only	Stuff --> R926, R925 No Stuff --> R921, R922, R924

JTAG MAPPING

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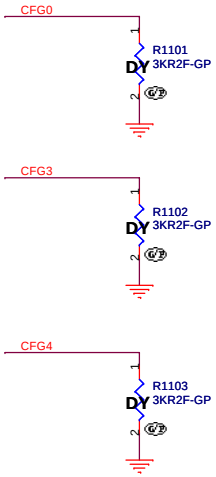
Title: CPU (THERMAL/CLOCK/PM)-3/8
Size | Document Number: RYU2 13 UMA | Rev: A00
Date: Tuesday, September 28, 2010 | Sheet 10 of 92

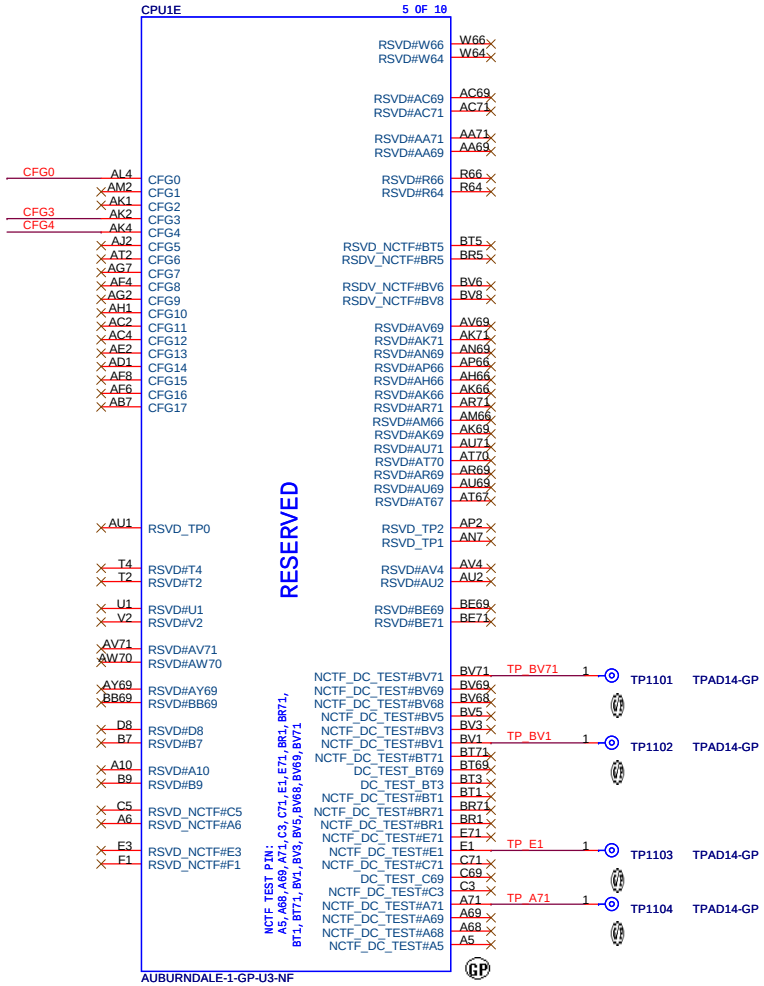
SSID = CPU



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Embedded DisplayPort Presence	
CFG4	1:Disabled - No Physical Di splay Port attached to Embedded DisplayPort 0:Enabled - An external DisplayPort device is connected to the Embedded DisplayPort



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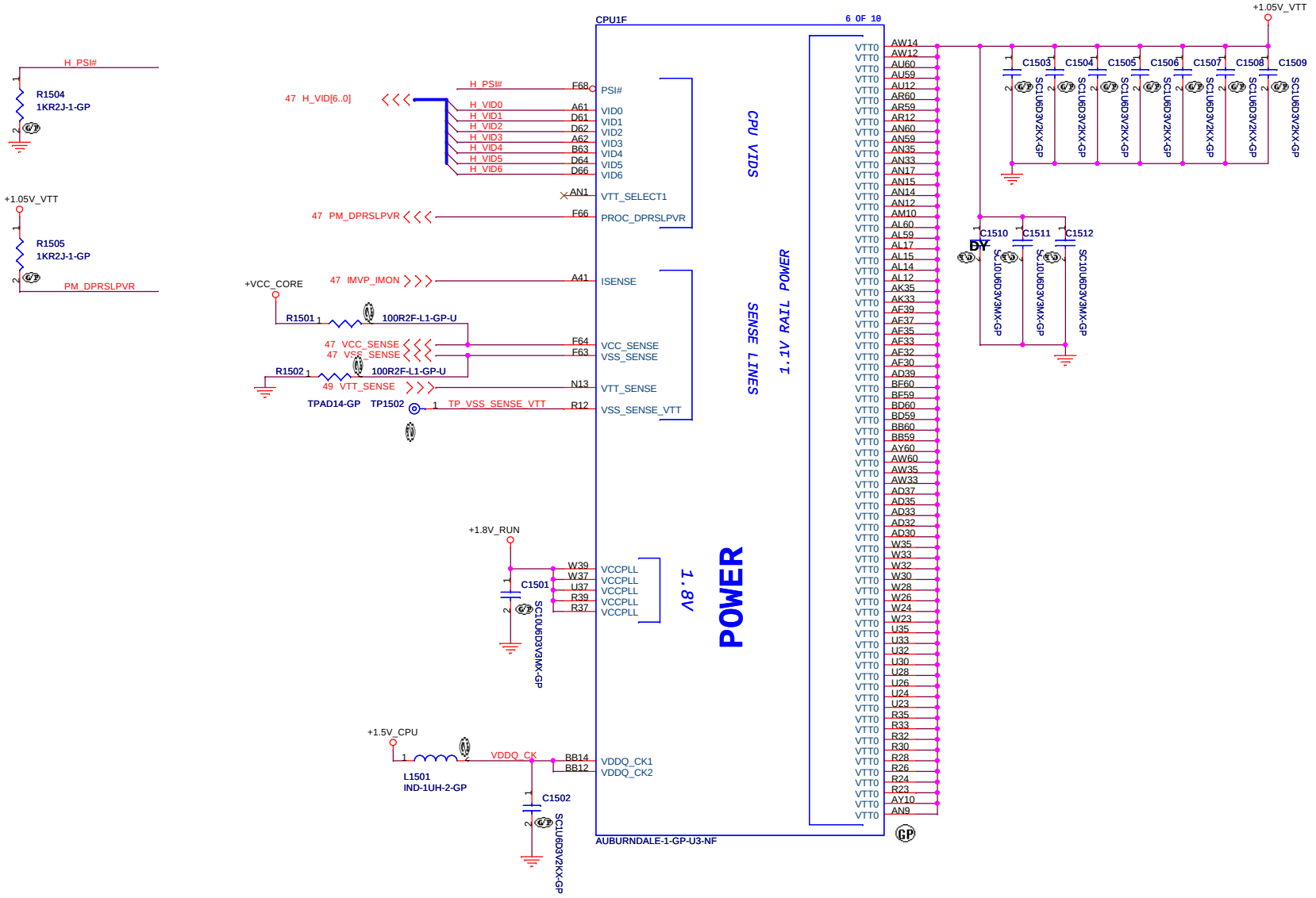
Title: CPU (RESERVED)-4/8

Size | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 11 of 92



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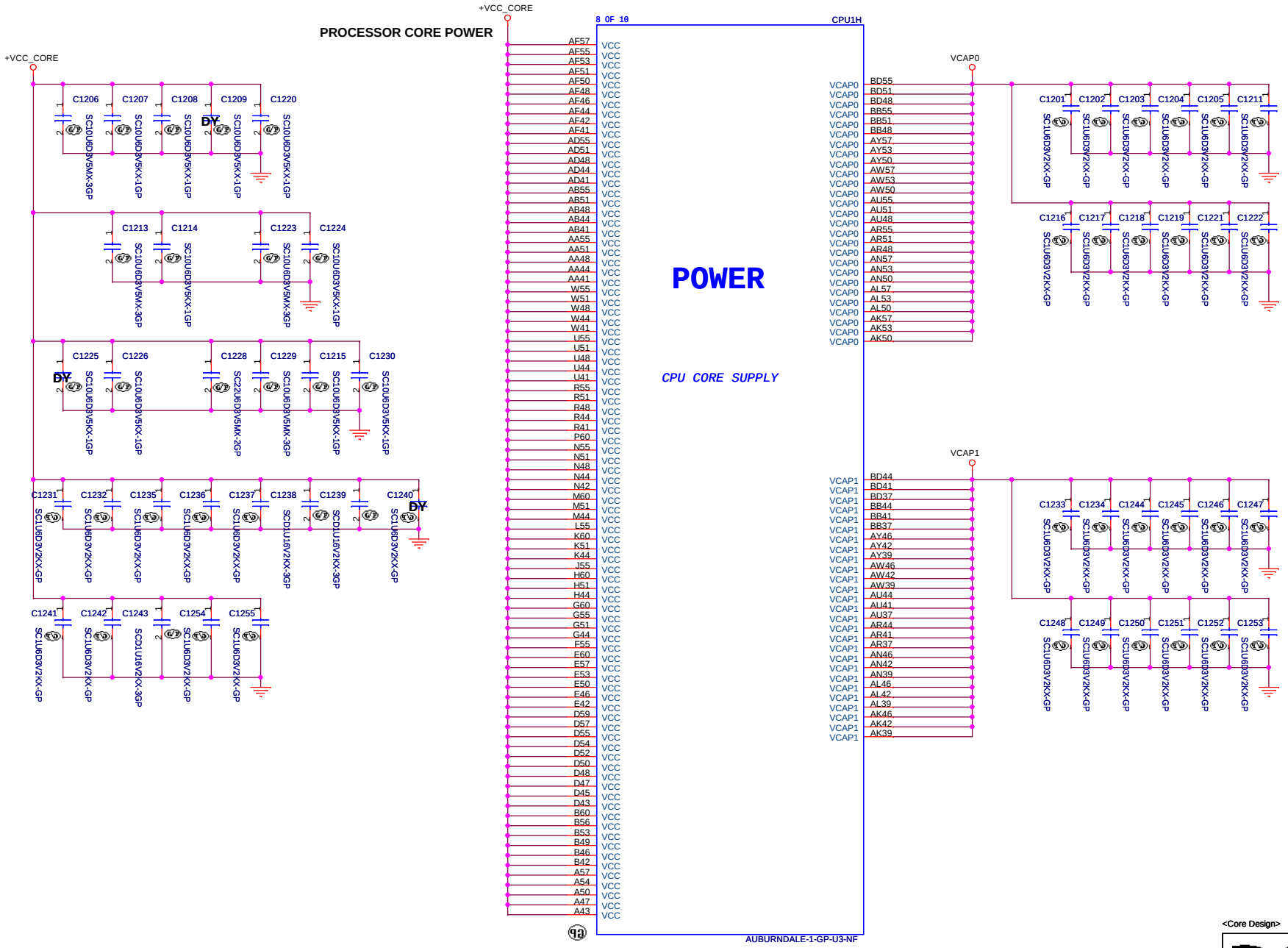
Title	CPU SFF PWR/VTT-5/8	
Size A3	Document Number RYU2 13 UMA	Rev A00
Date: Tuesday, September 28, 2010	Sheet 12 of 92	

SSID = CPU



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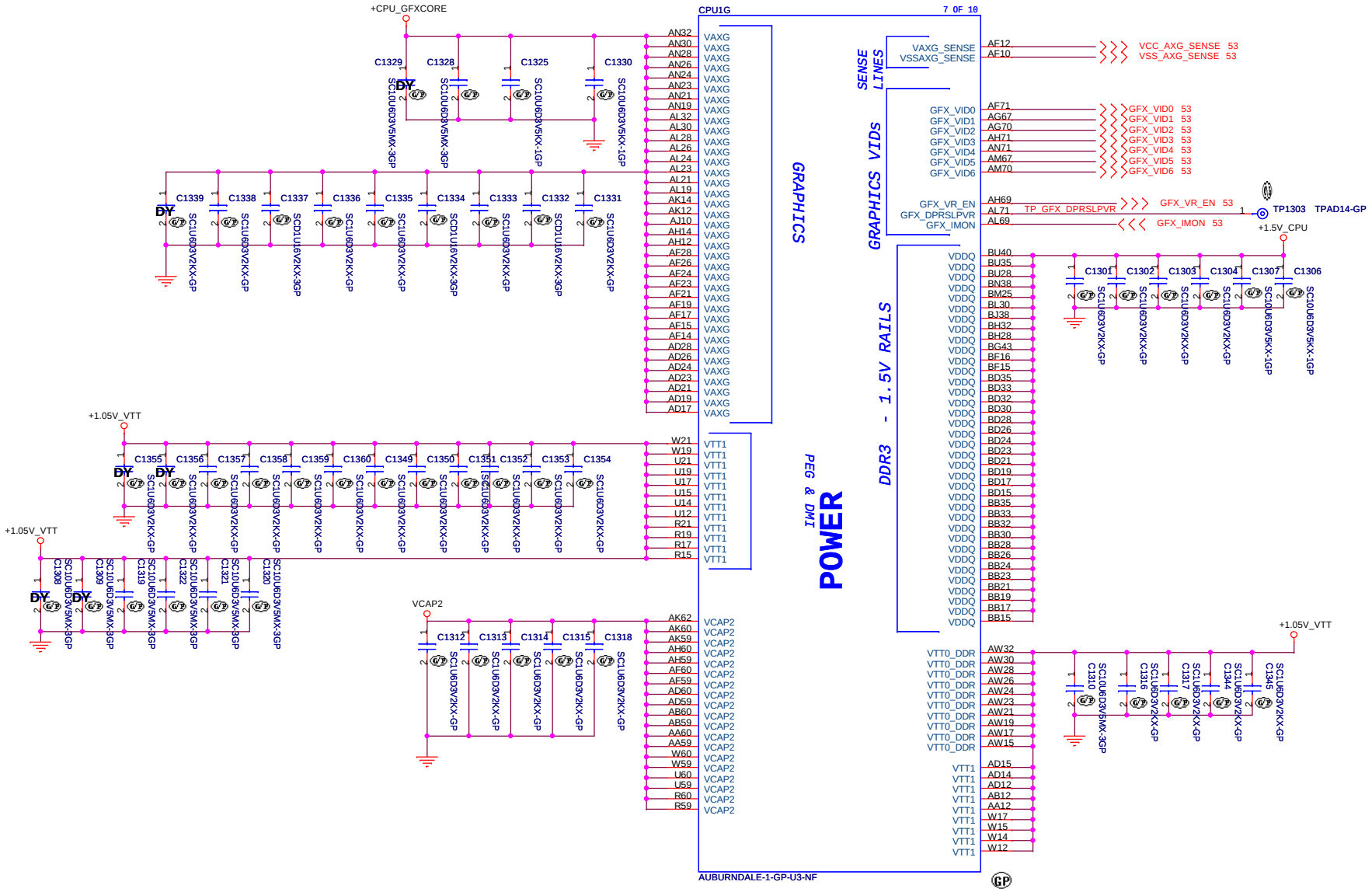
Title: CPU (VCC_CORE)-6/8

Size | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 13 of 92

SSID = CPU



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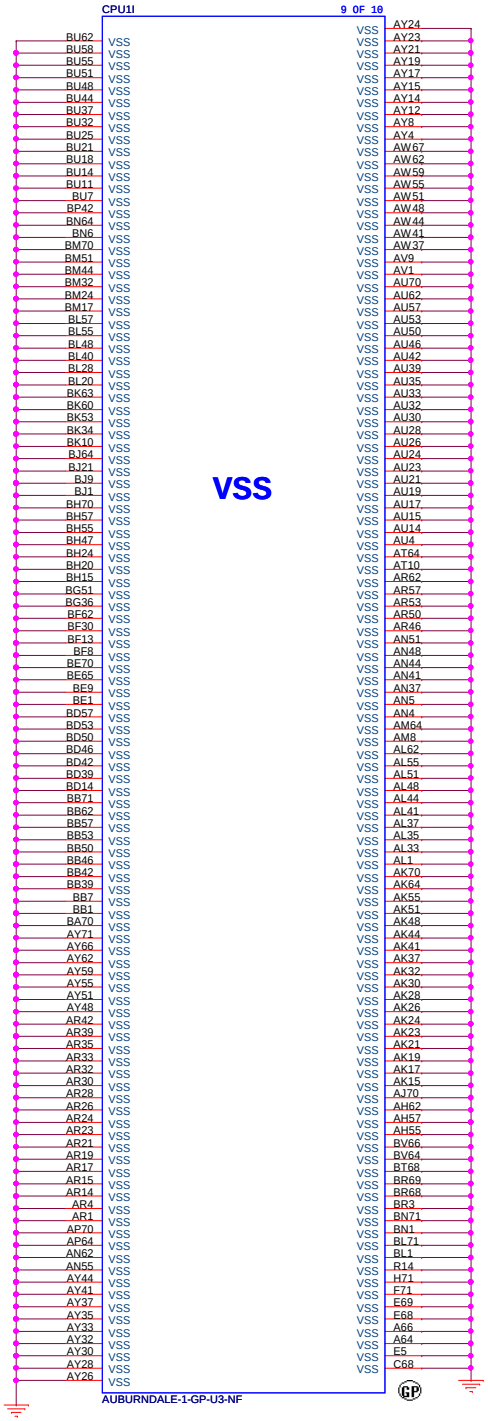
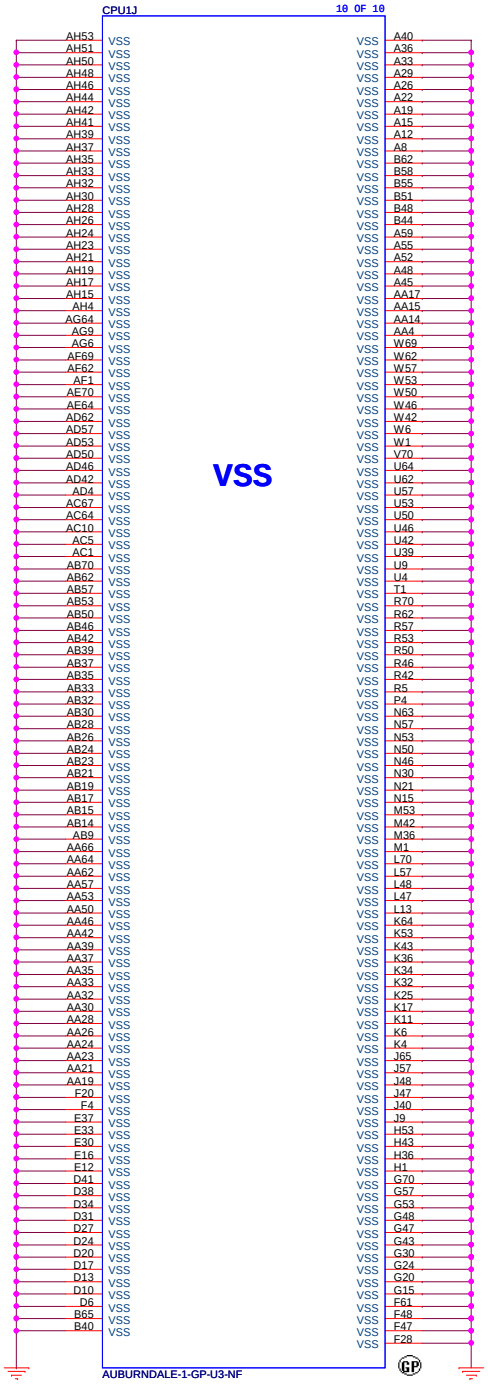
Title: CPU (VCC_GFXCORE)-7/8

Size | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 14 of 92





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Title: **CPU (VSS)-8/8**

Size	Document Number	Rev
	RYU2 13 UMA	A00

Date: Tuesday, September 28, 2010 Sheet 15 of 92

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Title	***(Reserved)***	
Size A4	Document Number ***RYU2 13 UMA***	Rev ***A00***
Date: Tuesday, September 28, 2010	Sheet 16 of 92	

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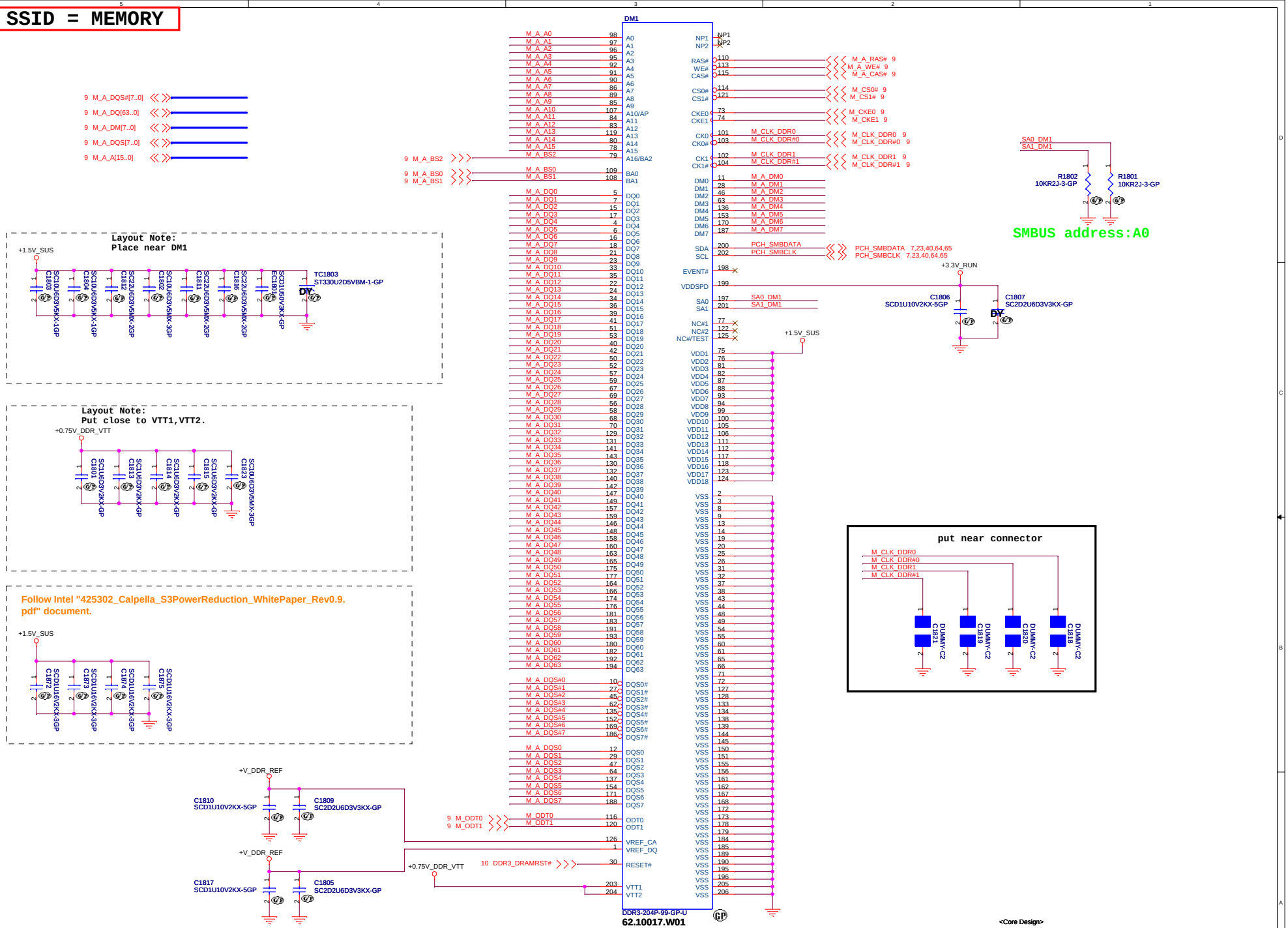
Title: *(Reserved)*

Size	Document Number	Rev
A4	*RYU2 13 UMA*	*A00*

Date: Tuesday, September 28, 2010 Sheet 17 of 92

SSID = MEMORY



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Title: DDRIII-SODIMM SLOT1

Size: Custom | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 18 of 92

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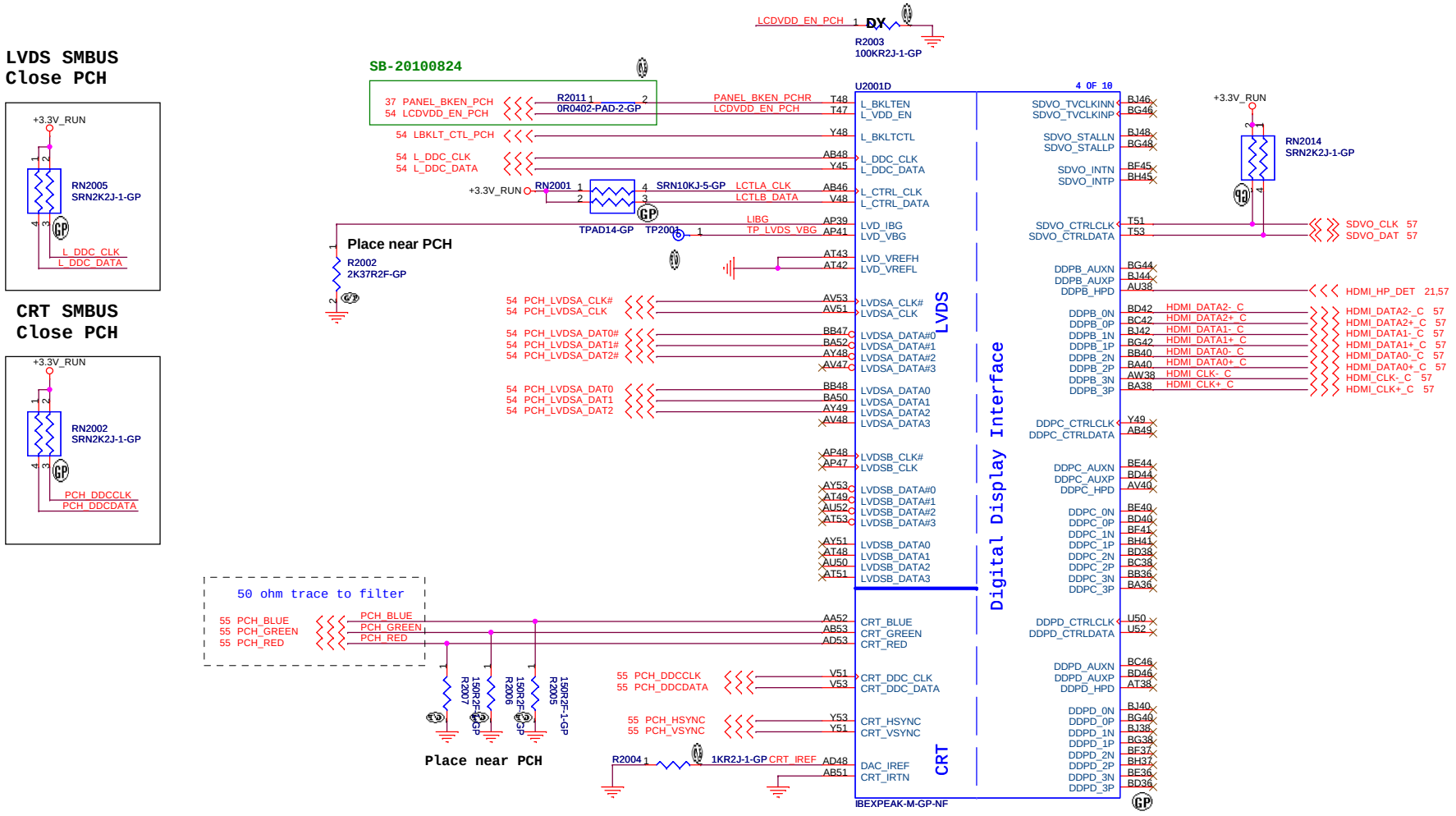
Title	***(Reserved)***	
Size A4	Document Number ***RYU2 13 UMA***	Rev ***A00***
Date: Tuesday, September 28, 2010	Sheet 19 of 92	

SSID = PCH



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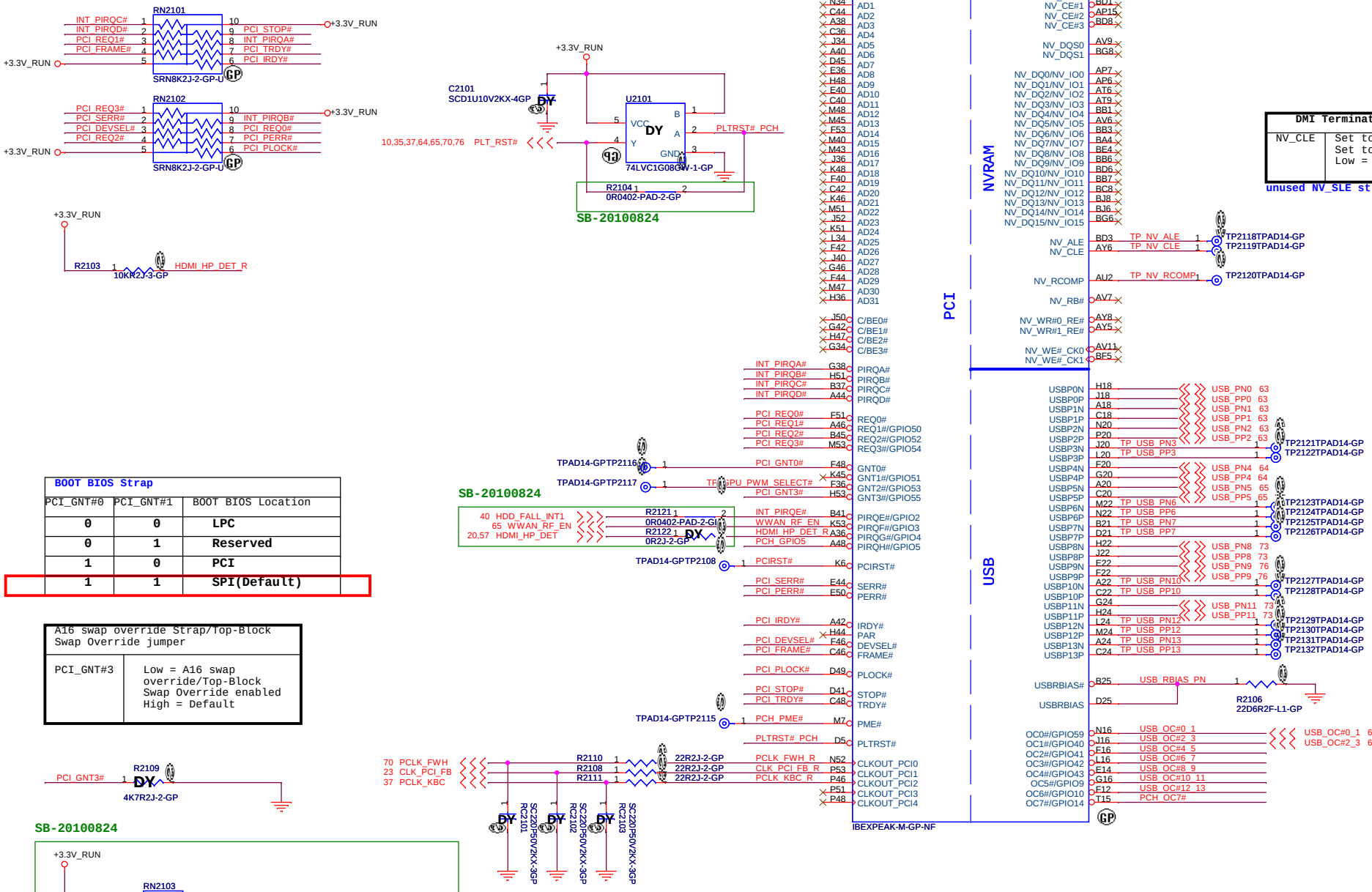
Title: PCH (LVDS/CRT/DDI)

Size | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 20 of 92

SSID = PCH



DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high. Low = Default

unused NV_SLE strap

BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI(Default)

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

USB	
Pair	Device
0	USB1 debug port
1	USB2
2	USB for ESATA
3	RESERVE
4	WLAN
5	WWAN
6	RESERVED (Not available for HM55)
7	RESERVED (Not available for HM55)
8	BLUETOOTH
9	Card Reader
10	RESERVED
11	CAMERA
12	RESERVED
13	RESERVED

Table 111. Overcurrent Pin Example Configuration

These OC7# pins are not used for USB overcurrent protection and should be configured as GPIOs. The unused USB ports can be left as no connect.

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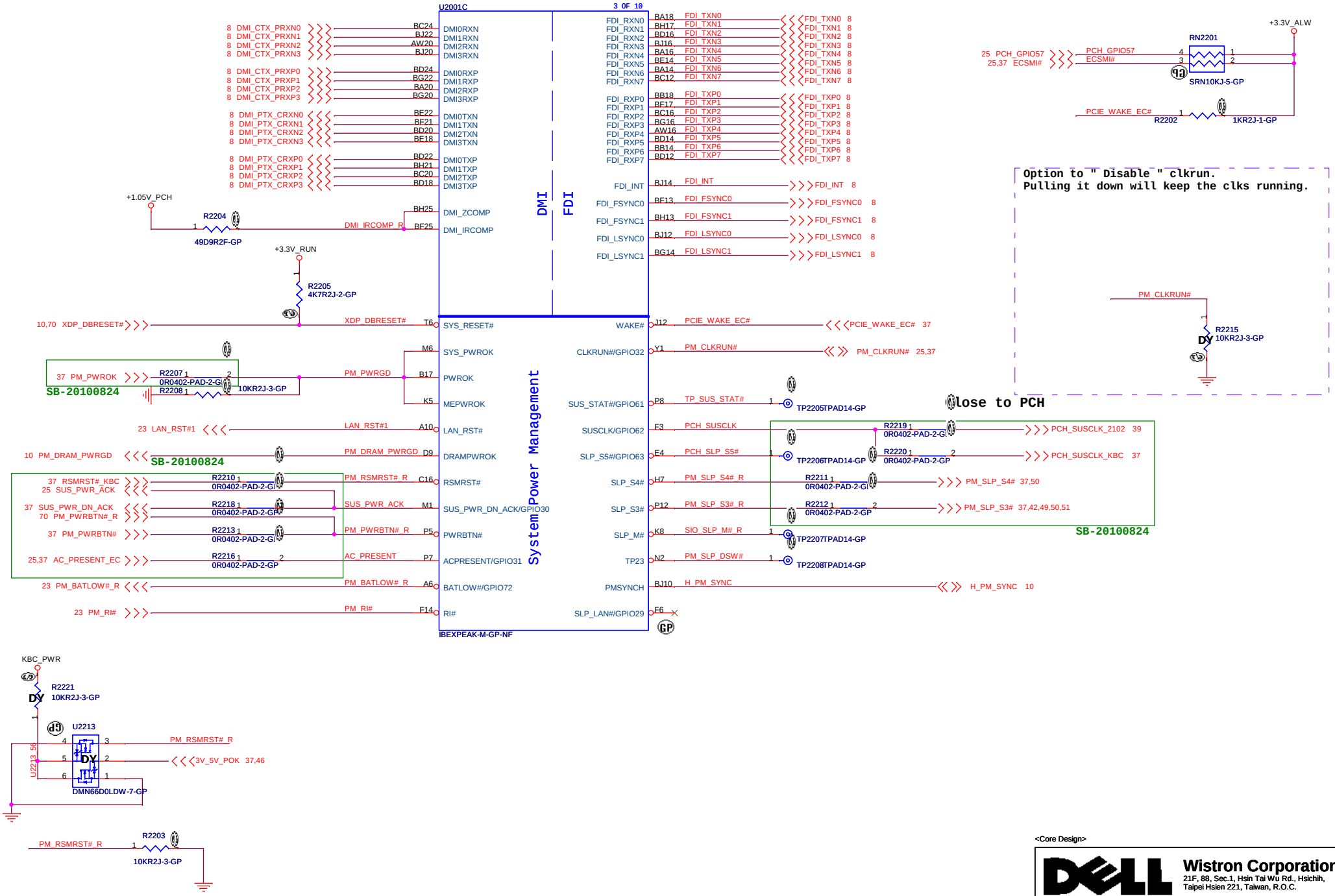
Title: PCH (PCI/USB/NVRAM)

Size: | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 21 of 92

SSID = PCH



<Core Design>

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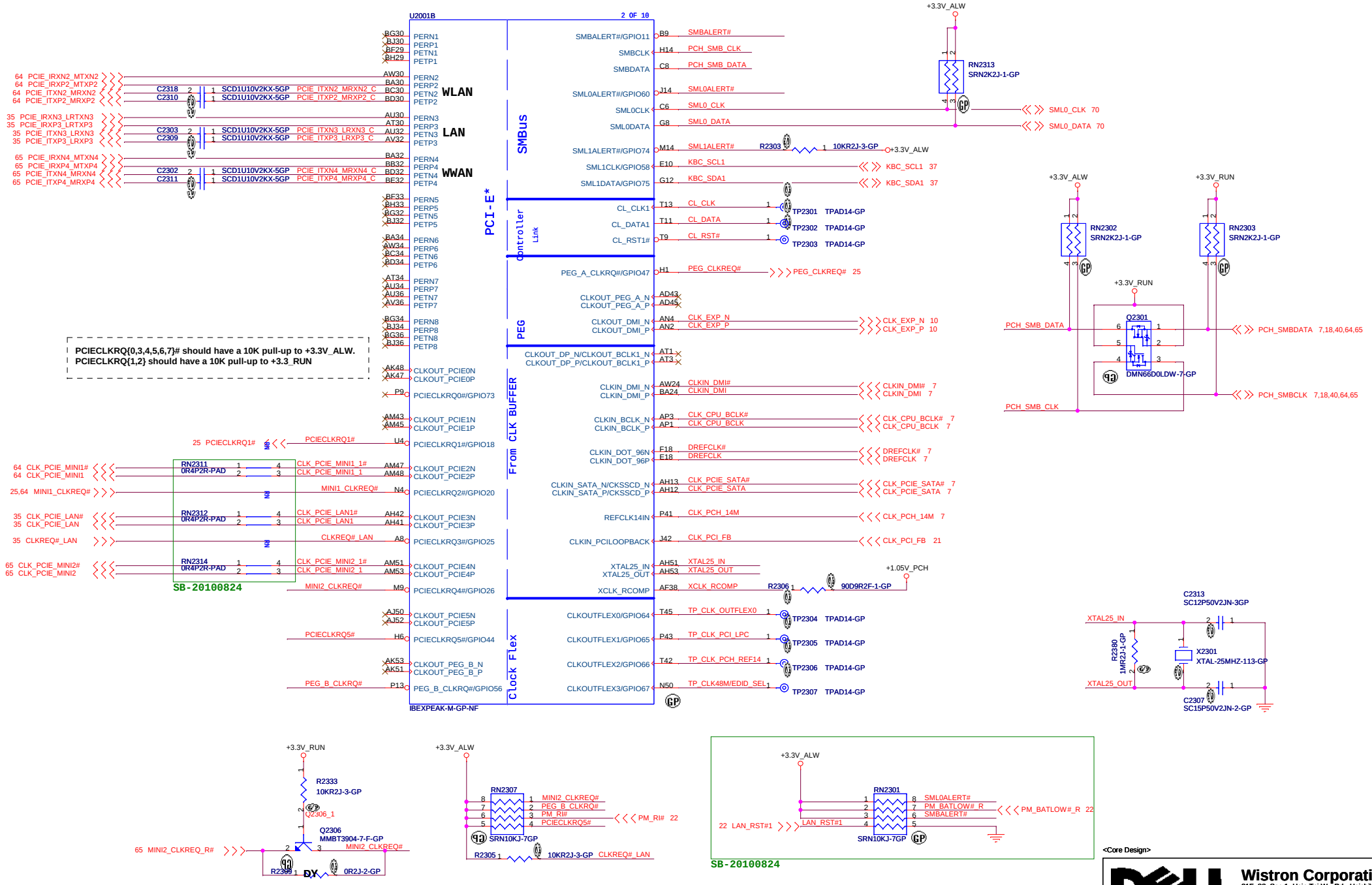
Title: PCH (DM I/FDI/PM)

Size | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 22 of 92

SSID = PCH



<Core Design>

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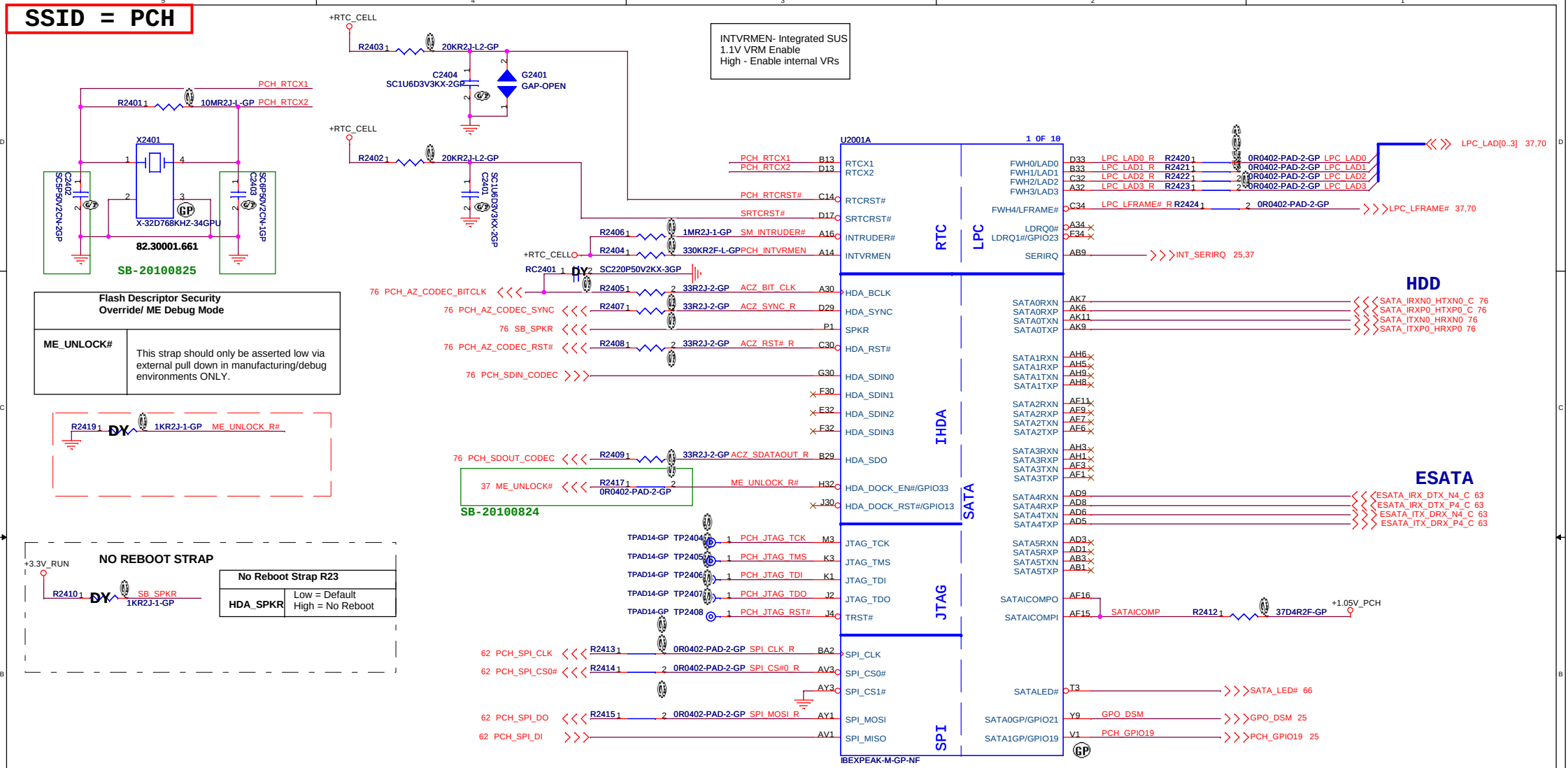
Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 23 of 92

SSID = PCH



<Core Design>

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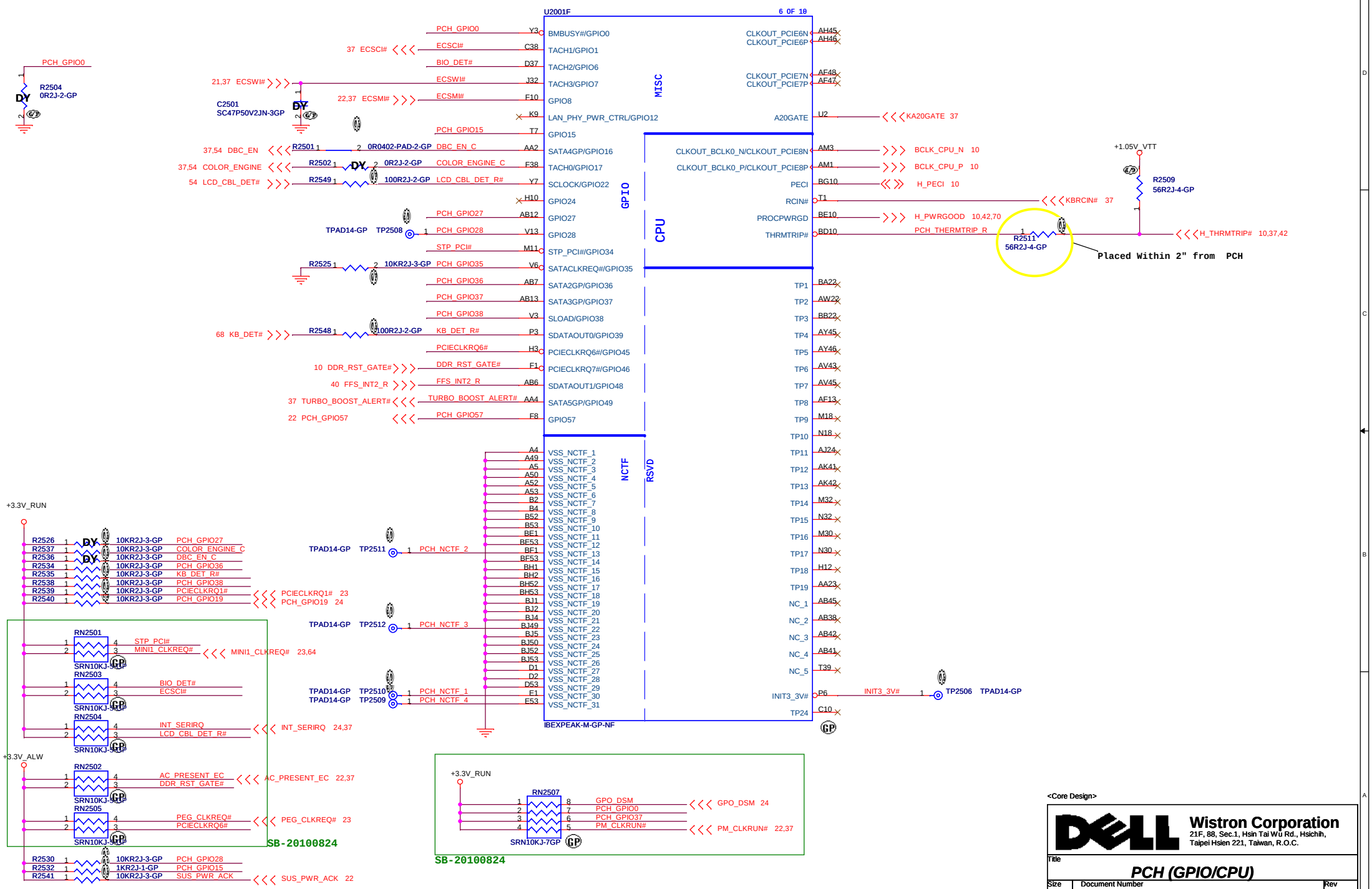
Title: **PCH (SPI/RTC/LPC/SATA/IHDA)**

Size | Document Number: **RYU2 13 UMA** | Rev: **A00**

Date: Tuesday, September 28, 2010 | Sheet 24 of 92

SSID = PCH



<Core Design>

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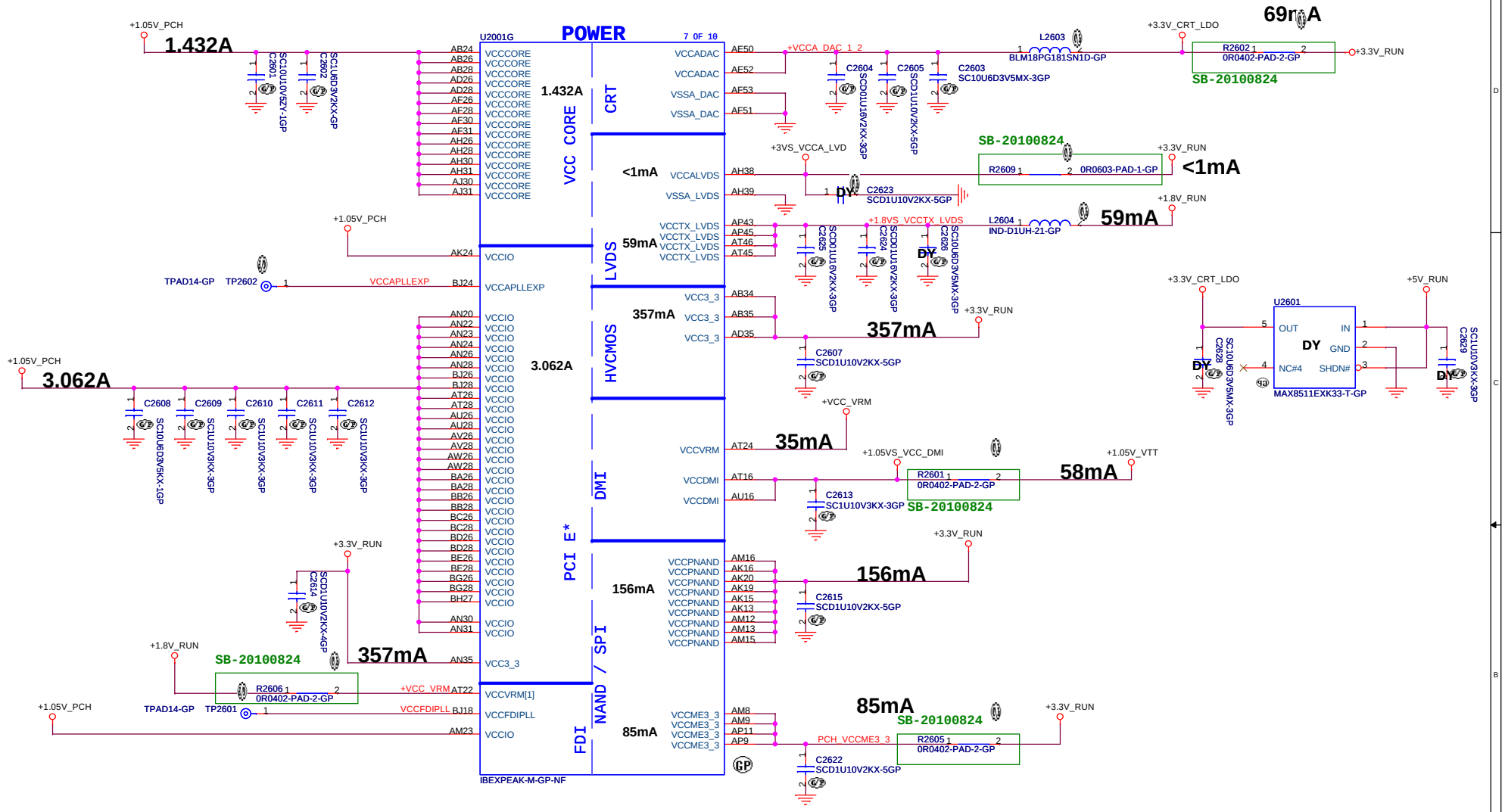
Title: PCH (GPIO/CPU)

Size | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 25 of 92

SSID = PCH



<Core Design>

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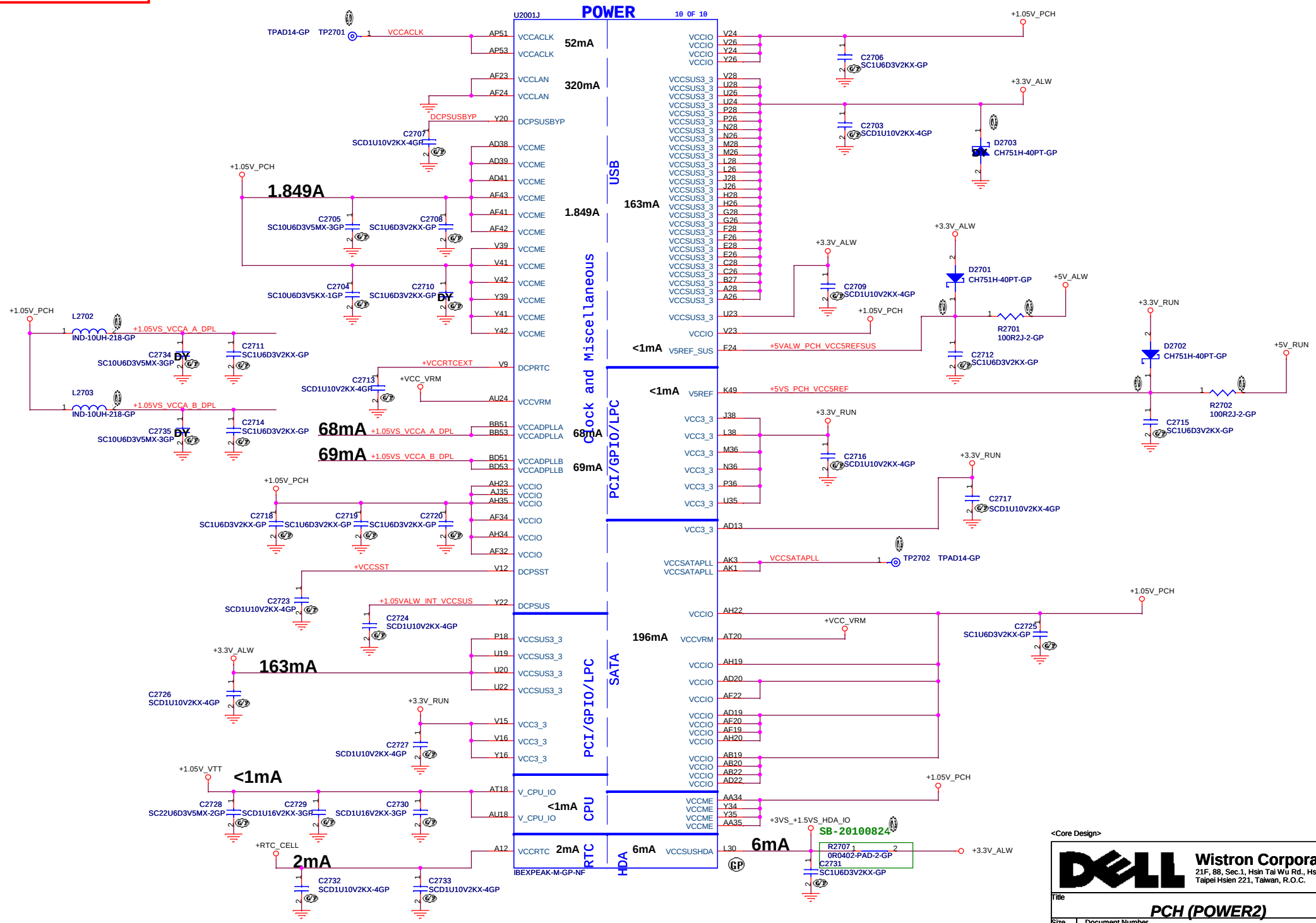
Title: **PCH (POWER1)**

Size	Document Number	Rev
	RYU2 13 UMA	A00

Date: Tuesday, September 28, 2010 Sheet 26 of 92

SSID = PCH



<Core Design>

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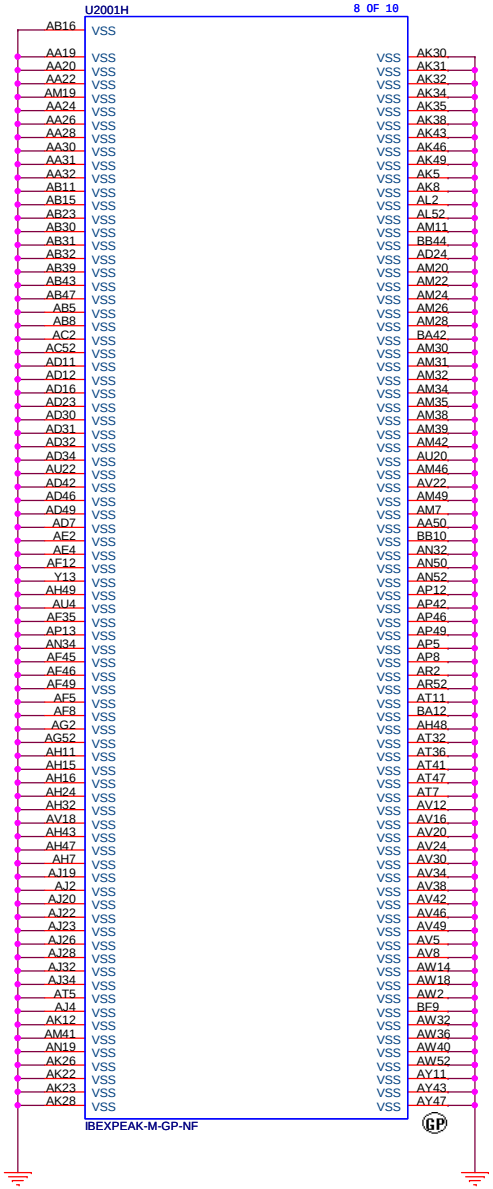
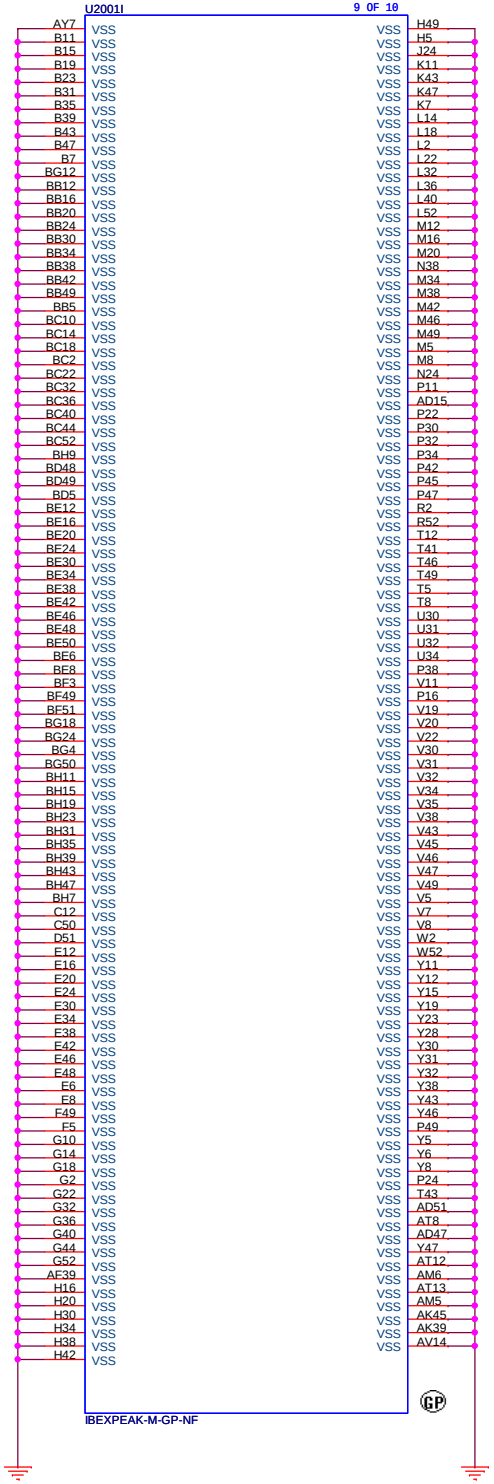
Title: PCH (POWER2)

Size | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 27 of 92

SSID = PCH





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Title		
	PCH (VSS)	
Size	Document Number	Rev
	RYU2 13 UMA	***A00***

Date: Tuesday, September 28, 2010 Sheet 28 of 92

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Title

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Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 Sheet 29 of 92

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Size A4	Document Number ***RYU2 13 UMA***	Rev ***A00***
Date: Tuesday, September 28, 2010	Sheet 30 of 92	

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Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 Sheet 31 of 92

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Title: *(Reserved)*

Size	Document Number	Rev
A4	*RYU2 13 UMA*	*A00*

Date: Tuesday, September 28, 2010 | Sheet 32 of 92

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Size	Document Number	Rev
A4	*RYU2 13 UMA*	*A00*

Date: Tuesday, September 28, 2010 | Sheet 33 of 92

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Title

(Reserved)

Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 Sheet 34 of 92

SSID = LOM

Placed withing 200mils of the REGOUT

REGOUT 60 mils — L3501 IND-4D7UH-233-GP — +1.05V_LOM — C3501 SC22U6D3V5MX-2GP, C3502 SCD1U10V2KX-5GP

Keep Caps withing 200mils of L3501

60 mils — R3509 0R0603-PAD-1-GP — SB-20100824

Close to U3501 pin21 — EVDD10 — C3503 SC1U6D3V2KX-GP, C3504 SCD1U10V2KX-5GP

R3512 0R0603-PAD-1-GP — SB-20100824

Close to U3501 pin3, 6, 9, 13, 29, 41, 45 — VDD10 — C3505, C3507, C3506, C3508, C3509, C3526, C3527 SCD1U10V2KX-5GP

+3.3V_ALW — 40 mils — C3521 SCD1U10V2KX-5GP — R3515 10KR2J-3-GP — PM_LAN_ENABLE_R — Q3501 2N7002A-7-GP — 37 PM_LAN_ENABLE

R3513 100KR2J-1-GP — LAN_EN_G — C3520 SC1U6D3V2KX-GP

R3516 0R3J-0-U-GP — Q3502 AO3403-GP — +3.3V_LAN — C3522 SCD1U10V2KX-5GP, C3523 SC10U6D3V5MX-3GP

+3.3V_LAN — R3502 10KR2J-3-GP — CLKREQ#_P1 — Q3506 MMBT3904-7-F-GP — 23 CLKREQ#_LAN — CLKREQ#_LAN_R — R3539 0R2J-2-GP

+3.3V_LAN — R3501 10KR2J-3-GP

AVDD33_REG — R3508 0R0402-PAD-2-GP — SB-20100824 — +3.3V_LAN — C3528 SCD1U10V2KX-4GP, C3515 SC4D7U6D3V3KX-GP — C3529, C3530, C3531, C3532, C3533, C3534 SCD1U10V2KX-4GP

Close to U3501 pin34, 35

Stuff R3514 if switching regulator is enabled.
Stuff R3511 if external power 1.2V is used.

SB-20100824 — ENSWREG — R3514 0R0402-PAD-2-GP — +3.3V_LAN — R3511 0R2J-2-GP

+3.3V_LAN — VDD10 — AVDD33_REG

37 PCIE_WAKE_LAN# — PCIE_WAKE_LAN# — ISOLATE# R — PLT_RST_LAN# — ENSWREG — REGOUT — EECS — LED3/EEDO — LED2/EEDI — LED3/EEDO 61

10,21,37,64,65,70,76 PLT_RST# — PLT_RST# — R3505 — 0R0402-PAD-2-GP

U3501 RTL8111E-VB-GR-GP

PERST# ISOLATE# DVDD33 LANWAKE# DVDD10 EECS/SCL LED3/EEDO EEDI/SDA ENSWREG VDDREG REGOUT

+3.3V_RUN — R3504 1KR2J-1-GP — ISOLATE# R — R3503 15KR2J-1-GP

C3511 & C3510 must be near U3501

23 PCIE_IRXN3_LRTXN3 — C3511 SCD1U10V2KX-5GP — PCIE_RXN3
23 PCIE_IRXP3_LRTXP3 — C3510 SCD1U10V2KX-5GP — PCIE_RXP3
EVDD10
23 CLK_PCIE_LAN#
23 CLK_PCIE_LAN
23 PCIE_ITXN3_LRXN3
23 PCIE_ITXP3_LRXP3

R3536 10KR2J-3-GP — CLKREQ# LAN R — SMBDATA_LOM — VDD10

GND, HSON, HSOP, EVDD10, REFCLK_N, REFCLK_P, HSIN, HSIP, CLKREQ#, SMBDATA, SMBCLK, DVDD10

LED1/EESK — GPO/SMBALERT — DVDD33 — LED0 — DVDD10 — AVDD33 — CKXTAL1 — CKXTAL2 — AVDD10 — RSET — AVDD33 — AVDD33

LED1/EESK — GPO_LOM — R3510 1KR2J-1-GP — +3.3V_LAN — LED1/EESK 61 — LAN_TX/RX_L# 61 — VDD10 — LAN_X1 — LAN_X2 — RSET — R3525 2K49R2F-GP — +3.3V_LAN

AVDD33 MDIN3 MDIP3 AVDD10 MDIN2 MDIP2 AVDD10 MDIN1 MDIP1 AVDD10 MDIN0 MDIP0 GND

+3.3V_LAN

NB_LOM_TRD0 — NB_LOM_TRD0# — NB_LOM_TRD0 61 — NB_LOM_TRD0# 61
NB_LOM_TRD1 — NB_LOM_TRD1# — NB_LOM_TRD1 61 — NB_LOM_TRD1# 61
NB_LOM_TRD2 — NB_LOM_TRD2# — NB_LOM_TRD2 61 — NB_LOM_TRD2# 61
NB_LOM_TRD3 — NB_LOM_TRD3# — NB_LOM_TRD3 61 — NB_LOM_TRD3# 61
VDD10

C3513 SC15P50V2JN-2-GP — LAN_X1 — X3501 XTAL-25MHZ-113-GP — C3514 SC15P50V2JN-2-GP — LAN_X2

SB-20100824 — RN3501 SRN10KJ-5-GP — EECS — LED2/EEDI

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Title: (Reserved)

Size	Document Number	Rev
Custom	RYU2 13 UMA	A00

Date: Tuesday, September 28, 2010 Sheet 35 of 92

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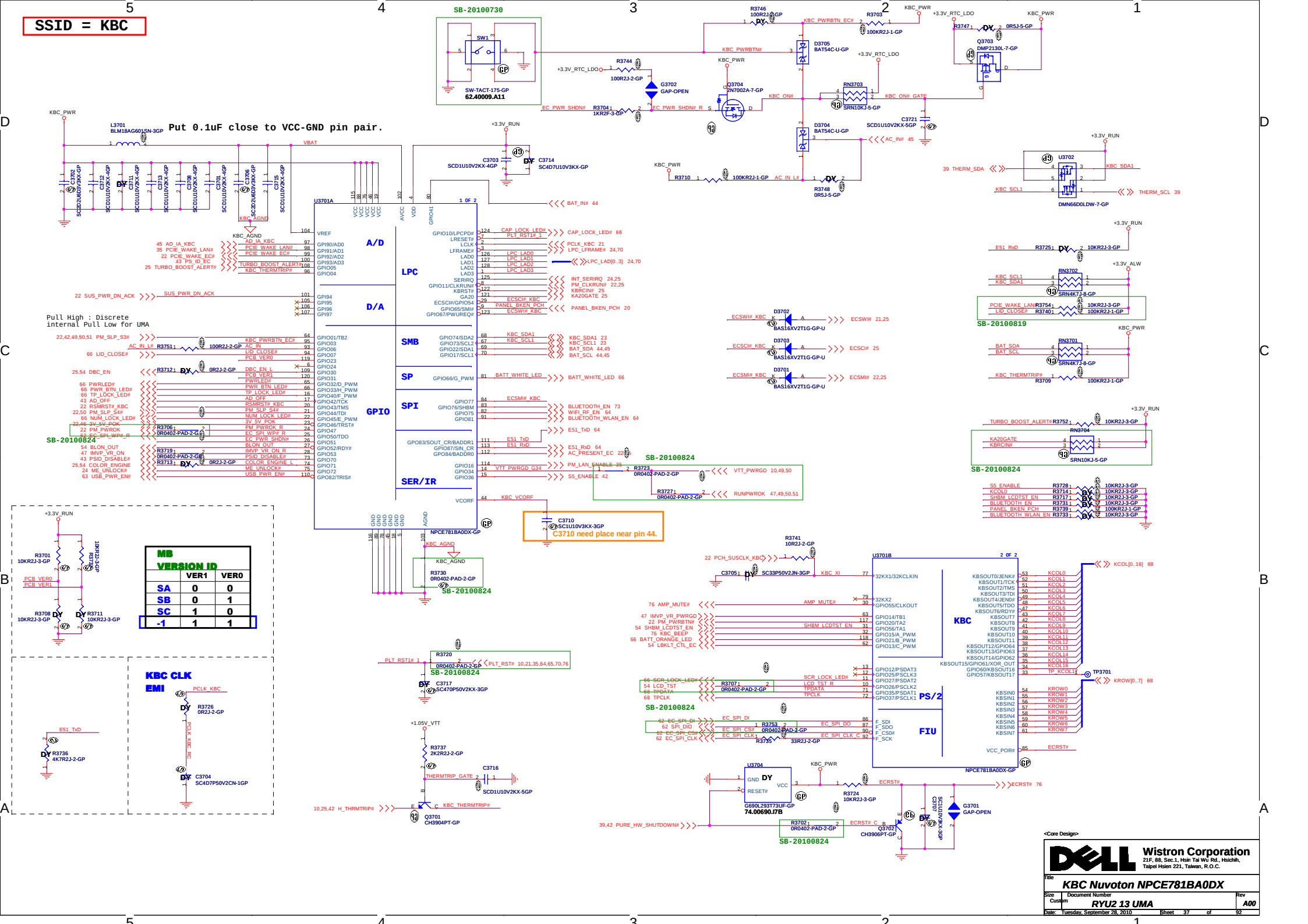
Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 | Sheet 36 of 92


SSID = KBC
Put 0.1uF close to VCC-GND pin pair.
U3701A
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
NPCE781BA0DX-GP
C3710 need place near pin 44.
SB-20100730
SW-TACT-175-GP
62.40009.A11
SB-20100824
SB-20100819
MB VERSION ID
VER1 VER0
SA 0 0
SB 0 1
SC 1 0
-1 1 1
KBC CLK EMI
U3701B
KBC
PS/2
FIU
NPCE781BA0DX-GP
U3702
DMN66D0LDW-7-GP
U3704
G690L293T73UF-GP
74.00690.I7B
Q3702
CH3906PT-GP
Q3701
CH3904PT-GP
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KBC Nuvoton NPCE781BA0DX
Size Custom
Document Number RYU2 13 UMA
Rev A00
Date: Tuesday, September 28, 2010
Sheet 37 of 92

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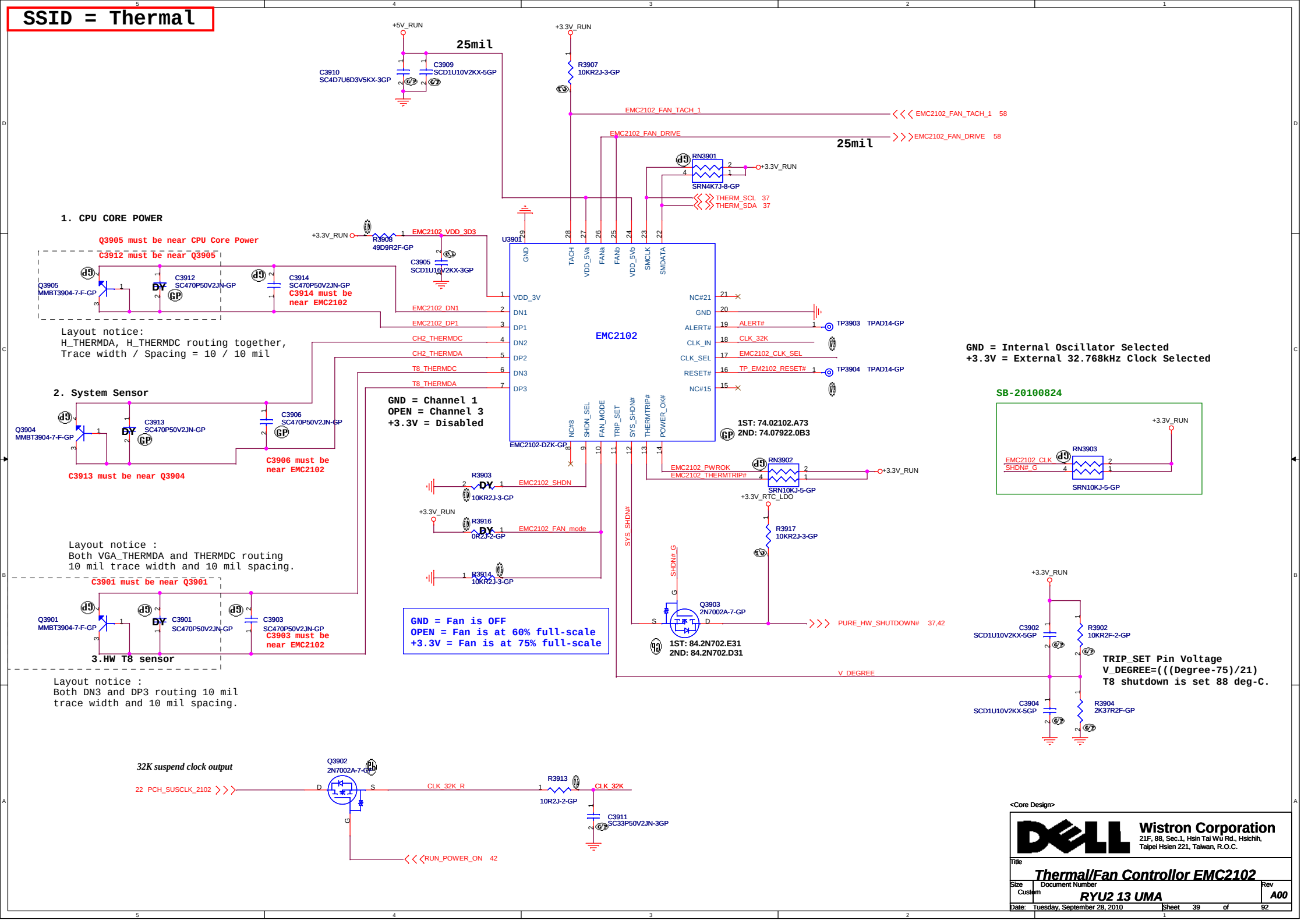
(Reserved)

Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 Sheet 38 of 92

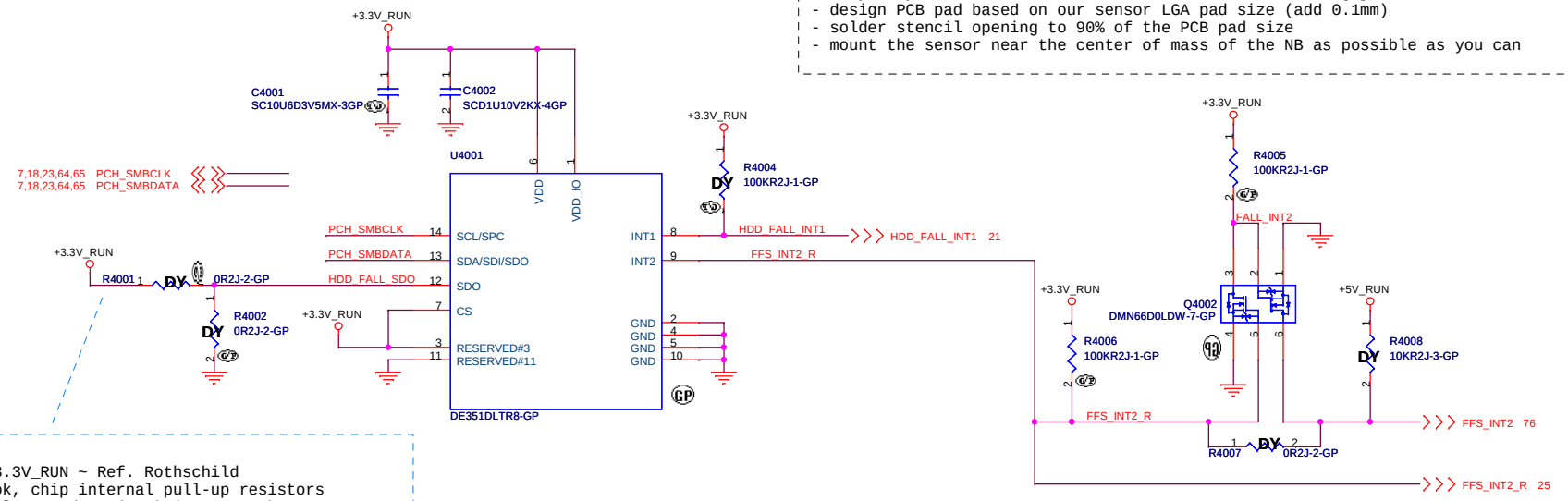
SSID = Thermal



SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



09/0422
(#1) Just pull +3.3V_RUN ~ Ref. Rothschild
(#2) FAE/ DY is ok, chip internal pull-up resistors
(#3) From spec, Slave ADdress(SAD) is 001110xb
Pull HIGH SAD is 0011101b
Pull GND SAD is 0011100b

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

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Title: Free Fall Sensor

Size: A3 | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 40 of 92

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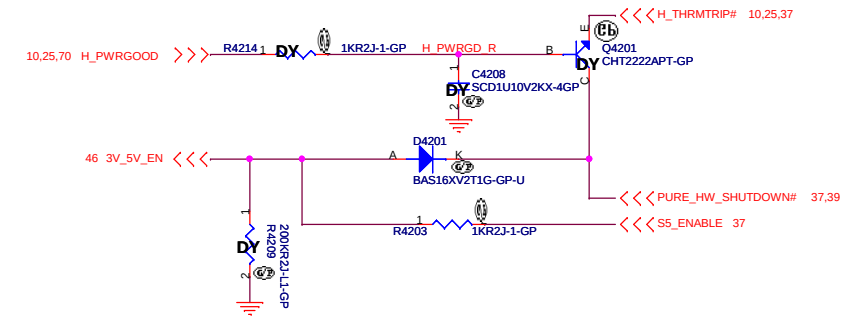
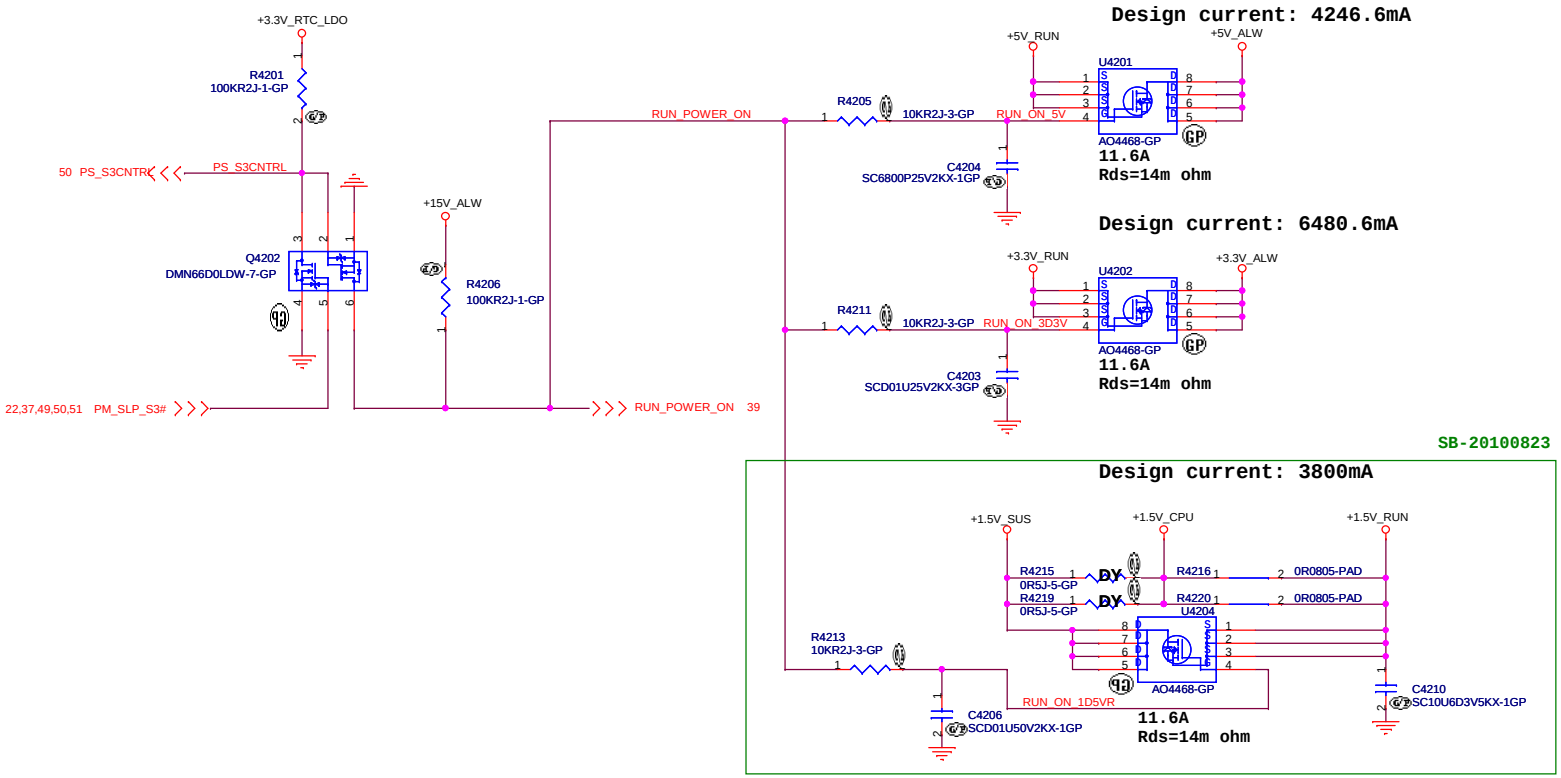
Title: *(Reserved)*

Size	Document Number	Rev
A4	*RYU2 13 UMA*	*A00*

Date: Tuesday, September 28, 2010 Sheet 41 of 92

SSID = Reset.Suspend





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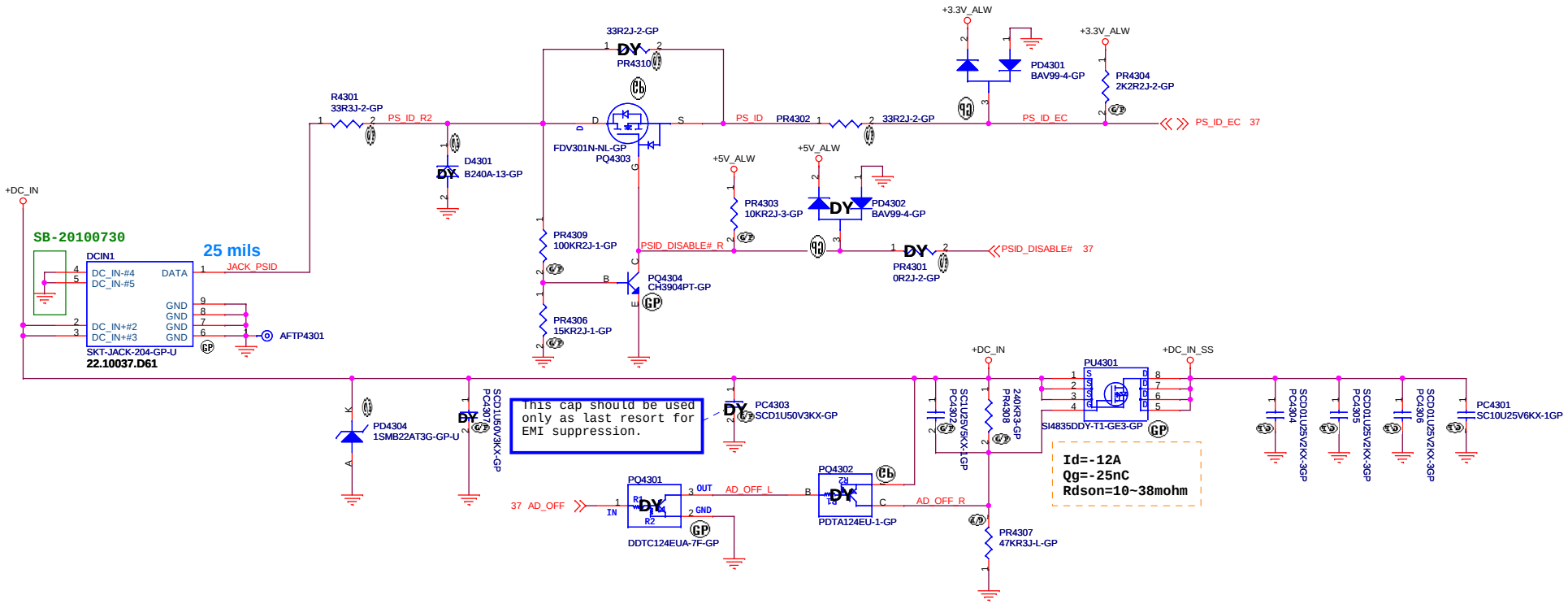
Title: ***Power Plane Enable***

Size	Document Number	Rev
Custom	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 Sheet 42 of 92

SSID = DCIN



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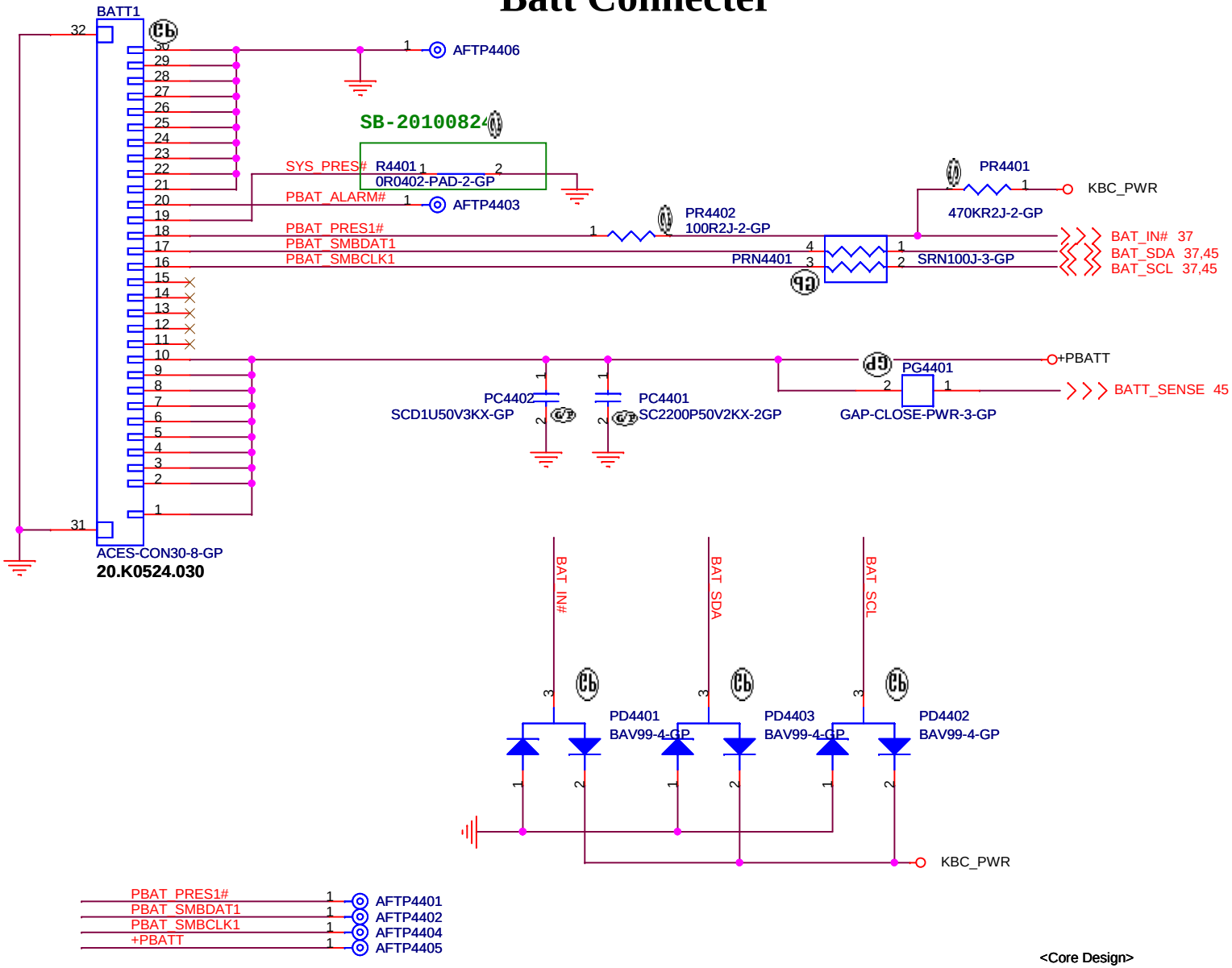
Title: DCIN

Size: Custom | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 43 of 92

SSID = BATT

Batt Connecter



PBAT_PRES1# — AFTP4401
PBAT_SMBDAT1 — AFTP4402
PBAT_SMBCLK1 — AFTP4404
+PBATT — AFTP4405

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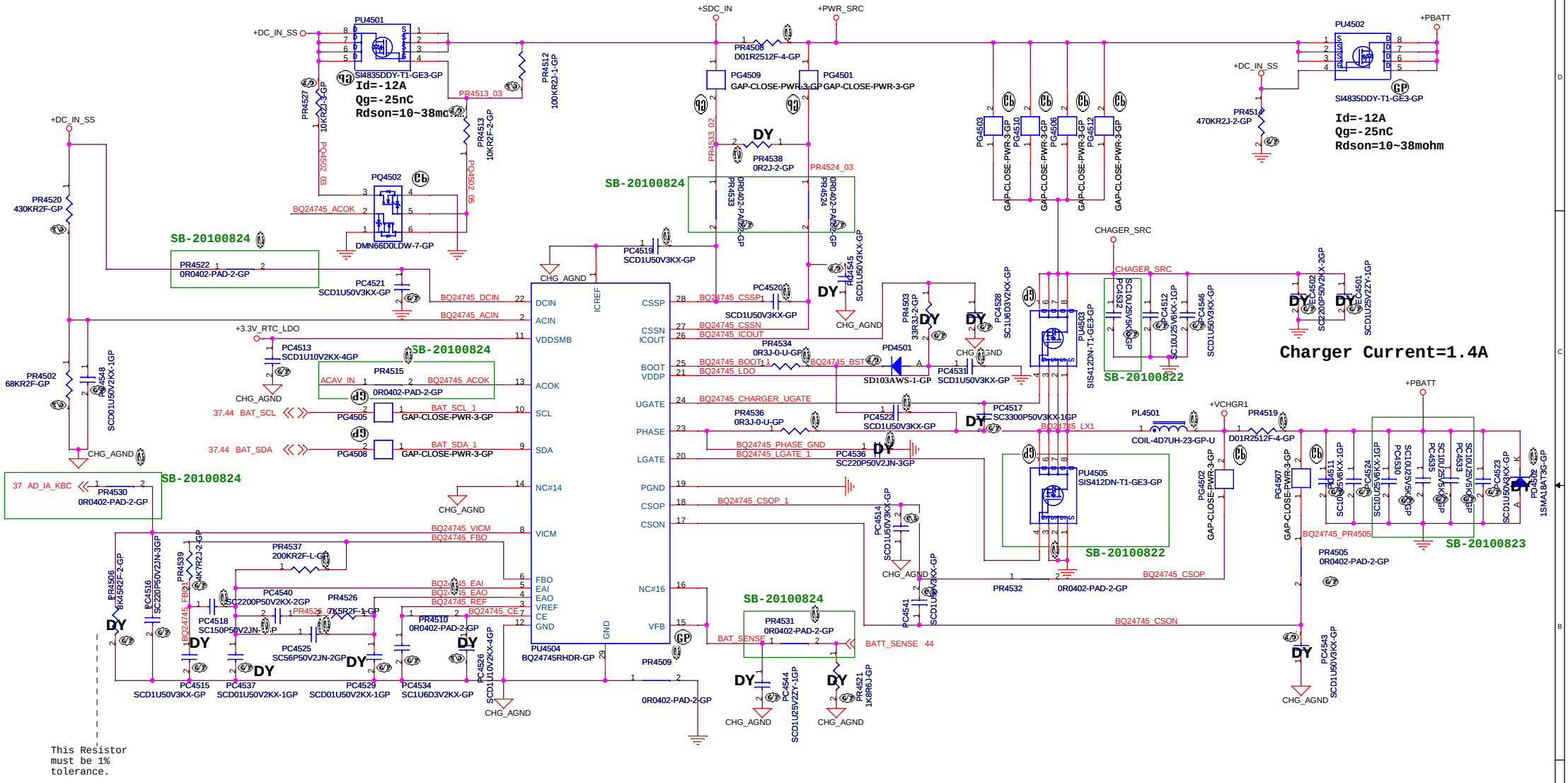
Title: ***Batt Connecter***

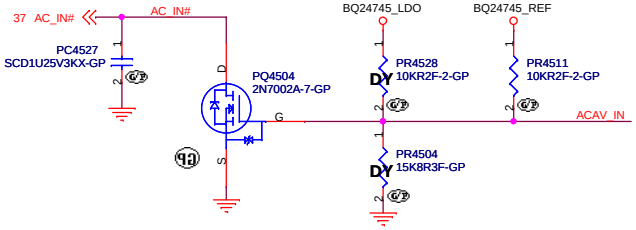
Size	Document Number	Rev
A4	RYU2 13 UMA	A00

Date: Tuesday, September 28, 2010 Sheet 44 of 92

SSID = Charger



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH PCMB061H-2R2MS Cyntec 70mohm Idc =3.5Arms 68.4R710.20W
O/P cap: 10U 25V K1206 X5R/ 78.10622.52L
H/S: SiS412DN 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: Si7716ADN 13.5mOhm/16.5mOhm@4.5Vgs/ 84.06690.E37



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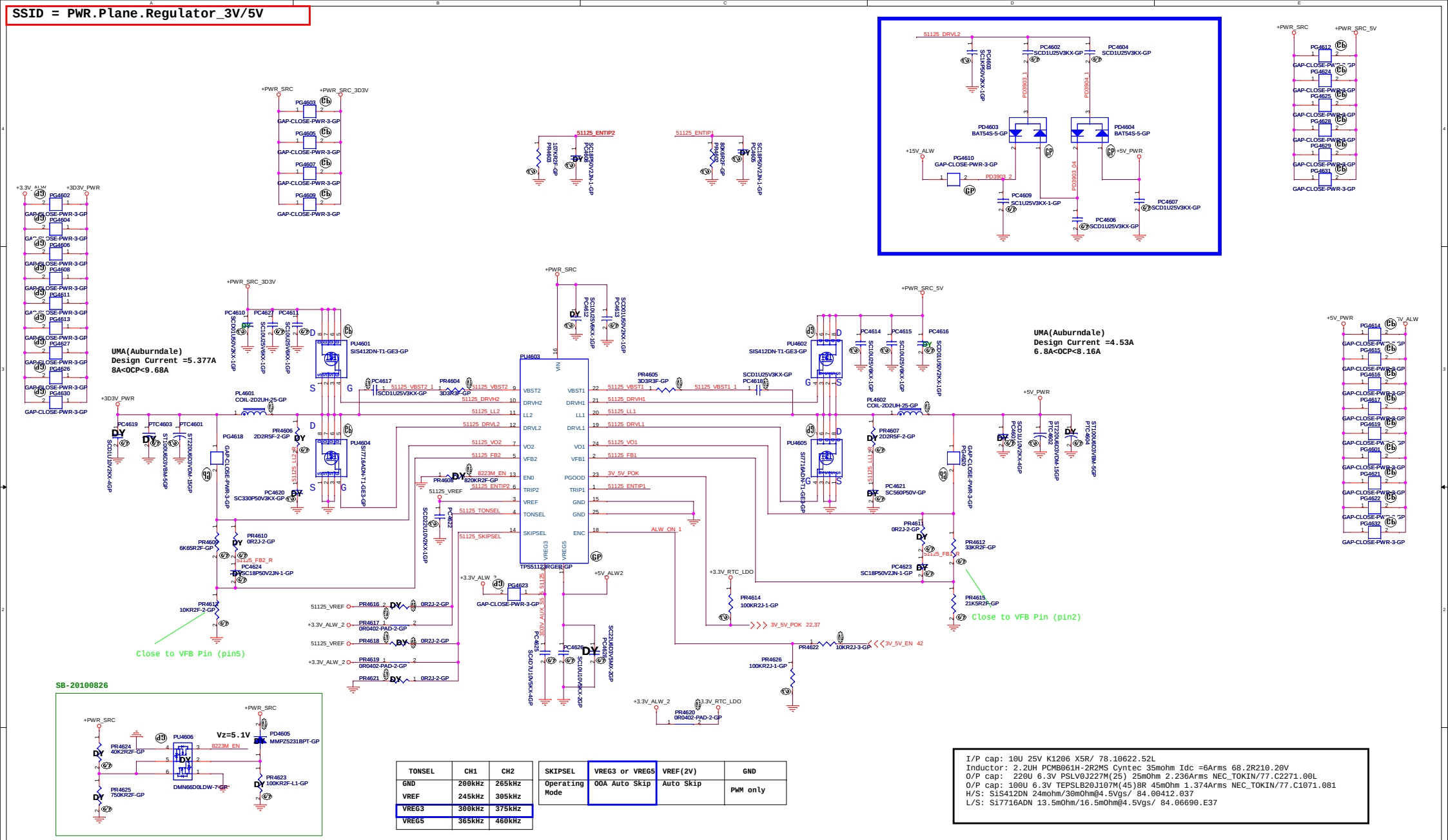
Title: CHARGER BQ24745

Size: Custom | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 45 of 92

SSID = PWR.Plane.Regulator_3V/5V



TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH PCMB061H-2R2MS Cyntec 35mohm Idc =6Arms 68.2R210.20V
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: SiS412DN 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: Si7716ADN 13.5mOhm/16.5mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH PCMB061H-2R2MS Cyntec 35mohm Idc =6Arms 68.2R210.20V
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: SiS412DN 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: Si7716ADN 13.5mOhm/16.5mOhm@4.5Vgs/ 84.06690.E37

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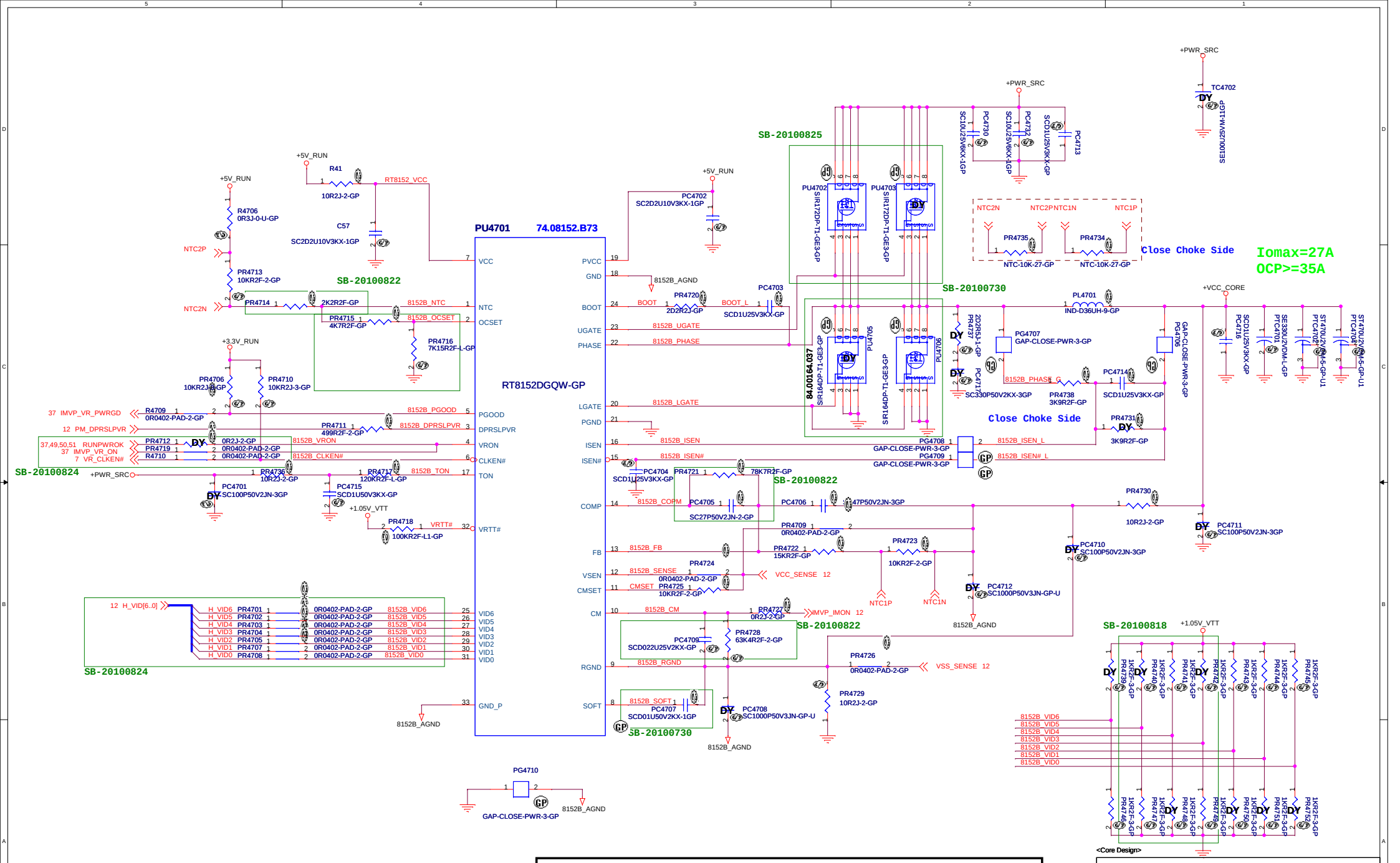
Title: TPS51123RGER_5V/3D3V

Size: Custom | Document Number: Winery13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 46 of 92



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: CHOKE 0.36UH PCMC104T-R36 Cyntec 1.05mohm Idc =30Arms 68.R3610.20C
O/P cap: EEFLX0D331R EL 330U 2V M 7.3*4.3 6mOhm 3.5Arms PANASONIC 79.33719.2EL
O/P cap: EL330U2V EEFSX0D331ER 9mOhm 3 Arms PANASONIC/79.33719.L01
H/S: SI7686DP 10mohm/14mOhm@4.5Vgs/ 84.07686.A37
L/S: SIR164DP 2.6mOhm/3.2mOhm@4.5Vgs/ 84.00164.037

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Title: RT8152_CPU_CORE

Size: Custom | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 47 of 92

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<Core Design>

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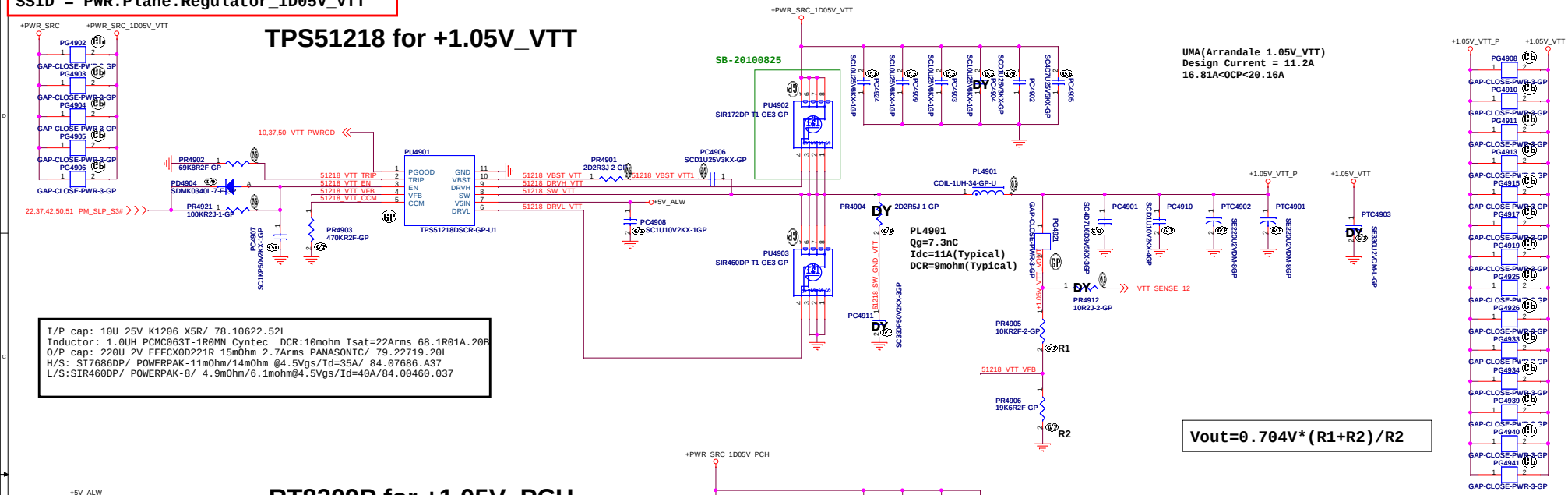
Title	***(Reserved)***	
Size A4	Document Number ***RYU2 13 UMA***	Rev ***A00***
Date: Tuesday, September 28, 2010	Sheet 48 of 92	

SSID = PWR.Plane.Regulator_1D05V_VTT

TPS51218 for +1.05V_VTT



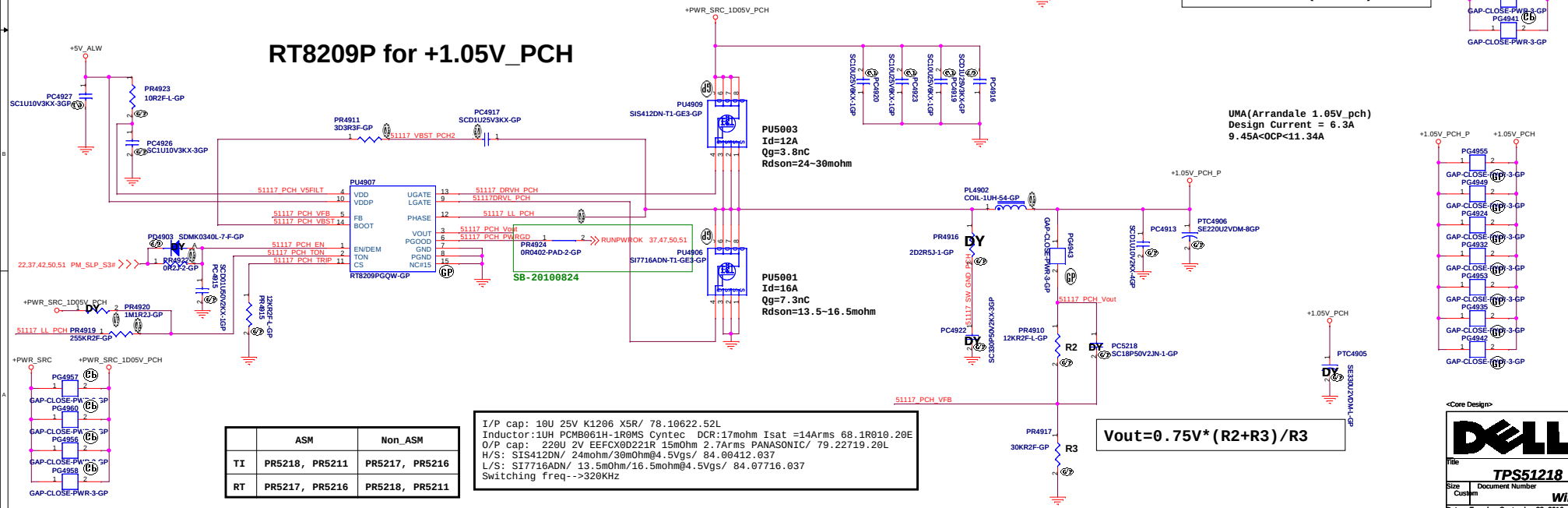
UMA(Arrandale 1.05V_VTT)
Design Current = 11.2A
16.81A<OCP<20.16A

PL4901
Qg=7.3nC
Idc=11A(Typical)
DCR=9mohm(Typical)

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.0UH PCMC063T-1R0MN Cyntec DCR:10mohm Isat=22Arms 68.1R01A.20B
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-11mOhm/14mOhm @4.5Vgs/Id=35A/ 84.07686.A37
L/S:SIR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/Id=40A/84.00460.037

Vout=0.704V*(R1+R2)/R2

RT8209P for +1.05V_PCH



PU5003
Id=12A
Qg=3.8nC
Rdson=24~30mohm

PU5001
Id=16A
Qg=7.3nC
Rdson=13.5~16.5mohm

UMA(Arrandale 1.05V_pch)
Design Current = 6.3A
9.45A<OCP<11.34A

Vout=0.75V*(R2+R3)/R3

	ASM	Non_ASM
TI	PR5218, PR5211	PR5217, PR5216
RT	PR5217, PR5216	PR5218, PR5211

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor:1UH PCMB061H-1R0MS Cyntec DCR:17mohm Isat =14Arms 68.1R010.20E
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SI7716ADN/ 13.5mOhm/16.5mohm@4.5Vgs/ 84.07716.037
Switching freq-->320KHz

<Core Design>

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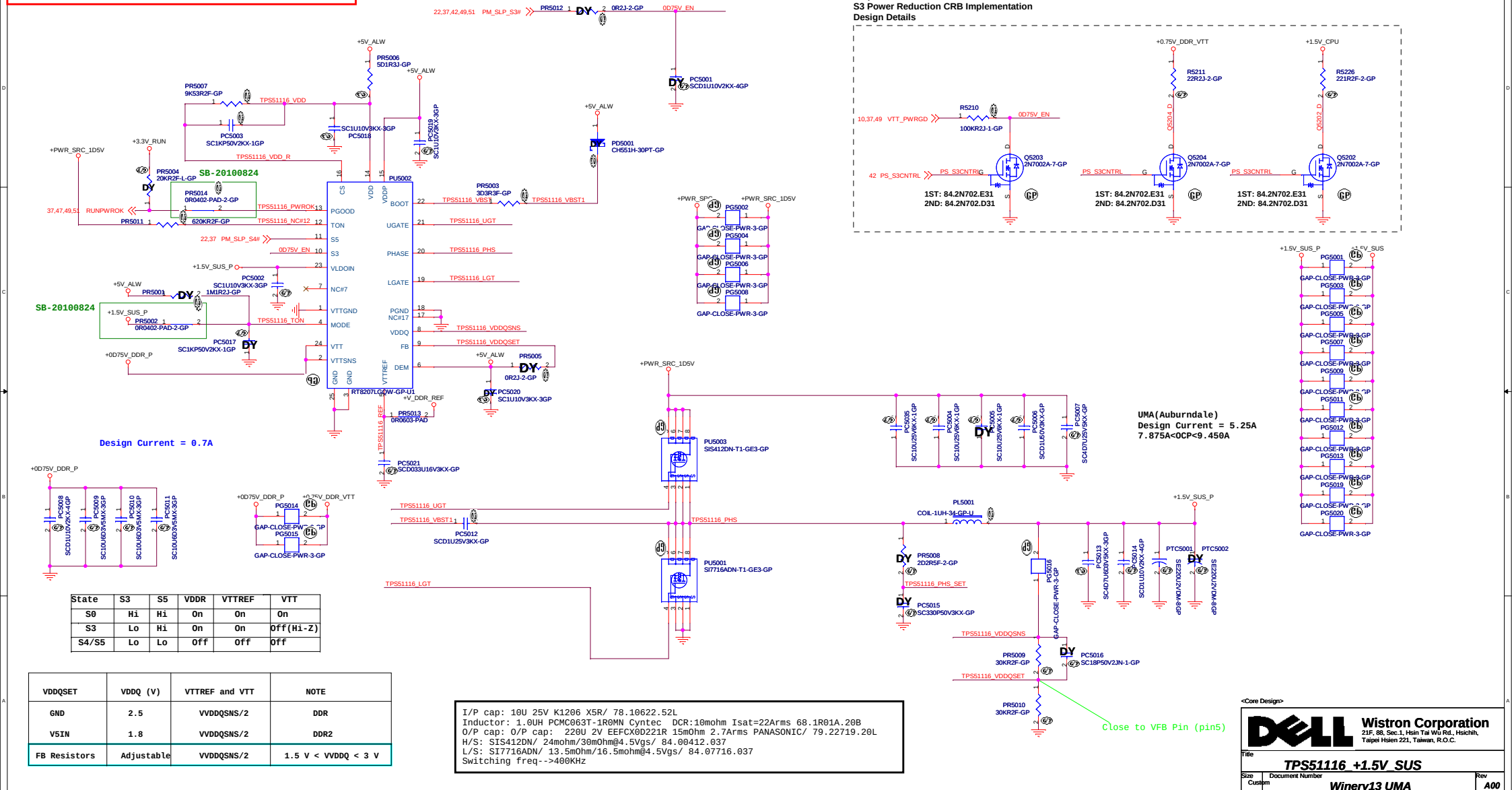
Title: TPS51218 +1.05V VTT
Size: Custom | Document Number: Winery13 UMA | Rev: A00
Date: Tuesday, September 28, 2010 | Sheet 49 of 92

SSID = PWR.Plane.Regulator_1p5v0p75v

Calpella Platform S3 Power Reduction Platform
S3 Power Reduction CRB Implementation
Design Details



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.0UH PCMC063T-1R0MN Cyntec DCR:10mohm Isat=22Arms 68.1R01A.20B
O/P cap: O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SI7716ADN/ 13.5mOhm/16.5mohm@4.5Vgs/ 84.07716.037
Switching freq-->400KHz

<Core Design>

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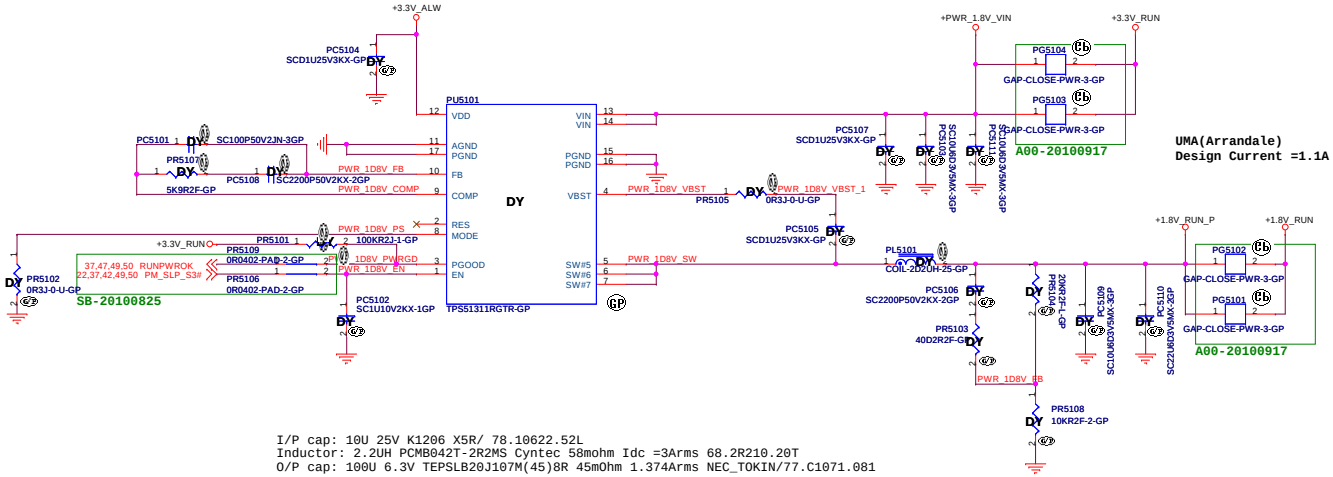
Title: TPS51116_+1.5V_SUS

Size: Custom | Document Number: Winery13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 50 of 92

SSID = PWR.Plane.Regulator_1p8v

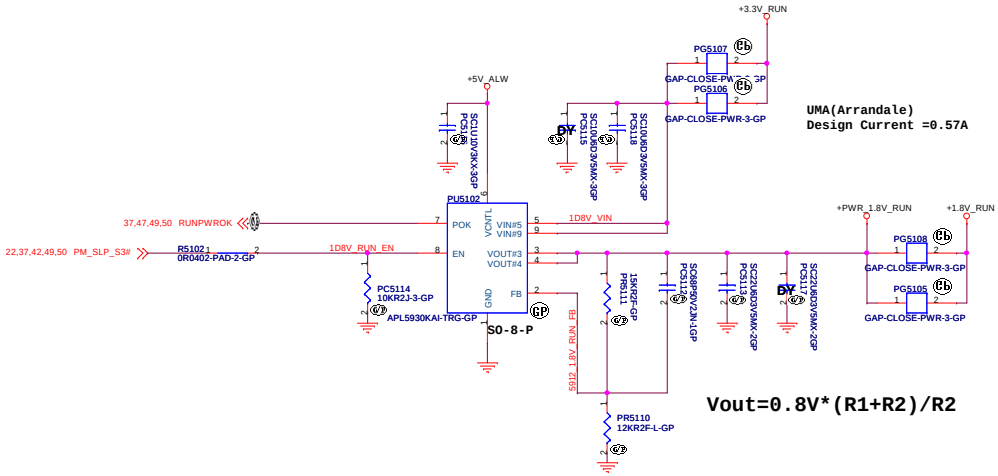
TPS51311RGTR for +1.8V_RUN



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH PCMB042T-2R2MS Cyntec 58mohm Idc =3Arms 68.2R210.20T
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081

SB-20100819

APL5930 for +1.8V_RUN



Vout=0.8V*(R1+R2)/R2

<Core Design>

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Title	TPS51311 +1.8V RUN	
Size: Custom	Document Number: RYU2 13 UMA	Rev: A00
Date: Tuesday, September 28, 2010	Sheet 51 of 92	

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<Core Design>

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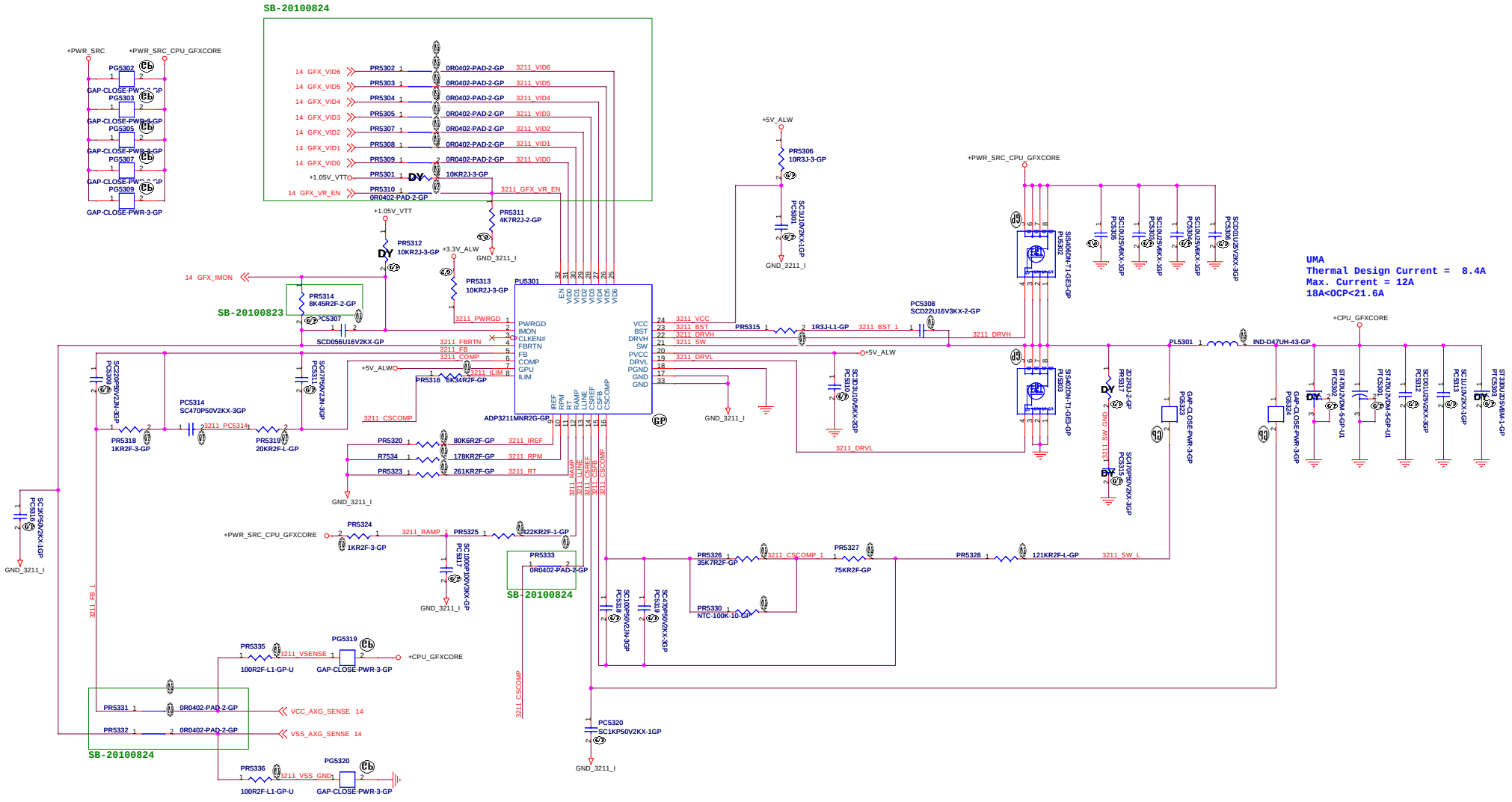
Title: ***(Reserved)***

Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 Sheet 52 of 92

SSID = CPU.GFX.Regulator



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.47UH PCMB061H-R47MS Cyntec DCR:8.4mohm Isat=18Arms 68.R4710.20C
O/P cap: 330U 2.5V M3528/ 9mOhm 3.073Arms NEC/TOKIN/ 80.3371V.A2L
O/P cap: EEFLX0D331R EL 330U 2V M 7.3*4.3 6mOhm 3.5Arms PANASONIC 79.33719 2EL
H/S: SIS406DN/ POWERPAK-8/11.5mOhm/14.5mOhm@4.5Vgs/Id=12.2A/ 84.00406.037
L/S: SIS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/Id=35A/ 84.00402.037

<Core Design>

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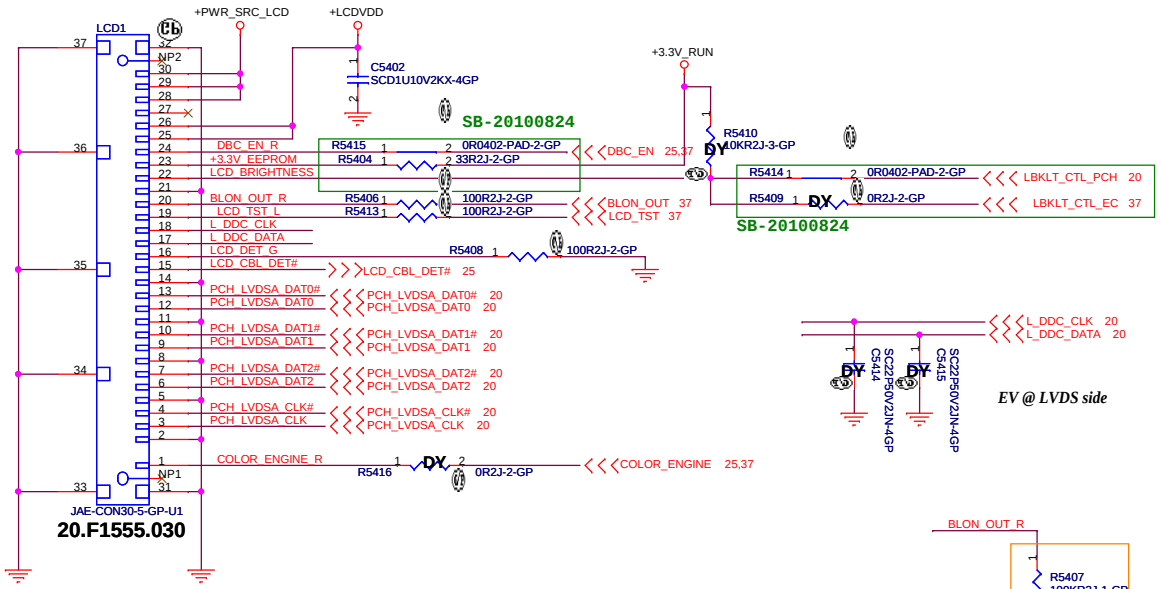
Title: ADP3211 CPU_GFXCORE

Size: Custom | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 53 of 92

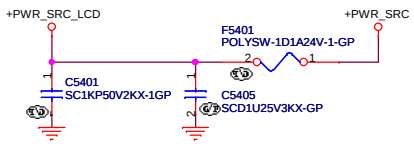
SSID = VIDEO

LVDS CONNECTOR



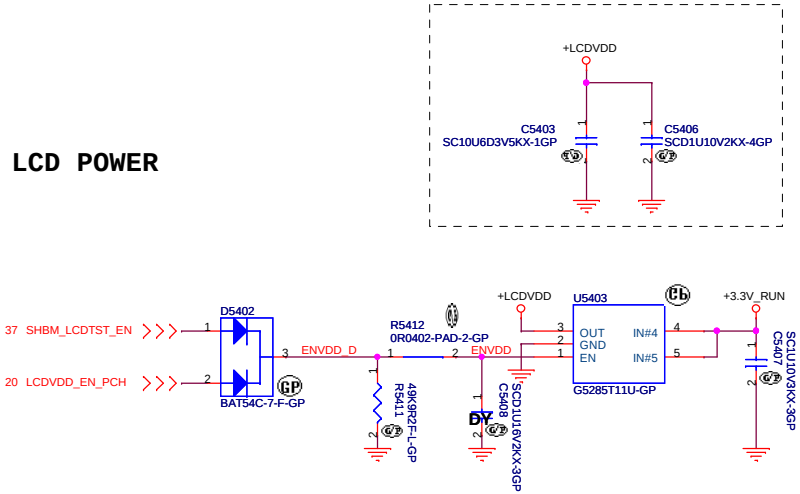
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



<Core Design>

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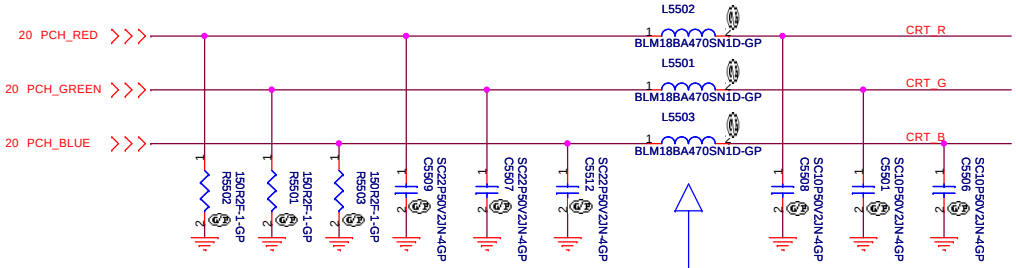
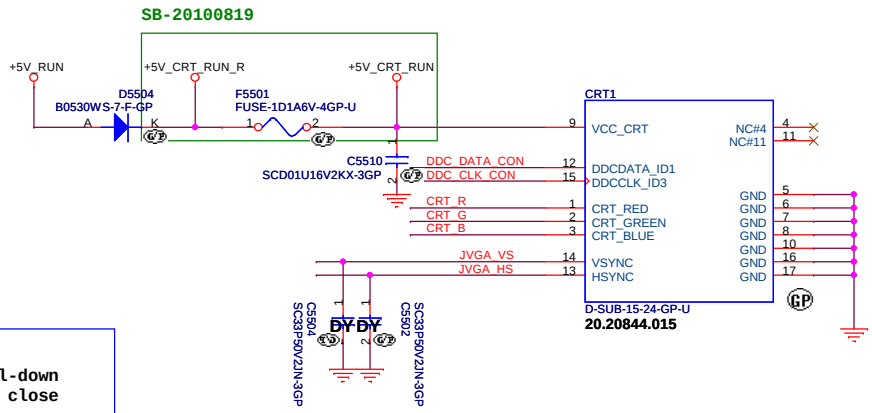
Title	LCD/Inverter Connector	
Size: Custom	Document Number: RYU2 13 UMA	Rev: A00
Date: Tuesday, September 28, 2010	Sheet 54 of 89	

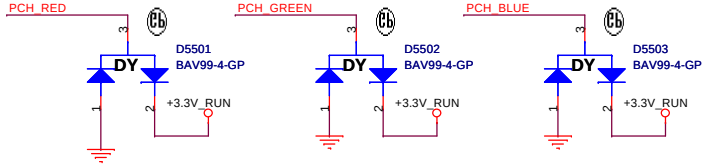
SSID = VIDEO



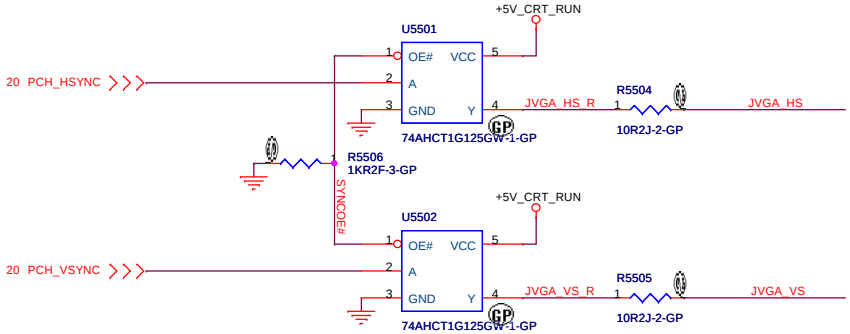


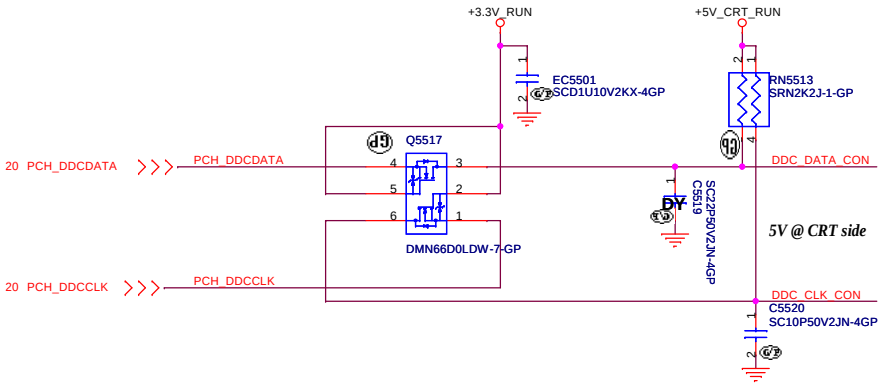
Layout Note:

*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



Hsync & Vsync





<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector

Size: A3 | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 55 of 92

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<Core Design>

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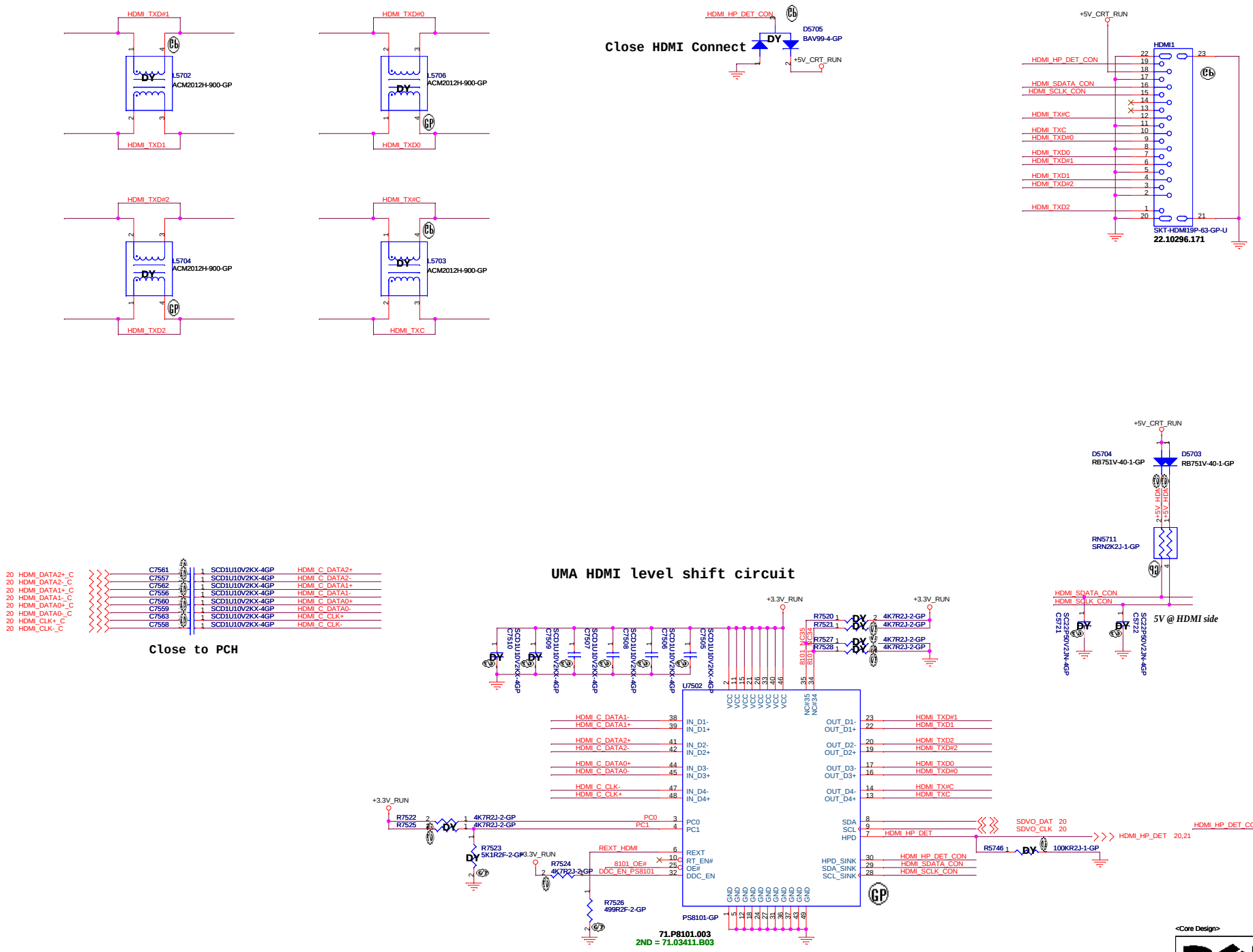
Title

(Reserved)

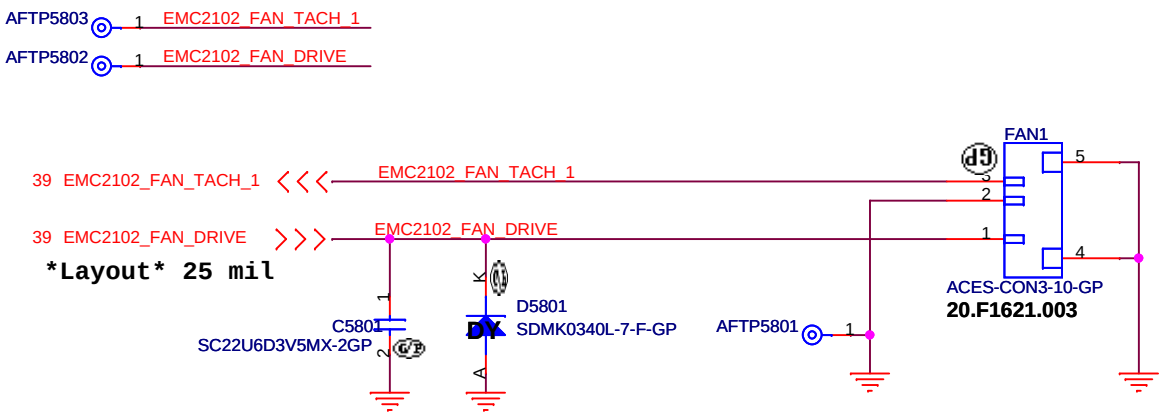
Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 Sheet 56 of 92


HDMI_TXD#1
L5702
ACM2012H-900-GP
HDMI_TXD1
HDMI_TXD#0
L5706
ACM2012H-900-GP
HDMI_TXD0
HDMI_TXD#2
L5704
ACM2012H-900-GP
HDMI_TXD2
HDMI_TX#C
L5703
ACM2012H-900-GP
HDMI_TXC
HDMI_HP_DET_CON
D5705
BAV99-4-GP
+5V_CRT_RUN
Close HDMI Connect
HDMI1
HDMI_HP_DET_CON
HDMI_SDATA_CON
HDMI_SCLK_CON
HDMI_TX#C
HDMI_TXC
HDMI_TXD#0
HDMI_TXD0
HDMI_TXD#1
HDMI_TXD1
HDMI_TXD#2
HDMI_TXD2
SKT-HDMI19P-63-GP-U
22.10296.171
D5704
RB751V-40-1-GP
D5703
RB751V-40-1-GP
RN5711
SRN2K2J-1-GP
5V @ HDMI side
C5721
C5722
SC22P50V2JN-4GP
20 HDMI_DATA2+_C
20 HDMI_DATA2-_C
20 HDMI_DATA1+_C
20 HDMI_DATA1-_C
20 HDMI_DATA0+_C
20 HDMI_DATA0-_C
20 HDMI_CLK+_C
20 HDMI_CLK-_C
C7561
C7557
C7562
C7556
C7560
C7559
C7563
C7558
SCD1U10V2KX-4GP
HDMI_C_DATA2+
HDMI_C_DATA2-
HDMI_C_DATA1+
HDMI_C_DATA1-
HDMI_C_DATA0+
HDMI_C_DATA0-
HDMI_C_CLK+
HDMI_C_CLK-
Close to PCH
UMA HDMI level shift circuit
+3.3V_RUN
R7520
R7521
R7527
R7528
4K7R2J-2-GP
U7502
PS8101-GP
HDMI_C_DATA1-
HDMI_C_DATA1+
HDMI_C_DATA2+
HDMI_C_DATA2-
HDMI_C_DATA0+
HDMI_C_DATA0-
HDMI_C_CLK-
HDMI_C_CLK+
IN_D1-
IN_D1+
IN_D2-
IN_D2+
IN_D3-
IN_D3+
IN_D4-
IN_D4+
PC0
PC1
REXT
RT_EN#
OE#
DDC_EN
OUT_D1-
OUT_D1+
OUT_D2-
OUT_D2+
OUT_D3-
OUT_D3+
OUT_D4-
OUT_D4+
SDA
SCL
HPD
HPD_SINK
SDA_SINK
SCL_SINK
HDMI_TXD#1
HDMI_TXD1
HDMI_TXD2
HDMI_TXD#2
HDMI_TXD0
HDMI_TXD#0
HDMI_TX#C
HDMI_TXC
HDMI_HP_DET
HDMI_HP_DET_CON
HDMI_SDATA_CON
HDMI_SCLK_CON
SDVO_DAT 20
SDVO_CLK 20
HDMI_HP_DET 20,21
R5746
100KR2J-1-GP
R7522
R7525
R7523
5K1R2F-2-GP
R7524
4K7R2J-2-GP
REXT_HDMI
8101_OE#
DDC_EN_PS8101
R7526
499R2F-2-GP
R7515
20KR2J-L2-GP
Q7503
2N7002A-7-GP
71.P8101.003
2ND = 71.03411.B03
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI Connector
Size
Custom
Document Number
RYU2 13 UMA
Rev
A00
Date: Tuesday, September 28, 2010
Sheet 57 of 92

SSID = Thermal

Fan Connector



<Core Design>

Wistron Corporation
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Title		
	FAN	
Size A4	Document Number RYU2 13 UMA	Rev A00
Date: Tuesday, September 28, 2010	Sheet 58 of 92	

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<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

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<Core Design>

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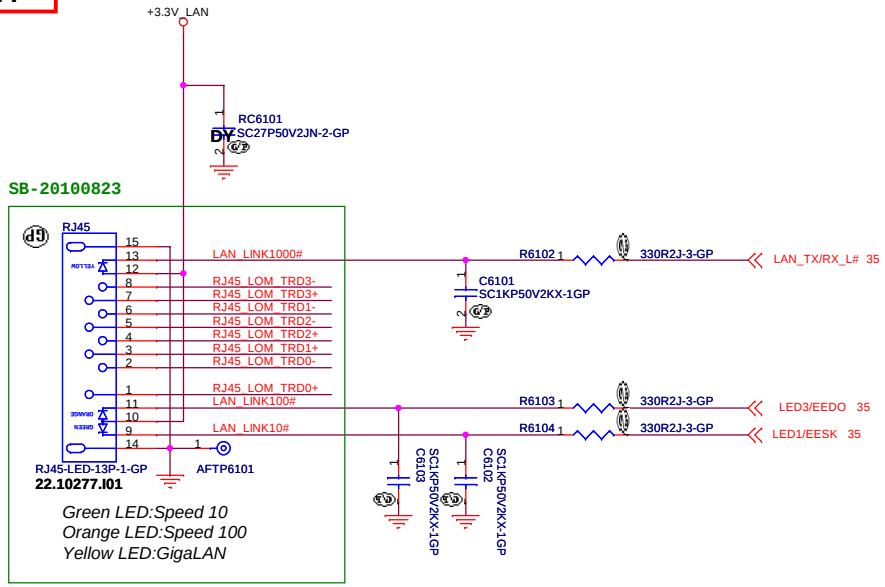
Title

(Reserved)

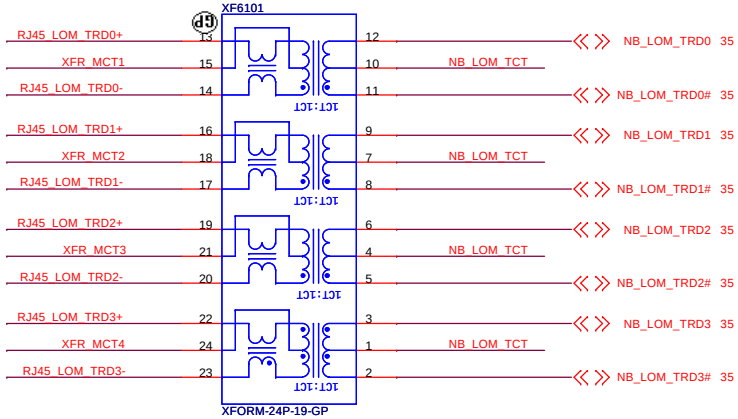
Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

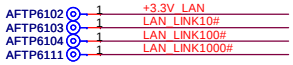
Date: Tuesday, September 28, 2010 Sheet 60 of 92

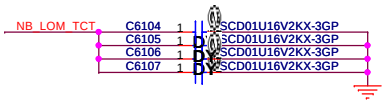
SSID = LOM

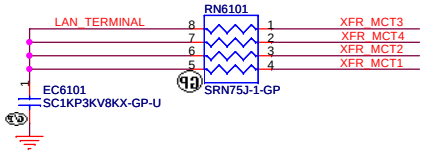


10/100/1000M Lan Transformer









1.Route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.Pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

Off /No link – no light
10Mbps – Green
100Mbps – Orange
1000Mbps – Yellow (Orange/Green Combination)
Activity LED - Separate blinking yellow LED to indicate traffic

<Core Design>

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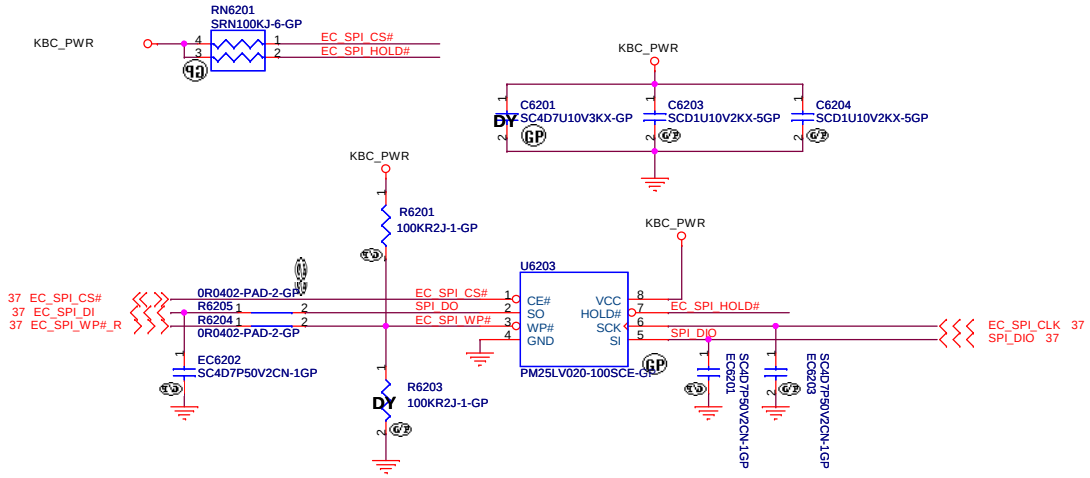
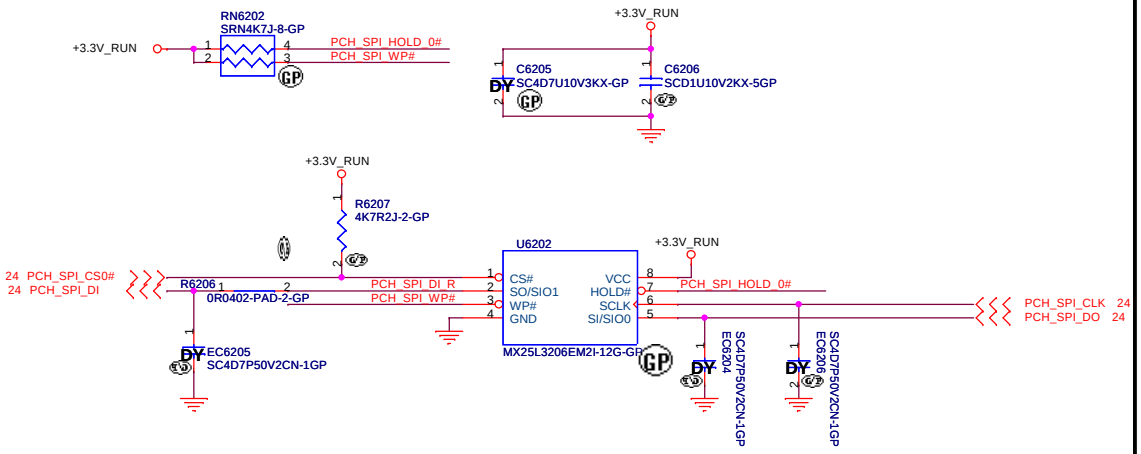
Title	***RJ45/Transformer***	
Size A3	Document Number ***RYU2 13 UMA***	Rev ***A00***
Date: Tuesday, September 28, 2010	Sheet 61 of 92	

SSID = Flash.ROM

SPI FLASH ROM (2M bits) for KBC

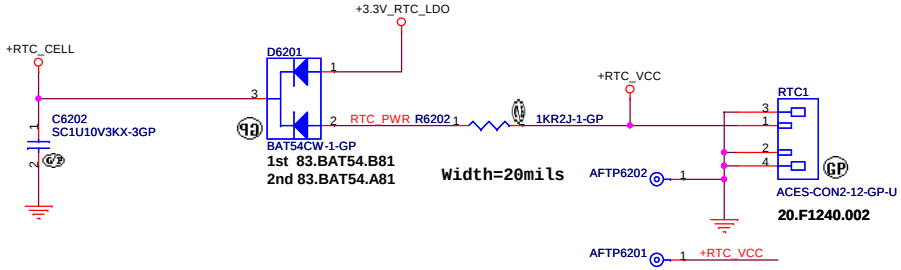


SPI FLASH ROM (32M bits) for PCH



SSID = RBATT

RTC Connector



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

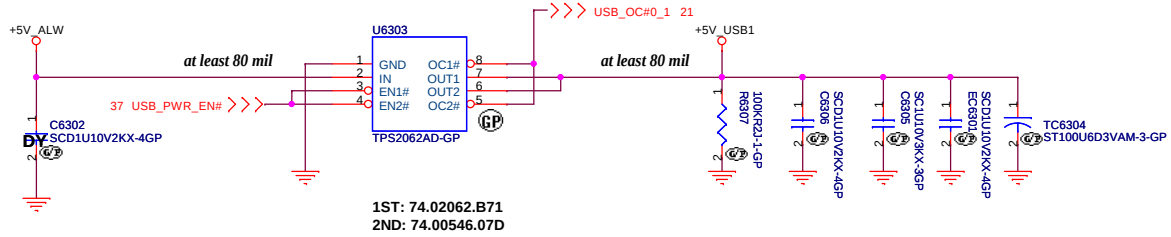
Title: EEPROM/RTC Connector

Size: A3 | Document Number: RYU2 13 UMA | Rev: A00

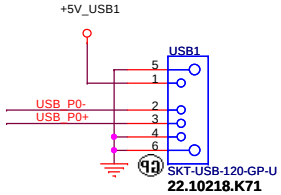
Date: Tuesday, September 28, 2010 | Sheet 62 of 92

SSID = USB

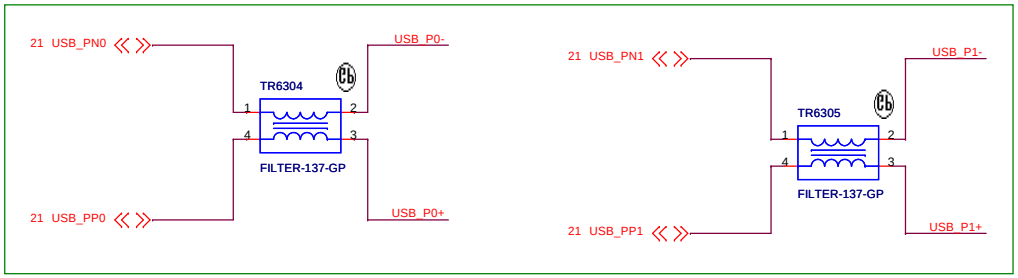
USB Port Power SW

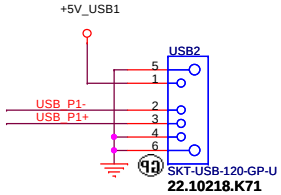


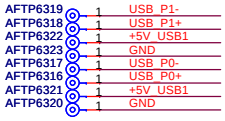
1ST: 74.02062.B71
2ND: 74.00546.07D



SB-20100824

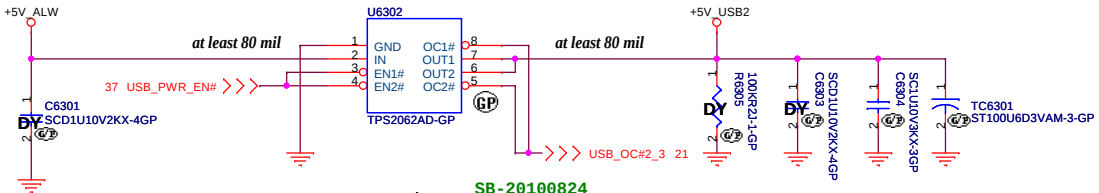


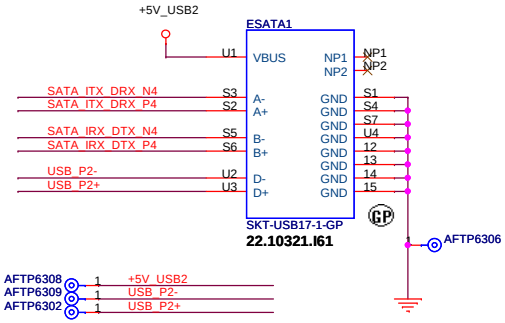




SSID = ESATA

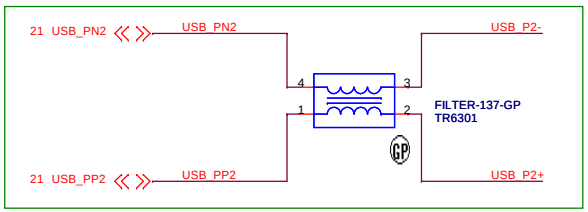
ESATA Power





SB-20100824

SB-20100824



SB-20100824

SB-20100824

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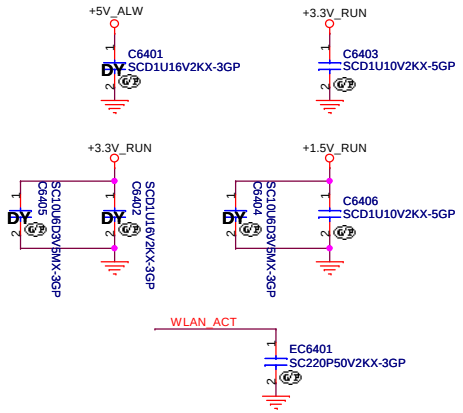
Title: USB/ESATA Port

Size	Document Number	Rev
A3	RYU2 13 UMA	A00

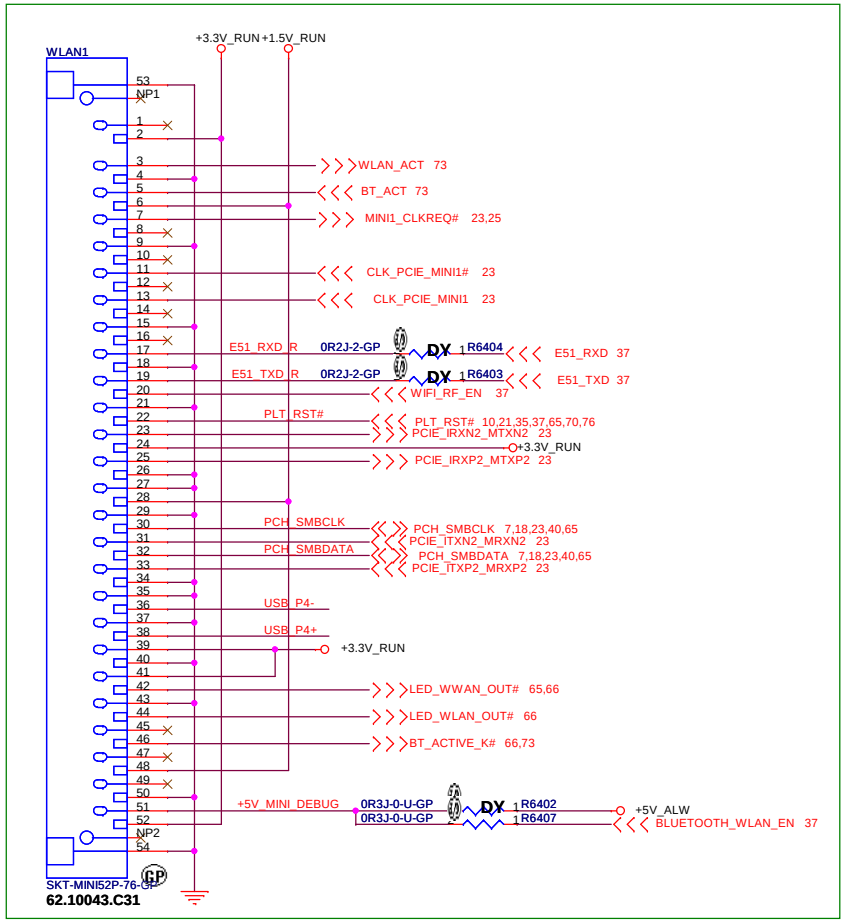
Date: Tuesday, September 28, 2010 Sheet 63 of 92

SSID = Wireless

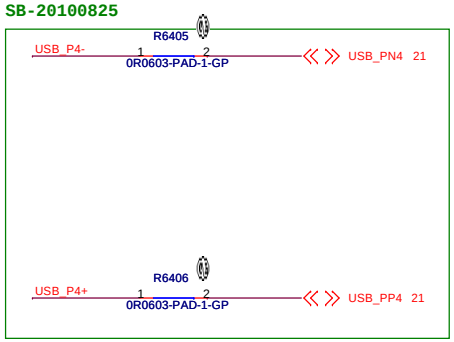
Mini Card Connector(802.11a/b/g/n)



SB-20100823



SB-20100825



<Core Design>

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Title: MINICARD(WLAN)/ITP CONN

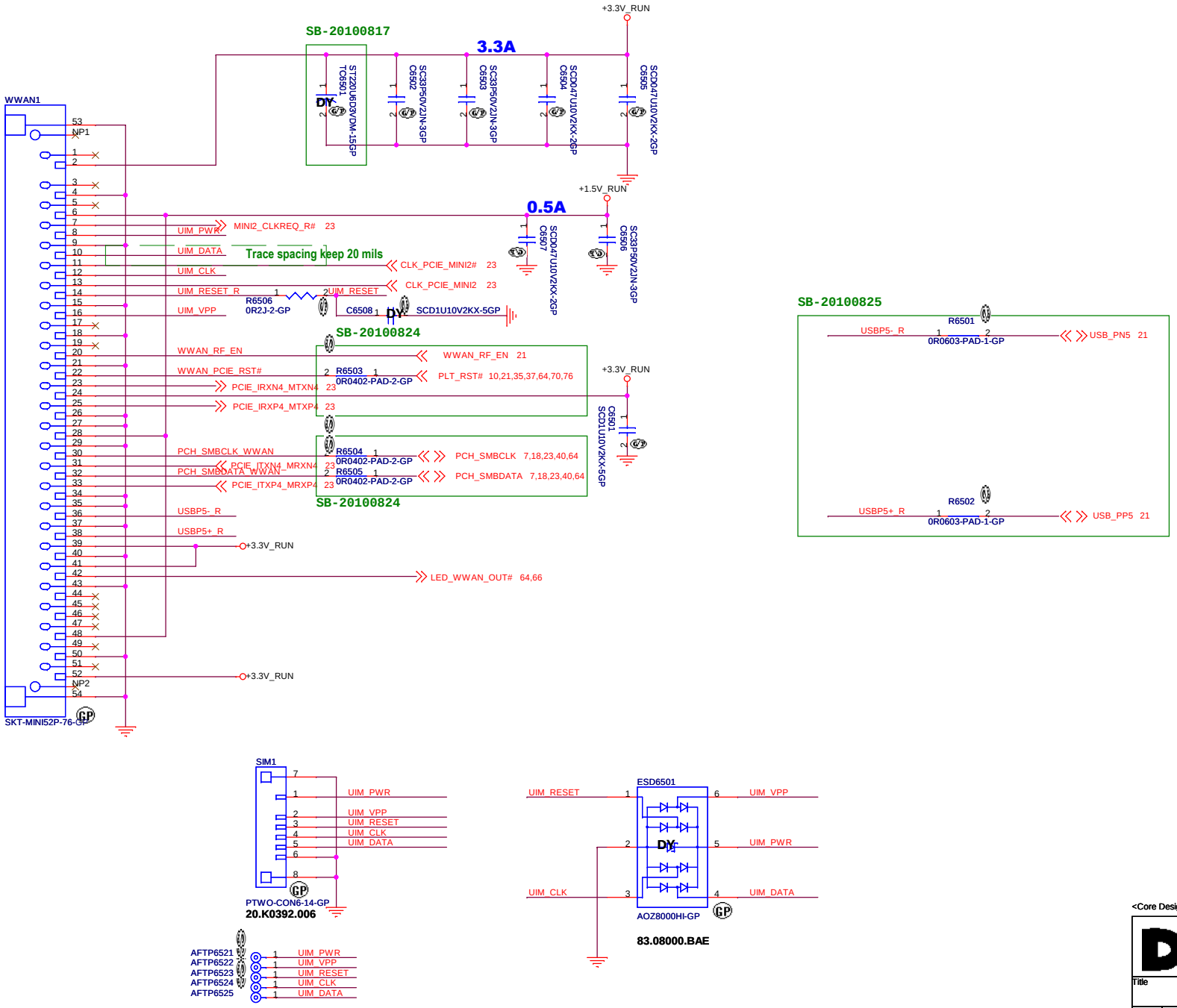
Size: A3 | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 64 of 92

SSID = WWAN

Layout note: Place caps C6501~C6507, TC6501 close WWAN1 connector.

MiniCard WWAN connector



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Title: WWAN Connector

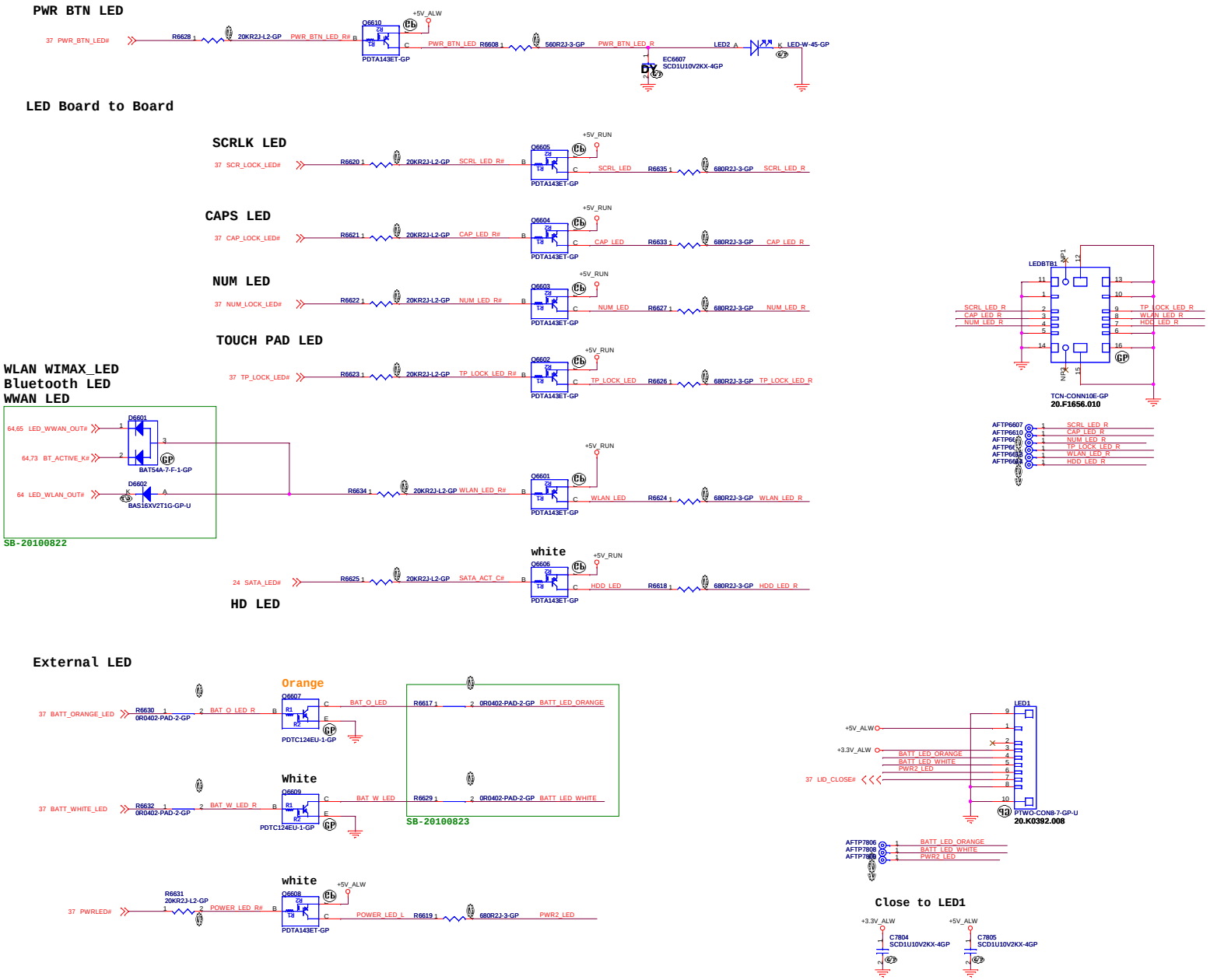
Size: A3 | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 65 of 92

SSID = LED

For LED & Capacity board:

LED Type	Color	Power rail
BATTERY LED1	Amber(Multi-color)	ALW
SCRL LED	White	ALW
CAP LED	White	ALW
NUM LED	White	ALW
PWR BTN LED	White	ALW
SATA ACT LED1	White	RUN
BT ACT LED	White	RUN
WLAN/WWAN ACT LED	White	RUN



<Core Design>
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Title: LED

Size: A2 | Document Number: RYU2 13 UMA | Rev: A00

Date: Tuesday, September 28, 2010 | Sheet 66 of 92

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Title

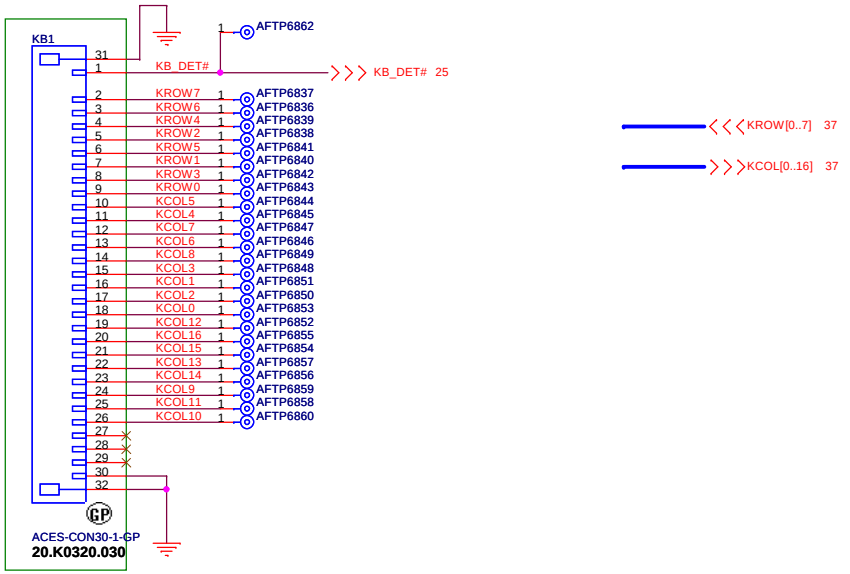
(Reserved)

Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 Sheet 67 of 92

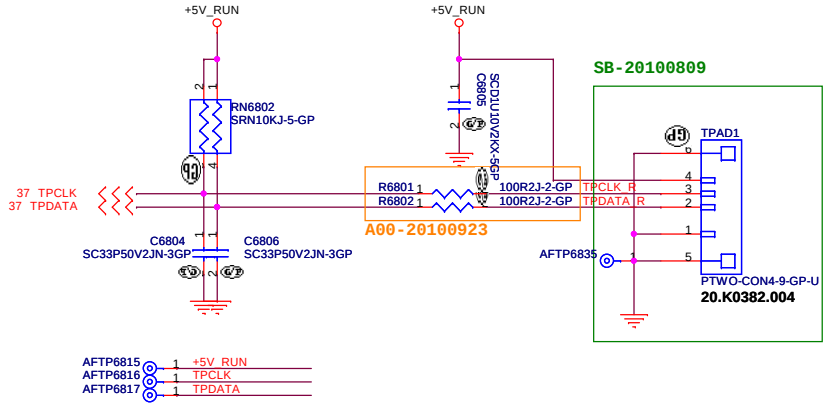
SSID = KBC

Internal KeyBoard Connector



SSID = Touch.Pad

TouchPad Connector



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Title: *Keyboard/Touch Pad*

Size	Document Number	Rev
A3	*RYU2 13 UMA*	*A00*

Date: Tuesday, September 28, 2010 Sheet 68 of 92

(Blank)

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Title

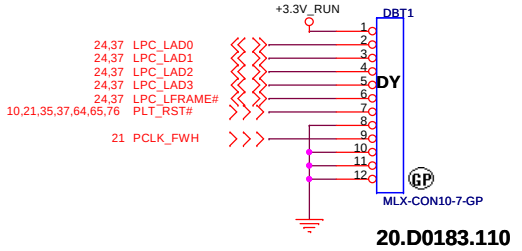
Hall sensor

Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

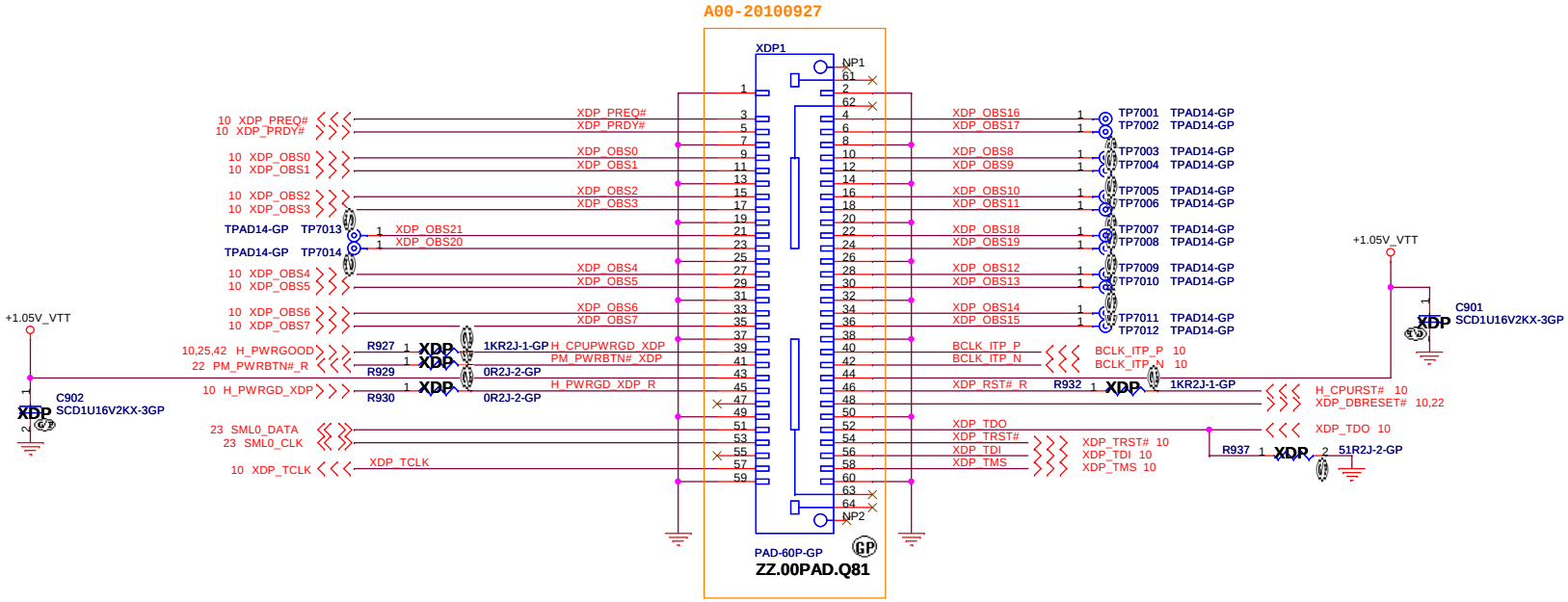
Date: Tuesday, September 28, 2010 Sheet 69 of 92

SSID = DEBUG PORT

GOLDEN FINGER FOR DEBUG BOARD



SSID = CPU



<Core Design>

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Title	Debug port	
Size A3	Document Number RYU2 13 UMA	Rev A00
Date: Tuesday, September 28, 2010	Sheet 70 of 92	

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<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 Sheet 71 of 92

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Title

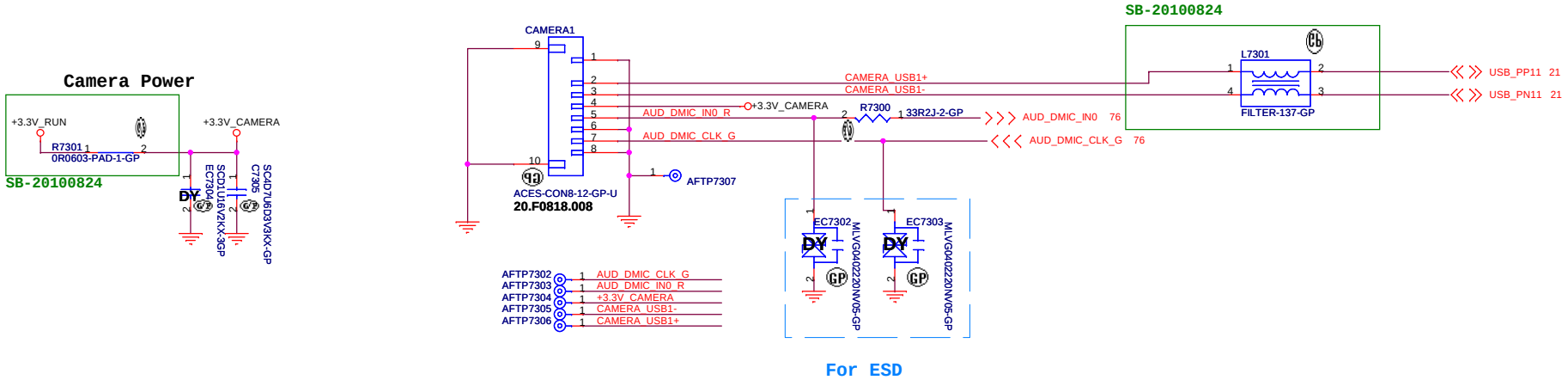
(Reserved)

Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 Sheet 72 of 92

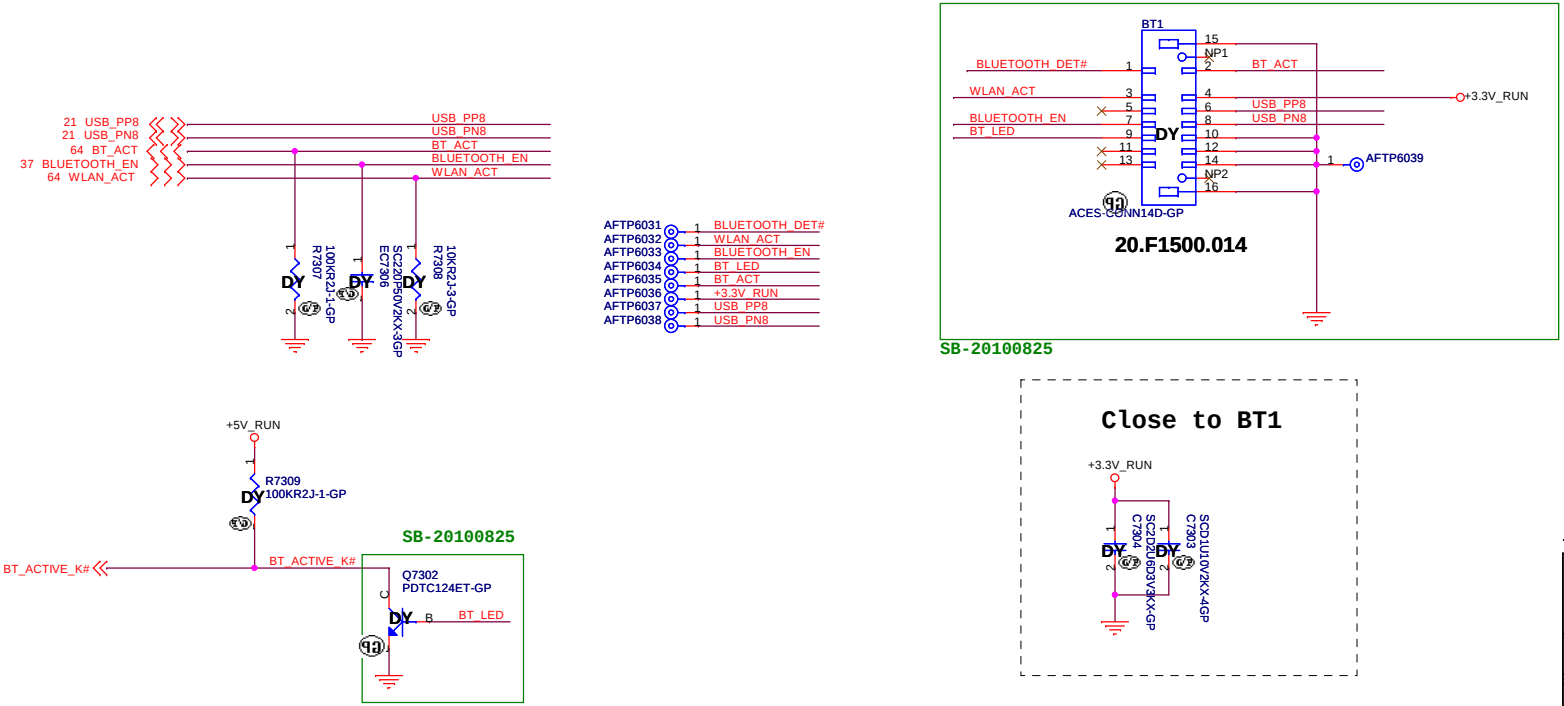
SSID = User.Interface

Camera Connector



SSID = User.Interface

Bluetooth cable conn.



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Title		
Camera CONN		
Size A3	Document Number RYU2 13 UMA	Rev A00
Date: Tuesday, September 28, 2010	Sheet 73 of 92	

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Title: *(Reserved)*

Size	Document Number	Rev
A4	*RYU2 13 UMA*	*A00*

Date: Tuesday, September 28, 2010 Sheet 74 of 92

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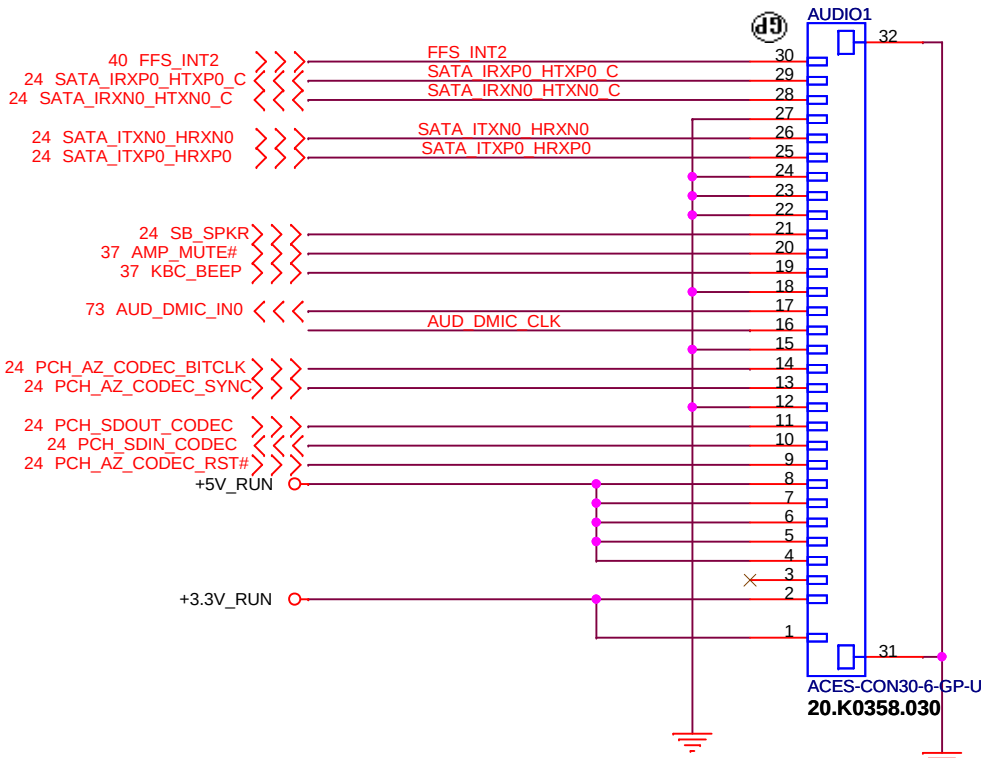
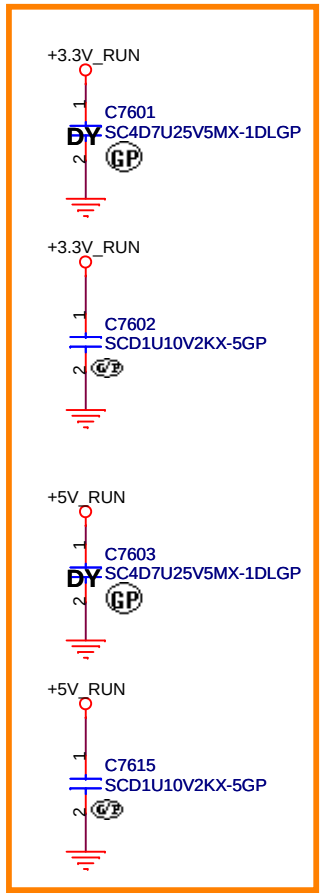
Title	***(Reserved)***	
Size A4	Document Number ***RYU2 13 UMA***	Rev ***A00***
Date: Tuesday, September 28, 2010	Sheet 75 of 92	

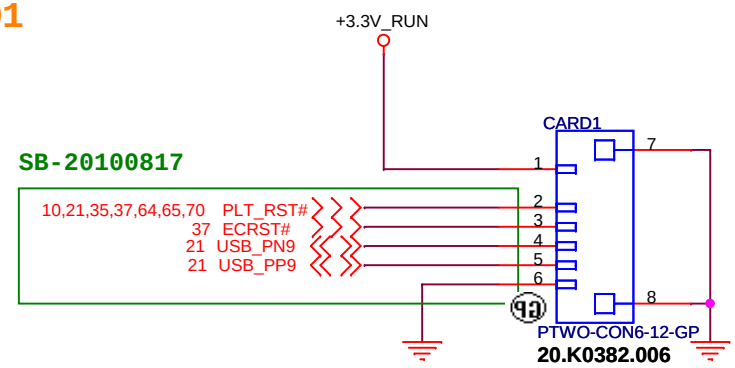
Audio baord CONN



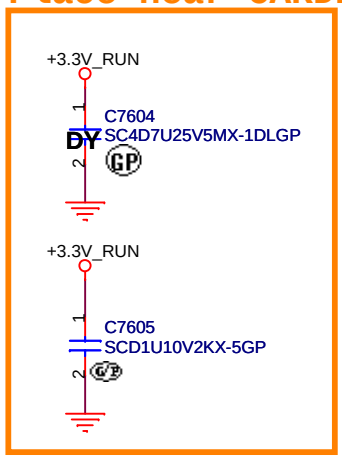
Place near AUDIO1

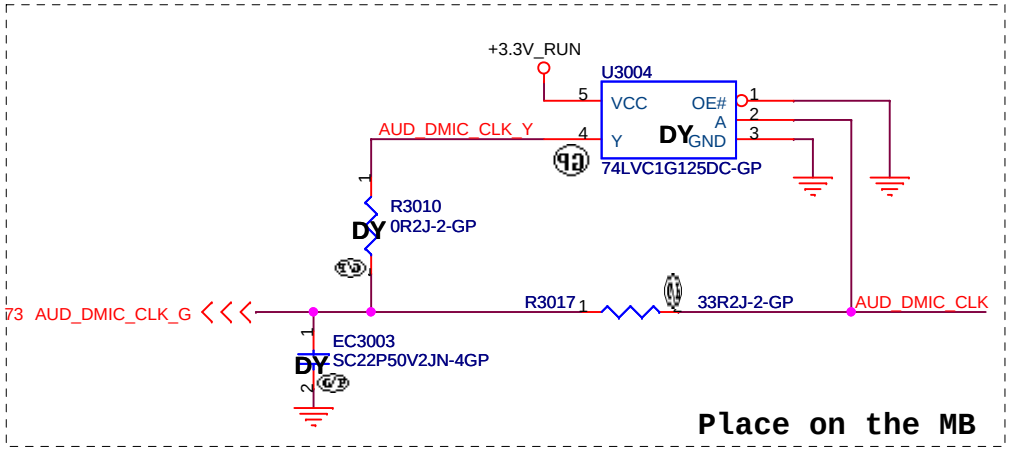


SB-20100817



Place near CARD1





<Core Design>

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Title: ***DC_IN Board BTB Connector***

Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 Sheet 76 of 92

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<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 Sheet 77 of 92

(Blank)

<Core Design>

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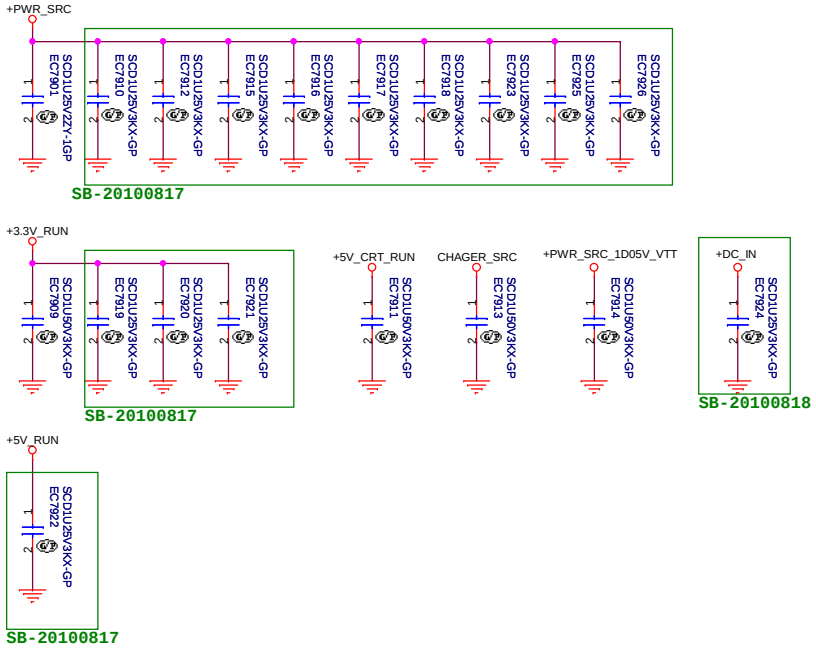
Title

(Reserved)

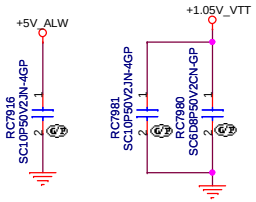
Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 Sheet 78 of 92

SSID = EMI

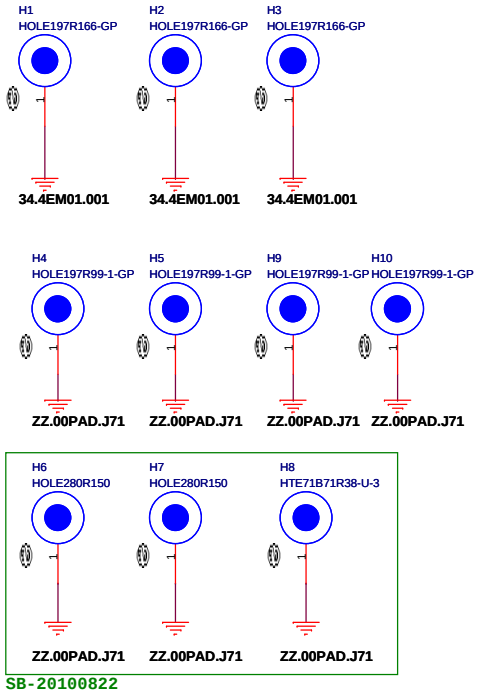


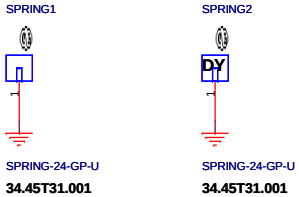
SSID = RF



SSID = Mechanical

HOLE:





<Core Design>

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Title: ***Miscellaneous Components***

Size: Custom | Document Number: ***RYU2 13 UMA*** | Rev: ***A00***

Date: Tuesday, September 28, 2010 | Sheet 79 of 89

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<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 Sheet 80 of 92

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<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 Sheet 81 of 92

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Title

(Reserved)

Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 Sheet 82 of 92

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<Core Design>

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Title: ***(Reserved)***

Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

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Title: ***(Reserved)***

Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 Sheet 84 of 92

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<Core Design>

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Title: ***(Reserved)***

Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 Sheet 85 of 92

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<Core Design>

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Title: ***(Reserved)***

Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 | Sheet 86 of 92

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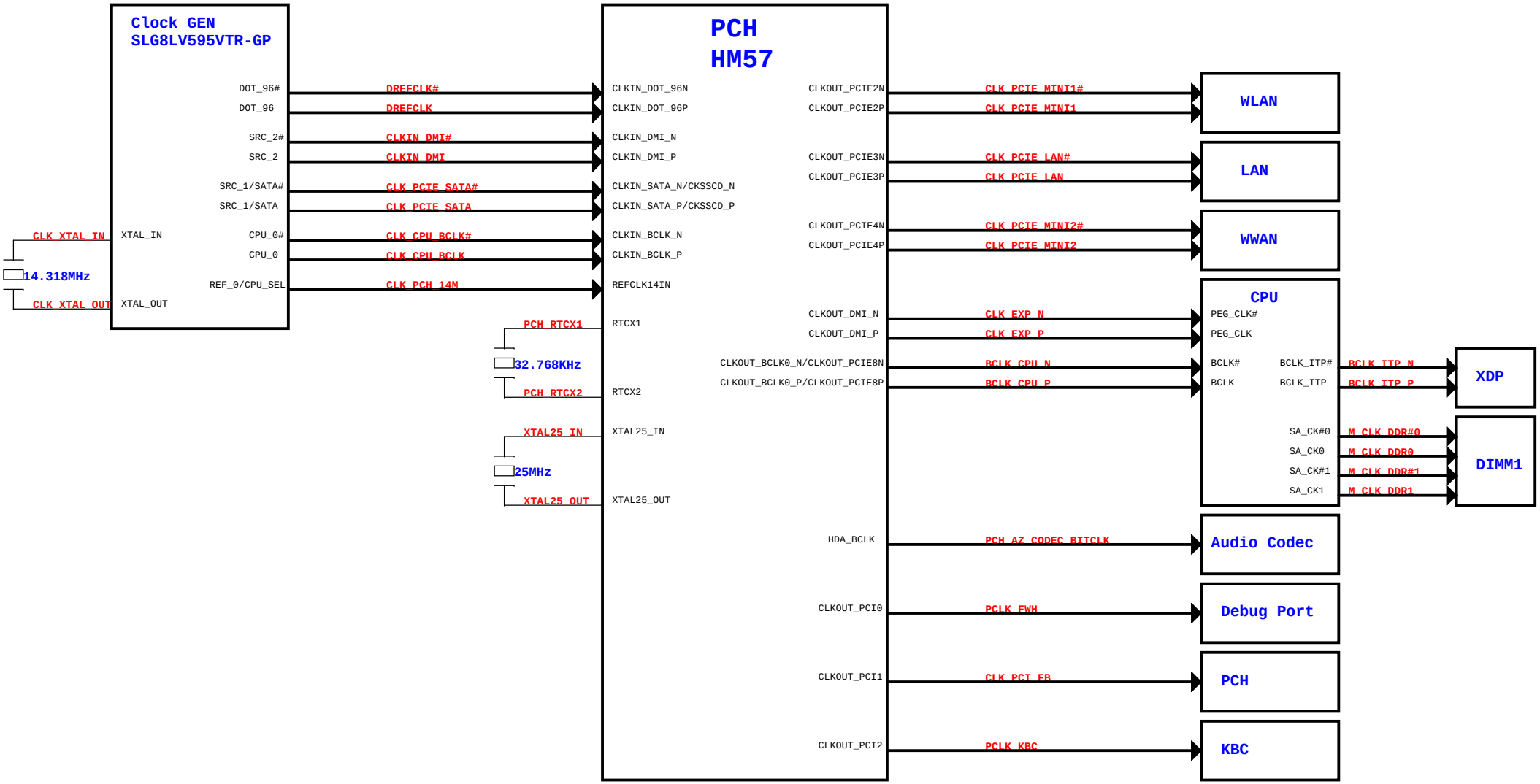
Title: ***(Reserved)***

Size	Document Number	Rev
A4	***RYU2 13 UMA***	***A00***

Date: Tuesday, September 28, 2010 | Sheet 87 of 92

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	43	2010/07/30	EE	+DC_IN short to GND	Modify DCIN1 connector pin4, pin5 connect to GND.	SB
2	37	2010/07/30	EE	SW1 always short to GND.	Change pin 6 connect to GND.	SB
3	68	2010/08/09	EE		Change TPAD1 pin defined.	SB
4	68	2010/08/13	EE		Change KB1 connector to 20.K0320.030.	SB
5	76	2010/08/17	EE		Add ECRST# connect to CARD1 pin 3.	SB
6	79	2010/08/17	EMI		Between +PWR_SRC and GND add 0.1uf/50v cap X 9. Between +3.3V_RUN and GND add 0.1uf/50v cap X 3. Between +5V_RUN and GND add 0.1uf/50v cap X 1. Between +DC_IN and GND add 0.1uf/50v cap X 1. Between +DC_IN and GND add 0.1uf/50v cap.	SB
7	47	2010/08/18	Power		Change +VCC_CORE VID3~5 from 001 to 010.	SB
8	37	2010/08/19	EE		Add LID_CLOSE# pull high resistor to +3.3V_ALW.	SB
9	51	2010/08/19	EE		Co-lay +1.8V_RUN LDO power solution.	SB
10	55	2010/08/19	EE		Between +5V_RUN and +5V_CRT_RUN add Fuse.	SB
11	45	2010/08/22	ME		Change PC4532, PC4530, PC4533 from 1206 size to 0805 size for ME request.	SB
12	45	2010/08/22	Power		Change PU4505 from SIS7716 to SIS412DN (84.00412.037). For cost down.	SB
13	47	2010/08/22	Power		PR4714 change to 2.2K for OTP & OCP setting. PR4715 change to 4.7K for OTP & OCP setting. PR4716 change to 7.15K for OTP & OCP setting. PR4721 change to 78.7K for Load Line & COMP setting. PC4705 change to 27pF for Load Line & COMP setting. PR4728 change to 63.4K for Current Monitor setting. PC4709 change to 22nF for Current Monitor setting.	SB
14	66	2010/08/22	EE		Add D6601, D6602 for wireless function.	SB
15	7	2010/08/23	RF		Add RC701, RC702 for RF request.	SB
16	42	2010/08/23	EE		Change +1.5V_CPU power rail from +1.5V_RUN to +1.5V_SUS.	SB
17	53	2010/08/23	Power		PR5314 :7.5k change to 8.45K(64.84515.6DL) for GFX core imon.	
18	61	2010/08/23	EE		Change RJ45 connector to 22.10277.I01 for hi-port fail.	SB
19	64,65	2010/08/23	EE		Change WLAN1, WWAN1 connector to 62.10043.C31.	SB



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Title: ***Clock Block Diagram***

Size	Document Number	Rev
A3	RYU2 13 UMA	A00

Date: Tuesday, September 28, 2010 Sheet 89 of 92

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
20	66	2010/08/23	EE		Change R6617, R6629 to 0ohm.	SB
21	63,73	2010/08/24	EMI		Change USB port0, port1, port2 and camera from 0 ohm to common chock.	SB
22	73	2010/08/25	EE		Dummy BT 365 function.	SB
23	24	2010/08/25	EE		Change C2402 from 12PF to 5PF.For Vendor recommend. Change C2403 from 12PF to 6PF.For Vendor recommend.	SB
24	7	2010/08/25	EE		Change C714, C715 from 12PF to 15PF for vendor recommend.	SB
25	47,49	2010/08/25	Power	SI7686DP-T1-GE3-GP will EOL.	PU4702, PU4703, PU4902: (SI7686DP-T1-GE3-GP) change to SIR172DP-T1-GE3-GP 84.00172.037	SB

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	7	2010/08/24	EE	Cost down	Change R708, R709, RN701, RN702, RN703, RN704 from 0 ohm to short pad.	SB
2	10	2010/08/23	EE	Cost down	Dummy U927, R989, R977, Q901, C915, R934, R989. Add R935, R919. Change R920 to 3 K ohm.	SB
3	10	2010/08/24	EE	Cost down	Change R906, R909, R921, R924, R926 from 0 ohm to short pad.	SB
4	20	2010/08/24	EE	Cost down	Change R2011 from 0 ohm to short pad.	SB
5	21	2010/08/24	EE	Cost down	Change R2104, R2121 from 0 ohm to short pad.	SB
6	21	2010/08/24	EE	Cost down	Change R2519, R2102, R2105 from single resistor to array resistor.	SB
7	22	2010/08/24	EE	Cost down	Change R2207, R2210, R2218, R2213, R2216, R2219, R2220, R2211, R2212 from 0 ohm to short pad.	SB
8	23	2010/08/24	EE	Cost down	Change RN2311, RN2312, RN2314 from 0 ohm to short pad.	SB
9	23	2010/08/24	EE	Cost down	Change R2302, R2201, R2301, R2209 from single resistor to array resistor.	SB
10	24	2010/08/24	EE	Cost down	Change R2417 from 0 ohm to short pad.	SB
11	25	2010/08/24	EE	Cost down	Change R2521, R2334, R2522, R2512, R2411, R2513, R2217, R2538, R2304, R2533, R2416, R2503, R2535, R2214 from single resistor to array resistor.	SB
12	26	2010/08/24	EE	Cost down	Change R2606, R2605, R2601, R2609, R2602 from 0 ohm to short pad.	SB
13	27	2010/08/24	EE	Cost down	Change R2707 from 0 ohm to short pad.	SB
14	35	2010/08/24	EE	Cost down	Change R3509, R3512, R3508, R3514 from 0 ohm to short pad.	SB
15	35	2010/08/24	EE	Cost down	Change R3517, R3518 from single resistor to array resistor.	SB
16	37	2010/08/24	EE	Cost down	Change R3706, R3730, RR3720, R3707, R3753, R3702, R3723, R3727 from 0 ohm to short pad.	SB
17	37	2010/08/24	EE	Cost down	Change R3742, R3743 from single resistor to array resistor.	SB
18	39	2010/08/24	EE	Cost down	Change R3910, R3906 from single resistor to array resistor.	SB
19	44	2010/08/24	EE	Cost down	Change R4401 from 0 ohm to short pad.	SB

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Title: *Change List(1/3)*

Size: A3 | Document Number: *RYU2 13 UMA* | Rev: *A00*

Date: Tuesday, September 28, 2010 | Sheet 91 of 89

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
20	45	2010/08/24	EE	Cost down	Change PR4522, PR4515, PR4530, PR4531, PR4533, PR4524 from 0 ohm to short pad.	SB
21	46	2010/08/26	EE	Cost down	Dummy PU4606, PD4605, PR4623, PR4624, PR4625.	SB
22	47	2010/08/24	EE	Cost down	Change PR4719, R4710, PR4701, PR4702, PR4703, PR4704, PR4705, PR4707, PR4708 from 0 ohm to short pad.	SB
23	49	2010/08/24	EE	Cost down	Change PR4924 from 0 ohm to short pad.	SB
24	50	2010/08/24	EE	Cost down	Change PR5014, PR5002 from 0 ohm to short pad.	SB
25	53	2010/08/24	EE	Cost down	Change PR5302, PR5303, PR5304, PR5305, PR5307, PR5308, PR5309, PR5310, PR5331, PR5332, PR5333 from 0 ohm to short pad.	SB
26	54	2010/08/24	EE	Cost down	Change R5415, R5414 from 0 ohm to short pad.	SB
27	63	2010/08/24	EE	Cost down	Change R6304, R6310, R6311, R6312 from 0 ohm to short pad.	SB
28	64	2010/08/25	EE	Cost down	Change R6405, R6406 from 0 ohm to short pad.	SB
29	65	2010/08/24	EE	Cost down	Change R6503, R6504, R6505, R6501, R6502 from 0 ohm to short pad.	SB