First International Computer,Inc

Portable Computer Group HW Department

Board name : MotherBoard Schematic

Project : PTT40TF

Version : 0.4

Initial Date : Jul 06 , 2007

Manager Sign by: AVERY

Drawing by : Tom Lin

Total confirm by: CC_TSAO

LAN Circuit check by:

Audio Circuit check by:

First International Computer, Inc.
5FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

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Title: PTT40TF>AMD+RS690M+SB600+M71S

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1. Schematic Page Description :

DAUGHTER BOARD

2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD17	X
AD27	X
AD29	X

BUSMASTER

REQ	CHIP
REQ0 / GNT0	X
REQ1 / GNT1	X
REQ2 / GNT2	X
REQ3 / GNT3	X
REQ4 / GNT4	X

IRQ Channel	Desciption
IRQ0	System timer
IRQ1	Keyboard
IRQ2	(Casacde)
IRQ3	LAN / MODEM
IRQ4	~~Serial Port~~
IRQ5	AUDIO / VGA / USB
IRQ6	~~FLOPPY DISK~~
IRQ7	~~LPT~~
IRQ8	RTC
IRQ9	ACPI
IRQ10	FIR (Disable by default) (MODEM/LAN)
IRQ11	~~Cardbus~~
IRQ12	PS/2 mouse
IRQ13	FPU
IRQ14	HDD
IRQ15	CDROM

DMA Channel	Device
DMA0	FIR (disable by default) (MODEM / LAN)
DMA1	~~ECP~~
DMA2	~~FLOPPY DISK~~
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

PCIINT	CHIP
IRQA	IEEE1394 (VIA VT6311S)
IRQB	X
IRQC	X
IRQD	X
IRQE / GPIO2	X
IRQE / GPIO3	X
IRQE / GPIO4	PASS0
IRQE / GPIO5	CRISIS

20051228A

First International Computer, Inc.
5FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

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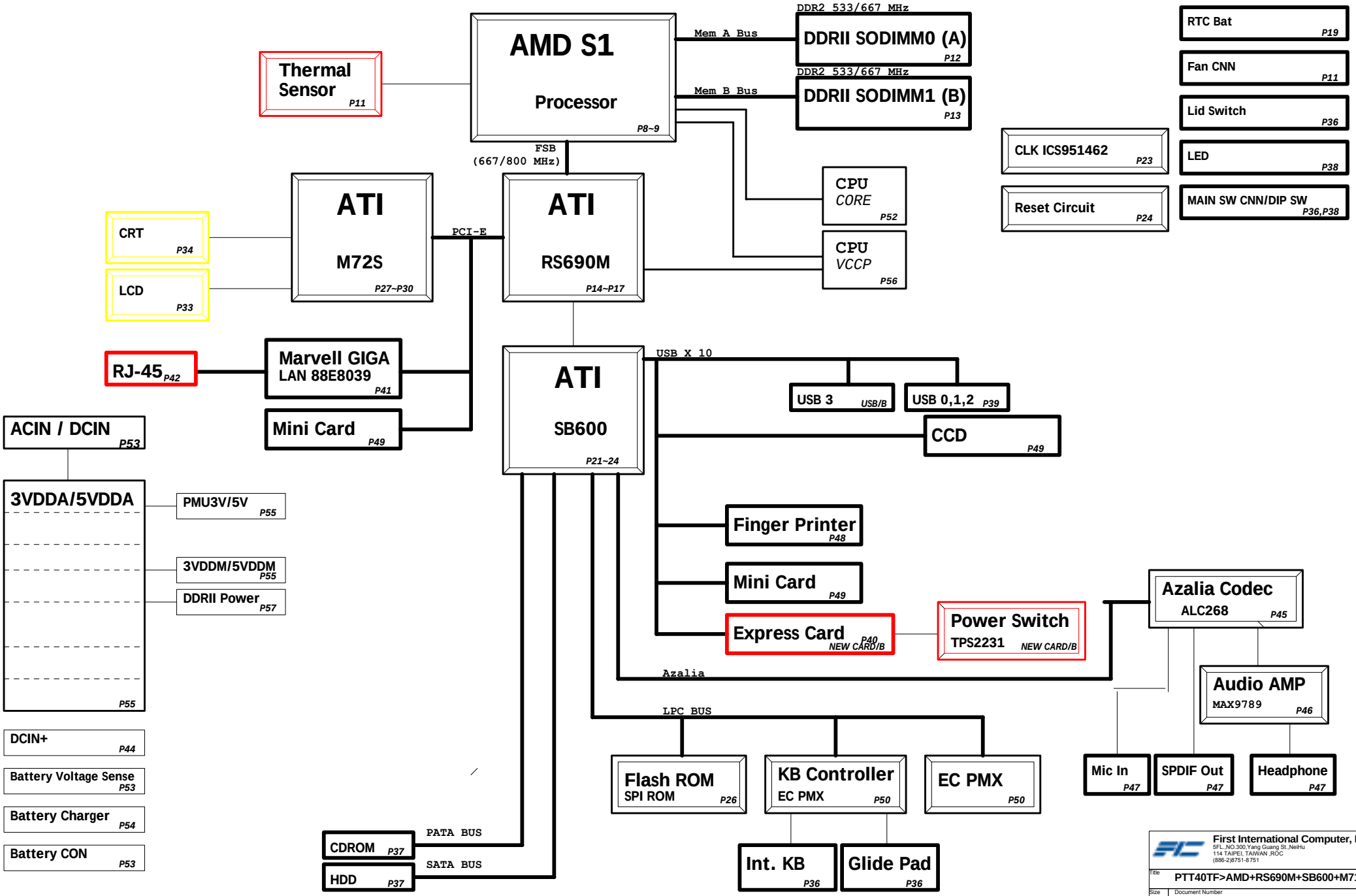
3. Block Diagram :



4. Nat name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON
3VDDA	3.3V always on power rail by DCON
3VDDM	3.3V switched power rail by SUSTAT_B#
5VDDM	5.0V switched power rail by SUSTAT_B#

VCC_CORE	Core Voltage for CPU
1.2VDDM	1.2V power rail for AGTL+ termination/Core for GMCH by SUSTAT_B#
1.5VDDM	1.5V power rail for CPU PLL/DMI;PCIE;DDRII DLLs for GMCH/Core;PCIE for ICH7m by SUSTAT_B#
1.8VDDS	1.8V power rail for DDRII by PSUSC#
0.9VDDT_DDRII	0.9V DDRII Termination Voltage by SUSTAT_B#

Part Naming Conventions

C = Capacitor
CN = Connector
D = Diode
F = Fuse
L = Inductor
Q = Transistor
R = Resistor
RP = Resistor Pack
U = Arbitrary Logic Device
Y = Crystal and Osc

Net Name Suffix

= Active Low signal

5. Board Stack up Description

PCB Layers

Layer 1	Component Side, Microstrip signal Layer
Layer 2	Ground Plane
Layer 3	Stripline Layer(High Speed)
Layer 4	Stripline Layer(High Speed)
Layer 5	Power Plane
Layer 6	Solder Side,Microstrip signal Layer

Layers : 6 Depth 1.2mm Impence 55 ohms +/- 10%

	Single End Impedance	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SRC Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
Host Bus	55 ohm +/- 15%		
DDR2 CLK	42 ohm +/- 15%	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	55 ohm +/- 15%		85 ohm +/- 20%
DDR2 Bus	55 ohm +/- 15%		
DMI Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
PCIE Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SATA		95 ohm +/- 15%	100 ohm +/- 15%
SDVO	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
LVDS		100 ohm +/- 15%	100 ohm +/- 15%
USB		90 ohm +/- 15%	90 ohm +/- 15%
IEEE1394		110 ohm +/- 15%	110 ohm +/- 15%
Lan	50 ohm +/- 15%		

First International Computer, Inc.
5FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751

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6.Schematic modify Item and History :

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114 TAIPEI, TAIWAN ,ROC
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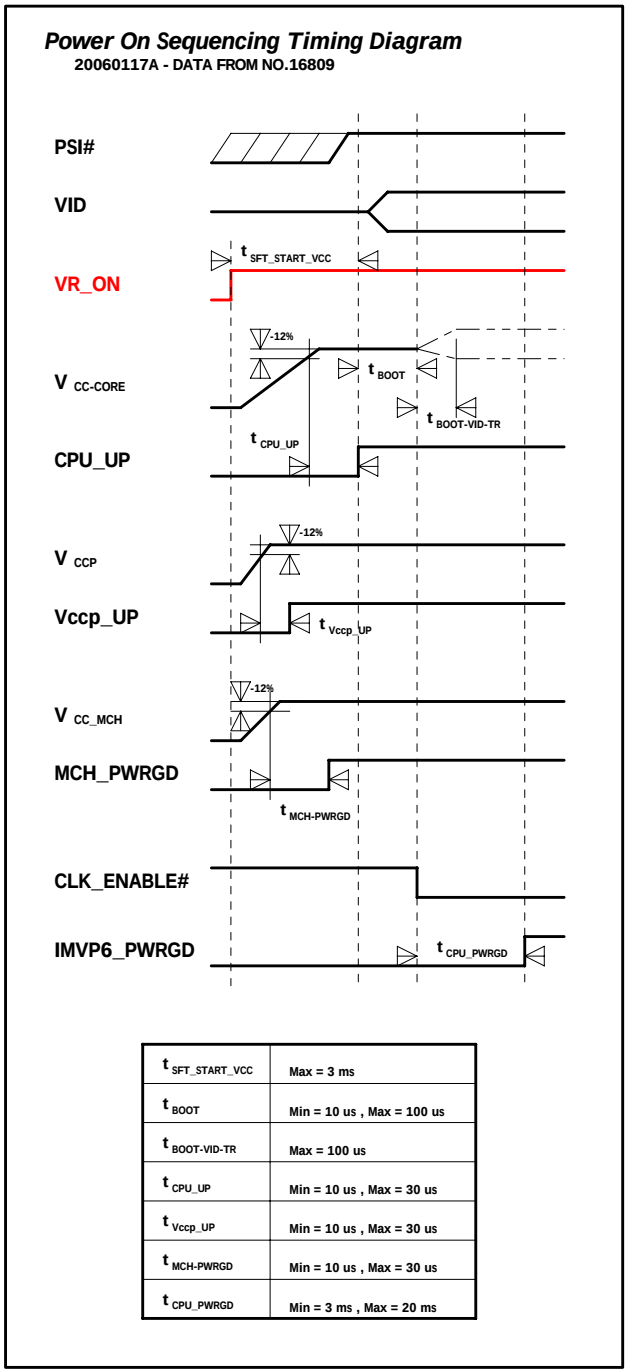
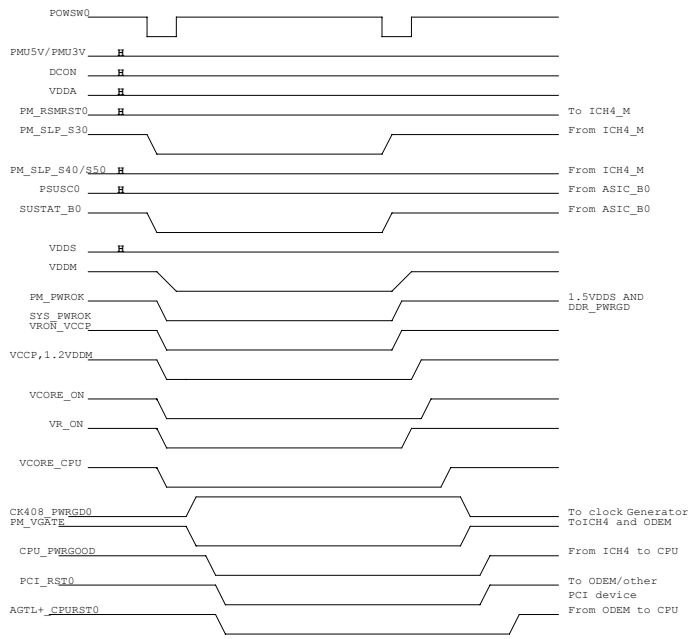
7. power on & off & S3 Sequence :

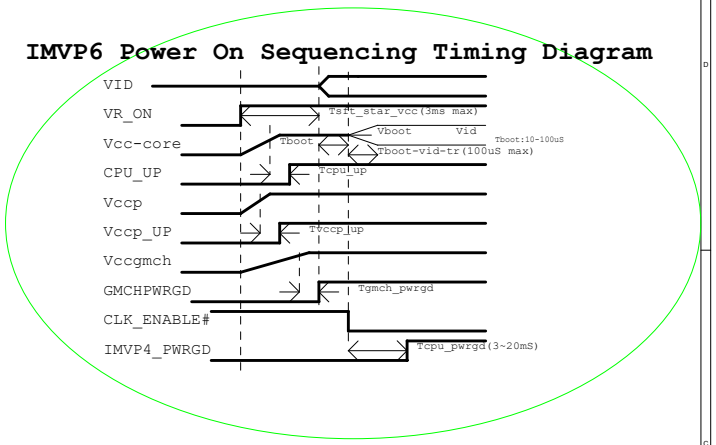


$t_{SFT\_START\_VCC}$	Max = 3 ms
t_{BOOT}	Min = 10 us , Max = 100 us
$t_{BOOT\text{-}VID\text{-}TR}$	Max = 100 us
t_{CPU_UP}	Min = 10 us , Max = 30 us
t_{Vccp_UP}	Min = 10 us , Max = 30 us
$t_{MCH\text{-}PWRGD}$	Min = 10 us , Max = 30 us
t_{CPU_PWRGD}	Min = 3 ms , Max = 20 ms

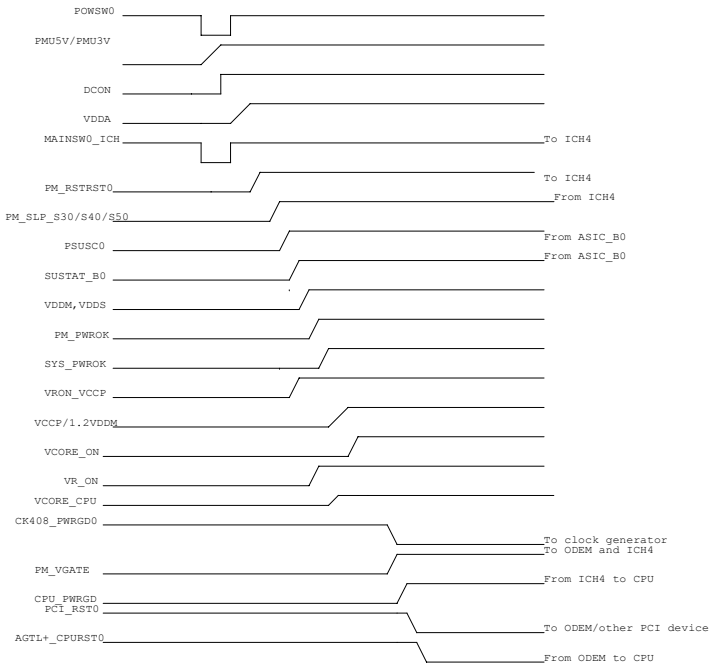
S3 SUSPEND AND RESUME TIMING



IMVP6 Power On Sequencing Timing Diagram



BATTERY ONLY POWER ON TIMING



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8. Layout Guideline :

Crestline DDRII Layout Guidelines

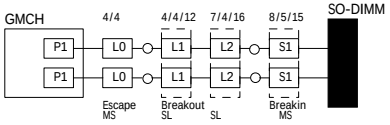
DDRII Signal Groups

Group	Signal Name
Data	SA_DQ[63..0]/SB_DQ[63..0] SA_DM[7..0]/SB_DM[7..0] SA_DQS[7..0]/SA_DQS#[7..0] SB_DQS[7..0]/SB_DQS#[7..0]
Address	SA_MA[13..0]/SB_MA[13..0] SA_BS[2..0]/SB_BS[2..0] SA_RAS#/SB_RAS# SA_CAS#/SB_CAS# SA_WE#/SB_WE#
Control	SM_CS#[3..0] SM_CKE[3..0] SM_ODT[3..0]
Clock	SM_CK[3..0] SM_CK#[3..0]
FeedBack	SA_RCVENOUT#/SB_RCVENOUT# SA_RCVENIN#/SB_RCVENIN#

Length Matching and Length Formulas

Signal Group	Minimum Length	Maximum Length
Control-to-Clock	Clock - 1.0"	Clock - 0.0"
Command-to-Clock	Clock - 1.0"	Clock + 1.0"
Strobe-to-Clock	Clock - 0.5"	Clock + 1.0"
Data-to-Strobe	Strobe - 220mils	Strobe - 180mils

CLK group : SM_CK[3..0],SM_CK#[3..0]

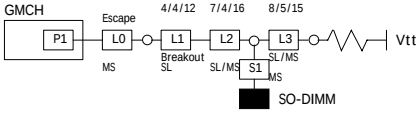


Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	42 +/- 15%
Differential Mode Impedance	70 +/- 20%
Nominal Trace Width	Inner Layer : 7 mils Outer Layer : 8 mils
Nominal CK to CK# Spacing (edge to edge)	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum Serpentine Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Spacing to Other DDR2	Inner Layer : 16 mils Outer Layer : 20 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length Range - P1	1000 mils +/- 250 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1	Min = 500 mils Max = 4000 mils
Total Length - P1 + L0 + L1 + L2 + S1	Max = 4500 mils Total Length for Channel A : X0 Total Length for Channel B : X1
Maximim Via Count	2 (Per side)
SCK to SCK# Length Matching	Match total length to within 5 mils
Clock to Clock Length Match (Total Length)	Match Channel A clocks to X0 +/- 20mils Match Channel A clocks to X1 +/- 20mils
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4/12 mils to other DDR2 Outer Layer : 5/15 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	CK to CK# spacing rule waived at connector spacing of 15 mils to other DDR2 Max. breakin length is 200 mils

Feedback group : SA_RCVENIN#],SA_RCVENOUT#,SB_RCVENIN#],SB_RCVENOUT#

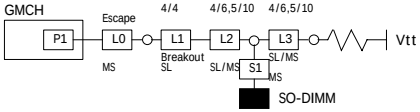
These signals are routed internally on the GMCH package and don't require any routing on the MB. As a result, can be left as NC.

Control group : SM_CKE[3..0],SM_CS#[3..0],SM_ODT[3..0]



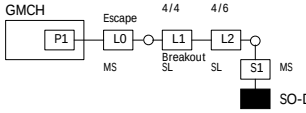
Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum CTRL Trace Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 200 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") </= CTRL </= (CLK-0.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Command group : SA_MA[13..0],SB_MA[13..0],SA_BS[2..0],SB_BS[2..0],SA_RAS#, SB_RAS#,SA_CAS#,SB_CAS#,SA_WE#,SB_WE#



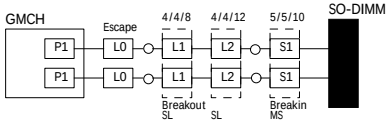
Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum CMD Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") </= CMD </= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Data group : SA_DQ[63..0],SB_DQ[63..0],SA_DM[7..0],SB_DM[7..0]



Topology	Point-to-Point
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQ Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 8 mils
Minimum Serpentine Spacing	Same as DQ-to-DQ routing
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Maximim Via Count	2
DQ/DM to DQS Length Matching (Total Length including package)	Match DQ/DM to [SDQS - 200mils] +/- 20mils, per byte lane
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Data Strobe group : SA_DQS[7..0],SA_DQS[7..0]#,SB_DQS[7..0],SB_DQS[7..0]#



Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	55 +/- 15%
Differential Mode Impedance	85 +/- 20%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Nominal DQS to DQS# Spacing (edge to edge)	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQS to DQ Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Serpentine Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length Range - P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Maximim Via Count	2 (Per side)
DQS to DQS# Length Matching	Match total length to within 5 mils
Clock to Clock Length Match (Total Length include package)	(CLK-0.5") </= DQS </= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 8 mils to other DDR2 Outer Layer : 10 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	DQS to DQS# spacing rule waived at connector spacing of 10 mils to other DDR2 Max. breakin length is 200 mils

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5FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
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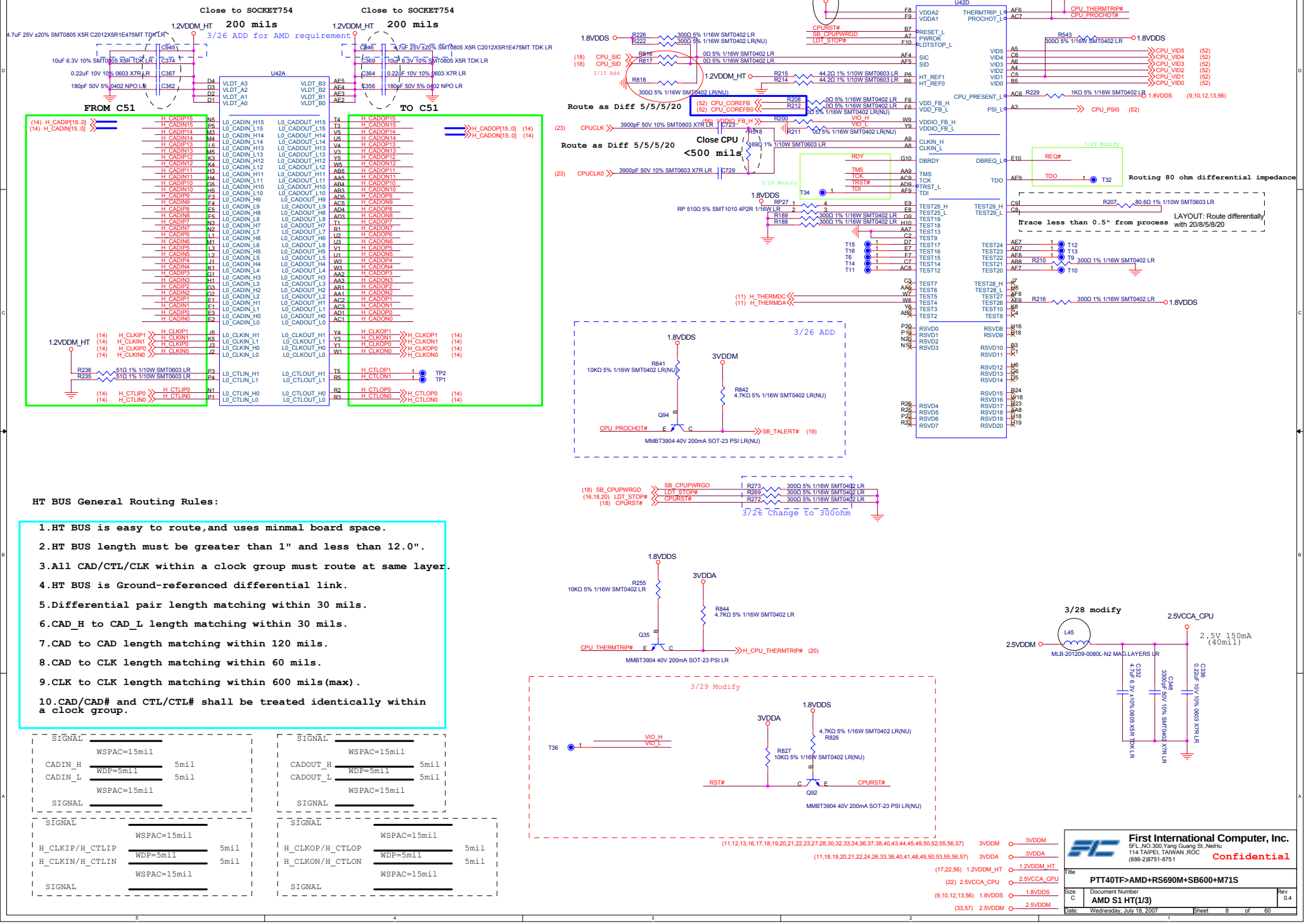
ClawHammer HT Interface



HT BUS General Routing Rules:

1. HT BUS is easy to route,and uses minmal board space.
2. HT BUS length must be greater than 1" and less than 12.0".
3. All CAD/CTL/CLK within a clock group must route at same layer.
4. HT BUS is Ground-referenced differential link.
5. Differential pair length matching within 30 mils.
6. CAD_H to CAD_L length matching within 30 mils.
7. CAD to CAD length matching within 120 mils.
8. CAD to CLK length matching within 60 mils.
9. CLK to CLK length matching within 600 mils(max).
10. CAD/CAD# and CTL/CTL# shall be treated identically within a clock group.

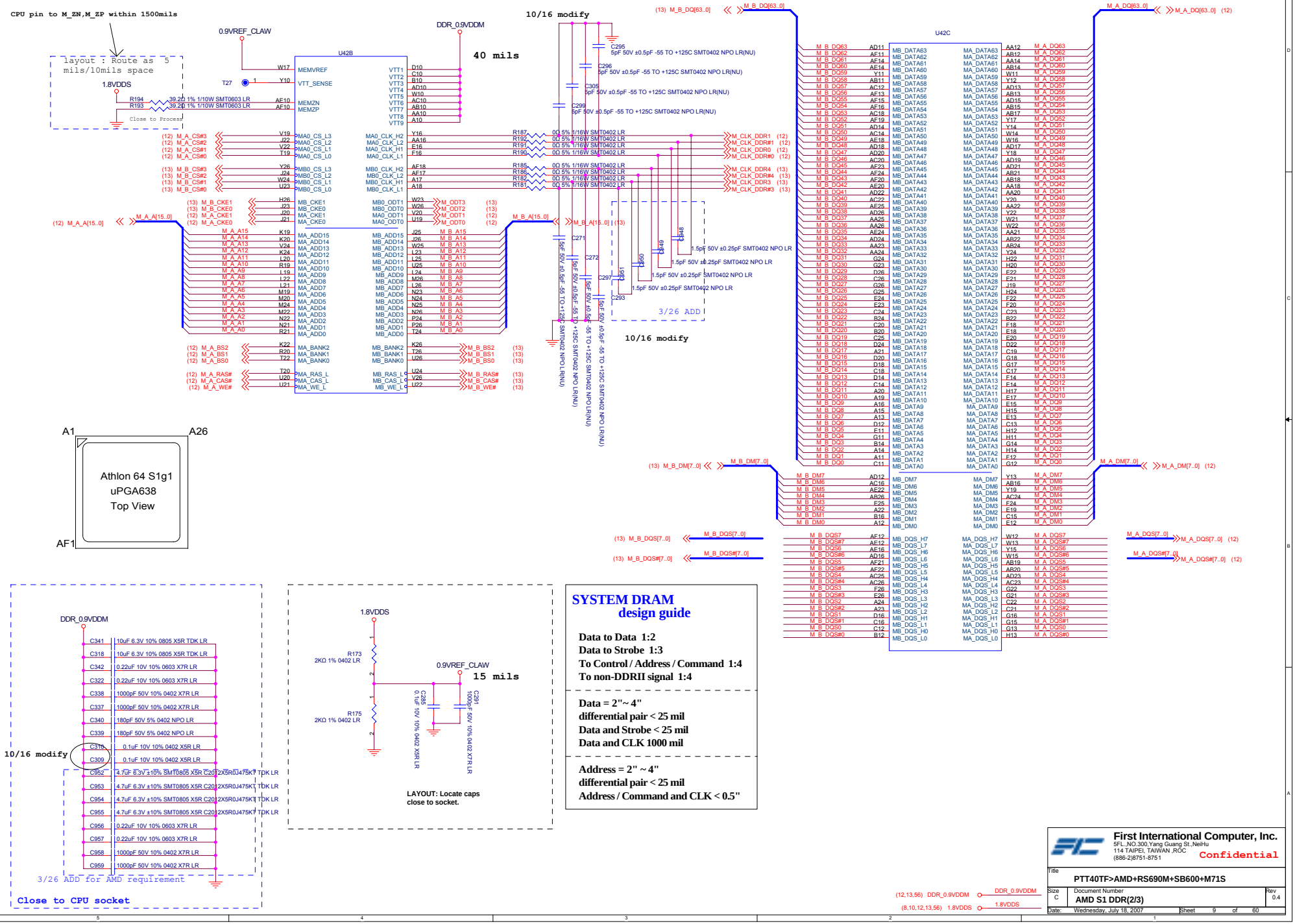
SIGNAL		
	WSPAC=15mil	
CADIN_H	WDP=5mil	5mil
CADIN_L		5mil
	WSPAC=15mil	
SIGNAL		

SIGNAL		
	WSPAC=15mil	
CADOUT_H	WDP=5mil	5mil
CADOUT_L		5mil
	WSPAC=15mil	
SIGNAL		

SIGNAL		
	WSPAC=15mil	
H_CLKIP/H_CTLIP	WDP=5mil	5mil
H_CLKIN/H_CTLIN		5mil
	WSPAC=15mil	
SIGNAL		

SIGNAL		
	WSPAC=15mil	
H_CLKOP/H_CTLOP	WDP=5mil	5mil
H_CLKON/H_CTLON		5mil
	WSPAC=15mil	
SIGNAL		

Clawhammer DDR Interface



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114 TAIPEI, TAIWAN ,ROC
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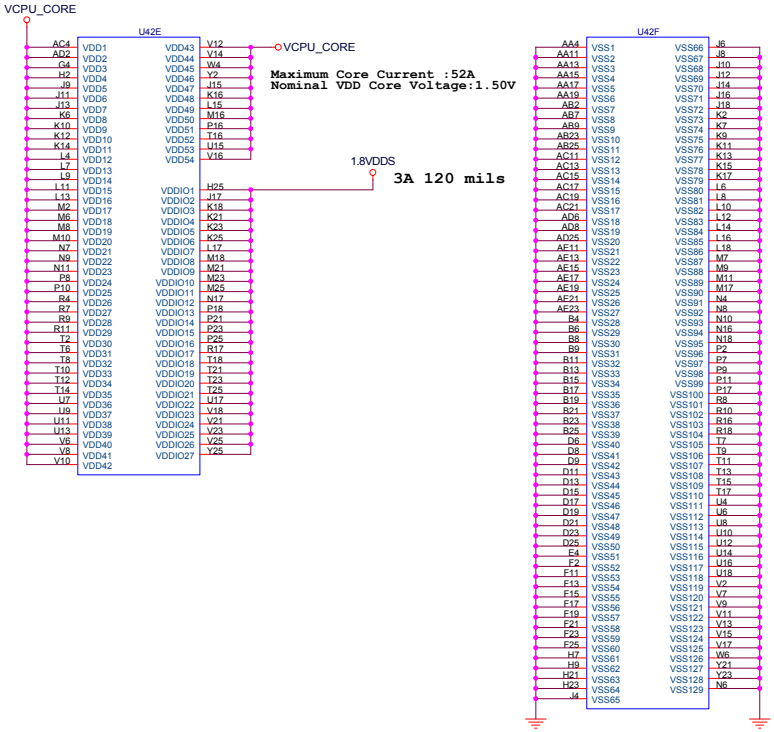

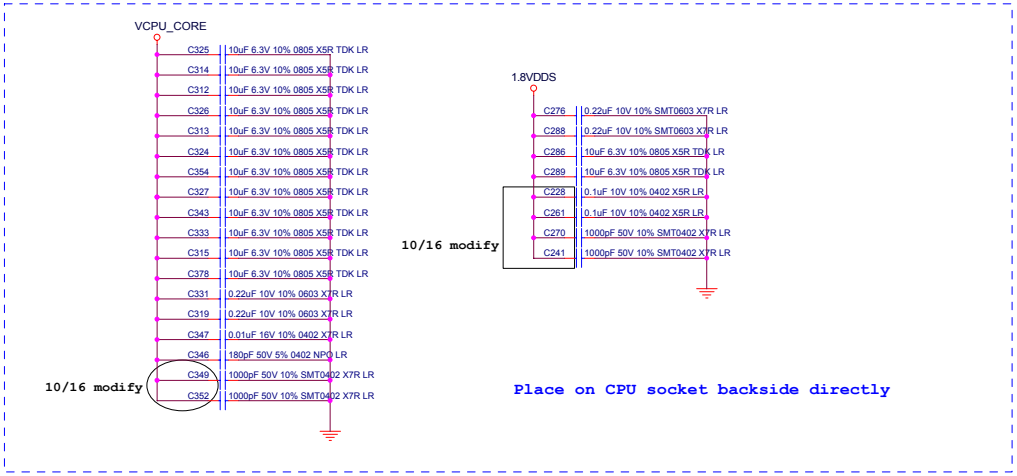

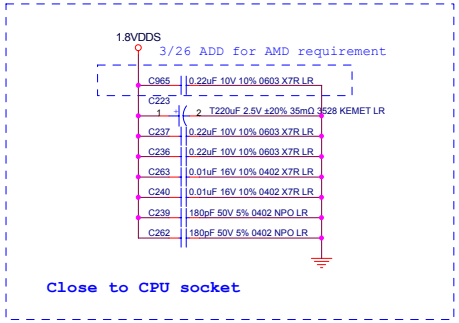

(52) VCPU_CORE — VCPU_CORE

(8,9,12,13,56) 1.8VDDS — 1.8VDDS

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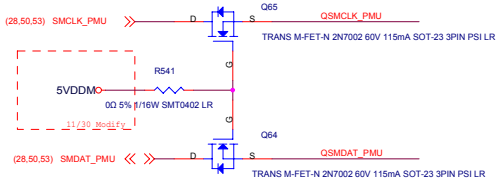
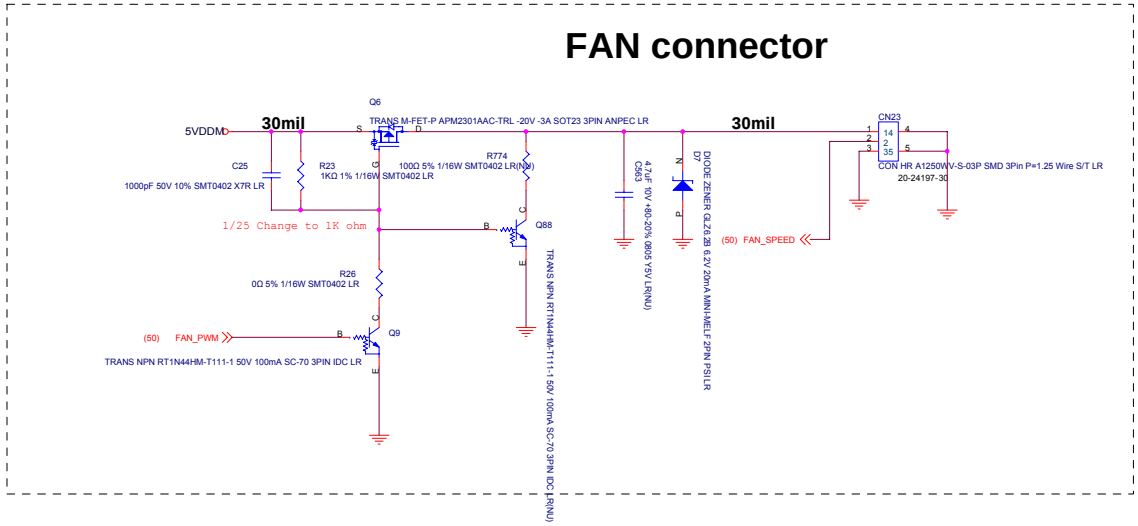
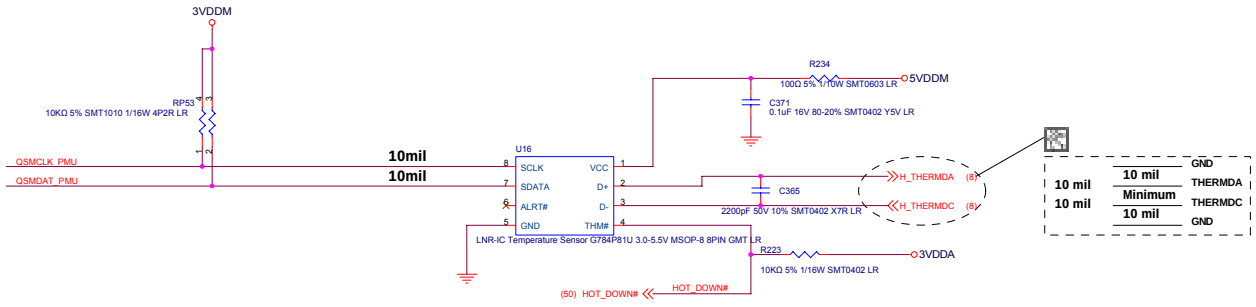
FAN Power Control



FAN connector



THERMAL SENSOR



(8,12,13,16,17,18,19,20,21,22,23,27,28,30,32,33,34,36,37,38,40,43,44,45,49,50,52,55,56,57) 3VDDM 3VDDM
(8,18,19,20,21,22,24,26,33,36,40,41,48,49,50,53,55,56,57) 3VDDA 3VDDA
(16,21,32,34,35,36,37,46,47,55,56) 5VDDM 5VDDM

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5FL.,NO.300,Yang Guang St.,NeiHu
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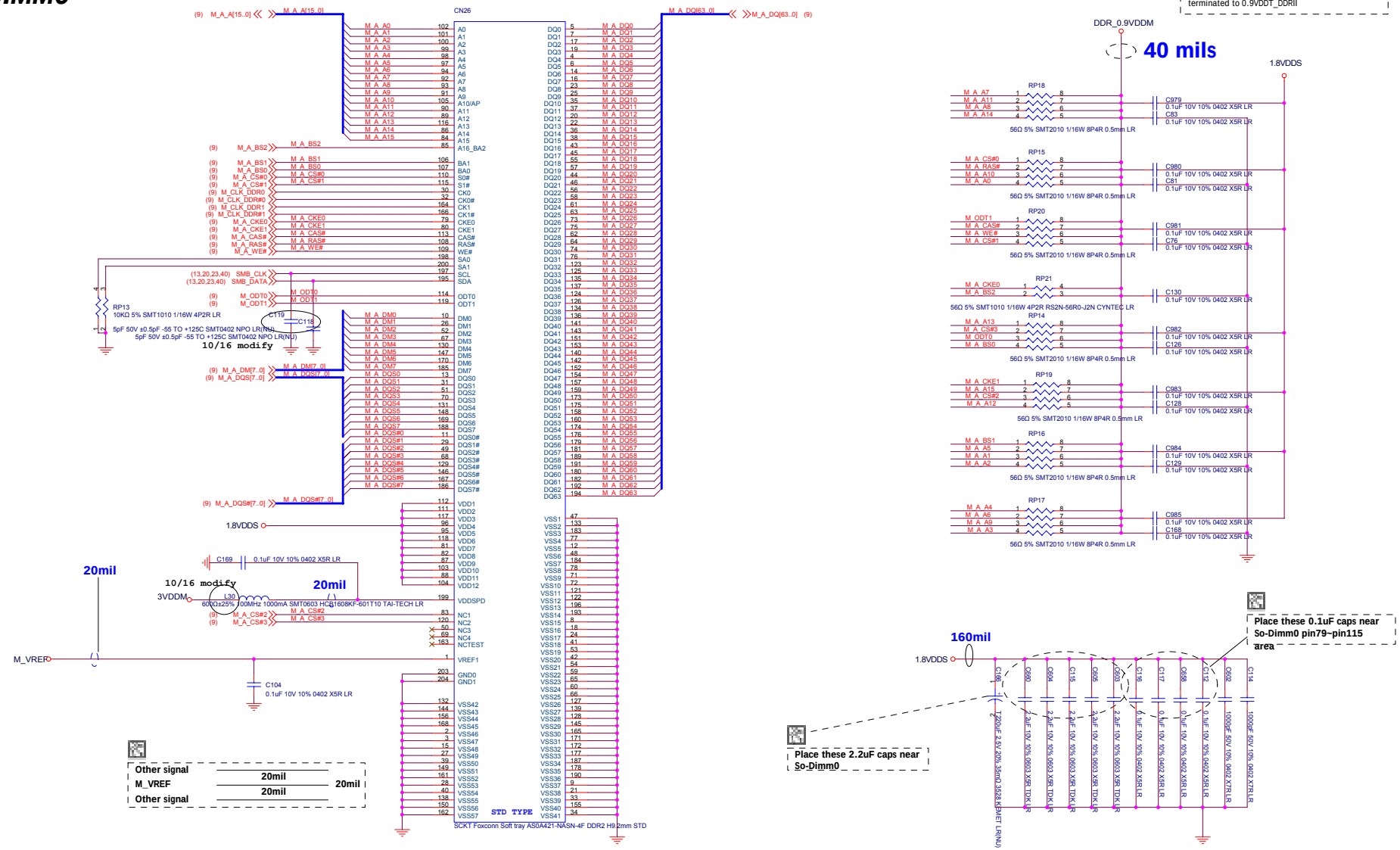
SO-DIMM0



(13,56) M_VREF	M_VREF	
(9,13,56) DDR_0.9VDDM	DDR_0.9VDDM	
(8,9,10,13,56) 1.8VDDS	1.8VDDS	
(8,11,13,16,17,18,19,20,21,22,23,27,28,30,32,33,34,36,37,38,40,43,44,45,49,50,52,55,56,57) 3VDDM	3VDDM	

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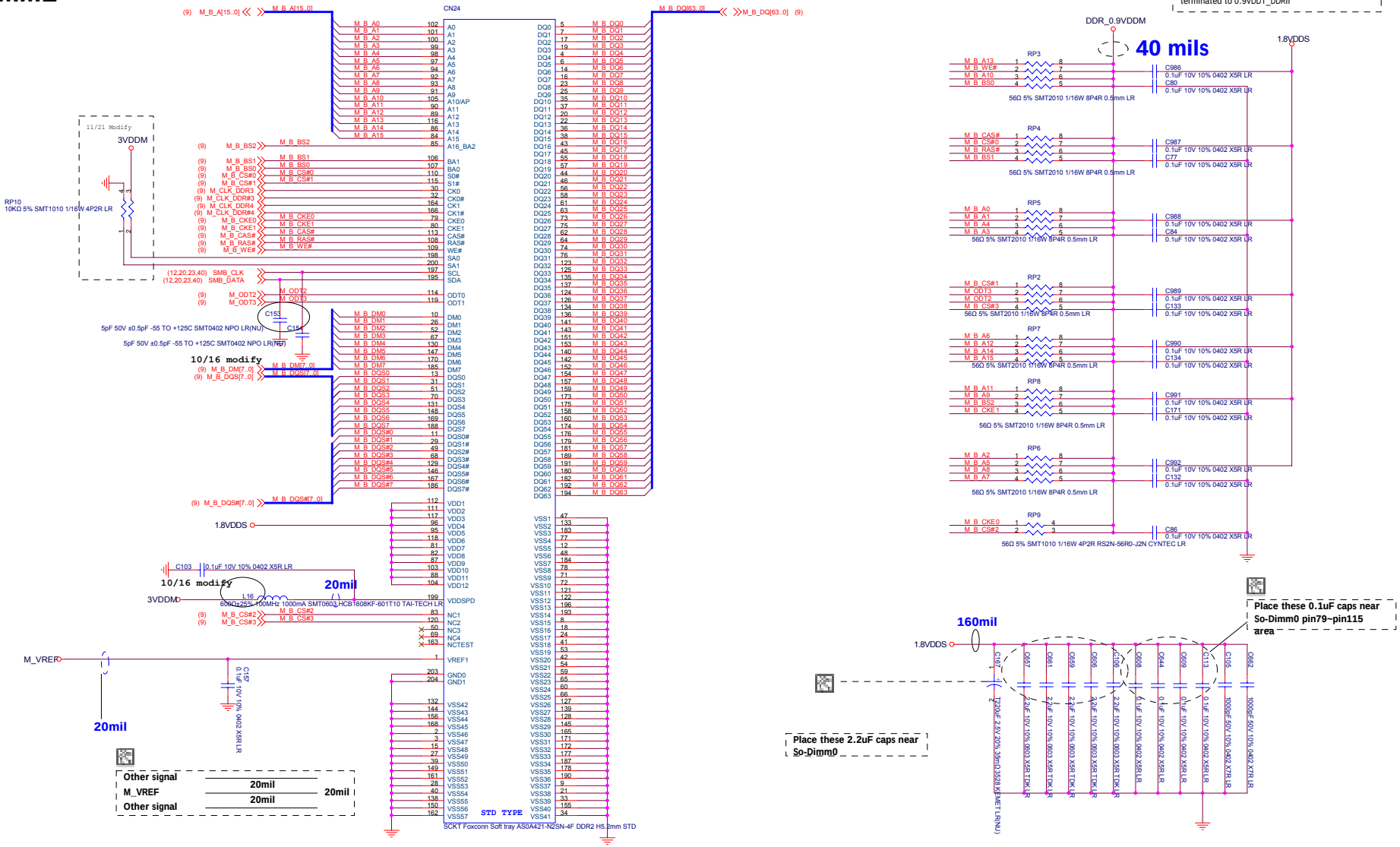
Size: C | Document Number: DDR2 SDRAM SO-DIMM0 | Rev: 0.4

Date: Wednesday, July 18, 2007 | Sheet 12 of 60

SO-DIMM1



(12,56) M_VREF	M_VREF	
(9,12,56) DDR_0.9VDDM	DDR_0.9VDDM	
(8,9,10,12,56) 1.8VDDS	1.8VDDS	
(8,11,12,16,17,18,19,20,21,22,23,27,28,30,32,33,34,36,37,38,40,43,44,45,49,50,52,55,56,57) 3VDDM	3VDDM	

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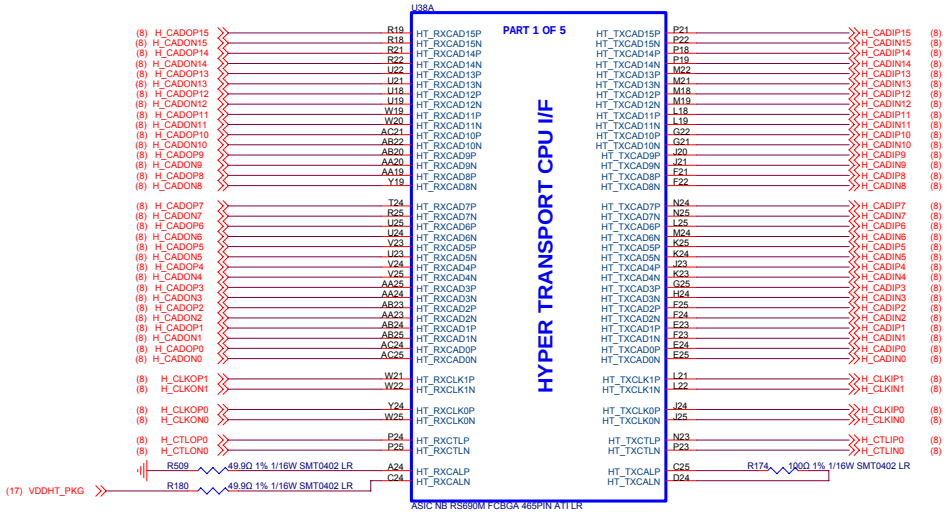
Title	PTT40TF>AMD+RS690M+SB600+M71S
Size C	Document Number: DDR2 SDRAM SO-DIMM1
Rev	0.4
Date: Wednesday, July 18, 2007	Sheet 13 of 60



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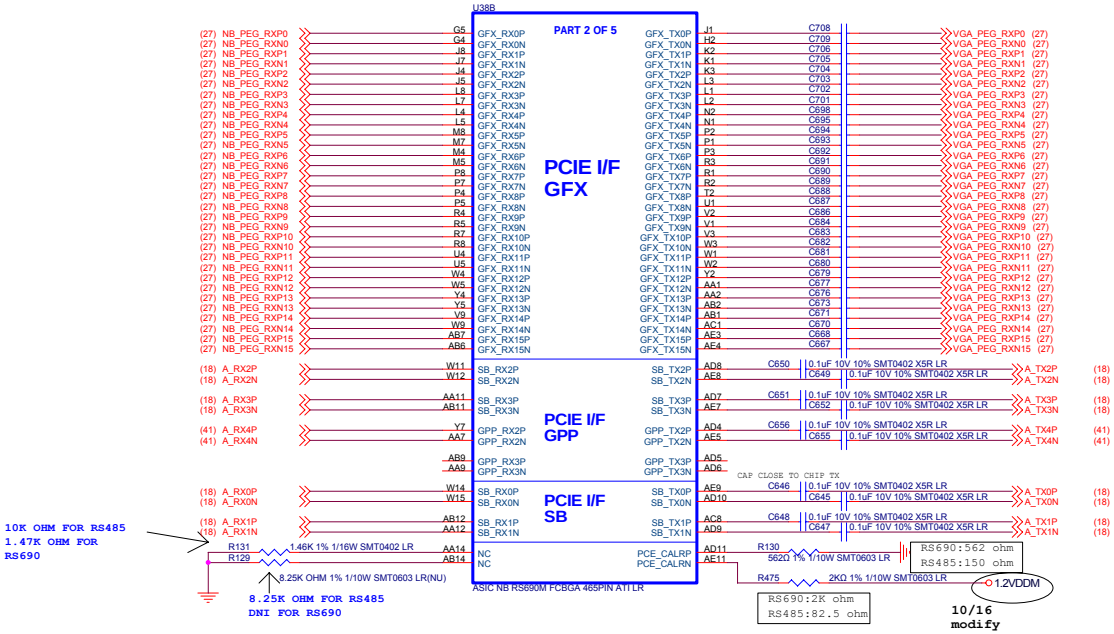
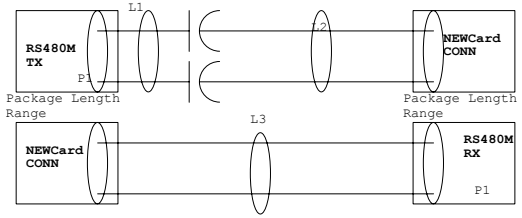
Title: **PTT40TF>AMD+RS690M+SB600+M71S**

Size	Document Number	Rev
C	**RS690M_HT (1/4)**	0.4

Date: Wednesday, July 18, 2007 Sheet 14 of 60





L1	L2	L3	Cap
Min 0.25" Max 14.75"	Max 14.75" - L1	Min 0.25" Max 15"	75nF ~200nF +/-20% 0402 or 0603

(16,17,18,19,21,56,57) 1.2VDDM 1.2VDDM

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Title: PTT40TF>AMD+RS690M+SB600+M71S

Size	Document Number	Rev
C	RS690M_PCIE (2/4)	0.4

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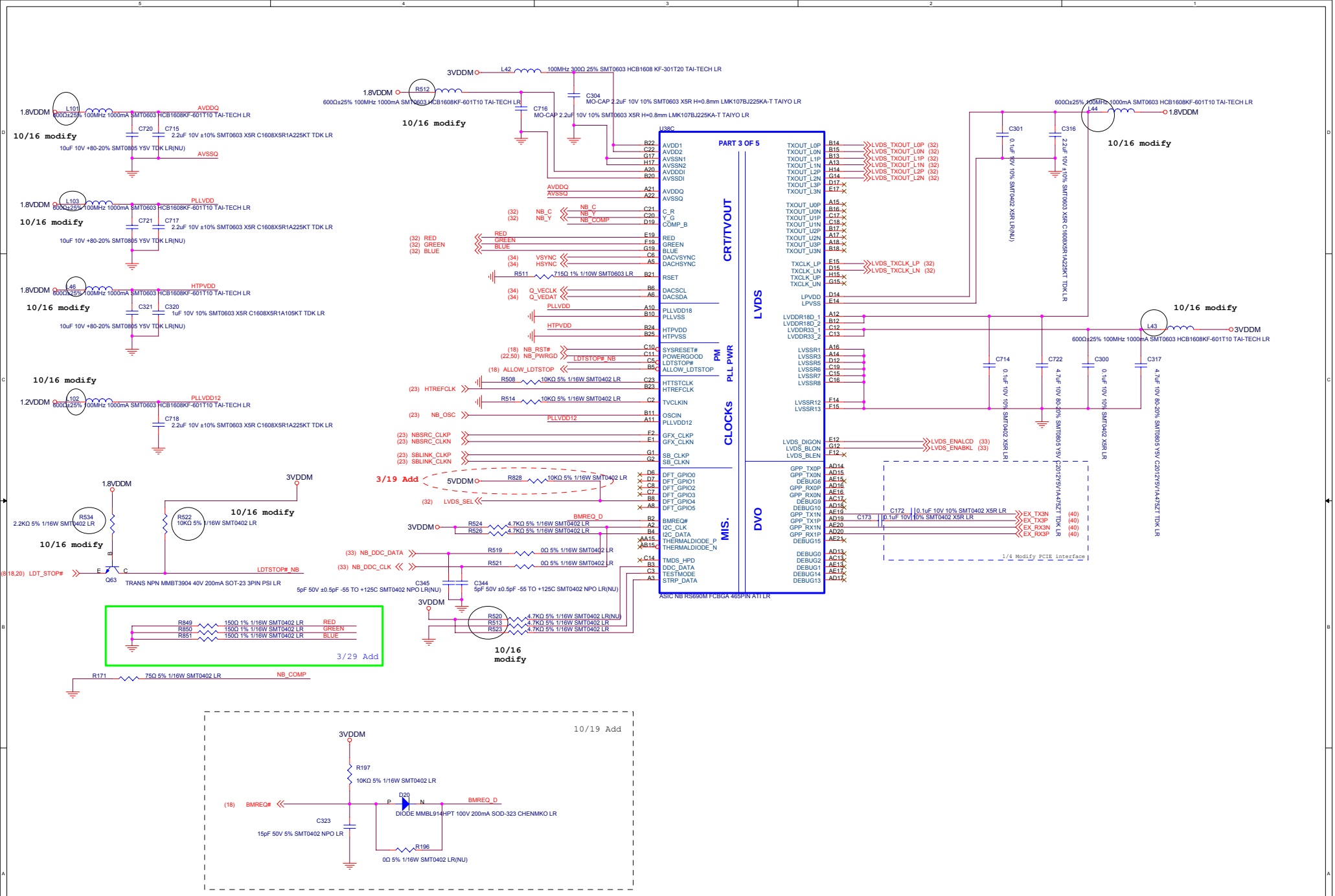

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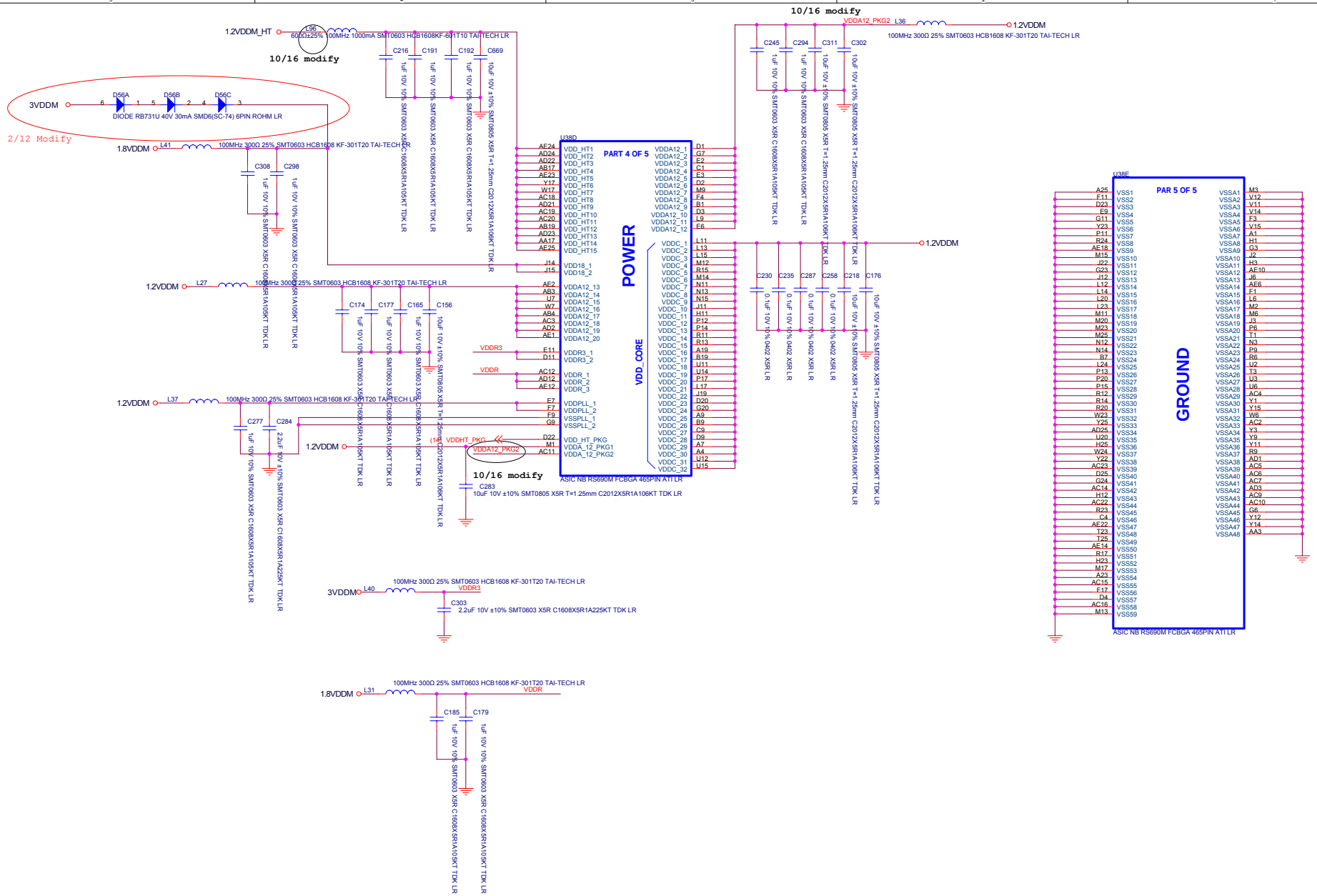
Size: C | Document Number: RS690M_VIDEO (3/4) | Rev: 0.4

Date: Wednesday, July 18, 2007 | Sheet 16 of 60



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Size	Document Number	Rev
C	RS690M_POWER (4/4)	0.4

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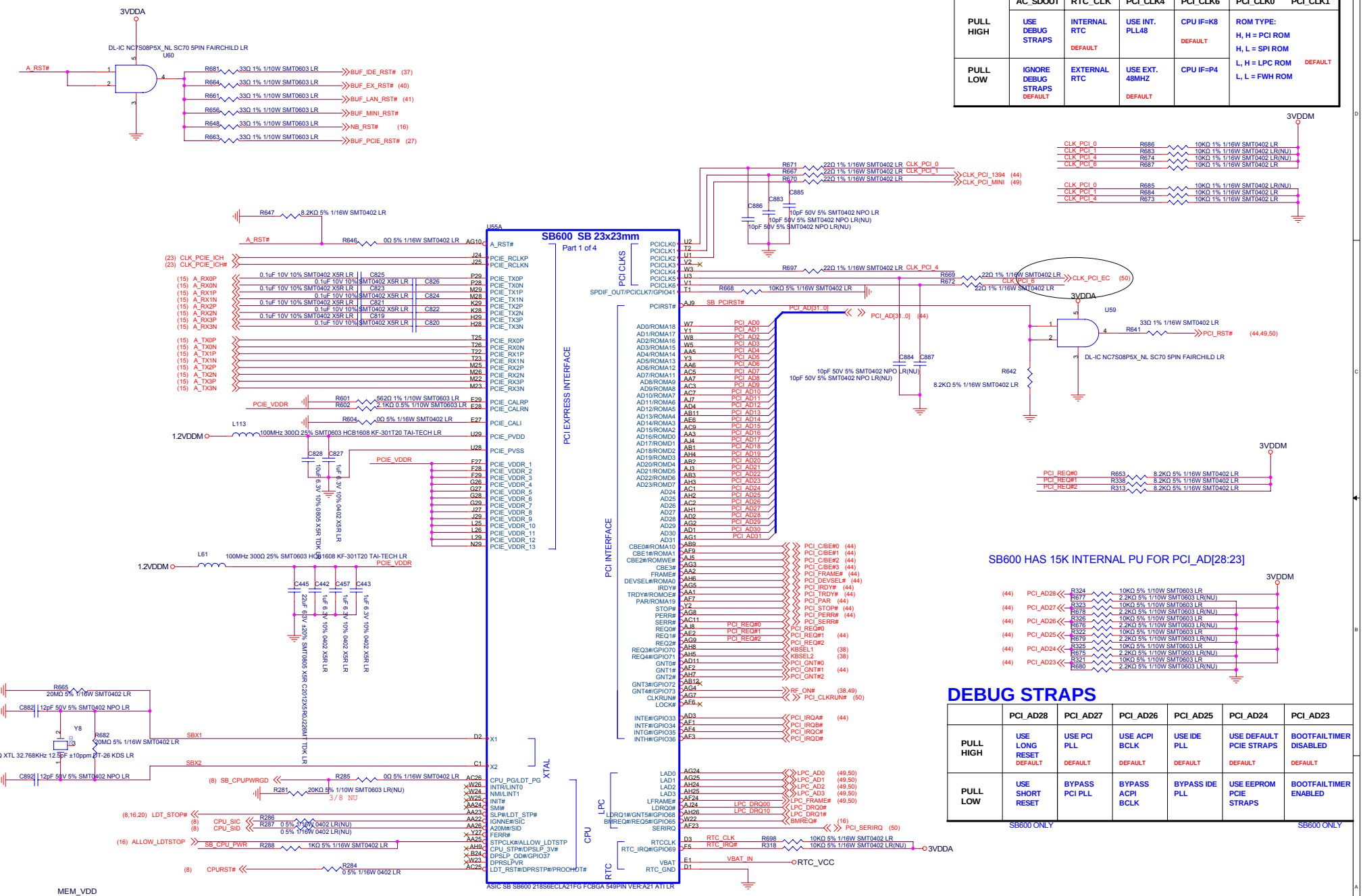
	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	



DEBUG STRAPS

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

SB600 ONLY SB600 ONLY

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Size: C | Document Number: SB600 PCI/LPC (1/4) | Rev: 0.4

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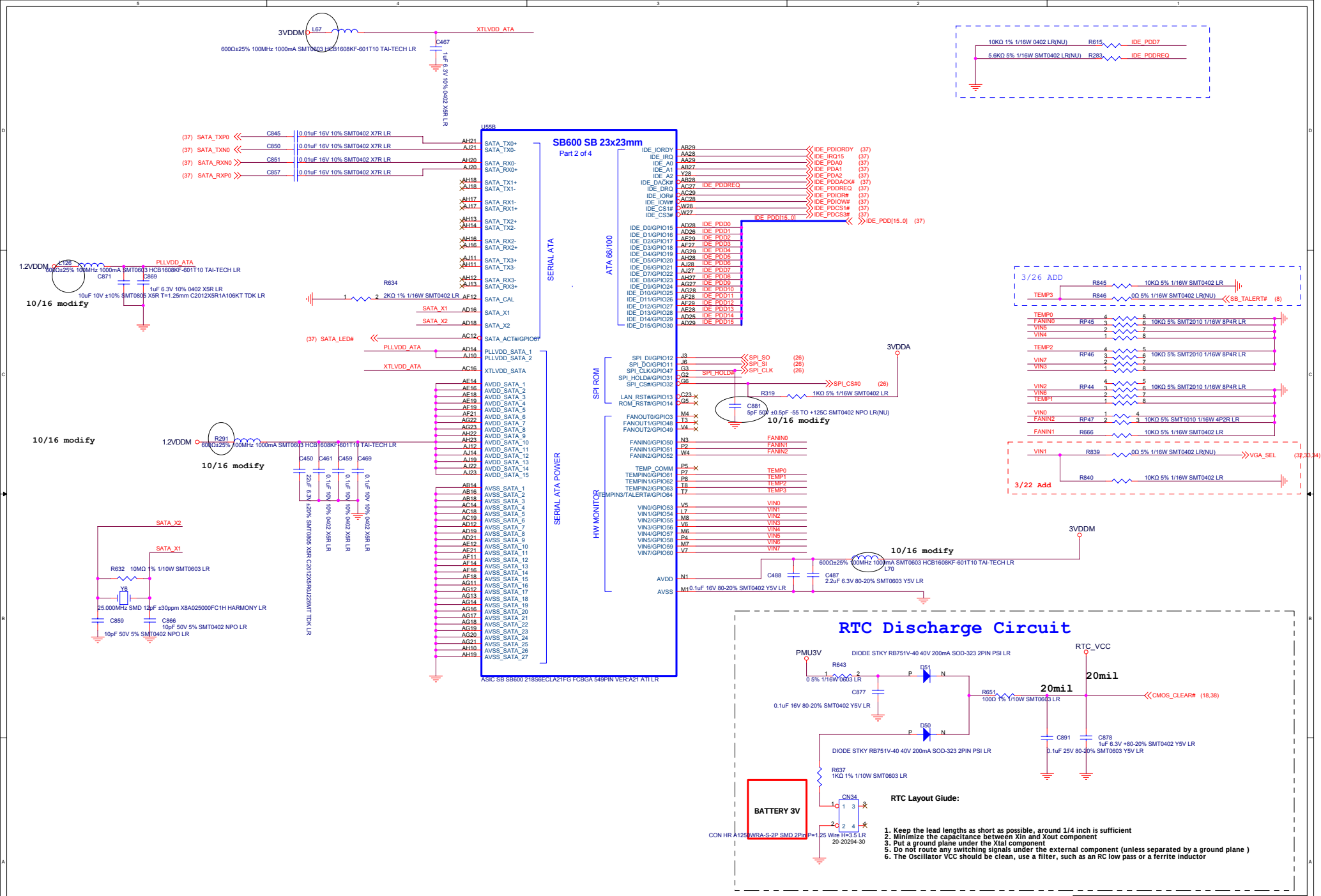
SB600 SB 23x23mm
Part 2 of 4
U55B
SERIAL ATA
ATA 66/100
SPI ROM
HW MONITOR
SERIAL ATA POWER
ASIC SB SB600 218S6ECLA21FG FCBGA 549PIN VER:A21 ATI LR
3/26 ADD
3/22 Add
10/16 modify
RTC Discharge Circuit
PMU3V
RTC_VCC
BATTERY 3V
CN34
RTC Layout Giude:
1. Keep the lead lengths as short as possible, around 1/4 inch is sufficient
2. Minimize the capacitance between Xin and Xout component
3. Put a ground plane under the Xtal component
5. Do not route any switching signals under the external component (unless separated by a ground plane)
6. The Oscillator VCC should be clean, use a filter, such as an RC low pass or a ferrite inductor
3VDDA
3VDDM
1.2VDDM
PLLVDD_ATA
XTLVDD_ATA
SATA_X1
SATA_X2
SATA_LED#
SATA_TXP0
SATA_TXN0
SATA_RXN0
SATA_RXP0
SATA_CAL
SATA_ACT#/GPIO67
IDE_PDD[15..0]
IDE_PDD[15..0] (37)
IDE_PDDREQ
IDE_PDIORDY (37)
IDE_IRQ15 (37)
IDE_PDA0 (37)
IDE_PDA1 (37)
IDE_PDA2 (37)
IDE_PDDACK# (37)
IDE_PDDREQ (37)
IDE_PDIOR# (37)
IDE_PDIOW# (37)
IDE_PDCS1# (37)
IDE_PDCS3# (37)
SPI_SO (26)
SPI_SI (26)
SPI_CLK (26)
SPI_CS#0 (26)
SPI_HOLD#
TEMP0
TEMP1
TEMP2
TEMP3
VIN0
VIN1
VIN2
VIN3
VIN4
VIN5
VIN6
VIN7
FANIN0
FANIN1
FANIN2
SB_TALERT# (8)
VGA_SEL (32,33,34)
CMOS_CLEAR# (18,38)
10KΩ 1% 1/16W 0402 LR(NU) R615 IDE_PDD7
5.6KΩ 5% 1/16W SMT0402 LR(NU) R283 IDE_PDDREQ
10KΩ 5% 1/16W SMT0402 LR
0Ω 5% 1/16W SMT0402 LR(NU)
10KΩ 5% SMT2010 1/16W 8P4R LR
10KΩ 5% SMT1010 1/16W 4P2R LR
600Ω±25% 100MHz 1000mA SMT0603 HCB1608KF-601T10 TAI-TECH LR
10uF 6.3V 10% 0402 X5R LR
1uF 6.3V 10% 0402 X5R LR
0.01uF 16V 10% SMT0402 X7R LR
2KΩ 1% 1/16W SMT0402 LR
1KΩ 5% 1/16W SMT0402 LR
5pF 50V ±0.5pF -55 TO +125C SMT0402 NPO LR(NU)
2.2uF 6.3V 80-20% SMT0603 Y5V LR
0.1uF 16V 80-20% SMT0402 Y5V LR
DIODE STKY RB751V-40 40V 200mA SOD-323 2PIN PSI LR
0 5% 1/16W 0603 LR
100Ω 1% 1/10W SMT0603 LR
0.1uF 25V 80-20% SMT0603 Y5V LR
1uF 6.3V +80-20% SMT0402 Y5V LR
1KΩ 1% 1/10W SMT0603 LR
CON HR A1250WRA-S-2P SMD 2Pin P=1.25 Wire H=3.5 LR 20-20294-30
10uF 10V ±10% SMT0805 X5R T=1.25mm C2012X5R1A106KT TDK LR
22uF 6.3V ±20% SMT0805 X5R C2012X5R0J226MT TDK LR
10MΩ 1% 1/10W SMT0603 LR
25.000MHz SMD 12pF ±30ppm X8A025000FC1H HARMONY LR
10pF 50V 5% SMT0402 NPO LR
10pF 50V 5% SMT0402 NPO LR
(8,11,18,20,21,22,24,26,33,36,40,41,48,49,50,53,55,56,57) 3VDDA
(18,38) RTC_VCC
(50,53,55) PMU3V
(15,16,17,18,21,56,57) 1.2VDDM
(8,11,12,13,16,17,18,20,21,22,23,27,28,30,32,33,34,36,37,38,40,43,44,45,49,50,52,55,56,57) 3VDDM
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Title
PTT40TF>AMD+RS690M+SB600+M71S
Size C
Document Number
SB600 SATA/PATA (2/4)
Rev 0.4
Date: Wednesday, July 18, 2007
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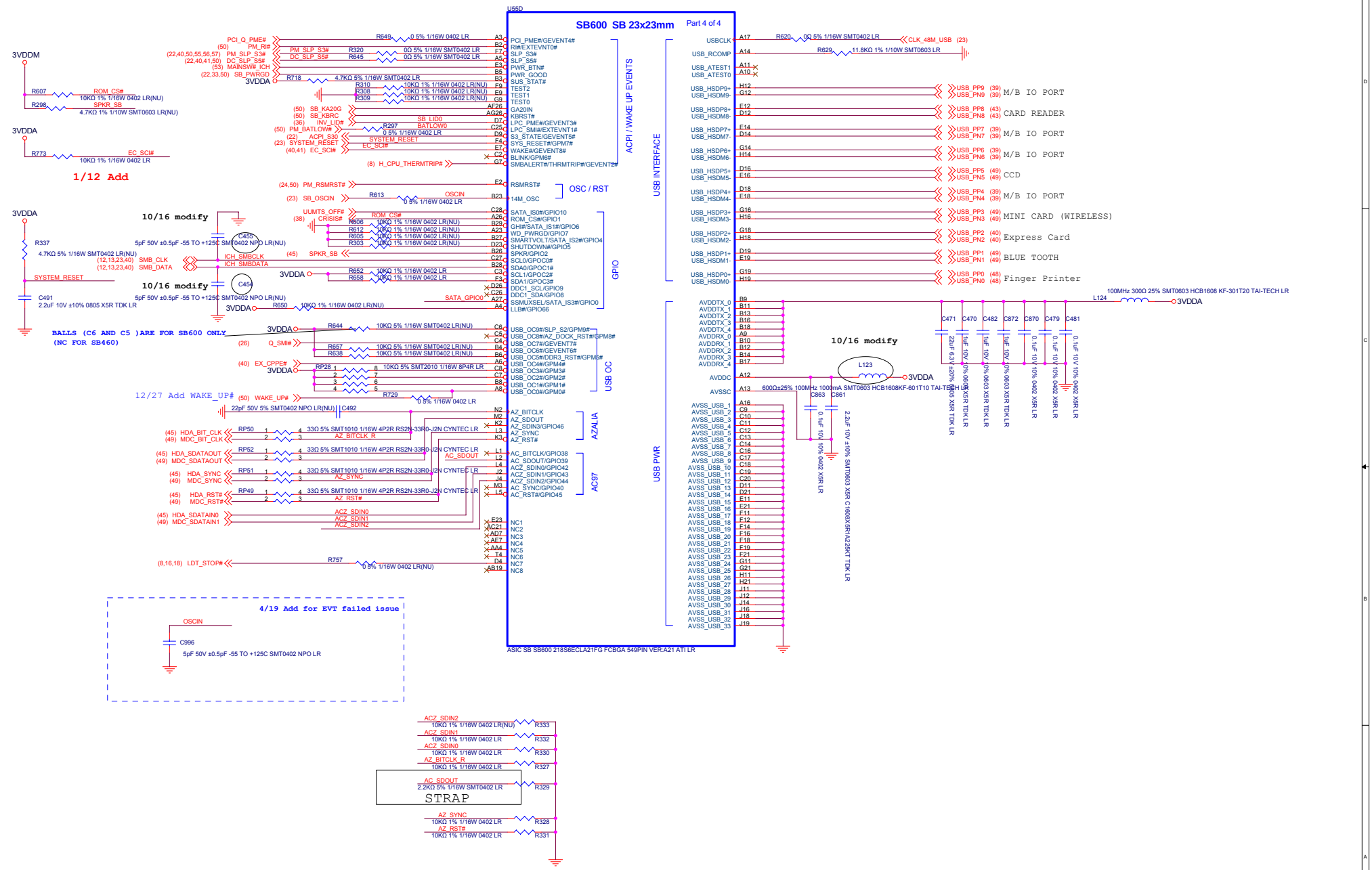

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Size: C | Document Number: SB600 USB/AZALIA (3/4) | Rev: 0.4

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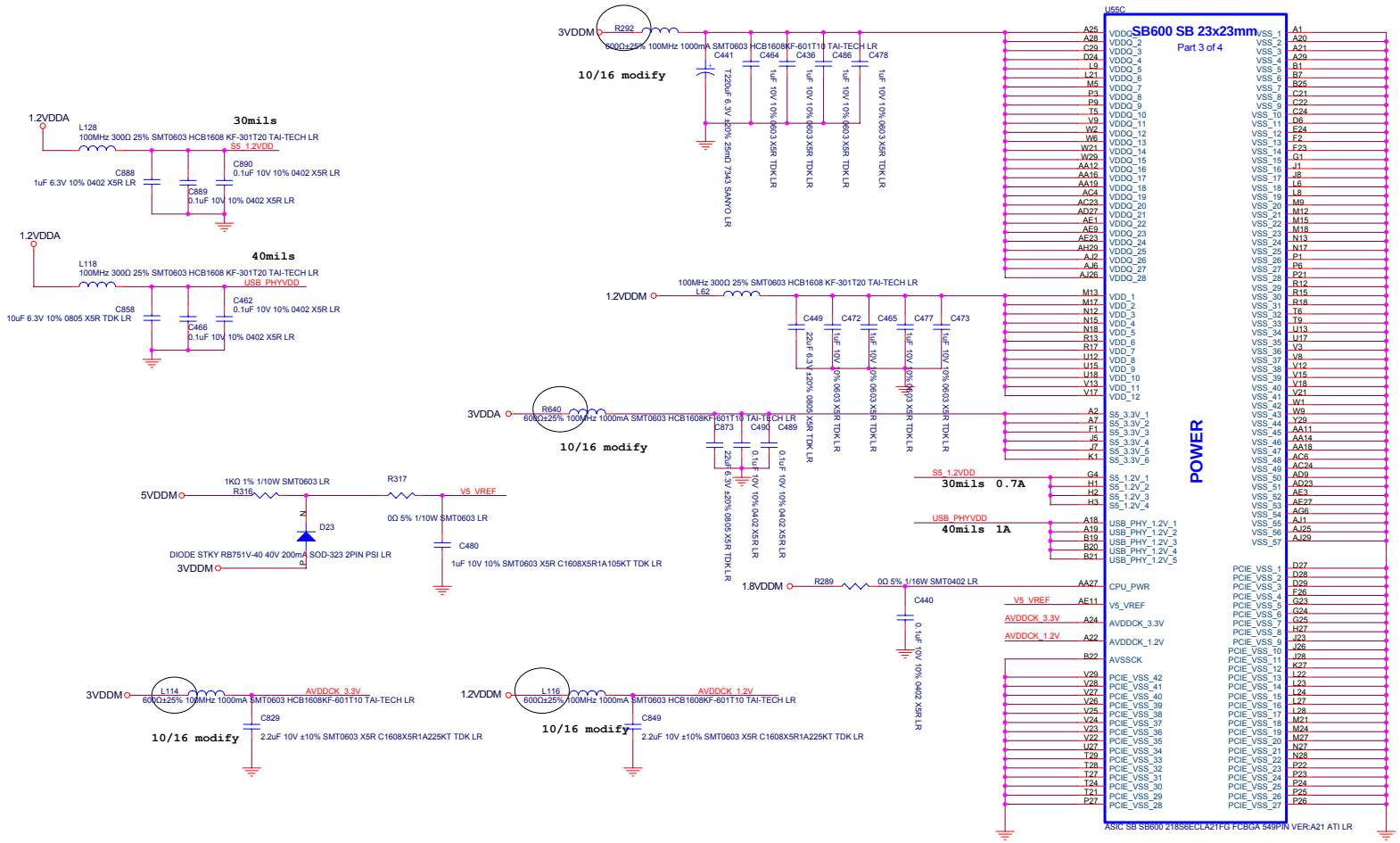

(8,11,18,19,20,22,24,26,33,36,40,41,48,49,50,53,55,56,57) 3VDDA — 3VDDA
(16,17,32,57) 1.8VDDM — 1.8VDDM
(57) 1.2VDDA — 1.2VDDA
(15,16,17,18,19,56,57) 1.2VDDM — 1.2VDDM
(11,16,32,34,35,36,37,46,47,55,56) 5VDDM — 5VDDM
(8,11,12,13,16,17,18,19,20,22,23,27,28,30,32,33,34,36,37,38,40,43,44,45,49,50,52,55,56,57) 3VDDM — 3VDDM

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Size	Document Number	Rev
C	SB600 POWER (4/4)	0.4

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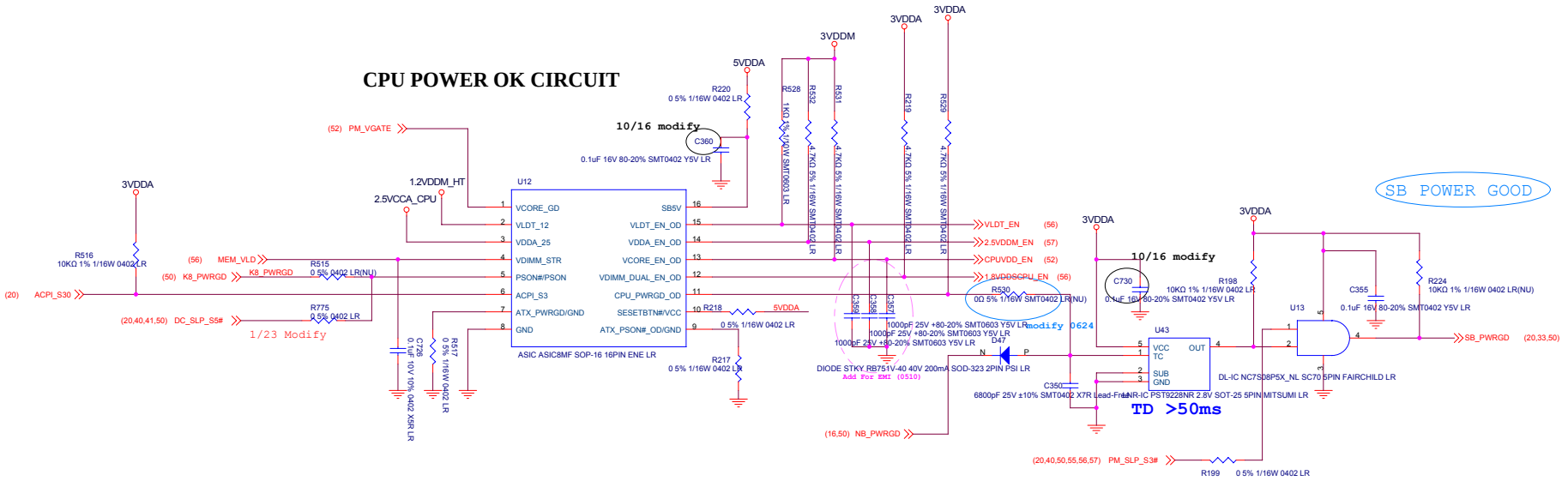
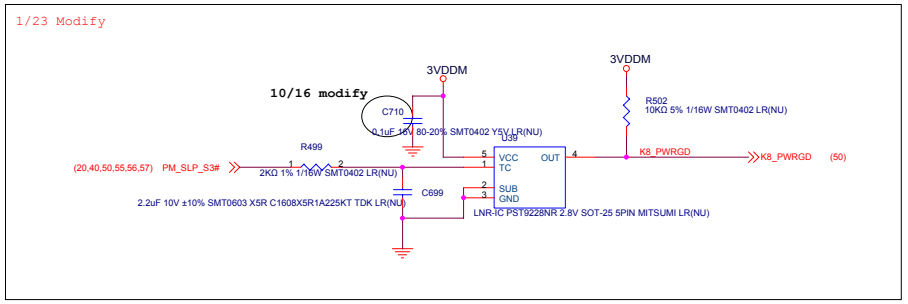
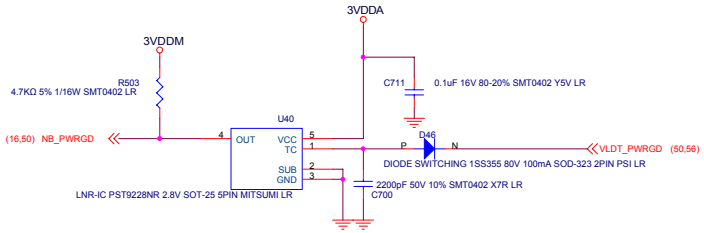
CPU POWER OK CIRCUIT







(38,39,49,52,55,56,57) 5VDDA — 5VDDA
(8,17,56) 1.2VDDM_HT — 1.2VDDM_HT
(8) 2.5VCCA_CPU — 2.5VCCA_CPU
(8,11,12,13,16,17,18,19,20,21,23,27,28,30,32,33,34,36,37,38,40,43,44,45,49,50,52,55,56,57) 3VDDM — 3VDDM
(8,11,18,19,20,21,24,26,33,36,40,41,48,49,50,53,55,56,57) 3VDDA — 3VDDA

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Size	Document Number	Rev
C	CPU Power OK / NB PWRGD	0.4

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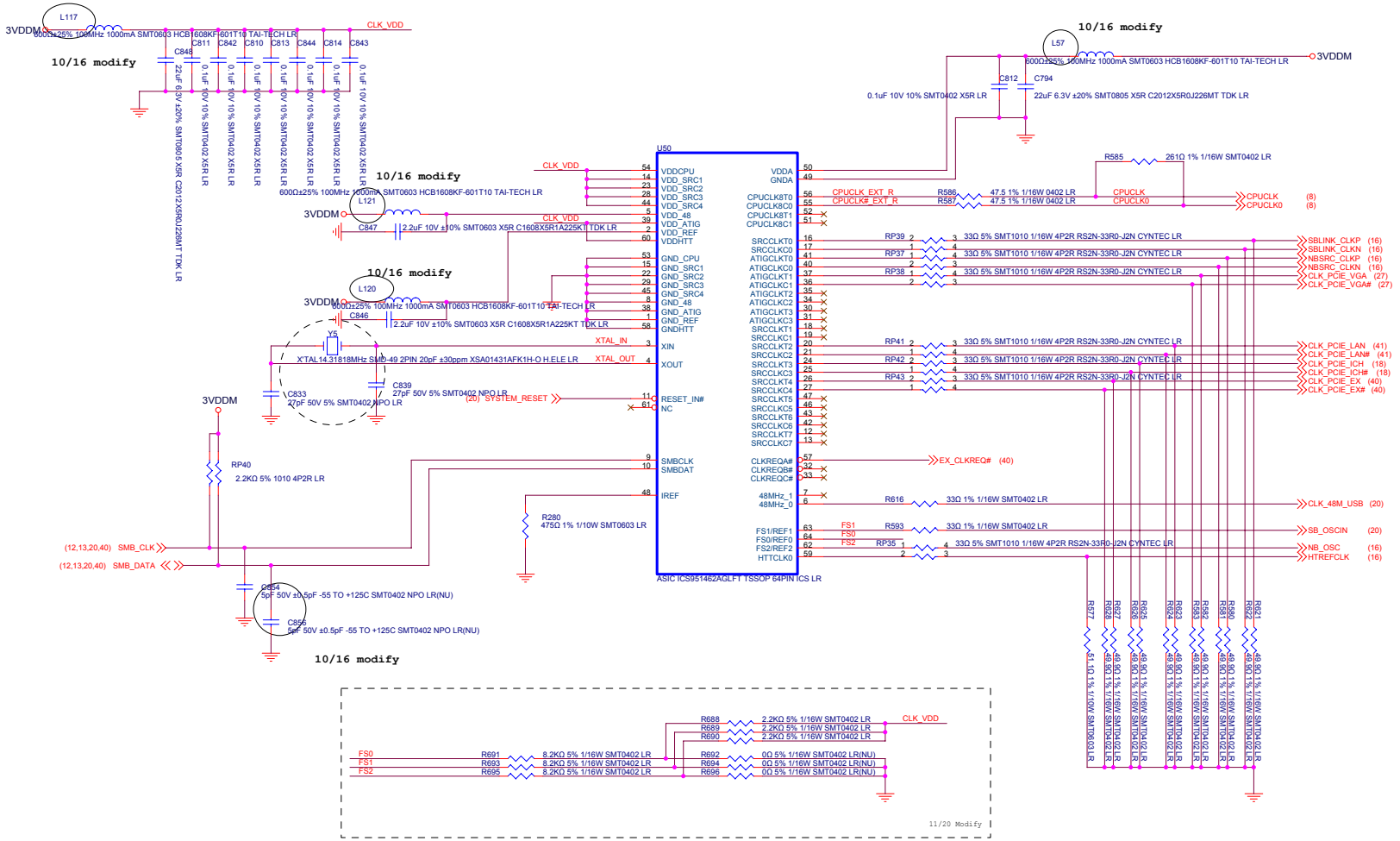

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

(8,11,12,13,16,17,18,19,20,21,22,27,28,30,32,33,34,36,37,38,40,43,44,45,49,50,52,55,56,57) 3VDDM 3VDDM

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Size: C | Document Number: CLOCK GENERATOR | Rev: 0.4

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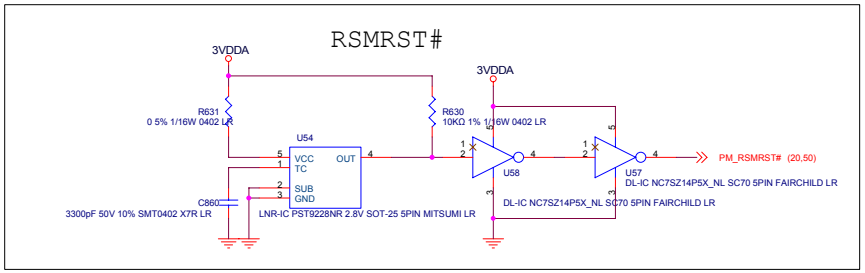
RESUME RESET



(8,11,18,19,20,21,22,26,33,36,40,41,48,49,50,53,55,56,57) 3VDDA 3VDDA

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Title	PTT40TF>AMD+RS690M+SB600+M71S	
Size C	Document Number **Reset Circuit**	Rev 0.4
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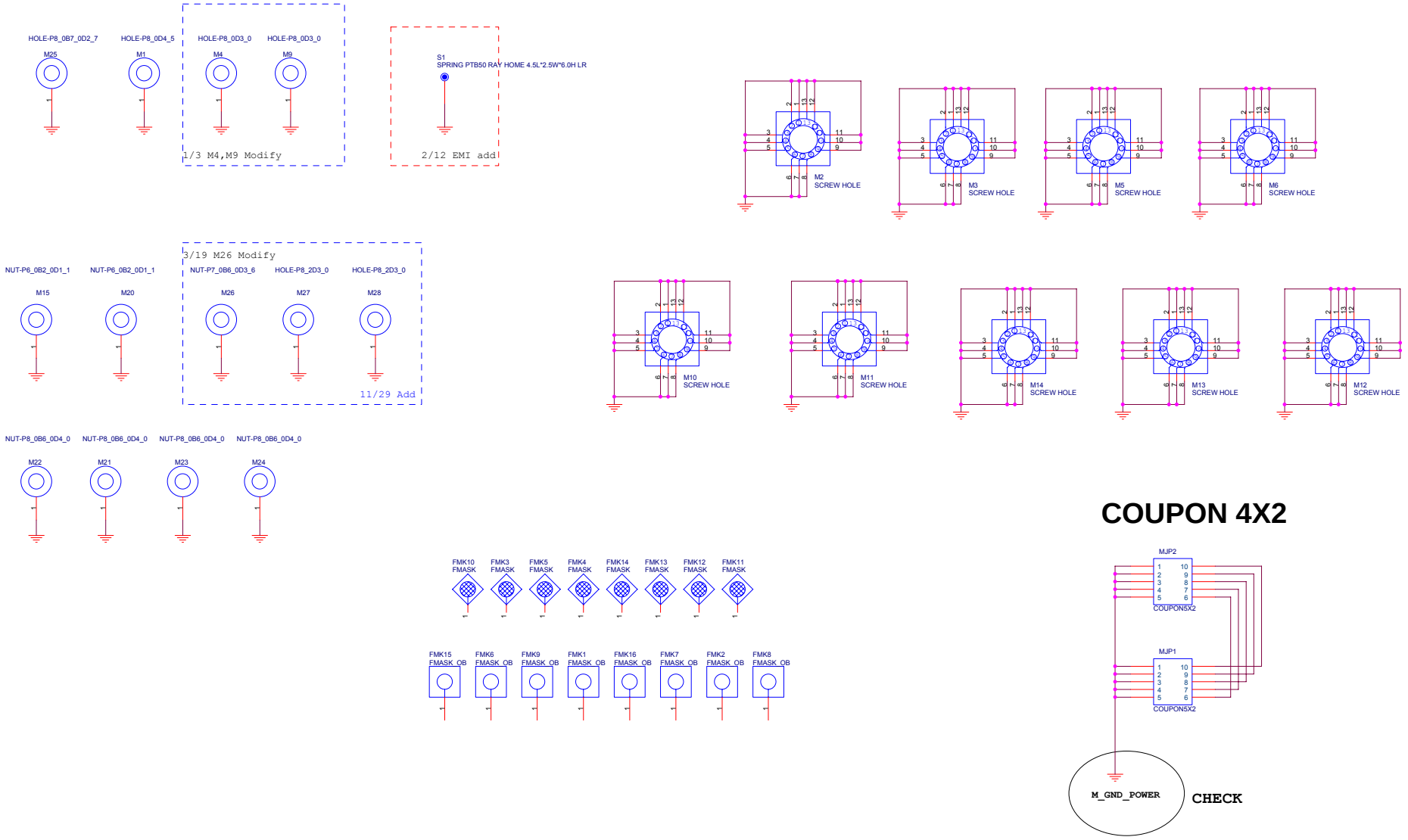

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Title	PTT40TF>AMD+RS690M+SB600+M71S
Size C	Document Number: Screw Hole
Rev	0.4
Date:	Wednesday, July 18, 2007
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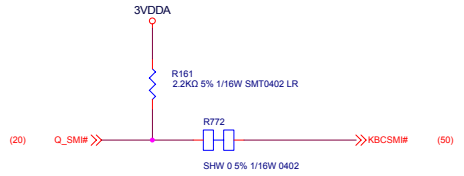
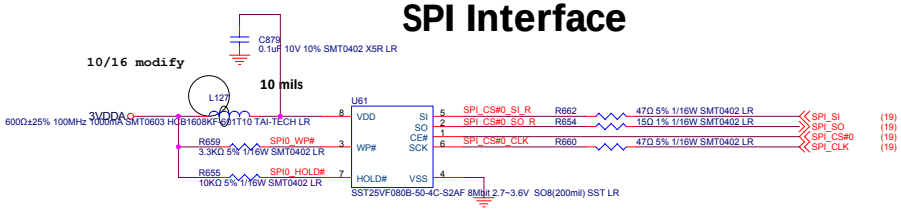


1/12 Modify

SPI Interface



(8,11,12,13,16,17,18,19,20,21,22,23,27,28,30,32,33,34,36,37,38,40,43,44,45,49,50,52,55,56,57) 3VDDM 3VDDM

(8,11,18,19,20,21,22,24,33,36,40,41,48,49,50,53,55,56,57) 3VDDA 3VDDA

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Title	PTT40TF>AMD+RS690M+SB600+M71S	
Size C	Document Number FirmWare Hub / SPI	Rev 0.4
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PCI-E LAYOUT GUIDE

Trace Length	Group Mismatch	Space
L<12"	<5mil	20:5:7:5:20 (L1,L6) 20:4:7:4:20 (L3,L4)

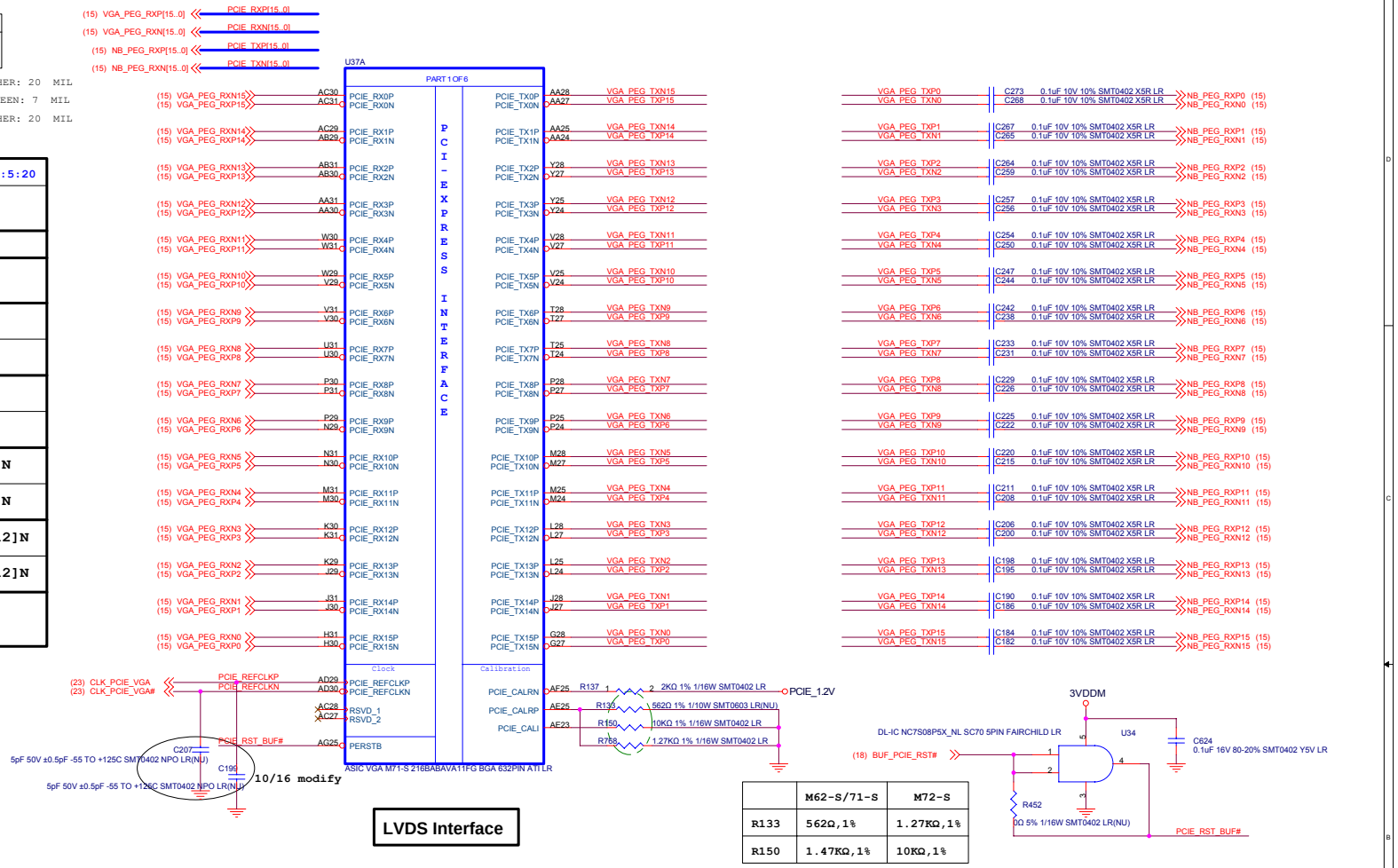
PCI-E clock must 100 ohms
PCI-E Trace length CONN to ATI chip L<3"
PCI-E data & control signals 5:20
PCI-E differential strobe pair
20:5:7:5:20

OTHER: 20 MIL
5 MIL BETWEEN: 7 MIL
5 MIL
OTHER: 20 MIL

PCI-E Clock Layout and Routing Guidelines

PCI-E CLK	Clock --> NB&VGA	5 mils/20 mils	20:5:5:5:20

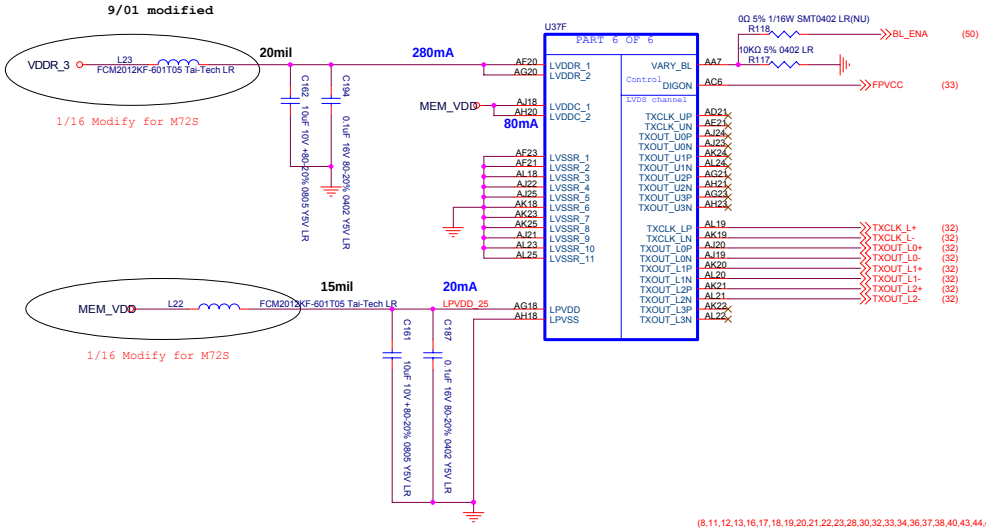
PCI_Express Bus Interface Pin Group	ADDRESS DATA & COMMAND
	PWRGD & PWRGD_MASK
PCI_Express Reference Clocks	PCIE_REFCLKP & PCIE_REFCLKN
PCI_Express Module 0	PCIE_TX[3:0]P & PCIE_TX[3:0]N
	PCIE_RX[3:0]P & PCIE_RX[3:0]N
PCI_Express Module 1	PCIE_TX[7:4]P & PCIE_TX[7:4]N
	PCIE_RX[7:4]P & PCIE_RX[7:4]N
PCI_Express Module 2	PCIE_TX[11:8]P & PCIE_TX[11:8]N
	PCIE_RX[11:8]P & PCIE_RX[11:8]N
PCI_Express Module 3	PCIE_TX[15:12]P & PCIE_TX[15:12]N
	PCIE_RX[15:12]P & PCIE_RX[15:12]N
PCI_Express Calibration Macro	PCIE_CALRN & PCIE_CALRP & PCIE_CALI



	M62-S/71-S	M72-S
R133	562Ω,1%	1.27KΩ,1%
R150	1.47KΩ,1%	10KΩ,1%

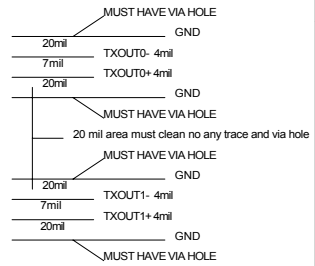
LVDS Interface

9/01 modified



The trace length of TXOUT0- should be equal to TXOUT0+
The trace length of TXOUT1- should be equal to TXOUT1+
The trace length of TXOUT2- should be equal to TXOUT2+
The trace length of TXCLK- should be equal to TXCLK+

Mismatch between TXLCK+/- and TXOUT+/- not exceed 25 mil



(28,30) VDDR_3 — VDDR_3
(18,28,29,30,31,56,57) MEM_VDD — MEM_VDD
(28,30,56) PCIE_1.2V — PCIE_1.2V
(8,11,12,13,16,17,18,19,20,21,22,23,28,30,32,33,34,36,37,38,40,43,44,45,49,50,52,55,56,57) 3VDDM — 3VDDM

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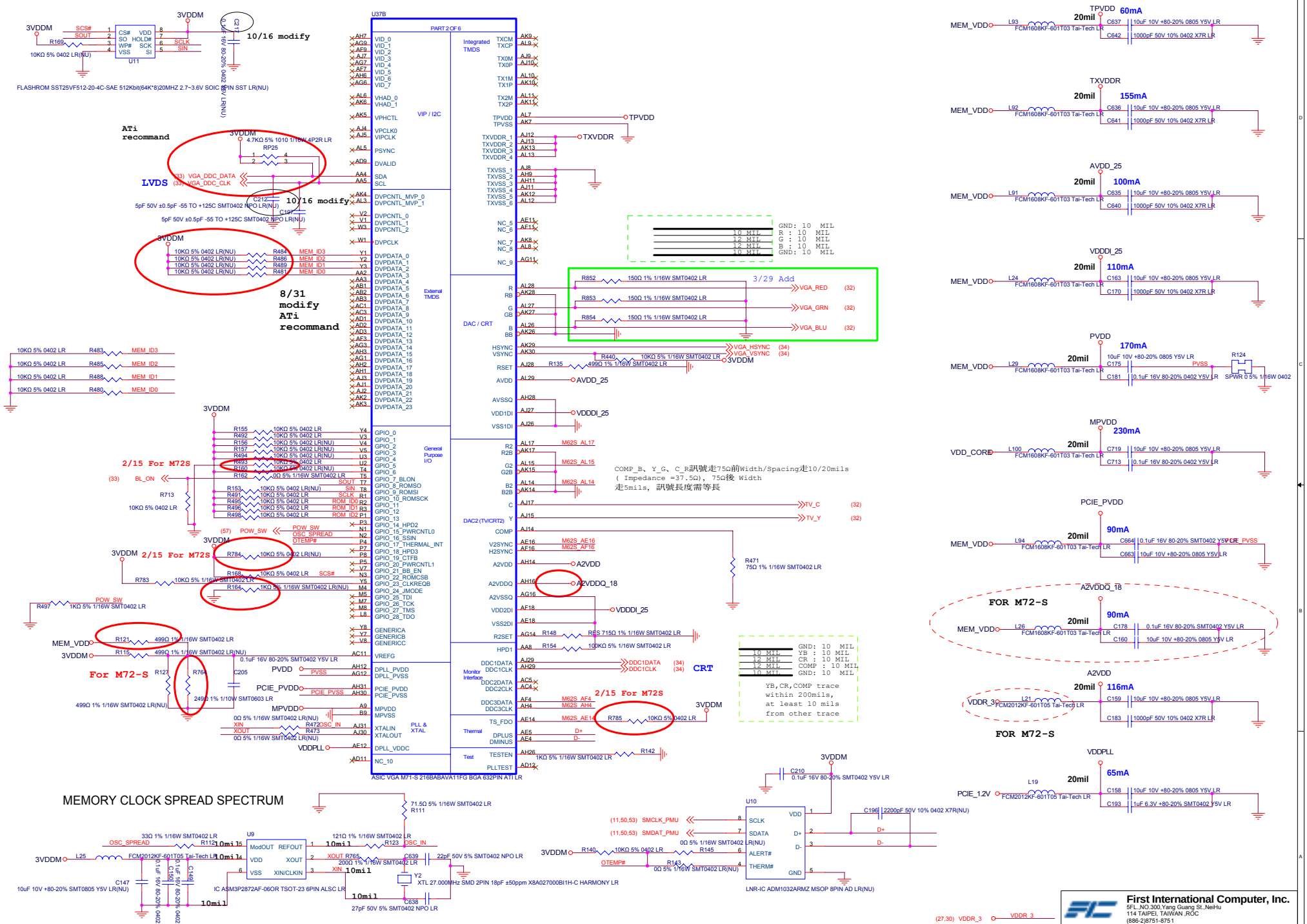
Title: PTT40TF>AMD+RS690M+SB600+M71S
Size: C | Document Number: M71-S PCI-E / LVDS | Rev: 0.4
Date: Wednesday, July 18, 2007 | Sheet 27 of 60


U37B
PART 2 OF 6
ASIC VGA M71-S 216BABAVA11FG BGA 632PIN A11 LR
VIP / I2C
Integrated TMDS
External TMDS
DAC / CRT
General Purpose I/O
DAC2 (TV/CRT2)
Monitor Interface
Thermal
Test
PLL & XTAL
FLASHROM SST25VF512-20-4C-SAE 512Kbit(64K*8)20MHZ 2.7~3.6V SOIC 8PIN SST LR(NU)
10/16 modify
ATi recommand
LVDS
8/31 modify ATi recommand
2/15 For M72S
For M72-S
FOR M72-S
CRT
3/29 Add
COMP_B、Y_G、C_R訊號走75Ω前Width/Spacing走10/20mils
(Impedance =37.5Ω), 75Ω後 Width
走5mils, 訊號長度需等長
YB,CR,COMP trace
within 200mils,
at least 10 mils
from other trace
MEMORY CLOCK SPREAD SPECTRUM
Vref clock swing level is VDDC for M62-S and M71-S ; 1.8V for M72-S ; Need to fine tune R80 and R106
LNR-IC ADM1032ARMZ MSOP 8PIN AD LR(NU)
IC ASM3P2872AF-06OR TSOT-23 6PIN ALSC LR
XTL 27.000MHz SMD 2PIN 18pF ±50ppm X8A027000BI1H-C HARMONY LR
TPVDD 60mA
TXVDDR 155mA
AVDD_25 100mA
VDDDI_25 110mA
PVDD 170mA
MPVDD 230mA
PCIE_PVDD 90mA
A2VDDQ_18 90mA
A2VDD 116mA
VDDPLL 65mA
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Title
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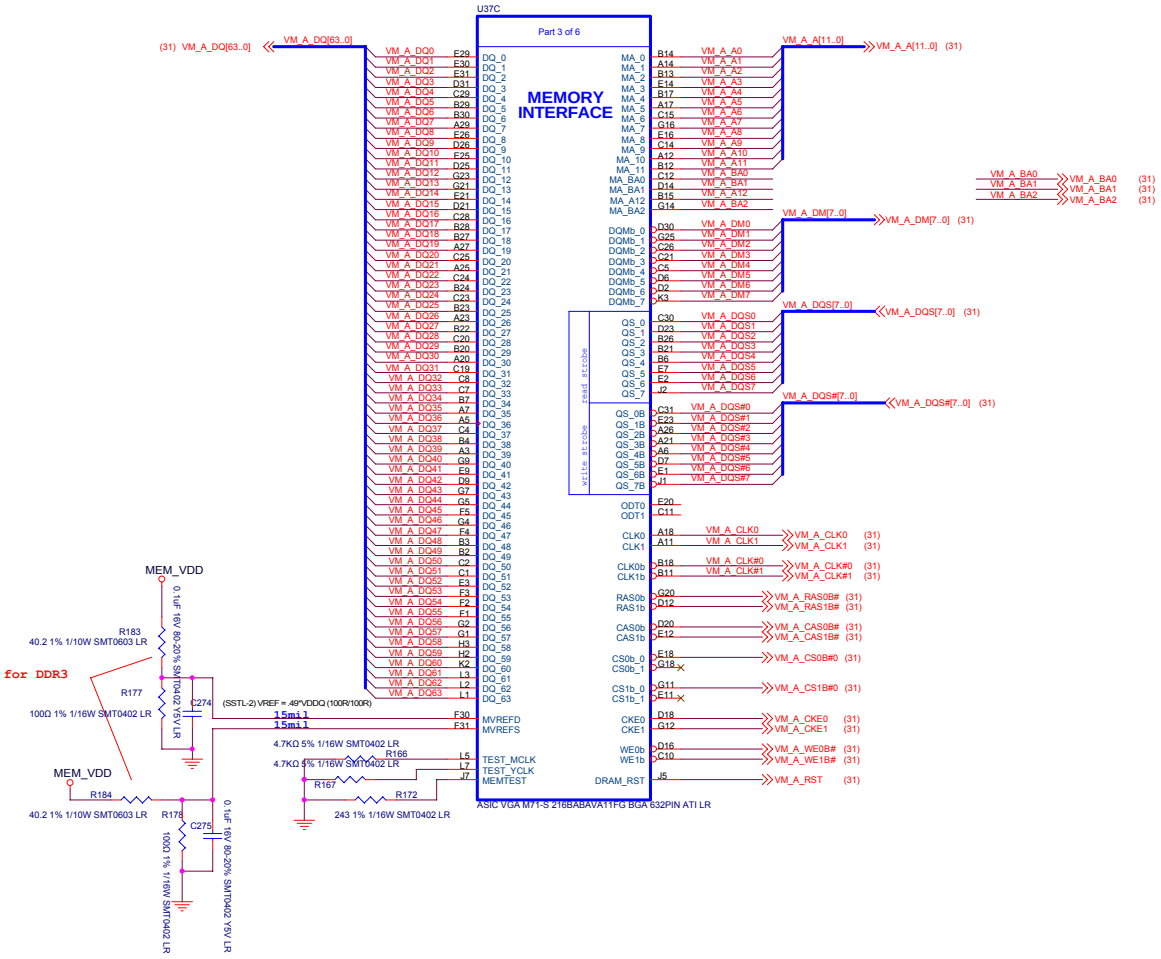
Size C
Document Number
M71-S VIDEO IF
Rev 0.4
Date: Wednesday, July 18, 2007
Sheet 28 of 60



1/9 Modify R183,R184 to 40.2 ohm for DDR3

Need equal length Length<=3000mil+/-50mil		
GND		5 mil
QSA	10 mil	5 mil
QSA#	10 mil	5 mil
GND	10 mil	5 mil

1. Data Group(MD,DQM, QS) Total length>1" ,<3"
2. The group trace lengths should be within +/- 50 mil of their respective strobe, the minimum is +/- 100 mil.
3. The difference in the length of strobe<= 0.5".
4. CLK pair lines, must be routed following the same rules for routing differential signals.
5. CLK lines must be routed to within 0.75".
6. The total line length of address/control lines within 0.5".

Need equal length Length<=3000mil+/-50mil		
OTHER SIGNAL		5 mil
MEM_MAA0	10 mil	5 mil
MEM_MAA1	10 mil	5 mil
MEM_MAA2	10 mil	5 mil
MEM_MAA3	10 mil	5 mil
MEM_MAA4	10 mil	5 mil
MEM_MAA5	10 mil	5 mil
MEM_MAA6	10 mil	5 mil
MEM_MAA7	10 mil	5 mil
MEM_MAA8	10 mil	5 mil
MEM_MAA9	10 mil	5 mil
MEM_MAA10	10 mil	5 mil
MEM_MAA11	10 mil	5 mil
MEM_MAA12	10 mil	5 mil
MEM_MAA13	10 mil	5 mil
OTHER SIGNAL		5 mil

Associated CLK	DATA	Mask	Strobe
CLK0,CLK0#	MD(7:0)	DQMA#0	DSA0 DQA#0
	MD(15:8)	DQMA#1	DSA1 DQA#1
	MD(23:16)	DQMA#2	DSA2 DQA#2
	MD(31:24)	DQMA#3	DSA3 DQA#3
CLK1,CLK1#	MD(39:32)	DQMA#4	DSA4 DQA#4
	MD(47:40)	DQMA#5	DSA5 DQA#5
	MD(55:48)	DQMA#6	DSA6 DQA#6
	MD(63:56)	DQMA#7	DSA7 DQA#7

Memory control signal:MEM_CS#,MEM_RAS#,MEM_CAS#,MEM_WE#,MEM_CKE(A/B)
Width:5mil , Space:7mil , Length<=3000mil+/-50mil

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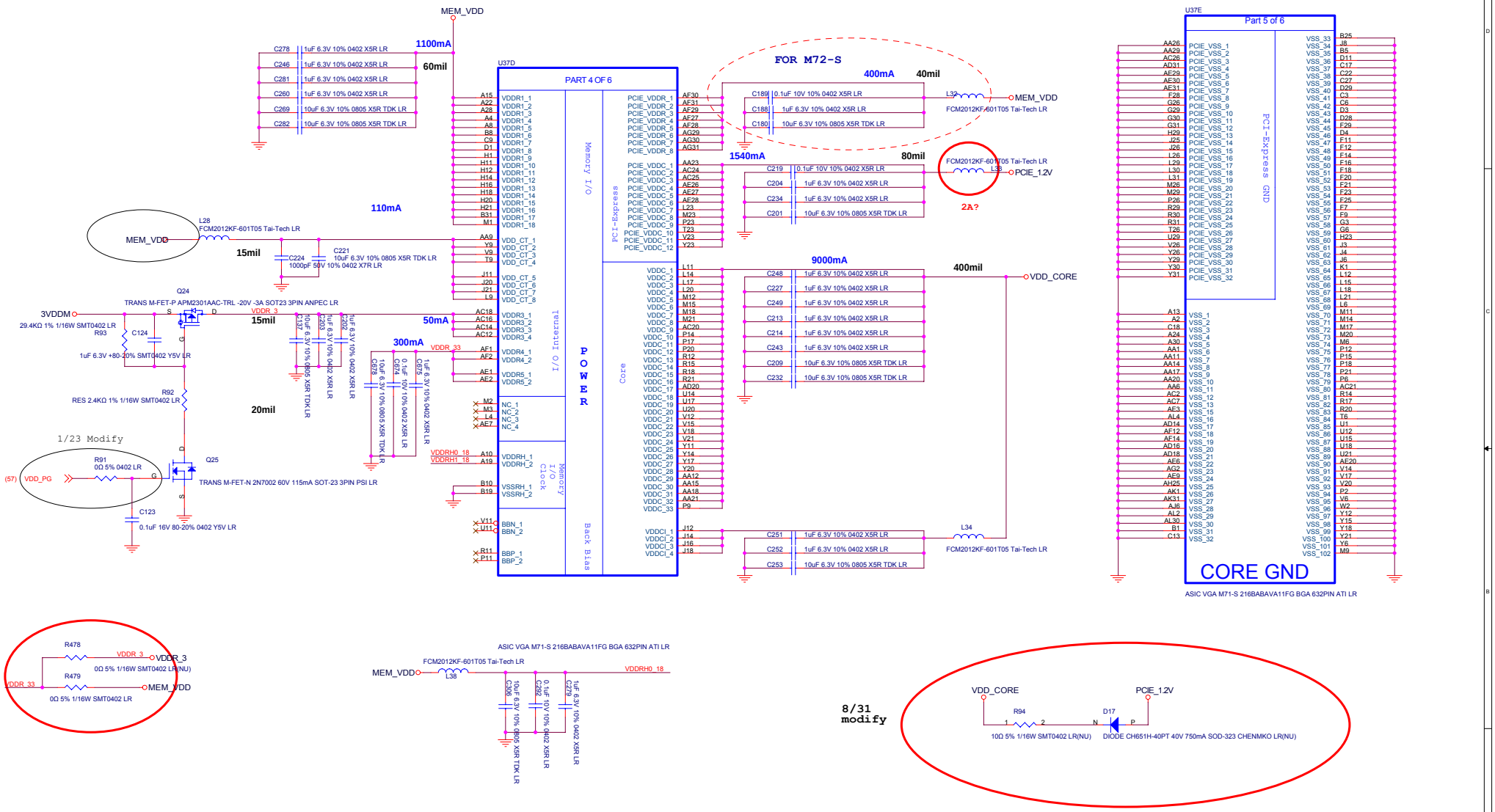
Size: C | Document Number: M71-S Memory IF | Rev: 0.4

Date: Wednesday, July 18, 2007 | Sheet 29 of 60



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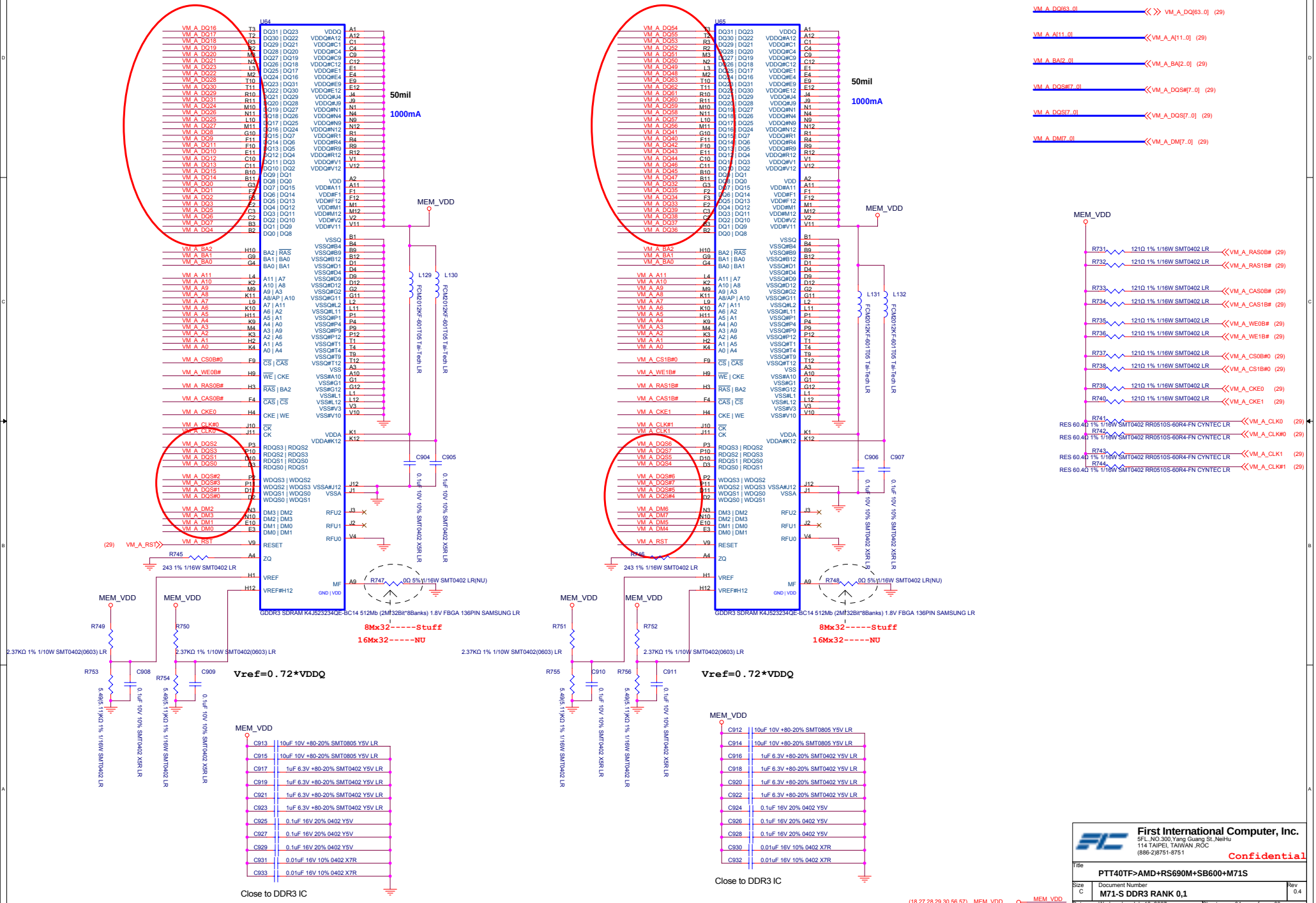
Size: C | Document Number: M71-S Power / GND | Rev: 0.4

Date: Wednesday, July 18, 2007 | Sheet 30 of 60

Samsung 16Mx32 | 02-41059-01



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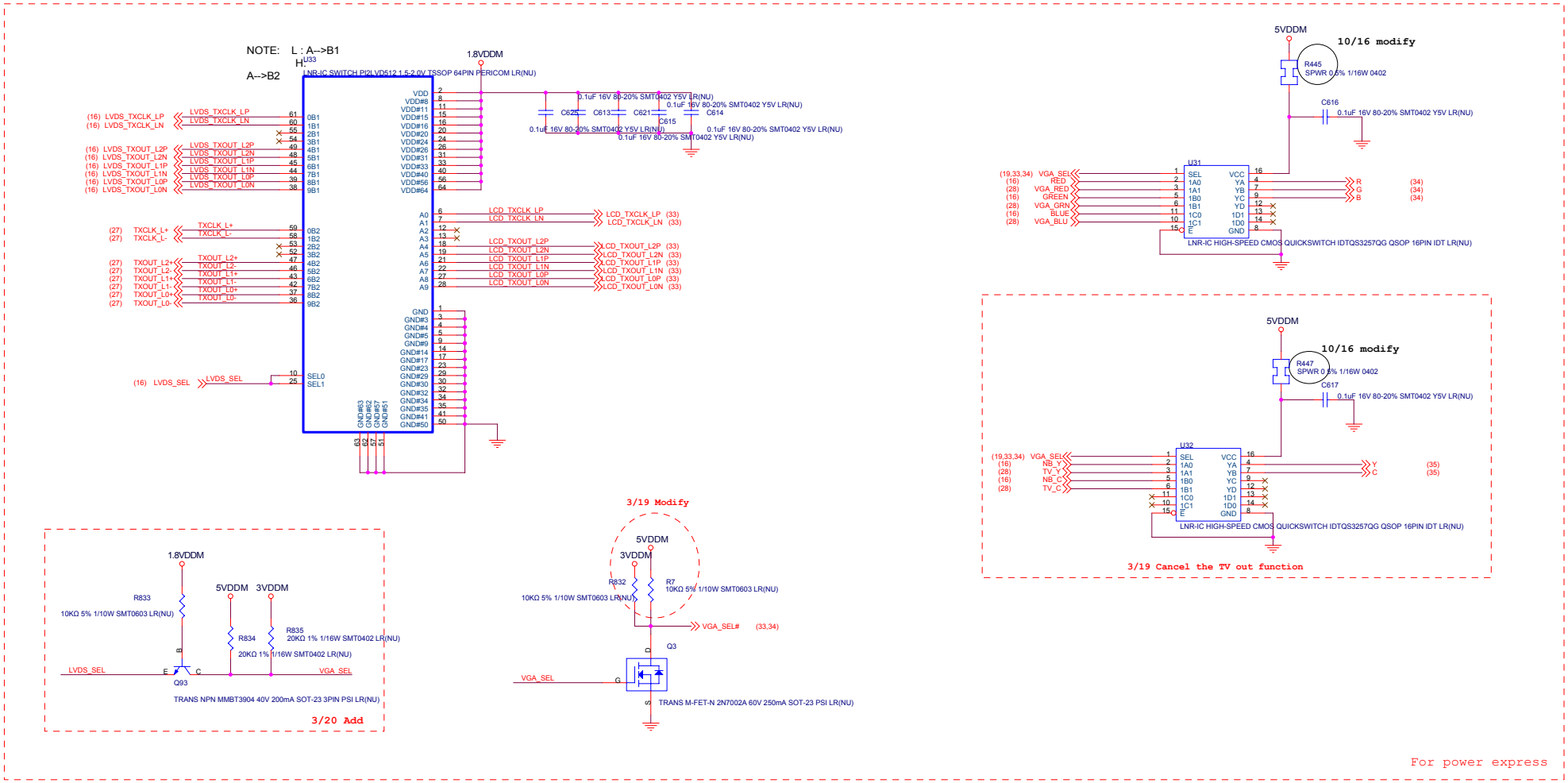
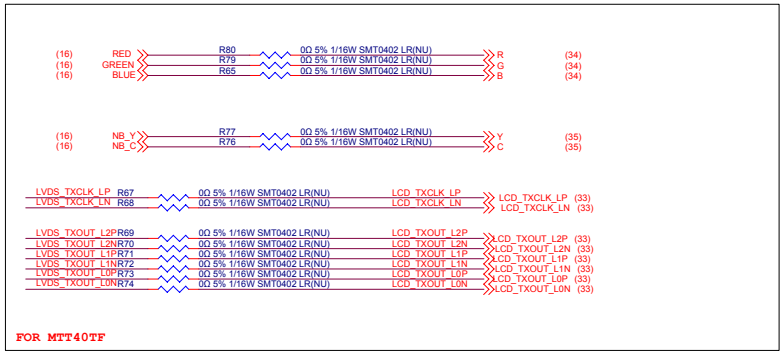
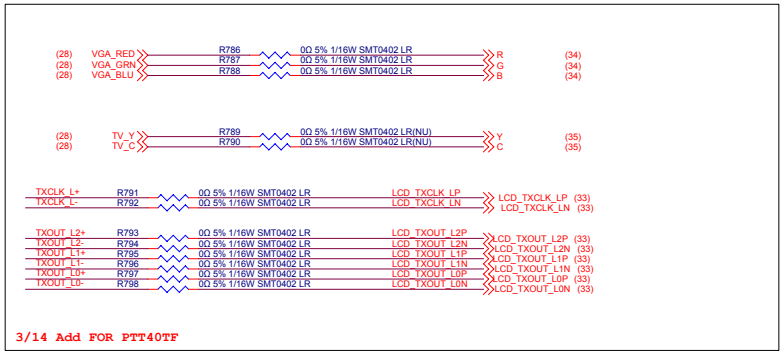
Size: C | Document Number: M71-S DDR3 RANK 0,1 | Rev: 0.4

Date: Wednesday, July 18, 2007 | Sheet 31 of 60







(8,11,12,13,16,17,18,19,20,21,22,23,27,28,30,33,34,36,37,38,40,43,44,45,49,50,52,55,56,57) 3VDDM — 3VDDM

(16,17,21,57) 1.8VDDM — 1.8VDDM

(11,16,21,34,35,36,37,46,47,55,56) 5VDDM — 5VDDM

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LVDS Signal Group Routing Guideline

GMCH — P1 — TL1 — LVDS CN

Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Differential Mode Impedance	100 +/- 20%
Nominal Trace Width	4 mils
Nominal Pair Spacing (Edge to edge)	7 mils
Minimum Pair-to-Pair Spacing	20 mils
Minimum Serpentine Spacing	20 mils
Minimum Spacing to Other LVDS	20 mils
Minimum Isolation Spacing to non-LVDS	20 mils
Maximim Via Count	2 (per line)
Package Length Range - P1	750 mils +/- 250 mils
Total MB Length - TL1	Max = 10"
Length Matching with Pair	Matching to within +/- 20mils
Clock to Data Length Matching (Total Length)	Matching Data to Clock within +/- 20mils
Clock A to Clock B Length Matching	Match Clock A to B within +/- 20mils
Breakout Exceptions (Reduce geometries for GMCH break-out region)	4/4 mils spacing allowed and 10 mils Pair-to-Pair spacing allowed Max. breakout length is 500 mils

***Cable Length must be less than 16"

Min : 80 MIL or Power Plane

Please close to LCD CONN

TRANS M-FET-P APM2679CC-TRL -20V -4A SOT-23-6 6PIN ANPEC LR

3VDDA (80mil) Q39 (80mil) R350 SPWR 0 5% 1/4W 1206 (80mil)

C525 0.1uF 16V 80-20% SMT0402 Y5V LR

R365 47KΩ 5% 1/16W SMT0402 LR

R367 4.7KΩ 5% 1/16W SMT0402 LR

C496 10uF 10V +80-20% SMT0805 Y5V LR

C496 0.1uF 16V 80-20% SMT0402 Y5V LR

R857 0Ω 5% 1/16W SMT0402 LR(NU) For MTT40TF

R855 0Ω 5% 1/16W SMT0402 LR For PTT40TF 4/19 Add

(16) LVDS_ENALCD — ENALCD — Q42 TRANS NPN RT1N441M-T111-1 50V 100mA SC-70 3PIN IDC LR

(27) FPVCC — DIODE STKY BAS40C 40V 200mA SOT-23 3PIN PSI LR(NU)

R859 1KΩ 5% 1/16W SMT0402 LR(NU) 5/15 Add

R369 100KΩ 5% 1/16W SMT0402 LR

4/25 Modify

3VDDM 20mil L71 600Ω±25% 100MHz 1000mA SMT0603 HCB1608KF-601T10 TAI-TECH LR 10/16 modify

RP1 RP 2.2KΩ 5% SMT1010 4P2R 1/16W LR

3VDDM 5pF 50V ±0.5pF -55 TO +125C SMT0402 NPO LR C6 C7 5pF 50V ±0.5pF -55 TO +125C SMT0402 NPO LR

C505 1000pF 50V 10% SMT0402 X7R LR

LCD_DDC_DATA LCD_DDC_CLK

INVENA (50) BRIGHTNESS

CN1

(32) LCD_TXCLK_LN (32) LCD_TXCLK_LP

(32) LCD_TXOUT_L2N (32) LCD_TXOUT_L2P

(32) LCD_TXOUT_L1N (32) LCD_TXOUT_L1P

(32) LCD_TXOUT_L0N (32) LCD_TXOUT_L0P

under connector

Please close to LCD CONN

100mil 100mil

L72 HCB2012KF-121T30 TAI-TECH LR 10/16 modify DCIN

C506 10uF 25V ±10% SMT1210 X7R C3225X7R1E106KT TDK LR(NU)

20-25355-00

CON ACES 88328-3001 SMD LVDS/LCD POWER 30 PIN F=1.0 H=6mm 直立(板上) LR

LCD brightness control from N.B.

3VDDM 2.5VDDM R368 1KΩ 1% 0402 LR(NU) R361 2.2KΩ 5% 0402 LR(NU)

(50) LCD_BRIGHTNESS — Q41 2N7002 60V 115mA SOT-23 PSI LR(NU) — BRIGHTNESS

R363 100KΩ 5% 0402 LR(NU) 1/23 Modify

R362 0Ω 5% 0402 LR

(28) VGA_DDC_DATA — R801 0Ω 5% 1/16W SMT0402 LR — Q43 TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR(NU) — LCD_DDC_DATA

(19,32,34) VGA_SEL — R371 0Ω 5% 1/16W SMT0402 LR(NU)

(28) VGA_DDC_CLK — Q44 TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR(NU) — LCD_DDC_CLK — R804 0Ω 5% 1/16W SMT0402 LR For PTT40TF

(16) NB_DDC_DATA — R805 0Ω 5% 1/16W SMT0402 LR(NU) — Q45 TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR(NU) — LCD_DDC_DATA

(32,34) VGA_SEL — R379 0Ω 5% 1/16W SMT0402 LR(NU)

(16) NB_DDC_CLK — Q46 TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR(NU) — LCD_DDC_CLK — R806 0Ω 5% 1/16W SMT0402 LR(NU) For MTT40TF

11/24 Modify

3VDDM R714 4.7KΩ 5% 1/16W SMT0402 LR

3VDDM R715 6.8KΩ 1% 1/10W SMT0603 LR — INVENA

1.5VDDM R716 2.7KΩ 5% 1/16W SMT0402 LR

(36,50) LID# — D18A — LCD_BLON — D18B — (20,22,50) SB_PWRGD — D18C

DIODE RB731U 40V 30mA SMD6(SC-74) 6PIN ROHM LR

Q78 TRANS NPN RT2N05M 50V 100mA SC-88A(SOT-353) 5PIN IDC LR

R858 0Ω 5% 1/16W SMT0402 LR(NU) For MTT40TF

R856 0Ω 5% 1/16W SMT0402 LR For PTT40TF 4/19 Add

(16) LVDS_ENABKL — D58 — LCD_BLON

(28) BL_ON — DIODE STKY BAS40C 40V 200mA SOT-23 3PIN PSI LR(NU)

R862 1KΩ 5% 1/16W SMT0402 LR(NU) 5/22 Add

R838 1KΩ 5% 1/16W SMT0402 LR

4/25 Modify

(40,57) 1.5VDDM — 1.5VDDM

(8,57) 2.5VDDM — 2.5VDDM

(8,11,12,13,16,17,18,19,20,21,22,23,27,28,30,32,34,36,37,38,40,43,44,45,49,50,52,55,56,57) 3VDDM — 3VDDM

(8,11,18,19,20,21,22,24,26,36,40,41,48,49,50,53,55,56,57) 3VDDA — 3VDDA

(52,53,54,55,56,57) DCIN — DCIN

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Size: C | Document Number: LCD CNN | Rev: 0.4

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CRT CIRCUIT

OPTIONAL ESD PROTECTION DIODES

【CRT Routing Rules】
1. R、G、B Trace Before 75 Ω = 10/25、After 75 Ω = 5/20
2. HSYNC、VSYNC = 5/20

WIDTH=10 MILS Z0=37.5 ohms

4/26 Modify

WIDTH= 5 MILS Z0=75 ohms

5VDDM

D4A D4B D4C D1A D1B D1C
DIODE ARRAY MMBD4448HTM-7-F 80V 500mA SOT-26 6PIN DIODES LR

C11 0.1uF 16V 80-20% SMT0402 Y5V LR
C12 0.1uF 16V 80-20% SMT0402 Y5V LR(NU)
C10 0.1uF 16V 80-20% SMT0402 Y5V LR(NU)

5VDDM F1 20mil D2 CRT5VS L1 20mil C2
750mA 13.2V SMT1812 miniSMDC075F-2 RAYCHEM LR
SS14 40V 1A SMA PSI LR
600Ω±25% 100MHz 1000mA SMT0603 HCB1608KF-601T10 TAI-TECH LR
0.1uF 25V 80-20% SMT0603 Y5V LR(NU)

(32) R — R360 0Ω 5% 1/10W SMT0603 LR — L79 68nH±5% 300mA SMT0805 HCI2012F-68NJ TAI-TECH LR
(32) G — R357 0Ω 5% 1/10W SMT0603 LR — L78 68nH±5% 300mA SMT0805 HCI2012F-68NJ TAI-TECH LR
(32) B — R356 0Ω 5% 1/10W SMT0603 LR — L77 68nH±5% 300mA SMT0805 HCI2012F-68NJ TAI-TECH LR
VEDAT 10mils — L76 100MHz 300Ω 25% SMT0603 HCB1608 KF-301T20 TAI-TECH LR
R352 39Ω 1% 1/10W SMT0603 LR
R351 39Ω 1% 1/10W SMT0603 LR
VECLK 10mils — L75 100MHz 300Ω 25% SMT0603 HCB1608 KF-301T20 TAI-TECH LR

R359 150Ω 1% 1/16W SMT0402 LR
R358 150Ω 1% 1/16W SMT0402 LR
R355 150Ω 1% 1/16W SMT0402 LR
C993 5pF 50V ±0.5pF -55 TO +125C SMT0402 NPO LR(NU)
C994 5pF 50V ±0.5pF -55 TO +125C SMT0402 NPO LR(NU)
C995 5pF 50V ±0.5pF -55 TO +125C SMT0402 NPO LR(NU)
C521 27pF 50V 5% SMT0402 NPO LR
C519 27pF 50V 5% SMT0402 NPO LR
C523 10pF 50V 5% SMT0402 NPO LR
C522 10pF 50V 5% SMT0402 NPO LR
C520 10pF 50V 5% SMT0402 NPO LR
C510 10pF 50V 5% SMT0402 NPO LR
C513 10pF 50V 5% SMT0402 NPO LR
C514 10pF 50V 5% SMT0402 NPO LR
C5 10uF 10V +80-20% SMT0805 Y5V LR(NU)
C508 27pF 50V 5% SMT0402 NPO LR
C509 27pF 50V 5% SMT0402 NPO LR
C512 27pF 50V 5% SMT0402 NPO LR
C511 27pF 50V 5% SMT0402 NPO LR

CN18
CON SUYIN D/P D-sub 15PIN 070546FR015S229CU(TUBE) LR
20-25071-00

R6 SPWR 0 5% 1/16W 0603
CRT_GND 10/16 GND_CRT

FOR PTT40TF

(28) VGA_HSYNC — 10mils — C600 27pF 50V 5% SMT0402 NPO LR(NU) — U30 DL-IC NC7SZ126P5X_NL SC-70 5PIN FAIRCHILD LR
(19,32,33) VGA_SEL — R437 0 5% 1/16W 0603 LR(NU) — R807 0Ω 5% 1/16W SMT0402 LR — 3VDDM — 10mils
(28) VGA_VSYNC — 10mils — C599 27pF 50V 5% SMT0402 NPO LR(NU) — U29 DL-IC NC7SZ126P5X_NL SC-70 5PIN FAIRCHILD LR

FOR MTT40TF

(16) HSYNC — 10mils — C598 27pF 50V 5% SMT0402 NPO LR(NU) — U28 DL-IC NC7SZ126P5X_NL SC-70 5PIN FAIRCHILD LR(NU)
(32,33) VGA_SEL# — R436 0 5% 1/16W 0603 LR(NU) — R811 0Ω 5% 1/16W SMT0402 LR(NU) — 3VDDM — 10mils
(16) VSYNC — 10mils — C597 27pF 50V 5% SMT0402 NPO LR(NU) — U27 DL-IC NC7SZ126P5X_NL SC-70 5PIN FAIRCHILD LR(NU)

FOR MTT40TF

(16) Q_VEDAT — R808 0Ω 5% 1/16W SMT0402 LR(NU) — Q83 TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR(NU) — VEDAT_R
(32,33) VGA_SEL# — R727 0Ω 5% 1/16W SMT0402 LR(NU)
(16) Q_VECLK — Q84 TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR(NU) — VECLK_R — R809 0Ω 5% 1/16W SMT0402 LR(NU)

FOR PTT40TF

(28) DDC1DATA — R810 0Ω 5% 1/16W SMT0402 LR — Q85 TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR(NU) — VEDAT_R
(19,32,33) VGA_SEL — R728 0Ω 5% 1/16W SMT0402 LR(NU)
(28) DDC1CLK — Q86 TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR(NU) — VECLK_R — R812 0Ω 5% 1/16W SMT0402 LR

C526 5pF 50V ±0.5pF -55 TO +125C SMT0402 NPO LR(NU)
VECLK_R — Q2 TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR — VECLK
3VDDM — RP29 4.7KΩ 5% 1010 1/16W 4P2R LR
VEDAT_R — Q1 TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR — VEDAT
C527 5pF 50V ±0.5pF -55 TO +125C SMT0402 NPO LR(NU)

CRT5VS
R4 6.8KΩ 1% 1/16W SMT0402 LR — VEDAT
R5 6.8KΩ 1% 1/16W SMT0402 LR — VECLK

(8,11,12,13,16,17,18,19,20,21,22,23,27,28,30,32,33,36,37,38,40,43,44,45,49,50,52,55,56,57) 3VDDM — 3VDDM
(11,16,21,32,35,36,37,46,47,55,56) 5VDDM — 5VDDM

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Size C	Document Number CRT Connector	Rev 0.4
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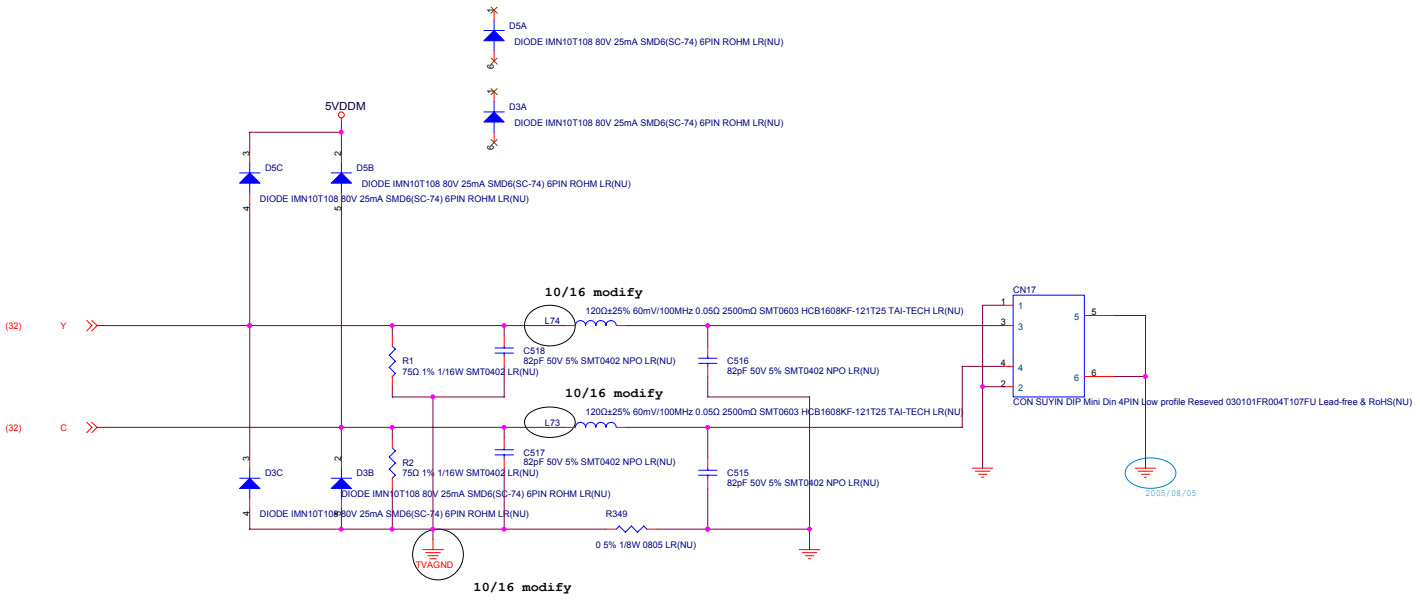
TV OUT CIRCUIT



3/19 Cancel the TV out function

(11,16,21,32,34,36,37,46,47,55,56) 5VDDM 5VDDM

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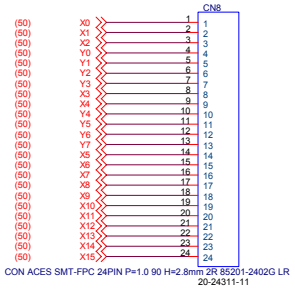
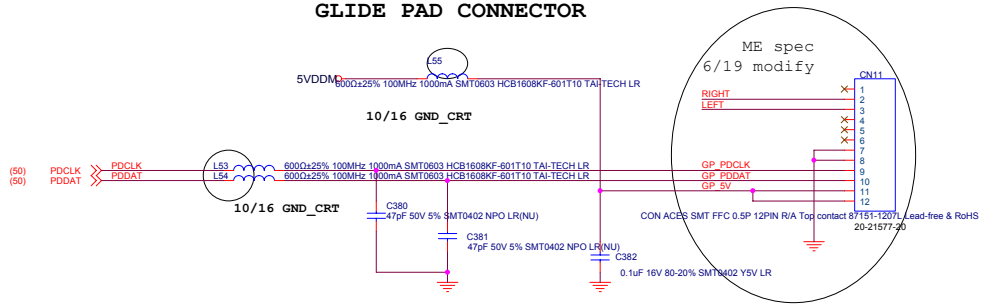
Size C	Document Number S-VEDIO	Rev 0.4
Date: Wednesday, July 18, 2007	Sheet 35 of 60	

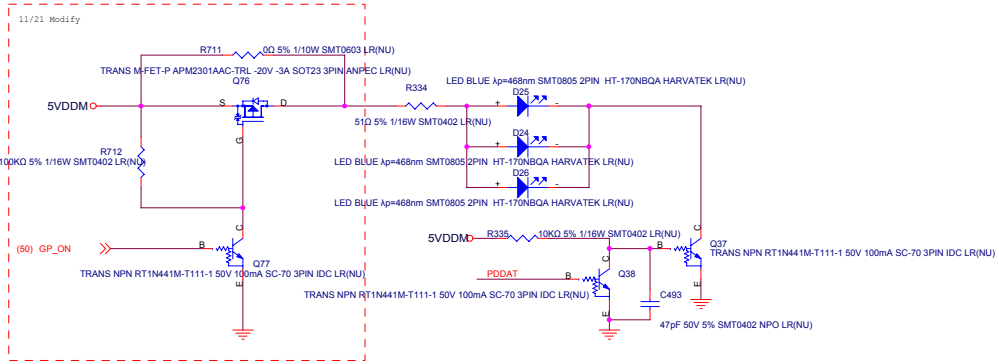
Same as CTx projects

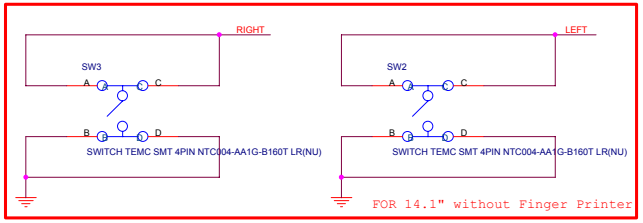
INT KB CNN

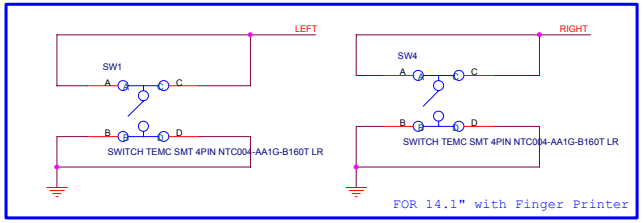


GLIDE PAD CONNECTOR

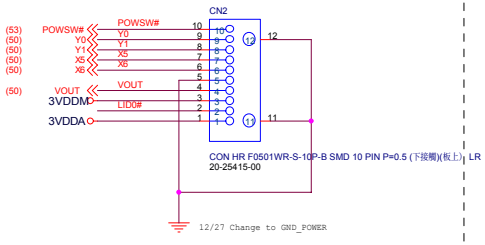




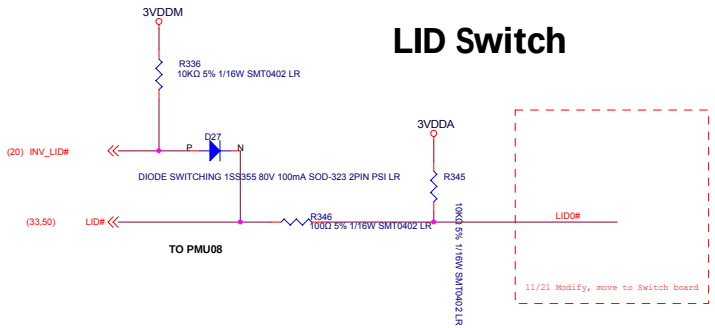




SWITCH BOARD CONNECTOR



LID Switch



(8,11,12,13,16,17,18,19,20,21,22,23,27,28,30,32,33,34,37,38,40,43,44,45,49,50,52,55,56,57) 3VDDM 3VDDM
(8,11,18,19,20,21,22,24,26,33,40,41,48,49,50,53,55,56,57) 3VDDA 3VDDA
(11,16,21,32,34,35,37,46,47,55,56) 5VDDM 5VDDM

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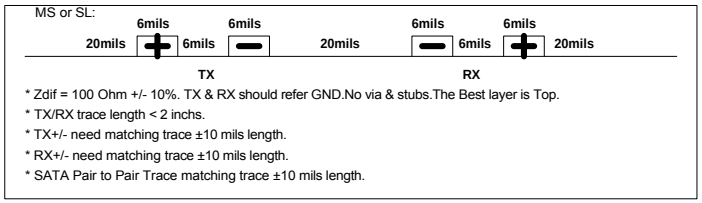
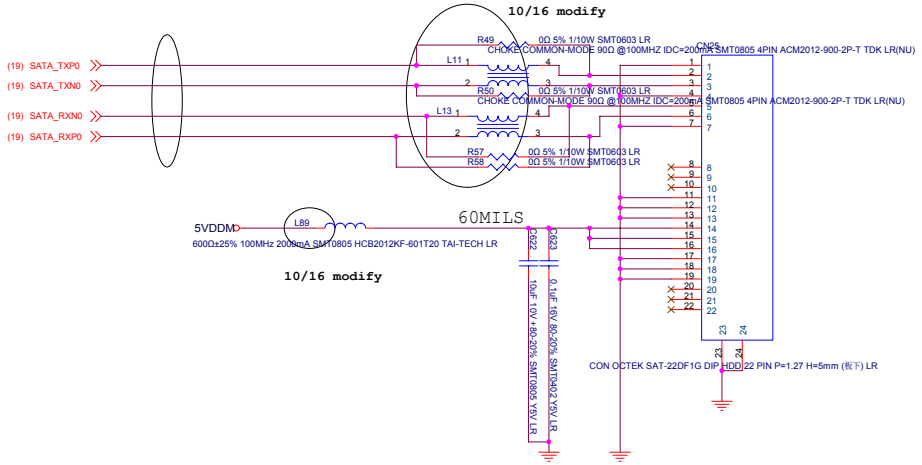
Size C	Document Number <INT K/B /LID/GP/SW CNN>	Rev 0.4
Date: Wednesday, July 18, 2007	Sheet 36 of 60	

SATA Layout Note:

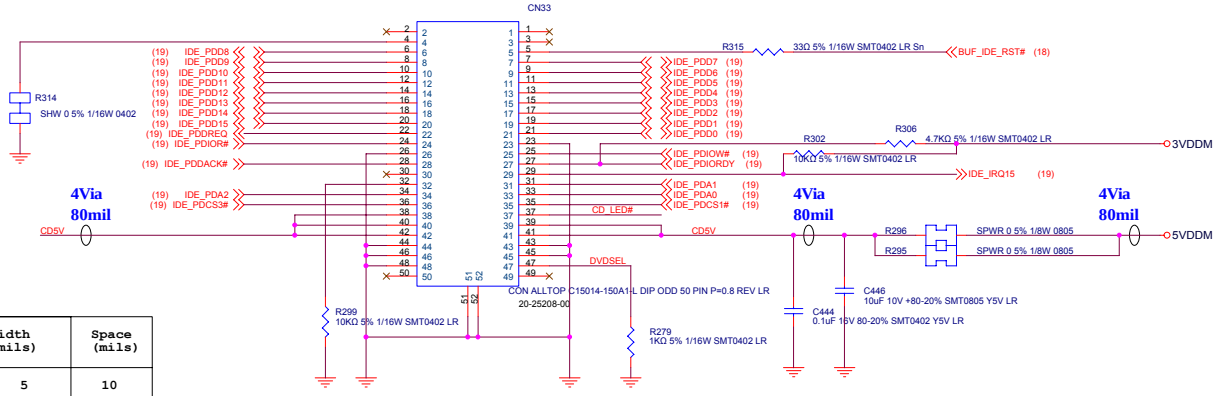


NOTE

SATA differential stripline 20:5:6:5:20
SATA differential mircostripline 20:6:6:6:20
請包GROUND

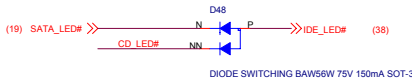


CD-ROM CNN



IDE Signals

Signals	MAX Length (inch)	Width (mils)	Space (mils)
IDE_PDD[15:0]	8	5	10
IDE_SDD[15:0]	8	5	10
IDE_PDA0-2	8	5	10
IDE_SDA0-2	8	5	10
IDE_PDCS 10-30#	8	5	10
IDE_PDDREQ	8	5	10
IDE_SDDREQ	8	5	10
IDE_PDIOW#	8	5	10
IDE_PATADET	8	5	10
IDE_SATADET	8	5	10
IDE_PDDACK#	8	5	10
IDE_SDDACK#	8	5	10



(8,11,12,13,16,17,18,19,20,21,22,23,27,28,30,32,33,34,36,38,40,43,44,45,49,50,52,55,56,57) 3VDDM — 3VDDM
(11,16,21,32,34,35,36,46,47,55,56) 5VDDM — 5VDDM

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Size	Document Number	Rev
C	SATA / IDE connector	0.4

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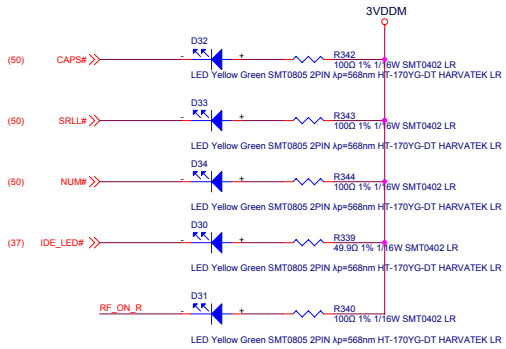
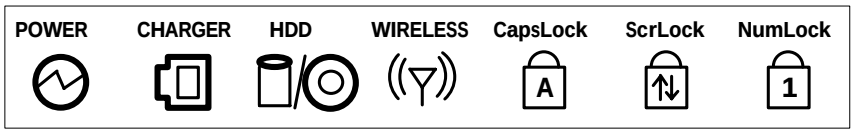
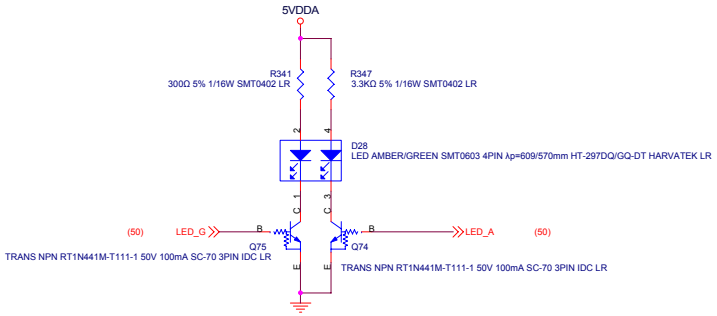
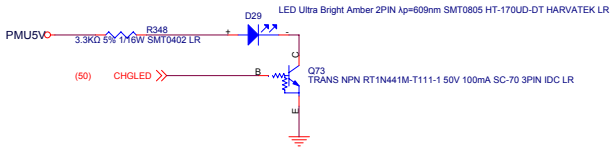
LED indicator control logic



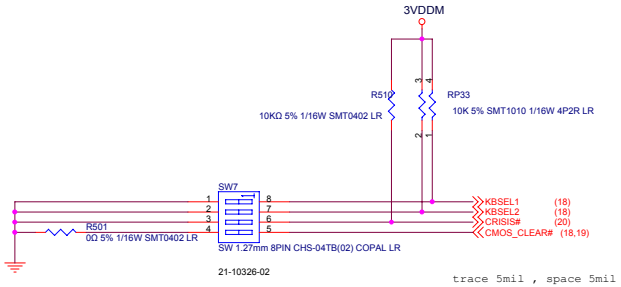
D28 D29 D30 D31 D32 D33 D34







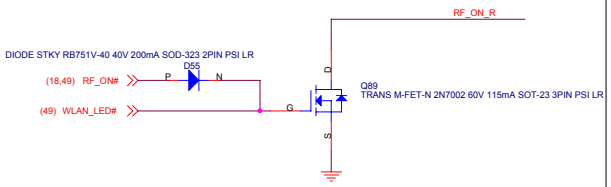
DIP SWITCH



12/27 R501 Change to RES 0 ohm

KBSEL2	KBSEL1	
ON	ON	UK Keyboard
	OFF	Reserved
OFF		JP Keyboard
OFF	OFF	US Keyboard

MB_ID0	ON	Reserved
	OFF	Reserved
LOGSEL	ON	Reserved
	OFF	Reserved
PASS0	ON	Override
	OFF	Available
DVDSEL	ON	CD-ROM
	OFF	DVD
CMOS_CLEAR	ON	Reset RTC
	OFF	NONE



1/24 add

(8,11,12,13,16,17,18,19,20,21,22,23,27,28,30,32,33,34,36,37,40,43,44,45,49,50,52,55,56,57) 3VDDM — 3VDDM
(22,39,49,52,55,56,57) 5VDDA — 5VDDA
(50,55) PMU5V — PMU5V

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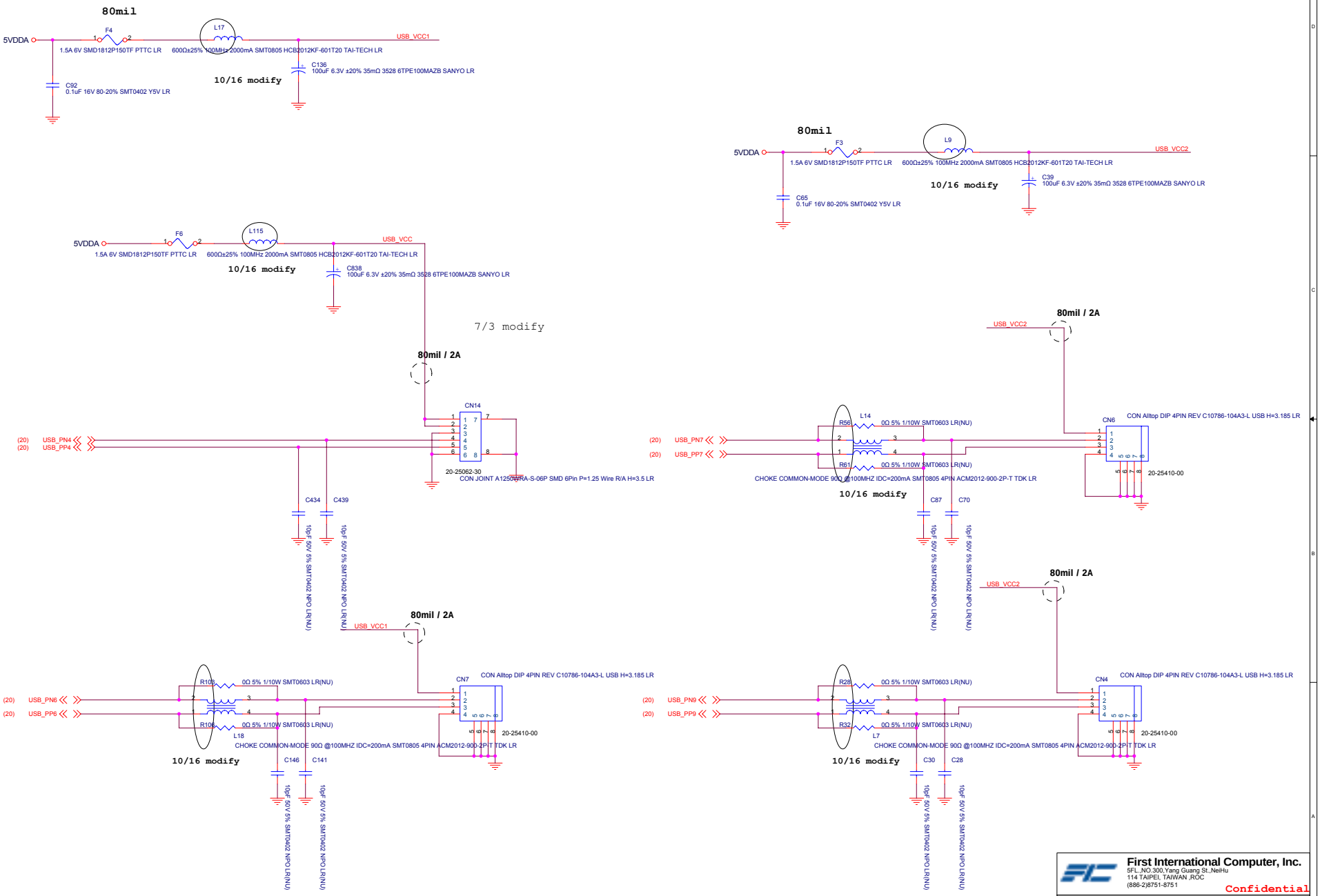
Size C | Document Number: DIP SW/ LED / READING LAMP | Rev 0.4

Date: Wednesday, July 18, 2007 | Sheet 38 of 60



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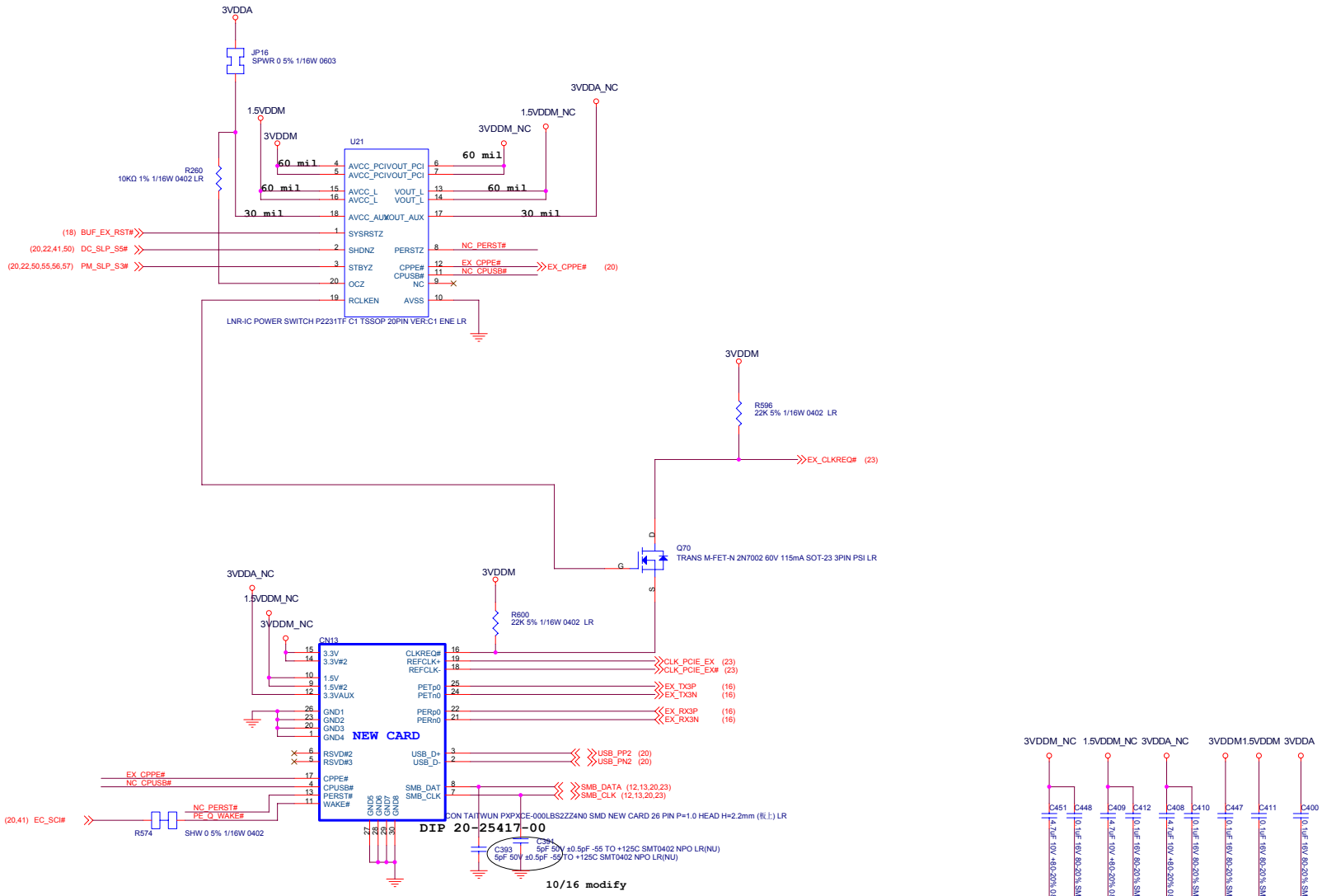
Title	PTT40TF>AMD+RS690M+SB600+M71S
Size C	Document Number: USB CNN
Rev	0.4
Date: Wednesday, July 18, 2007	Sheet 39 of 60



(33,57) 1.5VDDM — 1.5VDDM

(8,11,12,13,16,17,18,19,20,21,22,23,27,28,30,32,33,34,36,37,38,43,44,45,49,50,52,55,56,57) 3VDDM — 3VDDM

(8,11,18,19,20,21,22,24,26,33,36,41,48,49,50,53,55,56,57) 3VDDA — 3VDDA

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Title: **PTT40TF>AMD+RS690M+SB600+M71S**

Size	Document Number	Rev
C	New Card(express card)	0.4

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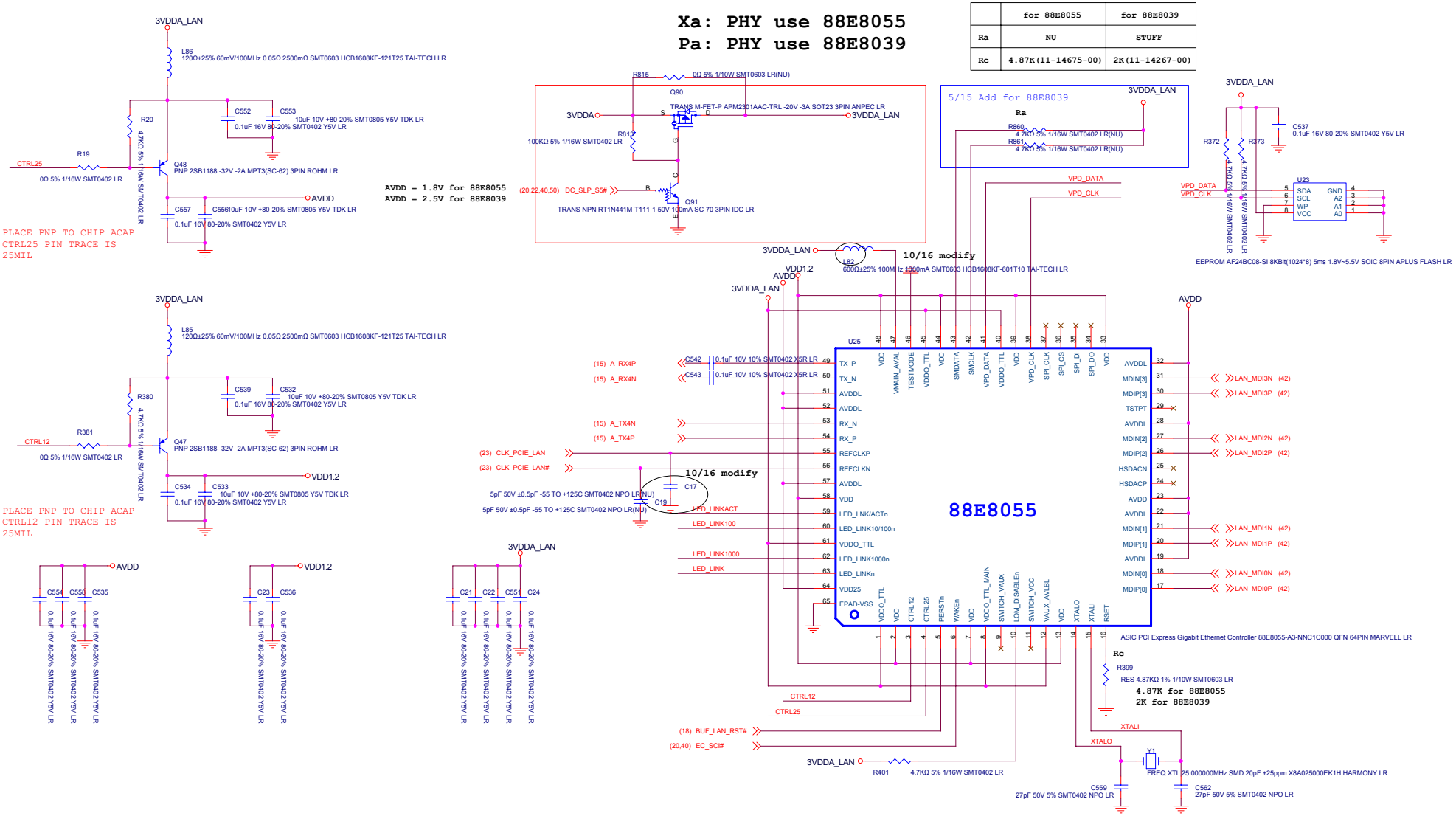

Layout Guide

1.The Lan Chip should be placed as close as possible to the transfer.
2. The resistor connected to RSET pin should be placed near to the Lan Chip,and away from signal traces(ex:MDI0+/-) and clock signals as far as possible.
3. The transfer should be placed as close as possible to the RJ45 connector.
4. The crystal should be placed far away from I/O ports and high frequency signal.
5. The termination resistors and capacitors should be placed closely to the Lan Chip.
6. The decoupling capacitors should be placed as close as posslble to the power pins,such that the distance from IC power pin to the capacitor is within 200mils.
7. Traces routed from the Lan Chip to the transfer,and to the RJ45 connector should be as short as possible.
8. The 10-12cm maximum lenghth between Lan Chip and transfer is achievable only when there's no interferences around.
9. All 4 pairs of the differential resister(49.9k) must close to Lan Chip,and make them(4pairs) as same as distant.
10.PLACE GND PLANE AS LARGE AS POSSIBLE
11.If power pins are next to each other and there is not much room to accommodate multipe capacitors,then the power pins can share the same capacitors.
12.It's important to separate digital signals from analog signals.If it is unavoidable to cross digtal signals with analog power do it at 90 degree angle.
13. The digital power plane should be separated from analog areas.
14. All analog decoupling capacitors should be placed as close to the IC as possible and the traces should be short.
15.The Lan Chip pin 1 facing the transformer,then you can make the signal shorter.

(42) AVDD — AVDD
(8,11,12,13,16,17,18,19,20,21,22,23,27,28,30,32,33,34,36,37,38,40,43,44,45,49,50,52,55,56,57) 3VDDM — 3VDDM
(8,11,18,19,20,21,22,24,26,33,36,40,48,49,50,53,55,56,57) 3VDDA — 3VDDA

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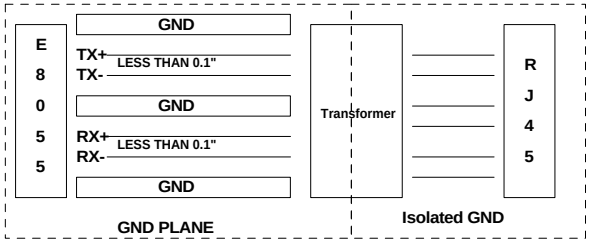
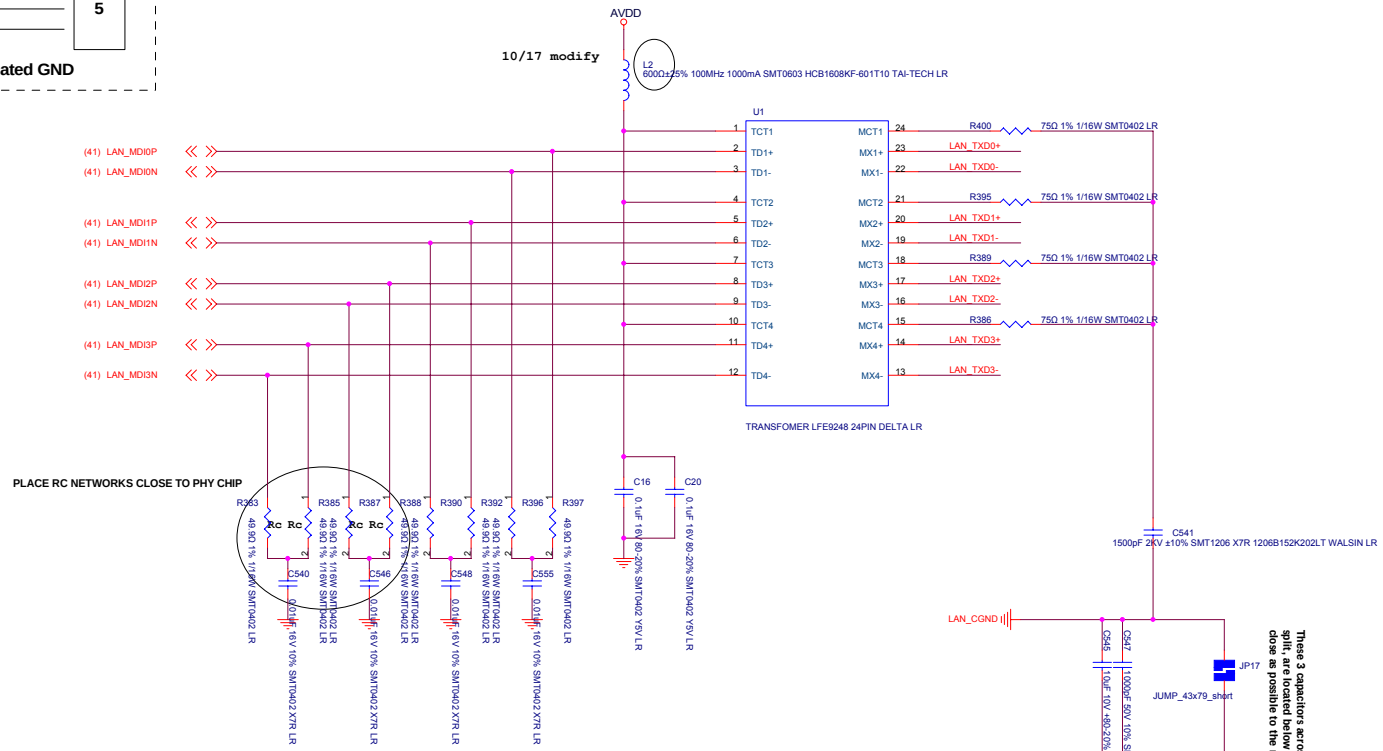
Title: PTT40TF>AMD+RS690M+SB600+M71S
Size: C | Document Number: PCIE GIGA LAN PHY 88E8055 | Rev: 0.4
Date: Wednesday, July 18, 2007 | Sheet 41 of 60

TX
RX

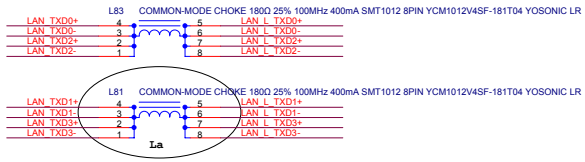
100 ohm ---> trace 4 mil , space 10 mil
50 mil space from other signals
Total Tace Length no more thans 4.8"
2 Differential pairs must have the same length

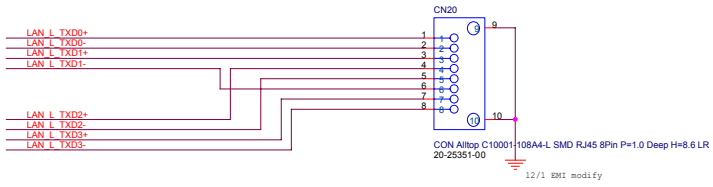


Xa: Transformer use LFE9248(12-01904-01)
Pa: Transformer use LFE8450(12-01905-01)



	for 88E8055	for 88E8039
Rc	STUFF	NU
La	STUFF	NU





(41) AVDD AVDD

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Size	Document Number	Rev
C	TRANSFORMER	0.4

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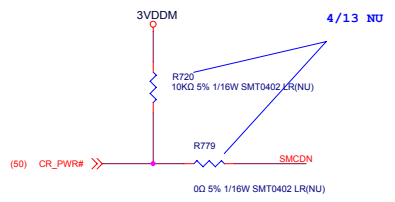
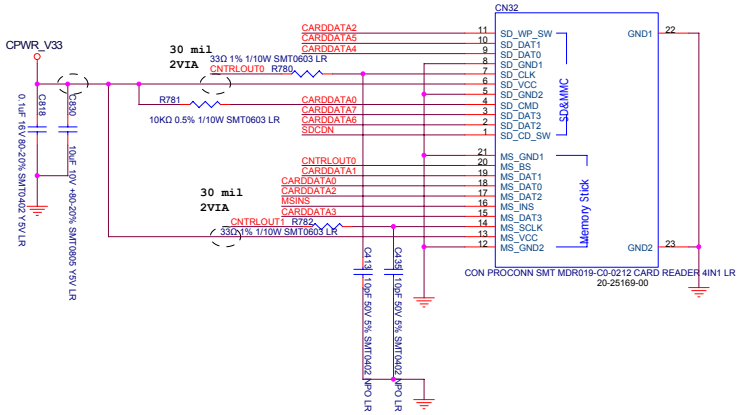
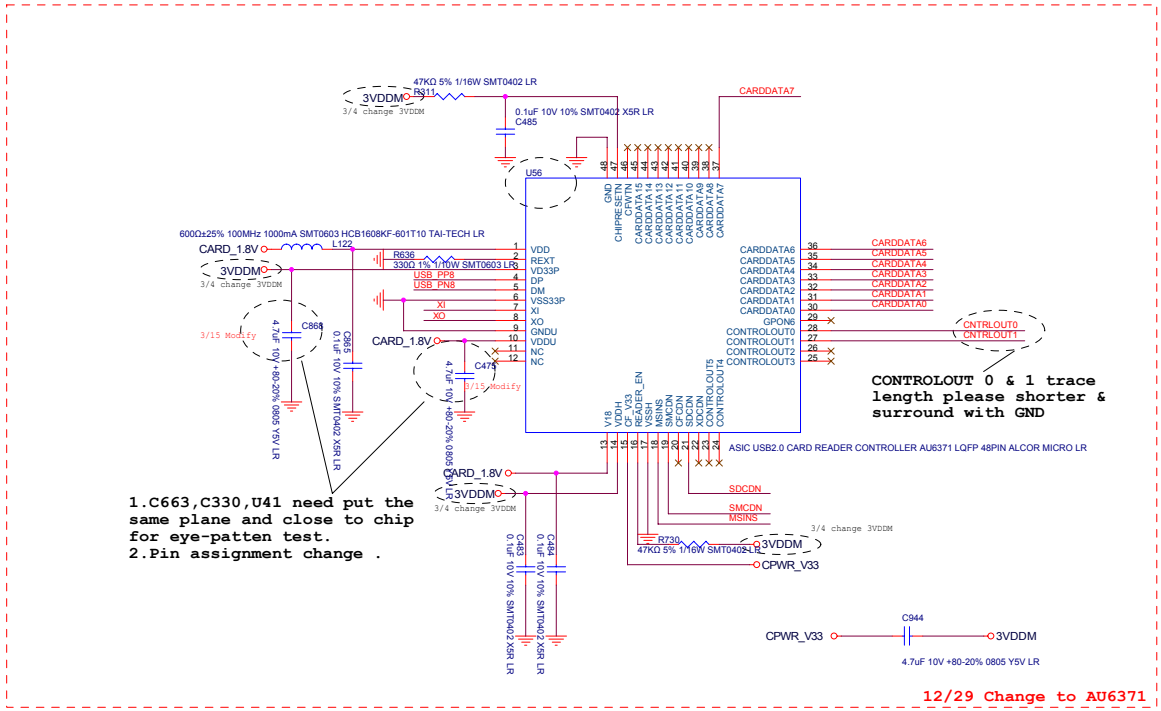
Pa: Stuff
Xa: No Stuff

Card control power solution

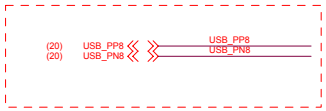


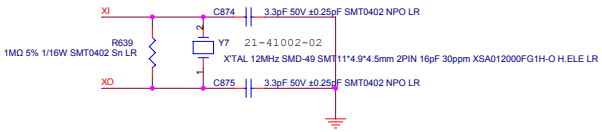
11/21 modify connector





INTERFACE





(8,11,12,13,16,17,18,19,20,21,22,23,27,28,30,32,33,34,36,37,38,40,44,45,49,50,52,55,56,57) 3VDDM 3VDDM

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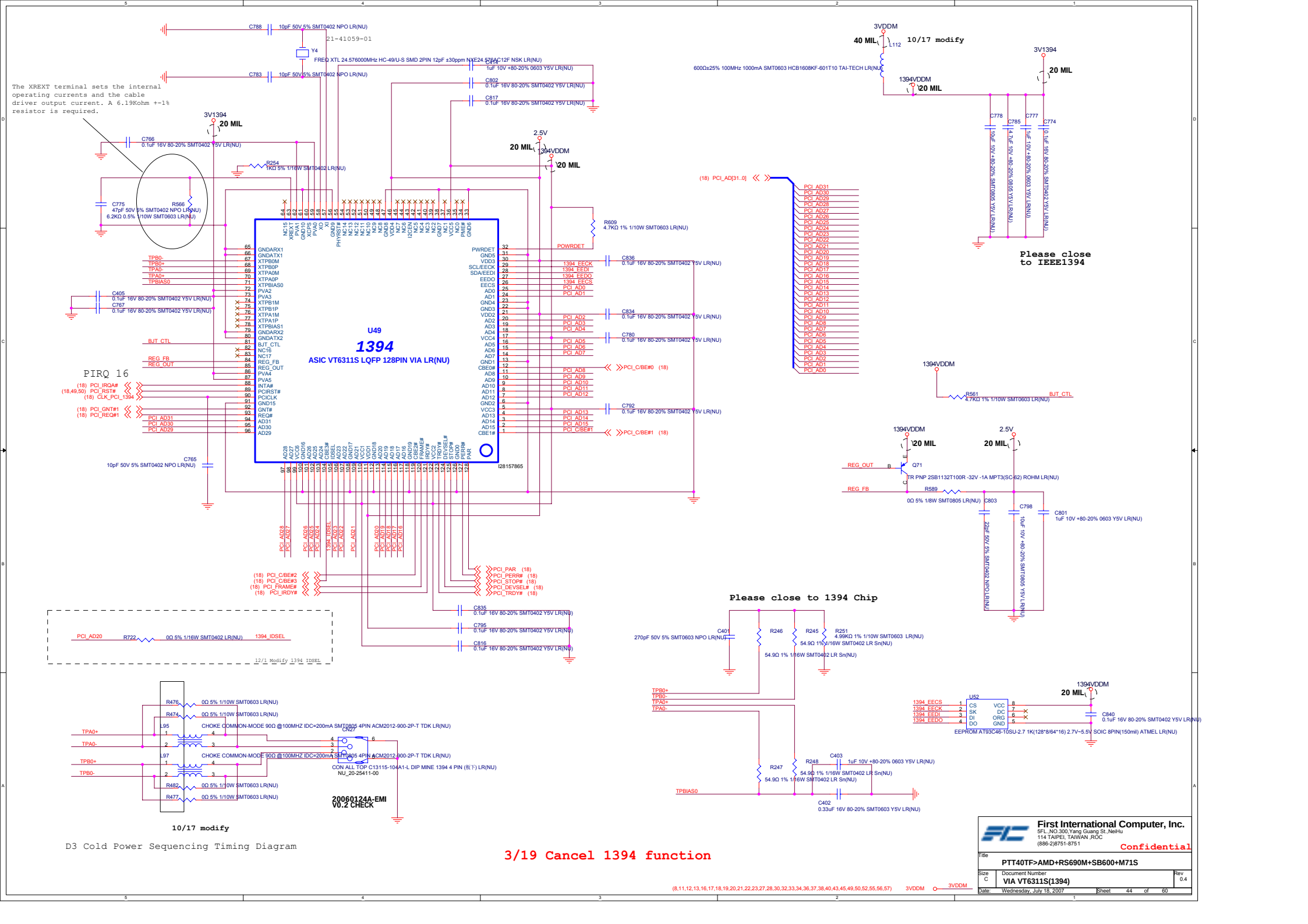
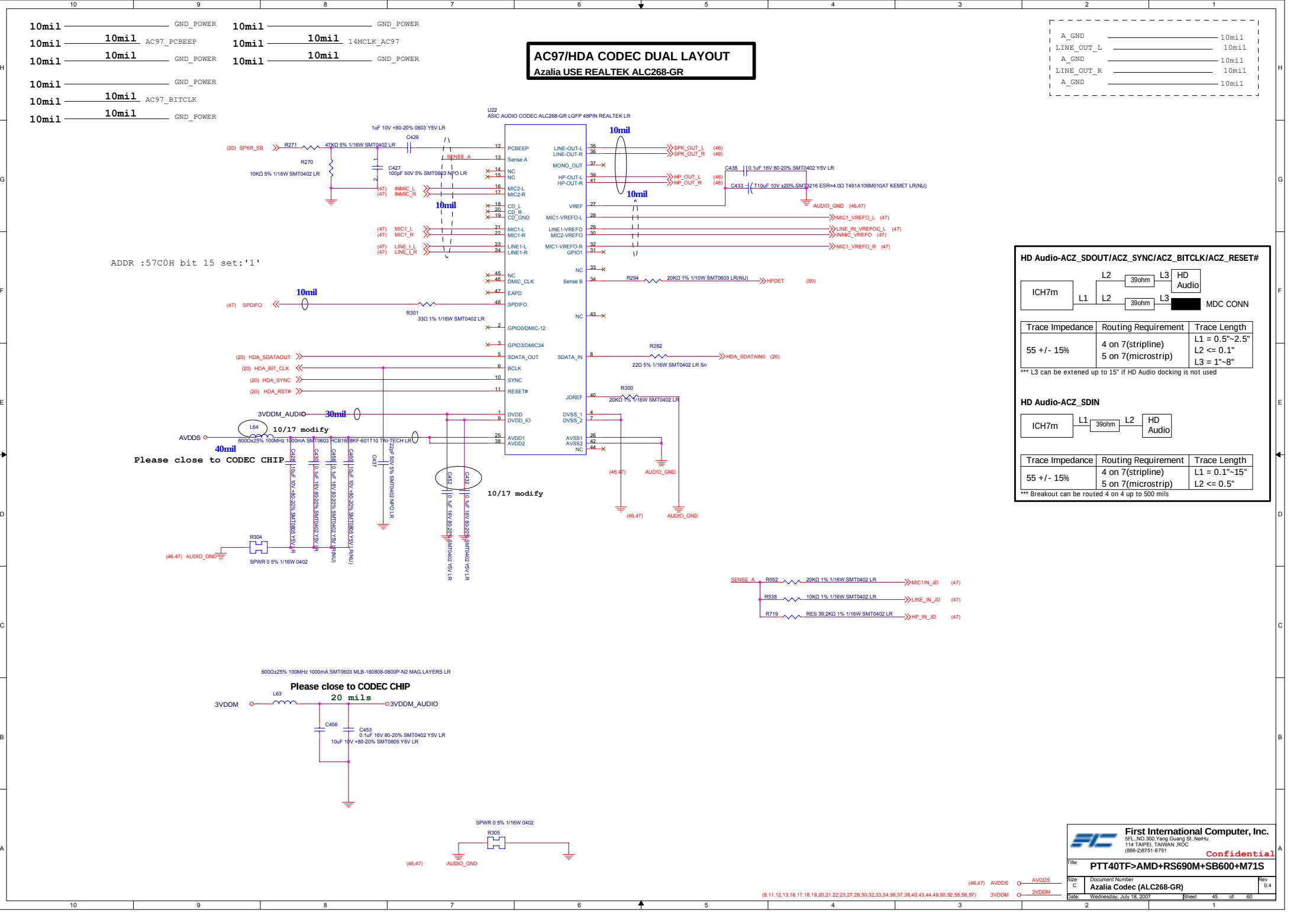
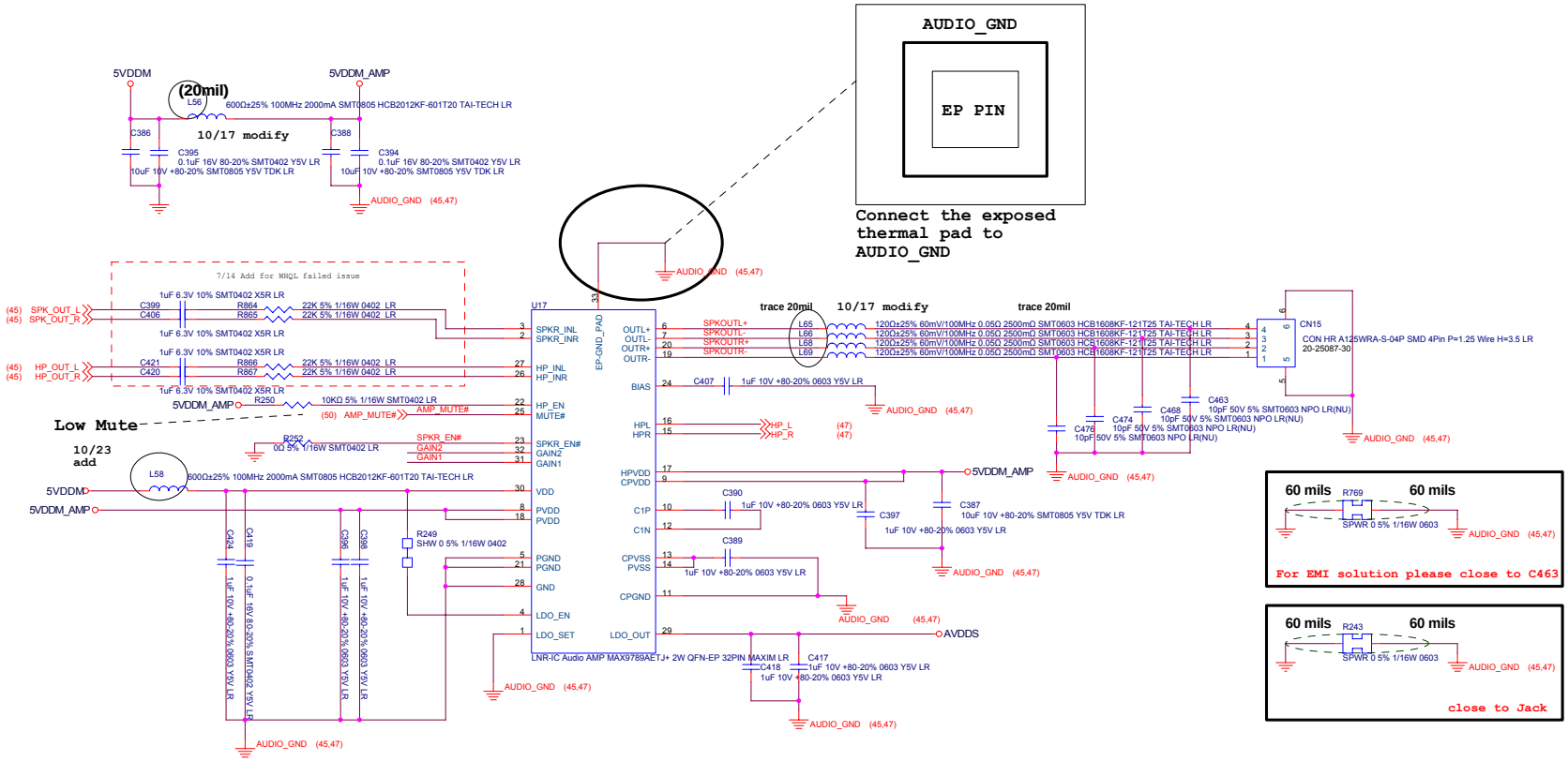
Title	PTT40TF>AMD+RS690M+SB600+M71S	
Size C	Document Number AU6366 Card Reader	Rev 0.4
Date: Wednesday, July 18, 2007	Sheet 43 of 60	


U49
1394
ASIC VT6311S LQFP 128PIN VIA LR(NU)
The XREXT terminal sets the internal operating currents and the cable driver output current. A 6.19Kohm +-1% resistor is required.
Please close to IEEE1394
Please close to 1394 Chip
PIRQ 16
10/17 modify
3/19 Cancel 1394 function
D3 Cold Power Sequencing Timing Diagram
20060124A-EMI V0.2 CHECK
First International Computer, Inc.
PTT40TF>AMD+RS690M+SB600+M71S
VIA VT6311S(1394)
Confidential
Date: Wednesday, July 18, 2007
Sheet 44 of 60

AC97/HDA CODEC DUAL LAYOUT

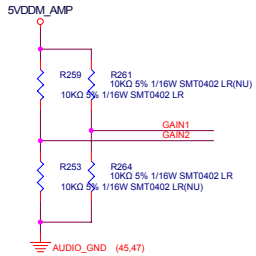
Azalia USE REALTEK ALC268-GR





SPKR_EN# = High :Disable Speaker Amplifiers

HP_EN = Low :Disable the Headphone Amplifiers



Speaker Mode gain(Max)

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

(45,47) AVDDS — AVDDS

(11,16,21,32,34,35,36,37,47,55,56) 5VDDM — 5VDDM

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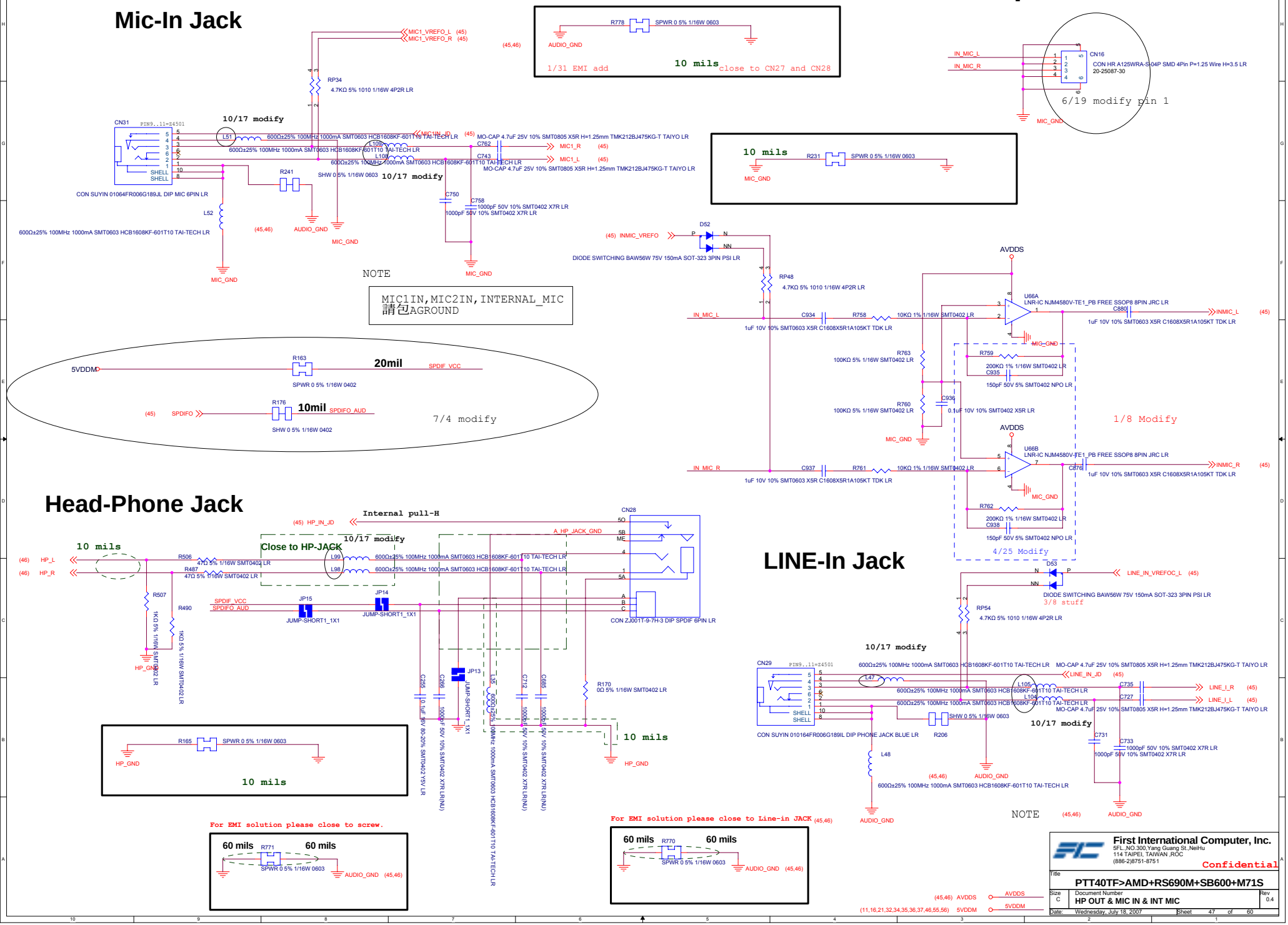
Mic-In Jack



Head-Phone Jack

LINE-In Jack

(45,46) AVDDS	AVDDS
(11,16,21,32,34,35,36,37,46,55,56) 5VDDM	5VDDM

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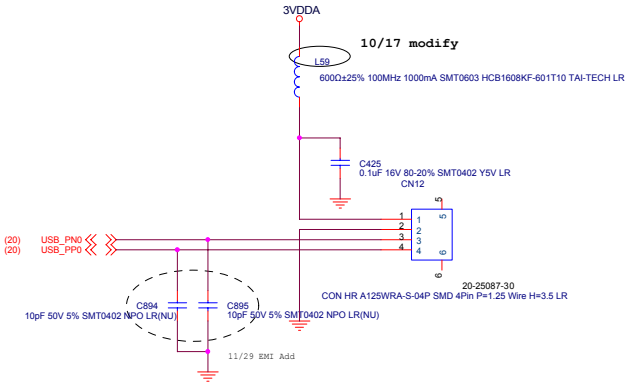
Title: PTT40TF>AMD+RS690M+SB600+M71S

Size: C | Document Number: HP OUT & MIC IN & INT MIC | Rev: 0.4

Date: Wednesday, July 18, 2007 | Sheet 47 of 60



AuthenTEC finger printer
USB Module CN

(8,11,18,19,20,21,22,24,26,33,36,40,41,49,50,53,55,56,57) 3VDDA 3VDDA

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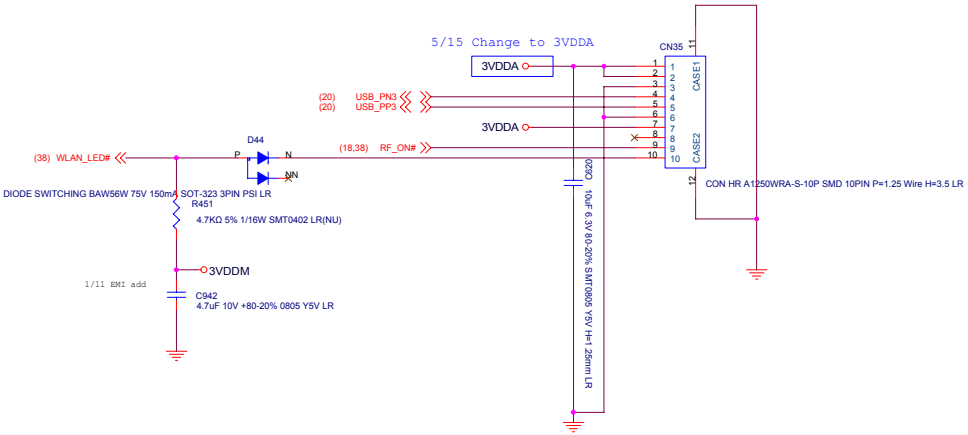
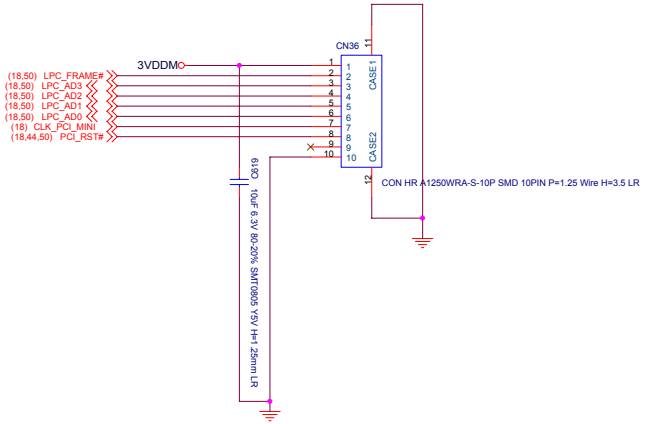
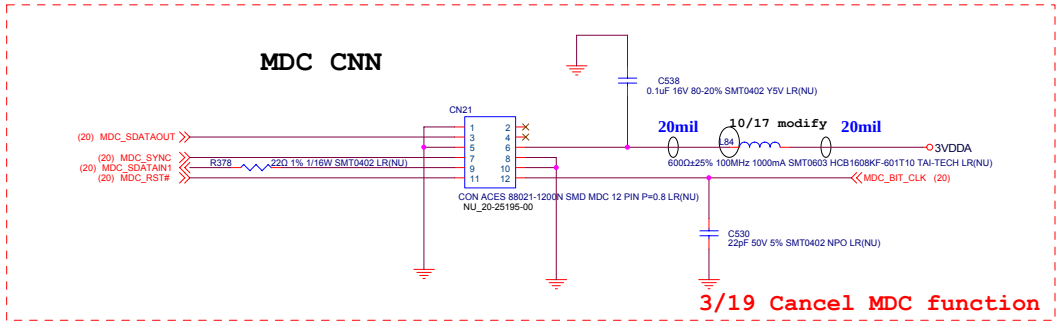
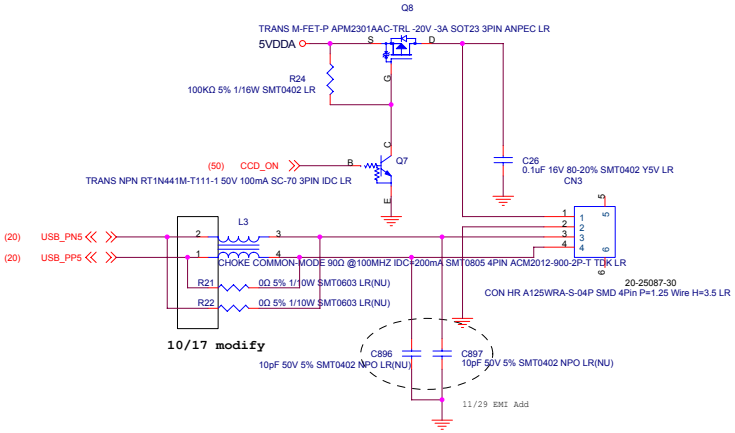
Size C	Document Number: Finger printer	Rev 0.4
Date: Wednesday, July 18, 2007	Sheet 48 of 60	

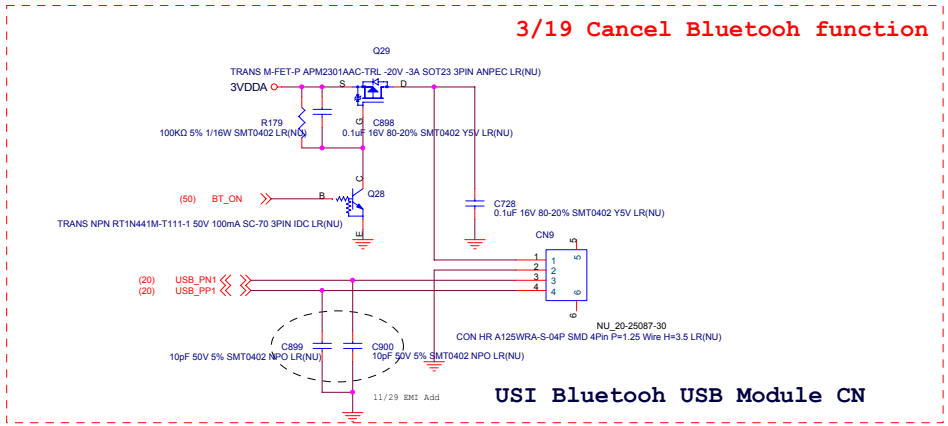
PCIE Mini Card Connector for Wireless Lan











CCD Module CN

(8,11,12,13,16,17,18,19,20,21,22,23,27,28,30,32,33,34,36,37,38,40,43,44,45,50,52,55,56,57) 3VDDM 3VDDM
(8,11,18,19,20,21,22,24,26,33,36,40,41,48,50,53,55,56,57) 3VDDA 3VDDA
(22,38,39,52,55,56,57) 5VDDA 5VDDA

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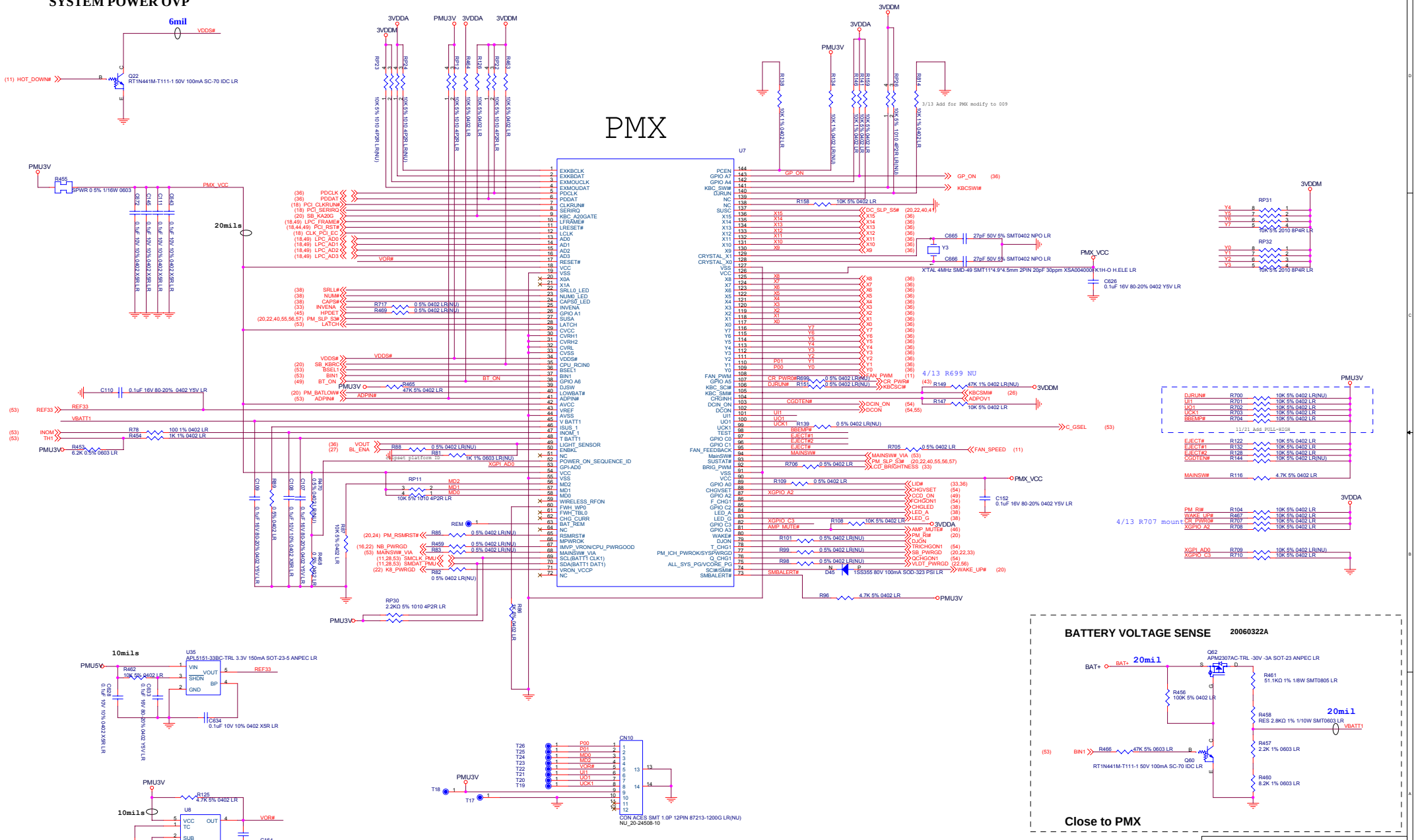
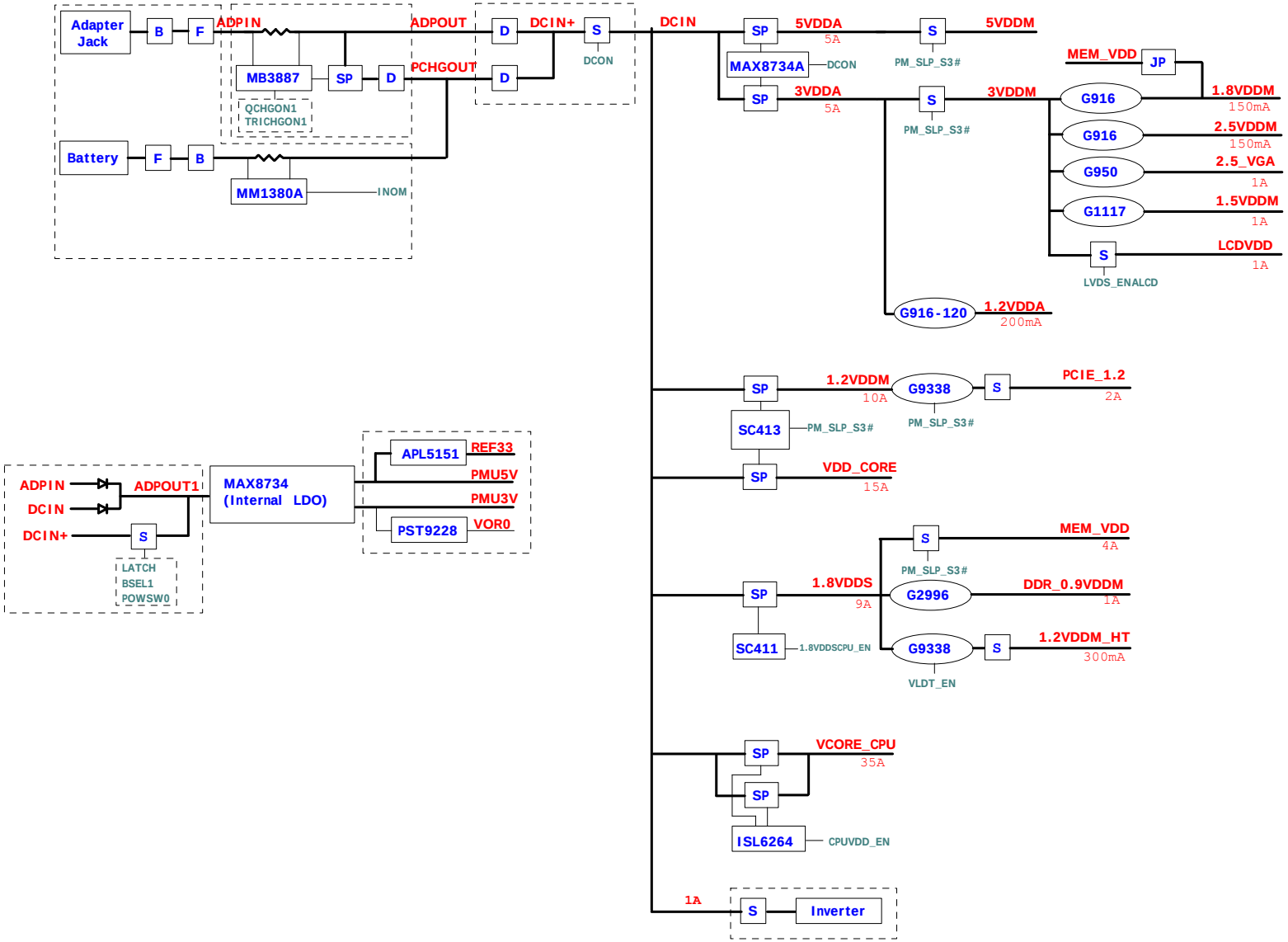
SYSTEM POWER OVP



PTT40TF Power Block



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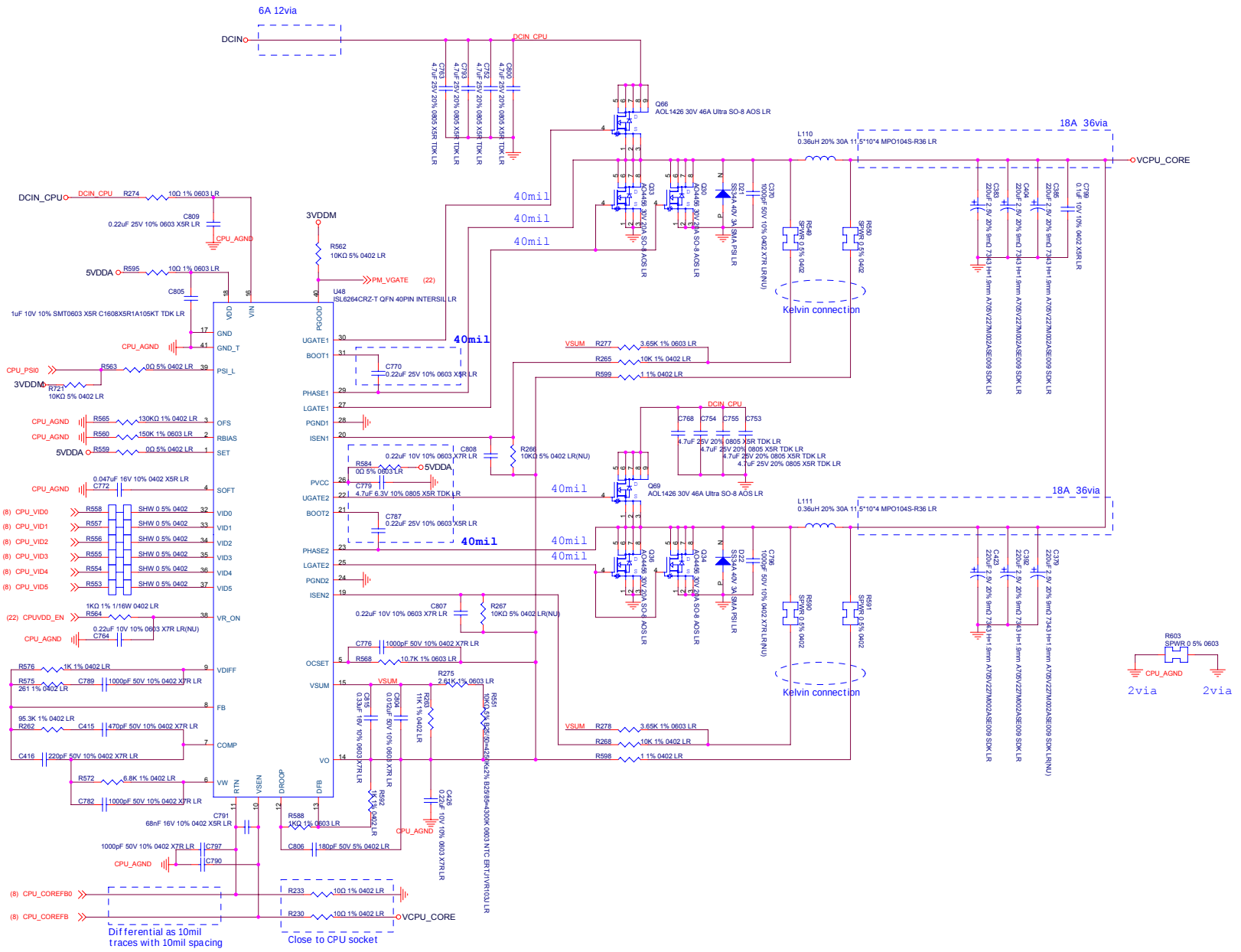
ISL6264 for AMD S1 CPU



(10) VCPU_CORE	VCPU_CORE	
(33,53,54,55,56,57) DCIN	DCIN	
(8,11,12,13,16,17,18,19,20,21,22,23,27,28,30,32,33,34,36,37,38,40,43,44,45,49,50,55,56,57) 3VDDM	3VDDM	
(22,38,39,49,55,56,57) 5VDDA	5VDDA	

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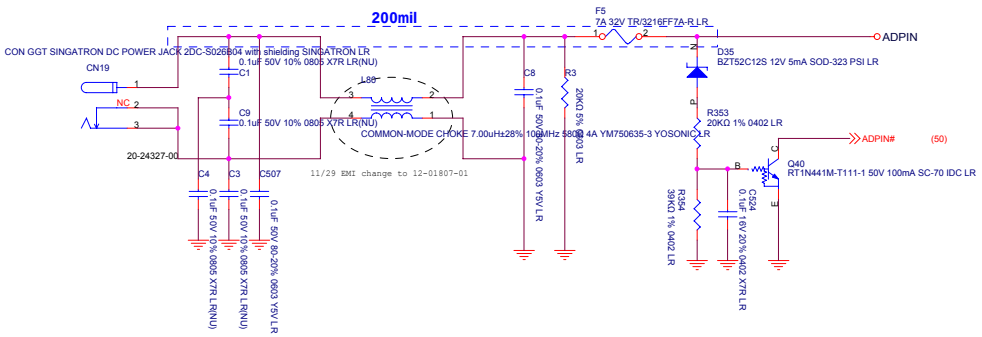
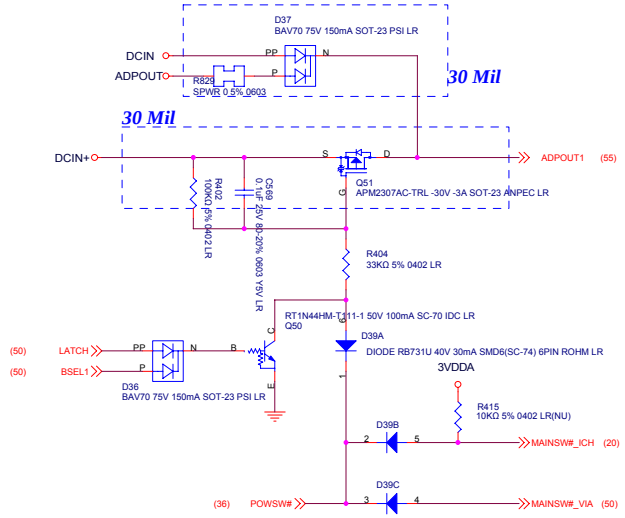
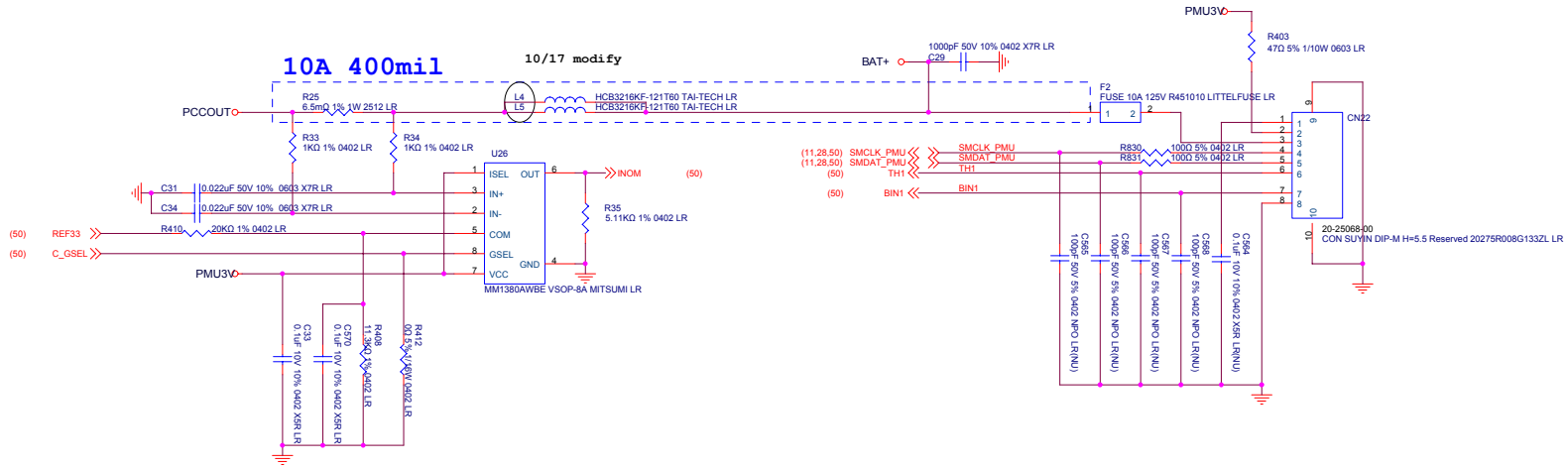
ADPIN



ADPOUT1



BATT CNN



(54)	ADPIN	ADPIN
(54)	PCCOUT	PCCOUT
(50,54)	BAT+	BAT+
(19,50,55)	PMU3V	PMU3V
(54)	ADPOUT	ADPOUT
(54)	DCIN+	DCIN+
(33,52,54,55,56,57)	DCIN	DCIN
(8,11,18,19,20,21,22,24,26,33,36,40,41,48,49,50,55,56,57)	3VDDA	3VDDA

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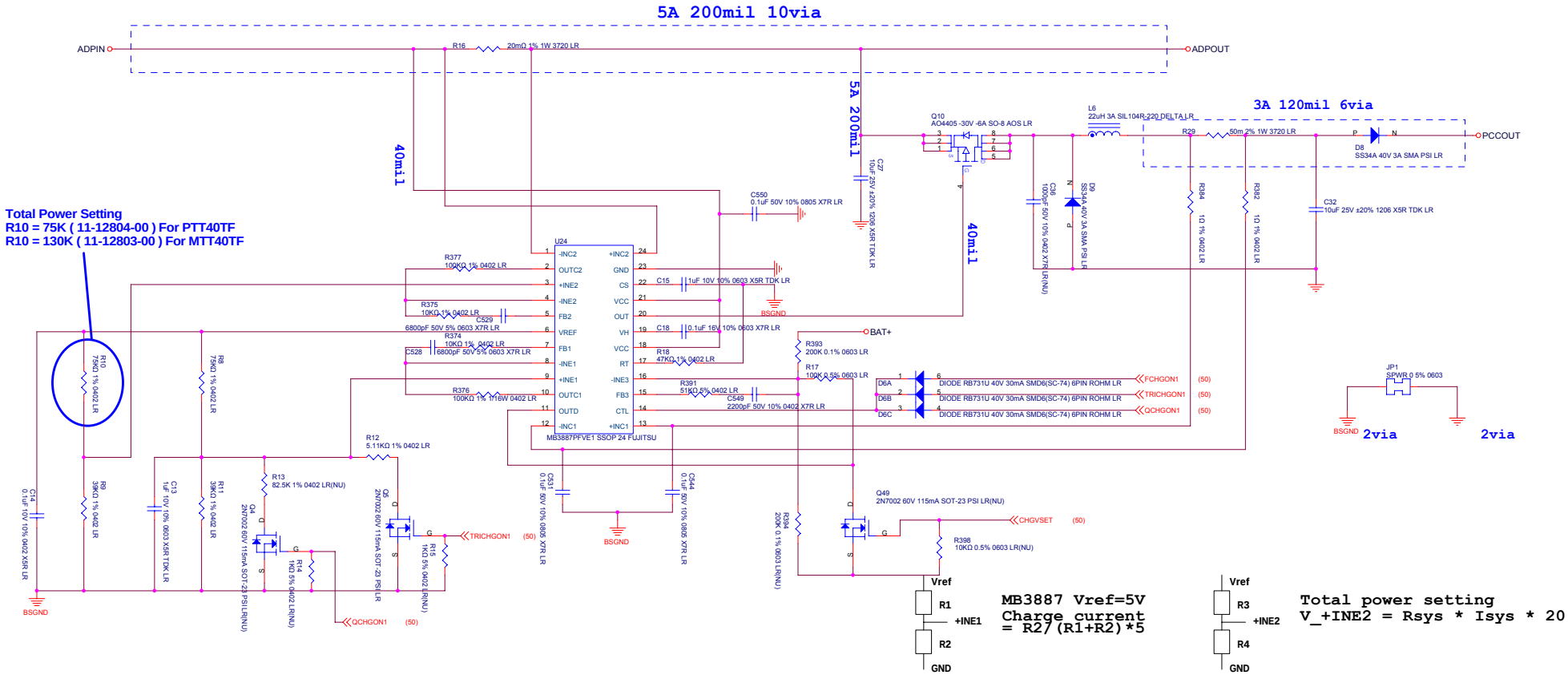
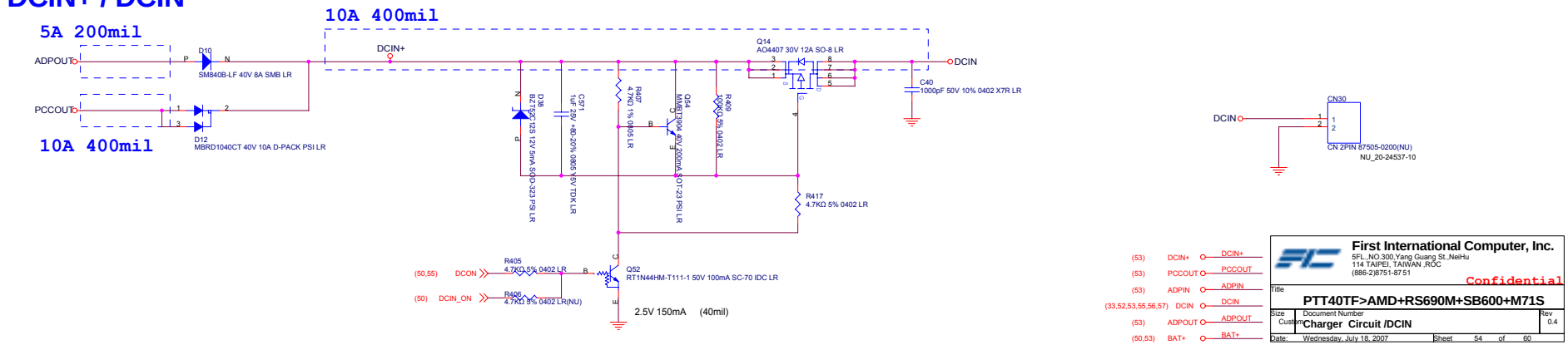
Charger



DCIN+ / DCIN



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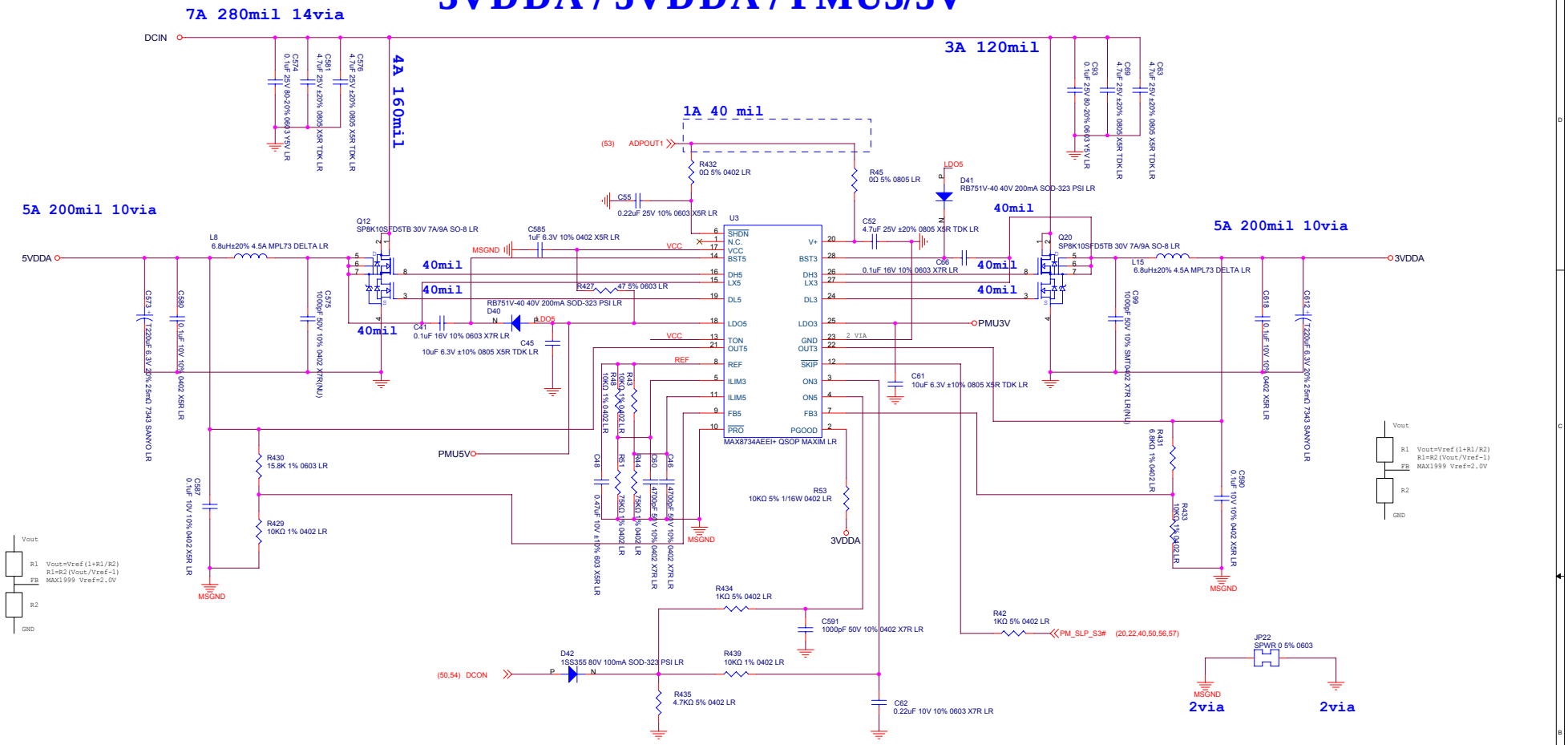
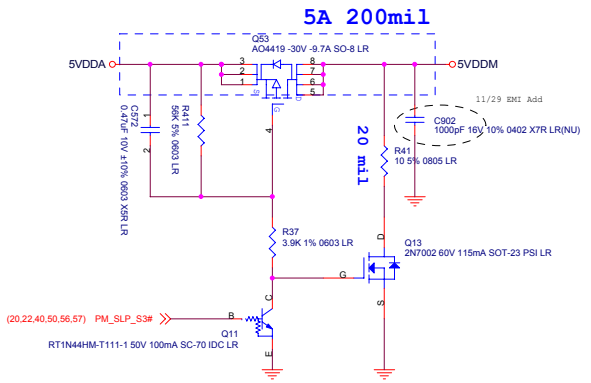
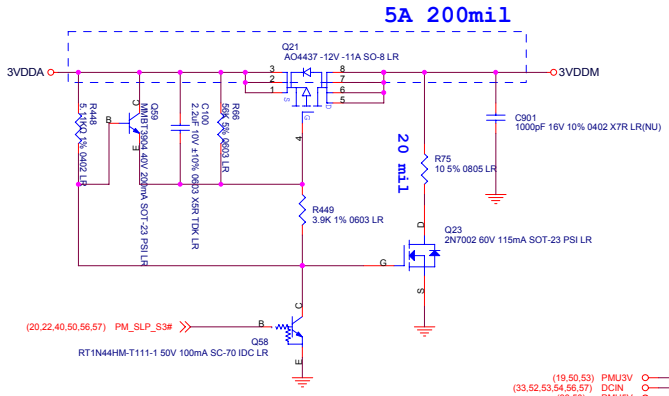
3VDDA / 5VDDA / PMU3/5V



3VDDM/5VDDM





(19,50,53) PMU3V — PMU3V
(33,52,53,54,56,57) DCIN — DCIN
(38,50) PMU5V — PMU5V
(11,16,21,32,34,35,36,37,46,47,56) 5VDDM — 5VDDM
(22,38,39,49,52,56,57) 5VDDA — 5VDDA
(8,11,12,13,16,17,18,19,20,21,22,23,27,28,30,32,33,34,36,37,38,40,43,44,45,49,50,52,56,57) 3VDDM — 3VDDM
(8,11,18,19,20,21,22,24,26,33,36,40,41,48,49,50,53,56,57) 3VDDA — 3VDDA

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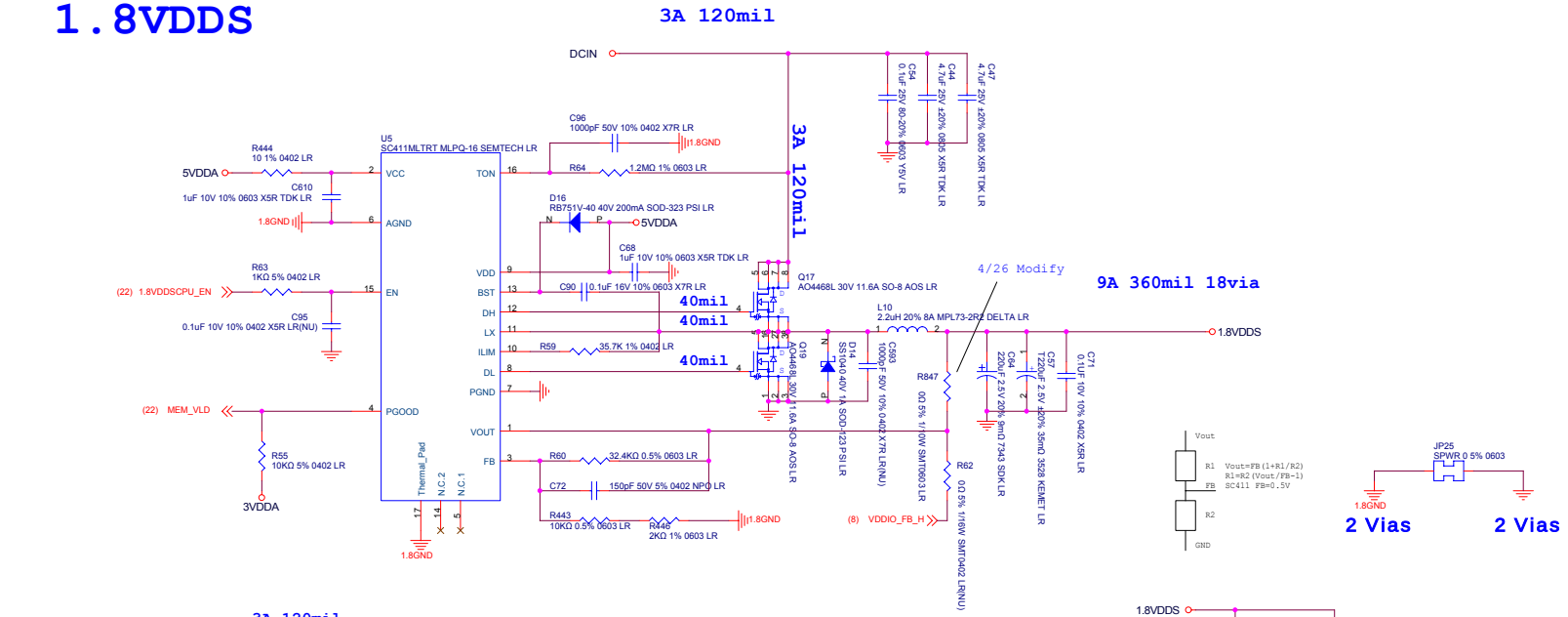
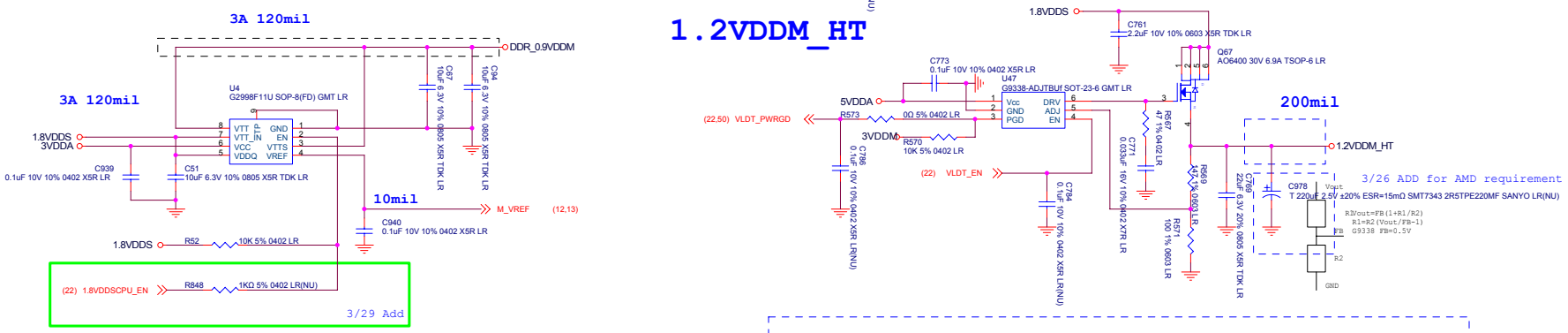
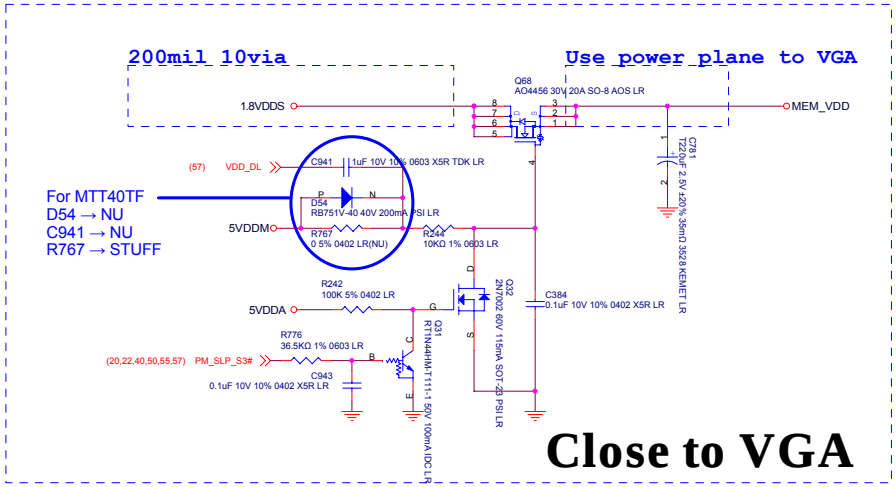
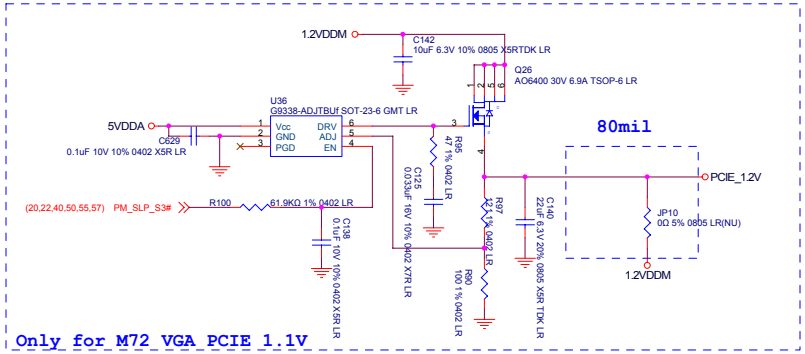
1.8VDDS



1.2VDDM_HT







(9,12,13) DDR_0.9VDDM	DDR_0.9VDDM	
(18,27,28,29,30,31,57) MEM_VDD	MEM_VDD	
(11,16,21,32,34,35,36,37,46,47,55) 5VDDM	5VDDM	
(8,11,12,13,16,17,18,19,20,21,22,23,27,28,30,32,33,34,36,37,38,40,43,44,45,49,50,52,55,57) 3VDDM	3VDDM	
(27,28,30) PCIE_1.2V	PCIE_1.2V	
(15,16,17,18,19,21,57) 1.2VDDM	1.2VDDM	
(8,17,22) 1.2VDDM_HT	1.2VDDM_HT	
(8,9,10,12,13) 1.8VDDS	1.8VDDS	
(33,52,53,54,55,57) DCIN	DCIN	
(8,11,18,19,20,21,22,24,26,33,36,40,41,48,49,50,53,55,57) 3VDDA	3VDDA	
(22,38,39,49,52,55,57) 5VDDA	5VDDA	

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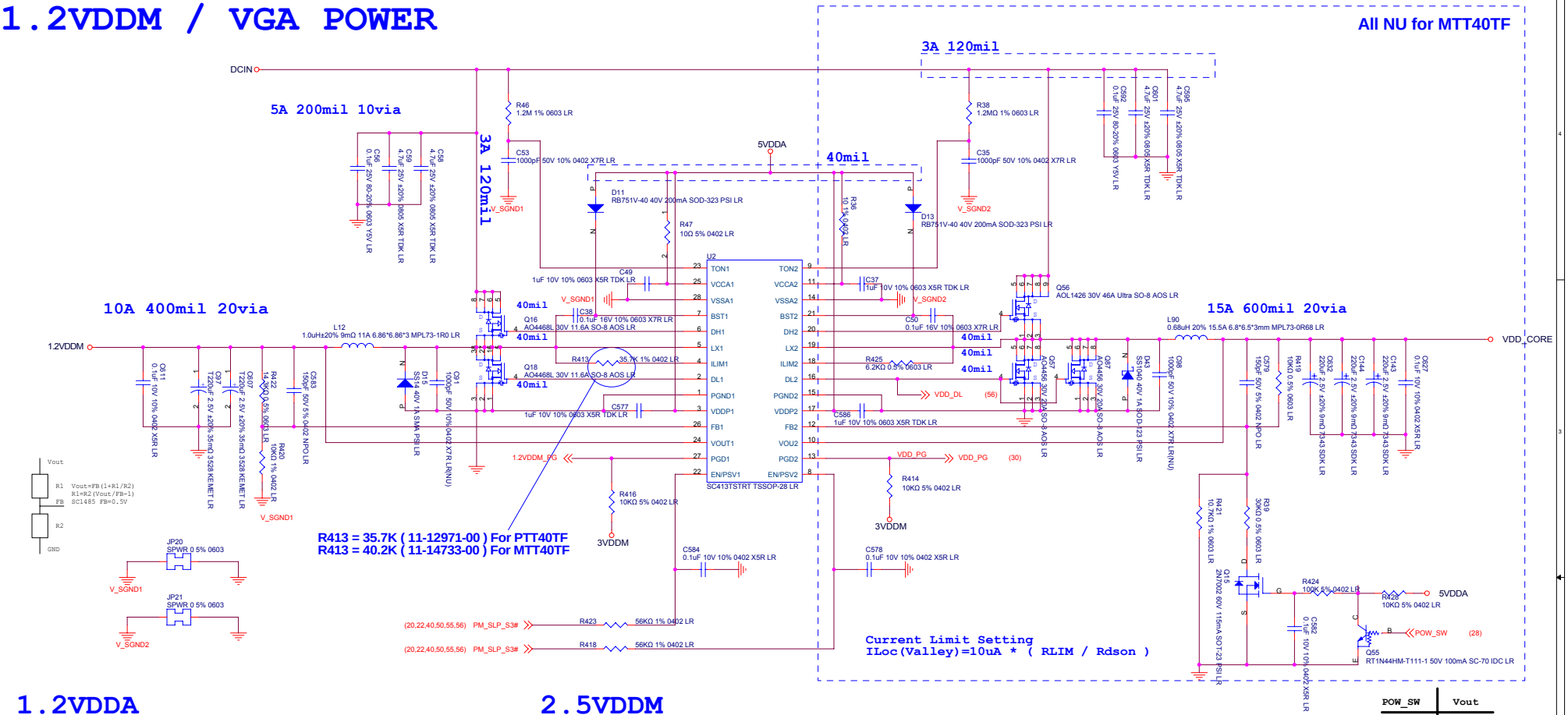
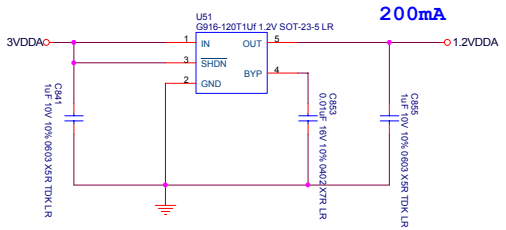
1.2VDDM / VGA POWER

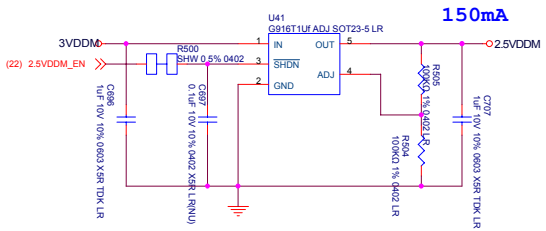


POW_SW	Vout
H	0.95V
L	1.1V

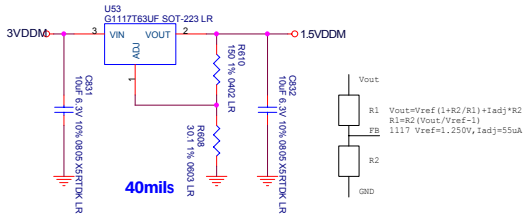
1.2VDDA



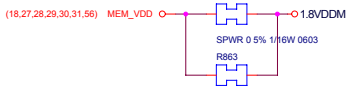
2.5VDDM

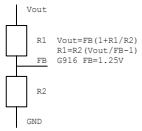


1.5VDDM



1.8VDDM





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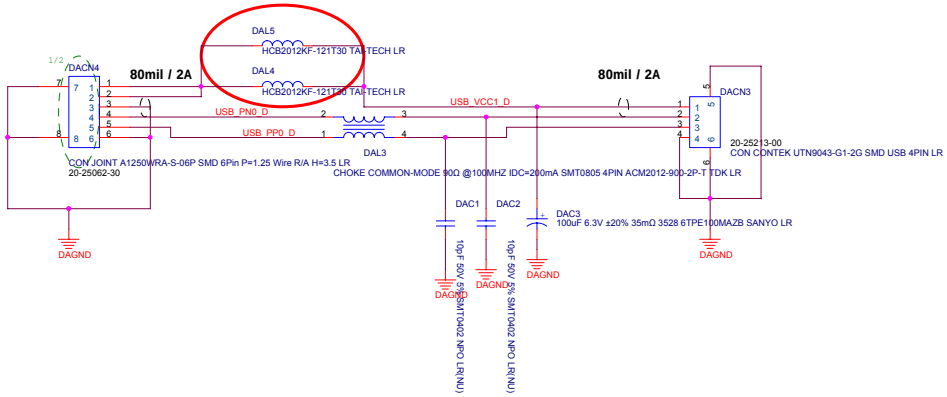
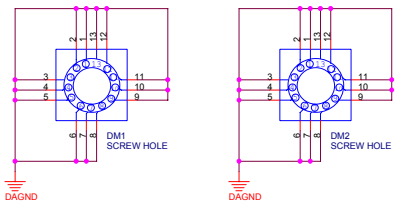
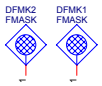
USB Board



For MDC modem





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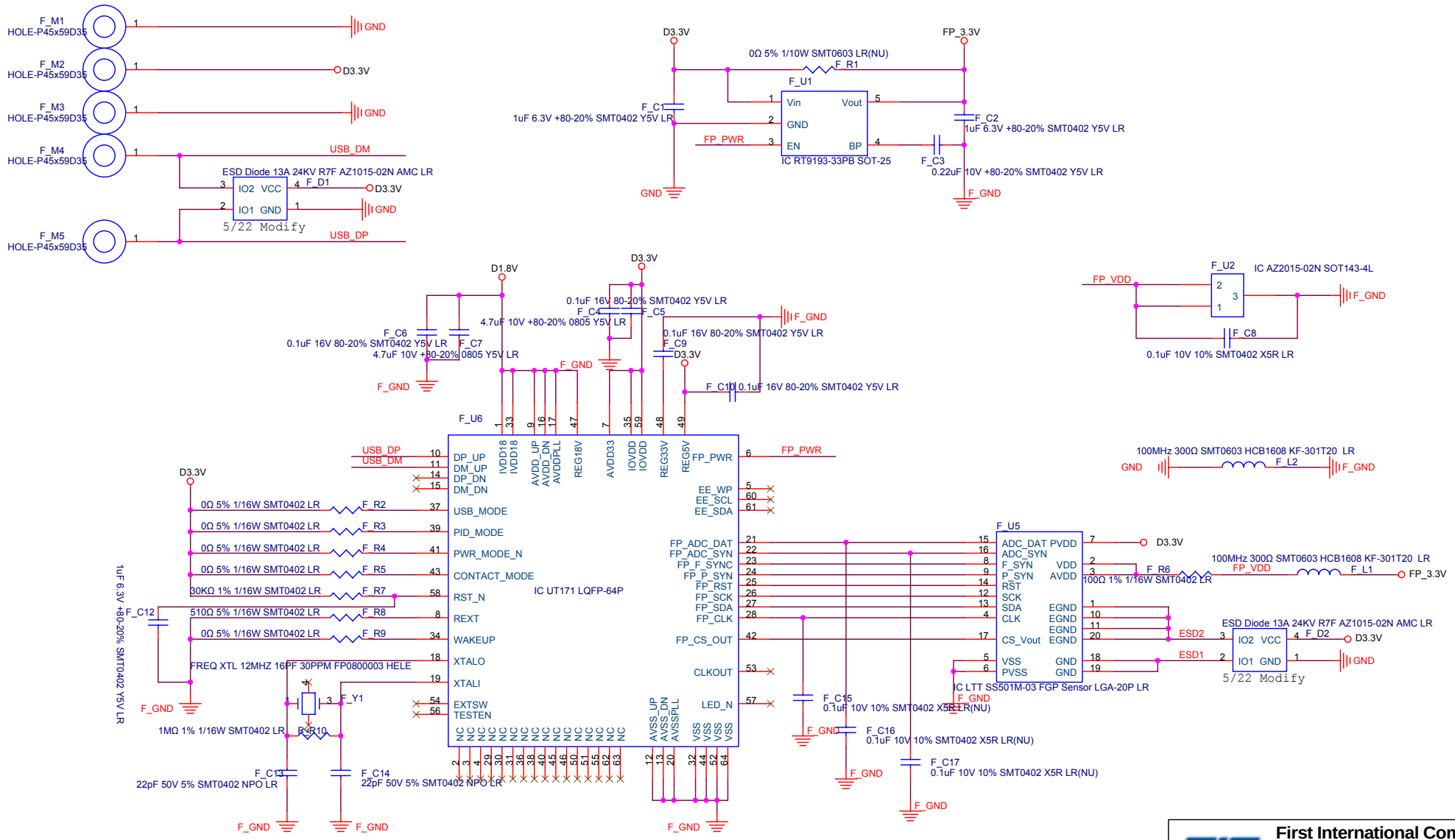

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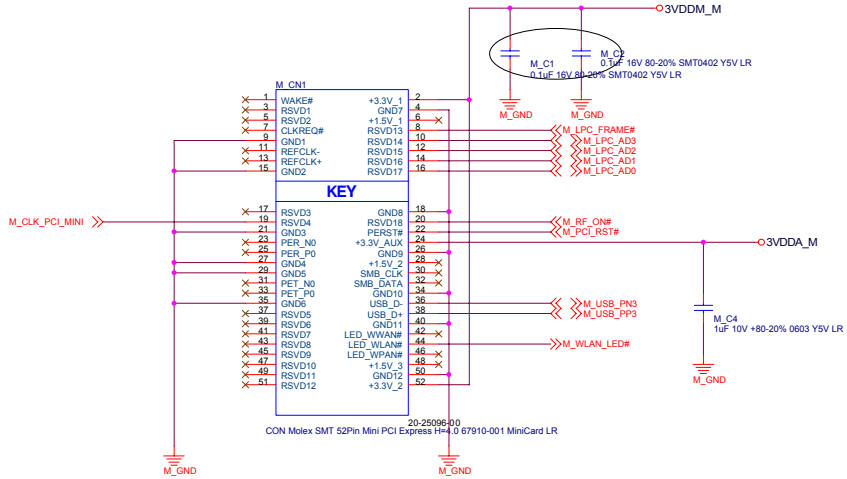
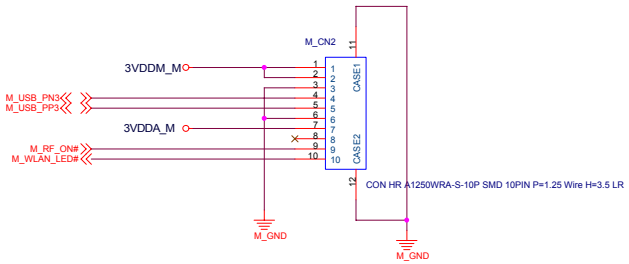
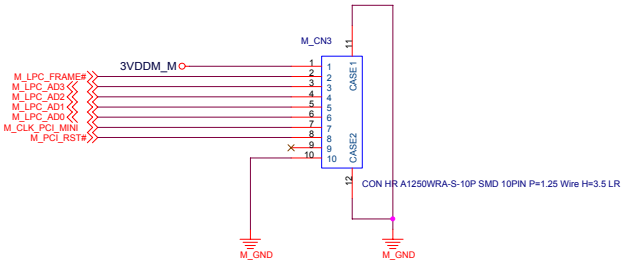
Please close to mini card
each pin

10/17 modify

PCIE Mini Card for Wireless Lan







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