Micro USB Switch with OVP and I²C Interface

General Description

The RT8973A is a USB port accessory detector and switch that is optimized to protect low voltage system from abnormal high input voltage (up to 28V). The RT8973A supports high speed USB operation and I²C interface control.

The RT8973A provides a device detection function by using the USB ID pin signal and the VBUS voltage. The ID pin resistance and VBUS voltage determine the unique characteristics for variety accessories. The host microprocessor can use I²C interface to control the switch position and read the results of the accessory detection. The RT8973A also detects USB chargers including dedicated chargers (D+/D- shorted) and high power host/hub chargers.

Features

- **Hi-Speed USB Operation**
- **UART Switch**
- **Interrupt for Device Insertion and Removal**
- **Interrupt for Protection Function**
- **Default Startup Mode for Factory Support**
- **Battery Charger Detection (BCD 1.2) Compliant**
- **28V Maximum Rating for DC Adapter**
- **Integrated Over-Voltage and Over-Current Protection FET On VBUS for Fault Isolation**
- **I²C Controlled Interface**

Applications

- Cellular Phone
- Smart Handheld Device

Ordering Information

RT8973A□

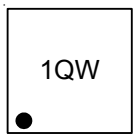
Package Type
WSC : WL-CSP-18B 1.27x2.47 (BSC)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

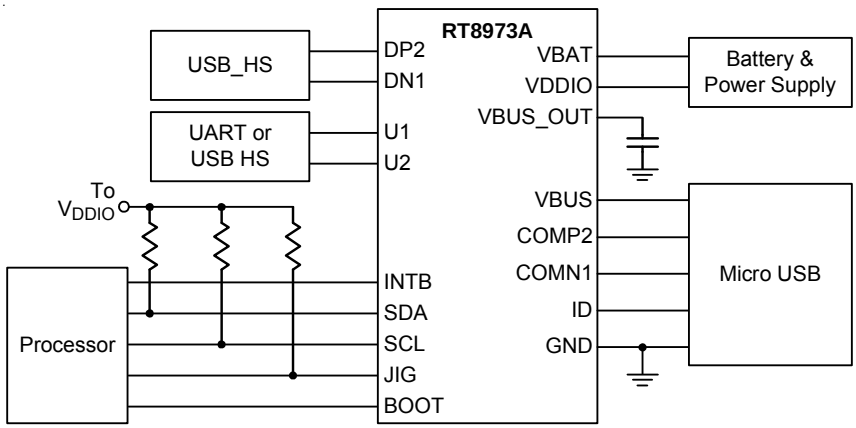
Marking Information



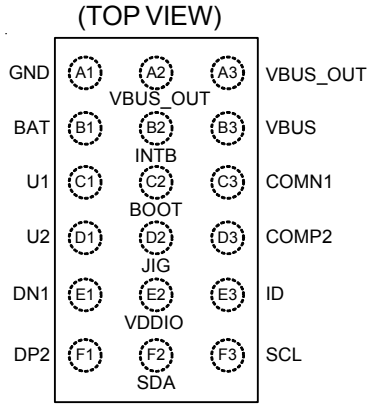
1Q : Product Code

W : Date Code

Simplified Application Circuit



Pin Configuration

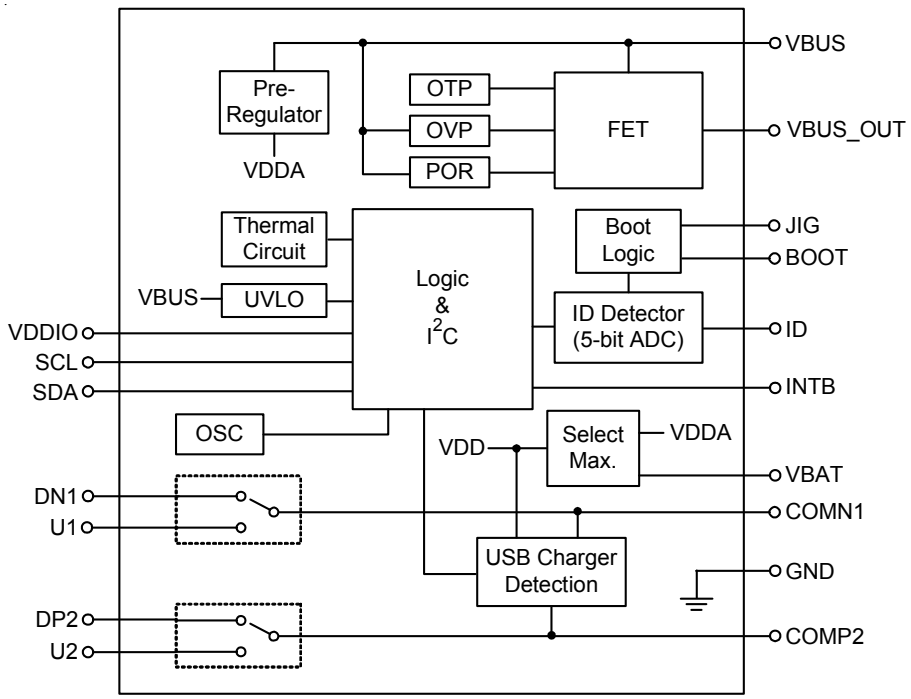


WL-CSP-18B 1.27x2.47 (BSC)

Functional Pin Description

Pin No.	Pin Name	Pin Function
A1	GND	Ground.
A2, A3	VBUS_OUT	Output through the power MOSFET.
B1	VBAT	Connected to battery.
B2	INTB	Interrupt to host (push-pull).
B3	VBUS	Connected to USB receptacle.
C1	U1	UART port.
C2	BOOT	BOOT mode out (push-pull).
C3	COMN1	USB D- port connected to USB receptacle.
D1	U2	UART port.
D2	JIG	JIG detection (open drain).
D3	COMP2	USB D+ port connected to USB receptacle.
E1	DN1	USB DN port connected to host.
E2	VDDIO	I/O voltage reference.
E3	ID	USB ID port connected to USB receptacle.
F1	DP2	USB DP port connected to host.
F2	SDA	I^2C serial data input/output. Connect an external pull up resistor.
F3	SCL	I^2C serial clock input. Connect an external pull up resistor.

Functional Block Diagram



Operation

The RT8973A is a USB port accessory detector and switch of USB and UART. The OVP function is optimized to protect low voltage system from abnormal high input voltage (up to 28V). The RT8973A supports accessory detection function through the unique characteristics from VBUS voltage, ID resistance and USB data line status.

The RT8973A is programmable by I^2C interface and it can communicate with microprocessor.

Absolute Maximum Ratings (Note 1)

- VBUS to GND ---------- –0.3V to 28V
- Other Pins to GND ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WL-CSP-18B 1.27x2.47 (BSC) ---------- 2.2W
- Package Thermal Resistance (Note 2)
  WL-CSP-18B 1.27x2.47 (BSC), θ_{JA} ---------- 45.4°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Battery Supply Voltage, VBAT ---------- 2.8V to 5.5V
- USB Supply Voltage, VBUS ---------- 4.3V to 6.7V
- Processor Supply Voltage, VDDIO ---------- 1.8V to 3.6V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{BAT} = 3.7V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DC Characteristics						
VBUS UVP Voltage	V_{UVP}		3.5	3.7	3.9	V
OTP	T_{OTP}	(Note 5)	--	135	--	°C
OTP Hysteresis	T_{OTP_H}	(Note 5)	--	10	--	°C
VBAT UVLO	$V_{VBATUVLO}$		1.1	1.8	2.1	V
VBAT Supply Current	I_{VBAT_S}	V_{BAT} = 4.2V, V_{BUS} = 0V, ID = OPEN, and ADC_EN = 1	--	25	--	μA
VBAT Leakage Current	I_{VBAT_L}	V_{BAT} = 4.2V, V_{BUS} = 0V, ID = OPEN, and ADC_EN = 0	--	10	15	μA
VBUS Supply Current	I_{VBUS_S}	V_{BAT} = 4.5V, V_{BUS} = 5V, ID = OPEN, and ADC_EN = 1	--	700	--	μA
VDDA	V_{DDA}	V_{BUS} = 5V	--	4.5	--	V
Battery Charging Spec.						
VDP_SRC Voltage	V_{DP_SRC}	With I_{DAT_SRC} = 0 to 250μA	0.5	--	0.7	V
VDAT_REF Voltage	V_{DAT_REF}		0.25	--	0.4	V
VLGC Voltage	V_{LGC}		0.8	--	2	V
DN Sink Current	I_{DN_SINK}	May be a resistance if desired	50	--	150	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
USB Analog Switch (DN1, DP2)						
Analog Signal Range	V_{DN}, V_{DP}		0	--	V_{DDA}	V
On-Resistance	R_{ON_USB}	V_{BAT} = 4.2V, I_{COM} = 10mA, V_{COM} = 0.75V	--	7.5	--	Ω
On-Resistance Match Between Channels	ΔR_{ON_USB}	V_{BAT} = 4.2V, I_{COM} = 10mA, V_{COM} = 400mV	--	0.5	--	Ω
Off Leakage Current	$I_{USB(OFF)}$	V_{BAT} = 4.2V, switch open, V_{DN1} or V_{DP2} = 0.3V, 2.5V, V_{COM} = 2.5V, 0.3V	–360	--	360	nA
On Leakage Current	$I_{USB(ON)}$	V_{BAT} = 4.2V, switch closed, V_{DN1} or V_{DP2} = 0.3V, 2.5V	–360	--	360	nA
UART/USB Analog Switch (U1, U2)						
Analog Signal Range	V_{U1}, V_{U2}		0	--	V_{DDA}	V
On-Resistance	R_{ON_UART}	V_{BAT} = 4.2V, I_{COM} = 10mA, V_{COM} = 0V to 3V	--	7.5	--	Ω
On-Resistance Match Between Channels	ΔR_{ON_UART}	V_{BAT} = 4.2V, I_{COM} = 10mA, V_{COM} = 1.5V	--	0.5	--	Ω
Off Leakage Current	I_{UART_OFF}	V_{BAT} = 4.2V, switch open, V_{U1} or V_{U2} = 0.3V, 2.5V, V_{COM} = 2.5V, 0.3V	–360	--	360	nA
On Leakage Current	I_{UART_ON}	V_{BAT} = 4.2V, switch closed, V_{U1} or V_{U2} = 0.3V, 2.5V	–360	--	360	nA
Digital Signals (INTB, SCL, SDA)						
Input Voltage, Logic-High	V_{IH}		1.4	--	--	V
Input Voltage, Logic-Low	V_{IL}		--	--	0.4	V
Input Leakage Current	I_{INLEAK}		–1	--	1	μA
Open Drain Low	V_{ODOL}	I_{SINK} = 1mA	--	--	0.4	V
Dynamic						
I^2C Max Clock	F_{I^2CCLK}		--	--	400	kHz
Analog Switch Turn-On Time	t_{ON}	I^2C stop to switch on; R_L = 50Ω	--	--	1	ms
Analog Switch Turn-Off Time	t_{OFF}	I^2C stop to switch off; R_L = 50Ω	--	--	1	ms
Break-Before-Make Delay Time	t_D	R_L = 50Ω	>0	--	--	μs
VDAT_SRC On-Time	$t_{DP\_SRC\_ON}$		40	--	--	ms
FET On Path						
VBUS POR Threshold Only for VBUS_OUT	V_{POR}	Rising	2.5	2.7	2.9	V
VBUS POR Hysteresis Only for VBUS_OUT	V_{POR_HYS}	Falling	--	100	--	mV
Deglitch Time of POR Only for VBUS_OUT	t_{POR}	Rising	--	300	--	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VBUS OVP Threshold Voltage	V_{OVP}	Rising	6.6	6.8	7	V
VBUS OVP Hysteresis	V_{OVP_HYS}	Falling	--	60	100	mV
VBUS OVP Propagation Delay to Turn-Off VBUS_OUT	t_{OVP_PD}	V_{BUS} = 5V to 10V	--	--	2	μs
VBUS OVP Recover Delay	t_{OVP_RD}	V_{BUS} = 10V to 5V	--	8	--	ms
Deglitch Time of OVP for 0x03 OVP	t_{OVP_D}	Rising	--	128	--	μs
OCP Threshold Current	I_{OCP}		2.3	2.5	2.7	A
OCP Blanking Time	t_{OCP_B}		--	180	--	μs
OCP Recover Delay	t_{OCP_RD}		--	64	--	ms
OTP Threshold to Turn-Off Only for VBUS_OUT	T_{OTP_FET}	Rising (Note5)	--	140	--	°C
OTP Threshold Hysteresis Only for VBUS_OUT	$T_{OTP\_FET\_HYS}$		--	20	--	°C
OTP Recover Delay	t_{OTD_FET}		--	8	--	ms
Soft-Start Time	t_{SS}		--	8	--	ms
FET On-Resistance	R_{ONFET}	I_{BUS_OUT} = 1000mA, 4.3V < V_{BUS} < 6.5V	--	100	200	mΩ

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

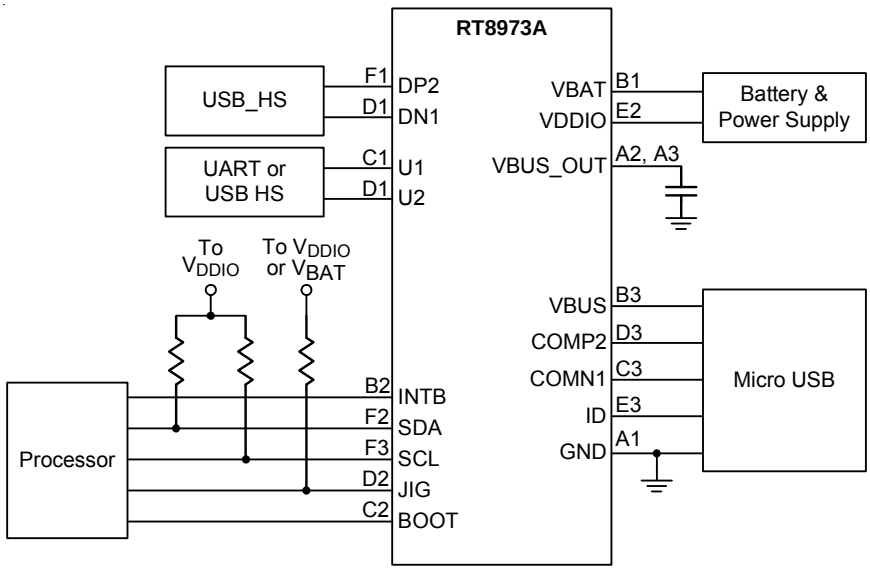
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

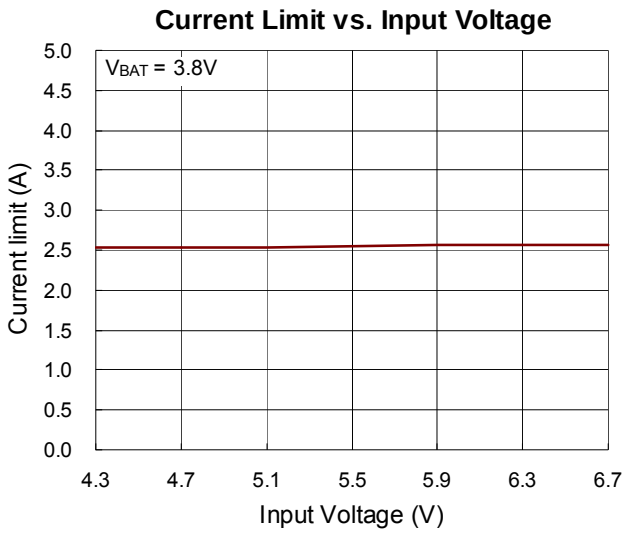
Note 4. The device is not guaranteed to function outside its operating conditions.

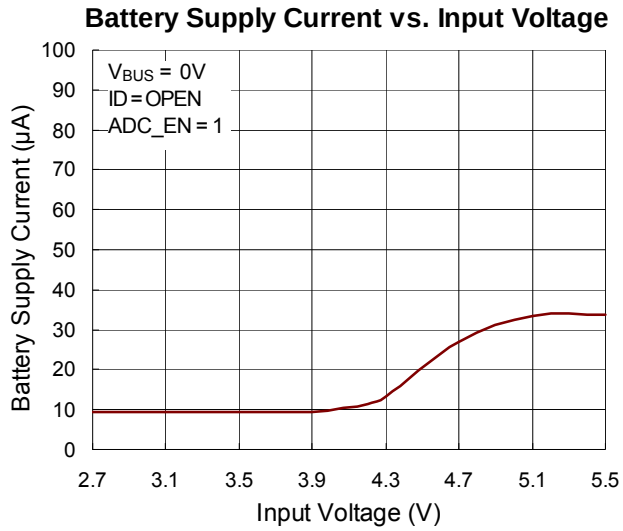
Note 5. Guaranteed by design.

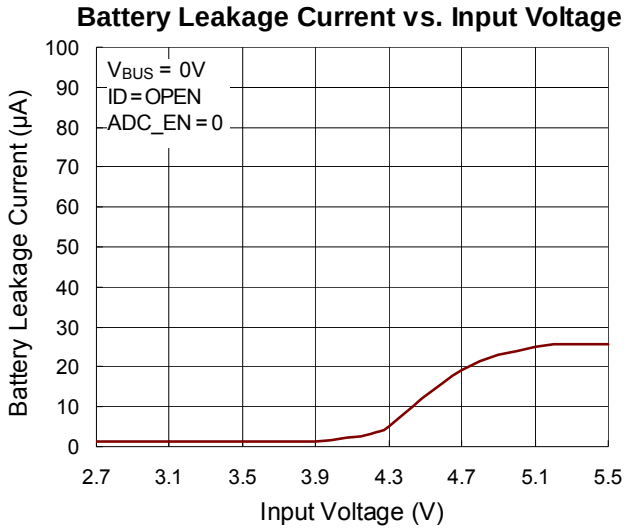
Typical Application Circuit

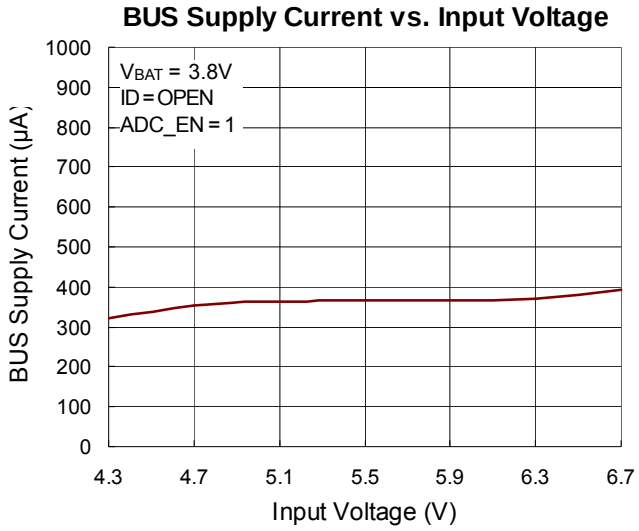


Typical Operating Characteristics









Application Information

Device Identification

The RT8973A supports multiple accessories by detecting unique characteristics including VBUS voltage, ID resistance and USB data line status. These characteristics are shown in Tables 1 to 3.

Table 1. ID Accessory Detection

ADC Code					V_{BUS} (V)	Equivalent R_{ID}			Description
4	3	2	1	0		Min.	Target	Max.	
0	0	0	0	0	N/A	--	0	--	OTG
0	0	0	0	1	N/A	1.9kΩ	2kΩ	2.1kΩ	Audio Send_End Button
0	0	0	1	0	N/A	2.5kΩ	2.6kΩ	2.7kΩ	Audio Remote S1 Button
0	0	0	1	1	N/A	3.1kΩ	3.2kΩ	3.3kΩ	Audio Remote S2 Button
0	0	1	0	0	N/A	3.9kΩ	4.01kΩ	4.1kΩ	Audio Remote S3 Button
0	0	1	0	1	N/A	4.7kΩ	4.82kΩ	5.0kΩ	Audio Remote S4 Button
0	0	1	1	0	N/A	5.8kΩ	6.03kΩ	6.2kΩ	Audio Remote S5 Button
0	0	1	1	1	N/A	7.8kΩ	8.03kΩ	8.3kΩ	Audio Remote S6 Button
0	1	0	0	0	N/A	9.7kΩ	10kΩ	10.3kΩ	Audio Remote S7 Button
0	1	0	0	1	N/A	11.7kΩ	12kΩ	12.4kΩ	Audio Remote S8 Button
0	1	0	1	0	N/A	14.0kΩ	14.5kΩ	14.9kΩ	Audio Remote S9 Button
0	1	0	1	1	N/A	16.7kΩ	17.2kΩ	17.7kΩ	Audio Remote S10 Button
0	1	1	0	0	N/A	19.9kΩ	20.5kΩ	21.1kΩ	Audio Remote S11 Button
0	1	1	0	1	N/A	23.3kΩ	24.1kΩ	24.8kΩ	Audio Remote S12 Button
0	1	1	1	0	N/A	27.8kΩ	28.7kΩ	29.6kΩ	Reserved Accessory #1
0	1	1	1	1	N/A	33.0kΩ	34kΩ	35.0kΩ	Reserved Accessory #2
1	0	0	0	0	N/A	39.0kΩ	40.2kΩ	41.4kΩ	Reserved Accessory #3
1	0	0	0	1	N/A	48.4kΩ	49.9kΩ	51.4kΩ	Reserved Accessory #4
1	0	0	1	0	N/A	63.0kΩ	64.9kΩ	66.8kΩ	Reserved Accessory #5
1	0	0	1	1	N/A	77.6kΩ	80kΩ	82.4kΩ	Audio Device Type 2
1	0	1	0	0	N/A	98.9kΩ	102kΩ	105.1kΩ	Phone Powered Device
1	0	1	0	1	N/A	117.4kΩ	121kΩ	124.6kΩ	Unknown Accessory
1	0	1	1	0	N/A	145.5kΩ	150kΩ	154.5kΩ	Unknown Accessory
1	0	1	1	1	5	176.4kΩ	200kΩ	206kΩ	Travel Adapter (TA) or Car Kit Type 1 Charger
1	1	0	0	0	5	247.3kΩ	255kΩ	262.7kΩ	Factory Mode Boot OFF-USB
1	1	0	0	1	5	291.9kΩ	301kΩ	310.1kΩ	Factory Mode Boot ON-USB
1	1	0	1	0	N/A	354kΩ	365kΩ	375.9kΩ	Unknown Accessory
1	1	0	1	1	N/A	428.7kΩ	442kΩ	455.3kΩ	Unknown Accessory
1	1	1	0	0	Open	507.3kΩ	523kΩ	538.7kΩ	Factory Mode Boot OFF-UART
1	1	1	0	1	Open	600.4kΩ	619kΩ	637.6kΩ	Factory Mode Boot ON-UART
1	1	1	1	0	N/A	750kΩ	1000kΩ	1030kΩ	Unknown Accessory
1	1	1	1	1	5	3MΩ	Open	Open	USB Accessory
Not any code above						3MΩ	None of the above ranges		Unknown Accessory

Table 2. ID Factory Cable Detection

Configuration Type		COMP2	COMN1	ID			BOOT	JIG
Factory Mode Jig : UART	Boot_On	U2	U1	600kΩ	619kΩ	637kΩ	HIGH	LOW
	Boot_Off	U2	U1	507kΩ	523kΩ	538kΩ	LOW	LOW
Factory Mode Jig : USB	Boot_On	DP2	DN1	292kΩ	301kΩ	310kΩ	HIGH	LOW
	Boot_Off	DP2	DN1	247kΩ	255kΩ	262kΩ	LOW	LOW

Note : The max allowable leakage current on ID must be less than 0.05μA.

Table 3. ID and VBUS Detection Table for USB Devices

V_{BUS_IN}	D+	D–	ID resistance to GND			Accessory Detected
			Min.	Typ.	Max.	
5V	Not Checked	Not Checked	174.6kΩ	200kΩ	206kΩ	TA (travel adapter) Charger (180kΩ) and Car Kit Charger Type 1 only (200kΩ)
5V	Shorted to D–	Shorted to D+	3MΩ	Open	Open	USB Dedicated Charging Port, Travel Adapter or Dedicated Charger (DCP)
5V	DP	DN	3MΩ	Open	Open	USB Charging Downstream Port (CDP)
5V	DP	DN	3MΩ	Open	Open	USB Standard Downstream Port (SDP)

Table 4. I²C Register Information

Address : 0010100x

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x01	Device ID	Revision Number					Vendor ID		
	Reset Value	0	0	0	0	1	0	1	0
	Read/Write	R	R	R	R	R	R	R	R
0x02	Control1	ADC_EN	USBCHDEN	CHGTYP	Switch Open	I²CRST_EN	Auto Config	Reserved	INT Mask
	Reset Value	1	1	1	0	0	1	N/A	1
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x03	Interrupt	OTP	ADC_CHG	Connect	OVP	DCD_T	CHGDET	Detach	Attach
	Reset Value	0	0	0	0	0	0	0	0
	Read/Write	R	R/C	R	R	R/C	R/C	R/C	R/C
0x04	Interrupt2	OVP_OCP	OCP	OCP_LATCH	OVP_FET	OTP_FET	POR	UVLO	Reserved
	Reset Value	0	0	0	0	0	0	0	0
	Read/Write	R/C	R/C	R	R/C	R/C	R	R	R
0x05	Interrupt Mask	OTP	ADC_CHG	Connect	OVP	DCD_T	CHGDET	Detach	Attach
	Reset Value	0	0	0	0	0	0	0	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x06	Interrupt Mask2	OVP_OCP	OCP	OCP_LATCH	OVP_FET	OTP_FET	POR	UVLO	Reserved
	Reset Value	1	0	0	0	0	1	1	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x07	ADC	Reserved	Reserved	Reserved	ADC Values				
	Reset Value	N/A	N/A	N/A	1	1	1	1	1
	Read/Write	R	R	R	R	R	R	R	R
0x0A	Device 1	Reserved	DCPORT	CDPORT	Car Kit Type1	UART	SDPORT	Reserved	OTG
	Reset Value	N/A	0	0	0	0	0	N/A	0
	Read/Write	R	R	R	R	R	R	R	R
0x0B	Device 2	Unknown Accessory	Reserved	Reserved	Reserved	JIG UART OFF	JIG UART ON	JIG USB OFF	JIG USB ON
	Reset Value	0	N/A	N/A	N/A	0	0	0	0
	Read/Write	R	R	R	R	R	R	R	R

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x13	MANUAL SW1	D– Switching			D+ Switching			Reserved	Reserved
	Reset Value	0	0	0	0	0	0	N/A	N/A
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x14	MANUAL SW2	Reserved	Reserved	Reserved	Reserved	BOOT SW	JIG ON	Reserved	FET_ON
	Reset Value	N/A	N/A	N/A	N/A	0	0	N/A	1
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x1B	RESET	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RESET
	Reset Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 5. Device ID 0x00 - Read Only

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x01	Device ID	Revision Number					Vendor ID		
	Reset Value	0	0	0	0	1	0	1	0
	Read/Write	R	R	R	R	R	R	R	R
Revision Number		Rev. 1 = 00001							
Vendor ID		Richtek = 010							

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	Control1	ADC_EN	USBCHDEN	CHGTYP	Switch Open	I^2CRST _EN	Auto Config	Reserved	INT Mask
	Reset Value	1	1	1	0	0	1	N/A	1
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADC_EN		0 : Disable ID pin detection function 1 : Enable ID pin detection function							
USBCHDEN		0 : Disable USB charger detection function 1 : Enable USB charger detection function							
CHGTYP		0 : Disable 2nd detection of USB charger function 1 : Enable 2nd detection of USB charger function							
Switch Open		0 : Automatic switching by accessory status 1 : Open all switches							
I^2CRST_EN		0 : Disable I^2C pull low reset (default) 1 : Enable I^2C pull low reset (SCL & SDA = 0 > 30ms typical)							
Auto Config		0 : Manual switching 1 : Auto-configuration							
INT_mask		0 : Unmask interrupt – interrupt baseband processor on change of state in Interrupt register 1 : Mask interrupt – do not interrupt baseband processor							

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x03	Interrupt	OTP	ADC_CHG	Connect	OVP	DCT_T	CHGDET	Detach	Attach
	Reset Value	0	0	0	0	0	0	0	0
	Read/Write	R	R/C	R	R	R/C	R/C	R/C	R/C

OTP	Monitor over temperature 0 : T < 125°C 1 : T > 135°C Any change in this bit triggers an interrupt.
ADC_CHG	0 : ADC values is not changed 1 : ADC values is changed The bit will interrupt only when ADC_CHG goes from 0 to 1, and clear after Baseband reads.
Connect	0 : Switch is not connected 1 : Switch is connected Any Change in this bit triggers an interrupt.
OVP	This OVP with 128μ deglitch time 0 : VBUS over voltage is not detected 1 : VBUS over voltage is detected Any Change in this bit triggers an interrupt.
DCD_T	0 : Data Contact Detection timeout is not detected 1 : Data Contact Detection timeout is detected The bit will interrupt only when DCD_T goes from 0 to 1.
CHGDET	Output of USB charger detection. The bit will be set to “1” if COMN > VDAT_REF & COMN < VLGC 0 : COMN < VDAT_REF or COMN > VLGC (charger port is not detected) 1 : COMN > VDAT_REF & COMN < VLGC (charger port is detected) The bit will interrupt only when CHGDET goes from 0 to 1.
Detach	0 : Accessory not detached 1 : Accessory detached The bit will interrupt only when Detach goes from 0 to 1, and clear to 0 after Baseband reads.
Attach	0 : Accessory not attached 1 : Accessory attached The bit will interrupt only when Attach goes from 0 to 1, and clear to 0 after Baseband reads.

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x04	Interrupt2	OVP _OCP	OCP	OCP _LATCH	OVP_FET	OTP_FET	POR	UVLO	Reserved
	Reset Value	0	0	0	0	0	0	0	0
	Read/Write	R/C	R/C	R	R/C	R/C	R	R	R

OVP_OCP	0 : VBUS OCP AND VBUS OVP not detected 1 : VBUS OCP OR VBUS OVP detected The bit will interrupt only when OVP_OCP goes from 0 to 1, and this bit will be clear to 0 after baseband reads.
OCP	0 : VBUS OCP is not detected 1 : VBUS OCP is detected The bit will interrupt only when OCP_EN goes from 0 to 1, and this bit will be clear to 0 after baseband reads.

OCP_LATCH	0 : VBUS OCP does not occur for consecutive 16 times. 1 : VBUS OCP occurs for consecutive 16 times. FET will be turn off unless the VBUS power re-toggle or 0x14 FET_ON set 1 to 0 to 1. Any change in this bit triggers an interrupt
OVP_FET	This OVP without deglitch time 0 : VBUS over voltage is not detected 1 : VBUS over voltage is detected The bit will interrupt only when OVP_FET goes from 0 to 1, and this bit will be clear to 0 after baseband reads.
OTP_FET	This over-temperature of MOSFET 0 : T <120°C 1 : T >150°C The bit will interrupt only when OTP_FET goes from 0 to 1, and this bit will be clear to 0 after baseband reads.
POR	0 : VBUS > 2.7V with 300ms deglitch time 1 : VBUS < 2.6V Any change in this bit triggers an interrupt.
UVLO	0 : VBUS voltage is higher than VUVP voltage 1 : VBUS voltage is lower than VUVP voltage Any change in this bit triggers an interrupt.

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x05	Interrupt Mask	OTP	ADC_CHG	Connect	OVP	DCD_T	CHGDET	Detach	Attach
	Reset Value	0	0	0	0	0	0	0	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
OTP		0 : Unmask OTP interrupt 1 : Mask OTP interrupt							
ADC_CHG		0 : Unmask ADC_CHG interrupt 1 : Mask ADC_CHG interrupt							
Connect		0 : Unmask connect interrupt 1 : Mask connect interrupt							
OVP		0 : Unmask OVP interrupt 1 : Mask OVP interrupt							
DCD_T		0 : Unmask DCD_T interrupt 1 : Mask DCD_T interrupt							
CHGDET		0 : Unmask CHGDET interrupt 1 : Mask CHGDET interrupt							
Detach		0 : Unmask detach interrupt 1 : Mask detach interrupt							
Attach		0 : Unmask attach interrupt 1 : Mask attach interrupt							

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x06	Interrupt Mask2	OVP _OCP	OCP	OCP _LATCH	OV _FET	OTP _FET	POR	UVLO	Reserved
	Reset Value	1	0	0	0	0	1	1	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
OVP_OCP		0 : Unmask OVP_OCP interrupt 1 : Mask OVP_OCP interrupt							
OCP		0 : Unmask OCP interrupt 1 : Mask OCP interrupt							
OCP_LATCH		0 : Unmask OCP_LATCH interrupt 1 : Mask OCP_LATCH interrupt							
OVP_FET		0 : Unmask OVP_FET interrupt 1 : Mask OVP_FET interrupt							
OTP_FET		0 : Unmask OTP_LATCH interrupt 1 : Mask OTP_LATCH interrupt							
POR		0 : Unmask POR interrupt 1 : Mask POR interrupt							
UVLO		0 : Unmask UVLO interrupt 1 : Mask UVLO interrupt							

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x07	ADC	Reserved	Reserved	Reserved	ADC Values				
	Reset Value	N/A	N/A	N/A	1	1	1	1	1
	Read/Write	R	R	R	R	R	R	R	R
ADC		ADC Values from ID Pin Detection							

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0A	Device 1	Reserved	DCPORT	CDPORT	Car Kit Type1	UART	SDPORT	Reserved	OTG
	Reset Value	N/A	0	0	0	0	0	N/A	0
	Read/Write	R	R	R	R	R	R	R	R
DCPORT		0 : USB Dedicated Charging Port (DCP) charger not detected 1 : USB Dedicated Charging Port (DCP) charger detected							
CDPORT		0 : USB Charging Downstream Port (CDP) charger not detected 1 : USB Charging Downstream Port (CDP) charger detected							
Car Kit Type 1		0 : Car Kit Type 1 & TA not detected 1 : Car Kit Type 1 & TA detected							
UART		0 : UART cable not detected 1 : UART cable detected							
Standard USB (SDPORT)		0 : USB Standard Downstream Port (SDP) charger not detected 1 : USB Standard Downstream Port (SDP) charger detected							
OTG		0 : OTG cable not detected 1 : OTG cable detected							

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0B	Device 2	Unknown Accessory	Reserved	Reserved	Reserved	JIG UART OFF	JIG UART ON	JIG USB OFF	JIG USB ON
	Reset Value	0	N/A	N/A	N/A	0	0	0	0
	Read/Write	R	R	R	R	R	R	R	R
Unknown Accessory		0 : Unknown accessory not detected 1 : Any accessory detected as unknown or an accessory that cannot be detected as being valid							
JIG UART OFF		0 : Factory mode BOOT_OFF_UART not detected 1 : Factory mode BOOT_OFF_UART detected							
JIG UART ON		0 : Factory mode cable UART path with BOOT_ON not detected 1 : Factory mode cable UART path with BOOT_ON detected							
JIG USB OFF		0 : Factory mode cable USB path with BOOT_OFF not detected 1 : Factory mode cable USB path with BOOT_OFF detected							
JIG USB ON		0 : Factory mode cable USB path with BOOT_ON not detected 1 : Factory mode cable USB path with BOOT_ON detected							

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x13	MANUAL SW1	D– Switching			D+ Switching			Reserved	Reserved
	Reset Value	0	0	0	0	0	0	N/A	N/A
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
D– Switching		000 : Switch Open 001 : COMN1 connected to DN1 of USB port 011 : COMN1 connected to U1 or UART port All others values : do not use							
DP Switching		000 : Switch Open 001 : COMP2 connected to DP2 of USB port 011 : COMP2 connected to U2 or UART port All others values : do not use							

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x14	MANUAL SW2	Reserved	Reserved	Reserved	Reserved	BOOT SW	JIG ON	Reserved	FET_ON
	Reset Value	N/A	N/A	N/A	N/A	0	0	N/A	1
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BOOT SW		0 : Low 1 : High							
JIG ON		0 : JIG output = high impedance 1 : JIG output = GND							
FET_ON		FET between VBUS and VBUS_OUT 0 : FET is turned off. OVP and OCP function disable 1 : FET is active, and FET is depended on OVP and OCP function.							

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1B	RESET	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RESET
	Reset Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET		0 : Do not reset the RT8973A 1 : Reset the RT8973A							

Power Up

The RT8973A has a threshold of 2.7V power on reset (POR) with a built-in hysteresis of 100mV. Before the input voltage reaches the POR threshold, the RT8973A is off. When the input voltage is over the POR threshold, the RT8973A will delay for 300ms and the soft-start will be activated after the 300ms delay. The 300ms delay allows the transient at the input during a hot insertion of the power supply to settle down before the IC starts to operate. During the soft-start transition, the RT8973A slowly turns on the internal MOSFET to reduce the inrush current.

Enable Control

When 0x14 FET_ON is set at 1 (default = 1), over voltage and over current protection function will be turned on. When 0x14 FET_ON is set at 0, the internal MOSFET will be turned off.

Over-Temperature Protection (OTP)

The RT8973A monitors its internal temperature to prevent thermal failures. The chip turns off the MOSFET when the junction temperature reaches 135°C. The IC will resume after the junction temperature is cooled down 10°C.

Input Over-Voltage Protection

The RT8973A monitors input voltage to prevent the input over-voltage lead to output system failures. The RT8973A input OVP threshold is set by the internal resistor. When the input voltage exceeds the threshold, the RT8973A outputs a logic signal to turn off the internal MOSFET within 2μs to prevent the high input voltage from damaging the electronics in the handheld system. The hysteresis of the input OVP threshold is 60mV. When the input voltage returns to normal operation voltage range, the RT8973A will re-enable the MOSFET.

Over-Current Protection (OCP)

The RT8973A monitors the output current to prevent the output short or the charging of the battery with an excessive current. The RT8973A has a built-in 180μs delay time to prevent any transient noise triggering the OCP. If the OCP situation keeps for 180μs, the internal MOSFET will be turned off and the 0x04 OCP_LATCH will change from 0 to 1. When the OCP happens for consecutive 16 times, the internal MOSFET will be turned off permanently unless the input power is recycled or the 0x14 FET_ON is changed from 0 to 1.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-18B 1.27x2.47 (BSC) package, the thermal resistance, θ_{JA}, is 45.4°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / (45.4°C/W) = 2.2W for a WL-CSP-18B 1.27x2.47 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

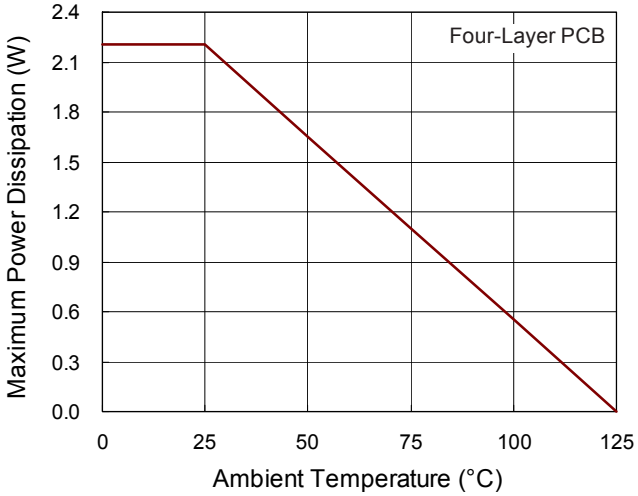
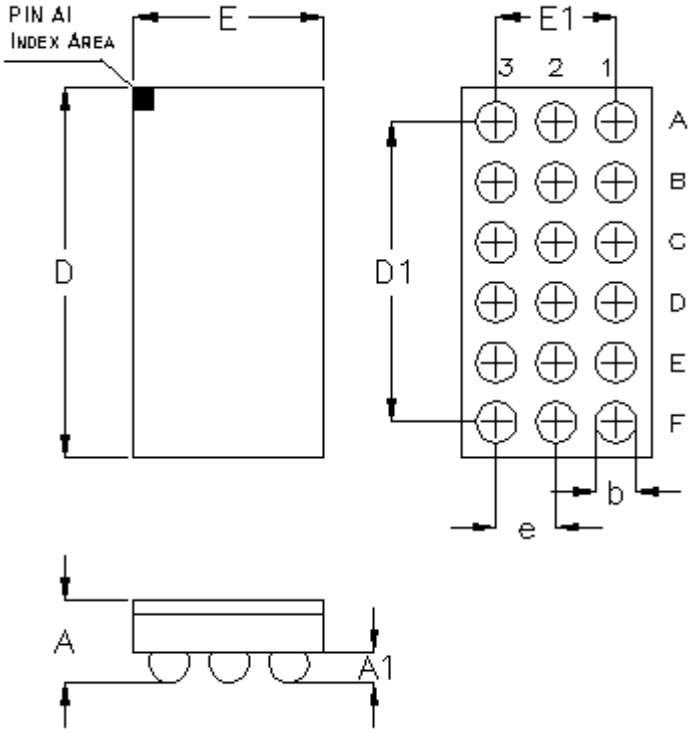


Figure 1. Derating Curve of Maximum Power Dissipation

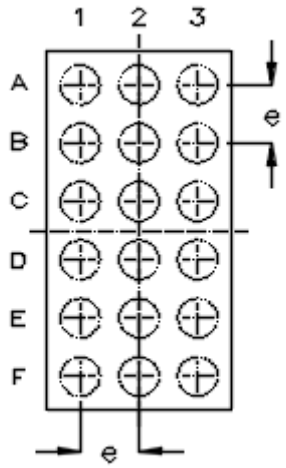
Outline Dimension

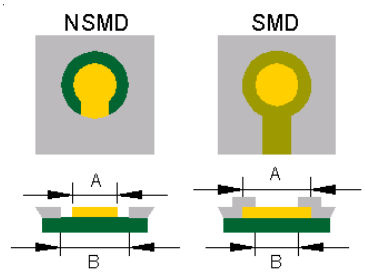


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max.
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	2.420	2.520	0.095	0.099
D1	2.000		0.079	
E	1.220	1.320	0.048	0.052
E1	0.800		0.031	
e	0.400		0.016	

18B WL-CSP 1.27x2.47 Package (BSC)

Footprint Information





Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.27*2.47-18(BSC)	18	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

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