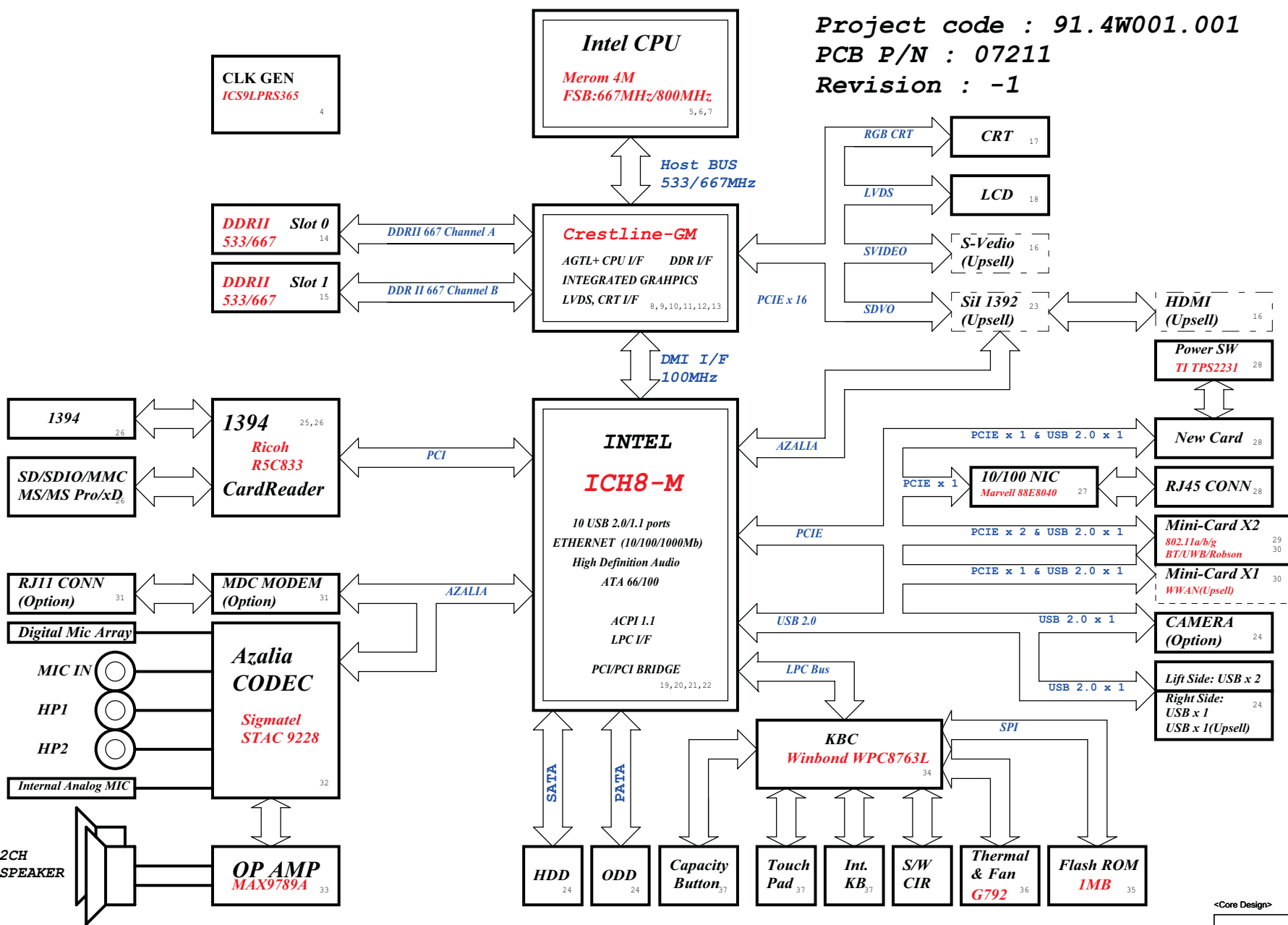


# Spears Intel UMA Block Diagram 2007/08/29

Project code : 91.4W001.001  
PCB P/N : 07211  
Revision : -1



CPU DC/DC	
ISL6262A	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC	
TPS5117	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0
	1D8V_S3

SYSTEM DC/DC	
TPS51120	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5
	5V_S5
	3D3V_S5

SYSTEM DC/DC	
TPS51100	
INPUTS	OUTPUTS
1D8V_S3	0D9V_S3

SYSTEM DC/DC	
LDO	
INPUTS	OUTPUTS
3D3V	2D5V
1D8V	1D5V_S0

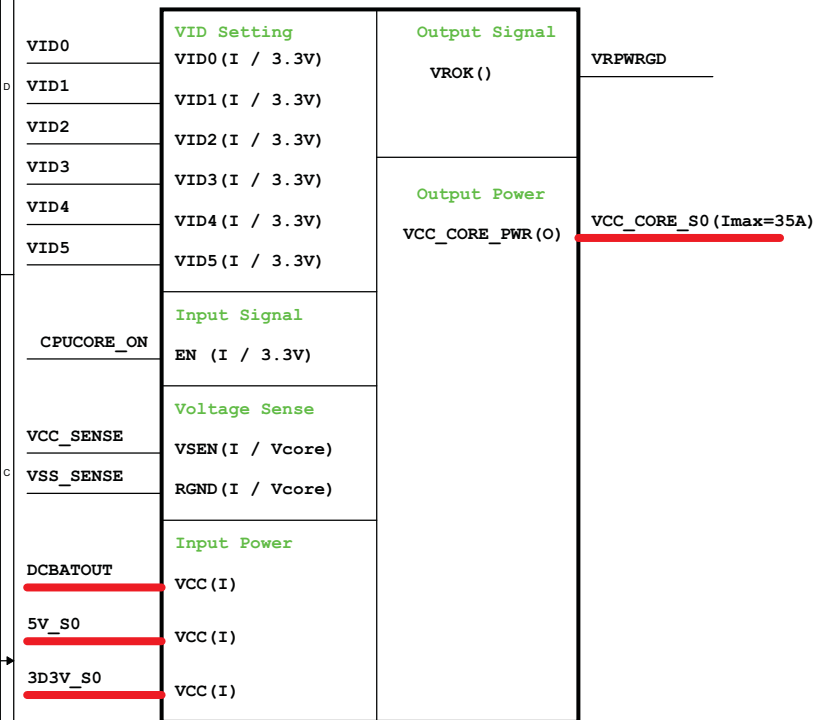
SYSTEM DC/DC	
LDO	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5
	1D5V_S0

MAXIM CHARGER	
MAX8731A	
INPUTS	OUTPUTS
AD+	DCBATOUT
BAT+	

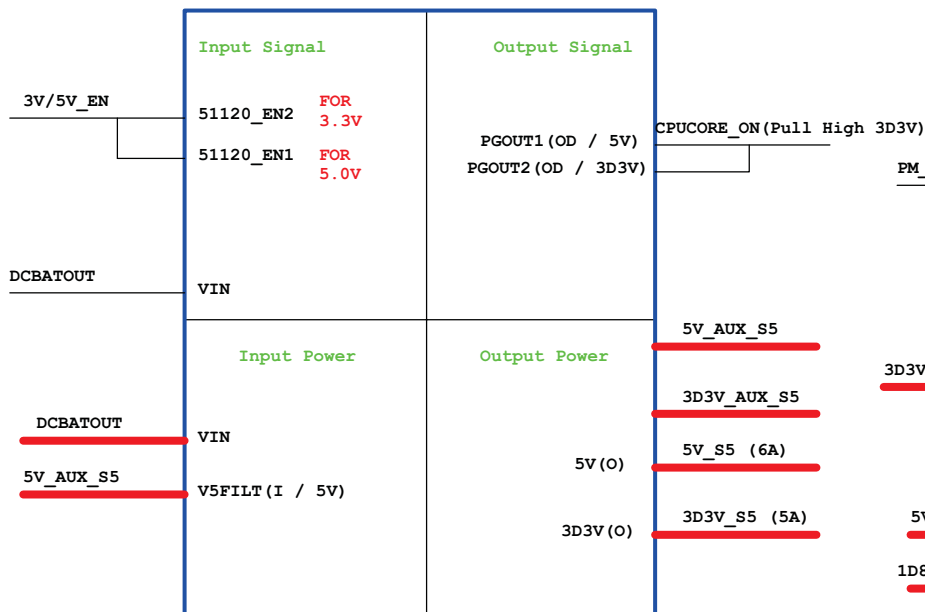
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緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
DS2 System Block Diagram	
Rev	Document Number
A3	Spears-Intel
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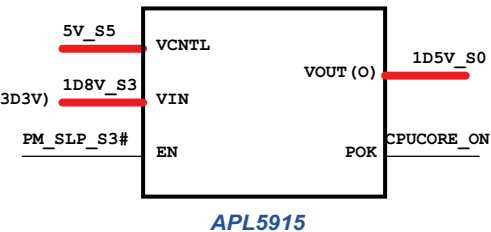
CPU\_CORE  
ISL6262A



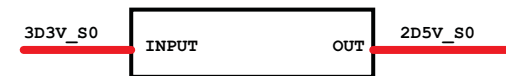
TI TPS51120  
3D3V/5V



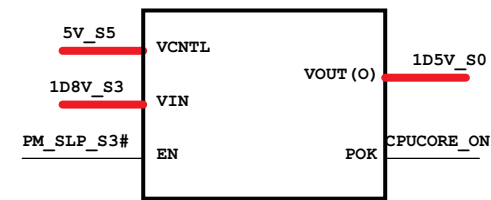
1D5V\_S0



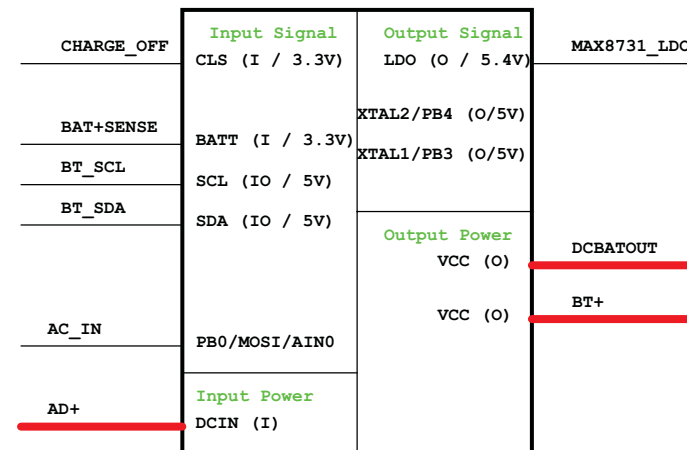
2D5V\_S0



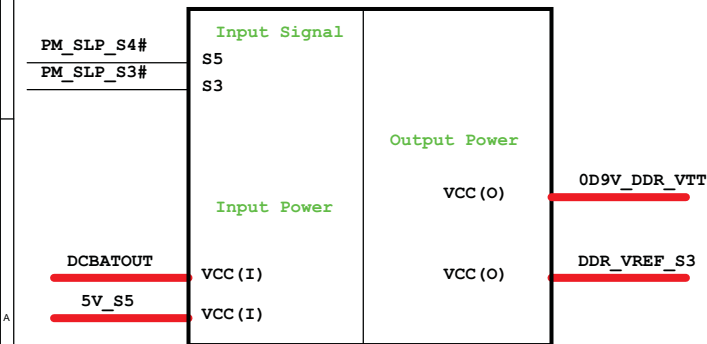
1D25V\_S0



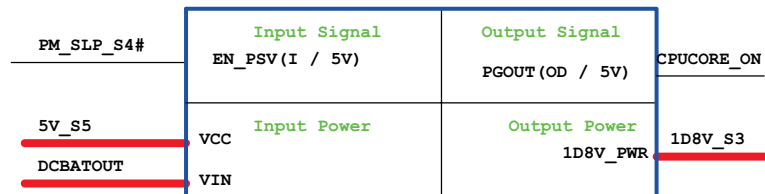
Charger\_MAX8731A



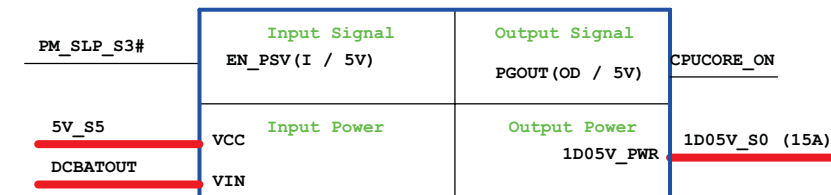
TI TPS51100  
0.9V/DDR\_VREF\_S3



TPS51117\_1D8V\_S3



TPS51117\_1D05V



## INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Config Registers: offset 224h)
HDA_SYNC	PCIe Port Config 1 bit0, Rising Edge of PWROK	Sets bit0 of RPC.PC (Config Registers: Offset 224h)
GNT2#	PCIe Port Config 2 bit0, Rising Edge of PWROK	Sets bit2 of RPC.PC (Config Registers: Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN. NOTE: This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h: bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05, VccCL1_05 VRM when sampled high
SATALED#	PCIe LAN REVERSAL. Rising Edge of PWROK	This signal has weak internal pull-up. set bit27 of MPC.LR (Device28: Function0: Offset D8)
SPKR	No Reboot. Rising Edge of PWROK	If sampled high, the system is strapped to the "No Reboot" mode (ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit. (Offset: 3410h: bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Internal Pull-Up. If sampled low, the Flash Descriptor Security will be overridden. If high, the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap			
ICH_RSVDTP3	AZ_DOUT_ICH	RSVD	Description
0	0	0	Enter XOR Chain
0	1	1	Normal Operation (default)
1	0	0	Set PCIe port config bit1
1	1	1	

A16 swap override strap	
PCI_GNT#3	low = A16 swap override enable high = default

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC (Default)

Integrated VccSus1_05, VccSus1_5, VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable
Integrated VccLAN1_05, VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Default High=No Reboot

8.2K PULL HIGH

## INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD



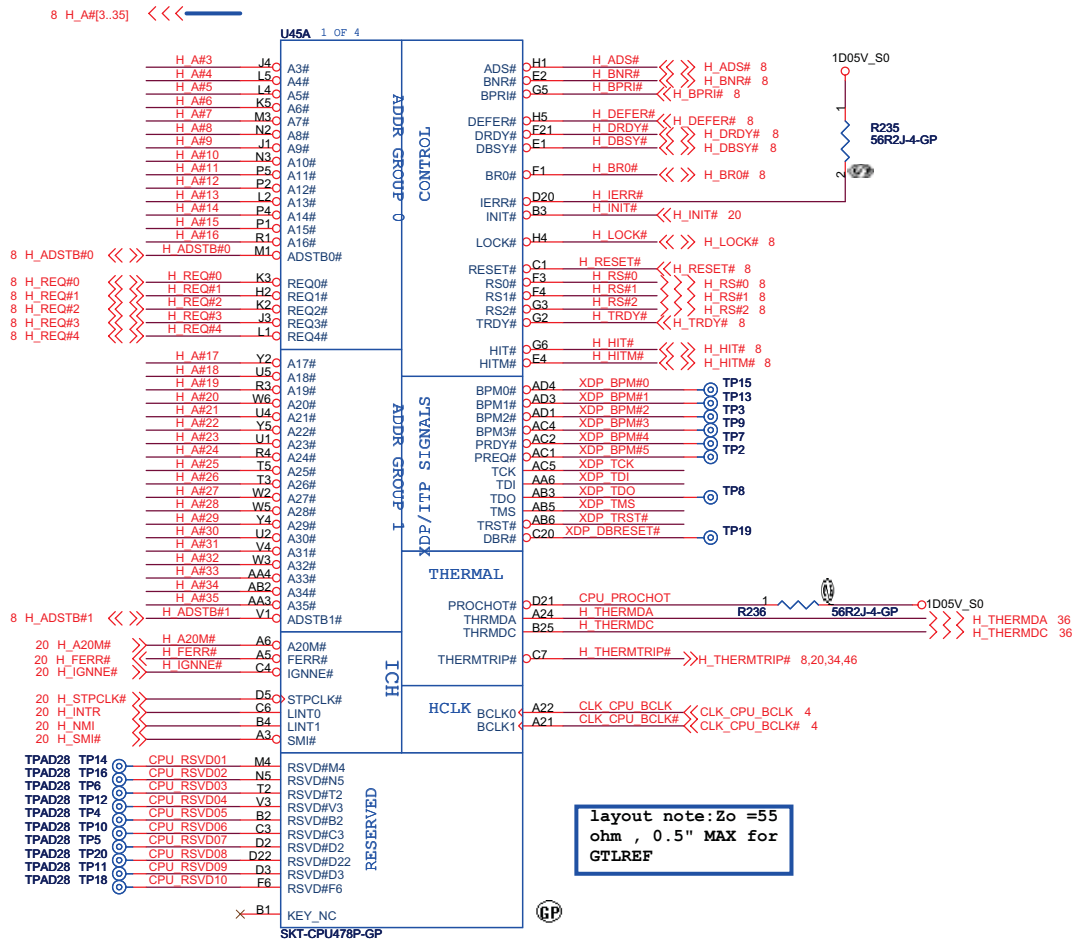
## INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal ★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode (Lanes ★ number in order)
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reserved	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIe	Only PCIe or SDVO is operation ★	PCIe and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

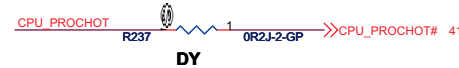
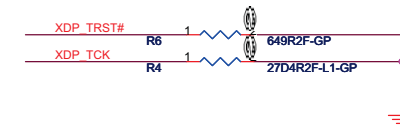
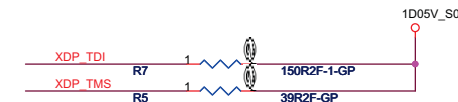
CFG 12	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

<Core Design>		
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Title		
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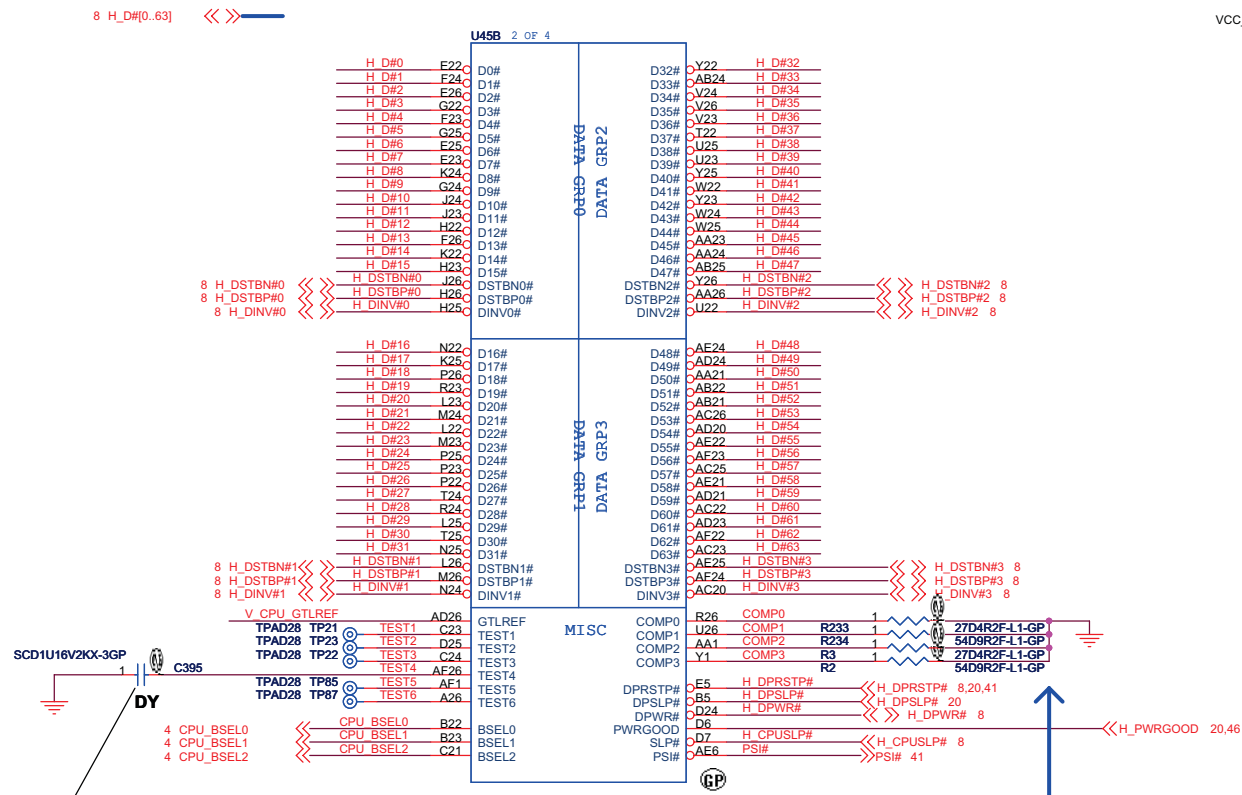




H\_THERMDA, H\_THERMDC routing together,  
Trace width / Spacing = 10 / 10 mil



<Core Design>

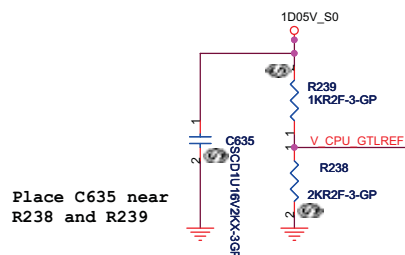


PLACE C25 close to the TEST4 PIN,  
make sure TEST3,TEST4,TEST5 trace  
routing is reference to GND and  
away other noisy signals

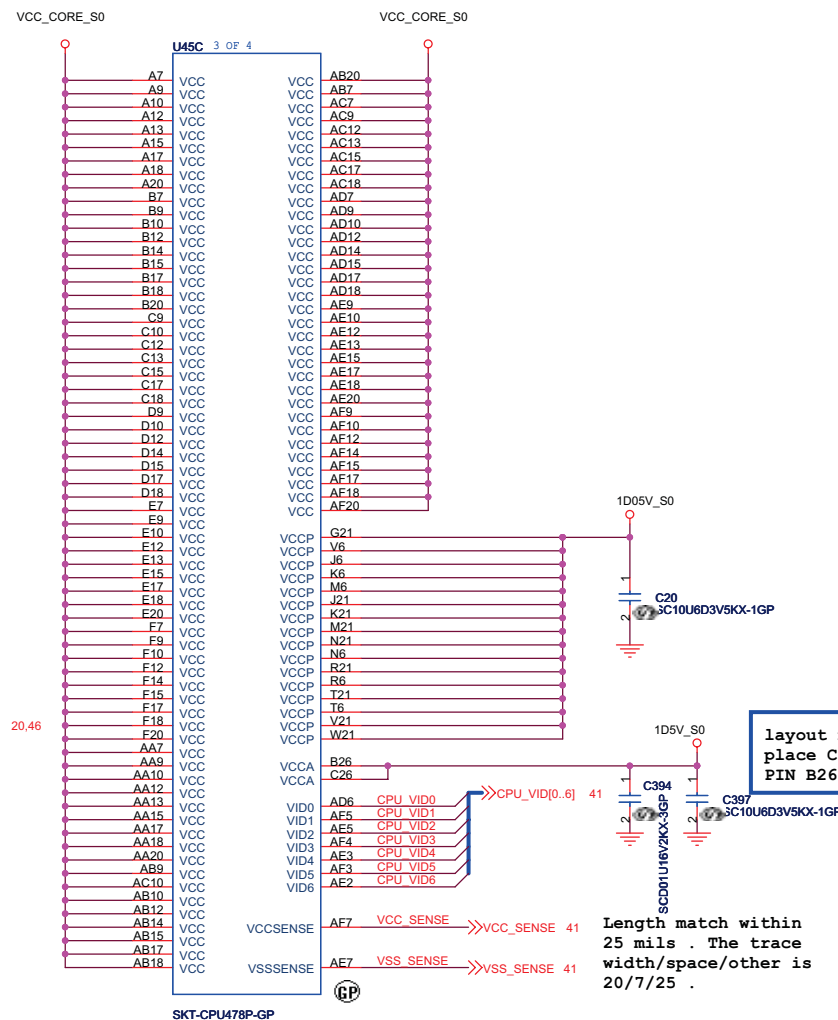
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor Placed  
within 0.5" of CPU  
pin. Trace should  
be at least 25 mils  
away from any other  
toggling signal .  
COMP[0,2] trace  
width is 18 mils.  
COMP[1,3] trace  
width is 4 mils .

Close to CPU  
pin AD26  
Z0=55 ohm  
with in  
500mils .

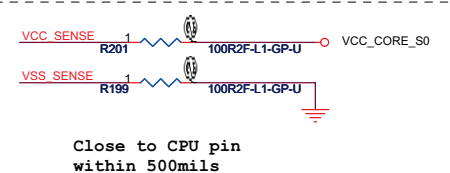


Place C635 near  
R238 and R239



layout note:  
place C3 near  
PIN B26

Length match within  
25 mils . The trace  
width/space/other is  
20/7/25 .



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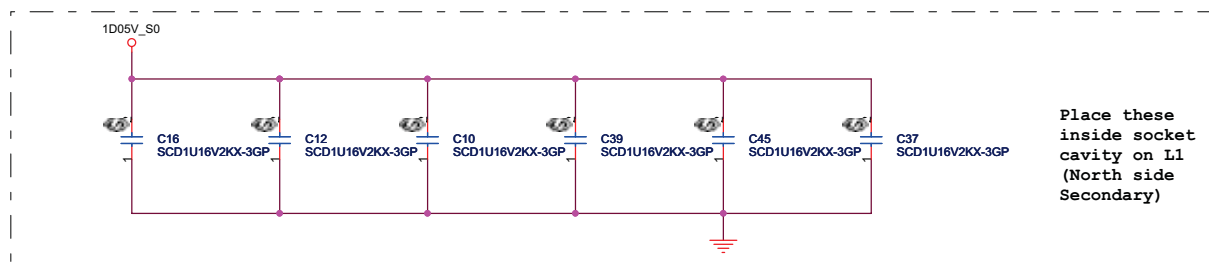
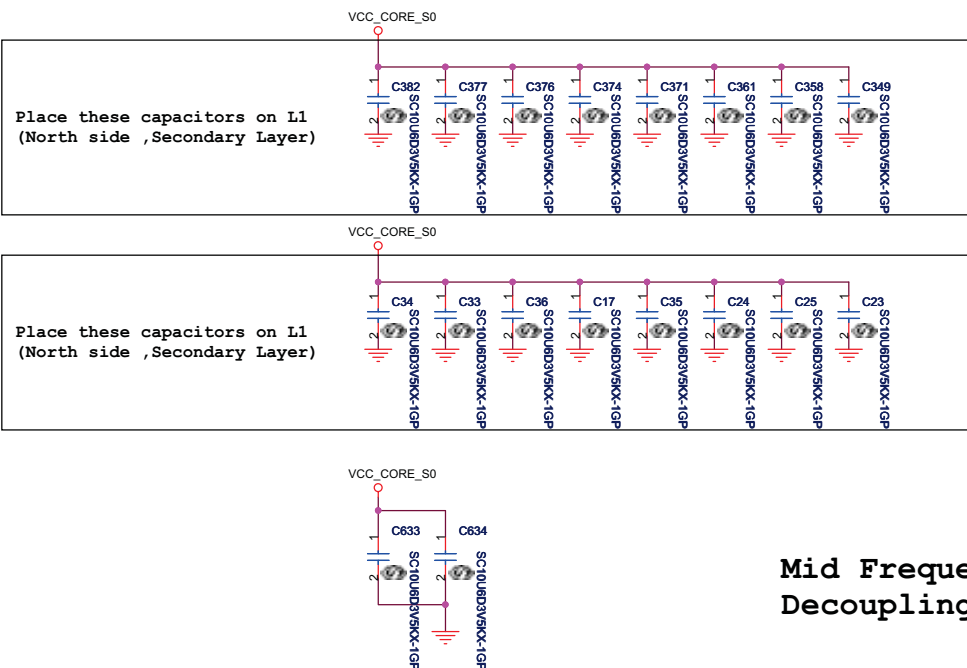
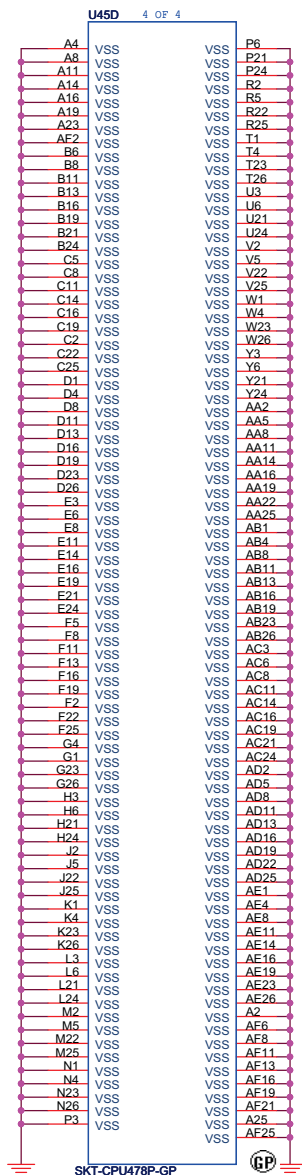
緯創資通

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih

**Title** ***Merion(2/3)-AGTL+/PWR***

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<Core Design>





D

C

B

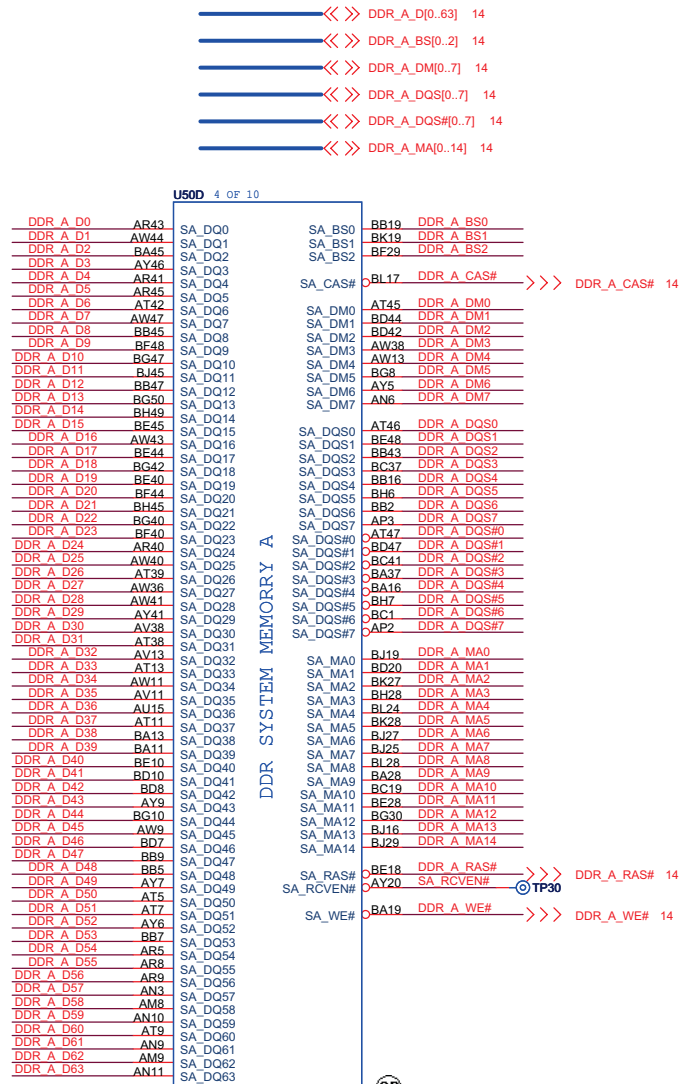
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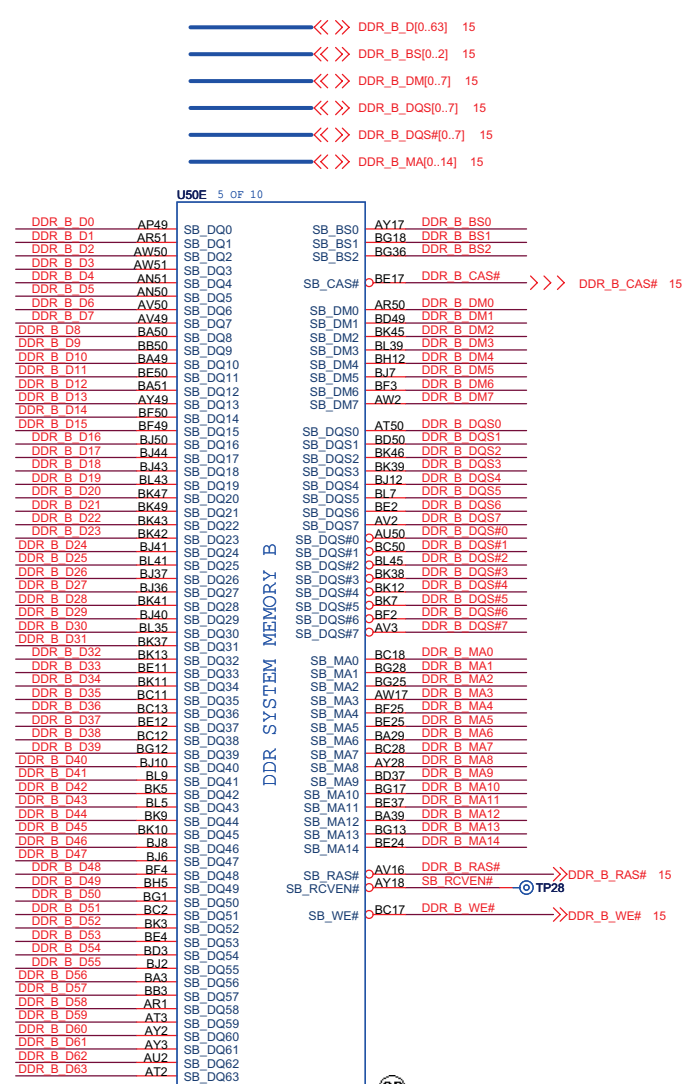
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CRESTLINE-GP-U-NF

NB:71.GM965.A0U

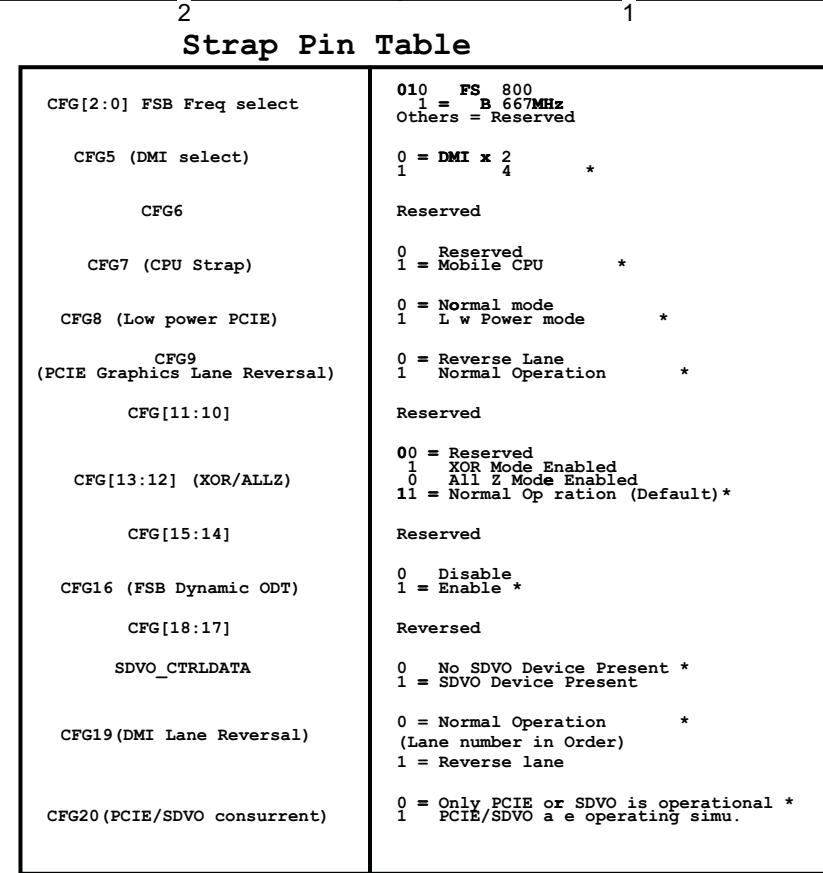


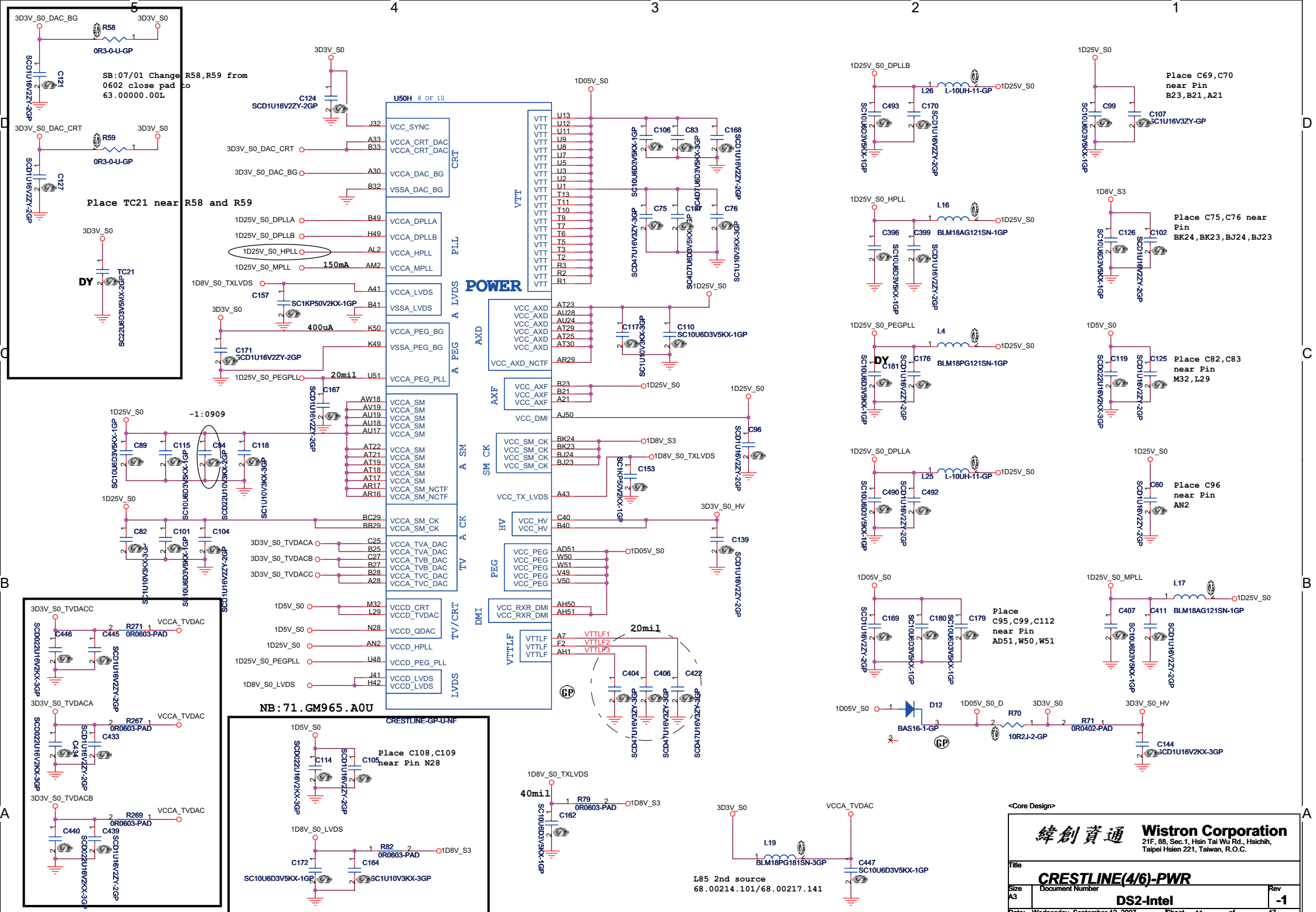
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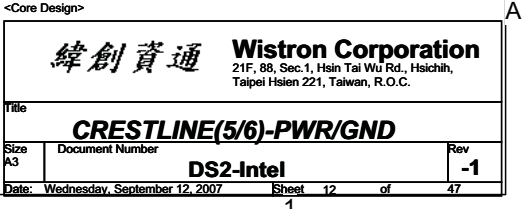
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A13	VSS	AW24
A15	VSS	AW29
A17	VSS	AW32
A24	VSS	AW5
AA21	VSS	AW7
AA24	VSS	AY10
AA29	VSS	AY24
AB20	VSS	AY37
AB23	VSS	AY42
AB26	VSS	AY43
AB28	VSS	AY45
AB31	VSS	AY47
AC10	VSS	AY50
AC13	VSS	B10
AC3	VSS	B20
AC39	VSS	B24
AC43	VSS	B29
AC47	VSS	B30
AD1	VSS	B35
AD21	VSS	B38
AD26	VSS	B43
AD29	VSS	B46
AD3	VSS	B5
AD41	VSS	B8
AD45	VSS	BA1
AD49	VSS	BA17
AD5	VSS	BA18
AD50	VSS	BA2
AD8	VSS	BA24
AE10	VSS	BB12
AE14	VSS	BB25
AE6	VSS	BB40
AE20	VSS	BB44
AE23	VSS	BB49
AE24	VSS	BB8
AE31	VSS	BC16
AG2	VSS	BC24
AG38	VSS	BC25
AG43	VSS	BC38
AG47	VSS	BC40
AG50	VSS	BC51
AH3	VSS	BD13
AH40	VSS	BD2
AH41	VSS	BD28
AH7	VSS	BD45
AH9	VSS	BD48
AJ11	VSS	BD5
AJ13	VSS	BE1
AJ21	VSS	BE19
AJ24	VSS	BE23
AJ29	VSS	BE30
AJ32	VSS	BE42
AJ43	VSS	BE51
AJ45	VSS	BE8
AJ49	VSS	BF12
AK20	VSS	BF16
AK21	VSS	BF36
AK26	VSS	BG19
AK28	VSS	BG2
AK31	VSS	BG24
AK51	VSS	BG29
AL1	VSS	BG39
AM11	VSS	BG48
AM13	VSS	BG5
AM3	VSS	BG51
AM4	VSS	BH17
AM41	VSS	BH30
AM45	VSS	BH44
AN1	VSS	BH46
AN38	VSS	BH8
AN39	VSS	BJ11
AN43	VSS	BJ13
AN5	VSS	BJ38
AN7	VSS	BJ4
AP4	VSS	BJ42
AP48	VSS	BJ46
AP50	VSS	BK15
AR11	VSS	BK17
AR2	VSS	BK25
AR39	VSS	BK29
AR44	VSS	BK36
AR47	VSS	BK40
AR7	VSS	BK44
AT10	VSS	BK6
AT14	VSS	BK8
AT41	VSS	BL11
AT49	VSS	BL13
AU1	VSS	BL19
AU23	VSS	BL22
AU29	VSS	BL37
AU3	VSS	BL47
AU36	VSS	C12
AU49	VSS	C16
AU51	VSS	C19
AV39	VSS	C28
AV48	VSS	C29
AW1	VSS	C33
AW12	VSS	C36
AW16	VSS	C41

CRESTLINE-GP-U-NF  
NB: 71 . GM965 . A0U

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C46	VSS	W11
C50	VSS	W39
C7	VSS	W43
D13	VSS	W47
D24	VSS	W5
D3	VSS	W7
D32	VSS	Y13
D39	VSS	Y2
D45	VSS	Y41
D49	VSS	Y45
E10	VSS	Y49
E16	VSS	Y5
E24	VSS	Y50
E28	VSS	Y11
E32	VSS	P29
E47	VSS	T29
F19	VSS	T31
F36	VSS	T33
F4	VSS	R28
F40	VSS	
F50	VSS	
G1	VSS	
G13	VSS	
G16	VSS	AA32
G19	VSS	AB32
G24	VSS	AD32
G28	VSS	AE28
G29	VSS	AF29
G33	VSS	AT27
G42	VSS	AV25
G45	VSS	H50
G48	VSS	
GB4	VSS	
H24	VSS	
H28	VSS	
H4	VSS	
H45	VSS	
J11	VSS	
J16	VSS	
J2	VSS	
J24	VSS	
J28	VSS	
J33	VSS	
J35	VSS	
J39	VSS	
K12	VSS	
K47	VSS	
K8	VSS	
L1	VSS	
L17	VSS	
L20	VSS	
L24	VSS	
L28	VSS	
L3	VSS	
L33	VSS	
L49	VSS	
M28	VSS	
M42	VSS	
M46	VSS	
M49	VSS	
M5	VSS	
M50	VSS	
M9	VSS	
N11	VSS	
N14	VSS	
N17	VSS	
N29	VSS	
N32	VSS	
N36	VSS	
N39	VSS	
N44	VSS	
N49	VSS	
N7	VSS	
P19	VSS	
P2	VSS	
P23	VSS	
P3	VSS	
P50	VSS	
R49	VSS	
T39	VSS	
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U50	VSS	
V2	VSS	
V3	VSS	

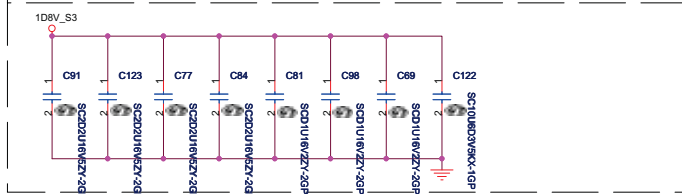
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NB: 71 . GM965 . A0U

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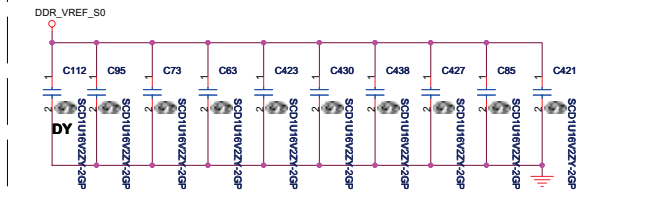
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Size		21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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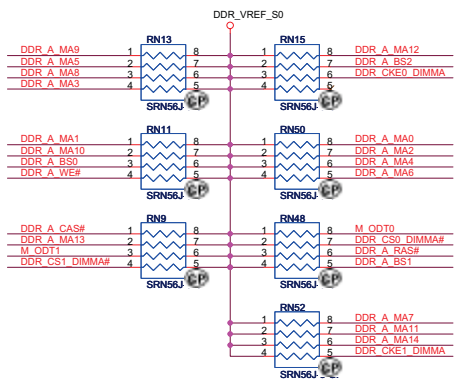
Layout Note:  
Place near DM1



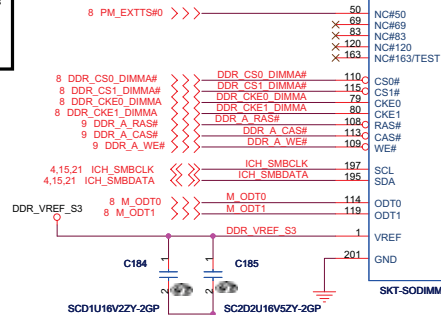
Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



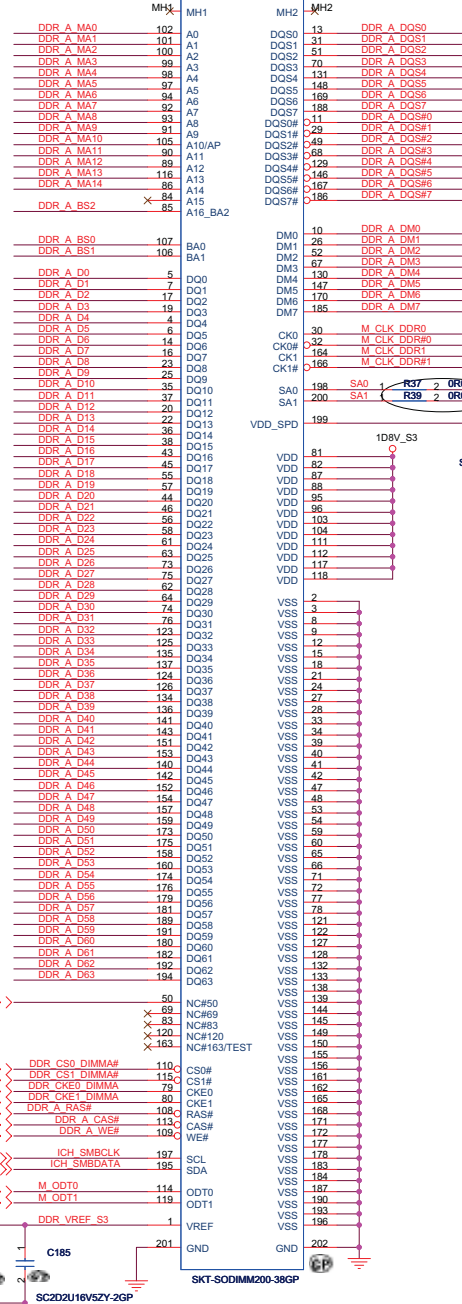
change to 8P4R



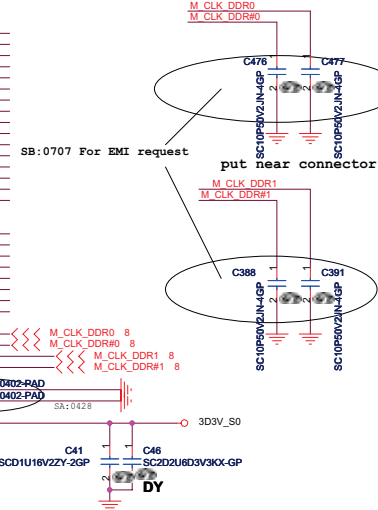
Layout Note:  
Place these resistors  
closely DM1, all  
trace length Max=1.5"



DM2



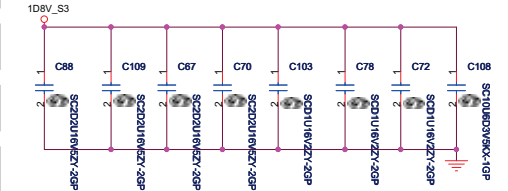
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2nd Source: 62.10017.A41



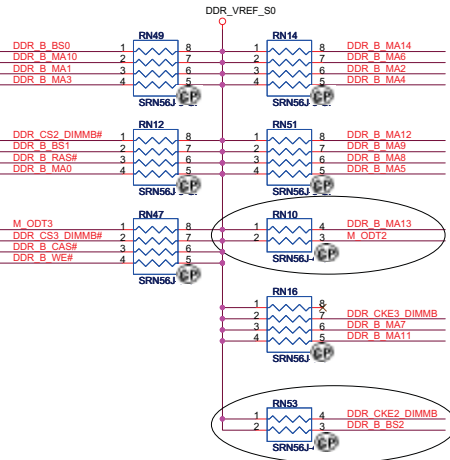
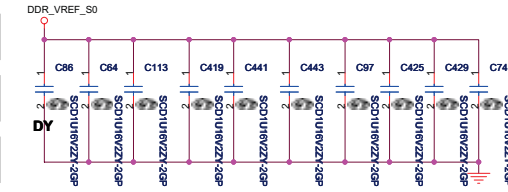


9 DDR\_B\_DQS# [0..7] <<>>  
 9 DDR\_B\_DQ [0..63] <<>>  
 9 DDR\_B\_DM [0..7] <<>>  
 9 DDR\_B\_DQS [0..7] <<>>  
 9 DDR\_B\_MA [0..14] <<>>  
 9 DDR\_B\_BS [0..2] <<>>

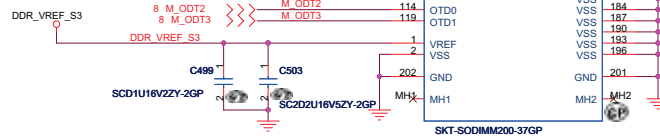
Layout Note:  
Place near DM2



Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9V5



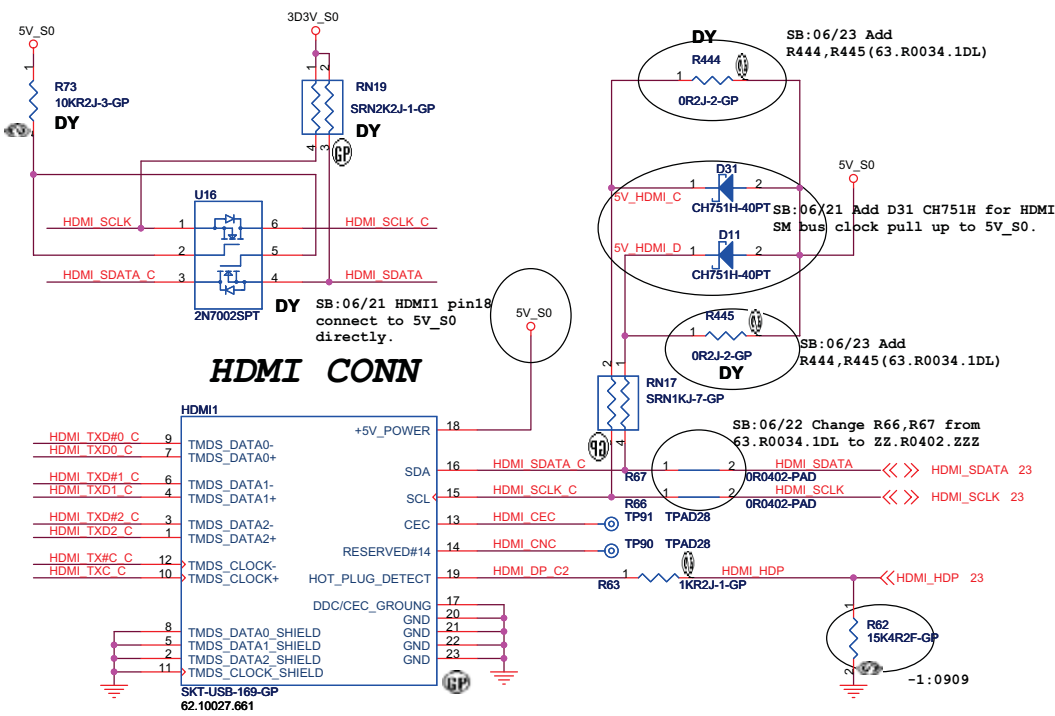
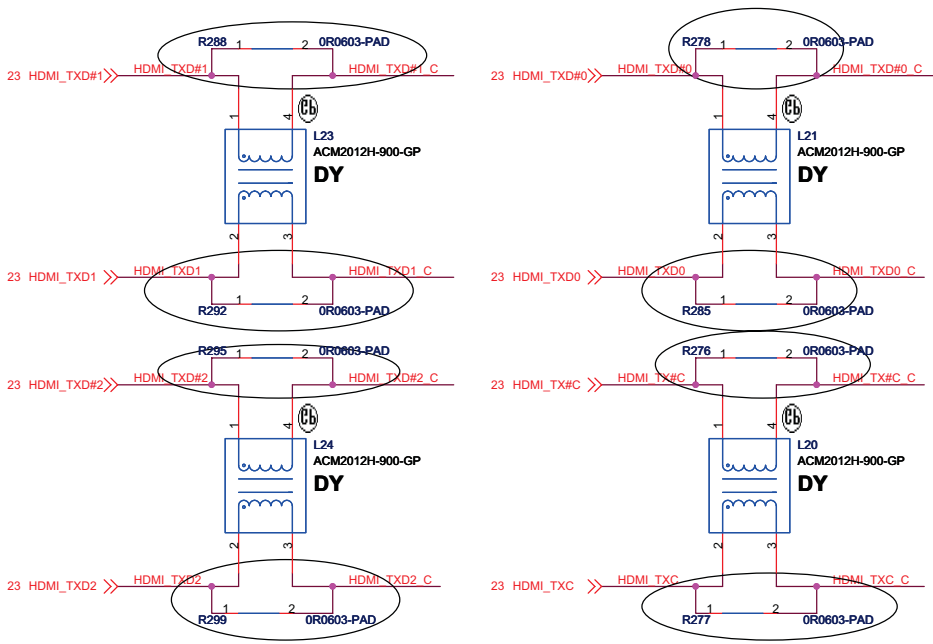
Layout Note:  
Place these resistors  
closely DM2, all  
trace length Max=1.5"



DDR_B_MA0	102	A0
DDR_B_MA1	101	A1
DDR_B_MA2	100	A2
DDR_B_MA3	99	A3
DDR_B_MA4	98	A4
DDR_B_MA5	97	A5
DDR_B_MA6	96	A6
DDR_B_MA7	95	A7
DDR_B_MA8	94	A8
DDR_B_MA9	93	A9
DDR_B_MA10	92	A10/AP
DDR_B_MA11	91	A11
DDR_B_MA12	90	A12
DDR_B_MA13	89	A13
DDR_B_MA14	88	A14
DDR_B_MA15	87	A15
DDR_B_BS2	86	A16/BA2
DDR_B_BS0	107	BA0
DDR_B_BS1	106	BA1
DDR_B_D0	5	DO0
DDR_B_D1	7	DO1
DDR_B_D2	17	DO2
DDR_B_D3	19	DO3
DDR_B_D4	4	DO4
DDR_B_D5	6	DO5
DDR_B_D6	14	DO6
DDR_B_D7	16	DO7
DDR_B_D8	23	DO8
DDR_B_D9	35	DO9
DDR_B_D10	37	DO10
DDR_B_D11	20	DO11
DDR_B_D12	22	DO12
DDR_B_D13	36	DO13
DDR_B_D14	38	DO14
DDR_B_D15	43	DO15
DDR_B_D16	45	DO16
DDR_B_D17	55	DO17
DDR_B_D18	57	DO18
DDR_B_D19	44	DO19
DDR_B_D20	46	DO20
DDR_B_D21	56	DO21
DDR_B_D22	58	DO22
DDR_B_D23	61	DO23
DDR_B_D24	63	DO24
DDR_B_D25	73	DO25
DDR_B_D26	75	DO26
DDR_B_D27	62	DO27
DDR_B_D28	64	DO28
DDR_B_D29	74	DO29
DDR_B_D30	76	DO30
DDR_B_D31	123	DO31
DDR_B_D32	125	DO32
DDR_B_D33	135	DO33
DDR_B_D34	137	DO34
DDR_B_D35	124	DO35
DDR_B_D36	126	DO36
DDR_B_D37	134	DO37
DDR_B_D38	136	DO38
DDR_B_D39	141	DO39
DDR_B_D40	143	DO40
DDR_B_D41	151	DO41
DDR_B_D42	153	DO42
DDR_B_D43	140	DO43
DDR_B_D44	142	DO44
DDR_B_D45	152	DO45
DDR_B_D46	154	DO46
DDR_B_D47	157	DO47
DDR_B_D48	159	DO48
DDR_B_D49	173	DO49
DDR_B_D50	175	DO50
DDR_B_D51	158	DO51
DDR_B_D52	160	DO52
DDR_B_D53	174	DO53
DDR_B_D54	176	DO54
DDR_B_D55	179	DO55
DDR_B_D56	181	DO56
DDR_B_D57	189	DO57
DDR_B_D58	190	DO58
DDR_B_D59	182	DO59
DDR_B_D60	192	DO60
DDR_B_D61	194	DO61
DDR_B_D62	110	DO62
DDR_B_D63	112	DO63

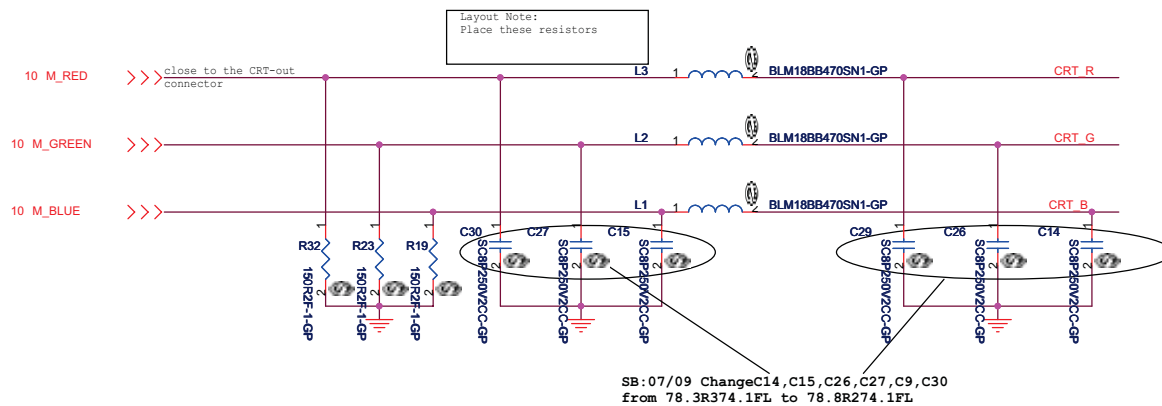
DDR_B_DQS#0	11	DQS#0
DDR_B_DQS#1	29	DQS#1
DDR_B_DQS#2	49	DQS#2
DDR_B_DQS#3	68	DQS#3
DDR_B_DQS#4	129	DQS#4
DDR_B_DQS#5	146	DQS#5
DDR_B_DQS#6	167	DQS#6
DDR_B_DQS#7	186	DQS#7
DDR_B_DQS#0	13	DQS#0
DDR_B_DQS#1	31	DQS#1
DDR_B_DQS#2	51	DQS#2
DDR_B_DQS#3	70	DQS#3
DDR_B_DQS#4	131	DQS#4
DDR_B_DQS#5	148	DQS#5
DDR_B_DQS#6	169	DQS#6
DDR_B_DQS#7	188	DQS#7

HDMI I/F & CONNECTOR

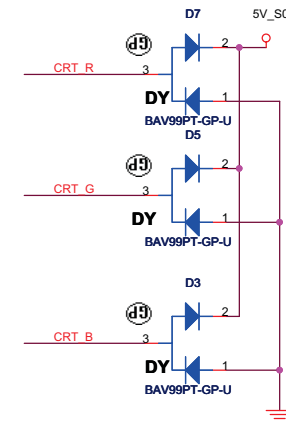
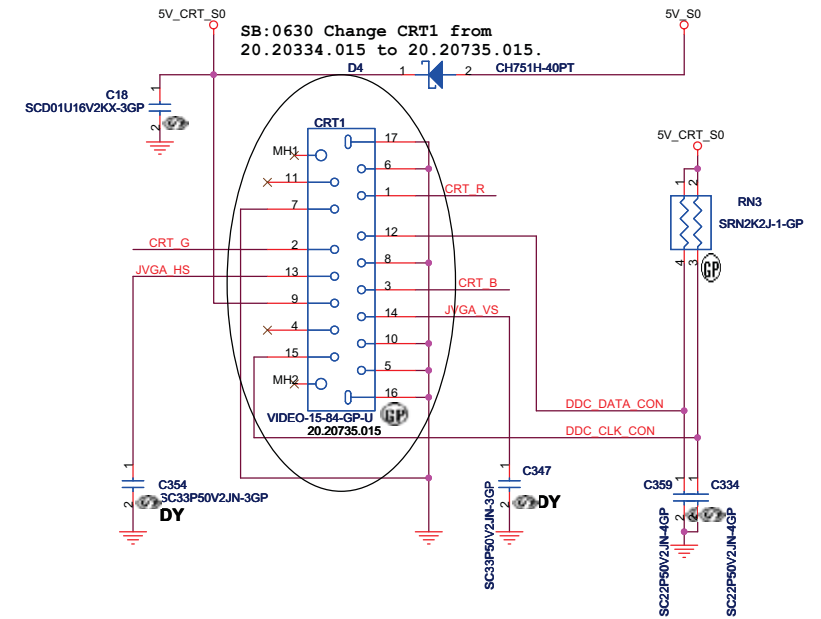
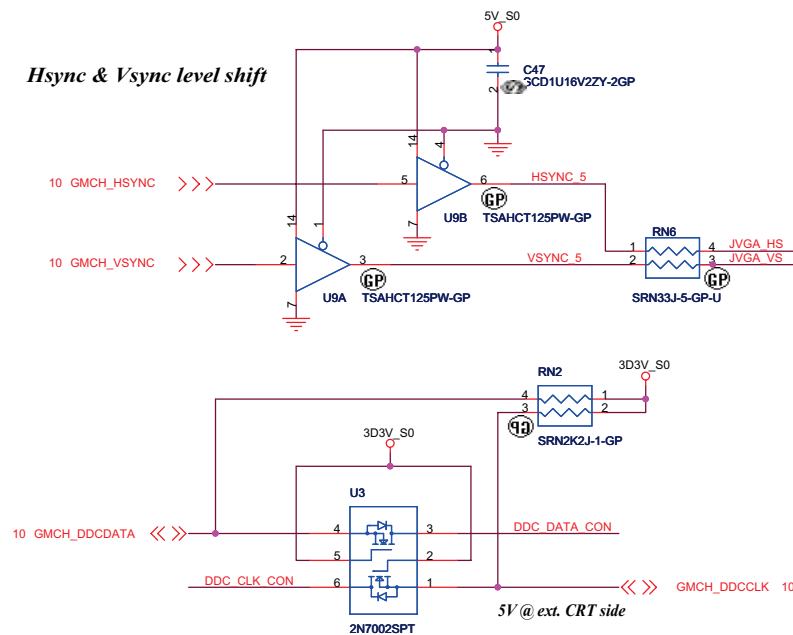


TV OUT CONN (Optional) Move to Right I/O Board

# CRT I/F & CONNECTOR



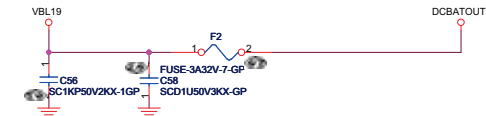
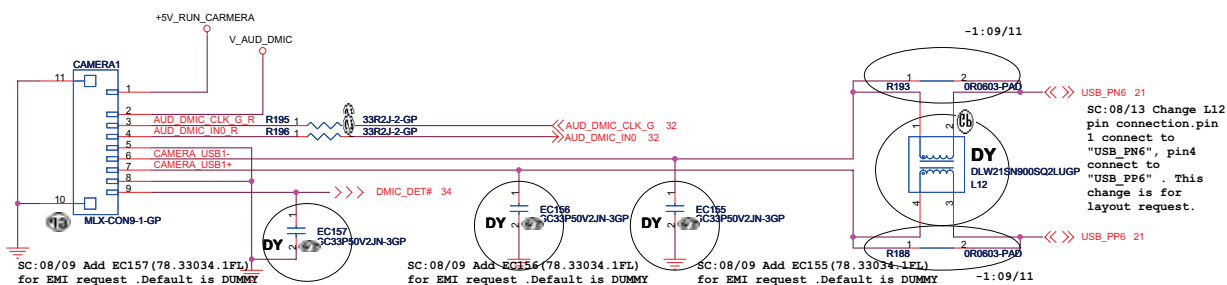
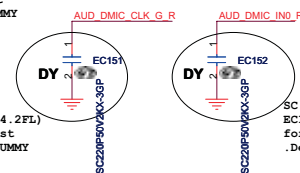
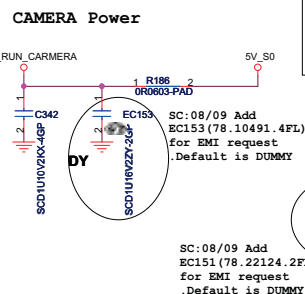
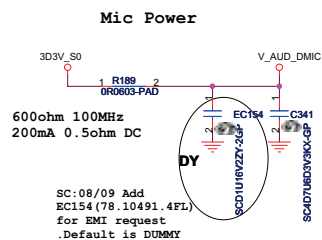
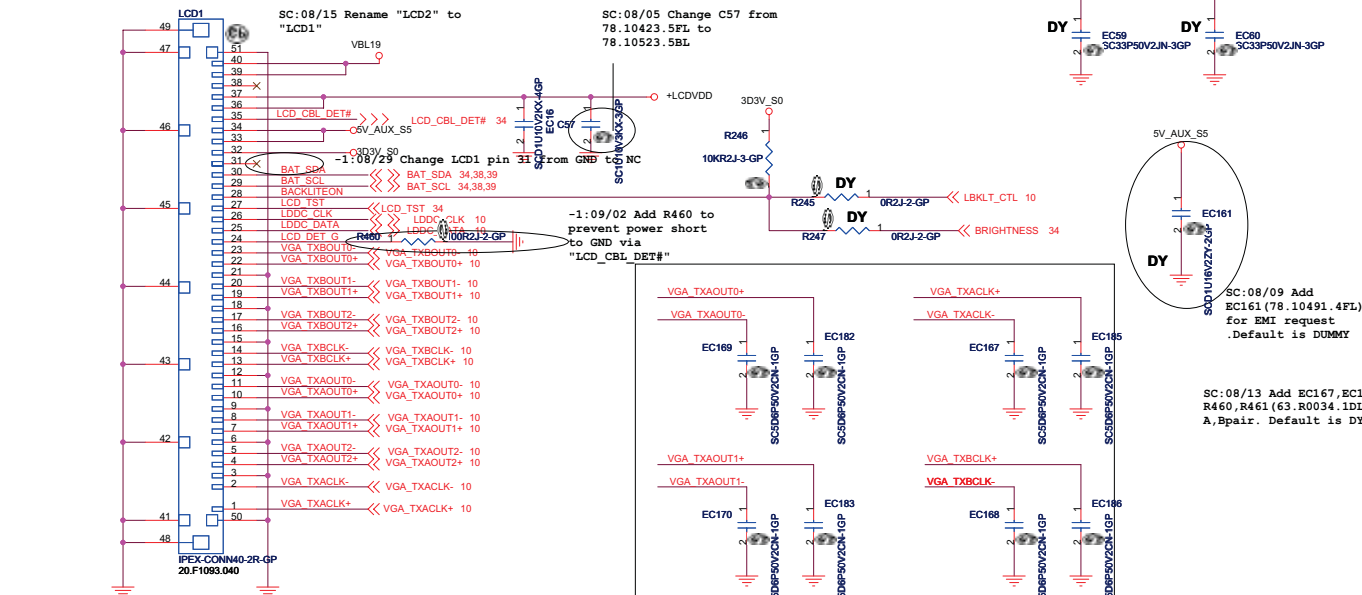
## Hsync & Vsync level shift



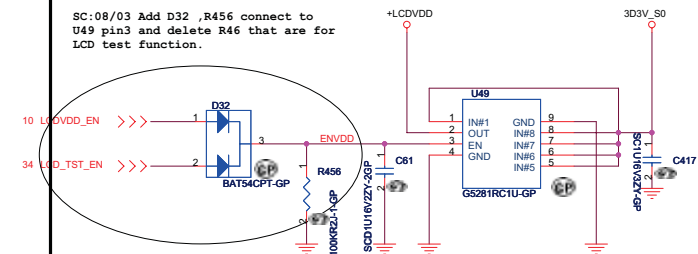
<Core Design>

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	<b>CRT Connector</b>
Size A3	Document Number <b>DS2-Intel</b>
Date: Wednesday, September 12, 2007	Sheet 17 of 47
Rev	<b>-1</b>

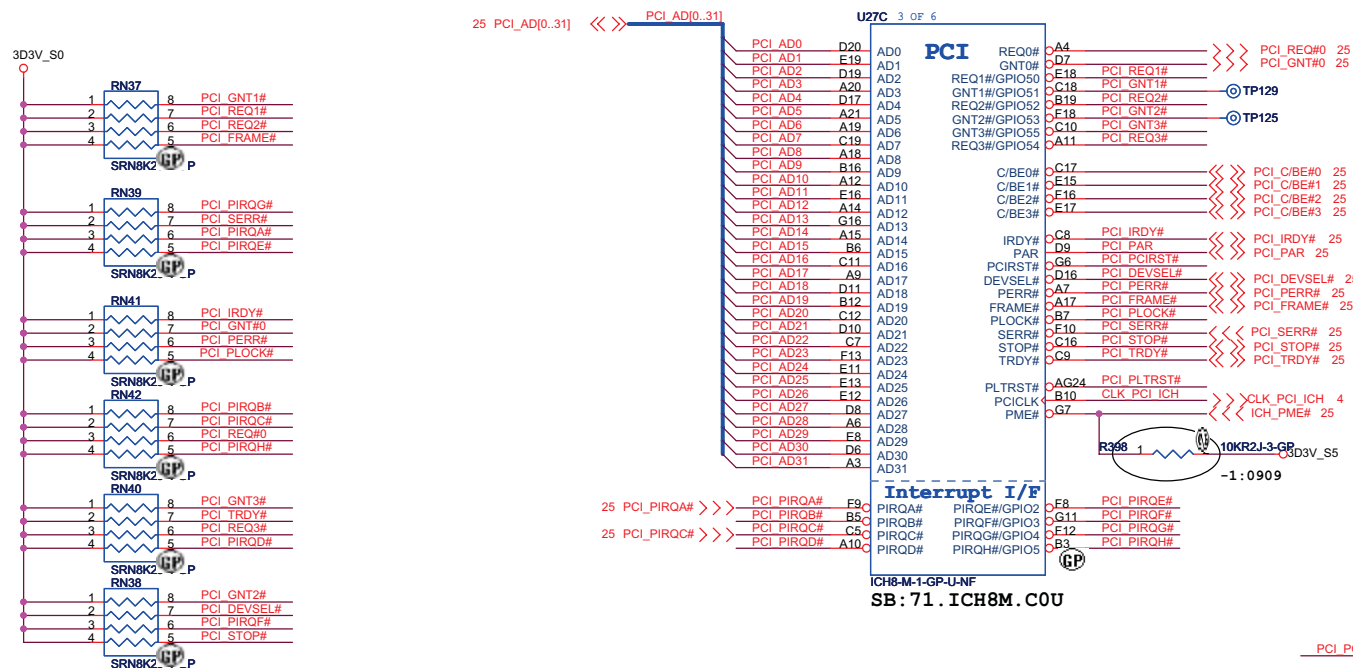
SC:08/09 Add LCD2 (20.F1093.040) ,please check LCD1 and LCD 2 layout overlap possibility.



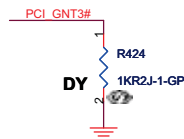
### INVERTER POWER



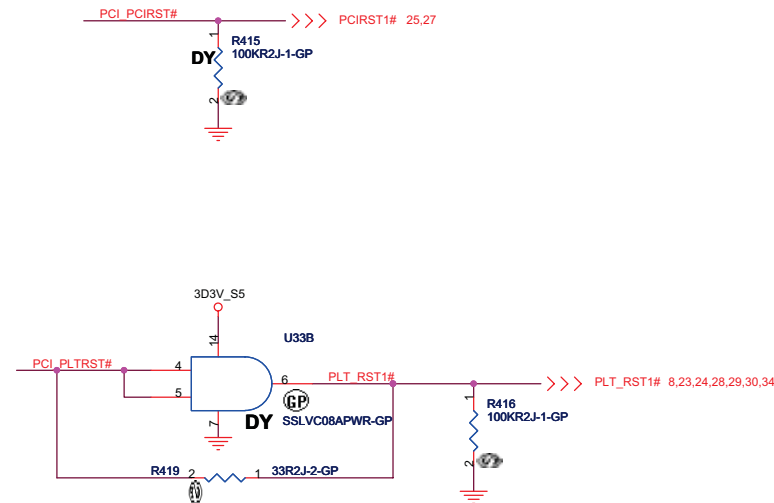
LCD POWER

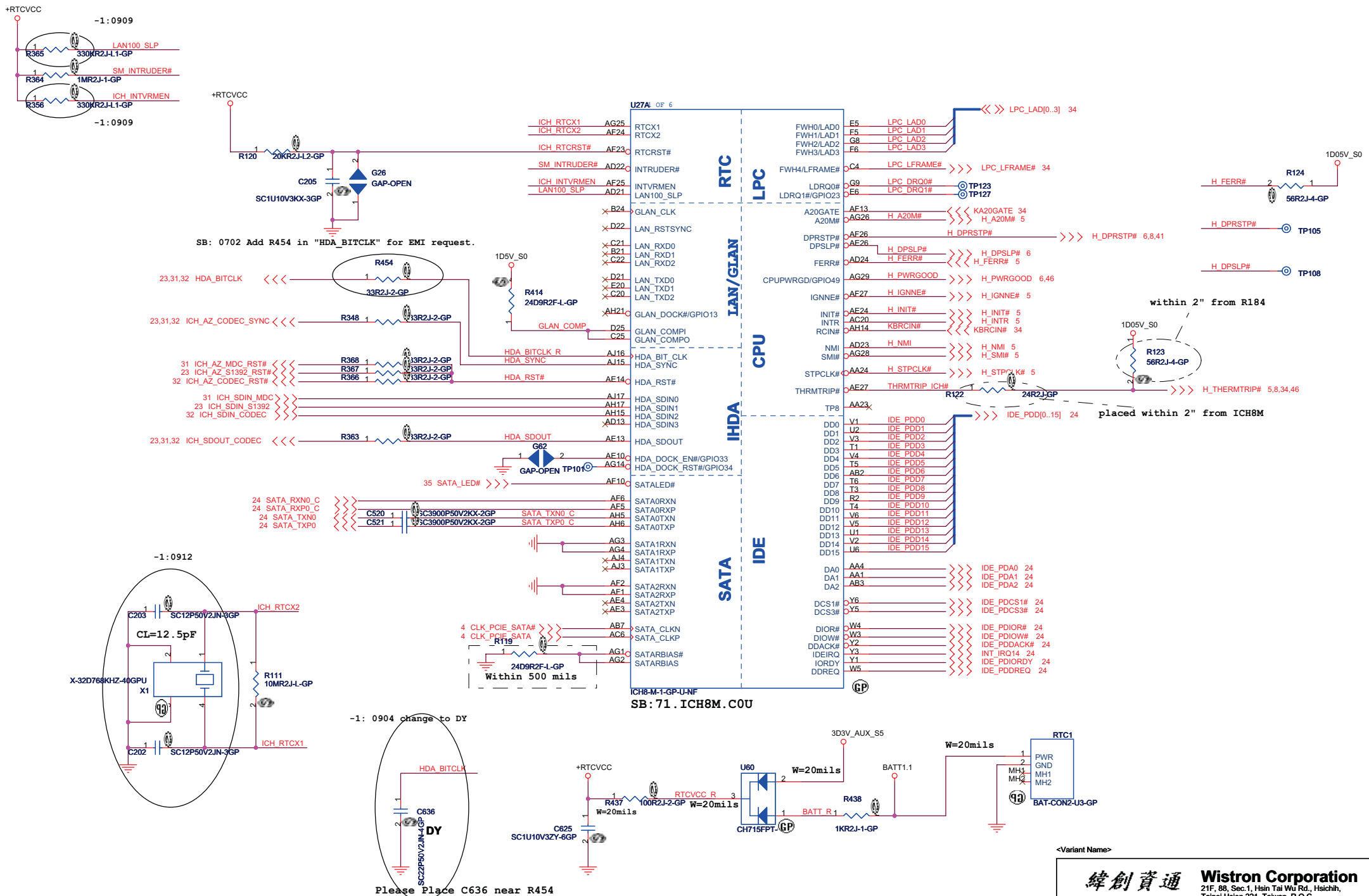


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *

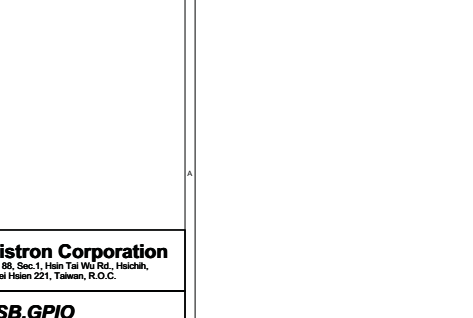
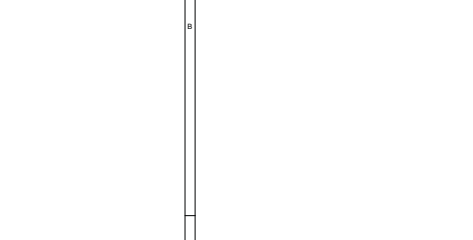
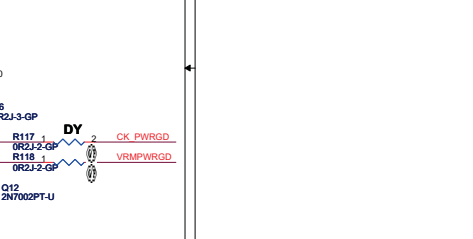
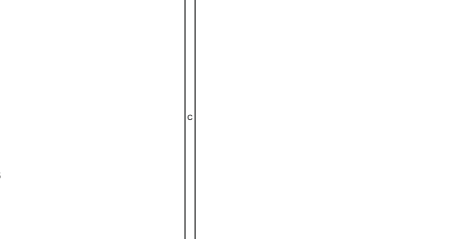
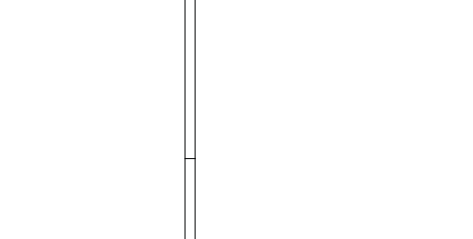
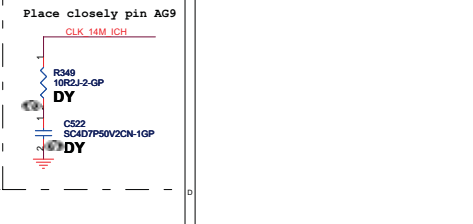
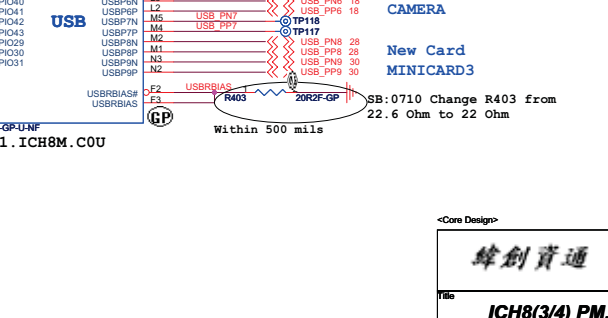
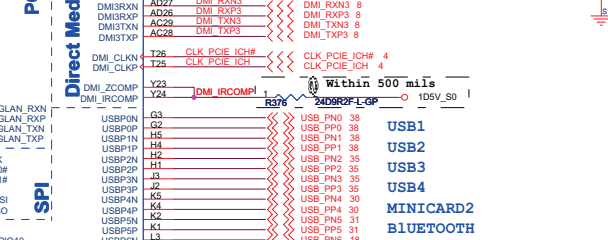
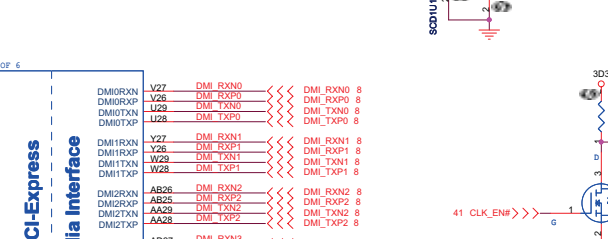
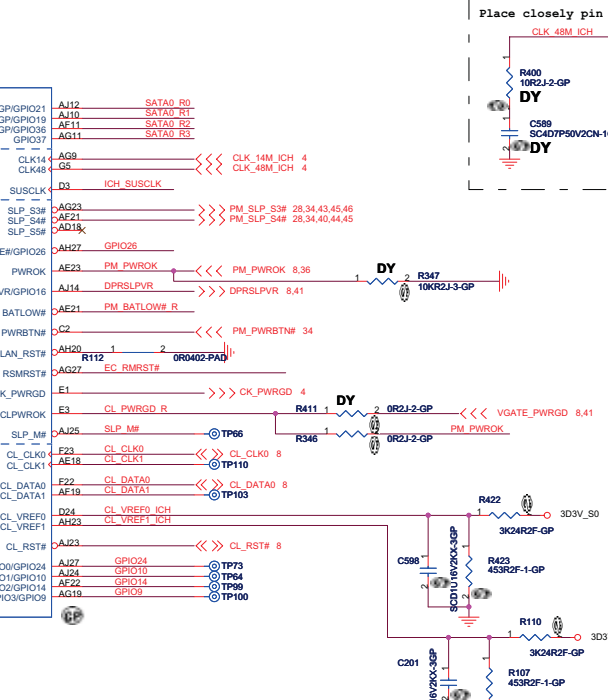
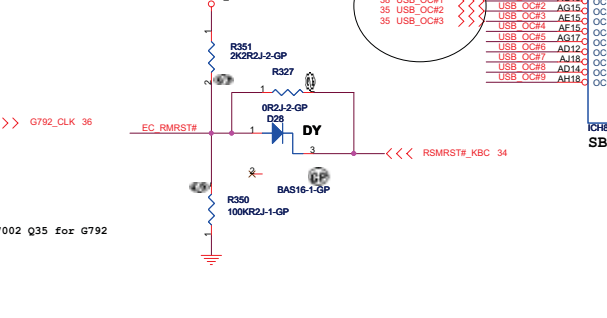
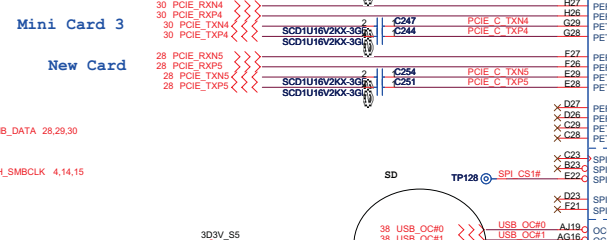
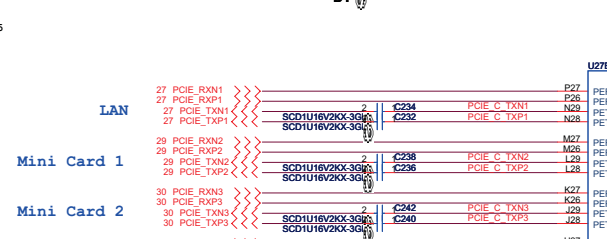
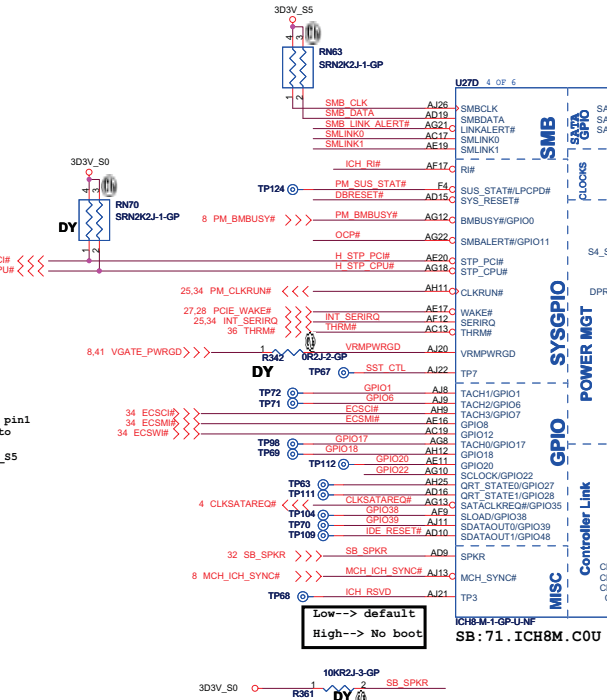
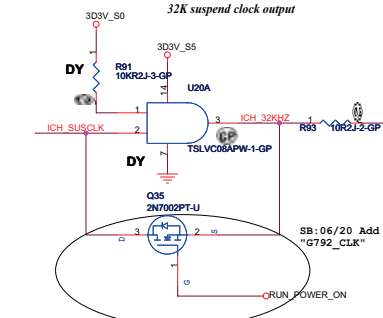
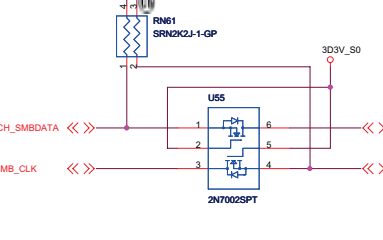
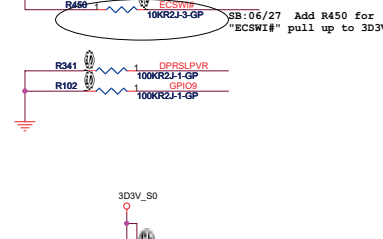
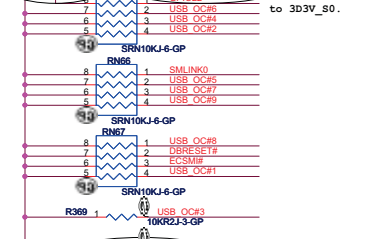
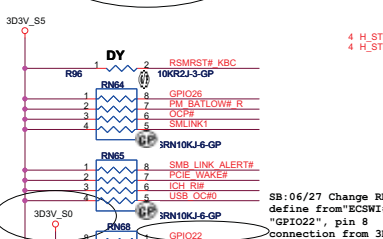
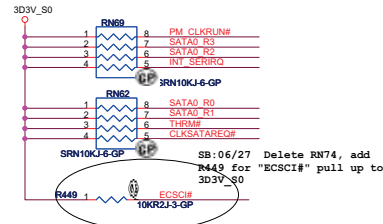


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



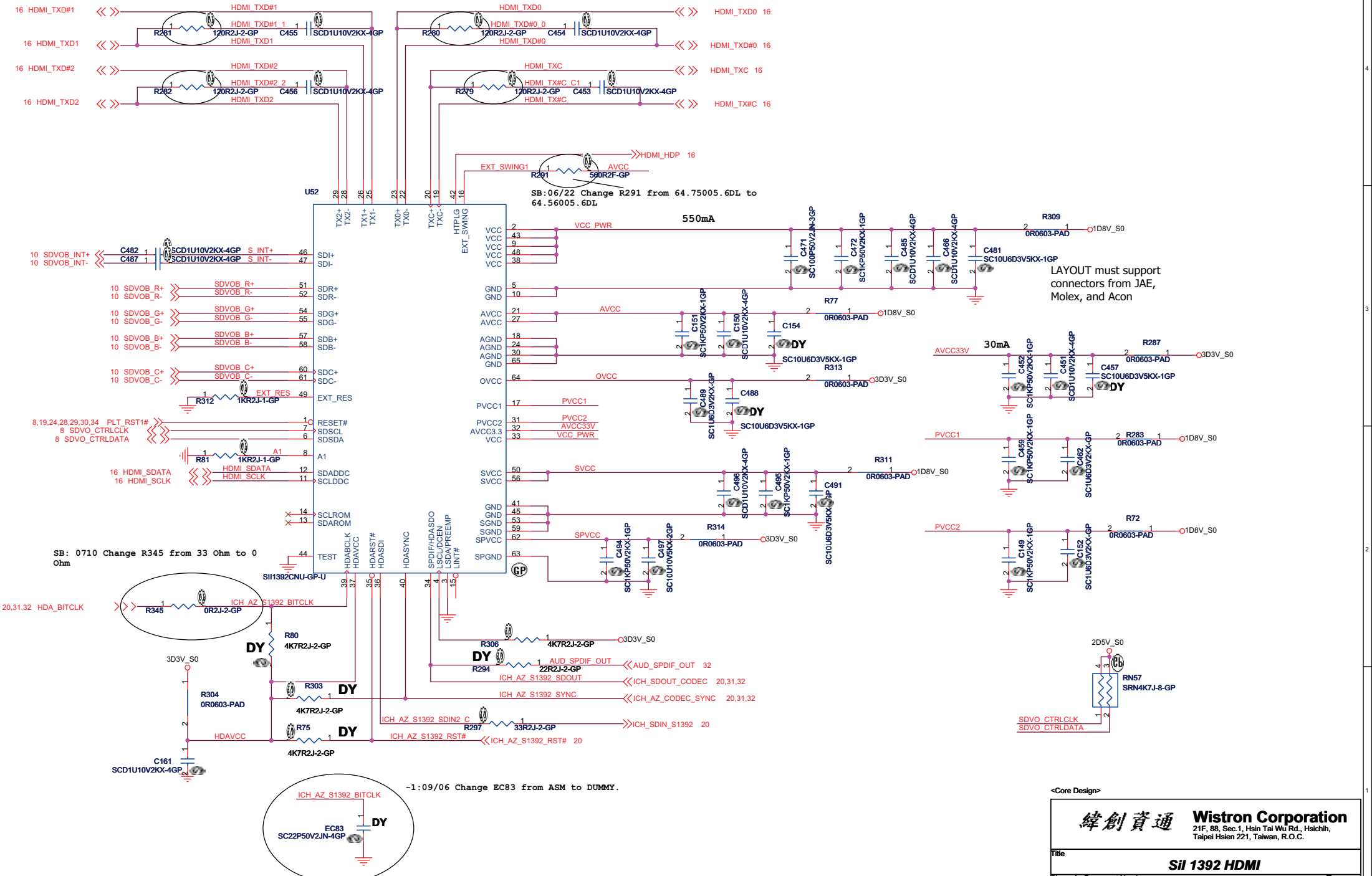








SB:06/22 Change R279,R280,R281,R282 from 63.30134.1DL  
to 63.12134.1DL



LAYOUT must support  
connectors from JAE,  
Molex, and Acon

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Sii 1392 HDMI

Size

A3

Document Number

DS2-Intel

Rev

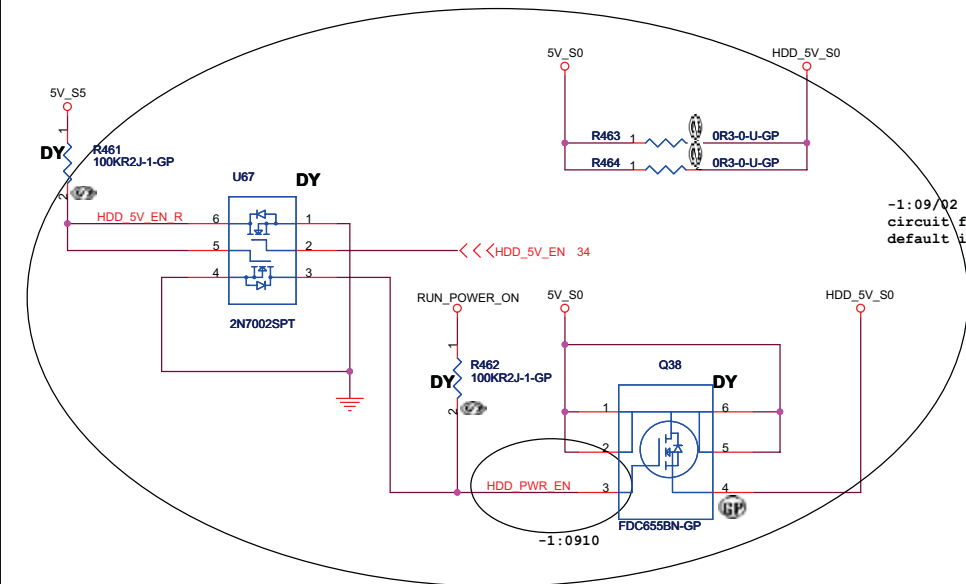
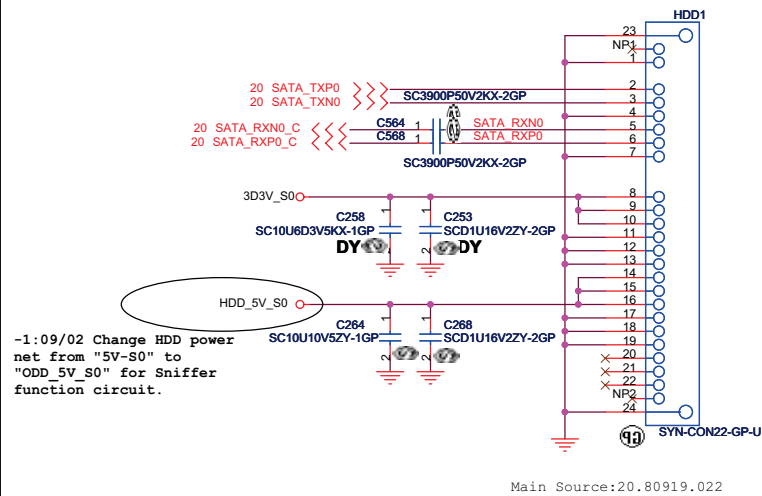
-1

Date: Wednesday, September 12, 2007

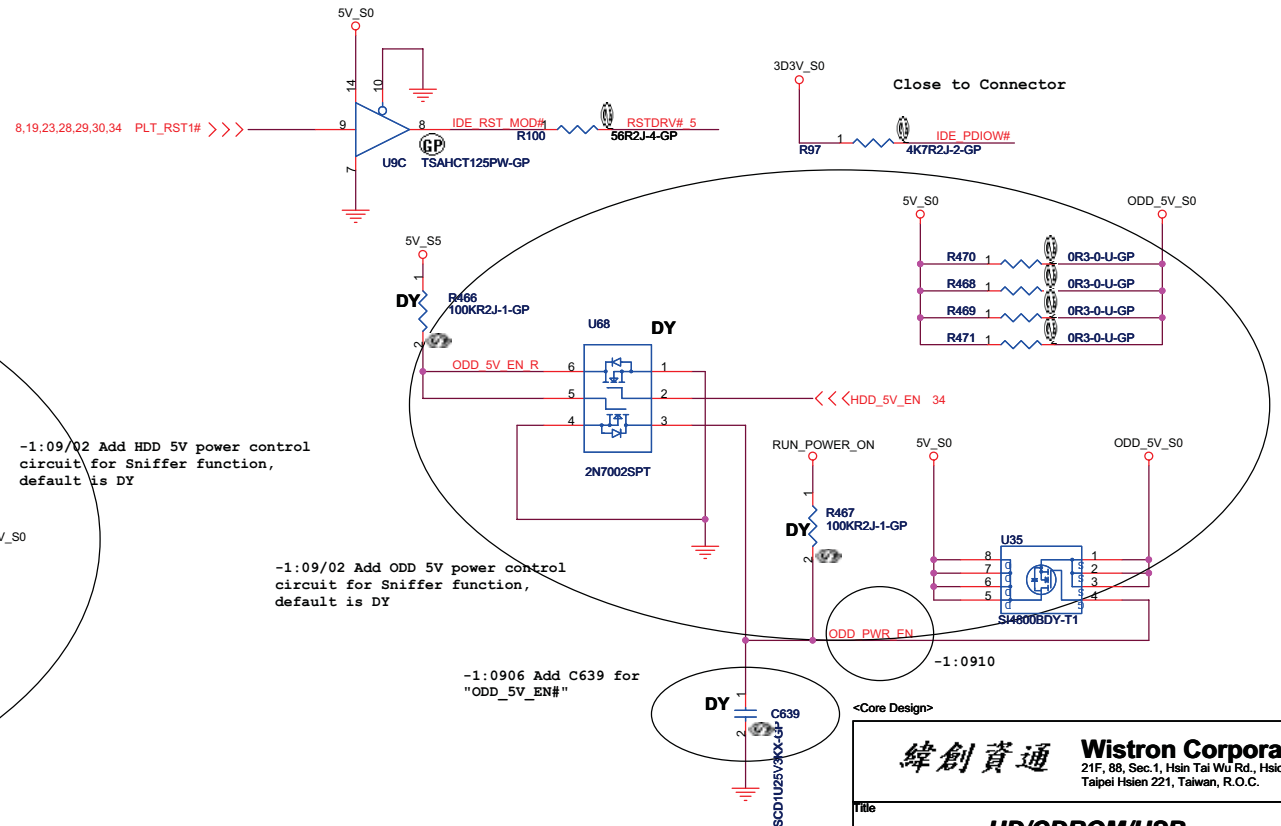
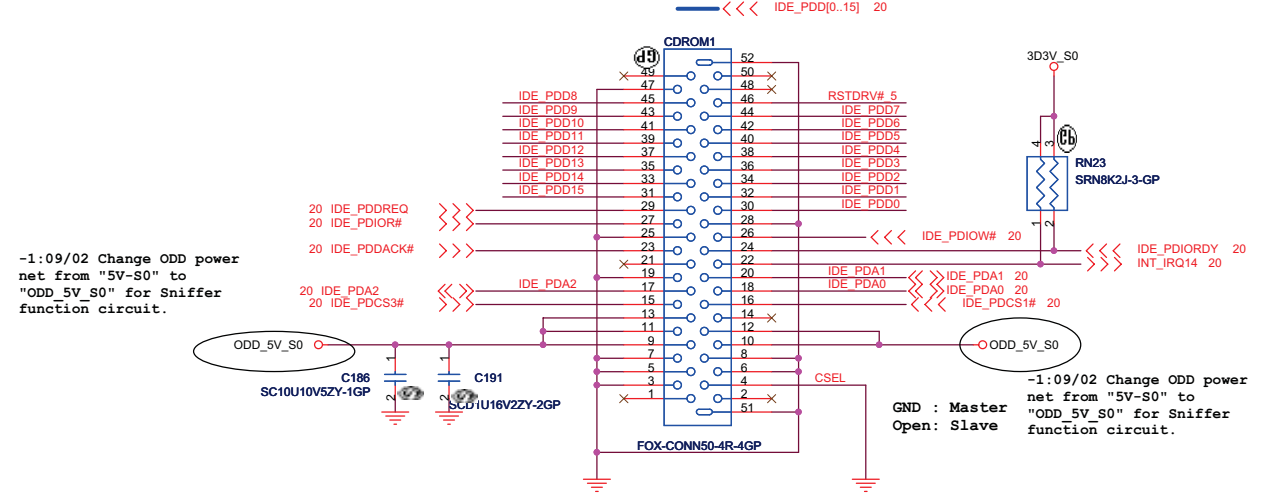
Sheet 23 of 47

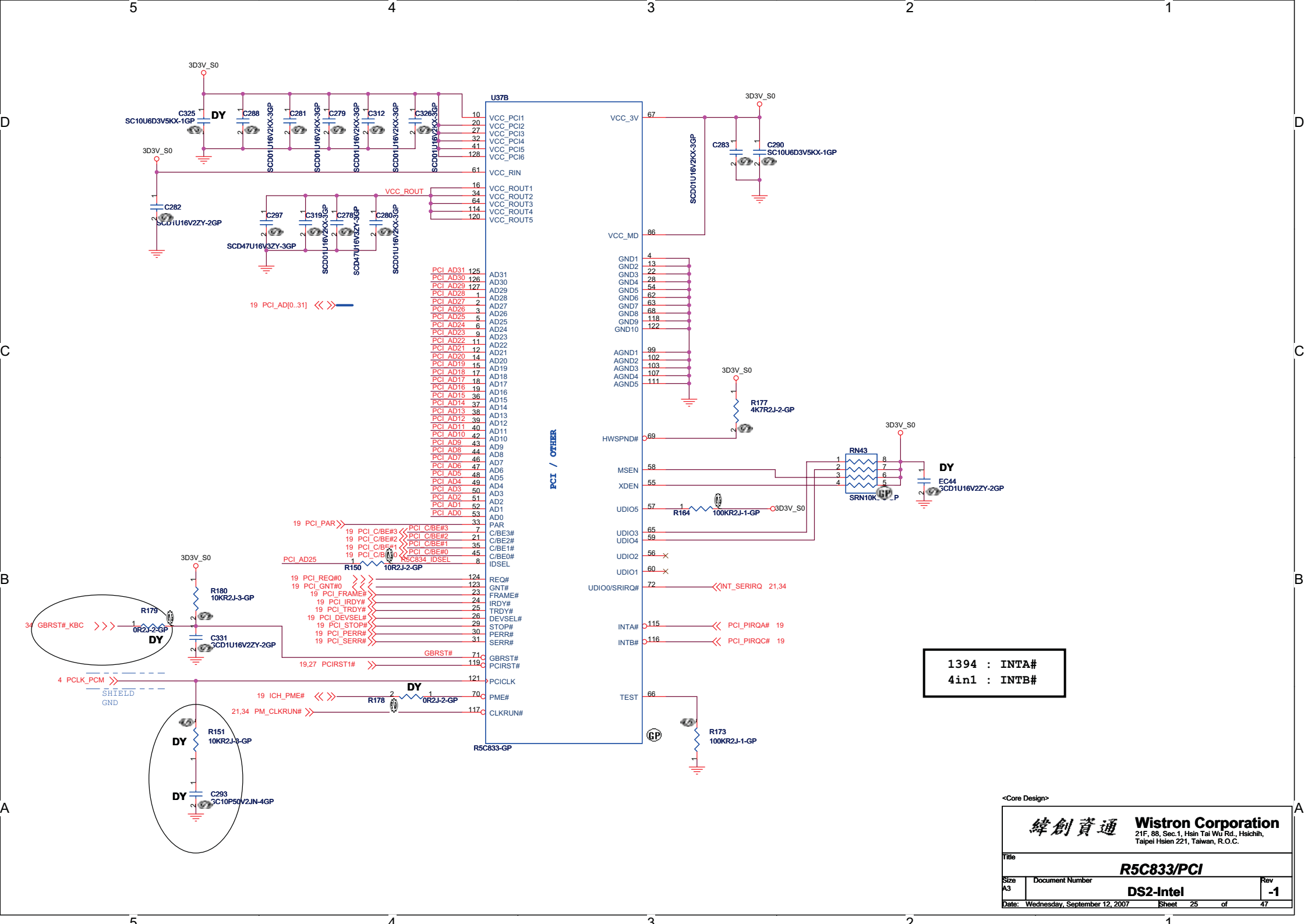
-1:09/06 Change EC83 from ASM to DUMMY.

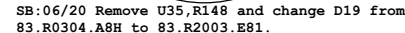
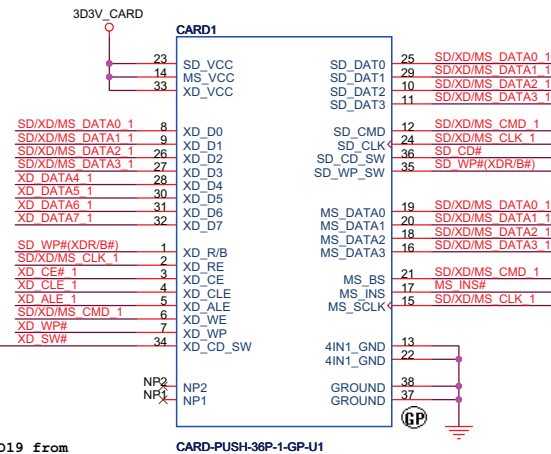
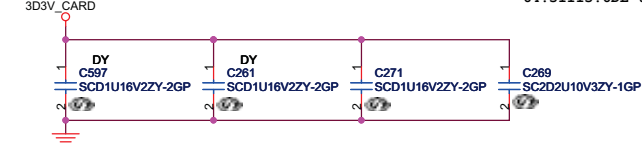
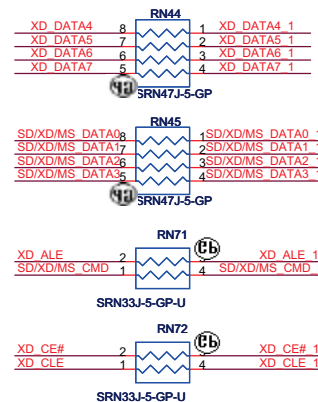
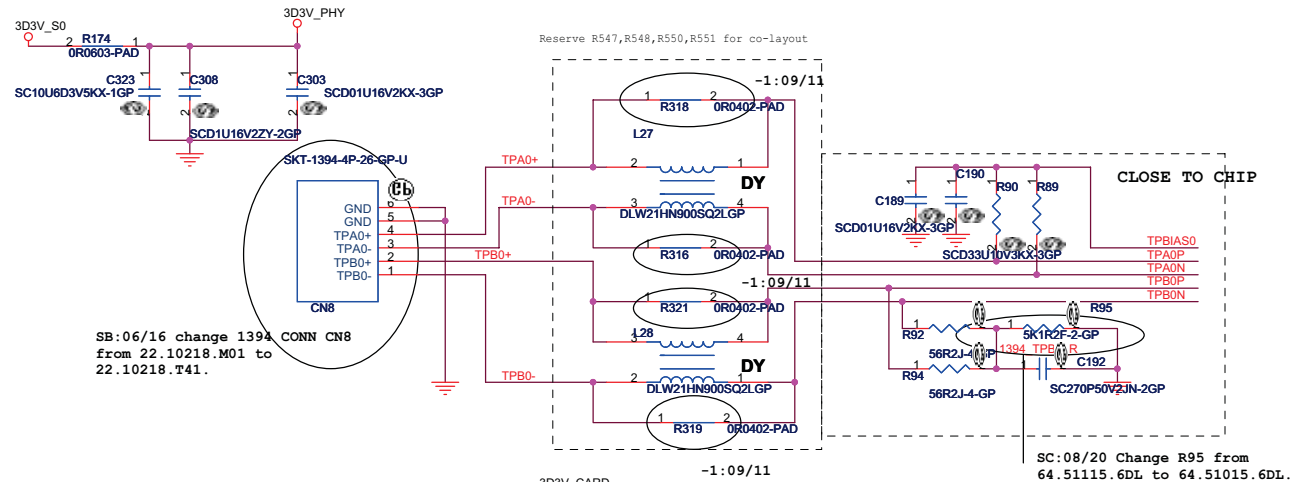
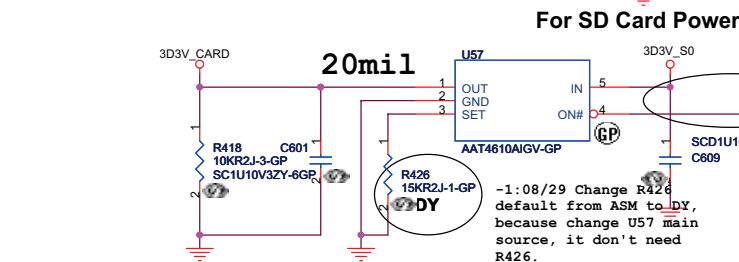
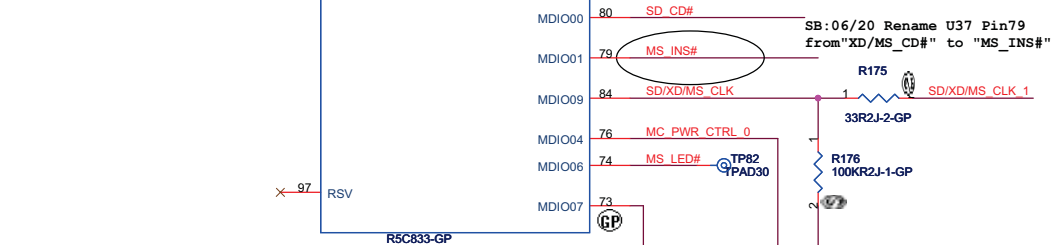
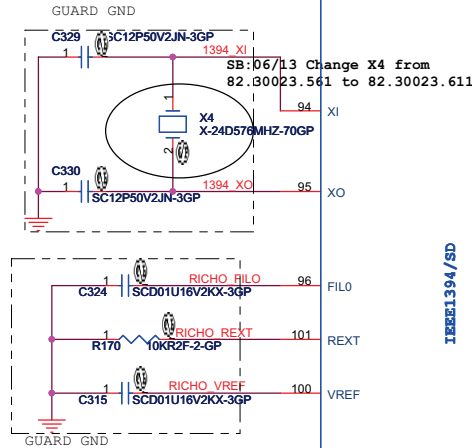
# SATA HD Connector



# CD-ROM Connector







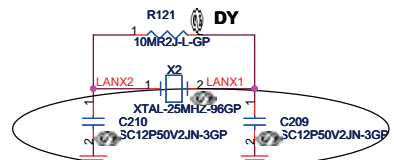
SB:06/20 Remove R427 and change U57  
pin4 connect to "MC\_PWR\_CTRL\_0"

	R426
AAT4610AIGV	15K
RT9711DPBG	DY
G5240D2TIU	DY

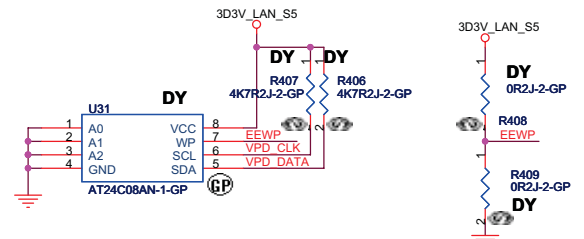


	R394	R354	R357	R362	R372	R377	C528	C544
88E8039	DY	1.91K	49.9	49.9	49.9	49.9	0.01u	0.01u
88E8040	4.7K	2K	DY	DY	DY	DY	DY	DY

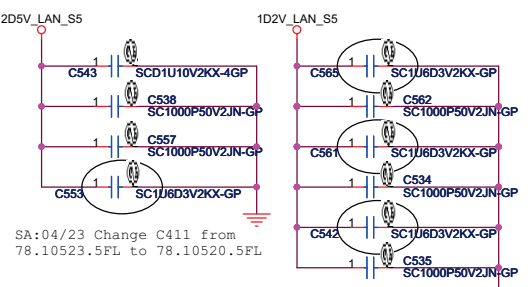
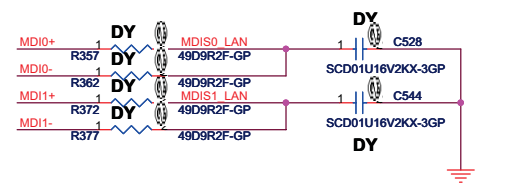
Note: Default is 88E8040



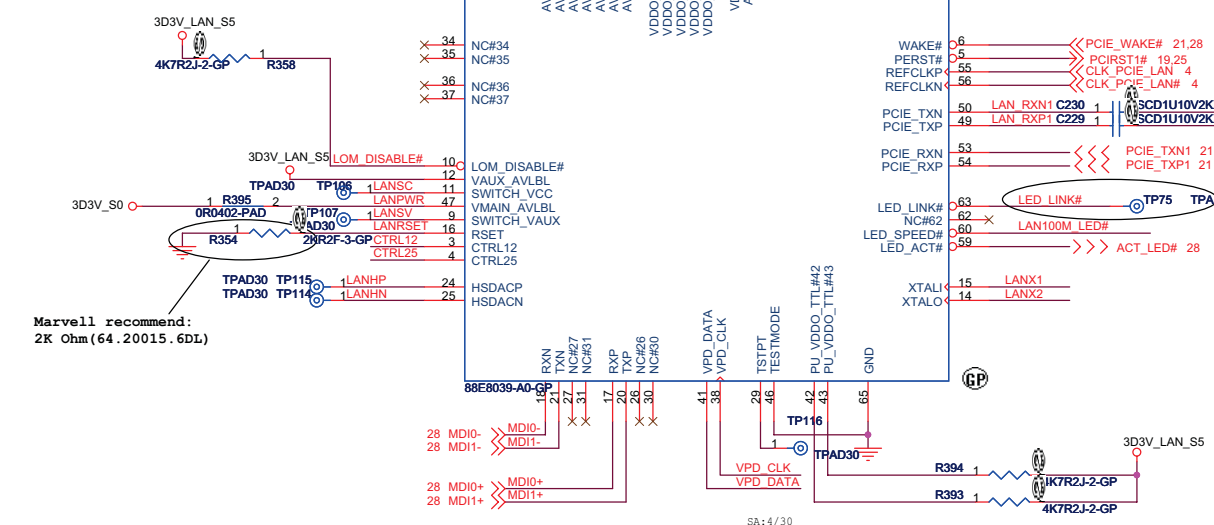
SB:06/13 Change C209,C210 from 27P to 12P



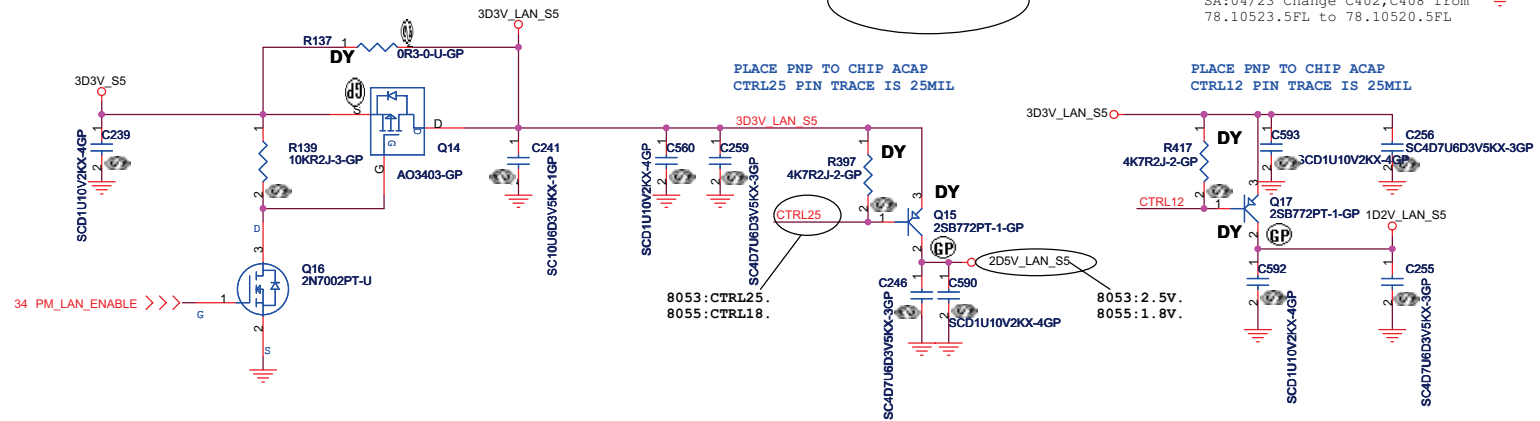
Pull up for AT24C08 another pull low



SA:04/23 Change C411 from 78.10523.5FL to 78.10520.5FL

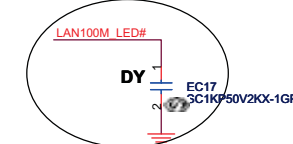
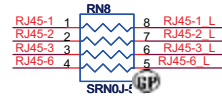
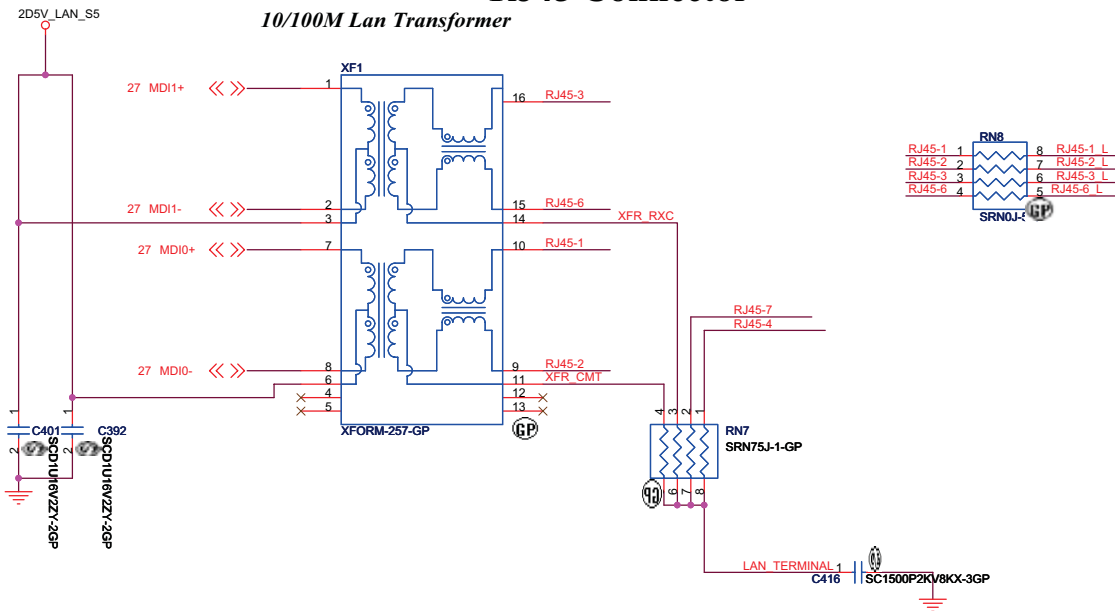


	R397	Q15	R417	Q17
88E8039	4K7	2SB772PT	4K7	2SB772PT
88E8040	DY	DY	DY	DY



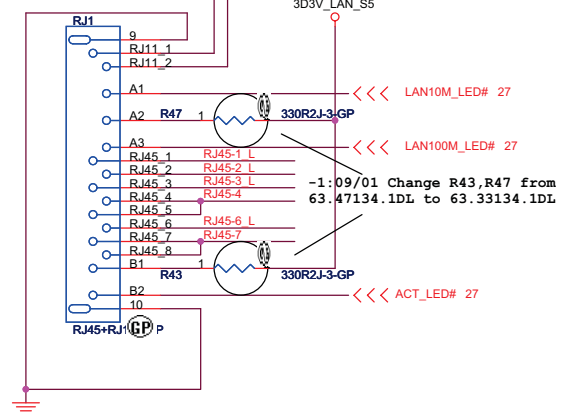
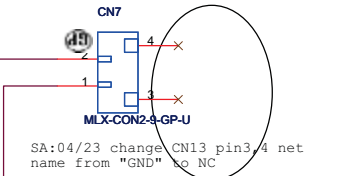
# RJ45 Connector

## 10/100M Lan Transformer



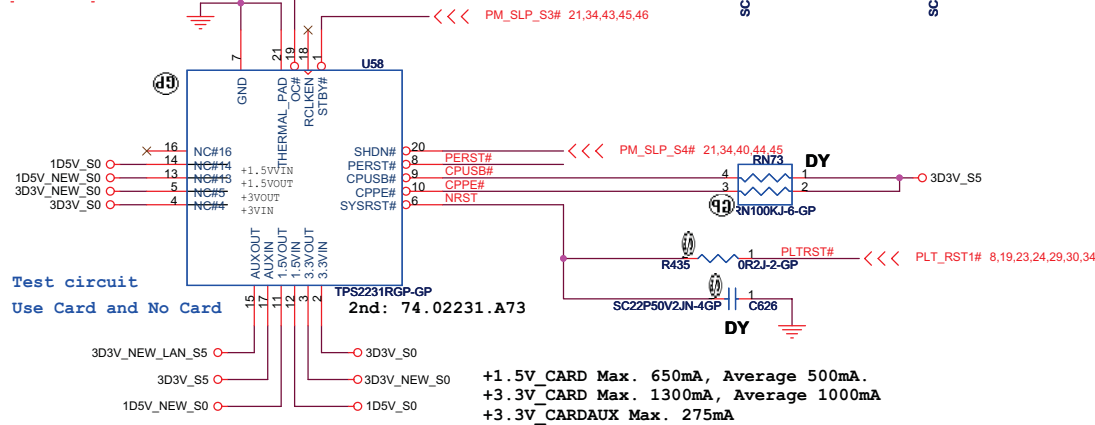
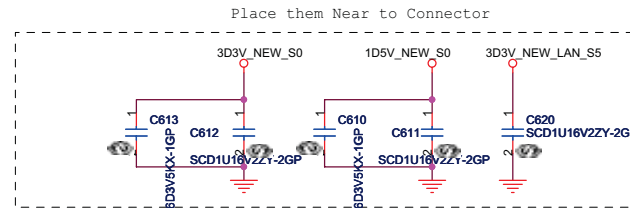
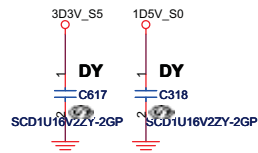
Green : Link up  
Blinking : TX/RX activity

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.



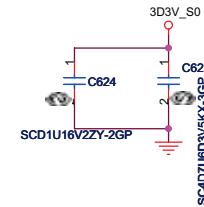
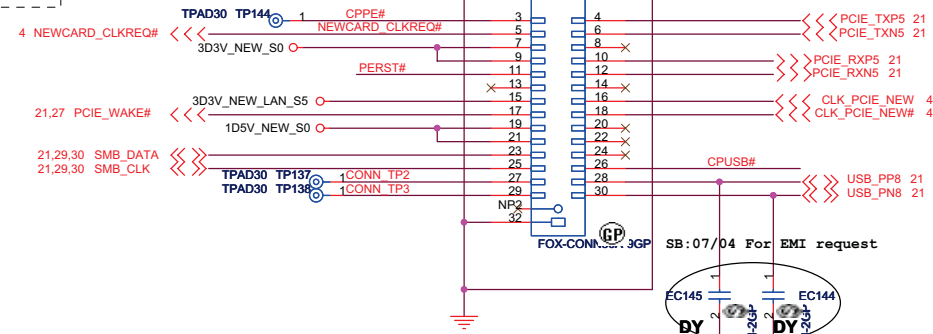
# NEWCARD Connector

Place them Near to Chip



Test circuit  
Use Card and No Card

+1.5V\_CARD Max. 650mA, Average 500mA.  
+3.3V\_CARD Max. 1300mA, Average 1000mA  
+3.3V\_CARDAUX Max. 275mA

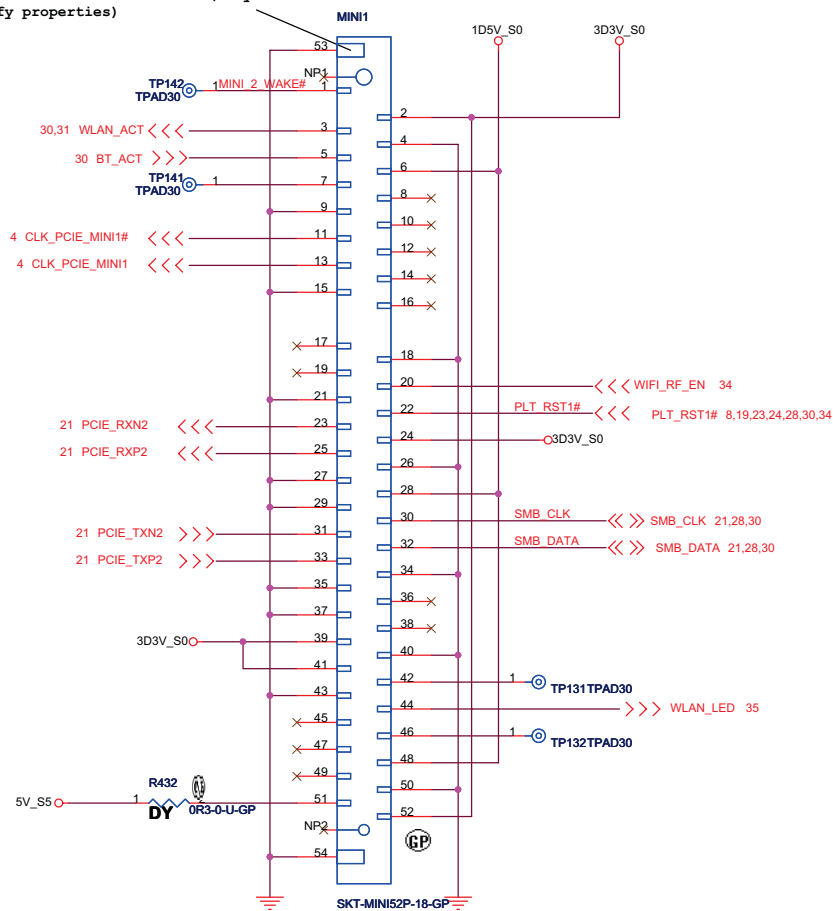


<Core Design>

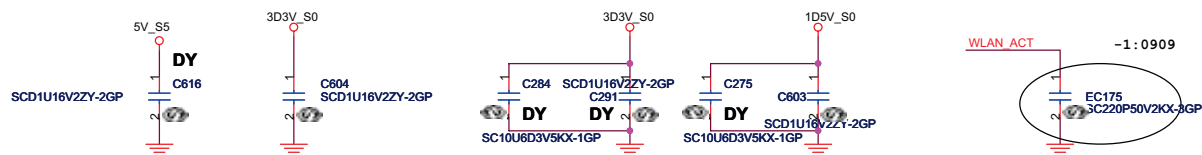
<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	<b>LAN connector/NEW CARD/SIM</b>
Size	A3
Document Number	<b>DS2-Intel</b>
Date	Wednesday, September 12, 2007
Sheet	26 of 47
Rev	<b>-1</b>

# Mini Card Connector 1(802.11a/b/g)

SB:06/22 Change MINI1,2,3 slot from  
62.10043.431 to 62.10043.551 (only  
modify properties)



Main Source:62.10043.431  
2nd Source: 20.F0992.052



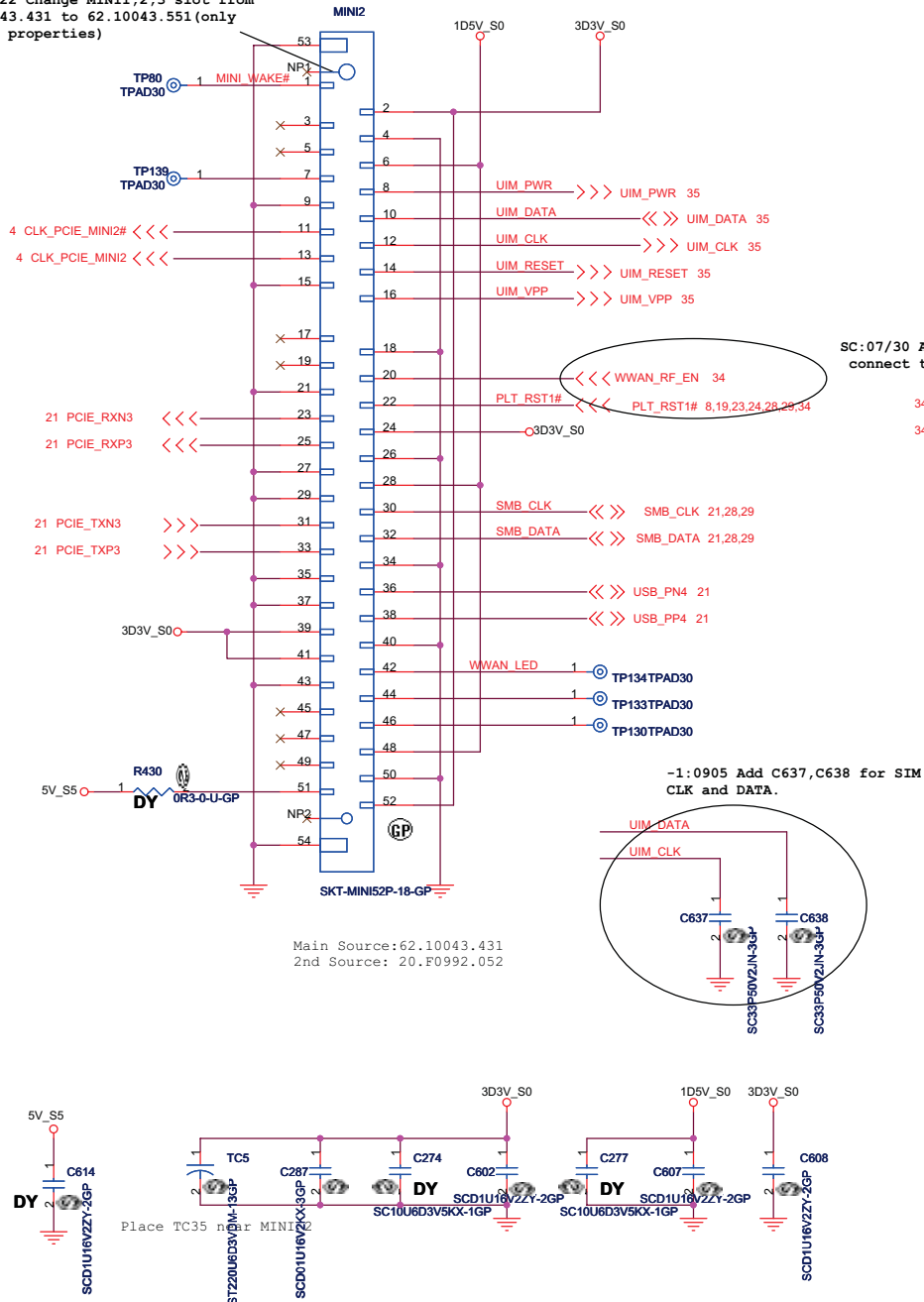
<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MINI CARD CONN 1			
Size A3	Document Number	Rev -1	
DS2-Intel			
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# Mini Card Connector

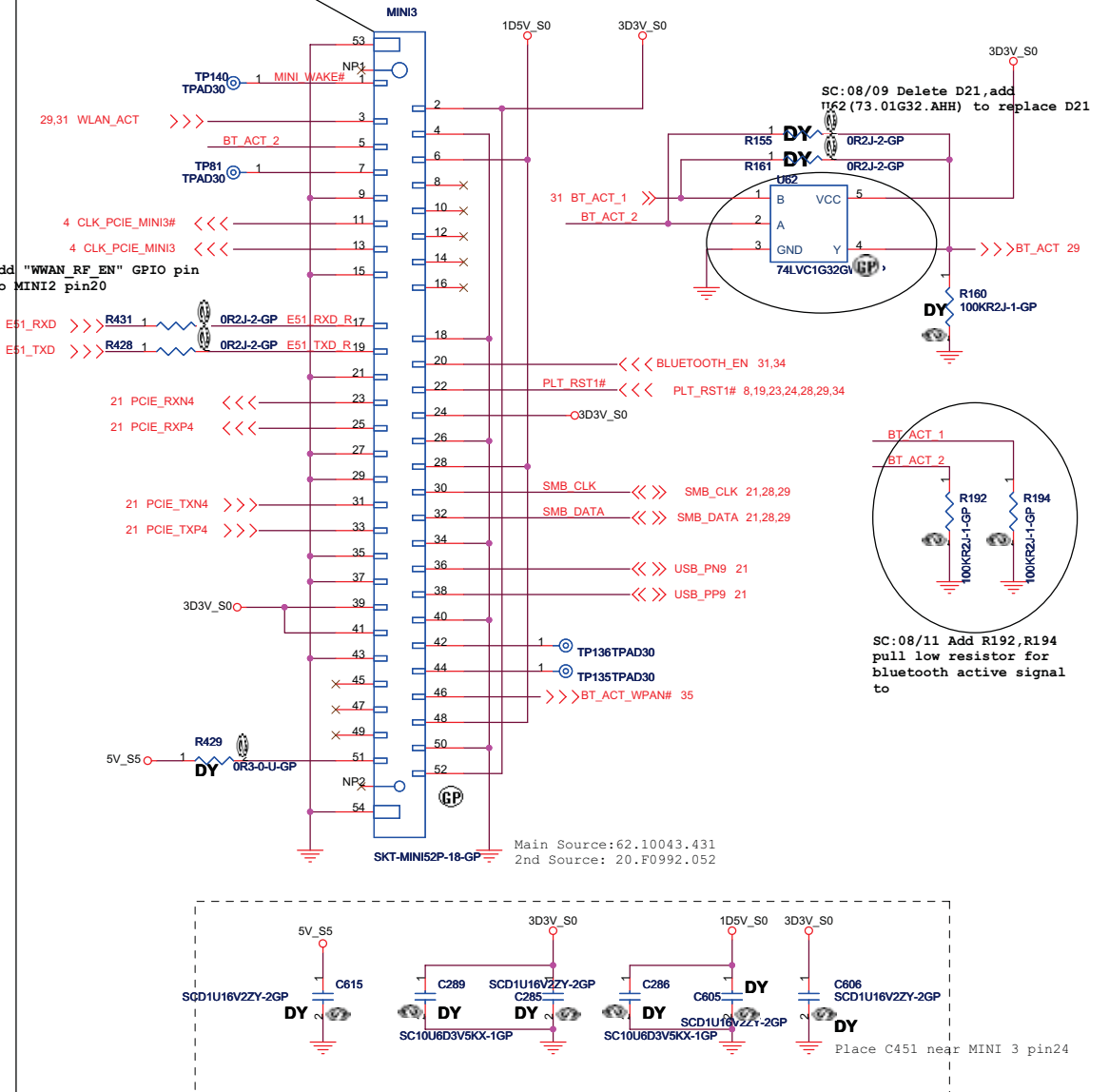
## Mini Card Connector 2(WWAN)

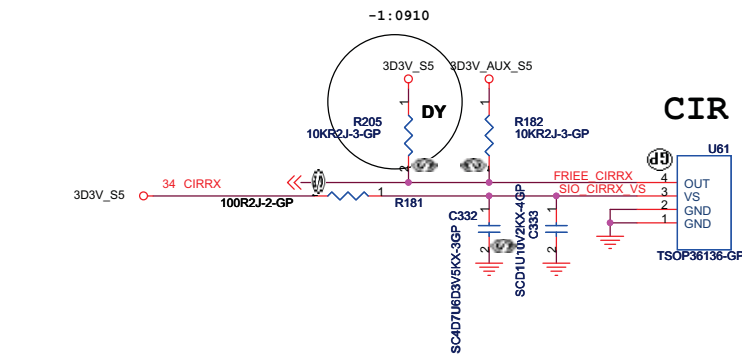
SB:06/22 Change MINI1,2,3 slot from 62.10043.431 to 62.10043.551(only modify properties)



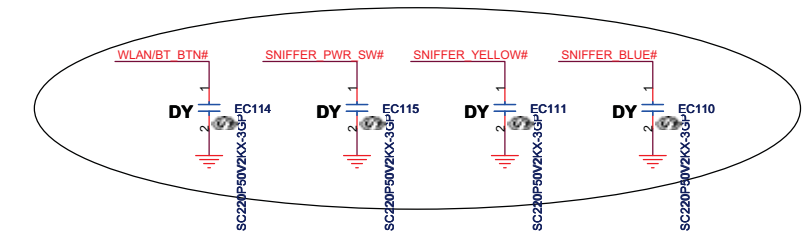
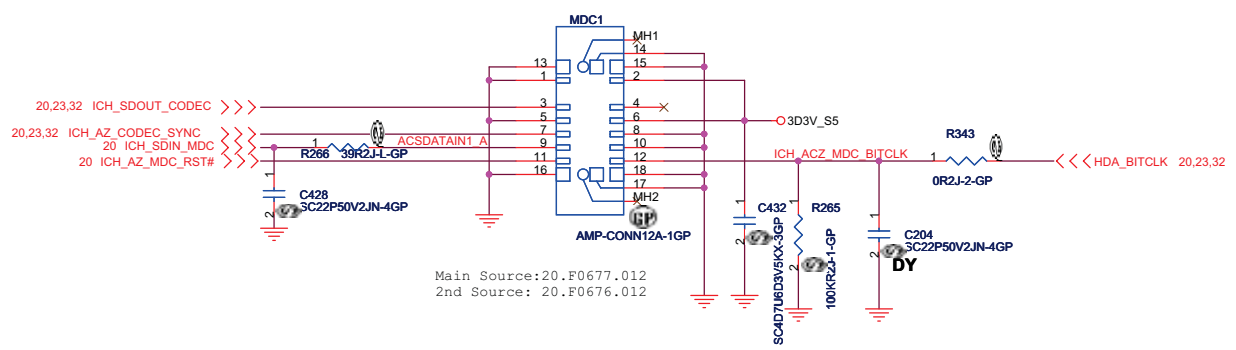
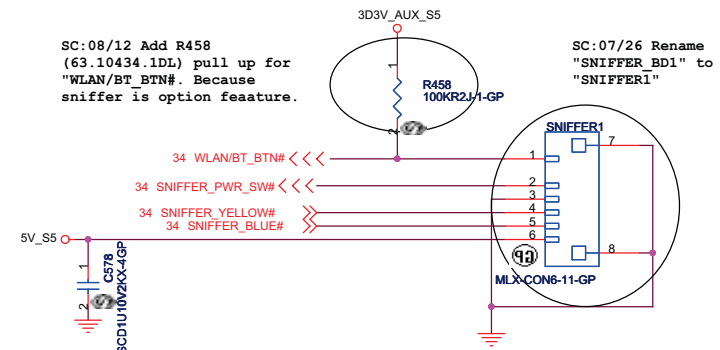
# Mini Card Connector 3(Robson)

SB:06/22 Change MINI1,2,3 slot from 62.10043.431 to 62.10043.551(only modify properties)

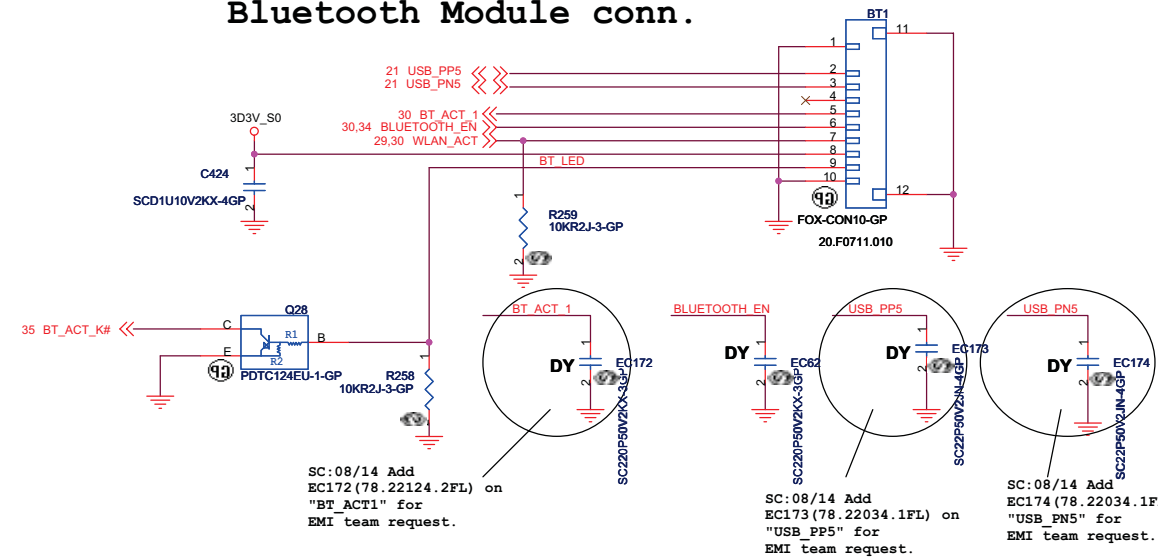




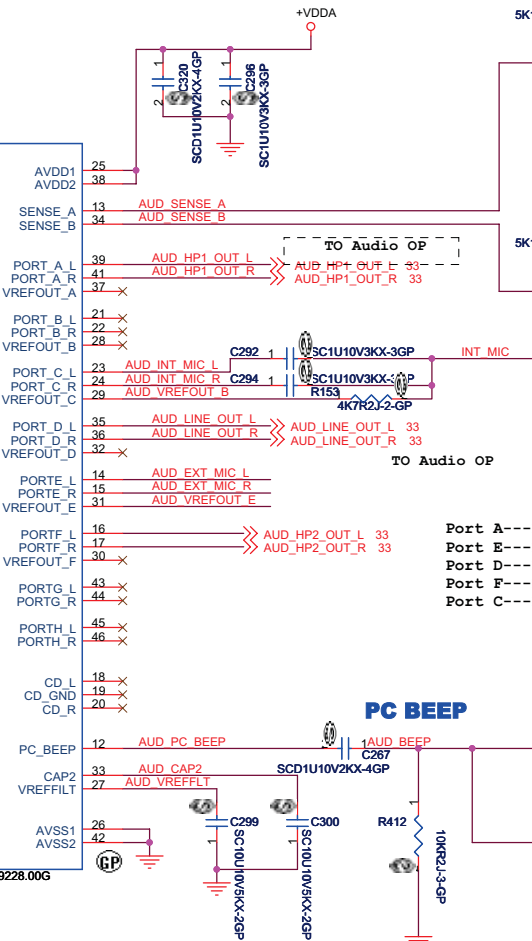
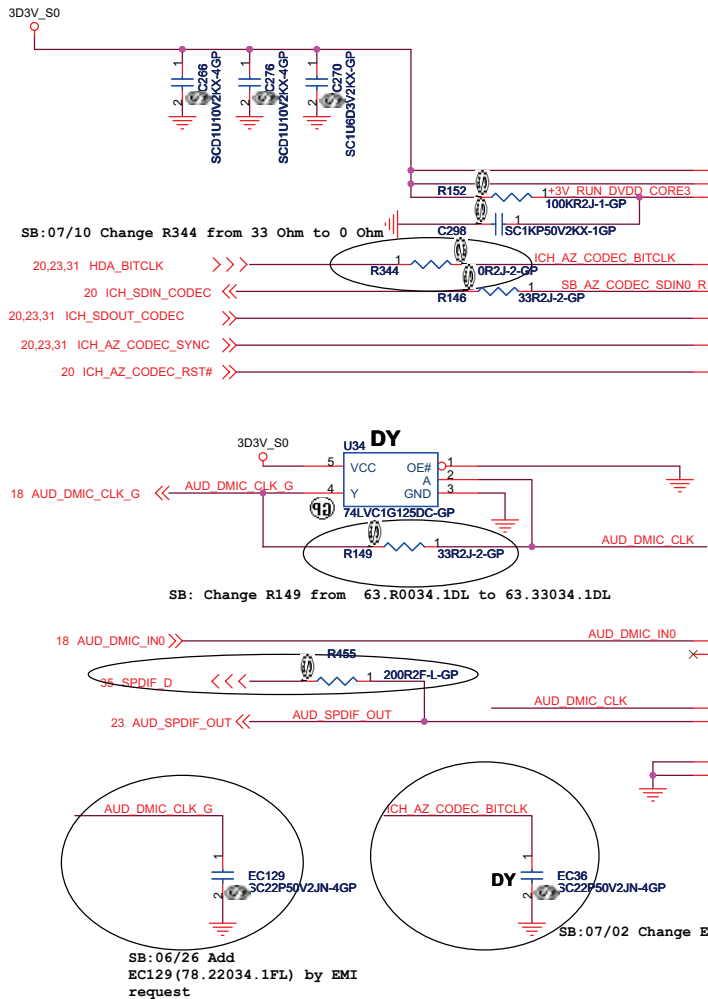
# CIR



# Bluetooth Module conn.



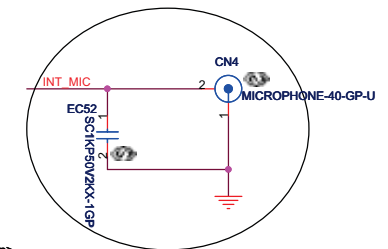
60ohm 100MHz  
3000mA 0.05ohm DC



Port A---> HP1  
Port E---> Ext Mic  
Port D---> Speaker  
Port F---> HP2  
Port C--->Int Mic

## Internal Microphone

-1:09/06 Change Int. MIC from  
23.42132.001 to 23.42143.001

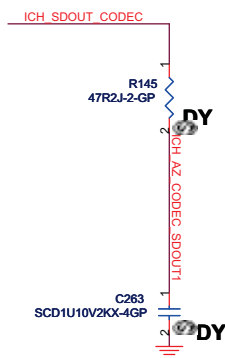


<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title			AUDIO CODEC STAC9228		
Size	A3	Document Number	DS2-Intel		
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					Rev -1

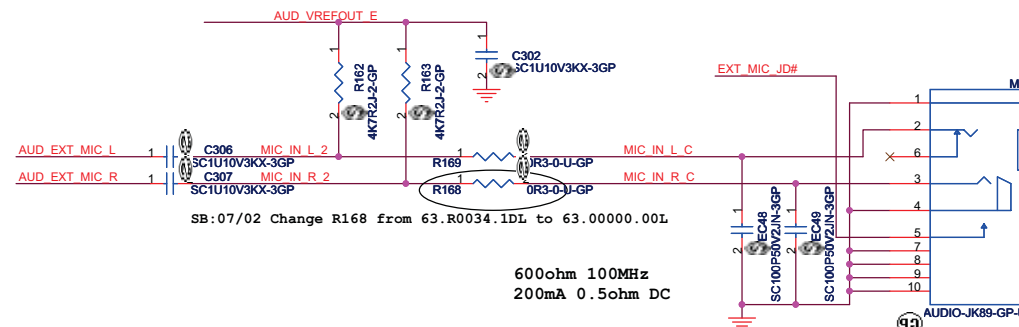
## Azalia I/F EMI



## Azalia I/F EMI



## MIC IN

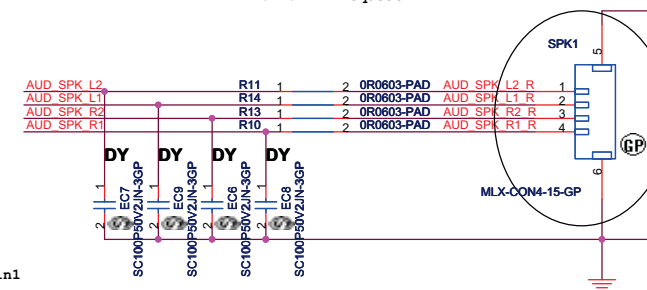


600ohm 100MHz  
200mA 0.5ohm DC

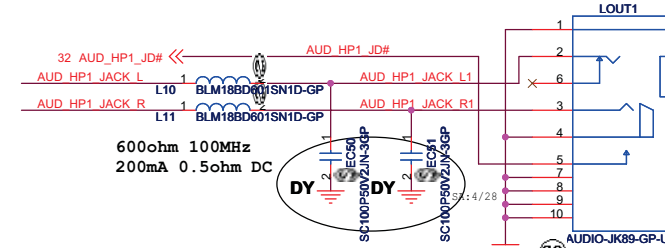


# Speaker

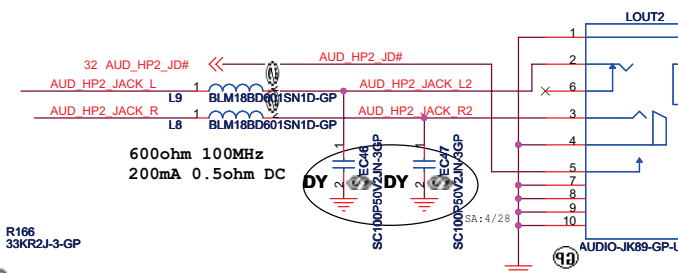
SC:08/11 Change SPK1 pin define that follow ME request



## LINE1 OUT



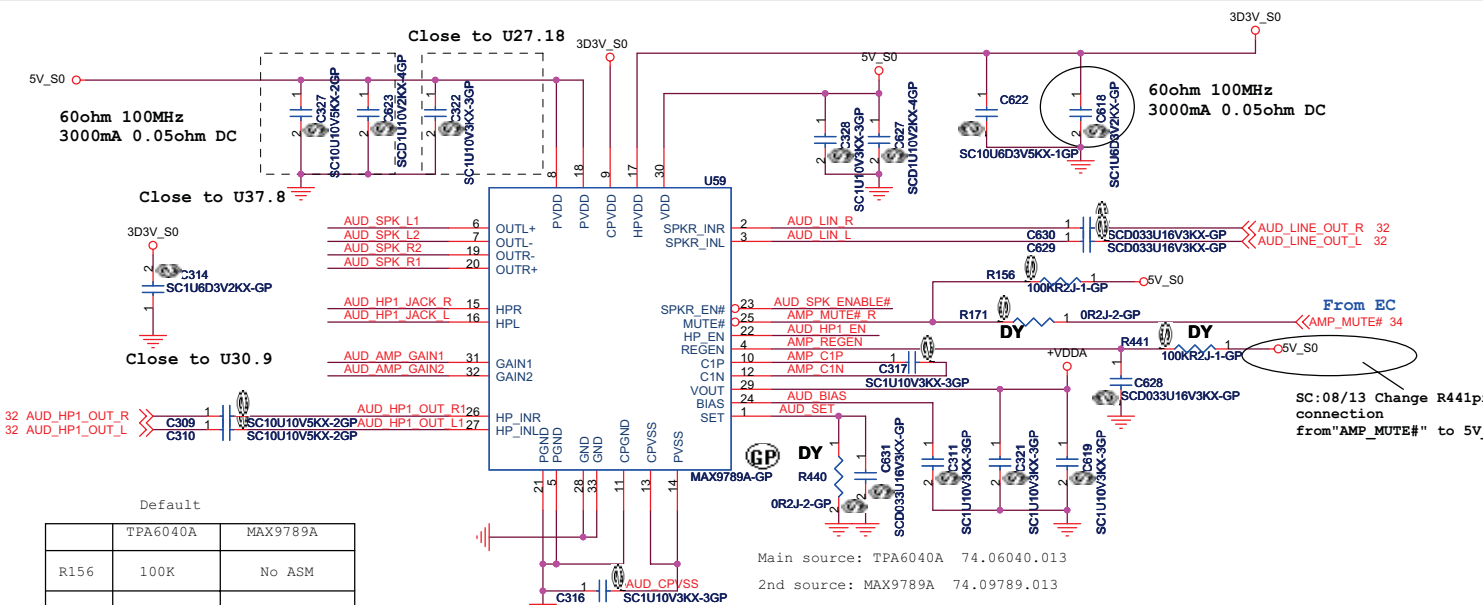
## LINE2 OUT



<Core Design>

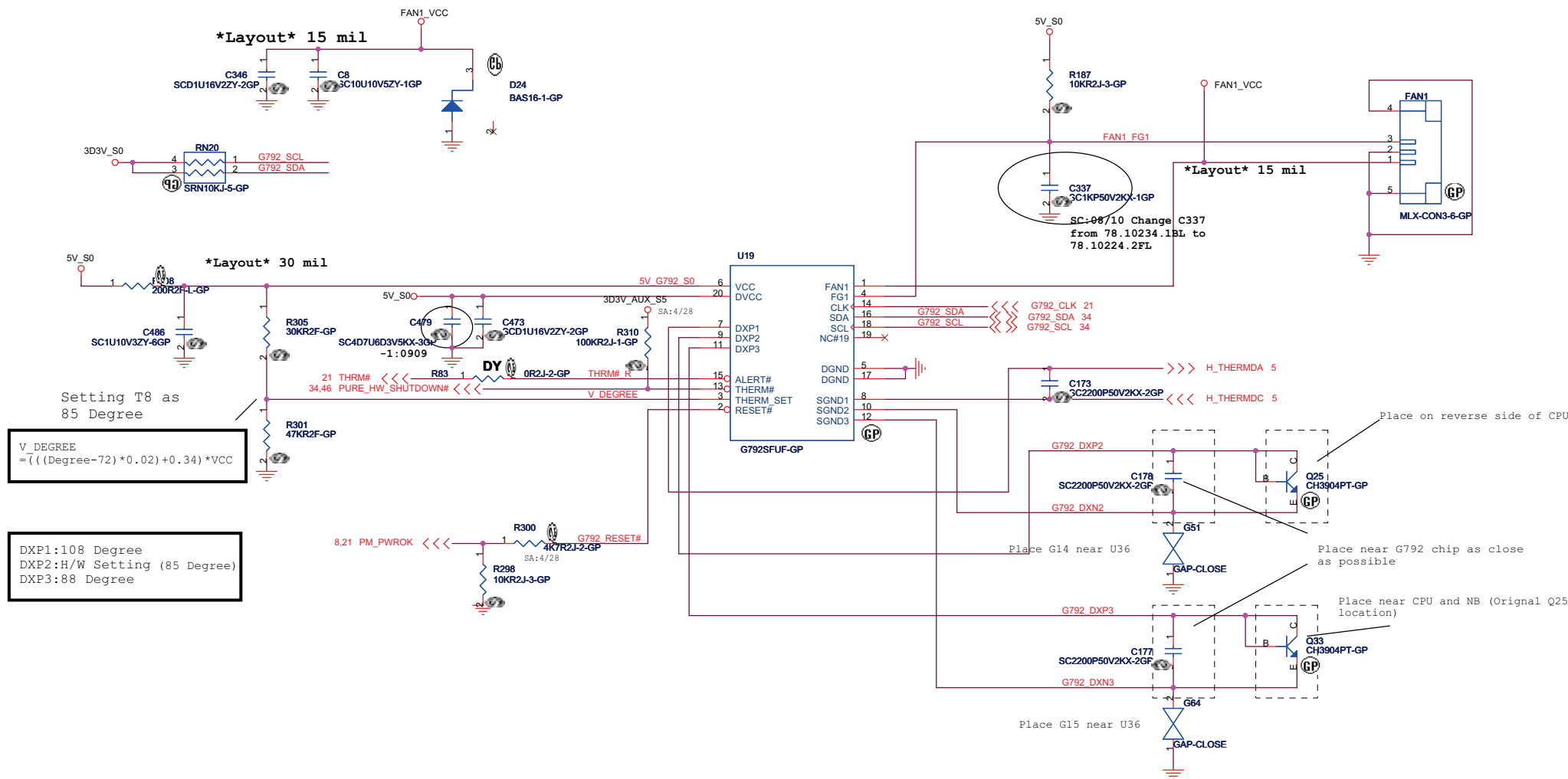
**緯創資通 Wistron Corporation**  
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Title		
AUDIO AMP/SPEAKER		
Size	Document Number	Rev
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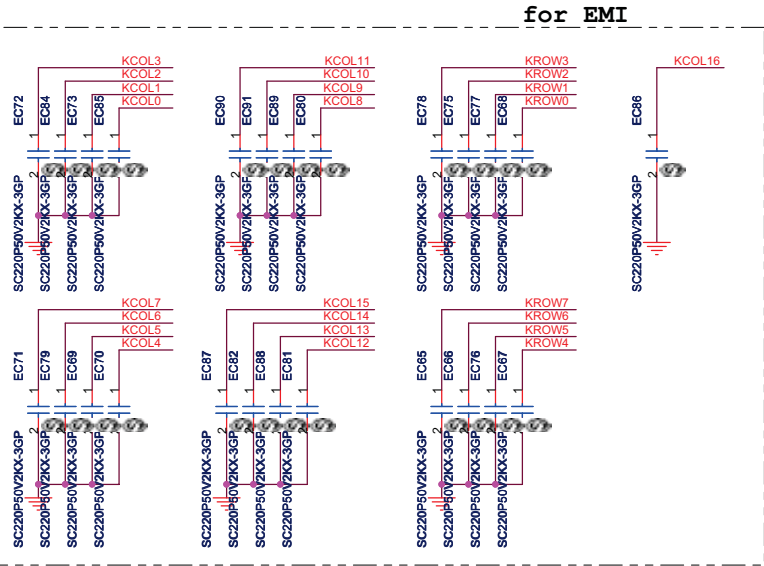
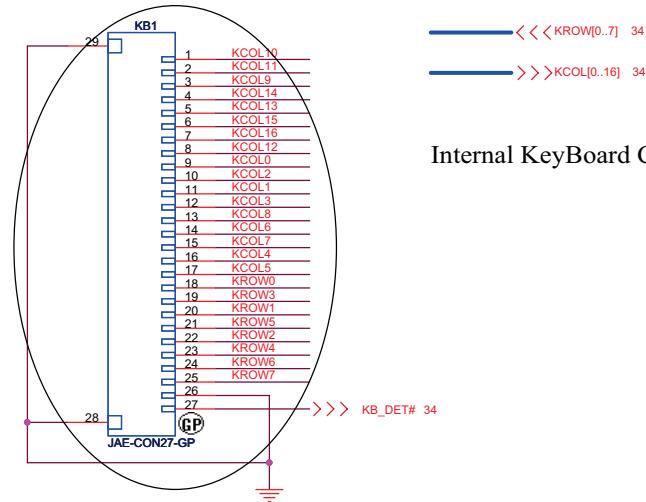




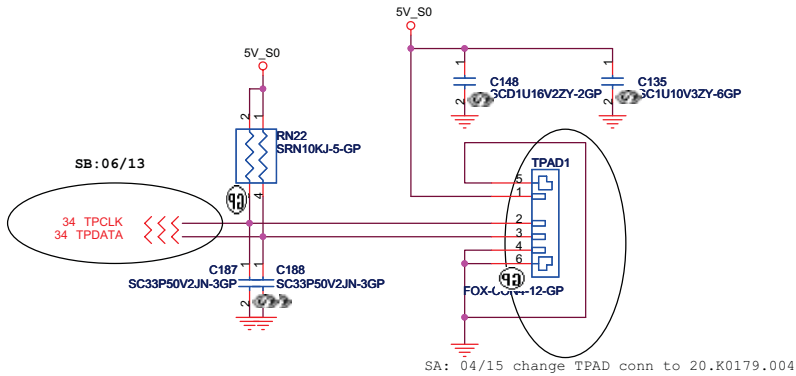




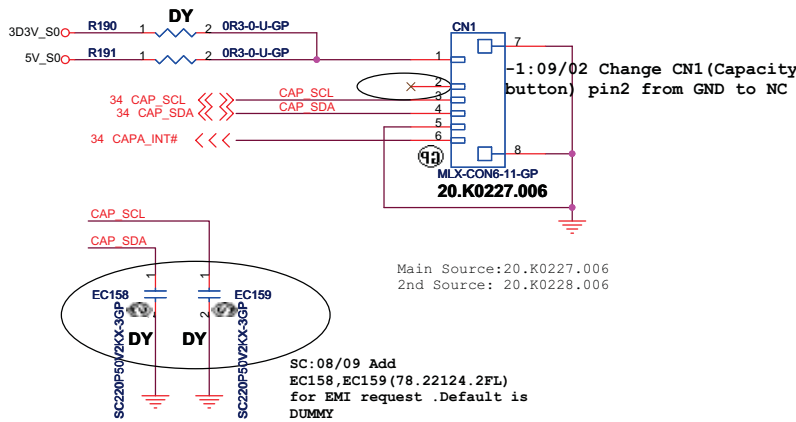
<Core Design>



## TouchPad Connector

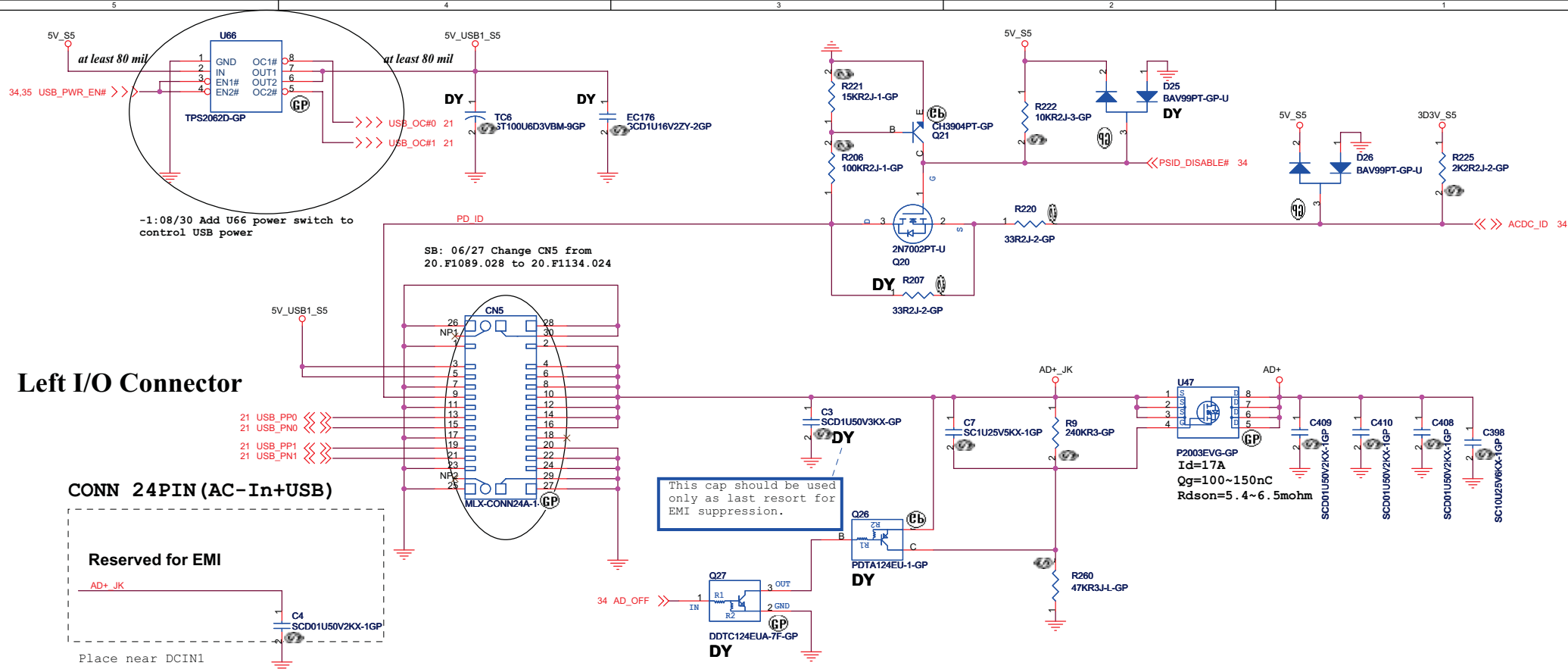


## CAPACITY BUTTON



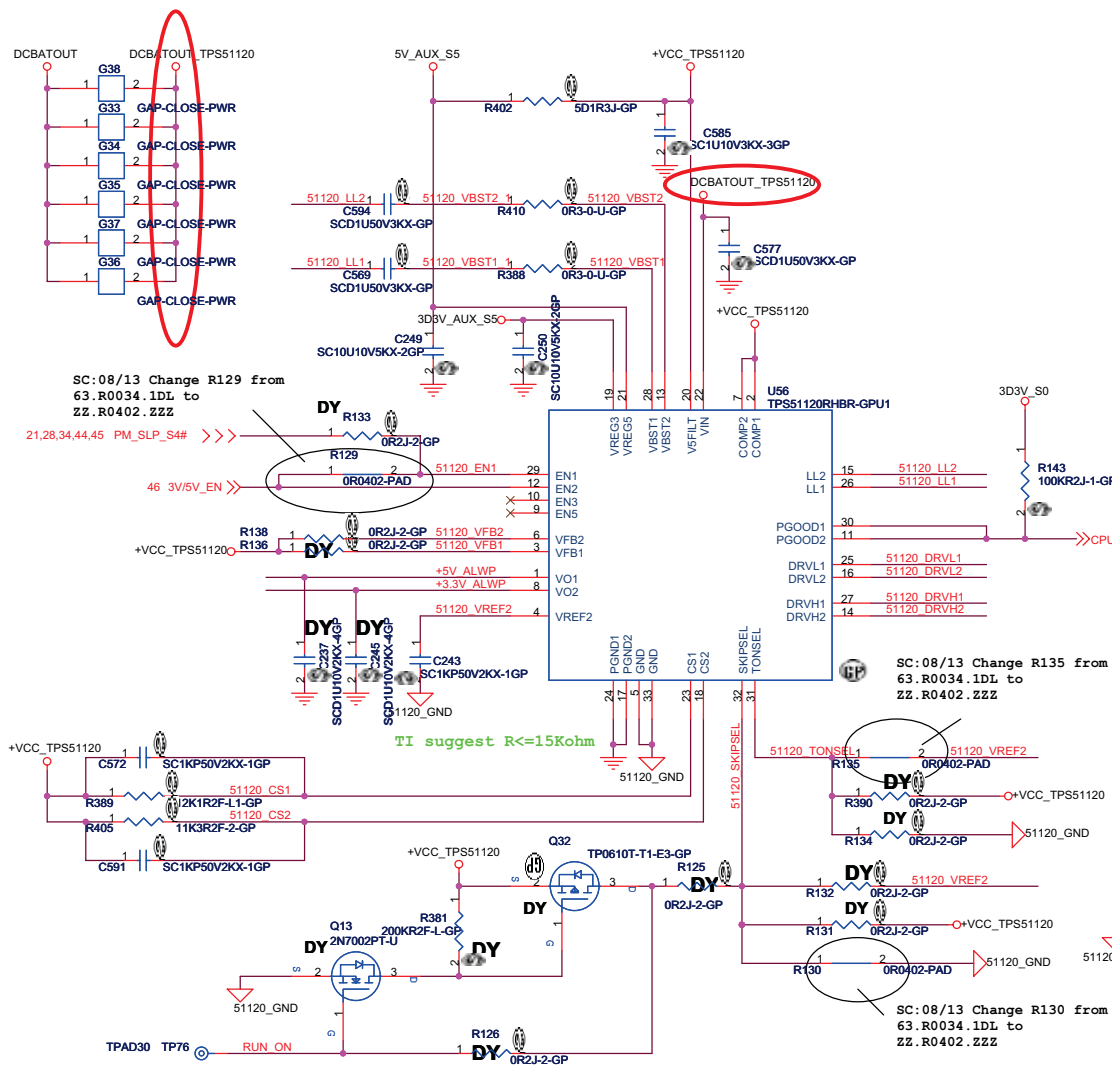
<Core Design>

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>KeyBoard-CONN</b>			
Size	Document Number	Rev	
A3		<b>DS2-Intel</b>	
Date: Wednesday, September 12, 2007		Sheet 37 of 47	<b>-1</b>



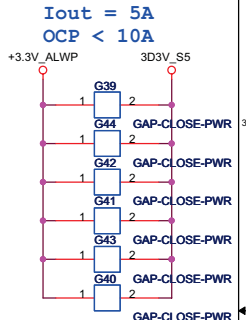
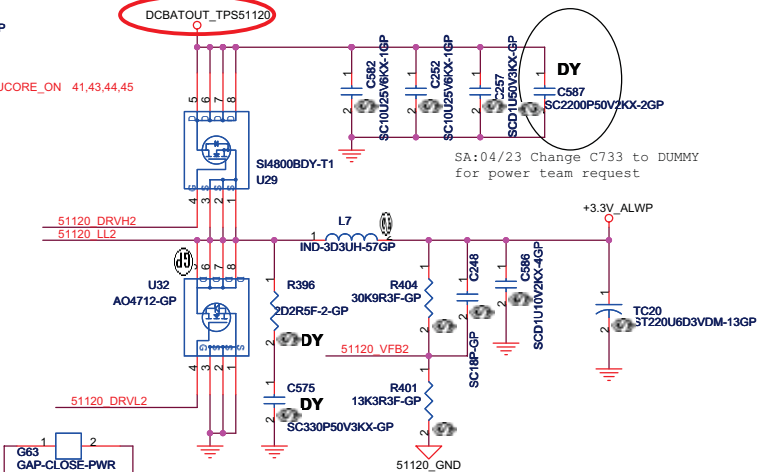
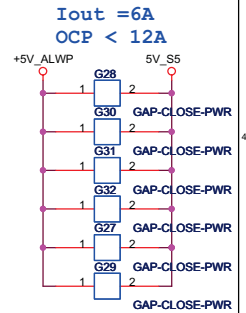
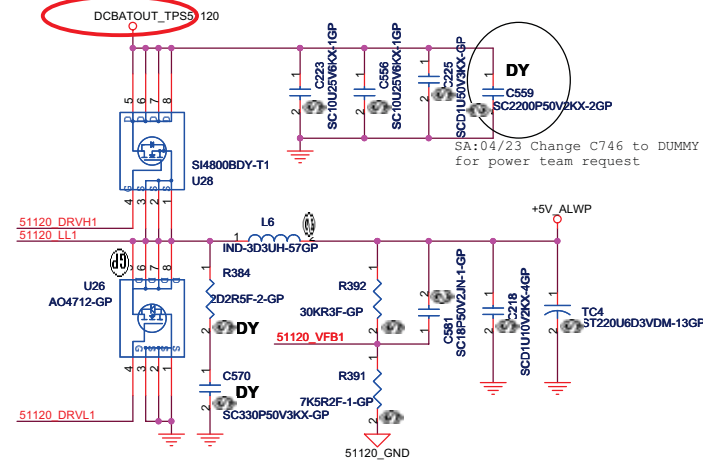






$$V_{out} = 1V * (R1 + R2) / R2$$

	SKIPSEL	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	5V Adj.	Fixed Output
VFB2	N/A	not use	Adj.	3.3V Fixed Output
EN1, EN2	Switcher OFF	not use	Switcher ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
 Inductor: 3.3UH CYNTEC 11Arms 14.5Apeak  
 O/P cap: 220U6.3V 6TPE220M 25mOhm 2.4Arms/ 77.22271.17L  
 H/S: AO4468 SO-8/ 30mOhm/ 4.5Vgs  
 L/S: AO4712 SO-8/ 7.3mOhm/ 4.5Vgs

<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C.

Title

**DC to DC 3.3V & 5V**

Size

Document Number

**DS2-Intel**

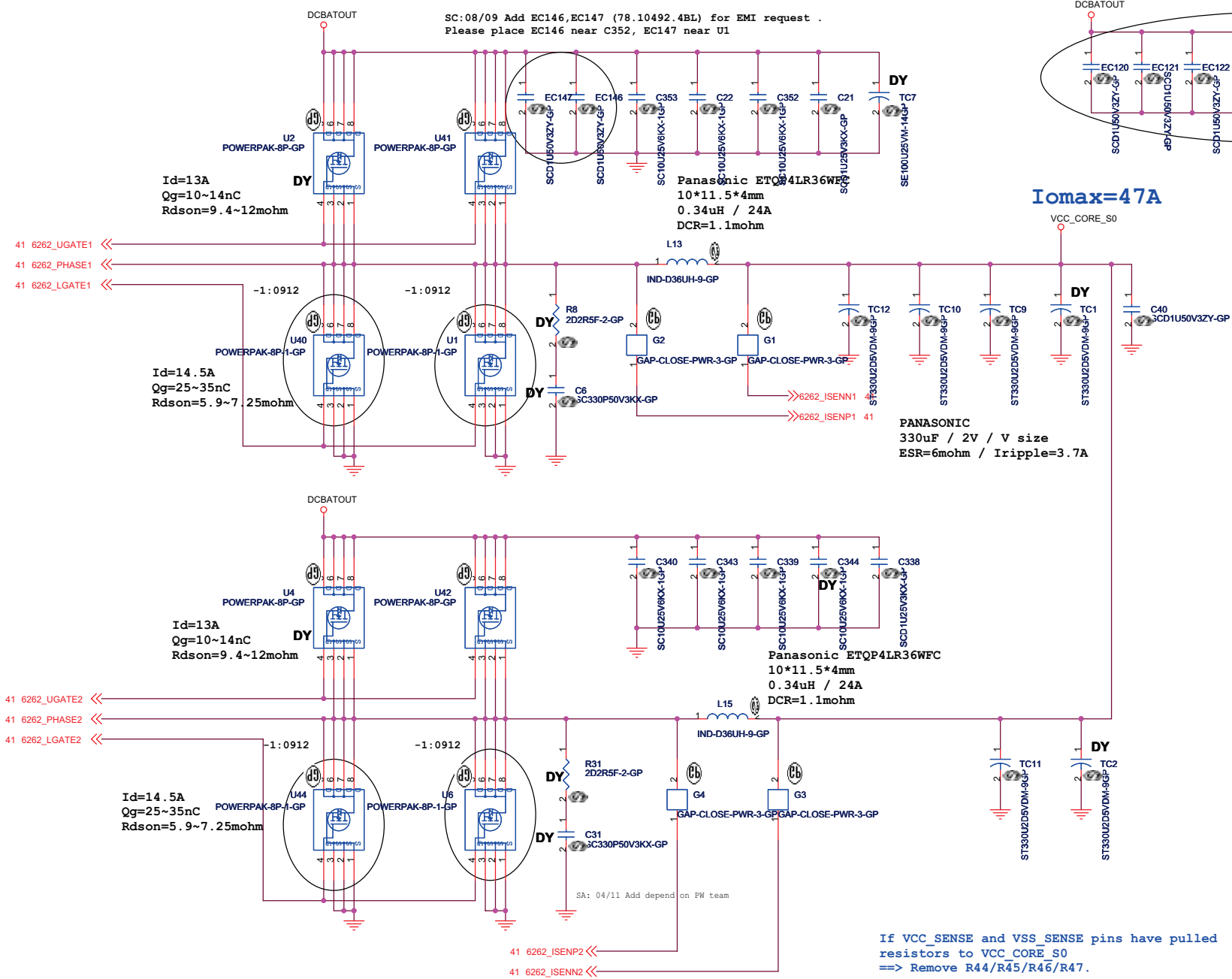
Rev

**-1**

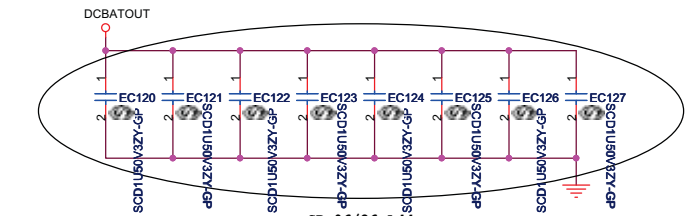
Date: Wednesday, September 12, 2007

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Iomax=47A



If VCC\_SENSE and VSS\_SENSE pins have pulled  
resistors to VCC\_CORE\_S0  
==> Remove R44/R45/R46/R47.



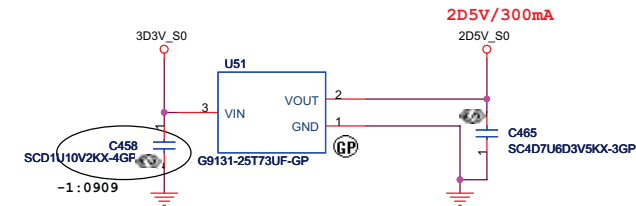
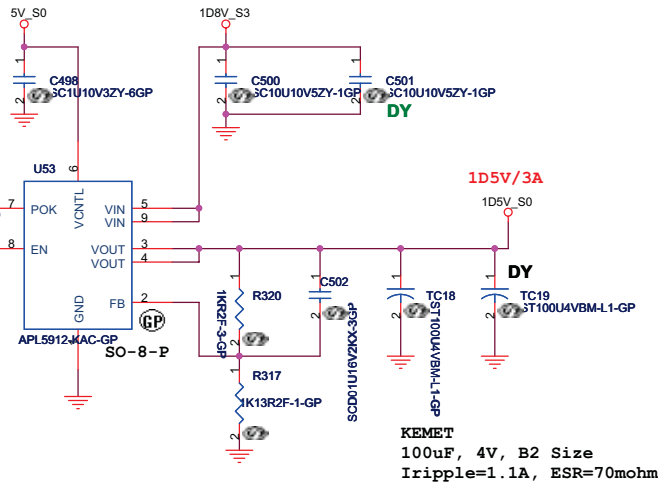




## 1D5V\_SB

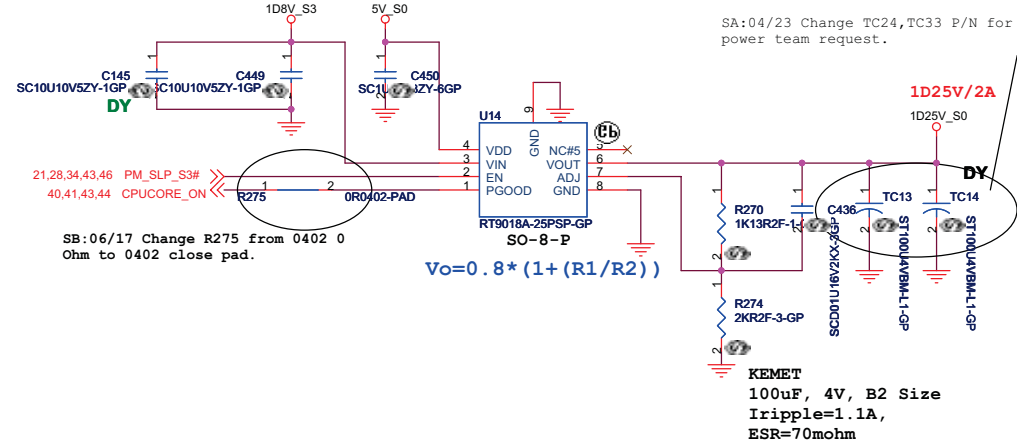
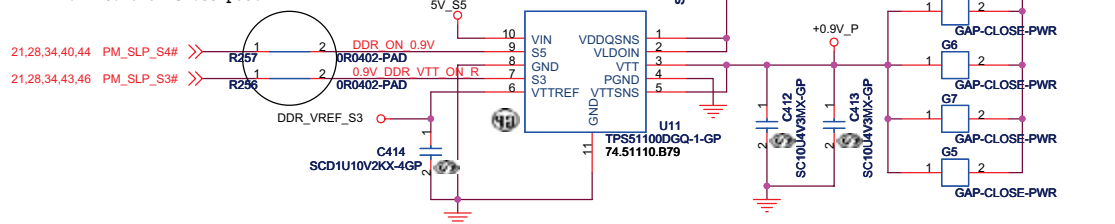
SB:06/17 Change R315 from 0402 0 Ohm to 0402 close pad.

40,41,43,44 CPUCORE\_ON << R315 0R0402-PAD  
21,28,34,43,46 PM\_SLP\_S3# >>  
 $V_o = 0.8 * (1 + (R1/R2))$

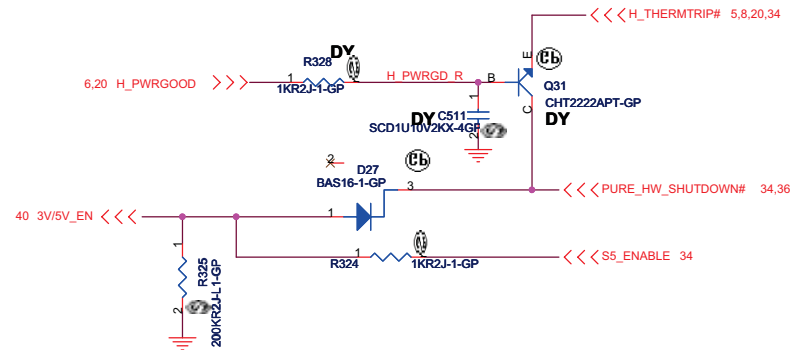


## SSID = PWR.Plane.Regulator\_0.9V

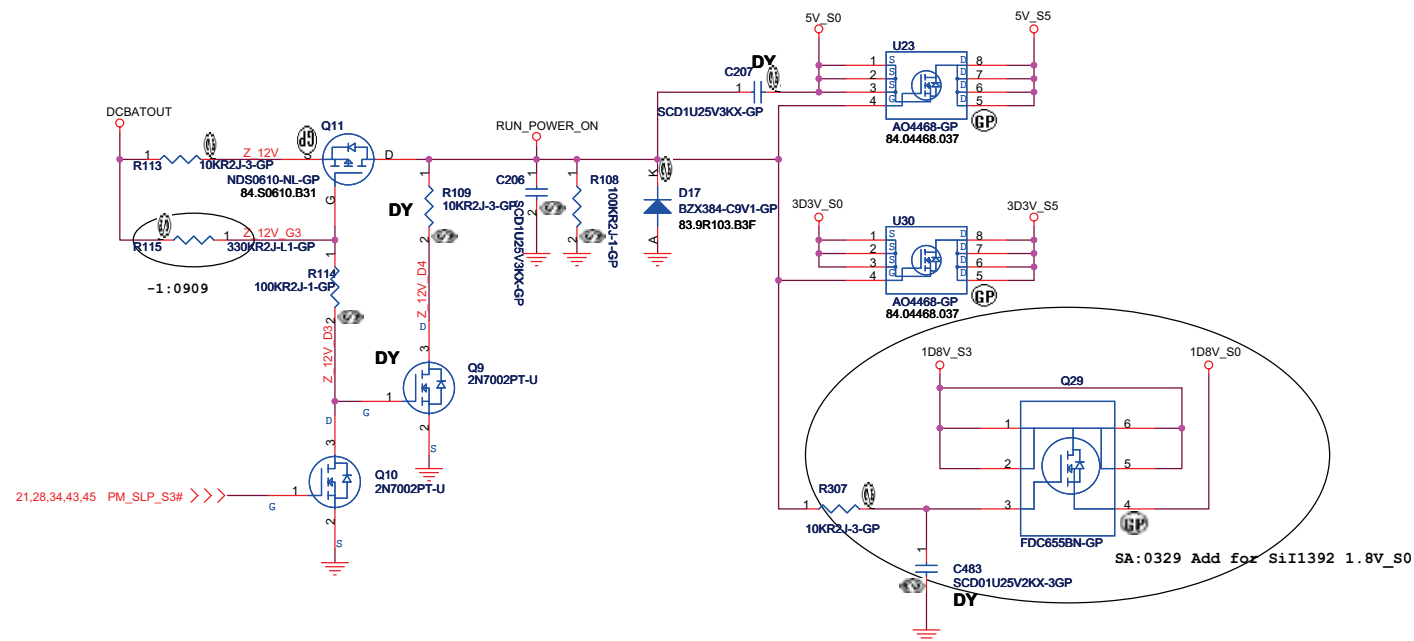
SB:06/17 Change R256, R257 from 0402 0 Ohm to 0402 close pad.



SA:04/23 Change TC24, TC33 P/N for power team request.

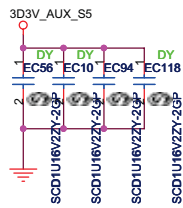


## Run Power

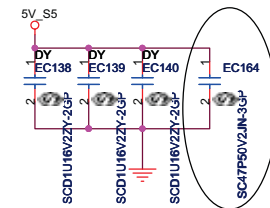
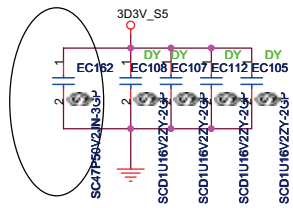


<Core Design>

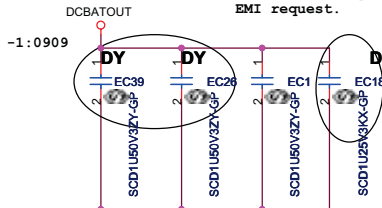
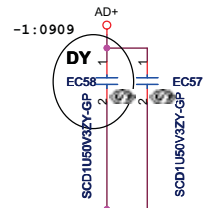
<b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>PWRPLANE&amp;RESETLOGIC</b>			
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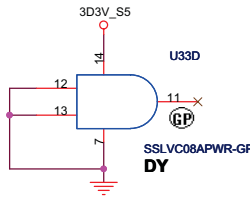
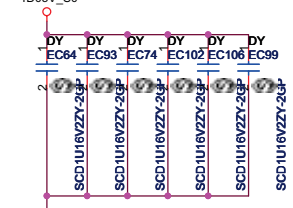
SC:08/11 Add EC162 on 3D3V\_S5 for RF team Request.



SC:08/11 Add EC164 on 5V\_S5 for RF team Request.

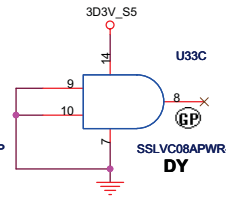


-1:0904 Add EC187(78.10422.2BL) for DCBATOUT decoupling , this is for EMI request.



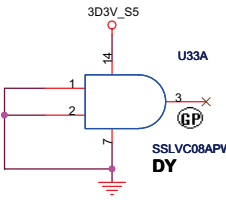
SSLVC08APWR-GP

DY



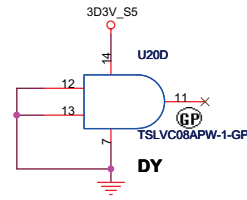
SSLVC08APWR-GP

DY



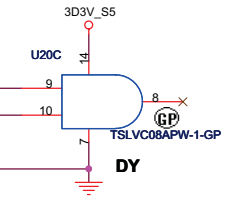
SSLVC08APWR-GP

DY



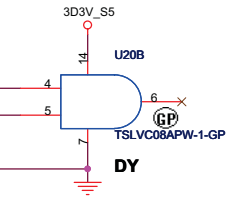
TSLVC08APW-1-GP

DY



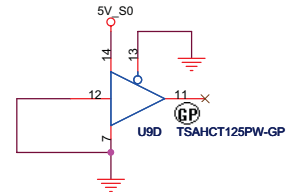
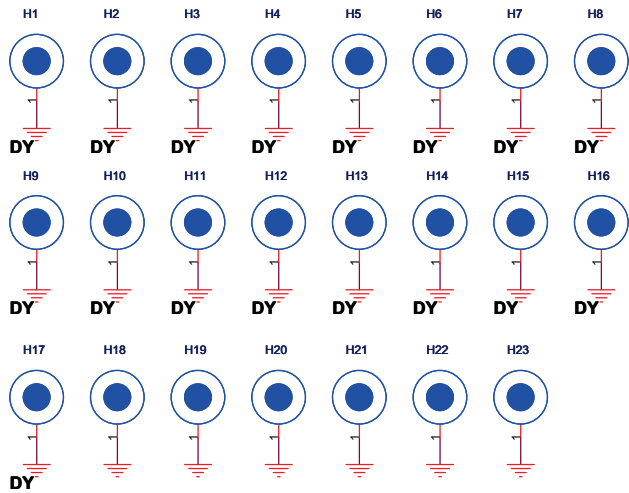
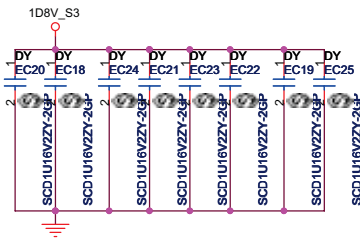
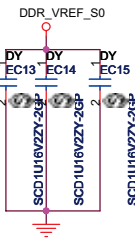
TSLVC08APW-1-GP

DY



TSLVC08APW-1-GP

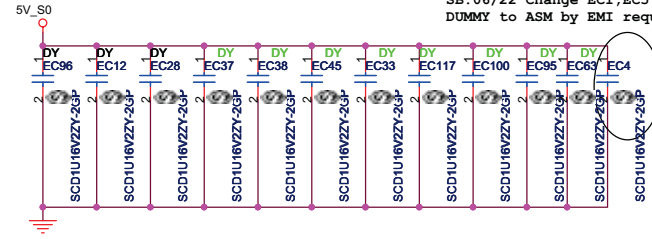
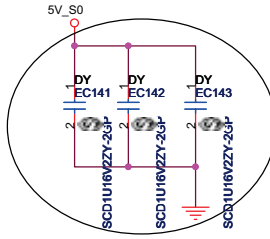
DY



U9D

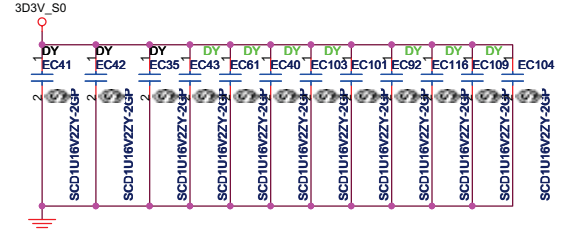
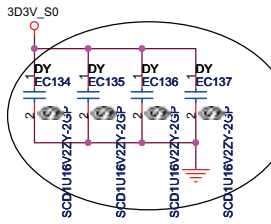
TSAHCT125PW-GP

SB:06/29 Add EC141, EC142, EC143 (78.10491.4FL) for EMI request



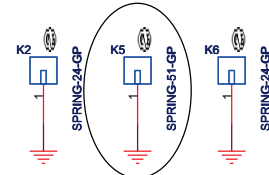
SB:06/22 Change EC1, EC5 from DUMMY to ASM by EMI request.

SB:06/29 Add EC134, EC135, EC136, EC137 (78.10491.4FL) for EMI request

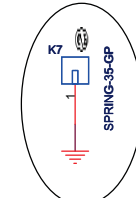


SC:08/15 Add EC177 (78.10491.4FL) on 3D3V\_S0 ,this is for EMI request. Default is DY

SC:08/09 Change K5 spring from 34.45T31.001to 34.4B312.002 for ME request



Place this spring near U40 (bottom side)



SC:08/11 Change K7 from 34.39S07.001 to 34.41P18.001.This change is for EMI request

