

# Compal Confidential

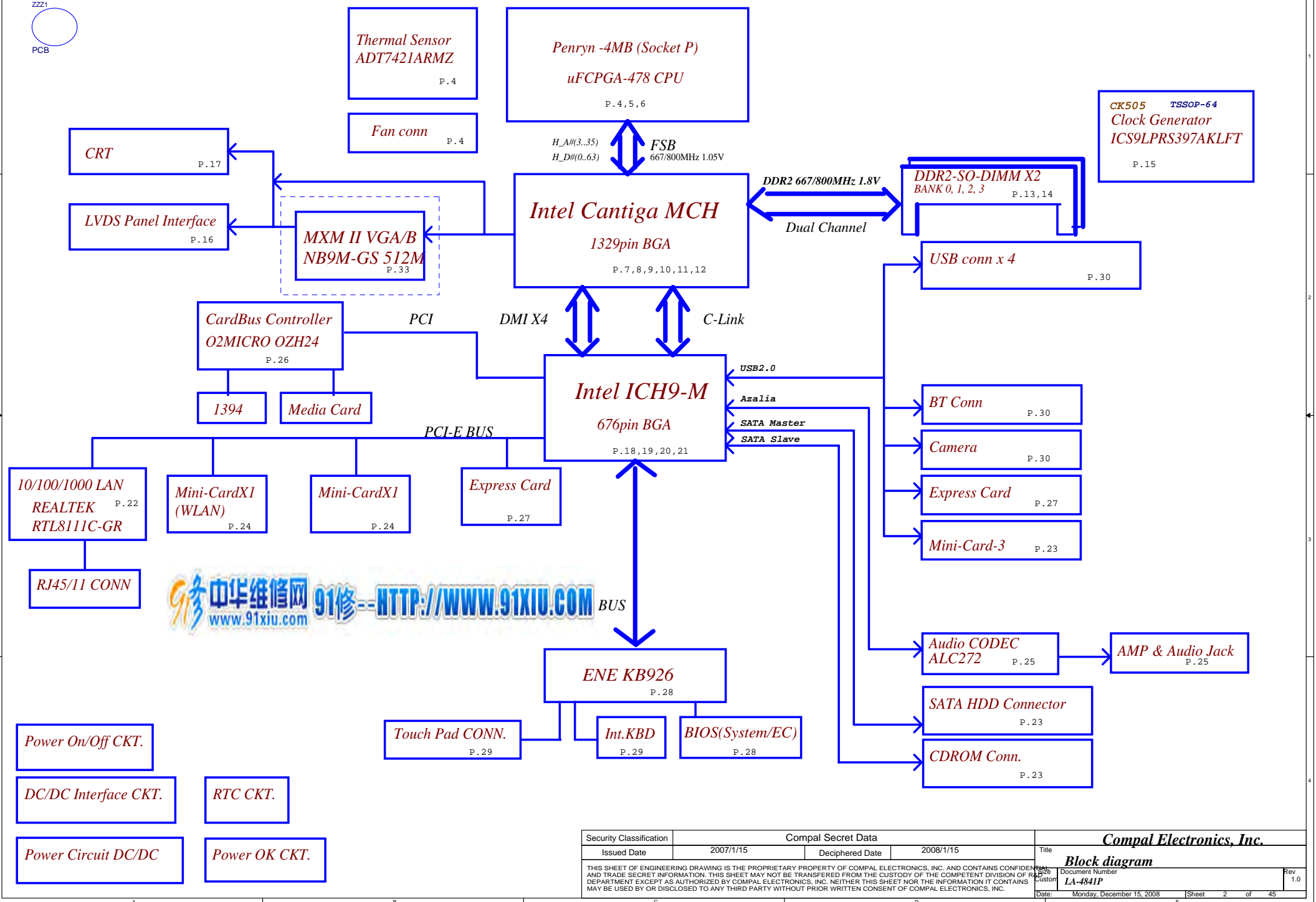
## Schematic Document

### Cantiga + ICH9

2008 / 12 / 10 Rev:1.0


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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	Cover Sheet
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## MLK 14



State \ power plane	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE  +VGA_CORE +2.5VS +1.8VS +1.2VS +0.9VGA
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build  
DEBUG@ : means just reserve for debug.

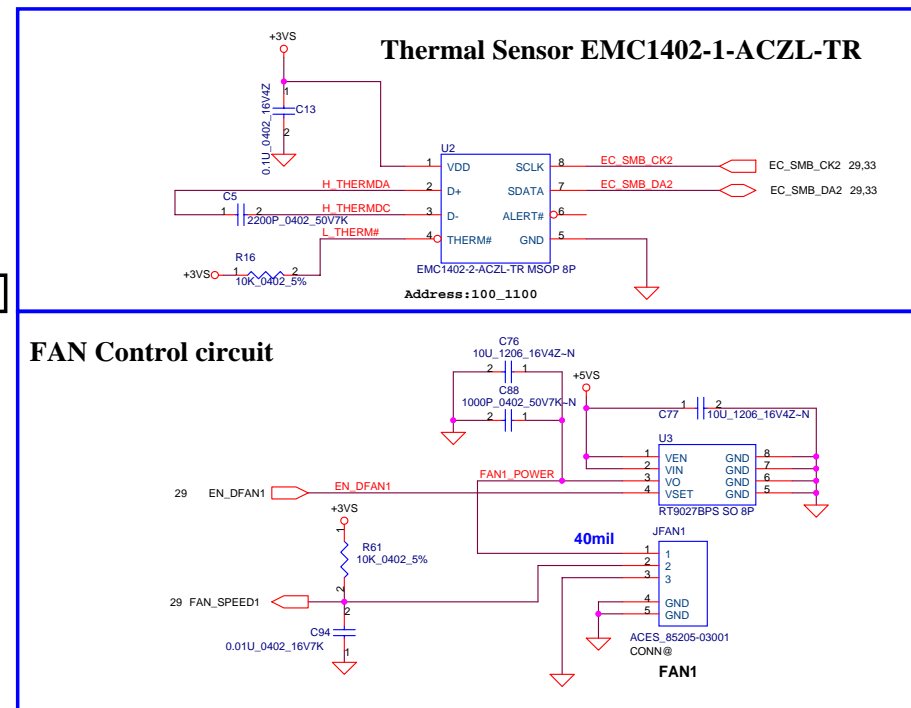
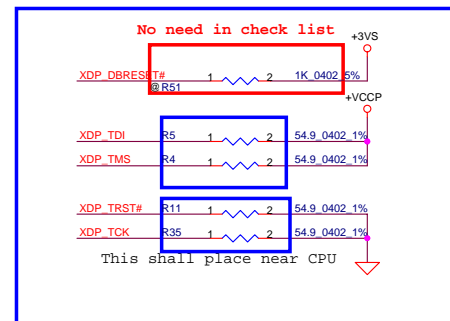
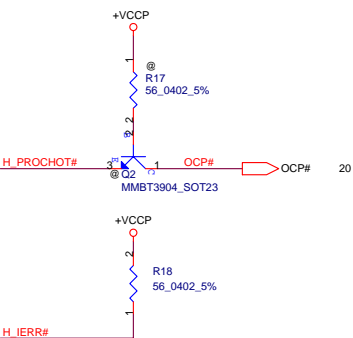
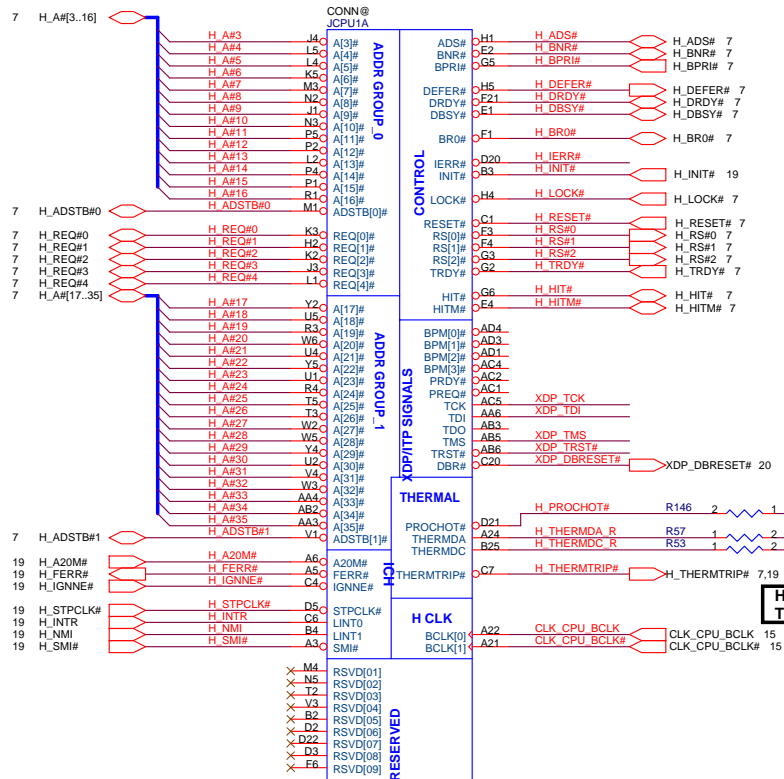
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

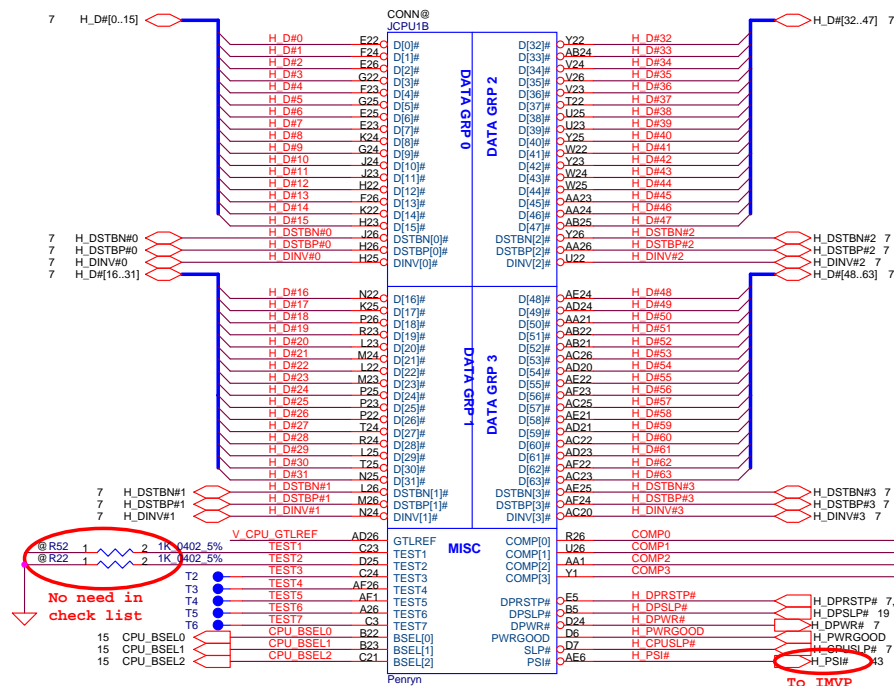
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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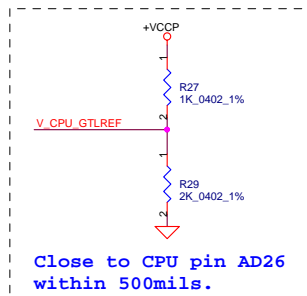


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layout note: Rout H\_DPRSTP# from ICH9 to IMVP6 then to GMCH & CPU  
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

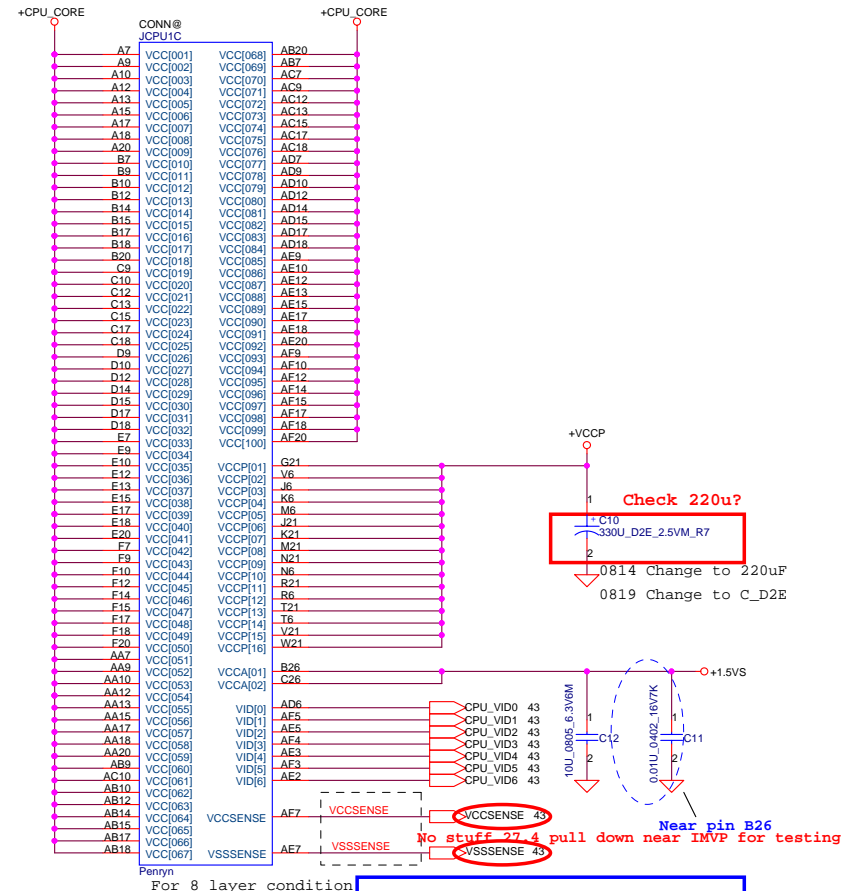
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



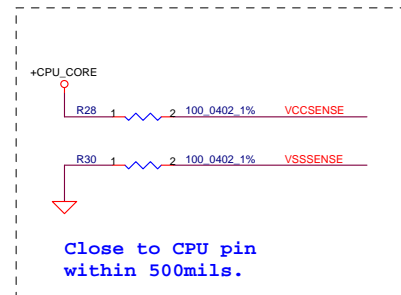
Close to CPU pin AD26 within 500mils.

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4

For 6 layer  
Z=27.4 ohm  
VCCSENSE, VSSSENSE/ 14mils (MS),  
16mils (SL) width, 7mils space, 25mils  
space to other signals Mismatch =25mils.



Length match within 25 mils.  
The trace width/space/other is 20/7/25.

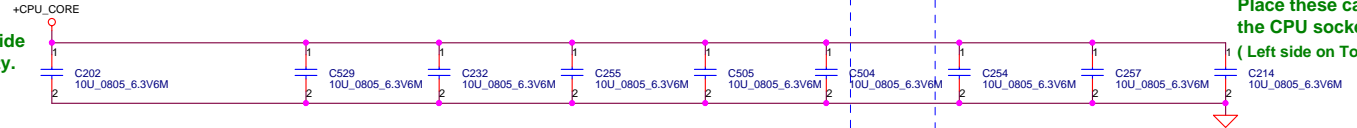


Close to CPU pin within 500mils.

High frequency decoupling  
10uF 0805 X5R -> 85 degree.

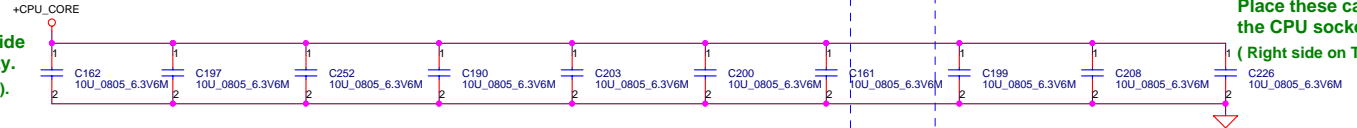
CONN@			
JCPU1D			
A4	VSS[001]	VSS[023]	P6
A8	VSS[002]	VSS[033]	P21
A11	VSS[003]	VSS[044]	P24
A14	VSS[004]	VSS[055]	R2
A16	VSS[005]	VSS[066]	R5
A19	VSS[006]	VSS[077]	R22
A23	VSS[007]	VSS[088]	R25
AE2	VSS[008]	VSS[099]	T4
B6	VSS[009]	VSS[100]	T23
B8	VSS[010]	VSS[011]	T26
B11	VSS[012]	VSS[022]	U3
B13	VSS[013]	VSS[033]	U6
B16	VSS[014]	VSS[044]	U21
B19	VSS[015]	VSS[055]	U24
B21	VSS[016]	VSS[066]	V2
B24	VSS[017]	VSS[077]	V5
C5	VSS[018]	VSS[088]	V22
C8	VSS[019]	VSS[099]	V25
C11	VSS[020]	VSS[101]	W1
C14	VSS[021]	VSS[102]	W23
C16	VSS[022]	VSS[103]	W26
C19	VSS[023]	VSS[104]	Y3
C22	VSS[024]	VSS[105]	Y6
C25	VSS[025]	VSS[106]	Y21
D1	VSS[026]	VSS[107]	Y24
D4	VSS[027]	VSS[108]	AA2
D8	VSS[028]	VSS[109]	AA5
D11	VSS[029]	VSS[110]	AA8
D13	VSS[030]	VSS[111]	AA11
D16	VSS[031]	VSS[112]	AA14
D19	VSS[032]	VSS[113]	AA16
D23	VSS[033]	VSS[114]	AA19
D26	VSS[034]	VSS[115]	AA22
E3	VSS[035]	VSS[116]	AA25
E6	VSS[036]	VSS[117]	AB1
E8	VSS[037]	VSS[118]	AB4
F11	VSS[038]	VSS[119]	AB8
F14	VSS[039]	VSS[120]	AB11
F16	VSS[040]	VSS[121]	AB13
F19	VSS[041]	VSS[122]	AB16
E21	VSS[042]	VSS[123]	AB19
E24	VSS[043]	VSS[124]	AB23
F5	VSS[044]	VSS[125]	AB26
F8	VSS[045]	VSS[126]	AC3
F11	VSS[046]	VSS[127]	AC6
F13	VSS[047]	VSS[128]	AC8
F16	VSS[048]	VSS[129]	AC11
F19	VSS[049]	VSS[130]	AC14
F22	VSS[050]	VSS[131]	AC16
F25	VSS[051]	VSS[132]	AC19
F28	VSS[052]	VSS[133]	AC21
G4	VSS[053]	VSS[134]	AC24
G1	VSS[054]	VSS[135]	AD2
G23	VSS[055]	VSS[136]	AD5
G26	VSS[056]	VSS[137]	AD8
H3	VSS[057]	VSS[138]	AD11
H6	VSS[058]	VSS[139]	AD13
H21	VSS[059]	VSS[140]	AD16
H24	VSS[060]	VSS[141]	AD19
J2	VSS[061]	VSS[142]	AD22
J5	VSS[062]	VSS[143]	AD25
J22	VSS[063]	VSS[144]	AE1
J25	VSS[064]	VSS[145]	AE4
K1	VSS[065]	VSS[146]	AE8
K4	VSS[066]	VSS[147]	AE11
K23	VSS[067]	VSS[148]	AE14
K26	VSS[068]	VSS[149]	AE16
L3	VSS[069]	VSS[150]	AE19
L6	VSS[070]	VSS[151]	AE23
L21	VSS[071]	VSS[152]	AE26
L24	VSS[072]	VSS[153]	A2
M2	VSS[073]	VSS[154]	AF6
M5	VSS[074]	VSS[155]	AF8
M22	VSS[075]	VSS[156]	AF11
M25	VSS[076]	VSS[157]	AF13
N1	VSS[077]	VSS[158]	AF16
N4	VSS[078]	VSS[159]	AF19
N23	VSS[079]	VSS[160]	AF21
N26	VSS[080]	VSS[161]	A25
N3	VSS[081]	VSS[162]	AF25
	VSS[163]		

Place these caps inside  
the CPU socket cavity.  
( Left side on Top ).



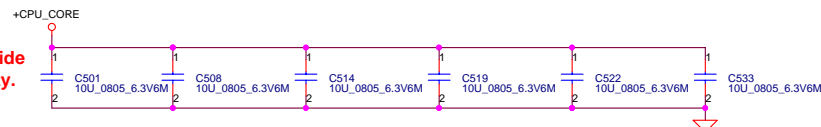
Place these caps inside  
the CPU socket.  
( Left side on Top ).

Place these caps inside  
the CPU socket cavity.  
( Right side on Top side ).

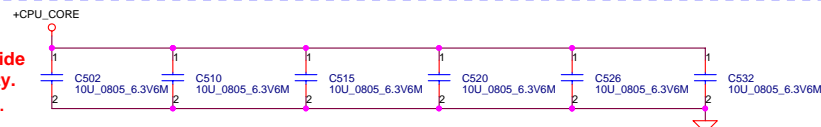


Place these caps inside  
the CPU socket.  
( Right side on Top ).

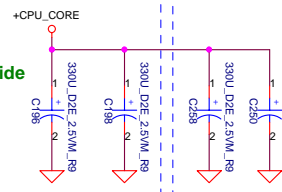
Place these caps inside  
the CPU socket cavity.  
( Left side on Bottom ).



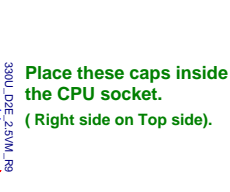
Place these caps inside  
the CPU socket cavity.  
( Right side on Bottom ).



Place these caps inside  
the CPU socket.  
( Left side on Top ).

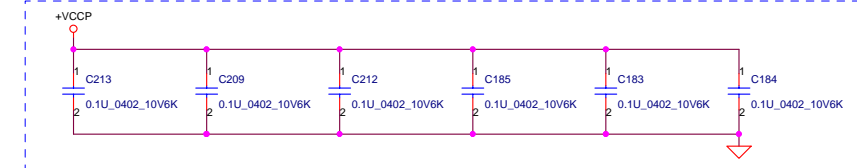


Place these caps inside  
the CPU socket.  
( Right side on Top side ).



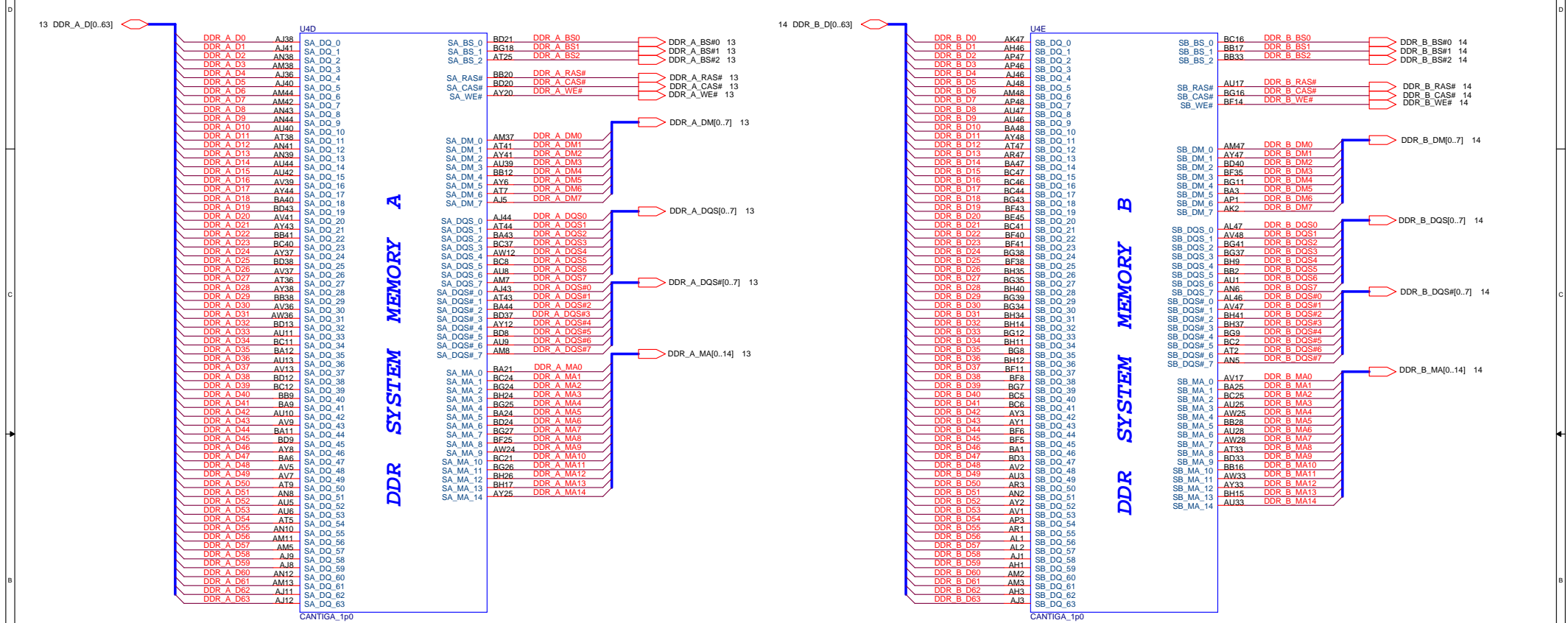
ESR <= 1.5m ohm  
Capacitor > 880 uF

Place these inside  
socket cavity on L8  
(North side  
Secondary)



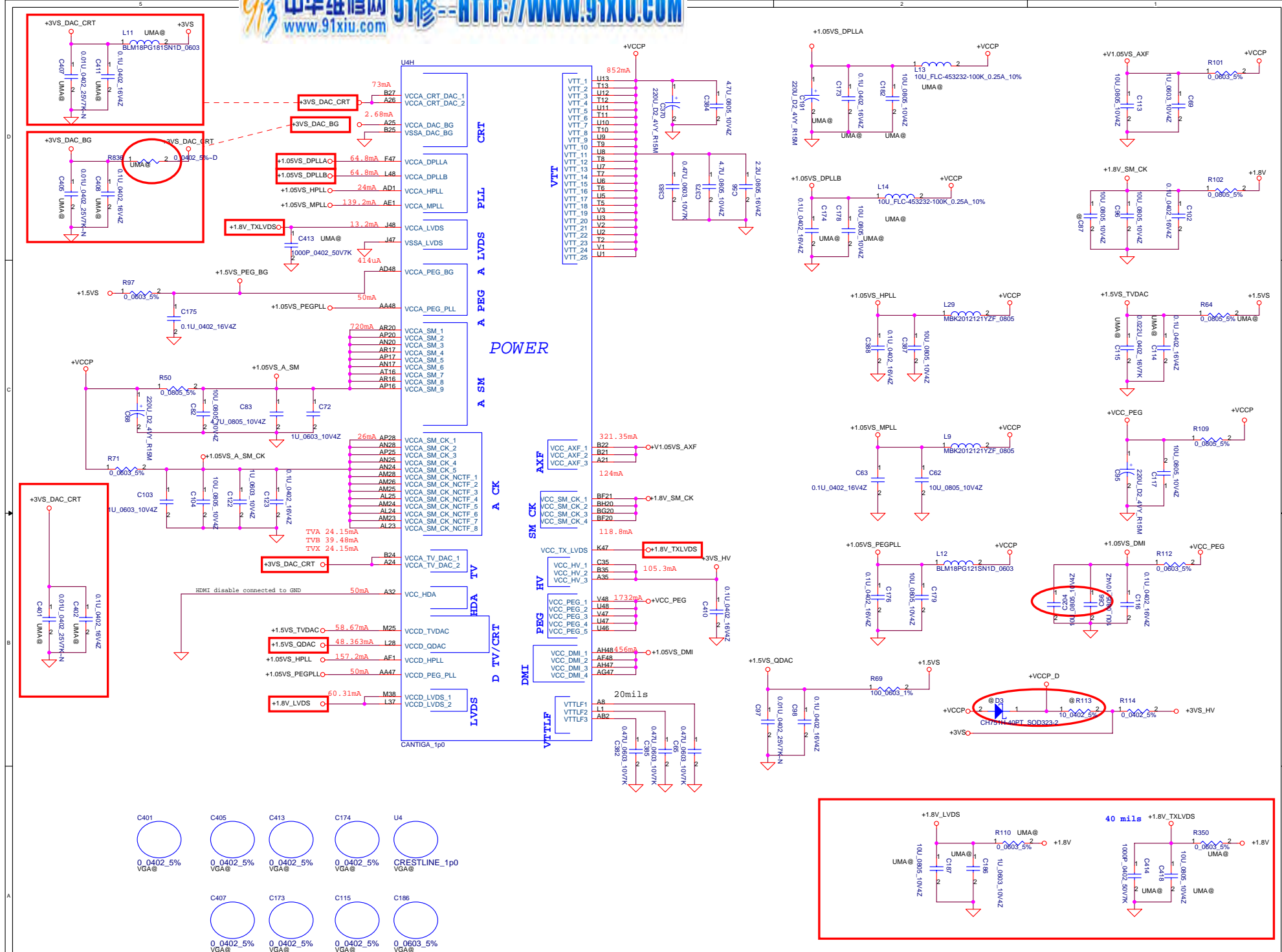






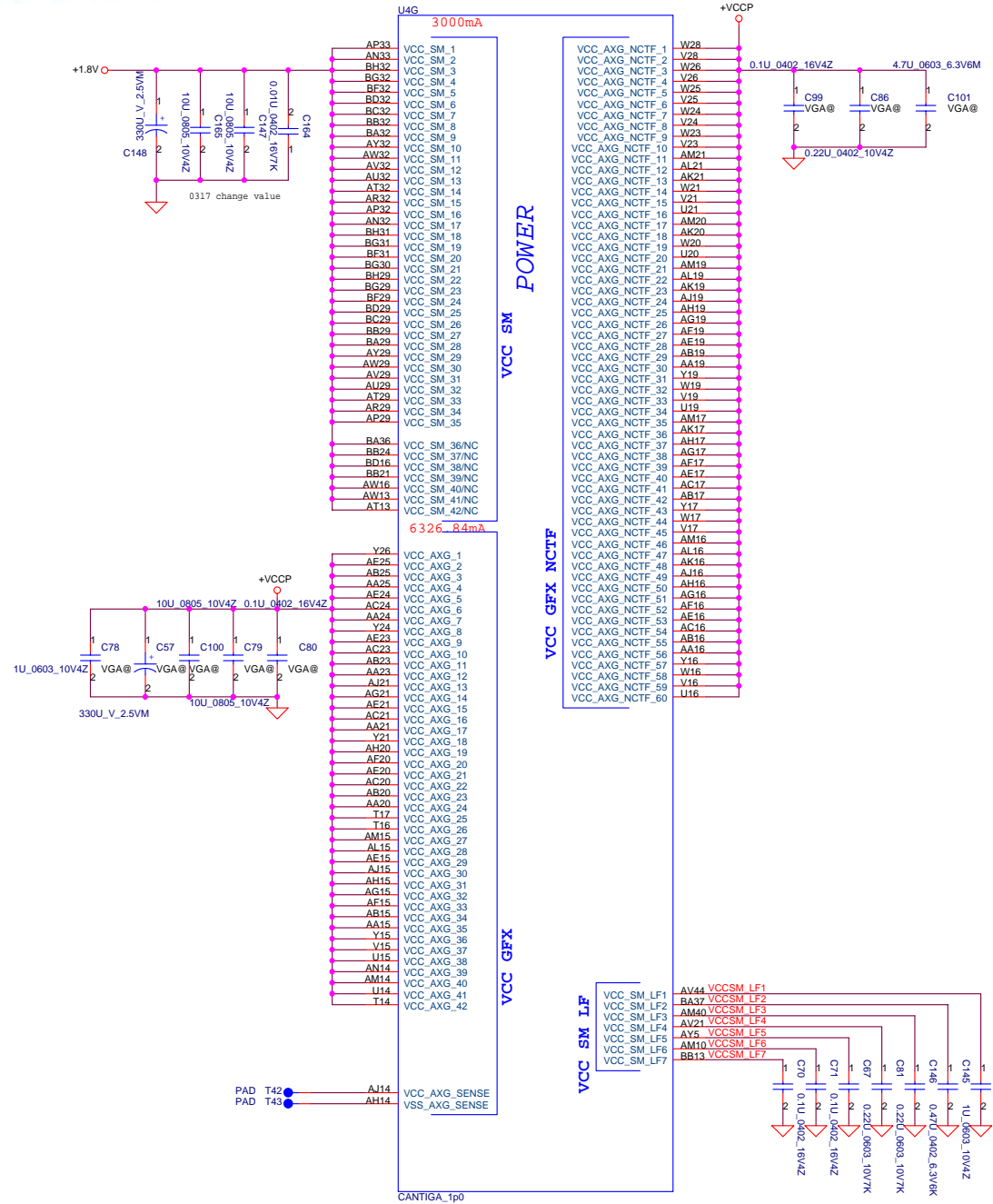
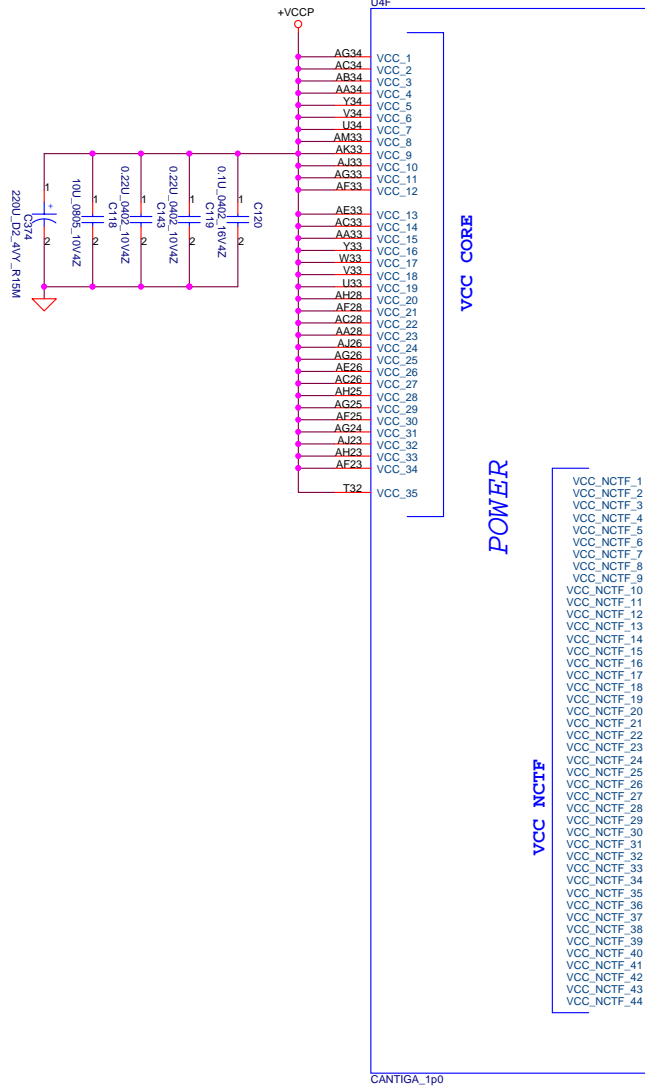


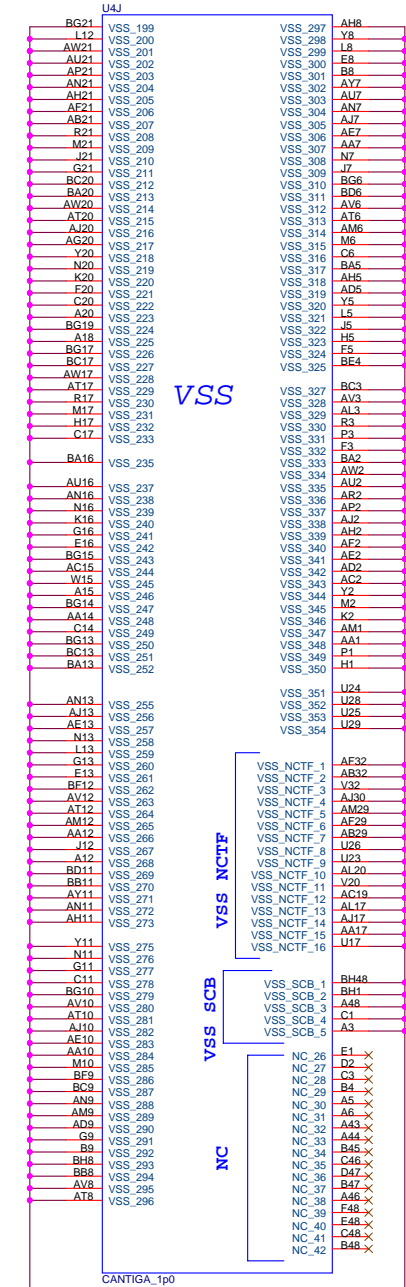
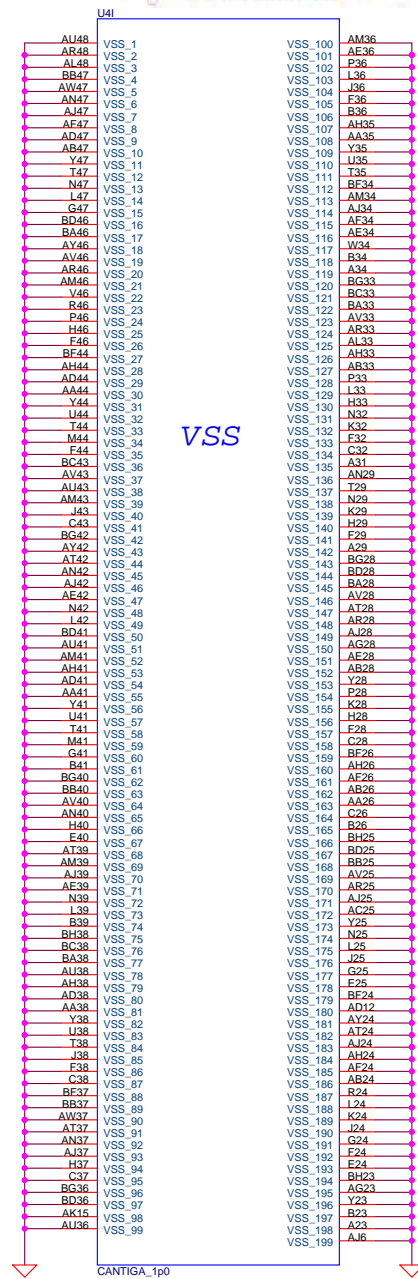


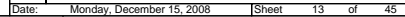


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Extenal Graphic: 1210.34mA  
integrated Graphic: 1930.4mA







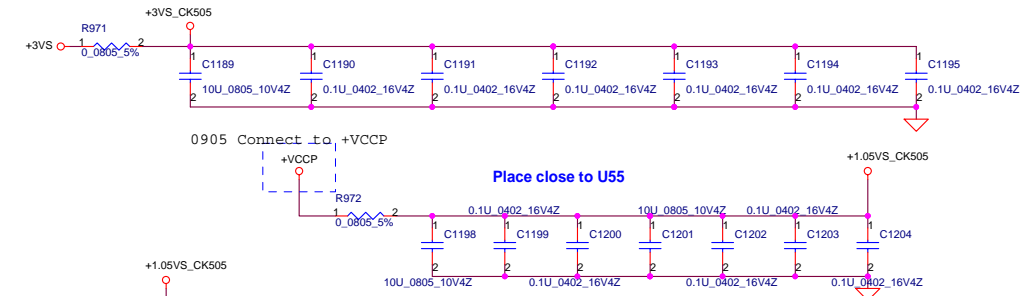
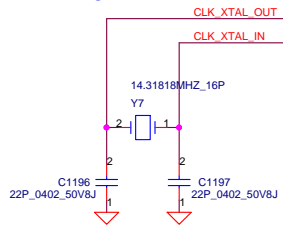




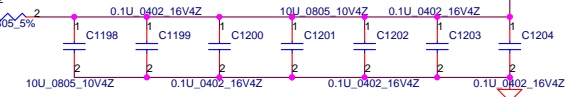


FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								

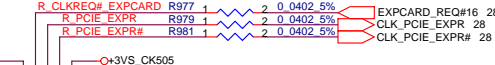
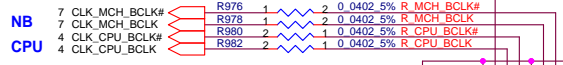
### Routing the trace at least 10mil



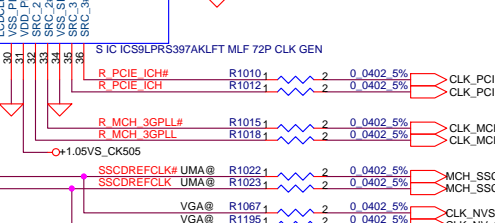
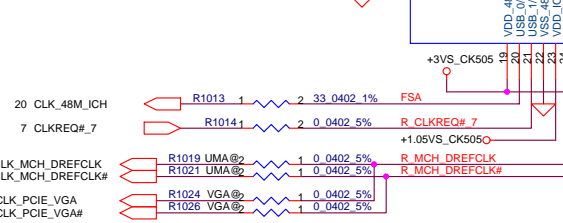
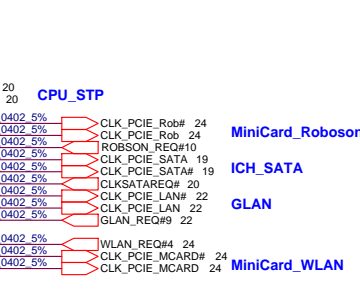
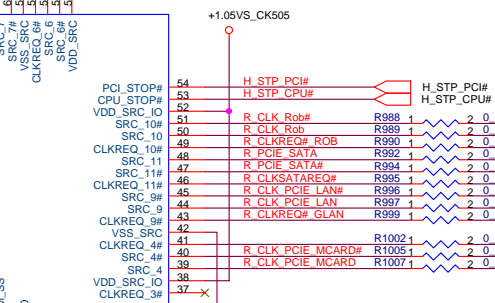
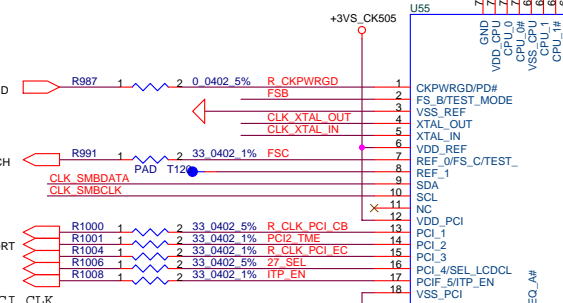
### Place close to U55



### NB CPU



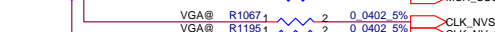
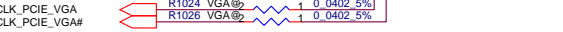
### Express Card



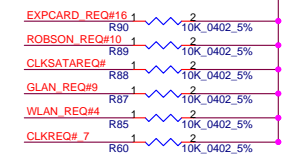
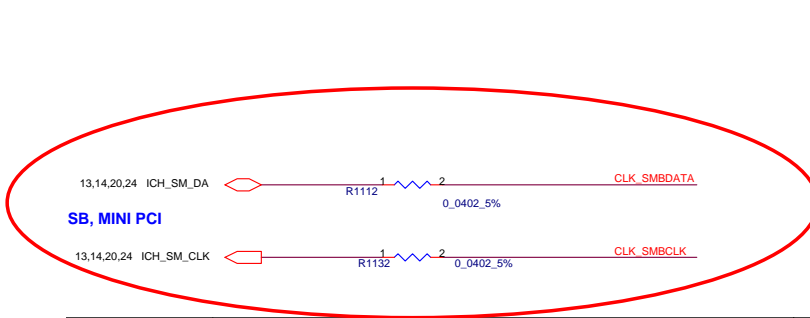
### NB (UMA)



### VGA (Discrete)



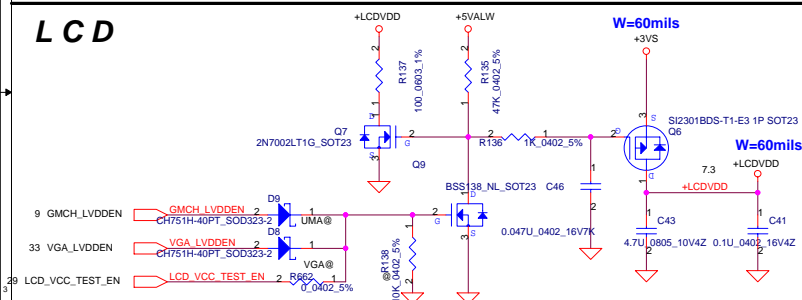
ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
27_SEL	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)
PCI2_TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
<div> <div> +3VS_CK505 R1029 10K_0402_5% ITP_EN R1032 10K_0402_5% </div> <div> +3VS_CK505 VGA@ R1030 10K_0402_5% 27_SEL UMA@ R1033 10K_0402_5% </div> <div> +3VS_CK505 R1031 10K_0402_5% PCI2_TME R1034 10K_0402_5% </div> </div>	



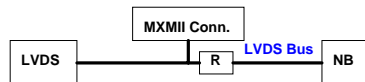
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JEPICO Conn.

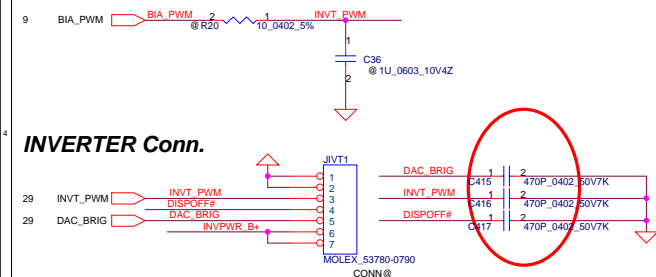
LCD



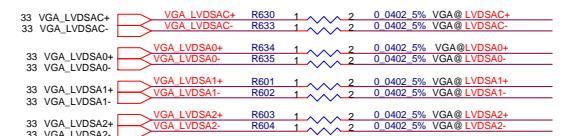
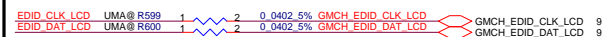
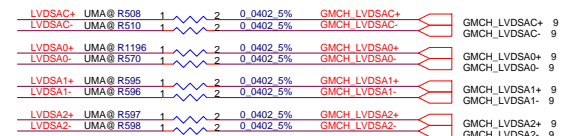
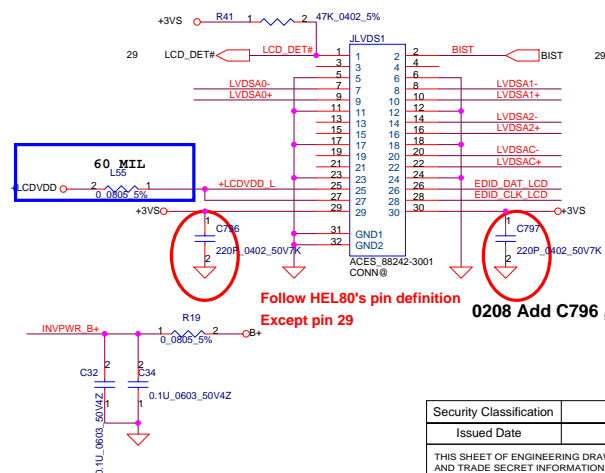
Routing Diagram



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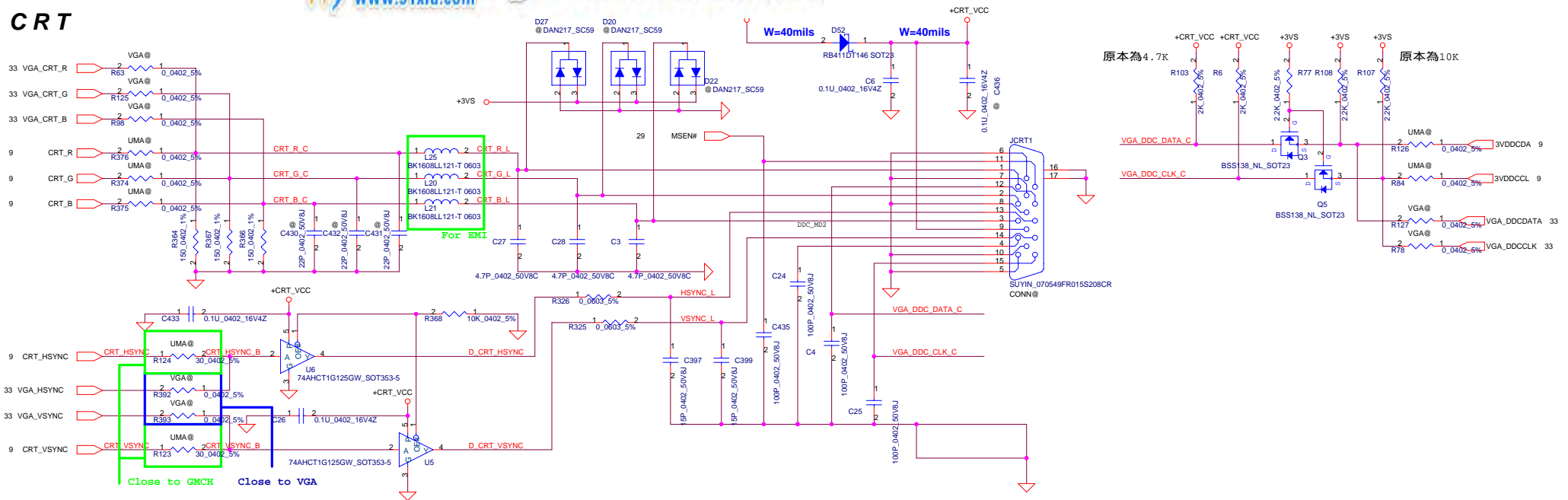


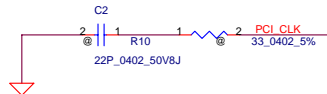
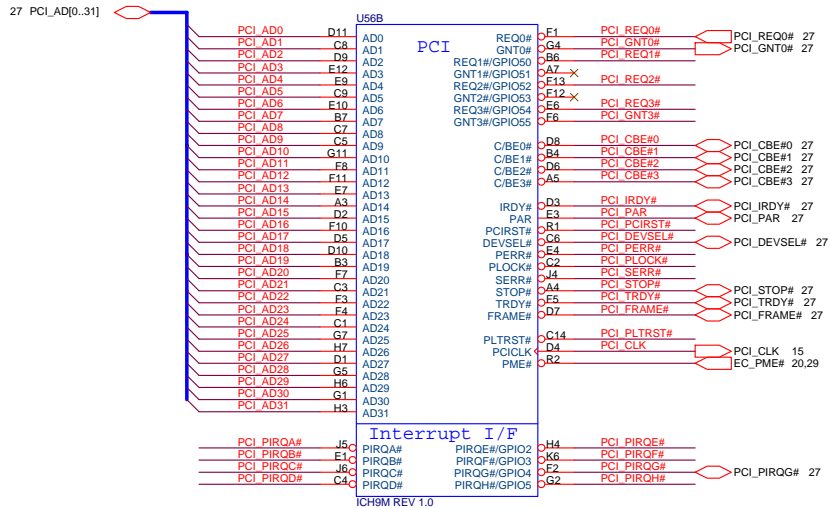
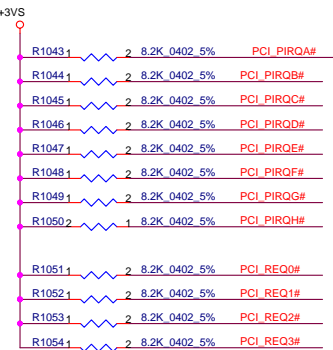
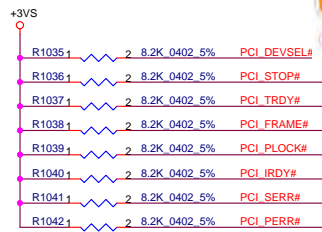
LCD/PANEL BD. Conn.



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						Custom	LA-4841P	1.0
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# CRT





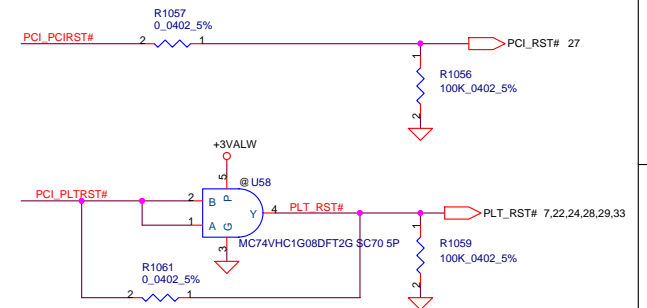
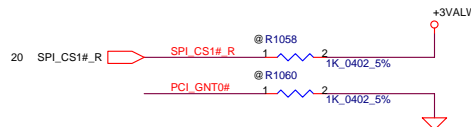
### A16 swap override Strap

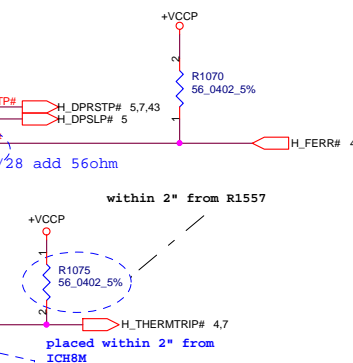
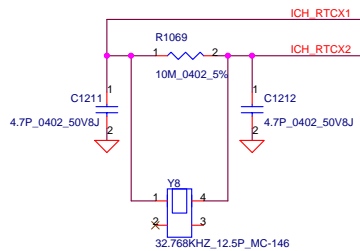
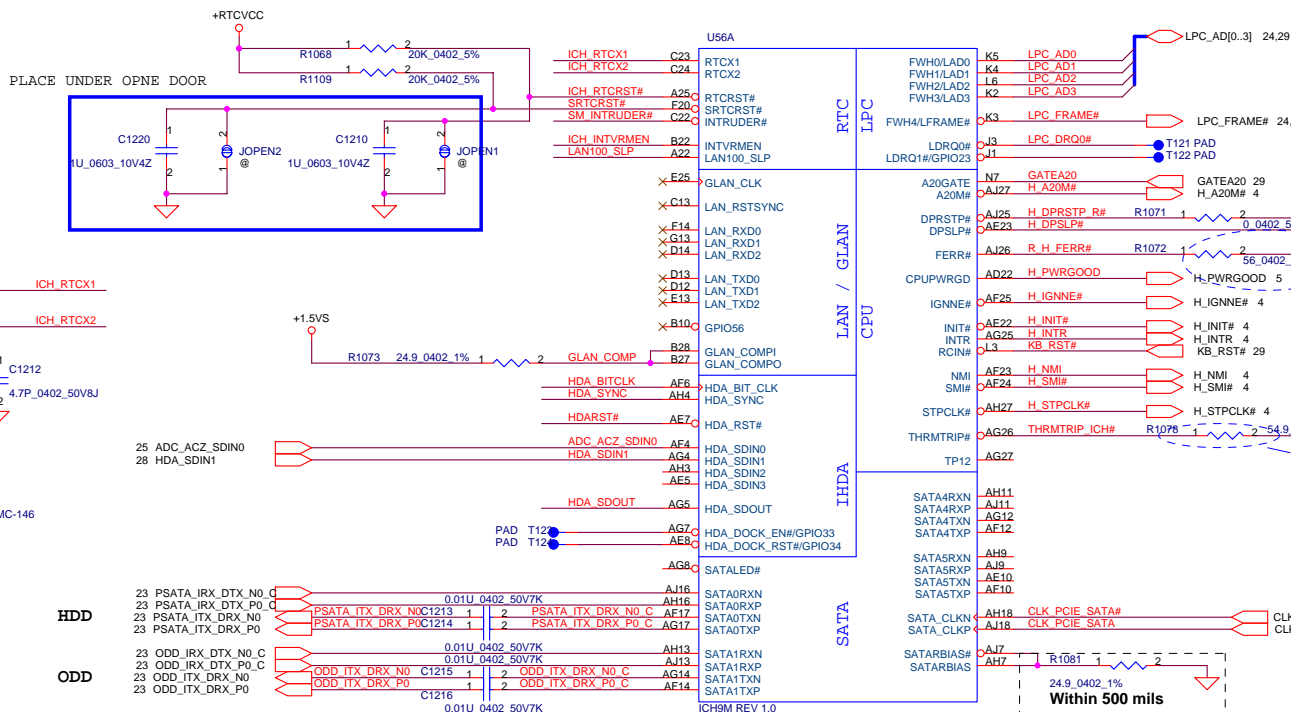
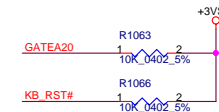
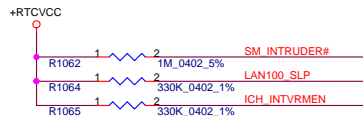
Low= A16 swap override Enble  
High= Default \*



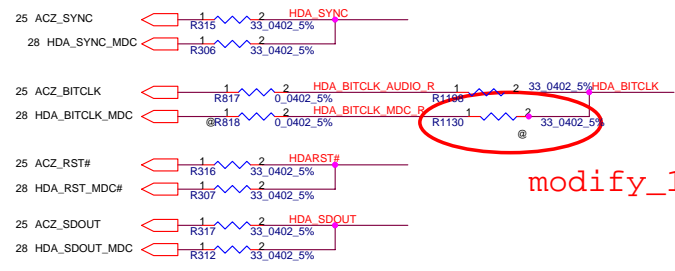
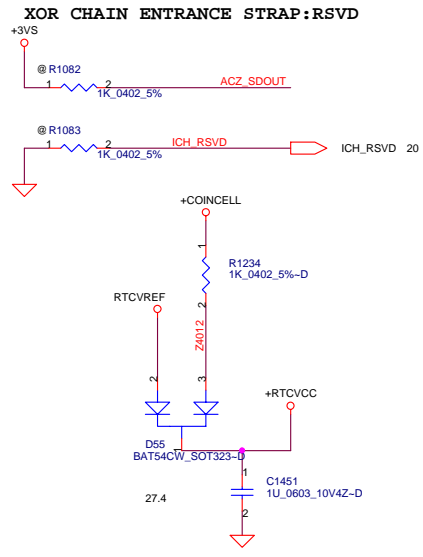
### Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



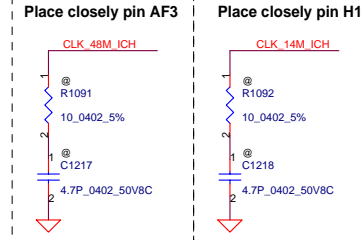


HDD  
23 PSATA\_IRX\_DTX\_NO\_C  
23 PSATA\_IRX\_DTX\_P0\_C  
23 PSATA\_ITX\_DRX\_NO\_C  
23 PSATA\_ITX\_DRX\_P0\_C  
23 ODD\_IRX\_DTX\_NO\_C  
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23 ODD\_ITX\_DRX\_NO\_C  
23 ODD\_ITX\_DRX\_P0\_C



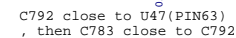
modify\_11/12

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				LA-4841P	1.0
Date: Monday, December 15, 2008				Sheet	19 of 45



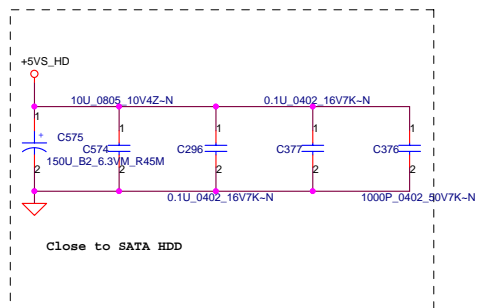
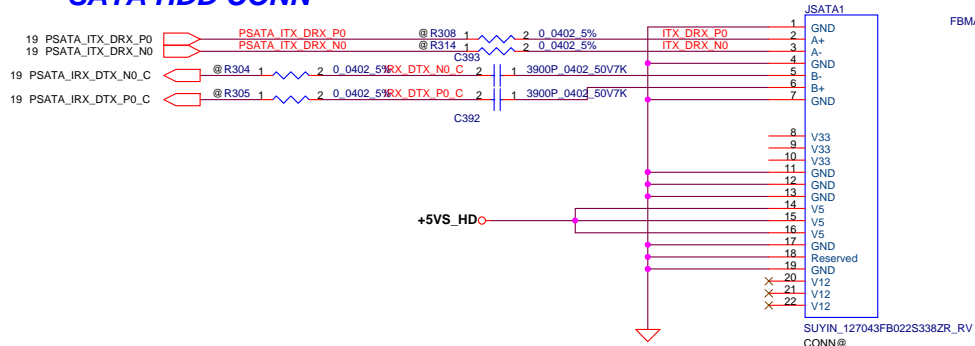






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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	
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				Size	Document Number
				Custom	LA-481P
Date: Monday, December 15, 2008				ISheet	22 of 45

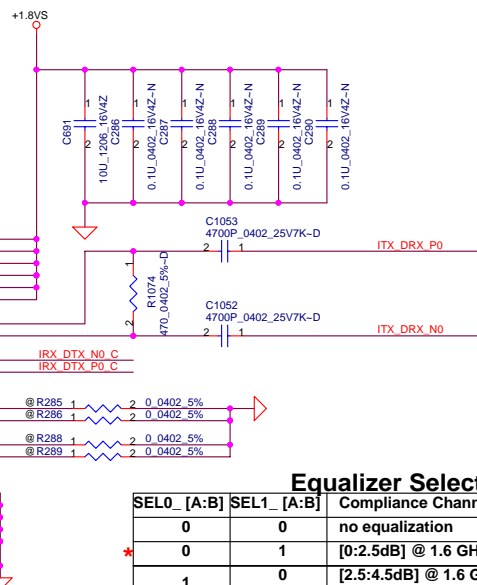
**SATA HDD CONN**



SEL2_ [A:B]	Swing
0	1x
1	1.2x

### Output De-emphasis Adjustment

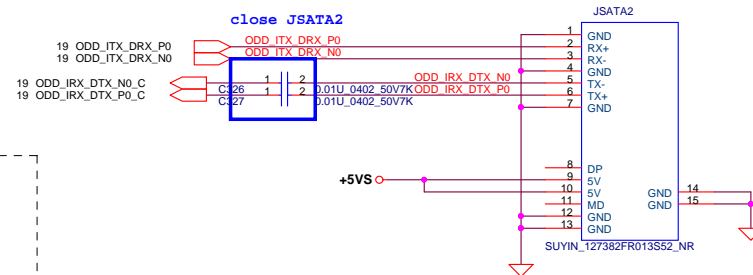
SEL3_ [A:B]	De-emphasis
0	0dB
1	-3.5dB



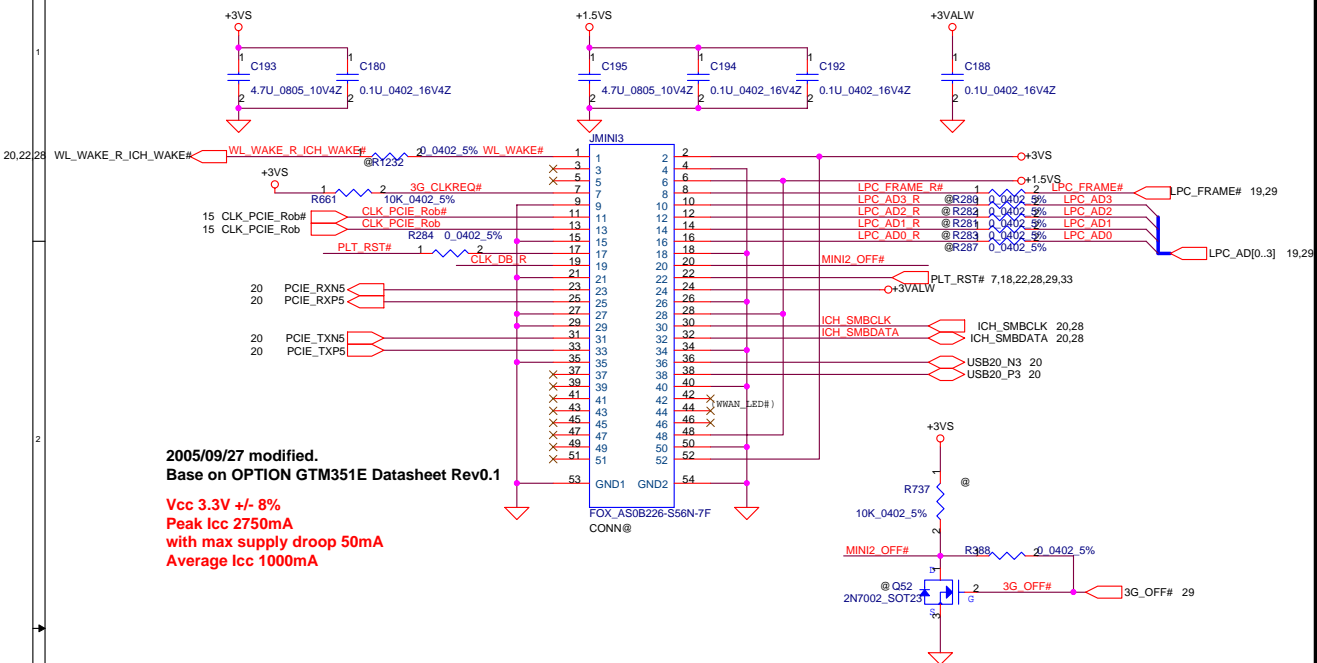
### Equalizer Selection

SEL0_ [A:B]	SEL1_ [A:B]	Compliance Channel
0	0	no equalization
0	1	[0:2.5dB] @ 1.6 GHz
1	0	[2.5:4.5dB] @ 1.6 GHz
1	1	[4.5:6.5dB] @ 1.6 GHz

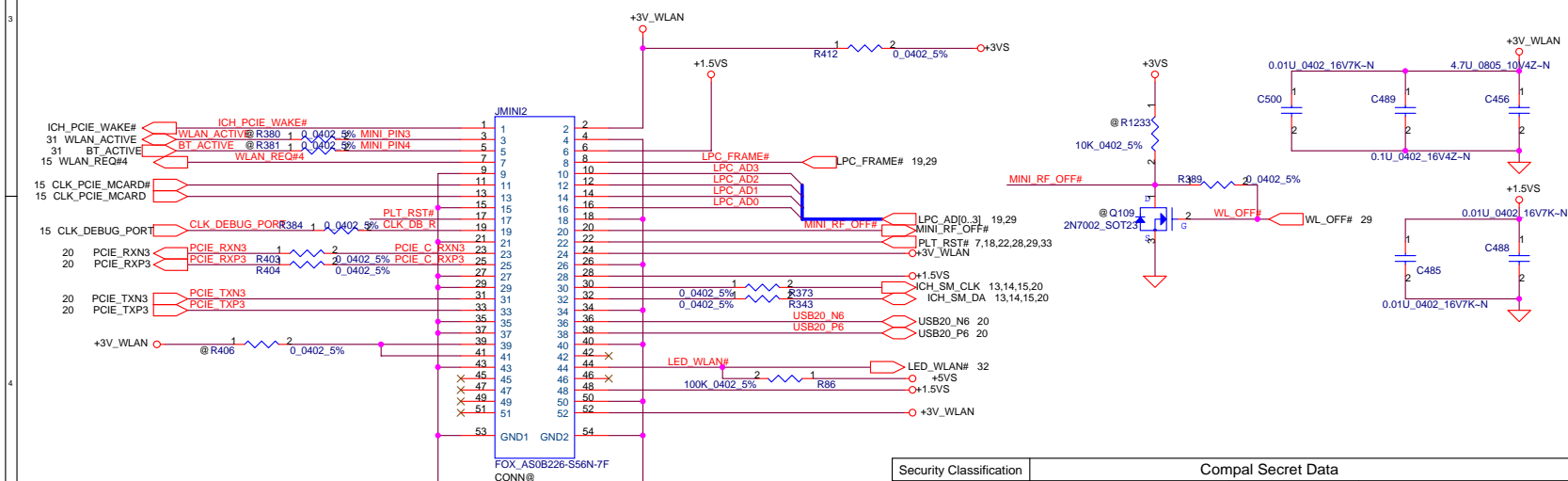
**SATA ODD CONN**



# Mini-Express Card for 3

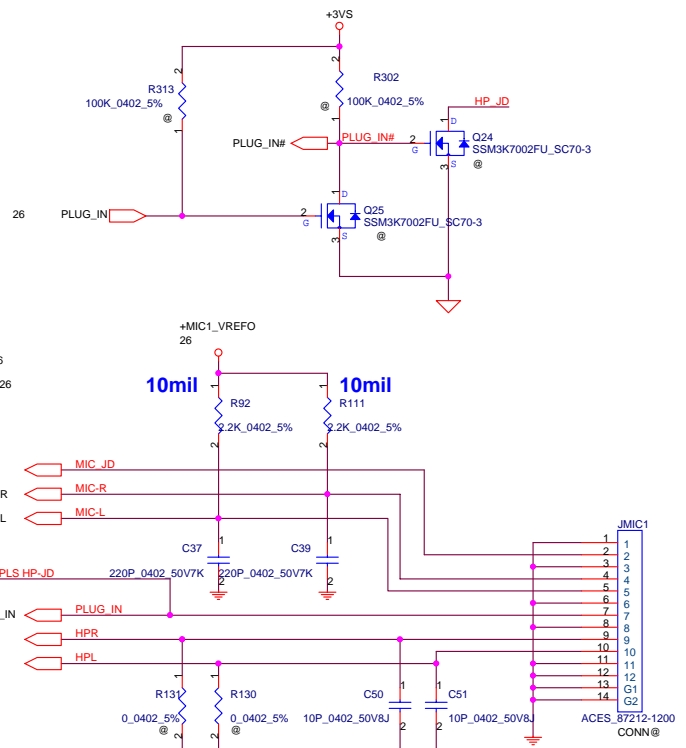
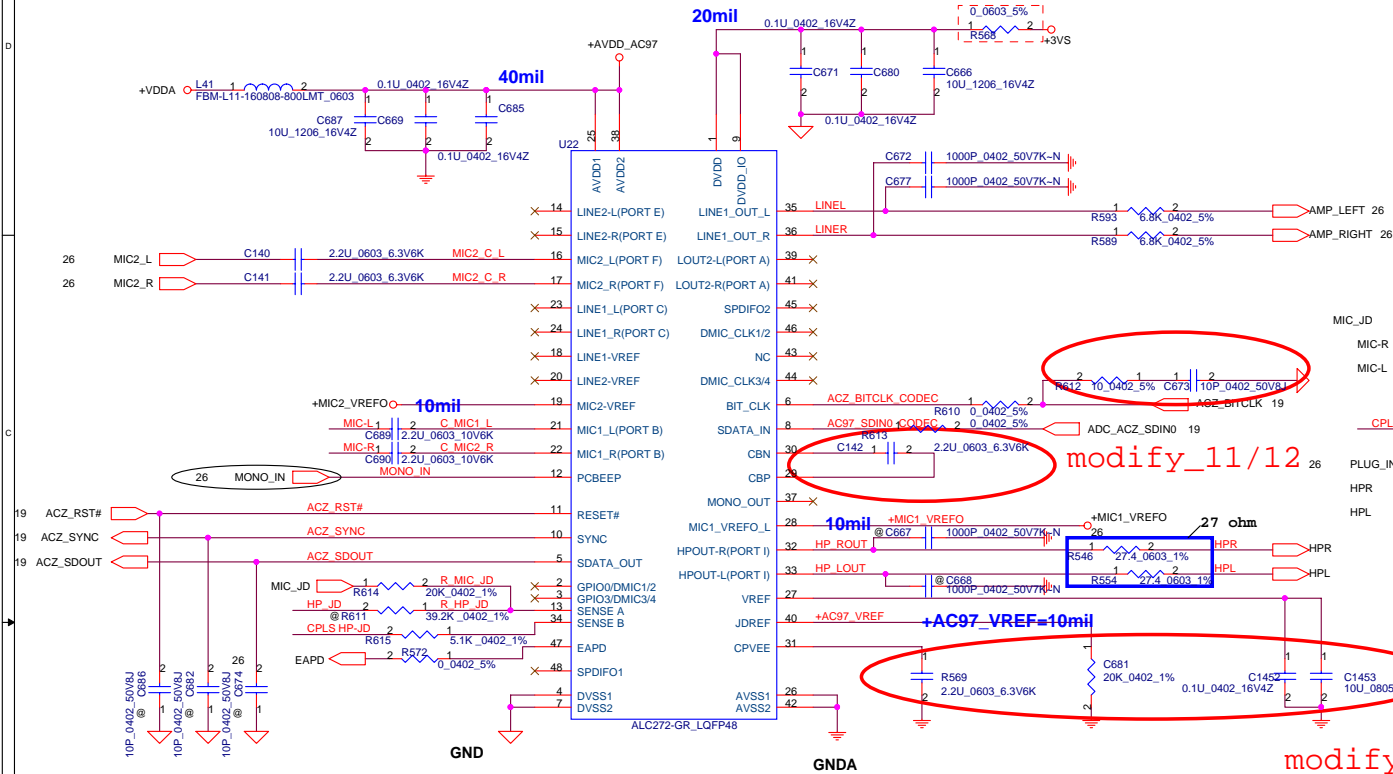


## Mini-Express Card---WLAN

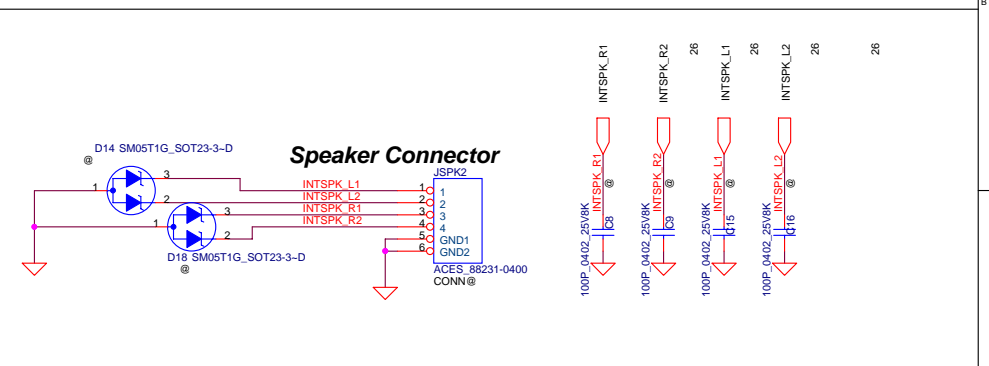
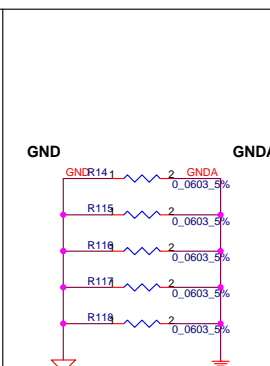
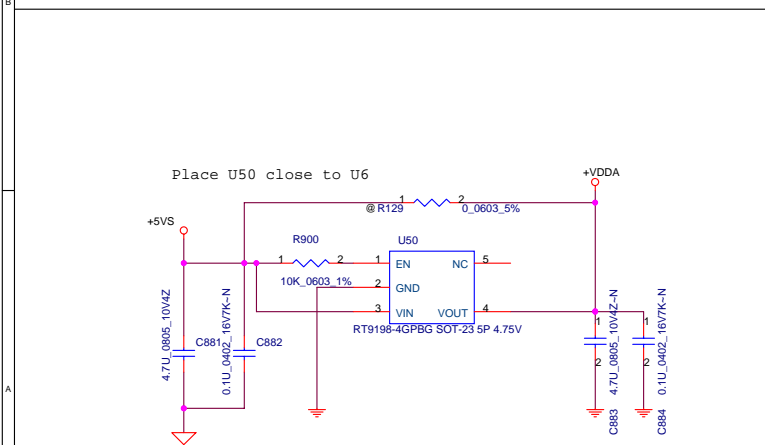


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								Document Number	
								LA-4841P	
Date:				Monday, December 15, 2008		Sheet 24 of 45			

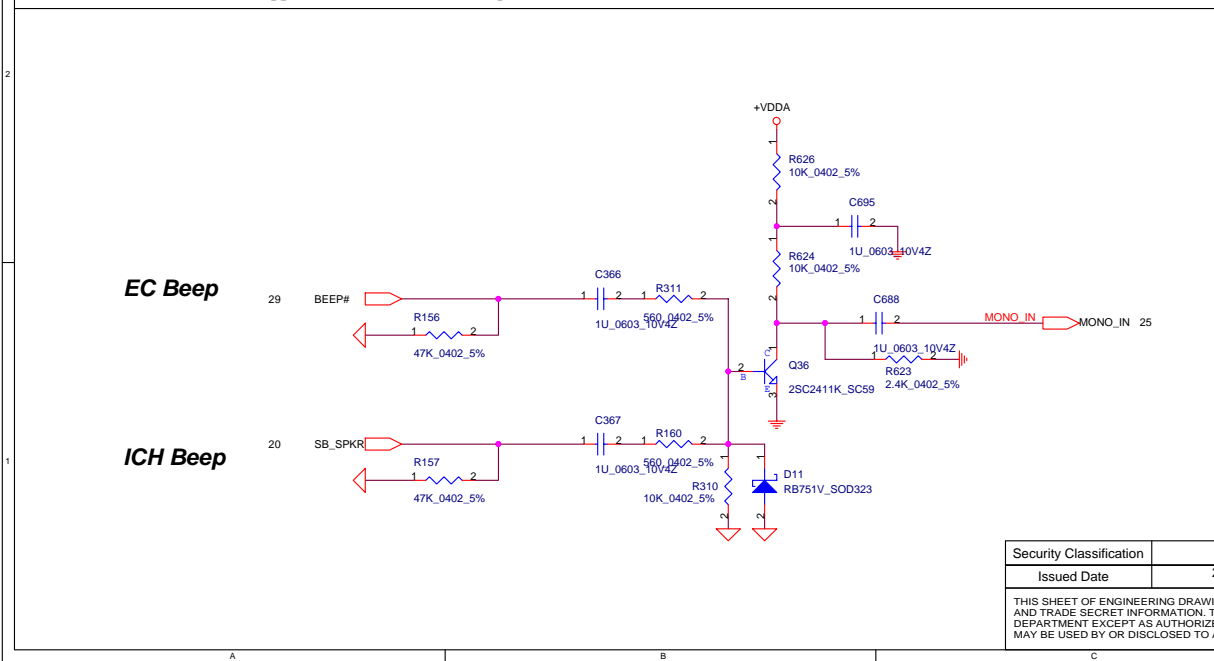
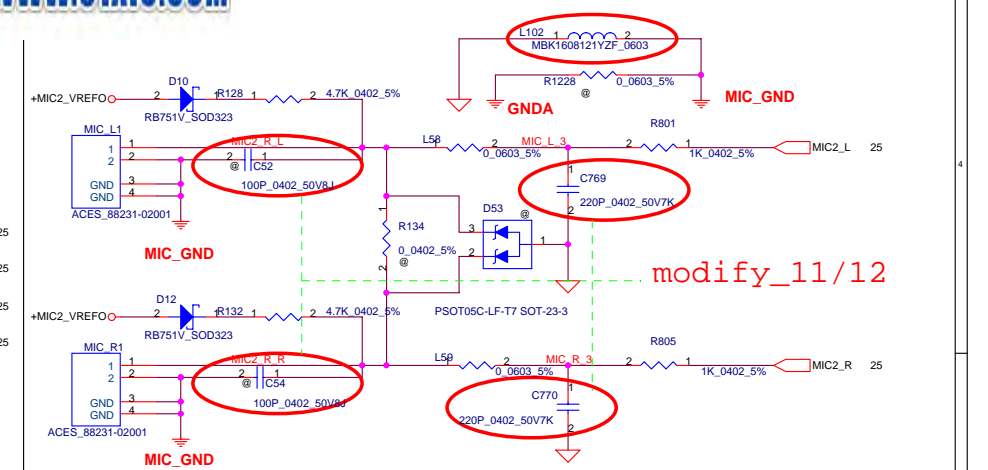
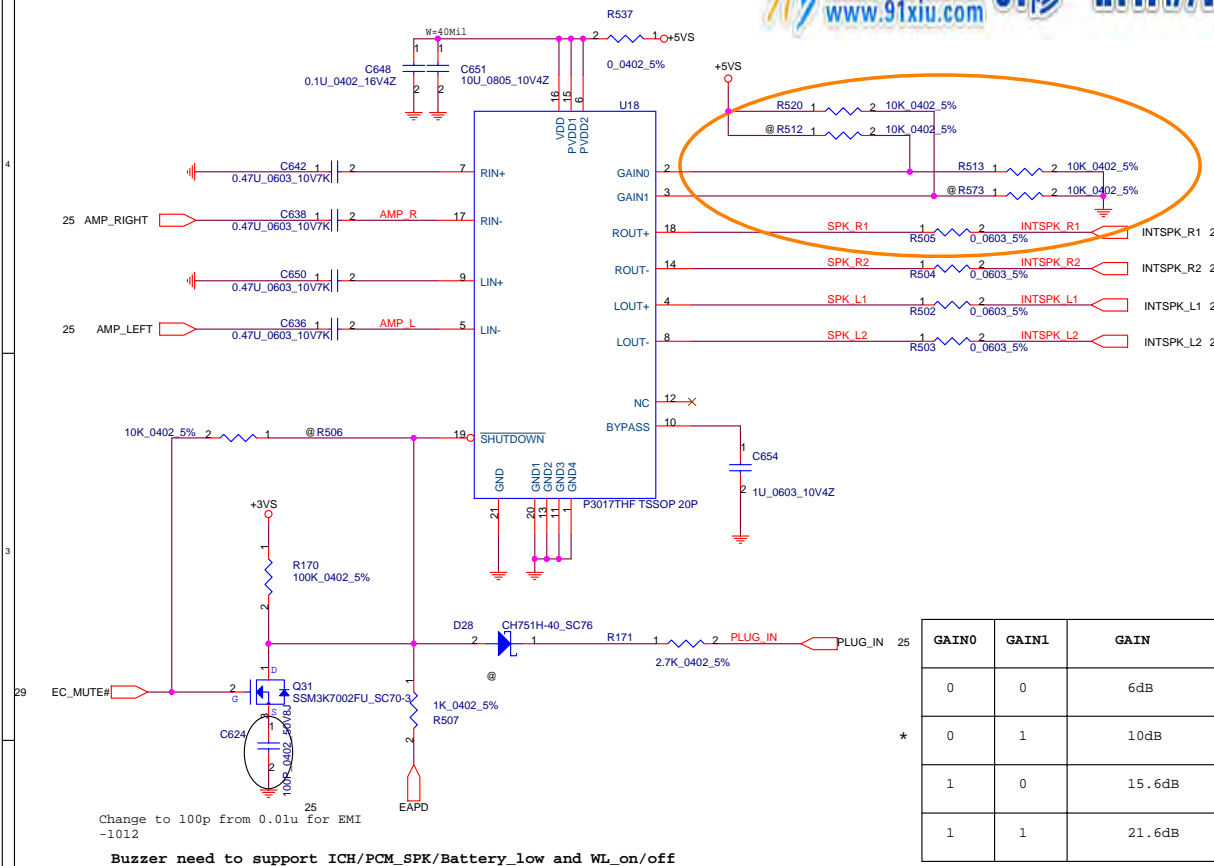
# HD Audio Codec



12/13 Modified this symbol for pin 13 and 14.  
Do not re-copy this symbol for other use



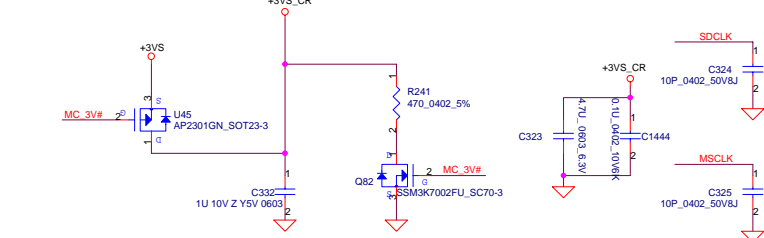
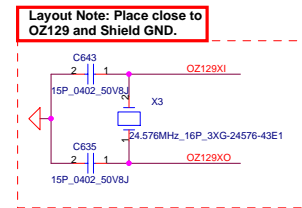
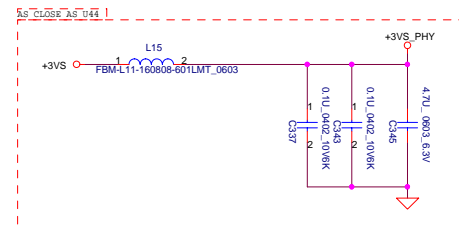
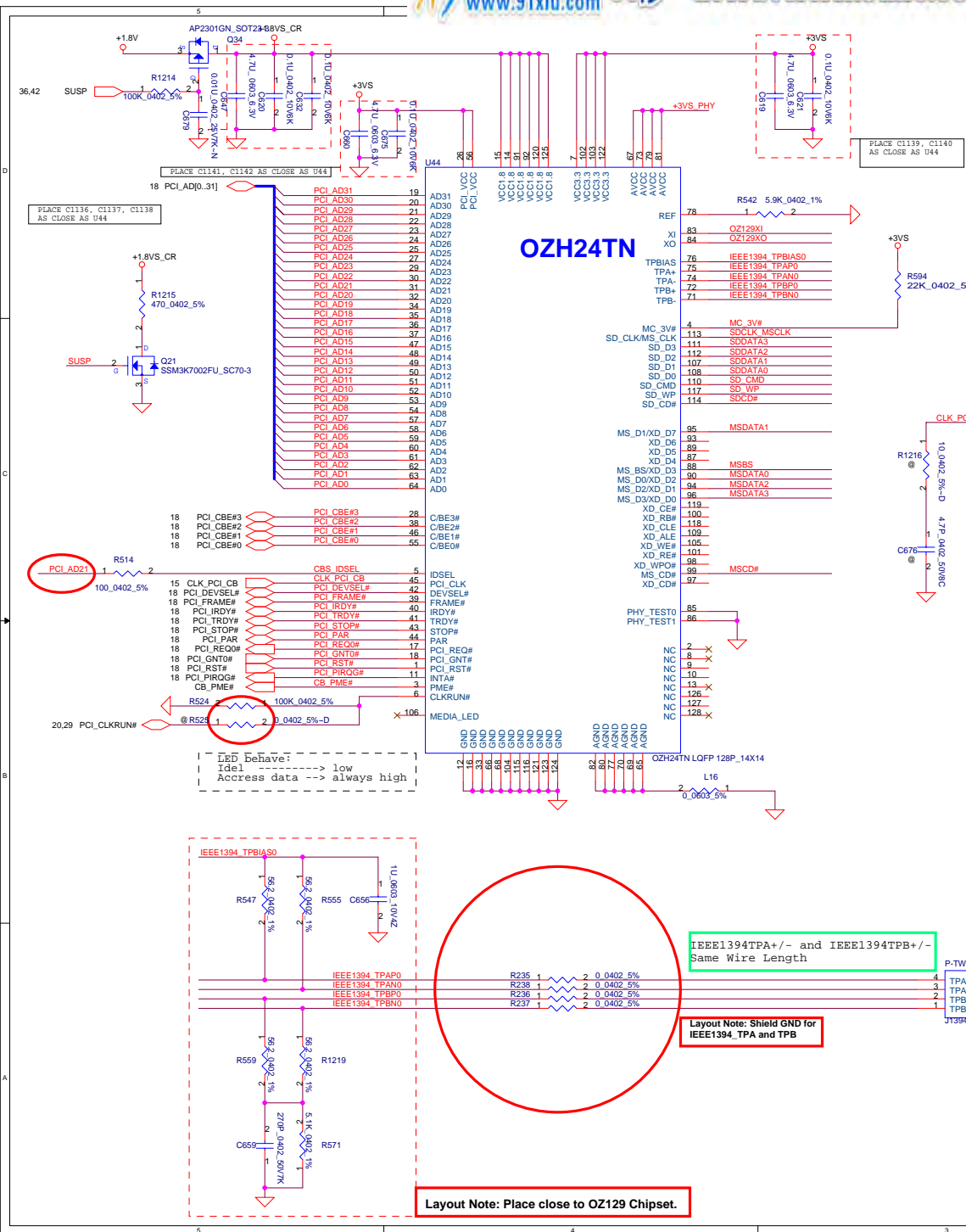
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GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

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C				Date:	Monday, December 15, 2008 Sheet 26 of 45

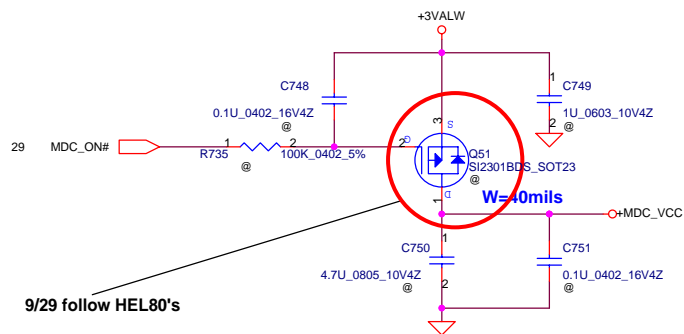
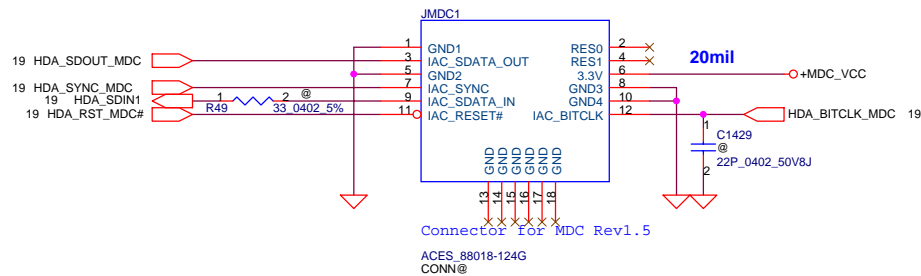




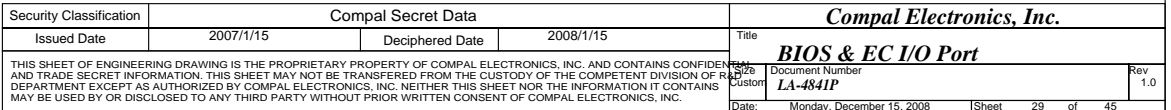
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Date: Monday, December 15, 2008				Sheet	27 of 45

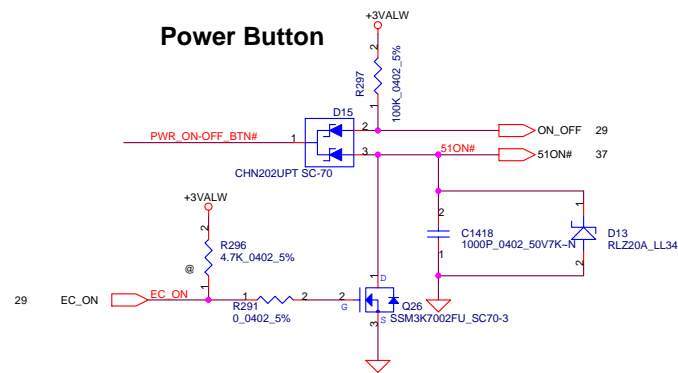
Pin connection diagram for the P2231NL\_QFN20 package. The diagram shows the internal connections of the package pins to the U11 chip. Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, and 20 are shown. Connections include: Pin 1 to C91 and C74; Pin 2 to C91 and C74; Pin 3 to C85; Pin 4 to C85; Pin 5 to C85; Pin 6 to PLT\_RST#; Pin 7 to SYSON; Pin 8 to SUSP#; Pin 9 to CPUSB#; Pin 10 to EXPR\_CPUSB#; Pin 11 to 1.5Vn; Pin 12 to 1.5Vn; Pin 13 to 1.5Vn; Pin 14 to 1.5Vn; Pin 15 to 3.3Vn; Pin 16 to 3.3Vn; Pin 17 to 3.3Vn; Pin 18 to 3.3Vn; Pin 19 to AUX\_IN; Pin 20 to AUX\_OUT. Power supply pins are connected to +1.5VS, +3VS, +3VALW, and +3VS\_PEC. Signal pins are connected to PLT\_RST#, SYSON, SUSP#, CPUSB#, EXPR\_CPUSB#, AUX\_IN, and AUX\_OUT. The package is labeled P2231NL\_QFN20.

+3V\_CARD Max. 1300mA, Average 1000mA

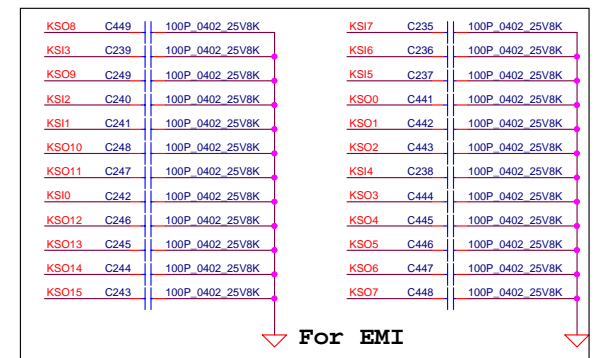
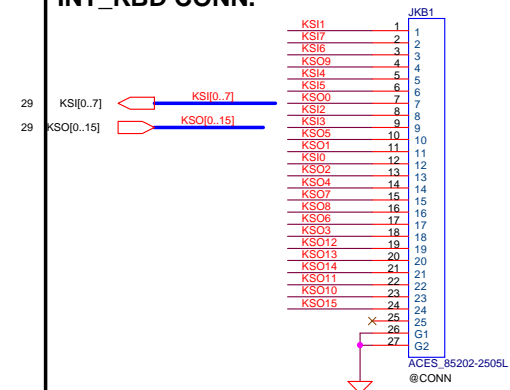


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				Customer	LA-484IP	1.0	
				Date:	Monday, December 15, 2008	Sheet 28 of 45	

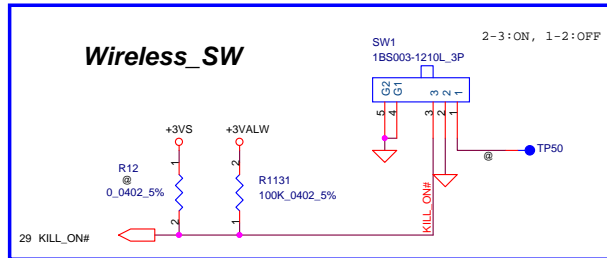




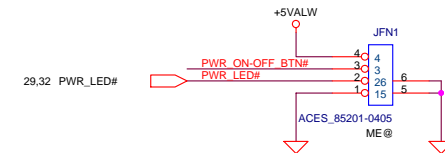
## INT\_KBD CONN.



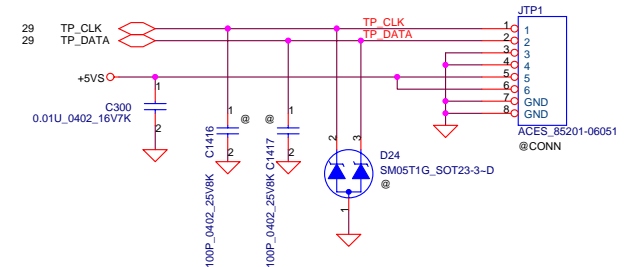
## SW/B CONN.



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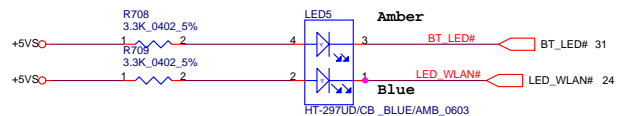
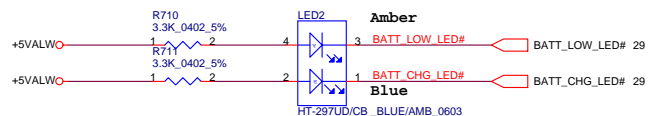
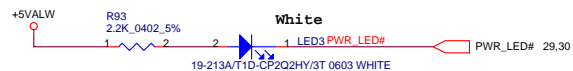


## Touch PAD/B CONN.



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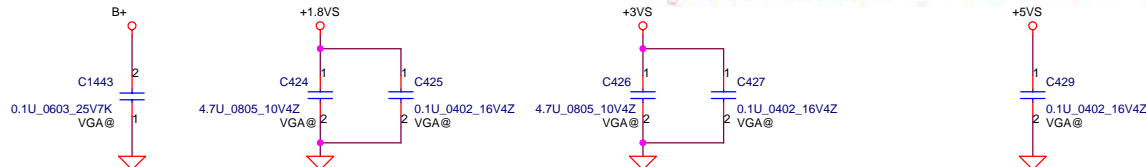


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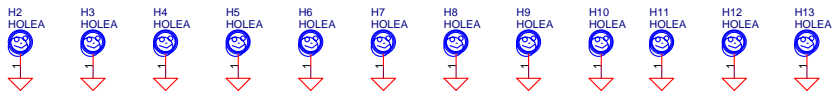


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				LA-4841P	1.0
				Date	Monday, December 15, 2008
				Sheet	33 of 45

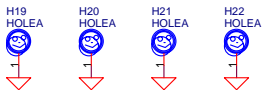
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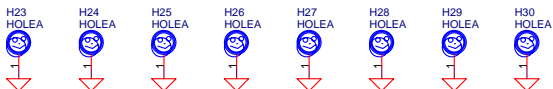
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H\_4P2



H\_3P2

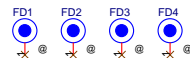


H\_5P6

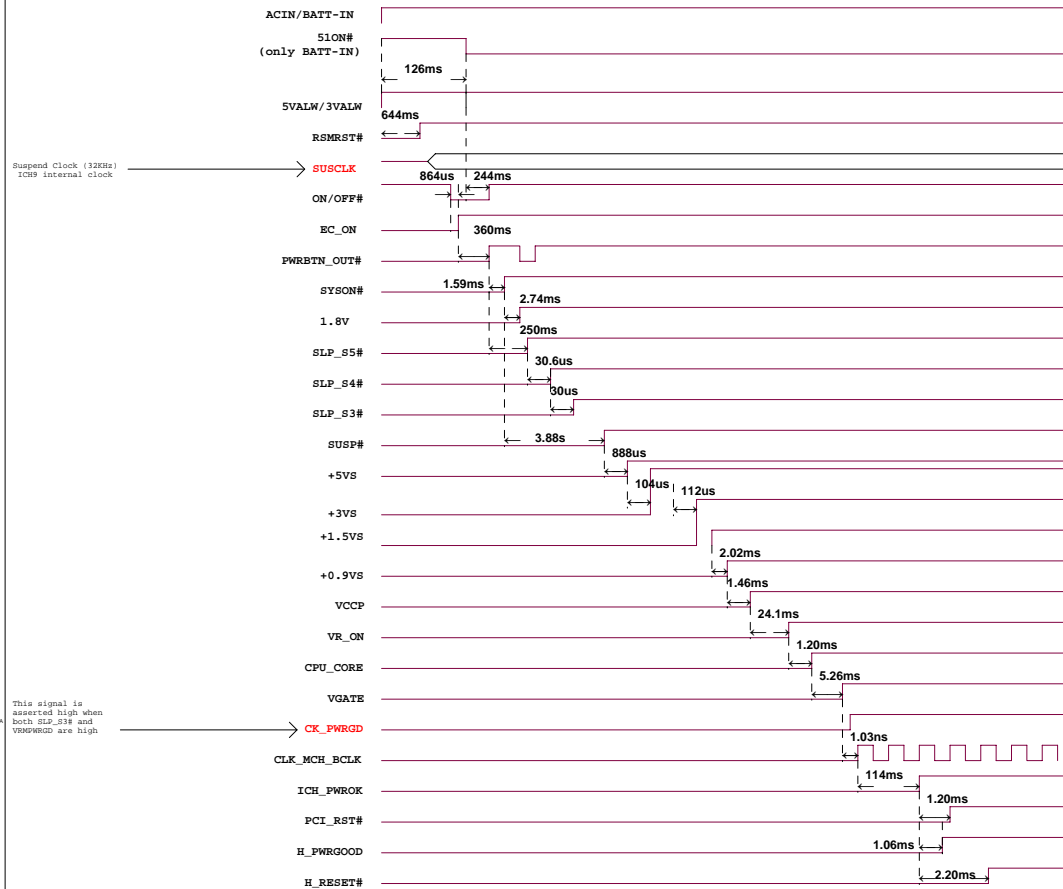


H\_4P4

H\_3P1N

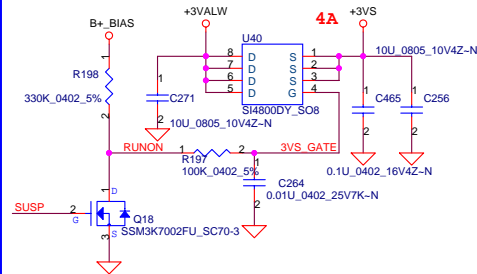


# KAL80 POWER UP SEQUENCE

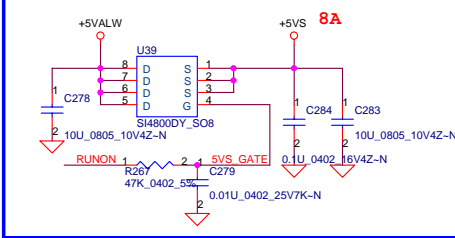


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## +3VALW to +3VS Transfer

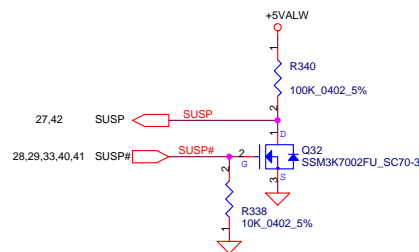
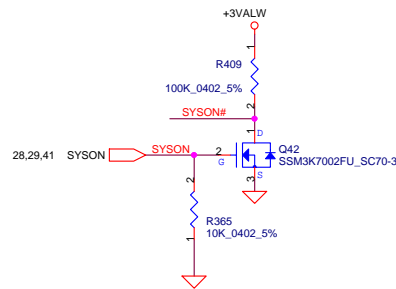
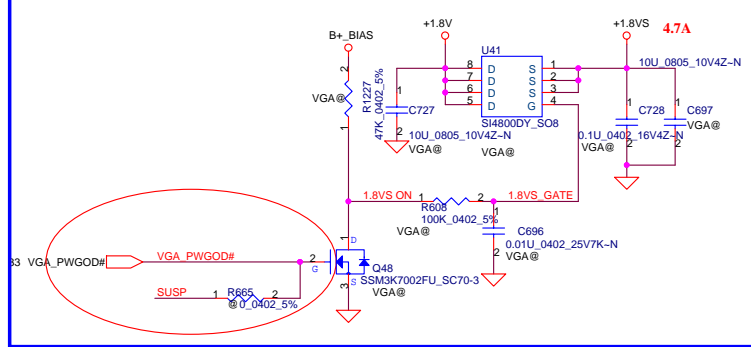


## +5VALW to +5VS Transfer

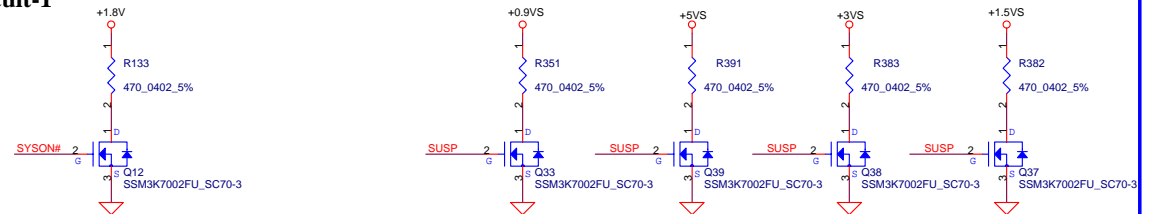


+CPU\_CORE --- C211 --- 0.1U\_0402\_16V4Z-N --- +VCCP

## +1.8V to +1.8VS Transfer

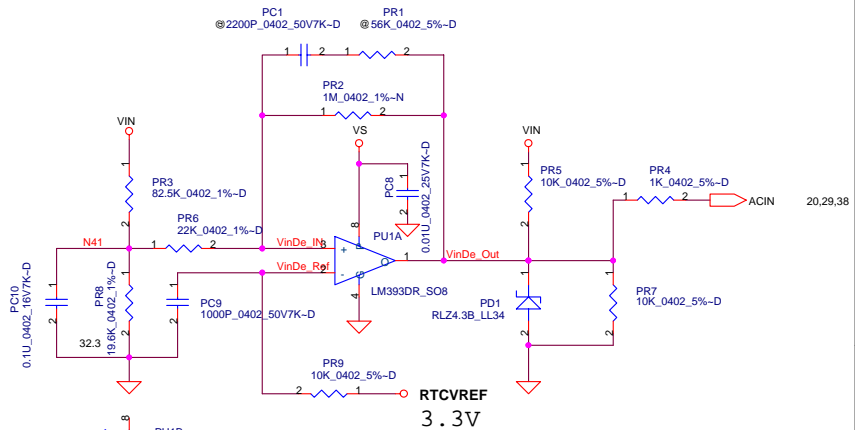
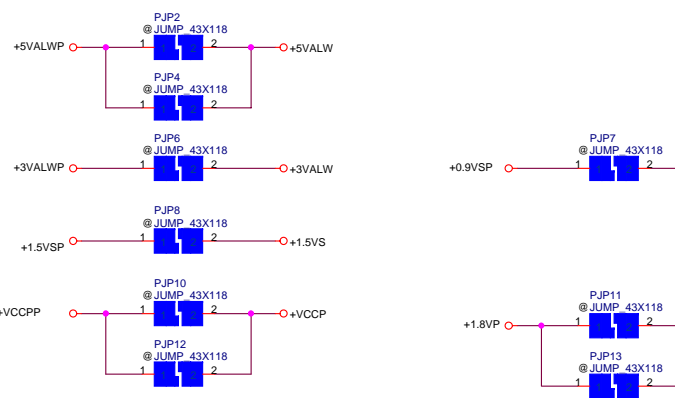
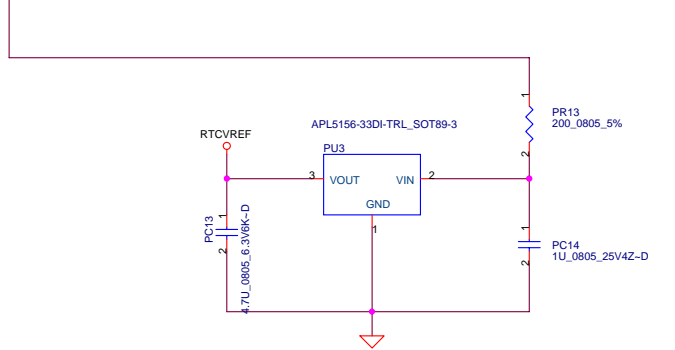
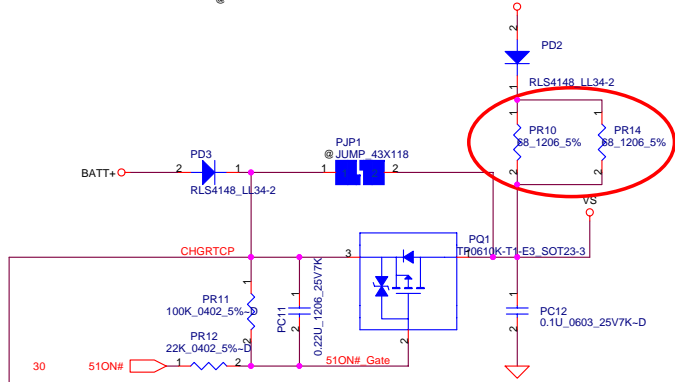
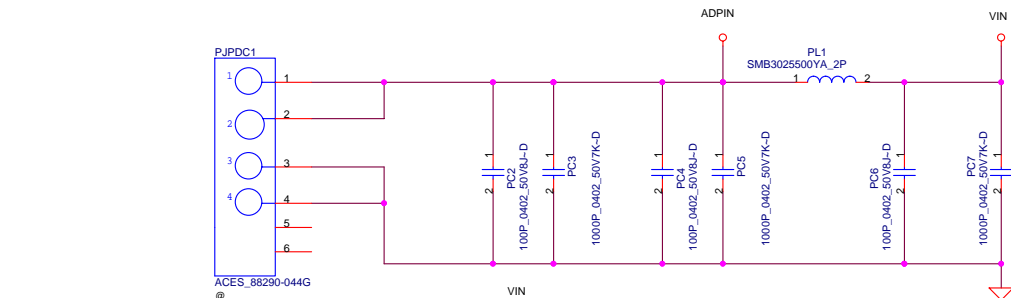


## Discharge circuit-1



SYSON -> SUSP# -> VGA\_ON->VGA\_PWGOD

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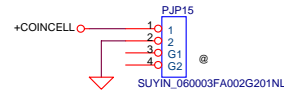
	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813

中华维修网 91修--HTTP://WWW.91XIU.COM

90W adapter  
 $I_{charge} = (V_{srset}/V_{vdac}) * (0.1/PR222) = 3A$   
 $I_{adapter} = (V_{vacset}/V_{vdac}) * (0.1/PR217) = 4.27A$   
 Input OVP : 22.3V  
 Input UVP : 16.98V  
 Fsw : 300KHz

中华维修网 91修 -- HTTP://WWW.91XIU.COM  
 www.91xiu.com

### COIN RTC Battery

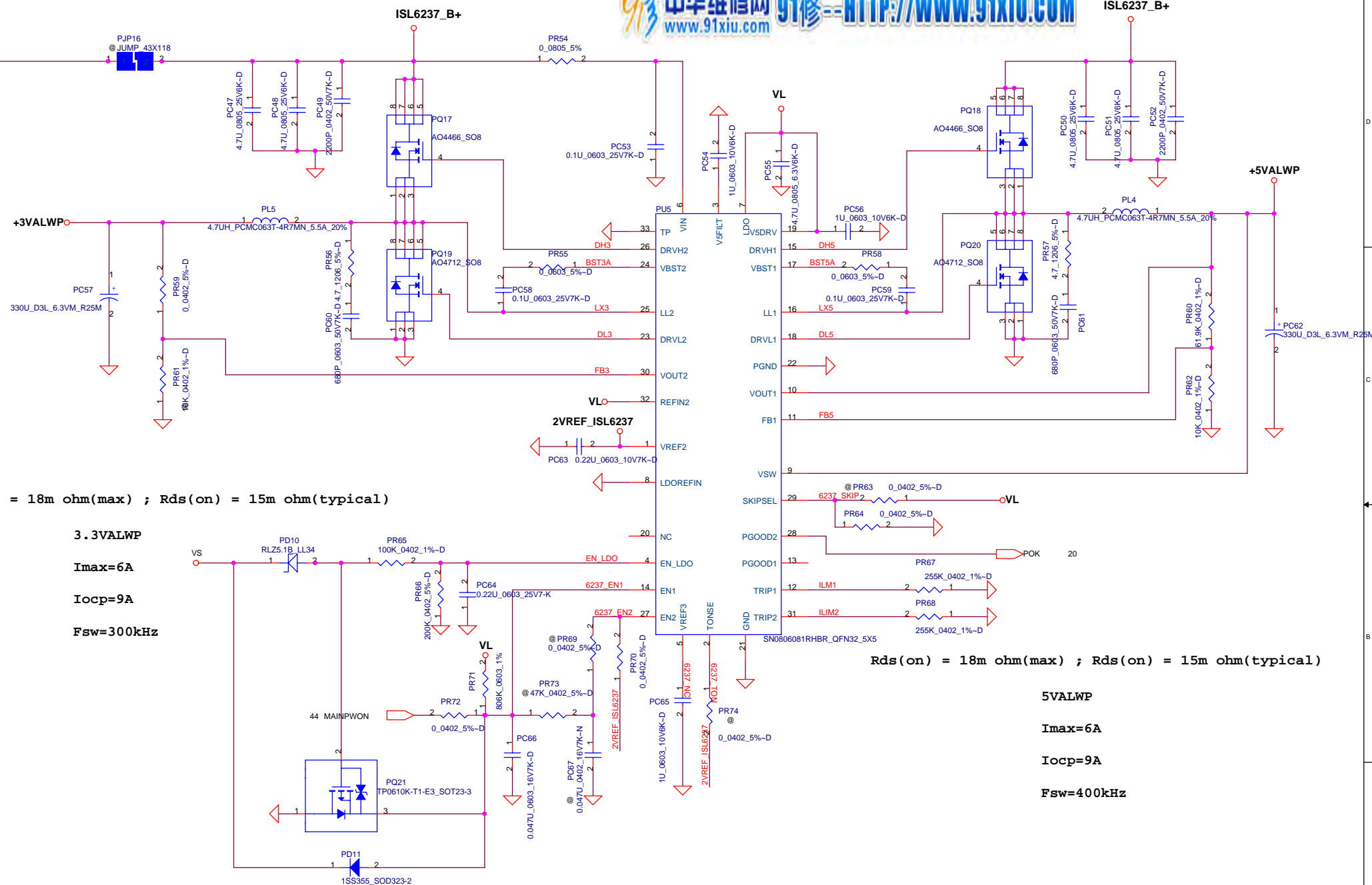


CHGVADJ	Battery Voltage/per cell
0V	3V
3.3V	4.2V

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Charger		
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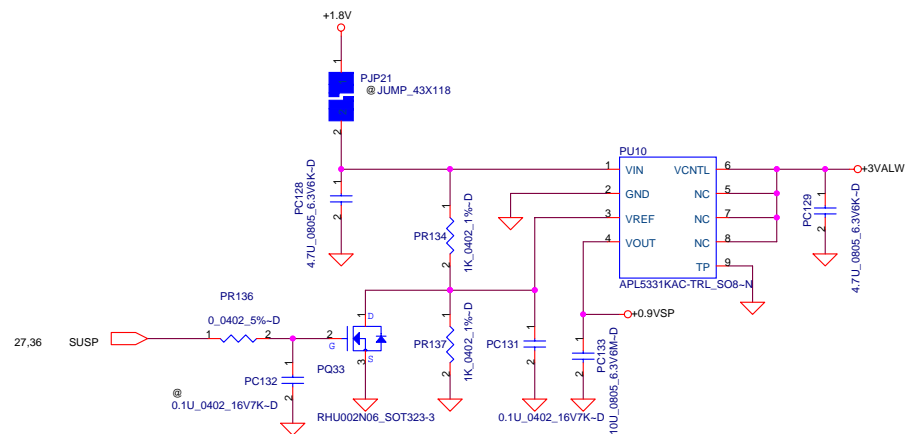
Rds(on) = 18m ohm(max) ; Rds(on) = 15m ohm(typical)

5VALWP  
Imax=6A  
Iocp=9A  
Fsw=400kHz

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Issued Date	2006/10/1	Deciphered Date	2007/05/30	Title	<b>+3VALWP, +5VALWP</b>	
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				Custom	<b>KFW11</b>	1.0
				Date:	Monday, December 15, 2008	Sheet 39 of 45

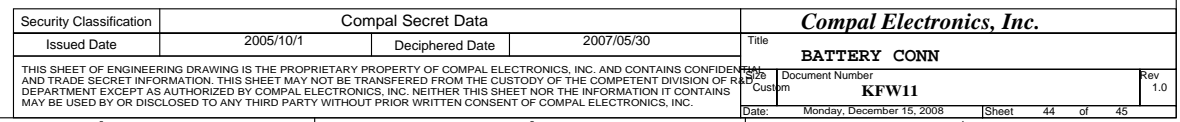
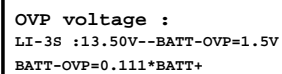
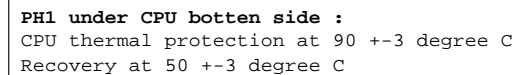






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