

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND1
LAYER 8 : BOT

VCC_CORE

+1.5V

+1.05V

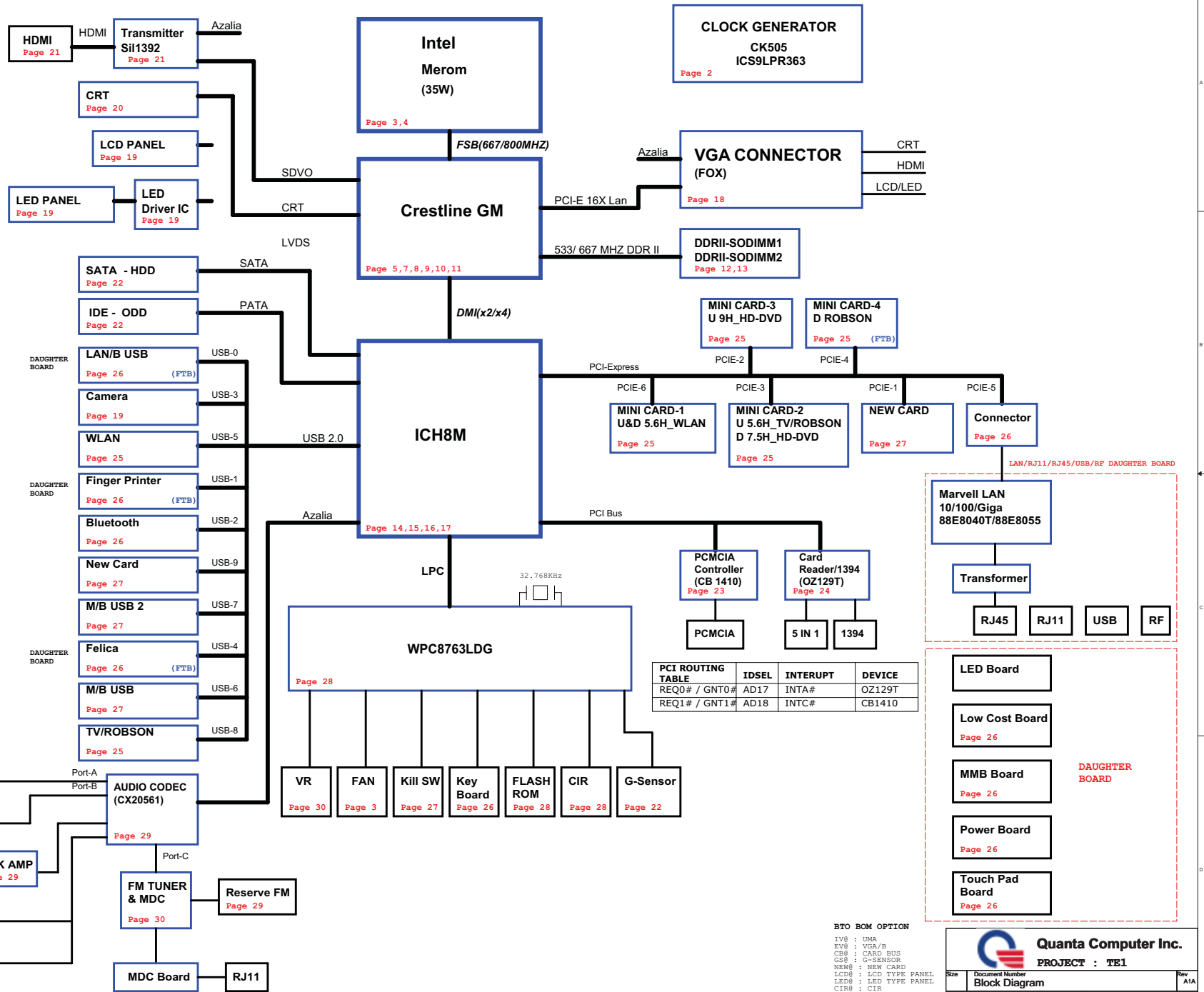
+1.25V

+1.8VSUS

+1.8V

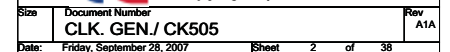
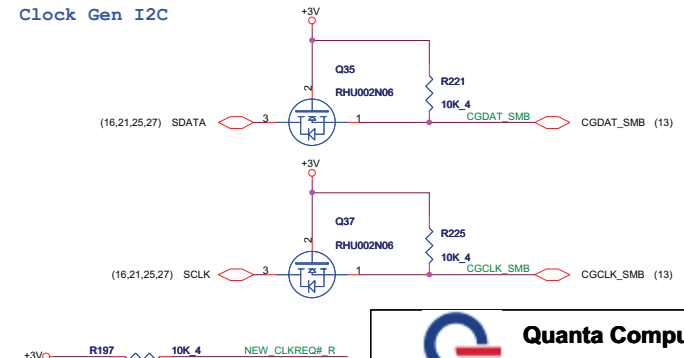
+3VPCU
+3V_S5
+3VSUS
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF

TE1 Block Diagram

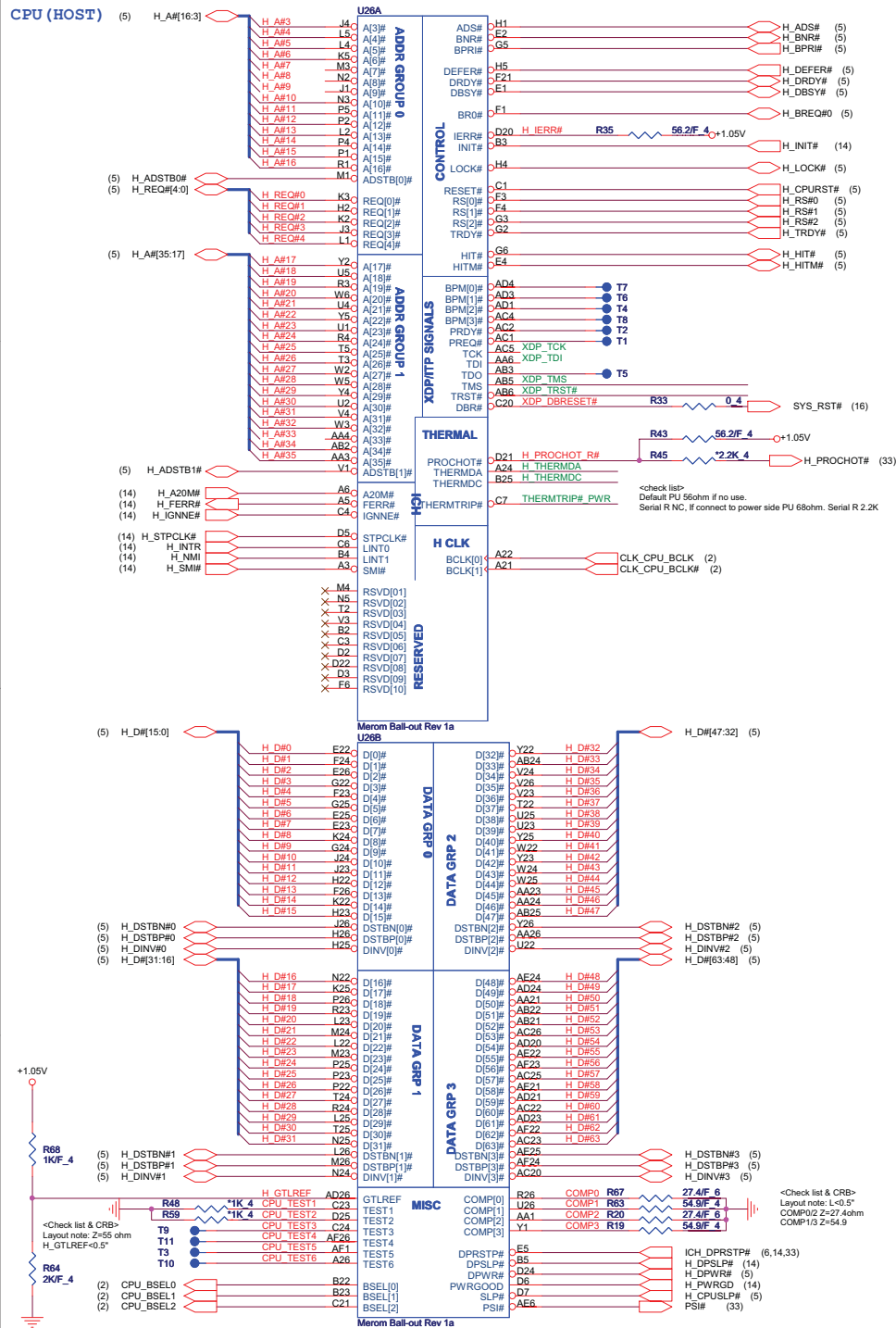


[illegible]

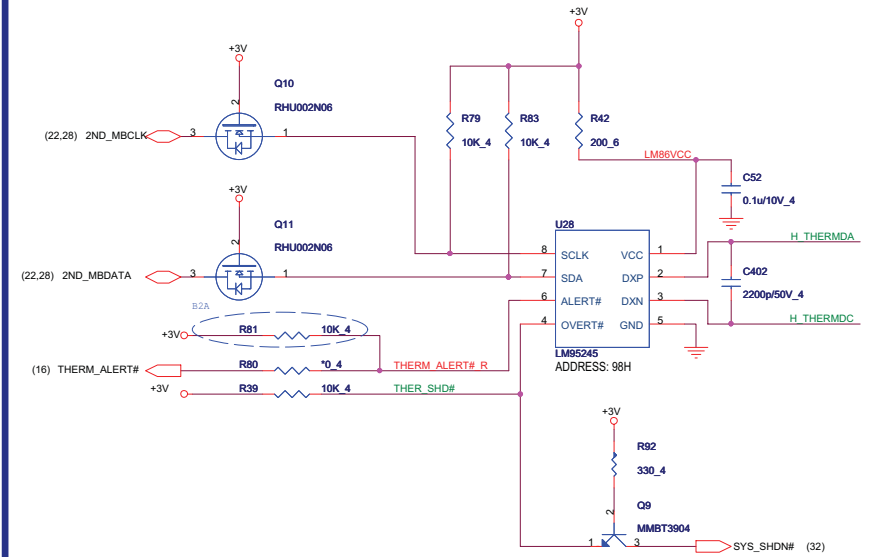
FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz



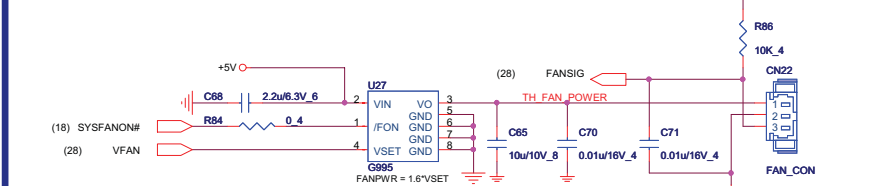
CPU (HOST)



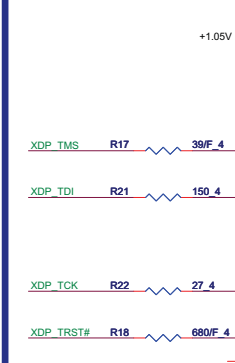
CPU Thermal monitor



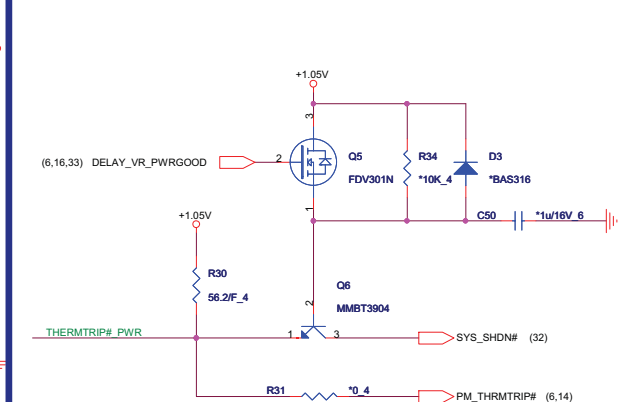
CPU FAN



PU/PD (ITP700)

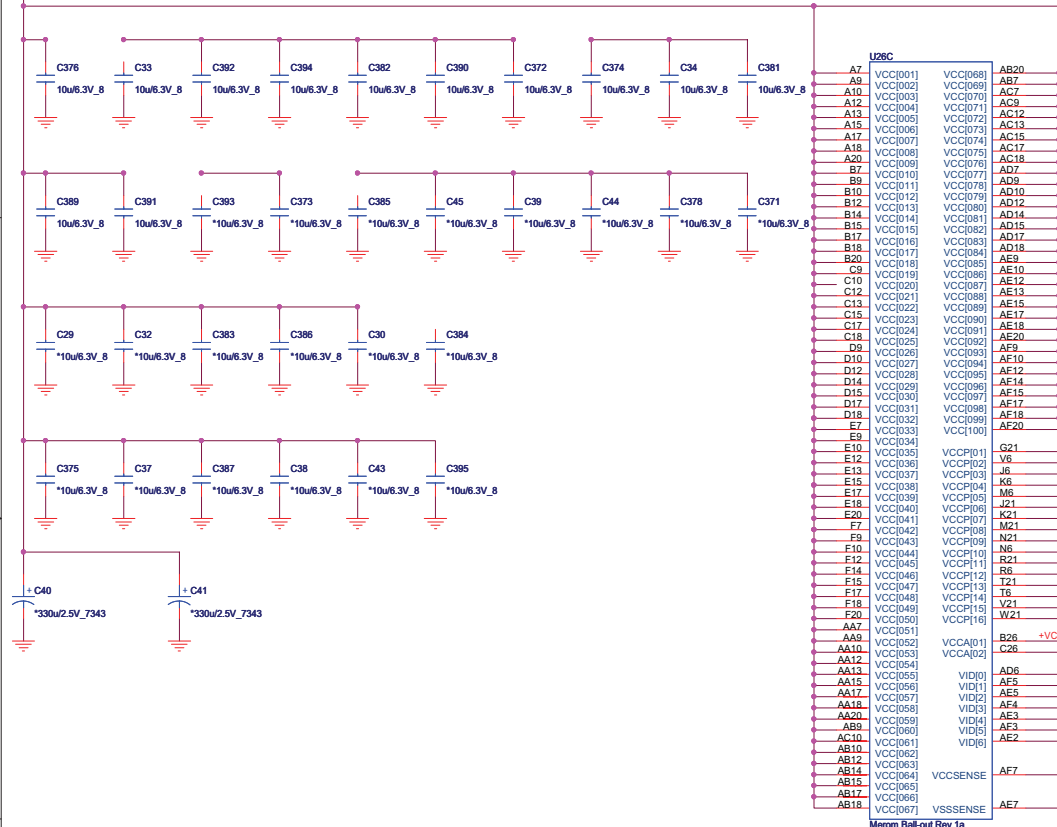


Thermal Trip



CPU (Power)

VCC_CORE



<REV.NO. 0.5/REF NO.19343>

Ivcc Max 52A

Ivccp Max 6A(VCCP supply before Vcc stable)

Max 2A(VCCP supply after Vcc stable)

Ivcca Max 130mA

+1.05V

<Check list>

ESR=12m ohm

+1.5V

+VCCA PROC

<CRB>

DTU near to B26 ball

VCC_CORE

R391

100F_6

VCCSENSE (33)

AE7

VSSSENSE (33)

AE7

<CRB>

Routing 27 Aohm with 50mils spacing

RUID near to CPU 1"

R390

100F_6

VCC_CORE

R73

0.01u/16V_4

C64

10u/10V_8

VCC_CORE

R74

0.01u/16V_6

C26

0.1u/16V_6

C25

330u/2.5V_7343

C35

ESR=12m ohm

<Check list>

ESR=12m ohm

+1.05V

<REV.NO. 0.5/REF NO.19343>

Ivcc Max 52A

Ivccp Max 6A(VCCP supply before Vcc stable)

Max 2A(VCCP supply after Vcc stable)

Ivcca Max 130mA

U26D

A4

VSS[001]

VSS[002]

VSS[003]

VSS[004]

VSS[005]

VSS[006]

VSS[007]

VSS[008]

VSS[009]

VSS[010]

VSS[011]

VSS[012]

VSS[013]

VSS[014]

VSS[015]

VSS[016]

VSS[017]

VSS[018]

VSS[019]

VSS[020]

VSS[021]

VSS[022]

VSS[023]

VSS[024]

VSS[025]

VSS[026]

VSS[027]

VSS[028]

VSS[029]

VSS[030]

VSS[031]

VSS[032]

VSS[033]

VSS[034]

VSS[035]

VSS[036]

VSS[037]

VSS[038]

VSS[039]

VSS[040]

VSS[041]

VSS[042]

VSS[043]

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VSS[066]

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VSS[068]

VSS[069]

VSS[070]

VSS[071]

VSS[072]

VSS[073]

VSS[074]

VSS[075]

VSS[076]

VSS[077]

VSS[078]

VSS[079]

VSS[080]

VSS[081]

VSS[082]

VSS[083]

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VSS[100]

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VSS[102]

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VSS[113]

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VSS[161]

VSS[162]

VSS[163]

VSS[164]

VSS[165]

VSS[166]

VSS[167]

VSS[168]

VSS[169]

VSS[170]

VSS[171]

VSS[172]

VSS[173]

VSS[174]

VSS[175]

VSS[176]

VSS[177]

VSS[178]

VSS[179]

VSS[180]

VSS[181]

VSS[182]

VSS[183]

VSS[184]

VSS[185]

VSS[186]

VSS[187]

VSS[188]

VSS[189]

VSS[190]

VSS[191]

VSS[192]

VSS[193]

VSS[194]

VSS[195]

VSS[196]

VSS[197]

VSS[198]

VSS[199]

VSS[200]

VSS[201]

VSS[202]

VSS[203]

VSS[204]

VSS[205]

VSS[206]

VSS[207]

VSS[208]

VSS[209]

VSS[210]

VSS[211]

VSS[212]

VSS[213]

VSS[214]

VSS[215]

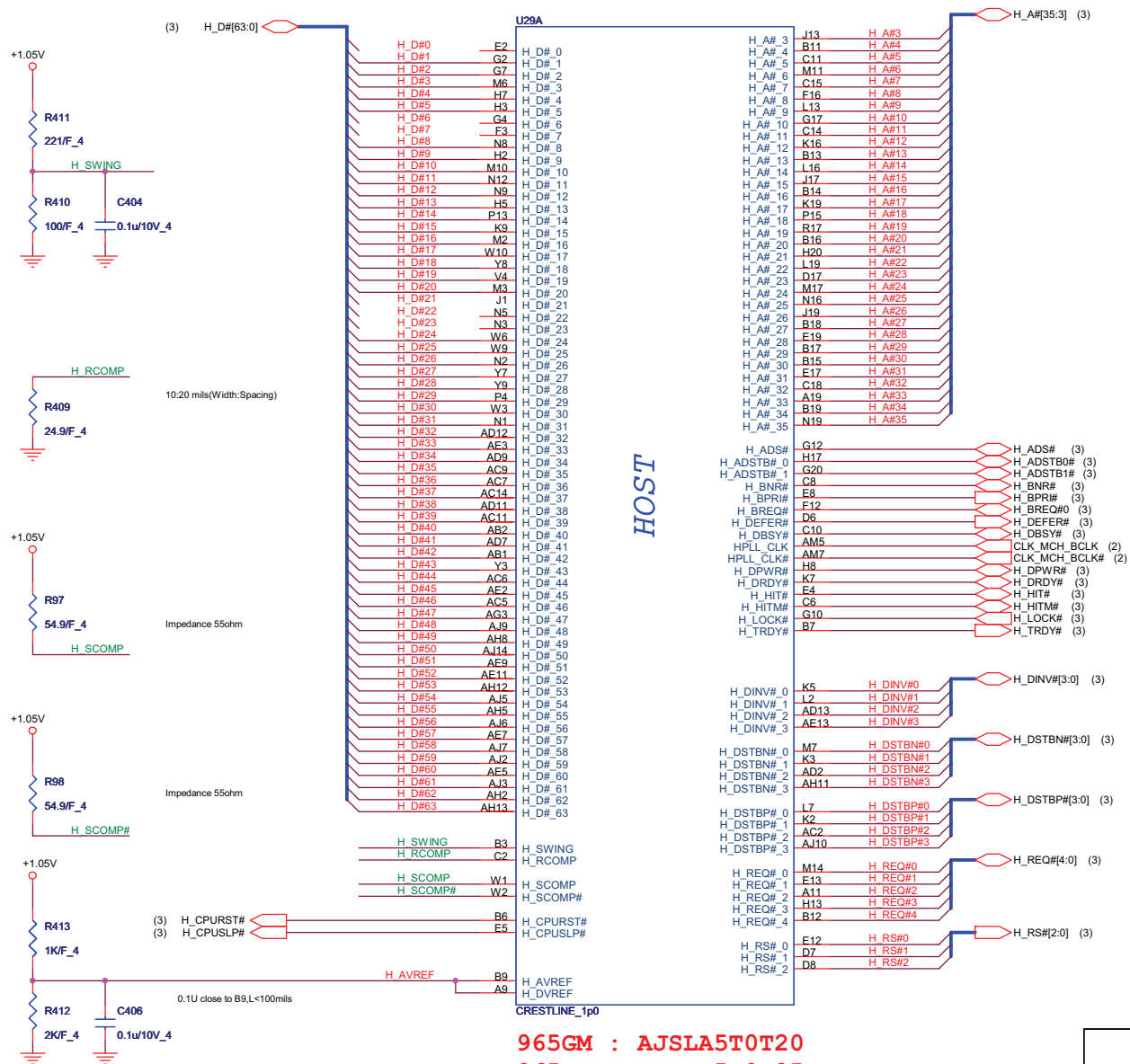
VSS[216]

VSS[217]

VSS[218]

VSS[219]

NB (HOST)



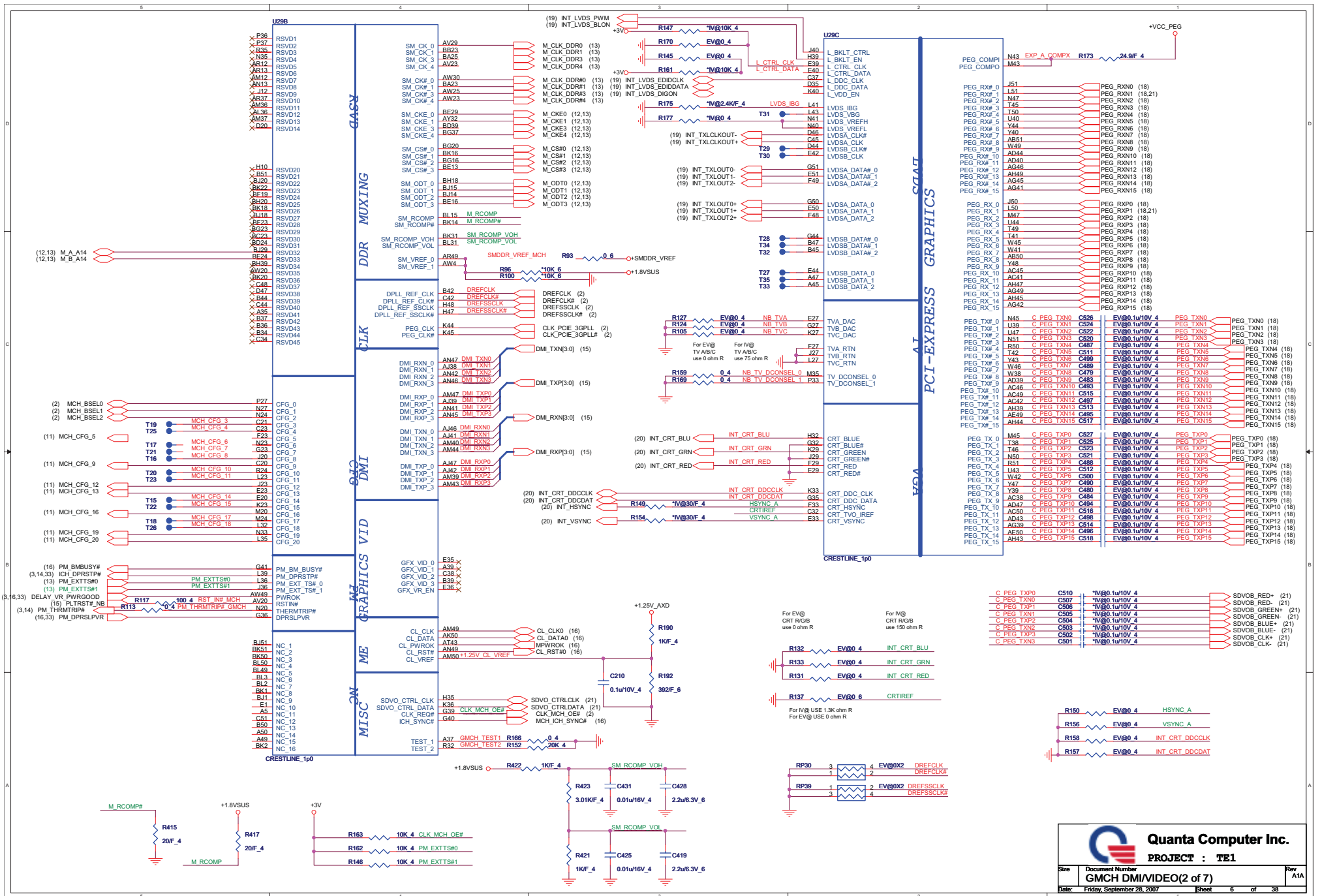
965GM : AJSLA5T0T20
965PM : AJSLA5U0T25
960GML : AJSLA5V0T09



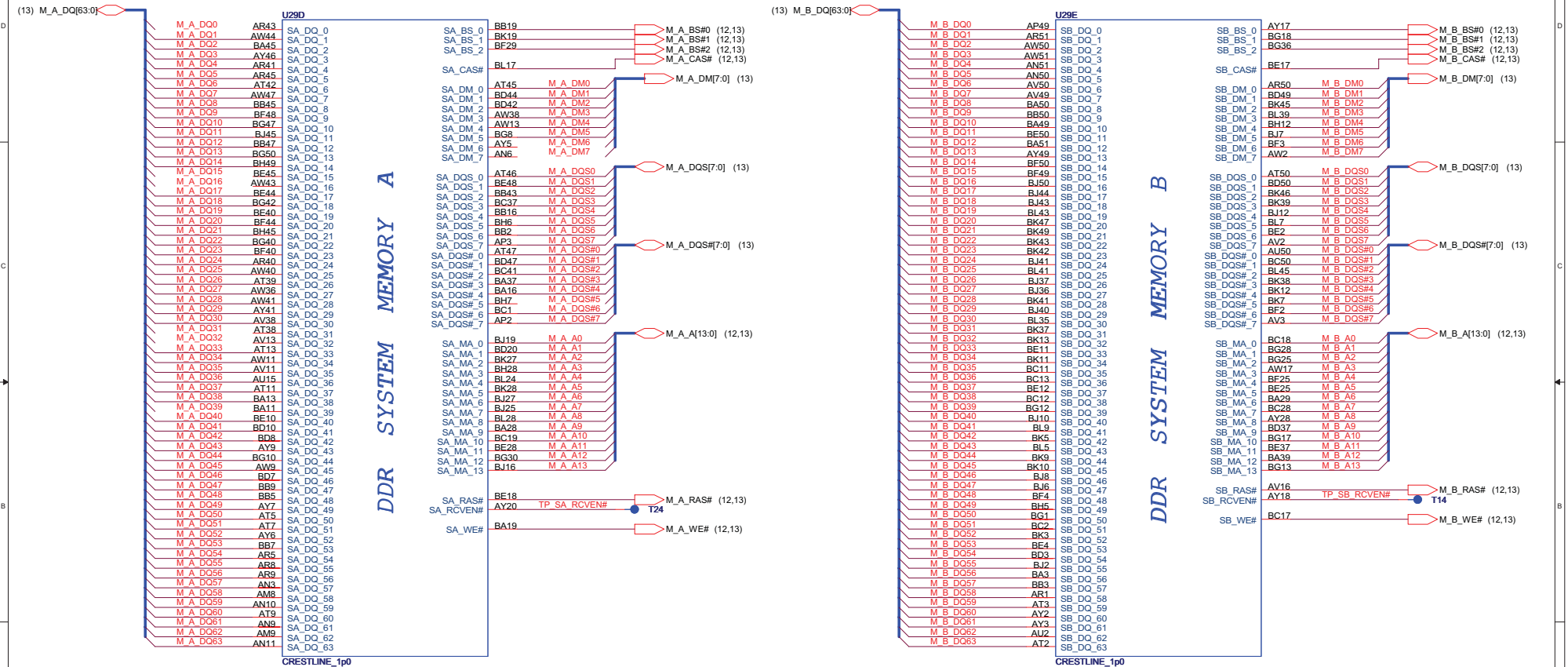
Quanta Computer Inc.
PROJECT : TE1

PROJECT : TE1

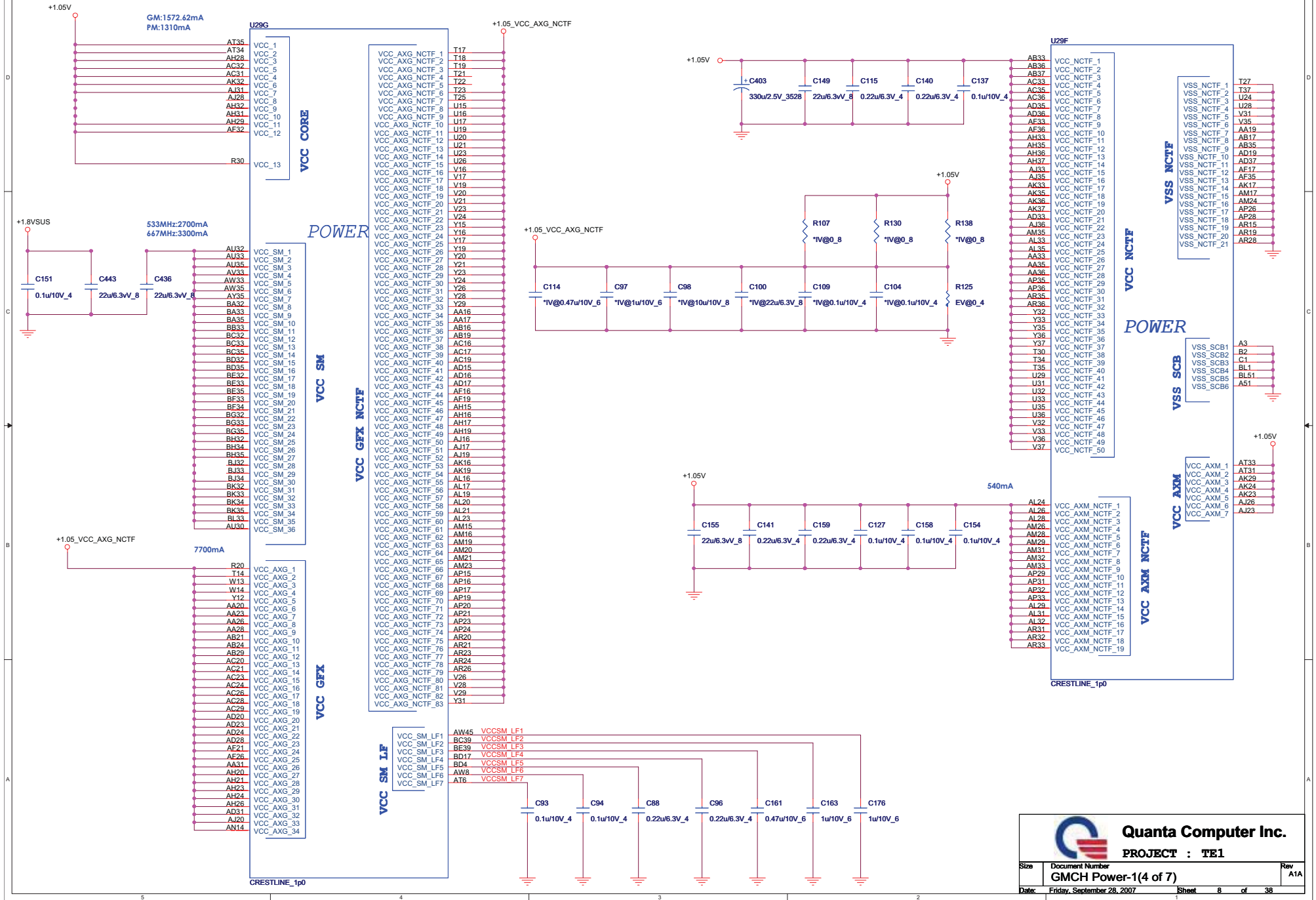
Size	Document Number GMCH HOST(1 of 7)	Rev A1A
Date:	Friday, September 28, 2007	Sheet 5 of 38



NB(Memory controller)



NB(Power-1)

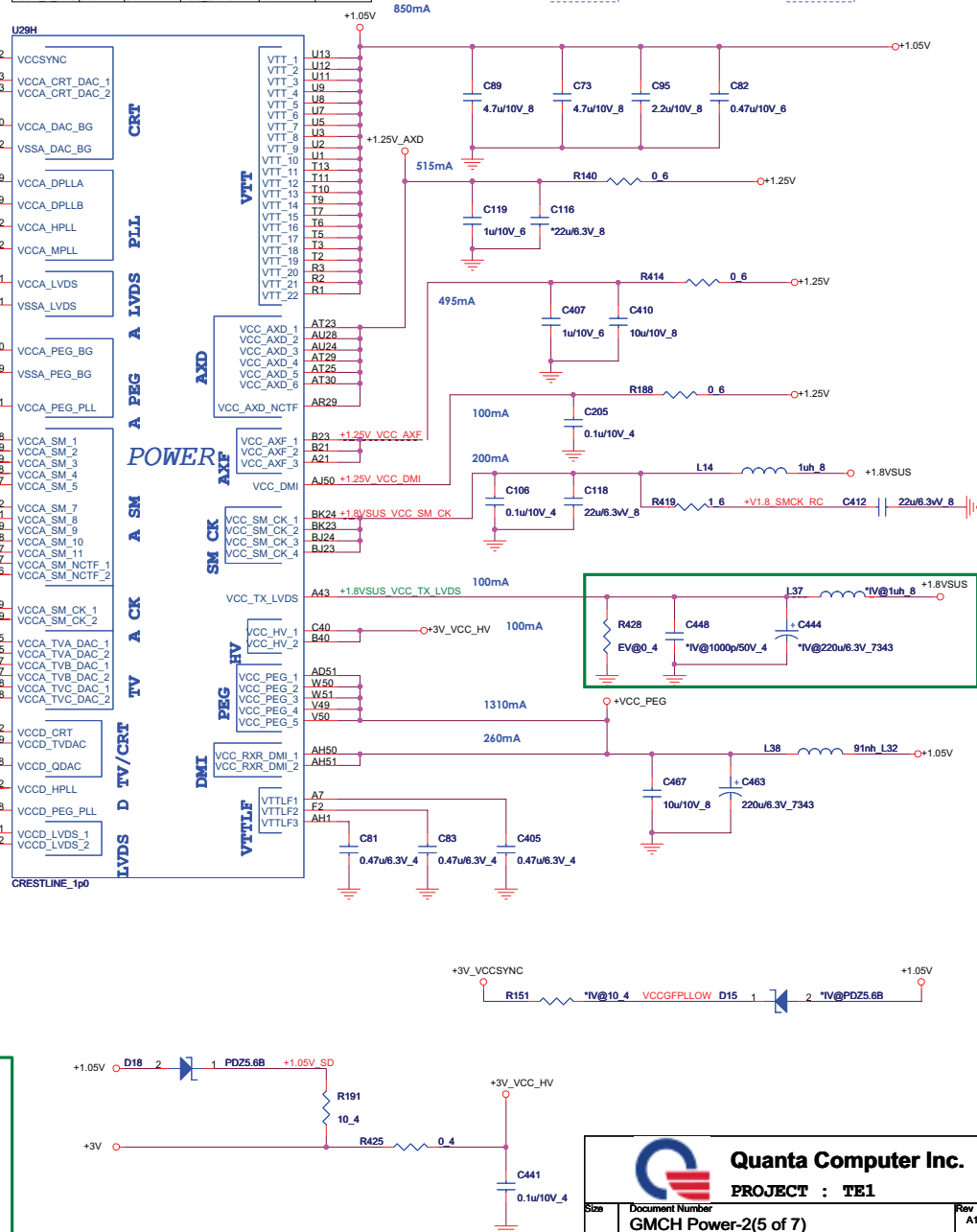


Ball	Enable	Disable	Ball	Enable	Disable
VCCA CRT	3.3V	GND	VCCA C_TVO	3.3V	GND
VCCD CRT	1.5V	GND	VCCD_TVO	1.5V	1.5V
VCCDO CRT	1.5V	GND	VCCABG DAC	3.3V	GND
VCCA A_TVO	3.3V	GND	VSSABG DAC	GND	GND
VCCA B_TVO	3.3V	GND	VCC SYNC	3.3V	GND

External VGA with EV@part, Internal VGA with IV@ part

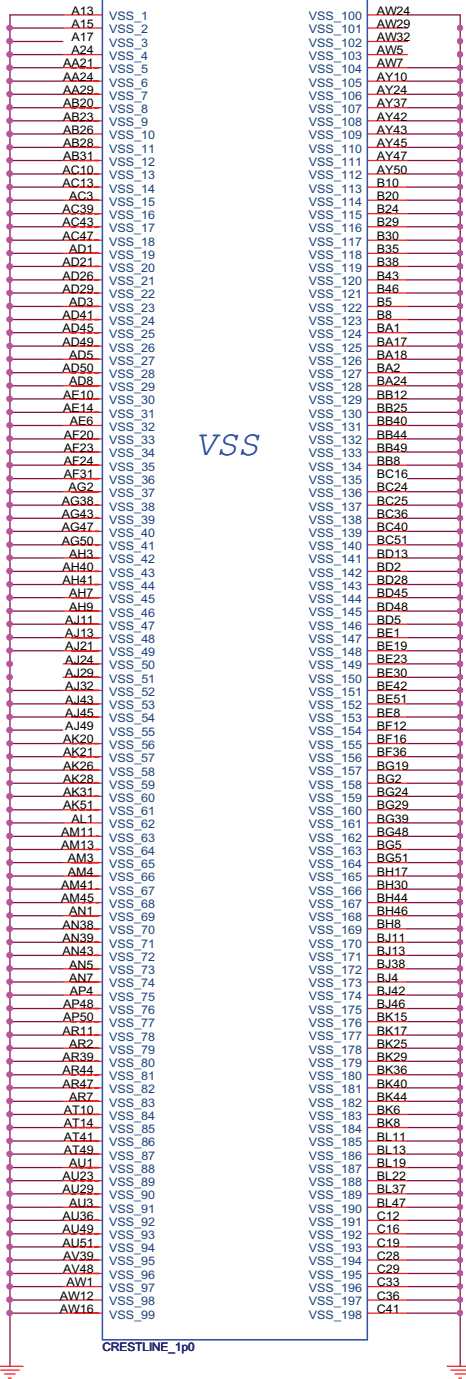
Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCTX_LVDS	GND	GND	1.8V

EXTERNAL *INTERNAL*

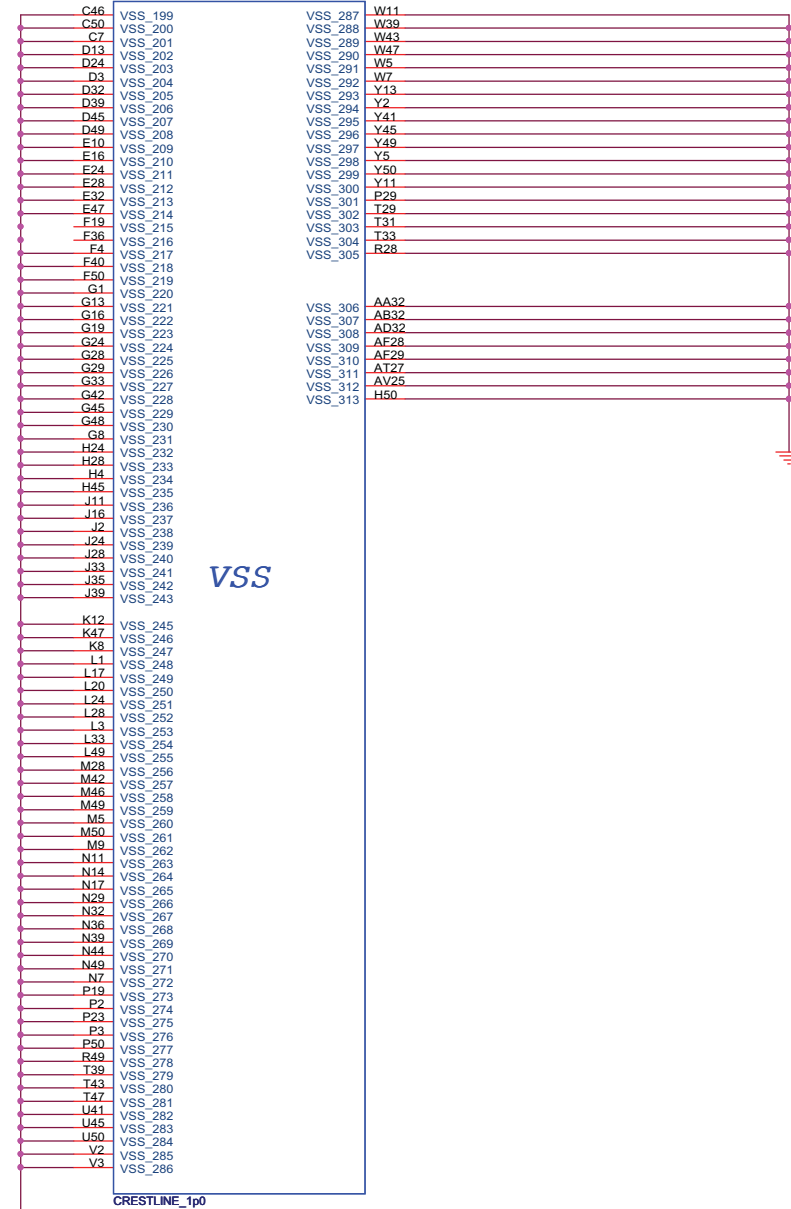


NB(Power-3)

U29I



U29J



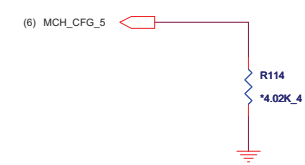
Strap table(base on checklist Ver1.6)

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal
CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	Intel? Management Engine Crypto strap	0 = Intel? Management Engine Crypto Transport Layer.Security (TLS) cipher suite with no confidentiality 1= Intel Management Engine Crypto TLS Cipher Suite with confidentiality (default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE is operation(Default) 1 = SDVO and PCIE are operating simultaneously via the PEG port

DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIx4(Default)
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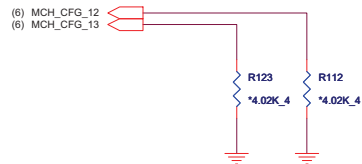
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane
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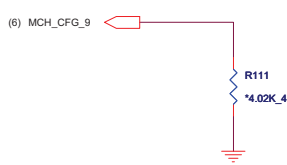
XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)
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SDVO Present

Strap define at External
HDMI control page

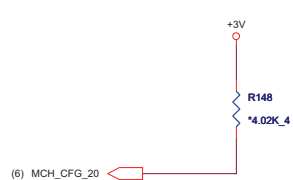
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)
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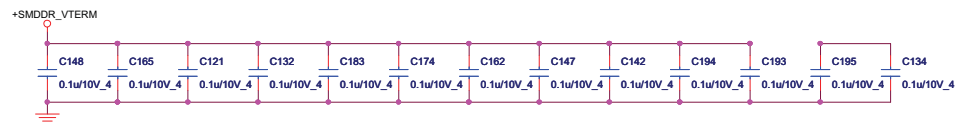


SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE is operational(Default) High = SDVO andPCIE are operating simultaneously via the PEG port
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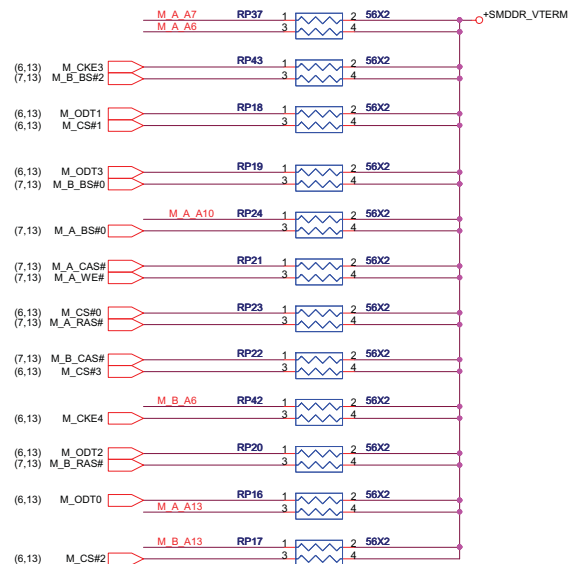
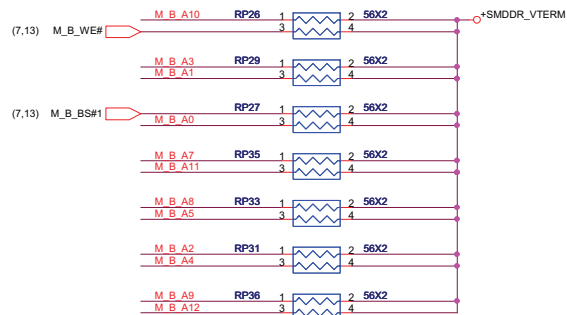
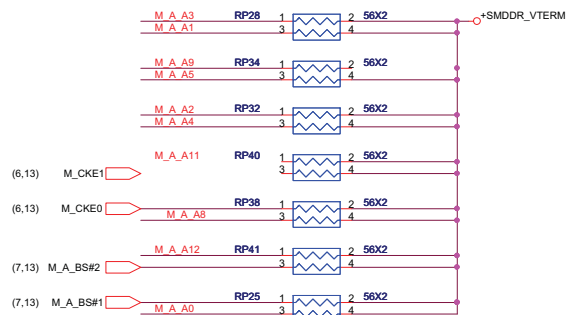
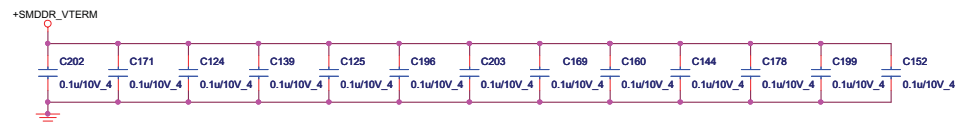


DDR2 A CHANNEL



Place one cap close to every 2 pull-up resistor terminated to SMDDR_VTERM

DDR2 B CHANNEL



DDR2 Dual channel A/B CONN

DDR2 VCC (SUS)
DDR2-600 each dimm is 2.8A
DDR2-667 EACH DIMM IS 2.6A
VTERM(SUS)
3A

+1.8VSUS

SMDDR_VREF_DIMM

CN25

VREF

DM0

DM1

DM2

DM3

DM4

DM5

DM6

DM7

DM8

DM9

DM10

DM11

DM12

DM13

DM14

DM15

DM16

DM17

DM18

DM19

DM20

DM21

DM22

DM23

DM24

DM25

DM26

DM27

DM28

DM29

DM30

DM31

DM32

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DM35

DM36

DM37

DM38

DM39

DM40

DM41

DM42

DM43

DM44

DM45

DM46

DM47

DM48

DM49

DM50

DM51

DM52

M_A_DQ6

M_A_DQ5

M_A_DQS#0

M_A_DQS#0

M_A_DQ2

M_A_DQ3

M_A_DQ9

M_A_DQ8

M_A_DQS#1

M_A_DQS#1

M_A_DQ14

M_A_DQ11

M_A_DQ17

M_A_DQ20

M_A_DQS#2

M_A_DQS#2

M_A_DQ23

M_A_DQ19

M_A_DQ28

M_A_DQ25

M_A_DM3

M_A_DQ26

M_A_DQ27

M_A_DQ28

M_A_DQ25

M_A_DM3

M_A_DQ26

M_A_DQ27

M_A_DQ28

M_A_DQ25

M_A_DM3

M_A_DQ26

M_A_DQ27

M_A_DQ28

M_A_DQ25

M_A_DM3

M_A_DQ26

M_A_DQ27

M_A_DQ28

M_A_DQ25

M_A_DM3

M_A_DQ26

M_A_DQ27

M_A_DQ28

M_A_DQ25

M_A_DM3

M_A_DQ26

M_A_DQ27

M_A_DQ28

M_A_DQ25

M_A_DM3

M_A_DQ26

M_A_DQ27

M_A_DQ28

M_A_DQ25

M_A_DM3

M_A_DQ26

(6,12) M_CKE0

(7,12) M_A_BS#2

M_A_A12

M_A_A9

M_A_A8

M_A_A5

M_A_A3

M_A_A1

M_A_A10

M_A_BS#0

M_A_WE#

M_A_CAS#

M_A_CS#1

M_ODT1

M_A_DQ36

M_A_DQ37

M_A_DQS#4

M_A_DQS#4

M_A_DQ39

M_A_DQ34

M_A_DQ40

M_A_DQ41

M_A_DQ41

M_A_DQ42

M_A_DQ46

M_A_DQ63

M_A_DQ49

M_A_DQS#6

M_A_DQS#6

M_A_DQ50

M_A_DQ51

M_A_DQ56

M_A_DQ60

M_A_DQ61

M_A_DQ67

M_A_DQ62

M_A_DQ63

CGDAT_SMB

CGCLK_SMB

VDD(SPD)

DDR2 5.6H

SO-DIMM0 SPD Address is 0xA0

SO-DIMM0 TS Address is 0x30

H: 5.6mm

CLOCK 0,1

CKE 0,1

SMDDR_VREF_DIMM

CN24

VREF

DM0

DM1

DM2

DM3

DM4

DM5

DM6

DM7

DM8

DM9

DM10

DM11

DM12

DM13

DM14

DM15

DM16

DM17

DM18

DM19

DM20

DM21

DM22

DM23

DM24

DM25

DM26

DM27

DM28

DM29

DM30

DM31

DM32

DM33

M_B_DQ0

M_B_DQ5

M_B_DQS#0

M_B_DQS#0

M_B_DQ7

M_B_DQ3

M_B_DQ9

M_B_DQ8

M_B_DQS#1

M_B_DQS#1

M_B_DQ11

M_B_DQ10

M_B_DQ20

M_B_DQ17

M_B_DQS#2

M_B_DQS#2

M_B_DQ22

M_B_DQ18

M_B_DQ28

M_B_DQ25

M_B_DM3

M_B_DQ26

M_B_DQ27

M_B_DQ28

M_B_DQ25

M_B_DM3

M_B_DQ26

M_B_DQ27

M_B_DQ28

M_B_DQ25

M_B_DM3

M_B_DQ26

M_B_DQ27

M_B_DQ28

M_B_DQ25

M_B_DM3

M_B_DQ26

(6,12) M_CKE3

(7,12) M_B_BS#2

M_B_A12

M_B_A9

M_B_A8

M_B_A5

M_B_A3

M_B_A1

M_B_A10

M_B_BS#0

M_B_WE#

M_B_CAS#

M_B_CS#3

M_ODT3

M_B_DQ37

M_B_DQ38

M_B_DQS#4

M_B_DQS#4

M_B_DQ34

M_B_DQ35

M_B_DQ35

M_B_DQ40

M_B_DQ41

M_B_DQ41

M_B_DQ45

M_B_DQ46

M_B_DQ43

M_B_DQ49

M_B_DQS#6

M_B_DQS#6

M_B_DQ51

M_B_DQ54

M_B_DQ56

M_B_DQ57

M_B_DQ59

M_B_DQ62

M_B_DQ62

CGDAT_SMB

CGCLK_SMB

VDD(SPD)

DDR2 10.1H

SO-DIMM1 SPD Address is 0xA4

SO-DIMM1 TS Address is 0x34

H: 10.1mm

CLOCK 3,4

CKE 2,3

Close to DIMM0

+1.8VSUS

C461

C447

C459

C438

C446

C440

*330u/2.5V_3528

2.2u/6.3V_6

2.2u/6.3V_6

2.2u/6.3V_6

2.2u/6.3V_6

2.2u/6.3V_6

2.2u/6.3V_6

2.2u/6.3V_6

2.2u/6.3V_6

2.2u/6.3V_6

2.2u/6.3V_6

+1.8VSUS

C136

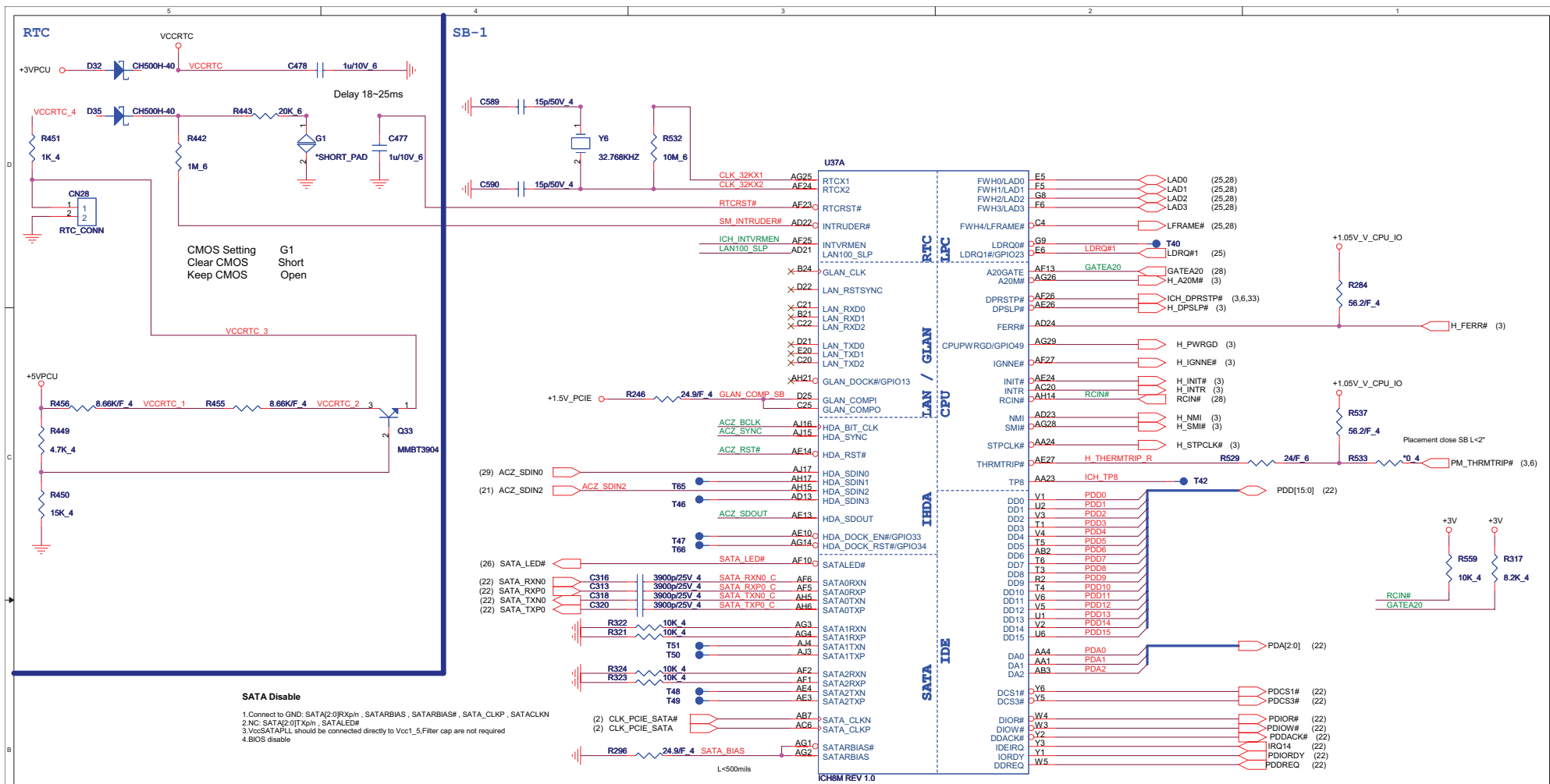
C180

C450

C168

C74

C78



SB Strap

ICH8-M Internal VR Enable strap (Internal VR for Vccsus1_5, VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
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ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1_05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
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XOR Chain Entrance Strap

ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIE port config bit 1

HDA

Quanta Computer Inc.

PROJECT : TE1

Size	Document Number	Rev
	ICH8M HOST(1 of 4)	A1A
Date:	Friday, September 28, 2007	Sheet 14 of 38

U37B

Pin	Function	Signal Type
A00	D20	Input
A01	E19	Input
A02	D19	Input
A03	A24	Input
A04	D17	Input
A05	A21	Input
A06	A16	Input
A07	C19	Input
A08	A18	Input
A09	B16	Input
A10	A12	Input
A11	E16	Input
A12	A14	Input
A13	G16	Input
A14	A15	Input
A15	B6	Input
A16	C11	Input
A17	A8	Input
A18	D11	Input
A19	B12	Input
A20	C12	Input
A21	D10	Input
A22	G7	Input
A23	F13	Input
A24	E11	Input
A25	E13	Input
A26	E12	Input
A27	D8	Input
A28	A6	Input
A29	E8	Input
A30	D6	Input
A31	A3	Input

PCI

Pin	Function	Signal Type
REQ0#	GNT0#	Output
REQ1#/GPI050	GNT1#/GPI051	Output
C18	GNT1#	Output
B19	REQ2#	Output
E18	GNT2#	Output
A11	REQ3#	Output
C10	GNT3#	Output
C17	CBE0#	Output
E15	CBE1#	Output
E16	CBE2#	Output
E17	CBE3#	Output
C8	IRDY#	Output
D9	PAR	Output
G6	PCIRST#	Output
D16	DEVSEL#	Output
A7	PERR#	Output
B7	LOCK#	Output
C10	SERR#	Output
C16	STOP#	Output
C9	TRDY#	Output
A17	FRAME#	Output
AG24	PLT_RST-#	Output
B10	PCLK_I#	Output
G7	PME#	Output

Interrupt I/O

Pin	Function	Signal Type
F8	INT#	Input
G11	INT#	Input
F12	INT#	Input
B3	INT#	Input
R234	0.4	Input
CRT_SENSE#		Input

CHRM Rev 1.0

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#	OZ129T
REQ1# / GNT1#	AD20	INTC#	CB1410

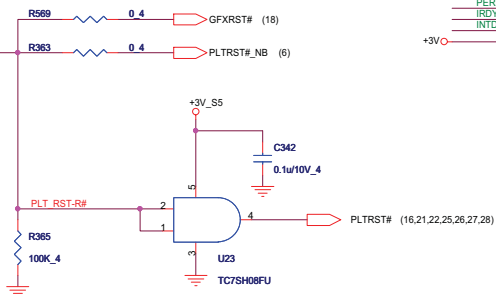
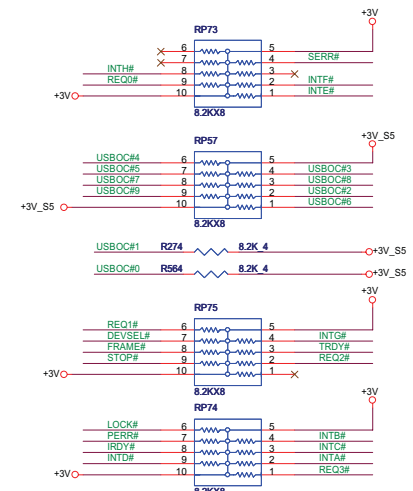
PCI_GNT#3	Low = A16 swap override enabled High = Default
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GNT3# R469 *1K 4

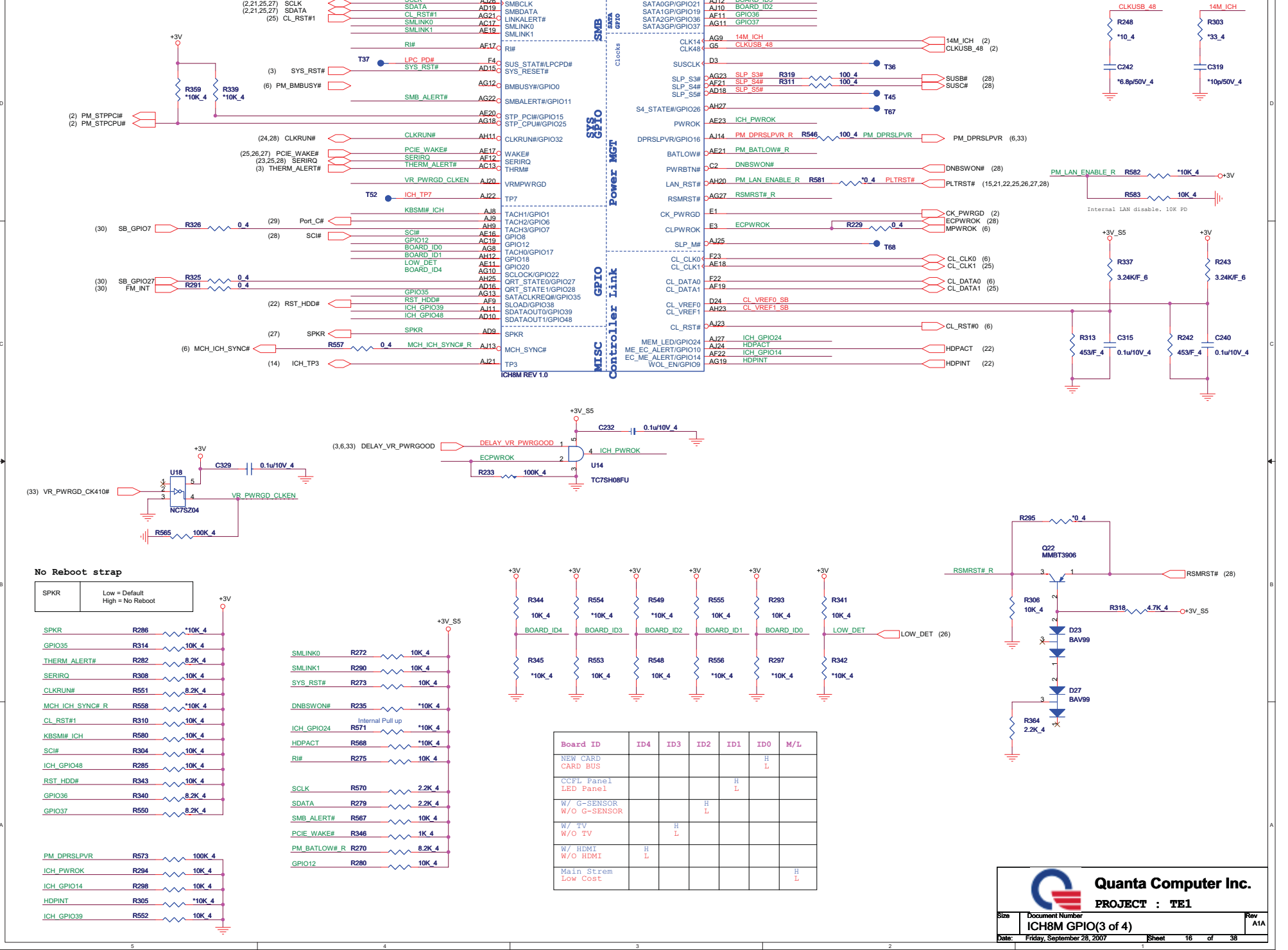
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

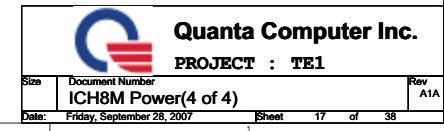
SPI_CS1# R467 *1K 4

GNT0# R244 *1K 4



SB-GPIO





VGA/B conn

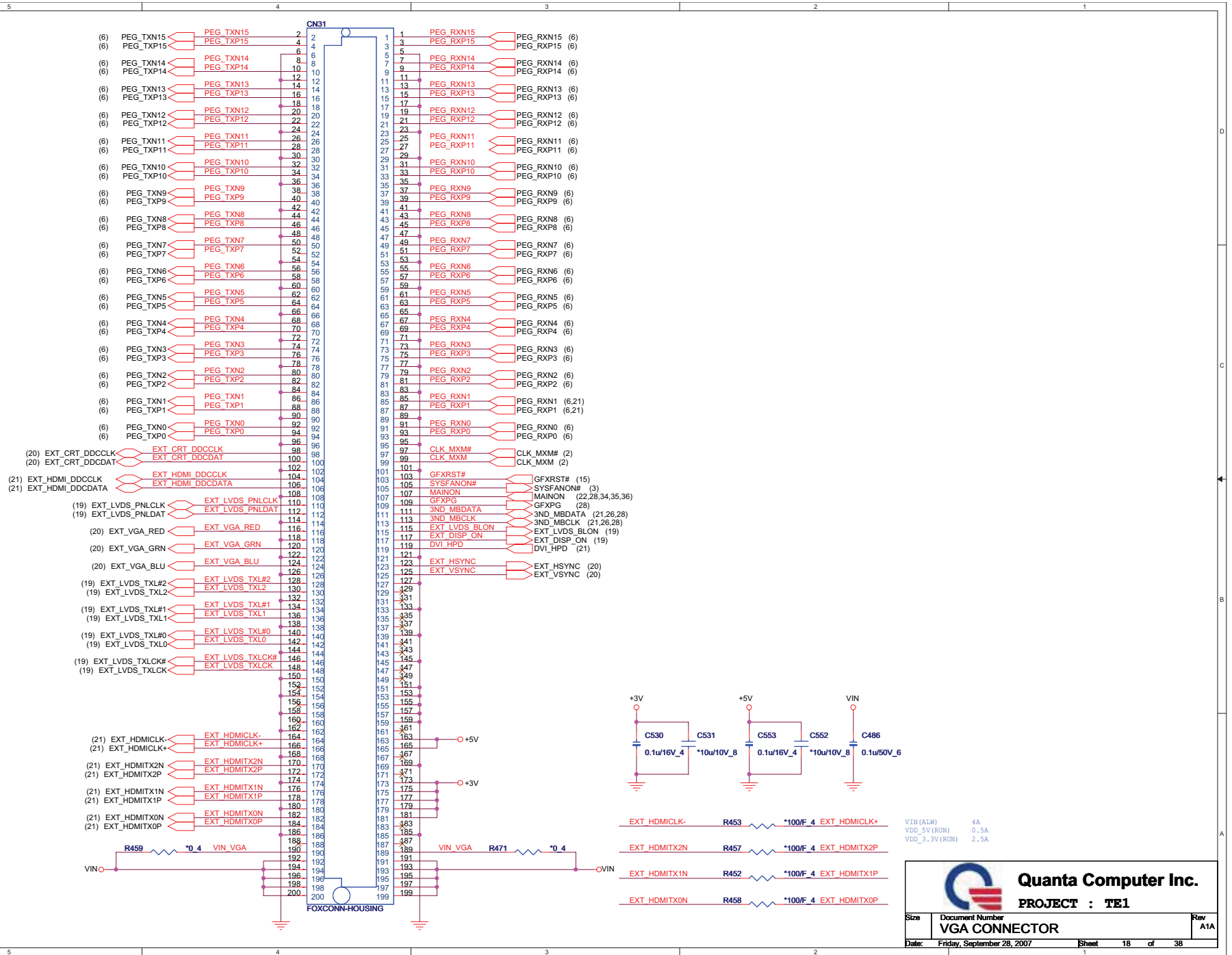


Figure 10 illustrates the pin connections for the LCD module, showing two rows of connections. The top row shows connections for TXCLKOUT+ and TXCLKOUT- signals, which are connected to RP11 and RP5 respectively. The bottom row shows connections for TXOUT2+, TXOUT2-, TXOUT1+, TXOUT1-, TXOUT0+, TXOUT0-, EDIDCLK+, EDIDCLK-, EDIDDATA+, and EDIDDATA- signals, which are connected to RP8, RP2, RP9, RP3, RP10, RP4, RP7, and RP1 respectively. Each connection is shown with a resistor (R5, R4) and a 2.2K resistor. The signals are labeled as TXCLKOUT+, TXCLKOUT-, TXOUT2+, TXOUT2-, TXOUT1+, TXOUT1-, TXOUT0+, TXOUT0-, EDIDCLK+, EDIDCLK-, EDIDDATA+, and EDIDDATA-.

The schematic diagram illustrates the power supply section for the USBP3 module. It features a +5V input connected to a MOSFET (Q28, AO3413) through a resistor R384 (0.8 ohms). The MOSFET's gate is connected to the +5V input. The MOSFET's drain is connected to the CCD_POWER line, which is also connected to a 10uF 10V capacitor (C380) and a 1000uF 50V capacitor (C359). The MOSFET's source is connected to ground. The CCD_POWER line is also connected to a 4.7K resistor (R382) and a MOSFET (Q29, DTC144EU) through a resistor R383 (4.7K ohms). The MOSFET Q29 is connected to the CCD_POWERON (28) line. The schematic also shows connections for USBP3+ LCD, USBP3+ LED, and USBP3- LED to various pins on the module.

The schematic diagram illustrates the LED driver circuit for the LED module. It features a power input section with a fuse F2 (LITTLE-0603-2A-32V) and a voltage divider network (R9, R10) for LCD VADJ. The main power path includes a diode D1 (LED@B140) and a current sense resistor R8 (LED@35.7K_4). The LED module is represented by a block with pins for VCC, GND, COMB, FFW, Vswell, IN1, IN2, IN3, and PAD. The circuit is powered by a 10U16V_6 battery and includes various capacitors (C1, C2, C3, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C110, C111, C112, C113, C114, C115, C116, C117, C118, C119, C120, C121, C122, C123, C124, C125, C126, C127, C128, C129, C130, C131, C132, C133, C134, C135, C136, C137, C138, C139, C140, C141, C142, C143, C144, C145, C146, C147, C148, C149, C150, C151, C152, C153, C154, C155, C156, C157, C158, C159, C160, C161, C162, C163, C164, C165, C166, C167, C168, C169, C170, C171, C172, C173, C174, C175, C176, C177, C178, C179, C180, C181, C182, C183, C184, C185, C186, C187, C188, C189, C190, C191, C192, C193, C194, C195, C196, C197, C198, C199, C200, C201, C202, C203, C204, C205, C206, C207, C208, C209, C210, C211, C212, C213, C214, C215, C216, C217, C218, C219, C220, C221, C222, C223, C224, C225, C226, C227, C228, C229, C230, C231, C232, C233, C234, C235, C236, C237, C238, C239, C240, C241, C242, C243, C244, C245, C246, C247, C248, C249, C250, C251, C252, C253, C254, C255, C256, C257, C258, C259, C260, C261, C262, C263, C264, C265, C266, C267, C268, C269, C270, C271, C272, C273, C274, C275, C276, C277, C278, C279, C280, C281, C282, C283, C284, C285, C286, C287, C288, C289, C290, C291, C292, C293, C294, C295, C296, C297, C298, C299, C300, C301, C302, C303, C304, C305, C306, C307, C308, C309, C310, C311, C312, C313, C314, C315, C316, C317, C318, C319, C320, C321, C322, C323, C324, C325, C326, C327, C328, C329, C330, C331, C332, C333, C334, C335, C336, C337, C338, C339, C340, C341, C342, C343, C344, C345, C346, C347, C348, C349, C350, C351, C352, C353, C354, C355, C356, C357, C358, C359, C360, C361, C362, C363, C364, C365, C366, C367, C368, C369, C370, C371, C372, C373, C374, C375, C376, C377, C378, C379, C380, C381, C382, C383, C384, C385, C386, C387, C388, C389, C390, C391, C392, C393, C394, C395, C396, C397, C398, C399, C400, C401, C402, C403, C404, C405, C406, C407, C408, C409, C410, C411, C412, C413, C414, C415, C416, C417, C418, C419, C420, C421, C422, C423, C424, C425, C426, C427, C428, C429, C430, C431, C432, C433, C434, C435, C436, C437, C438, C439, C440, C441, C442, C443, C444, C445, C446, C447, C448, C449, C450, C451, C452, C453, C454, C455, C456, C457, C458, C459, C460, C461, C462, C463, C464, C465, C466, C467, C468, C469, C470, C471, C472, C473, C474, C475, C476, C477, C478, C479, C480, C481, C482, C483, C484, C485, C486, C487, C488, C489, C490, C491, C492, C493, C494, C495, C496, C497, C498, C499, C500, C501, C502, C503, C504, C505, C506, C507, C508, C509, C510, C511, C512, C513, C514, C515, C516, C517, C518, C519, C520, C521, C522, C523, C524, C525, C526, C527, C528, C529, C530, C531, C532, C533, C534, C535, C536, C537, C538, C539, C540, C541, C542, C543, C544, C545, C546, C547, C548, C549, C550, C551, C552, C553, C554, C555, C556, C557, C558, C559, C560, C561, C562, C563, C564, C565, C566, C567, C568, C569, C570, C571, C572, C573, C574, C575, C576, C577, C578, C579, C580, C581, C582, C583, C584, C585, C586, C587, C588, C589, C590, C591, C592, C593, C594, C595, C596, C597, C598, C599, C600, C601, C602, C603, C604, C605, C606, C607, C608, C609, C610, C611, C612, C613, C614, C615, C616, C617, C618, C619, C620, C621, C622, C623, C624, C625, C626, C627, C628, C629, C630, C631, C632, C633, C634, C635, C636, C637, C638, C639, C640, C641, C642, C643, C644, C645, C646, C647, C648, C649, C650, C651, C652, C653, C654, C655, C656, C657, C658, C659, C660, C661, C662, C663, C664, C665, C666, C667, C668, C669, C670, C671, C672, C673, C674, C675, C676, C677, C678, C679, C680, C681, C682, C683, C684, C685, C686, C687, C688, C689, C690, C691, C692, C693, C694, C695, C696, C697, C698, C699, C700, C701, C702, C703, C704, C705, C706, C707, C708, C709, C710, C711, C712, C713, C714, C715, C716, C717, C718, C719, C720, C721, C722, C723, C724, C725, C726, C727, C728, C729, C730, C731, C732, C733, C734, C735, C736, C737, C738, C739, C740, C741, C742, C743, C744, C745, C746, C747, C748, C749, C750, C751, C752, C753, C754, C755, C756, C757, C758, C759, C760, C761, C762, C763, C764, C765, C766, C767, C768, C769, C770, C771, C772, C773, C774, C775, C776, C777, C778, C779, C780, C781, C782, C783, C784, C785, C786, C787, C788, C789, C790, C791, C792, C793, C794, C795, C796, C797, C798, C799, C800, C801, C802, C803, C804, C805, C806, C807, C808, C809, C810, C

[illegible][illegible][illegible]

INVC0 : 0.67A for E/E Reference only

VINO

R26

LCD@0.8

INVCC0

C27

C22

C17

LCD@10u/25V_1210

LCD@1000p/50V_4

LCD@0.1u/50V_6

INT MIC

CNR

2

1

ADD0GND

MIC_DATA

INT_MIC

(29) INT_MIC

R27

0.4

(6) INT_LVDS_PWM

(29) CONTRAST

R24

0.4

R23

0.4

+3V0

ADD0GND

LCD_POWER

ADD0GND

MIC_DATA

DISPON

LCD_VA0I

LCD_ENDDCLK

LCD_ENDDATA

USBP3+ LCD

USBP3- LCD

C364

C365

LCD@1000p/50V_6

LCD@1000p/50V_6

CNS

1

2

3

4

5

6

7

8

9

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11

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14

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OLCDVCC

LCD_TXCLKOUT+

LCD_TXCLKOUT-

LCD_TXL0UT0+

LCD_TXL0UT0-

LCD_TXL0UT1+

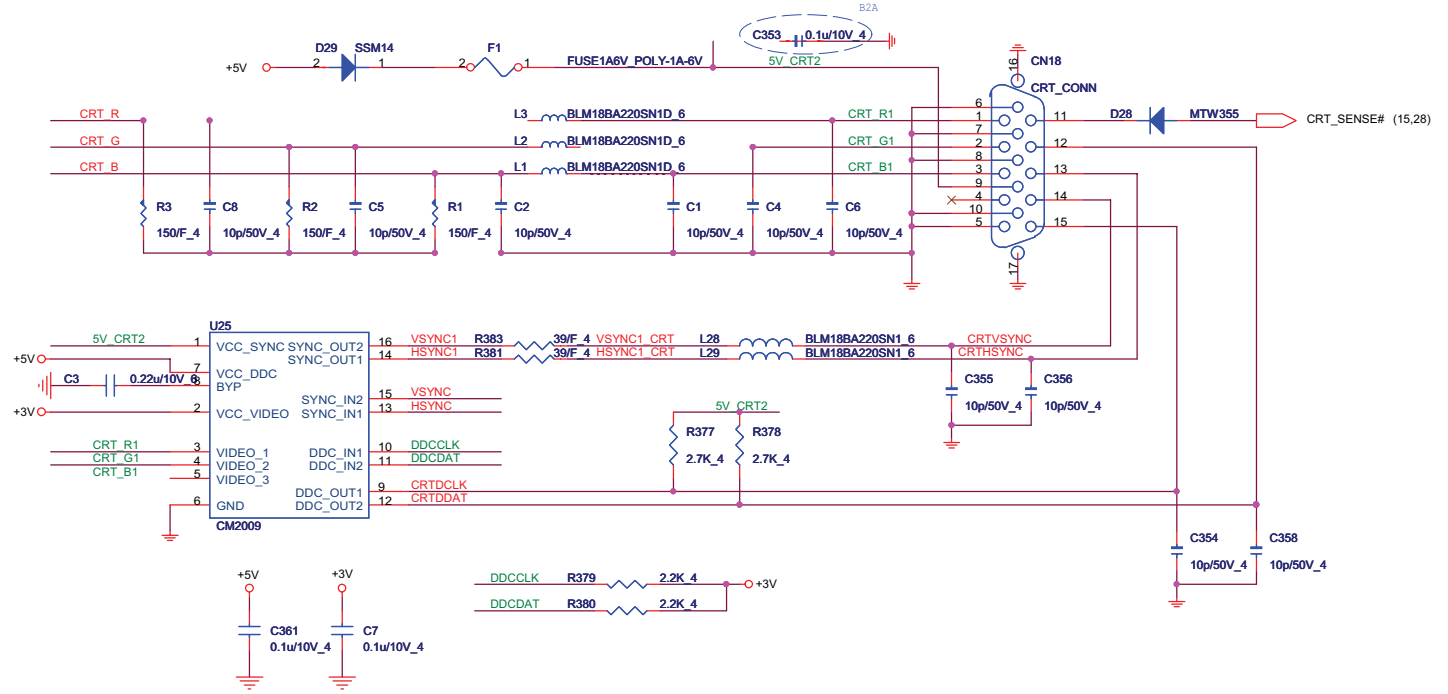
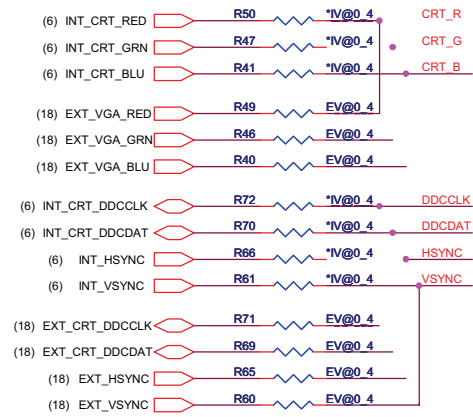
LCD_TXL0UT1-

LCD_TXL0UT2+

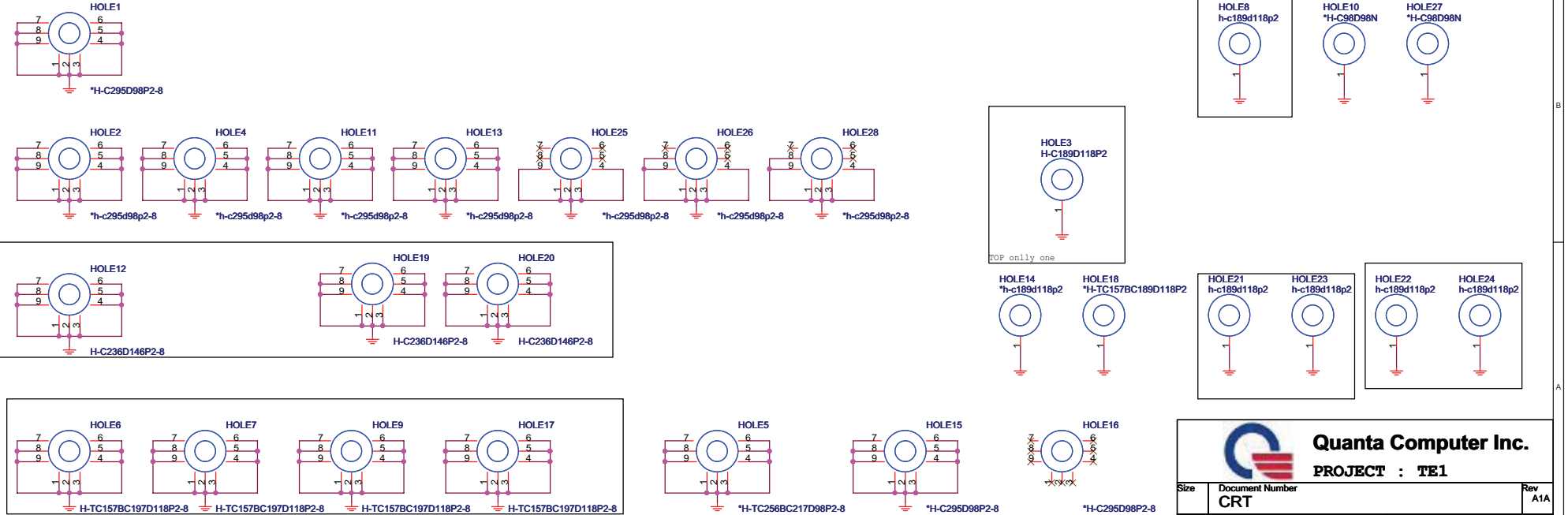
LCD_TXL0UT2-

LCD@CD_PANEL

CRT



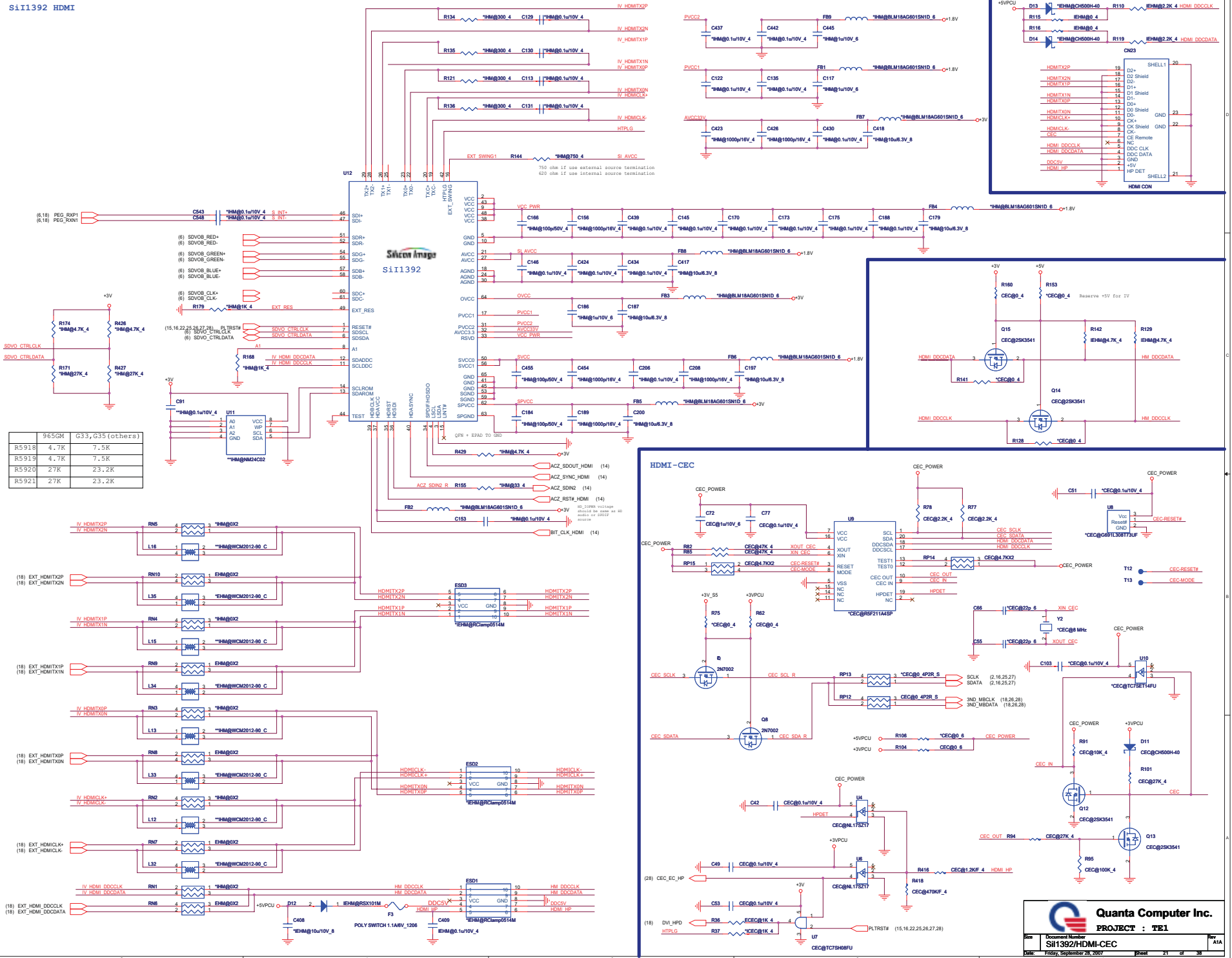
HOLE



Quanta Computer Inc.
PROJECT : TE1

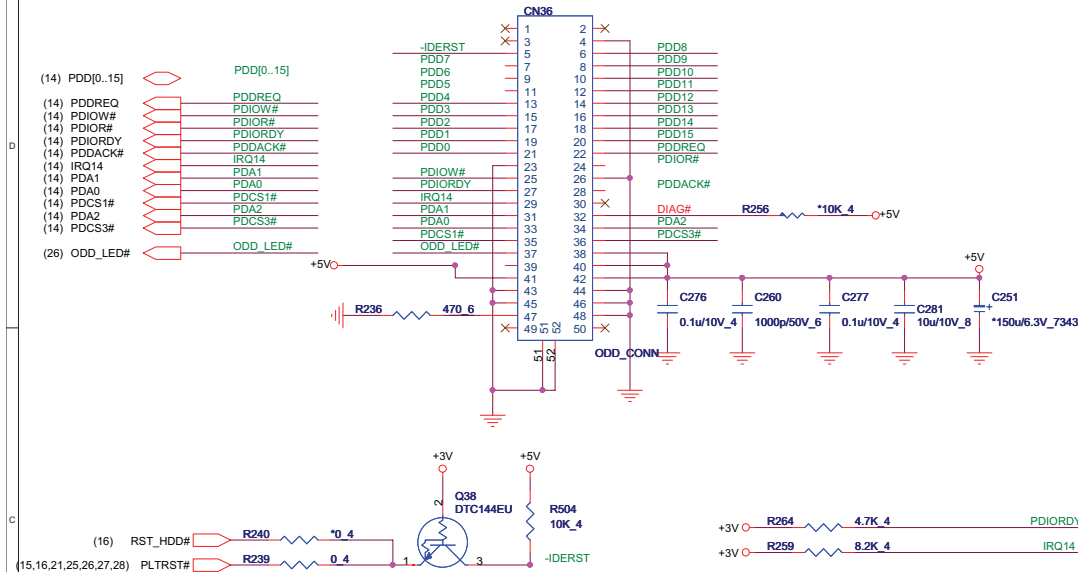
Size	Document Number	Rev
CRT		A1A
Date:	Saturday, September 29, 2007	Sheet 20 of 38

	965GM	G33, G35 (others)
R5918	4.7K	7.5K
R5919	4.7K	7.5K
R5920	27K	23.2K
R5921	27K	23.2K



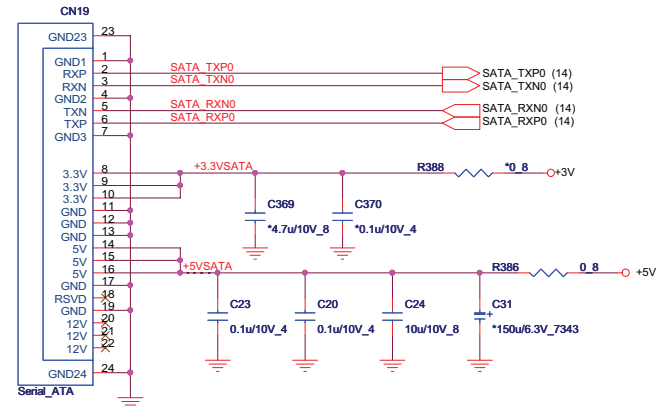
ODD

5VHDD (RUN) : 1A

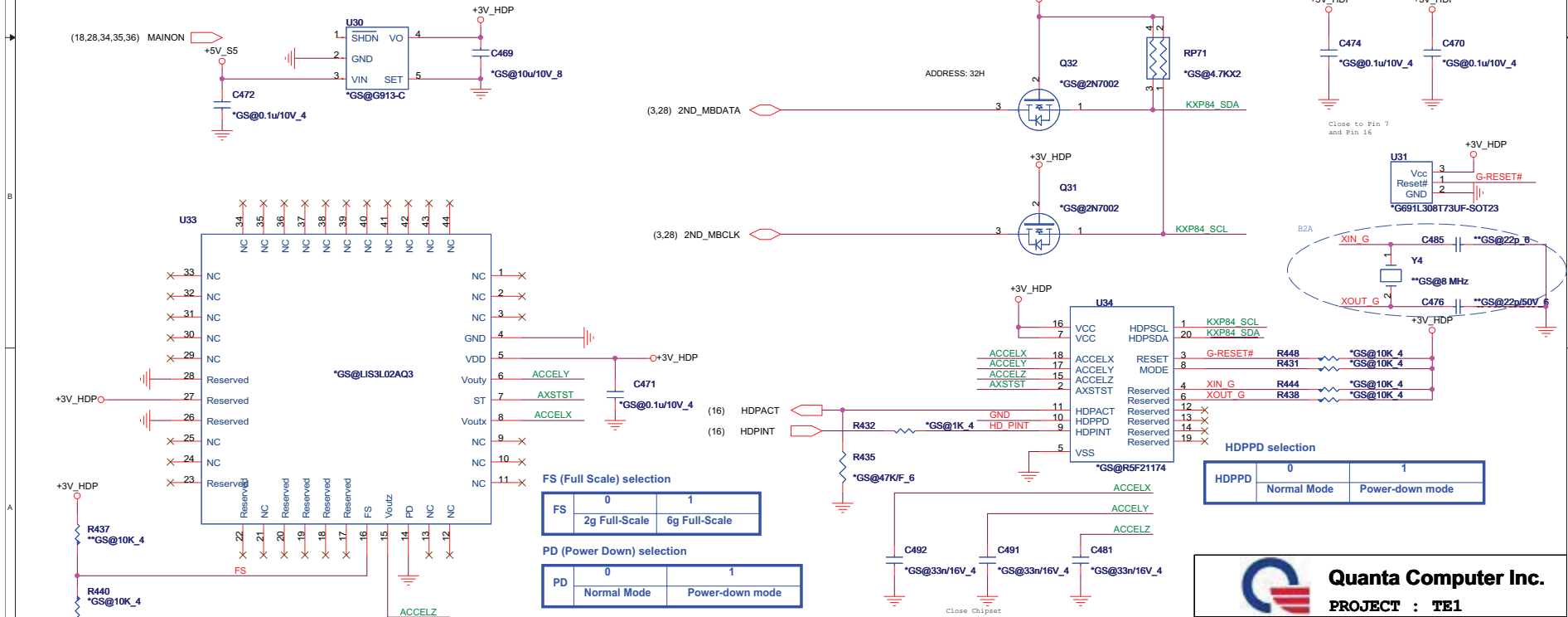


SATA HDD

5VHDD (RUN) : 1.8A



G SENSOR



FS (Full Scale) selection

FS	0	1
	2g Full-Scale	6g Full-Scale

PD (Power Down) selection

PD	0	1
	Normal Mode	Power-down mode

HDPPD selection

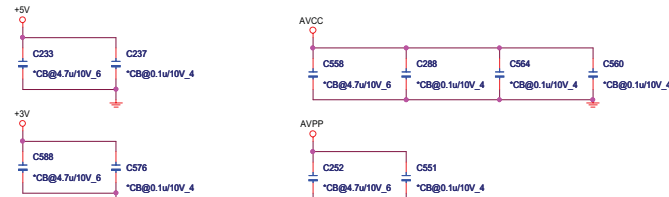
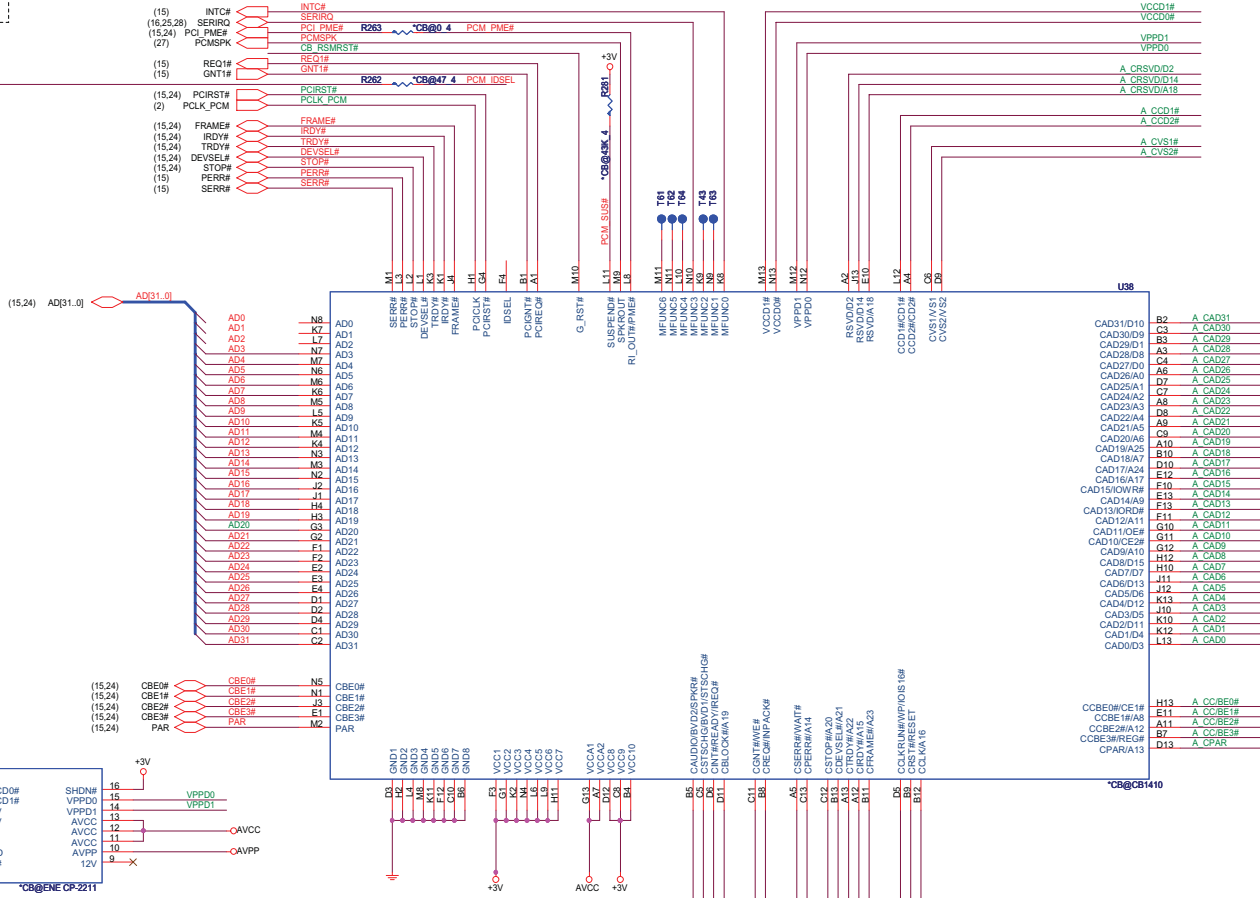
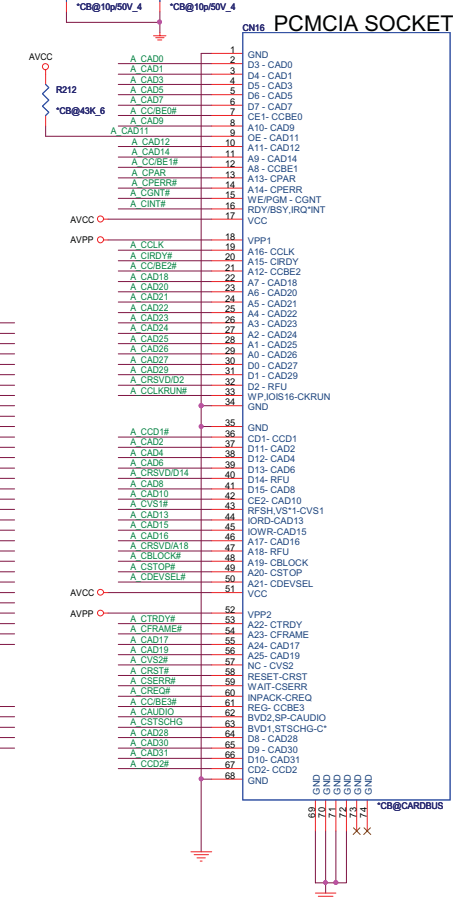
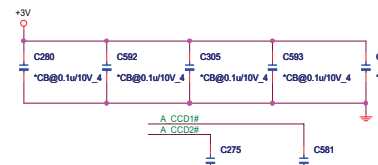
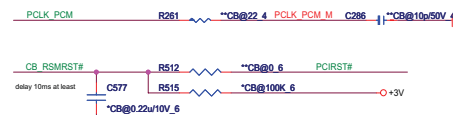
HDPPD	0	1
	Normal Mode	Power-down mode



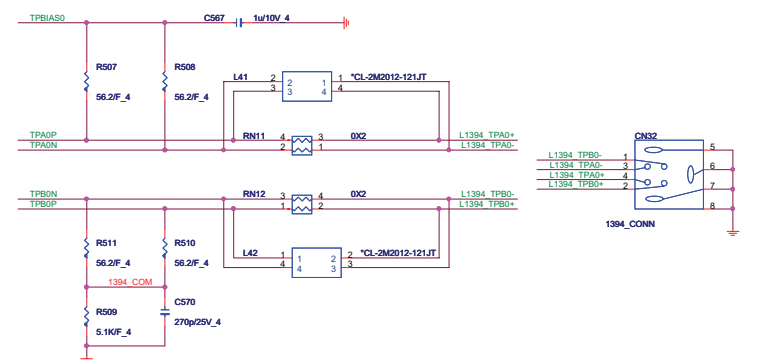
Quanta Computer Inc.

PROJECT : TE1

Size	Document Number	Rev
	SATA/PATA/G-SENSOR	A1A
Date	Sunday, September 30, 2007	Sheet 22 of 38

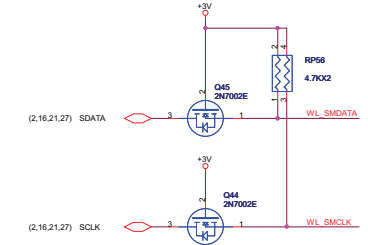
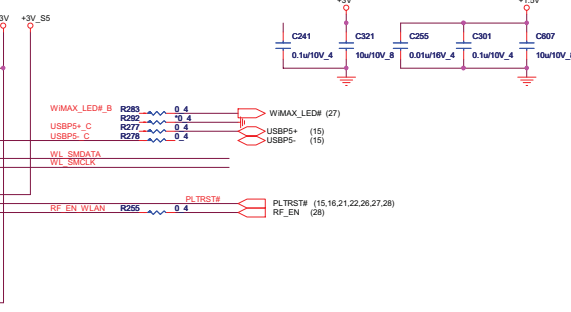
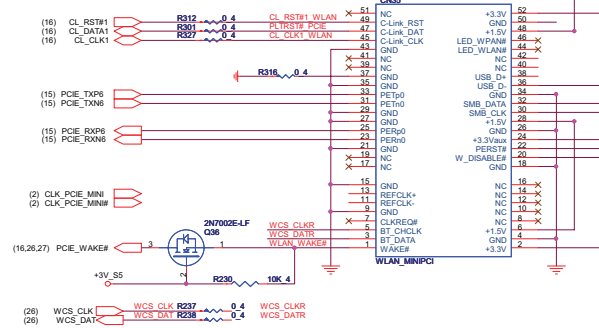
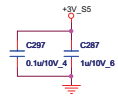


ID Select : AD17
Interrupt Pin : INTA#
Request Indicate : REQ0#
Grant Indicate : GNT0#



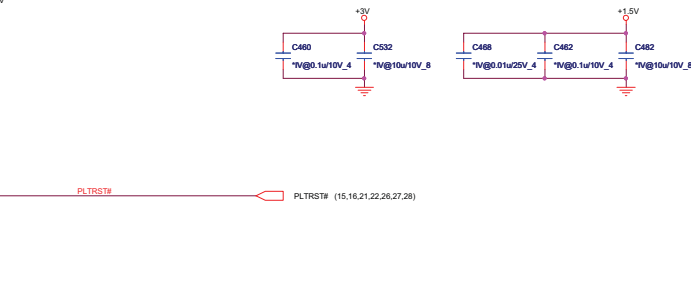
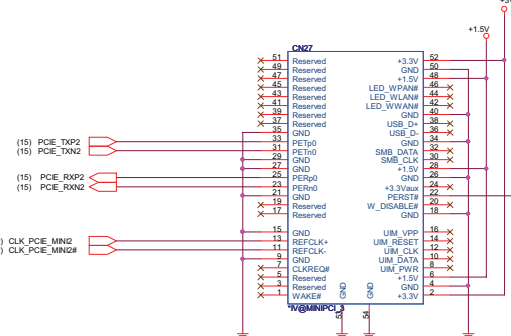
MINI Card 1 U&D 5.6H_WLAN

1.5V_VCC (R08) 0.5A
3.3V_VCC (R08) 1A
3.3V_AUX (R08) 0.005A



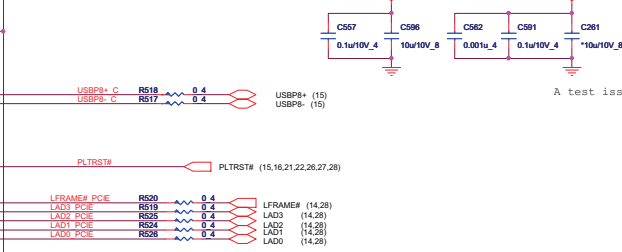
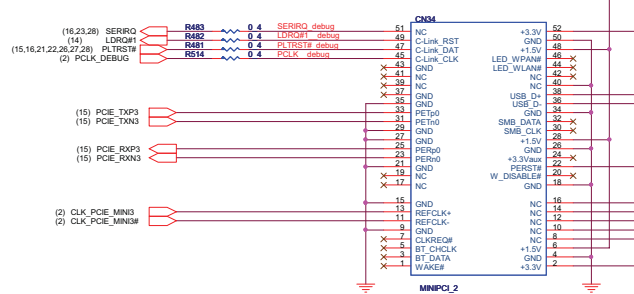
MINI Card 3 U 9H_HD-DVD

1.5V_VCC (R08) 0.5A
3.3V_VCC (R08) 1A



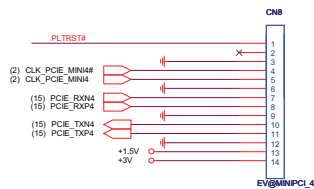
MINI Card 2 U 5.6H_TV/ROBSON D 7.5H_HD-DVD

1.5V_VCC (R08) 0.5A
3.3V_VCC (R08) 1A



A test issue : take out C261

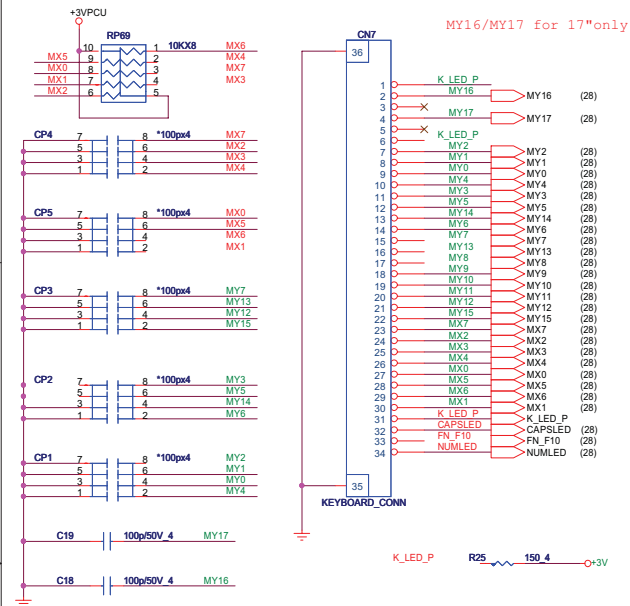
MINI Card 4-D/Robson



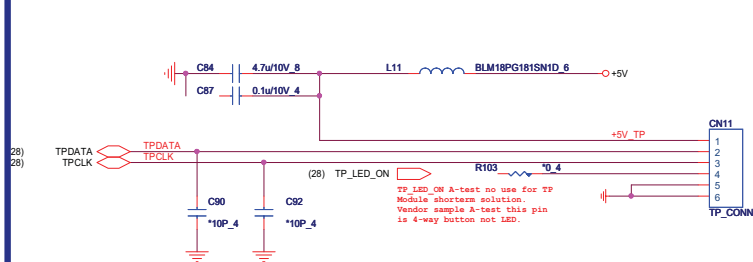
Remark1:TV/Robson or HD-DVD/Robson or
TV/HD-DVD for DRA 500
Remark2:TV is just for DRA (13*)

	UMA	Discrete
1	WLAN	WLAN
2	TV or Robson	HD-DVD
3	HD-DVD or Robson	N.C
4	N.C	Robson

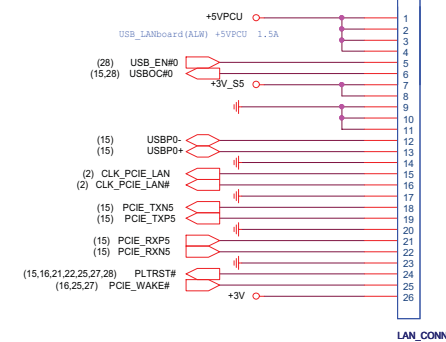
INT KeyBoard



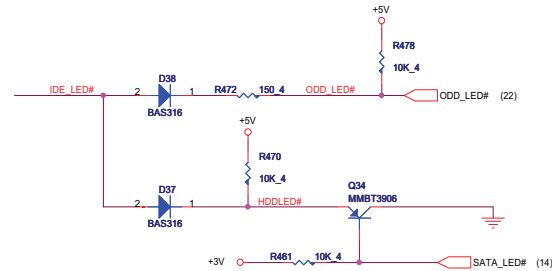
TP Board



RJ45/USB board



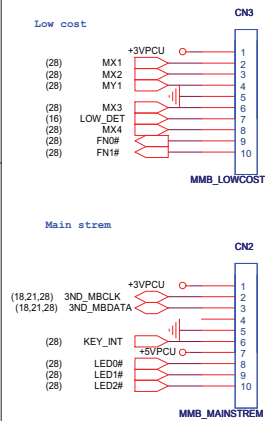
LED Board



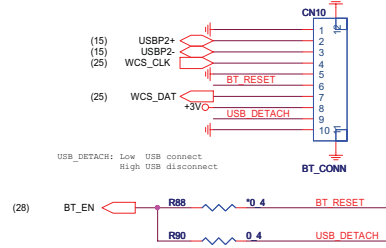
Pin connection diagram for CN13:

Pin	Signal
1	GND
2	+5VPCU
3	+5V
4	BATLED1#
5	BATLED0#
6	PWLED#
7	SUSLED_EC
8	IDE_LED#
9	TP_XD_LED
10	ACIN
11	
12	

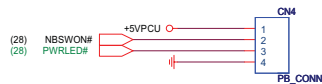
MMB



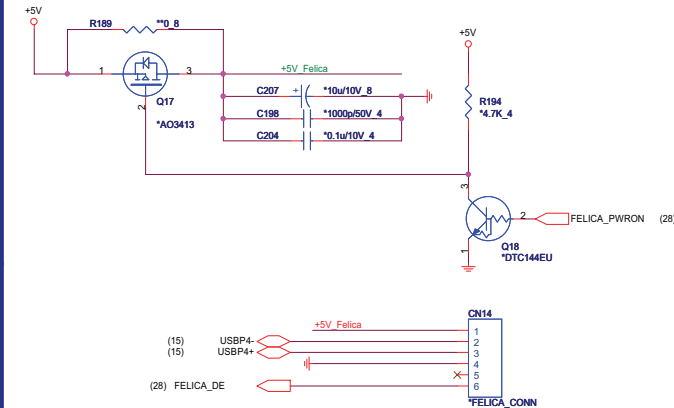
Bluetooth Module Conn



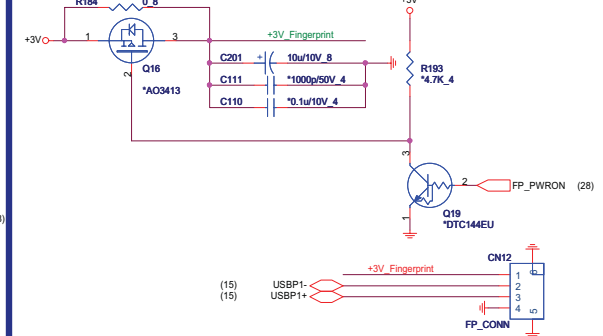
Power board



Felica

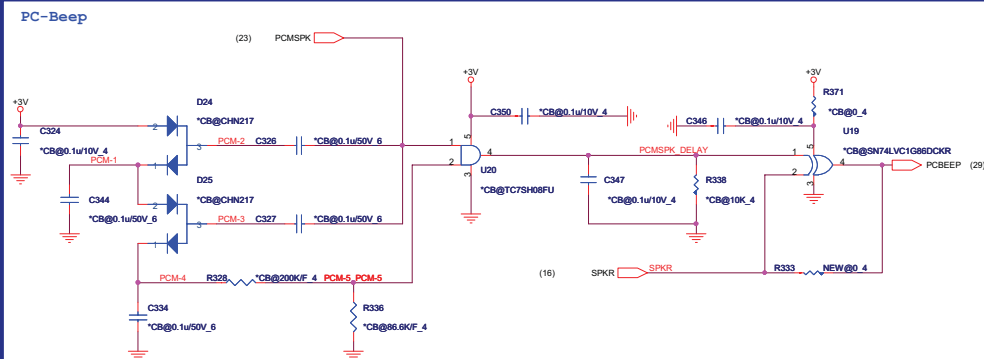
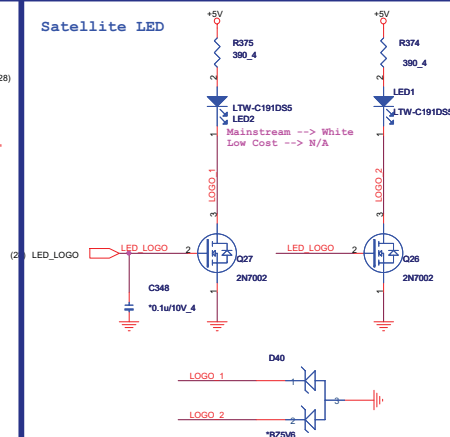
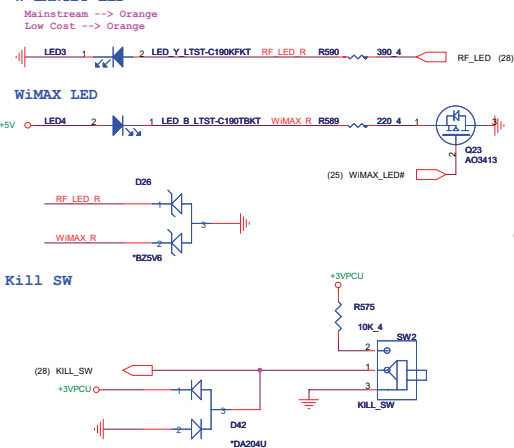
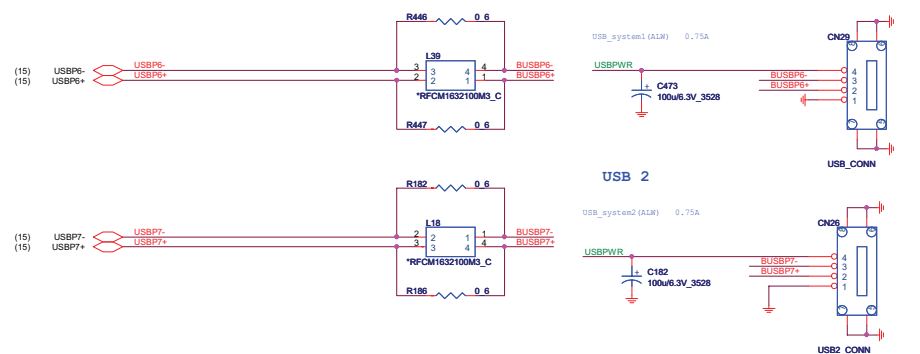
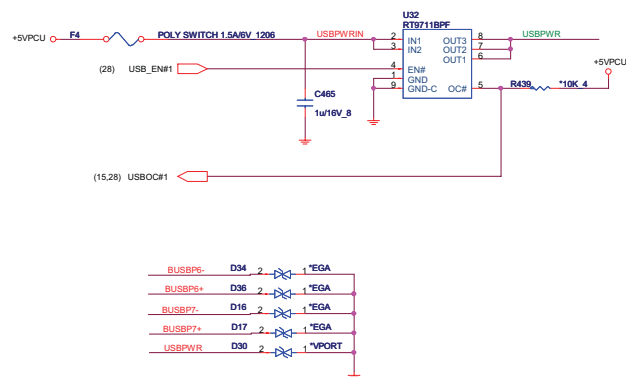
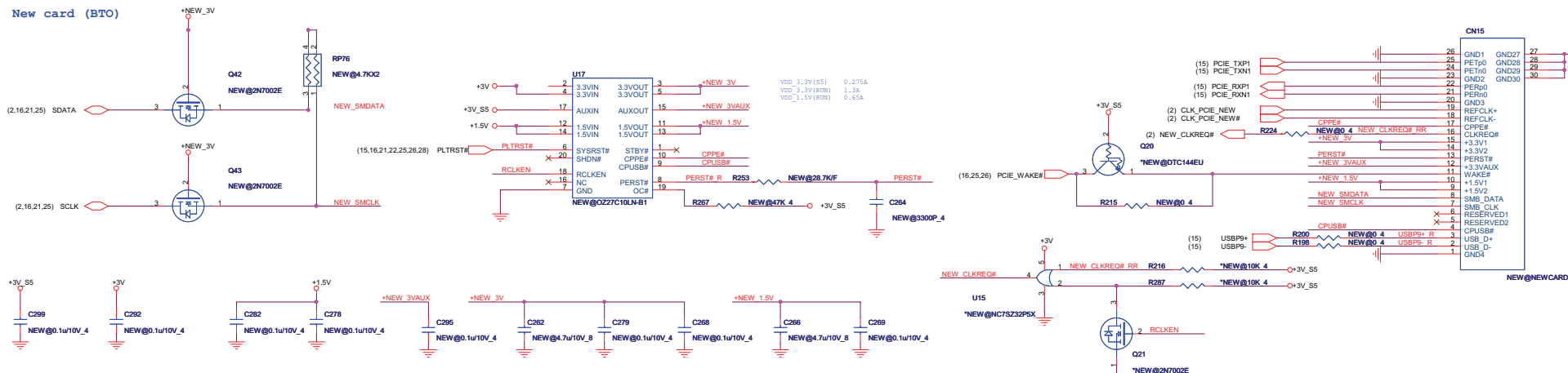


FP Board

**Quanta Computer Inc.**

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Signal	Pin	Termination
MBCLK	R395	4.7K 4
MBDATA	R394	4.7K 4
2ND MBCLK	R393	4.7K 4
2ND MBDATA	R392	4.7K 4
FN0#	R53	4.7K 4
FN1#	R52	4.7K 4
3ND MBCLK	R57	4.7K 4
3ND MBDATA	R56	4.7K 4
CRT SENSE#	R396	4.7K 4

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0	BADDR0	R56	10K	4
BADDR1	LED1#	R385	*10K	4
SHBM	RF_EN	R396	10K	4

Disabled ('1') if using FWH device on LPC.
Enabled ('Y') if using SPI flash for both system BIOS and EC firmware

FLASH

The diagram shows the FLASH memory section of the W25X80VSSG. The chip is connected to the SPI interface as follows:

- SPI SDI (pin 2):** Connected to R401 (33k) to +3VPU.
- SPI SDO (pin 5):** Connected to R403 (33k) to +3VPU.
- SPI SCK (pin 6):** Connected to R405 (33k) to +3VPU.
- SPI CS0# (pin 4):** Connected to R400 (10k) to +3VPU.

The chip is also connected to the power supply:

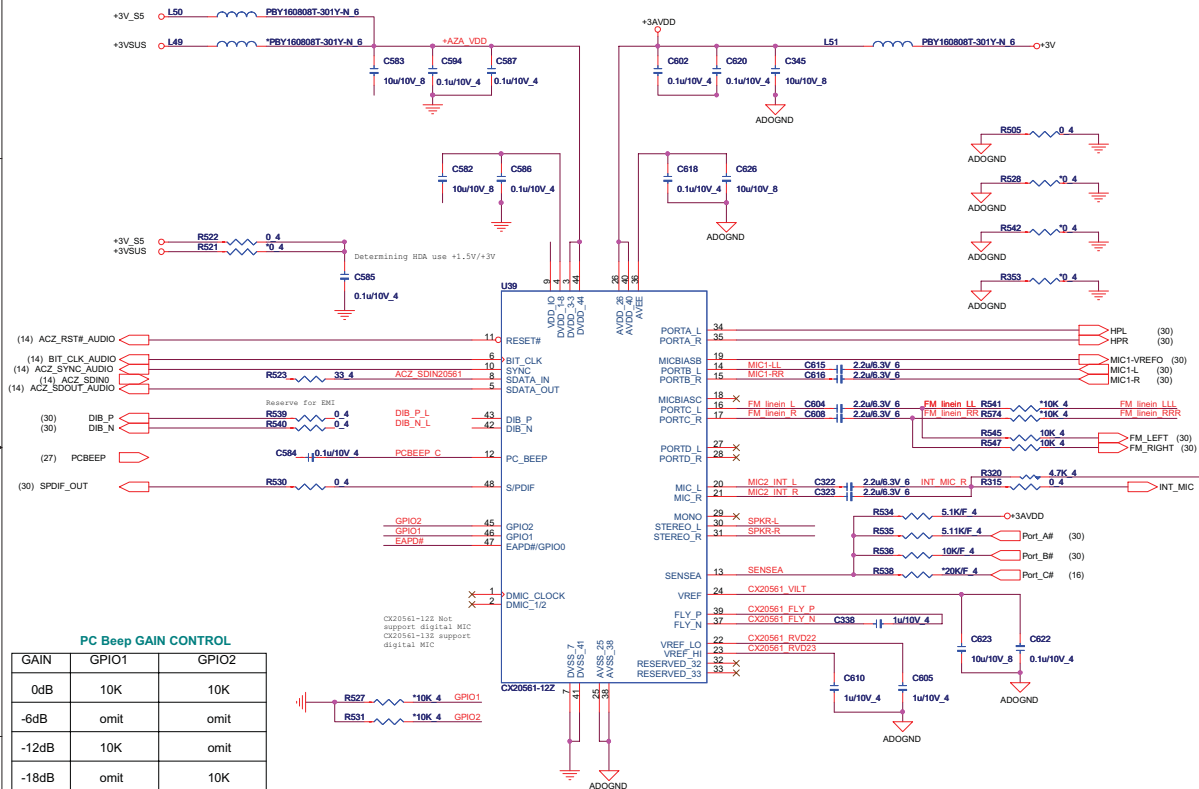
- VDD (pin 8):** Connected to +3VPU.
- HOLD (pin 7):** Connected to +3VPU.
- WP (pin 3):** Connected to +3VPU.
- VSS (pin 4):** Connected to ground.

A capacitor C396 (0.1uF/10V4) is connected between VDD and ground.

MXIC	MX25L8005M2C-15G	AKE5GFW020
Winbond	W25X80VSSIG	AKE3GFP0N0
EON	EN25F80-75HCP	AKE3GZP0Q0

The schematic diagram illustrates the power supply section of the CIR@10K board. It features a +5VPCU input line that branches into two paths. One path goes through a resistor R555 to a node labeled +5VPCU, which then connects to the VCC pin of the U42 IC. The other path goes through a resistor R586 to a node labeled CIR@0.4, which then connects to a capacitor C121. The output of C121 is labeled CIR@0.1uF10V.4. A second +5VPCU input is shown connected to a resistor R587, which then connects to the VCC pin of the U42 IC. The output of the U42 IC is labeled OUT. A 20 mliS timing component is also shown connected to the VCC pin of the U42 IC. The U42 IC is identified as CIR@R-IRM-V536-TR1.

Codec (CX20561)

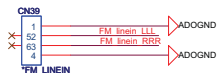


GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

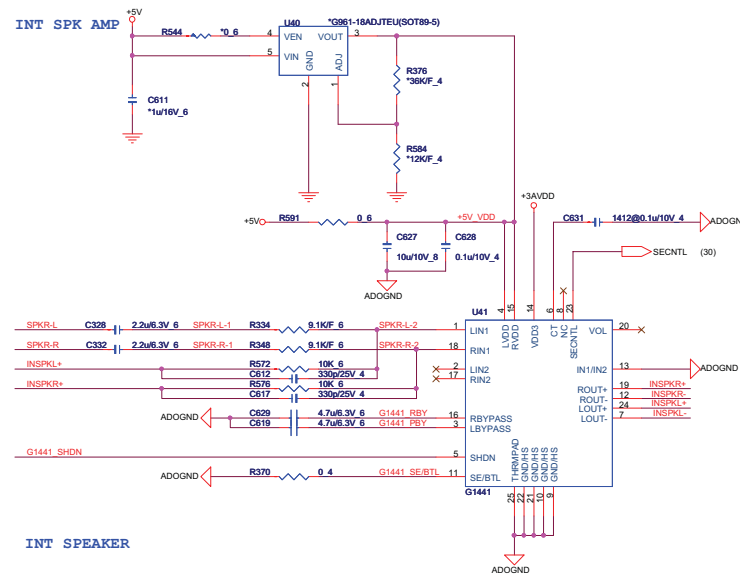
Reserve INTMIC



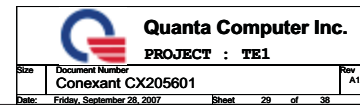
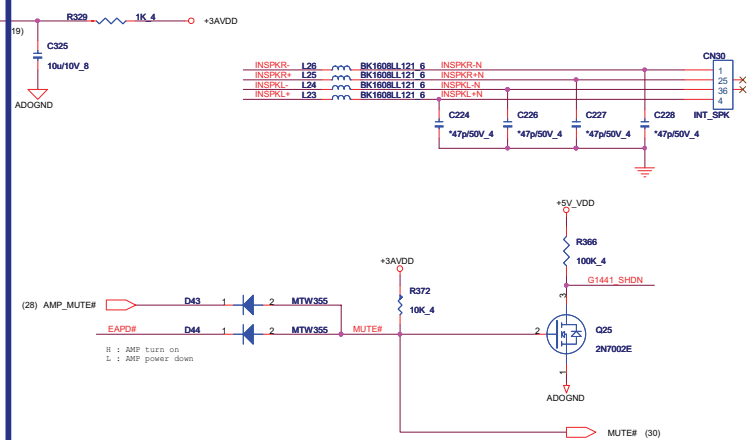
Reserve FM



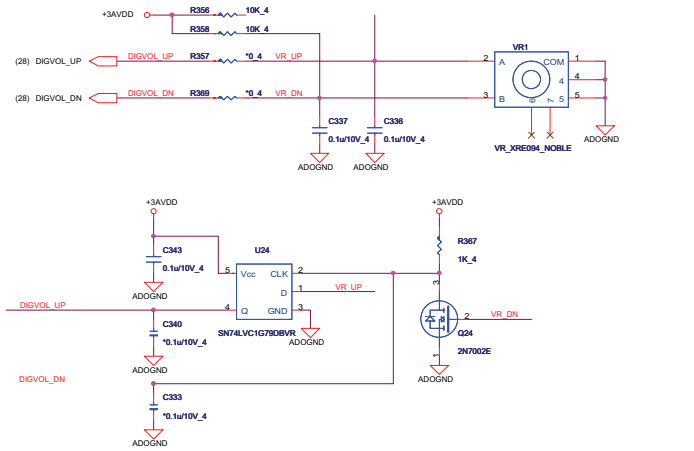
INT SPK AMP



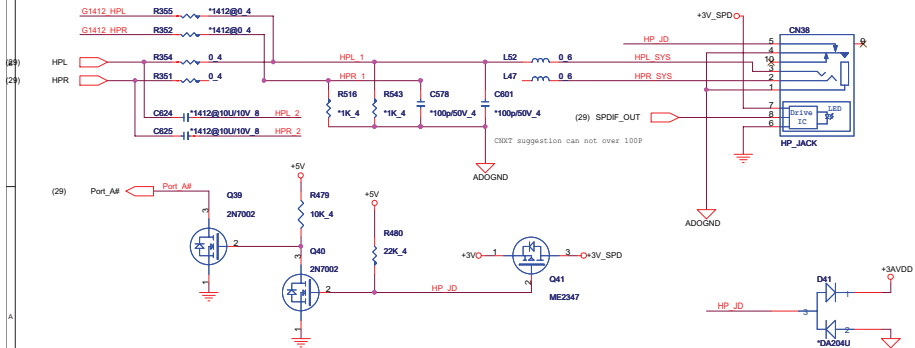
INT SPEAKER



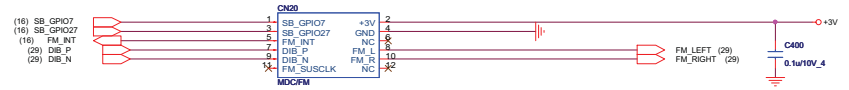
VR



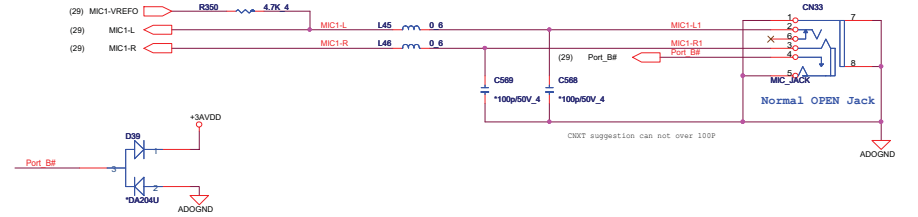
HP



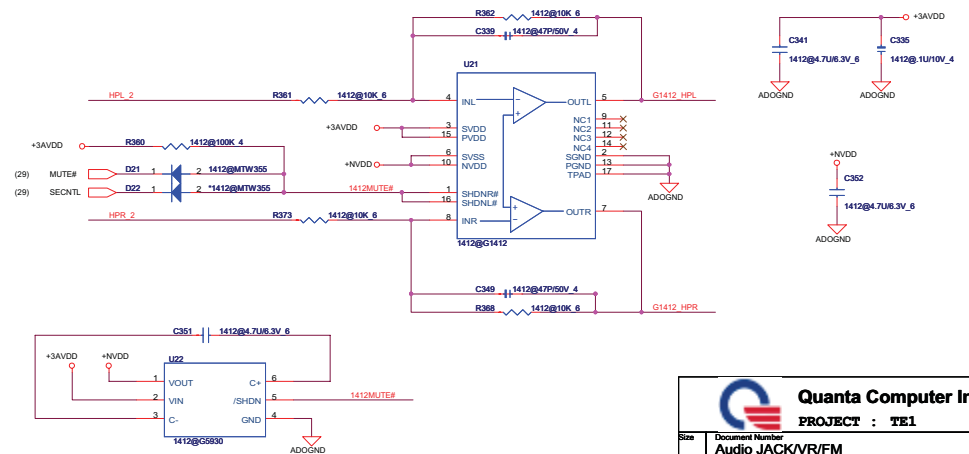
FM Tuner MDC

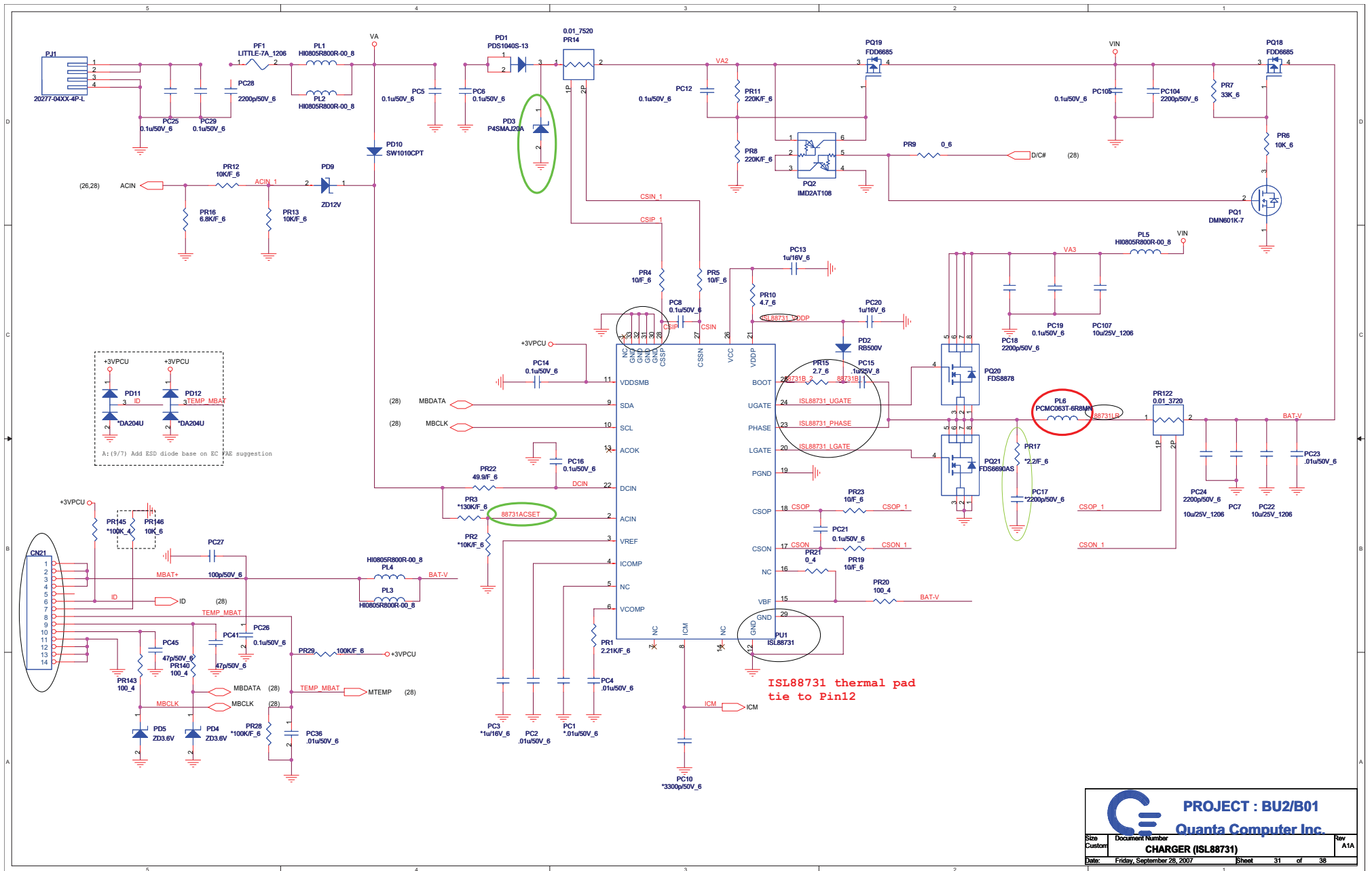


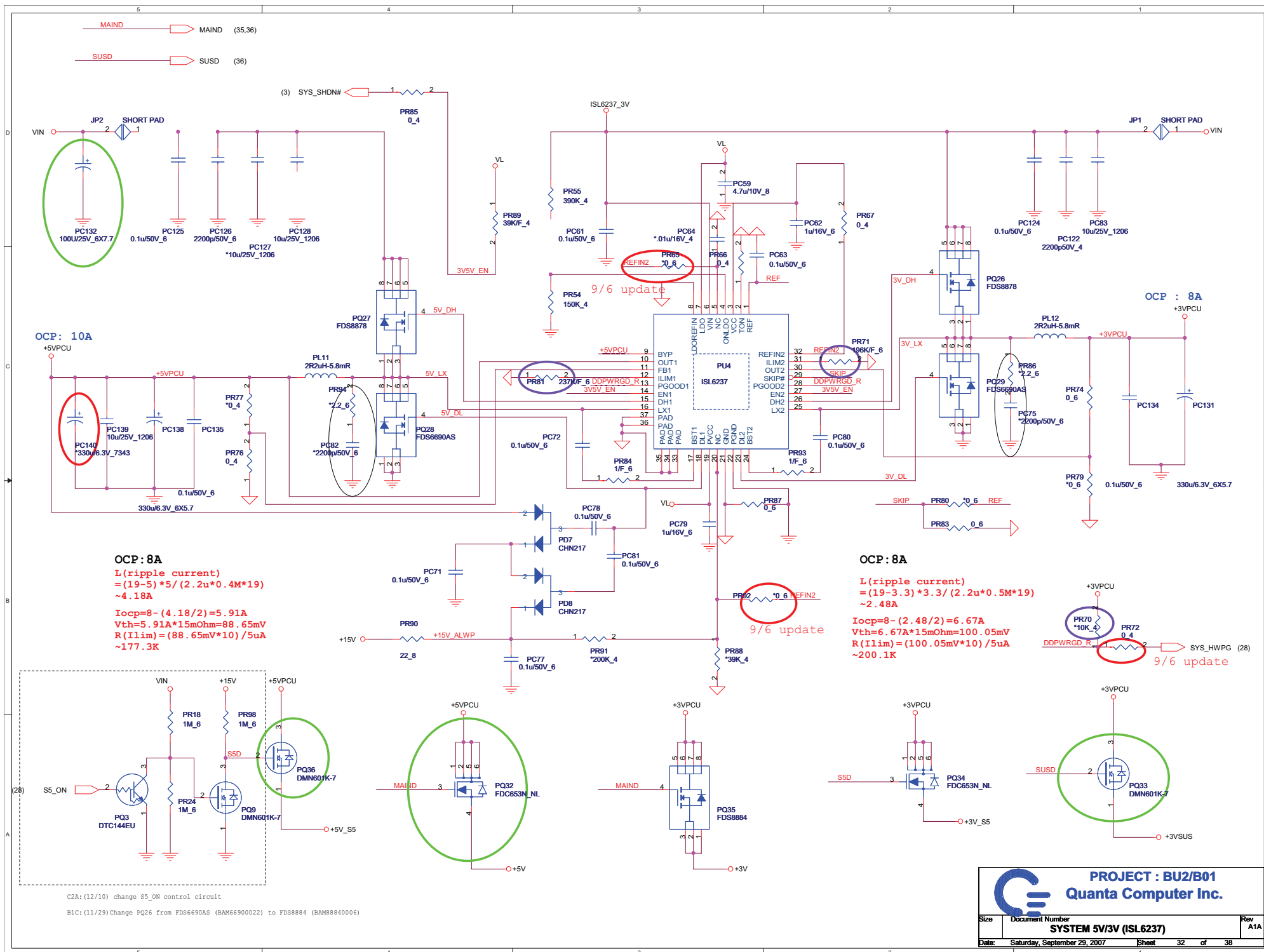
SYSTEM MIC

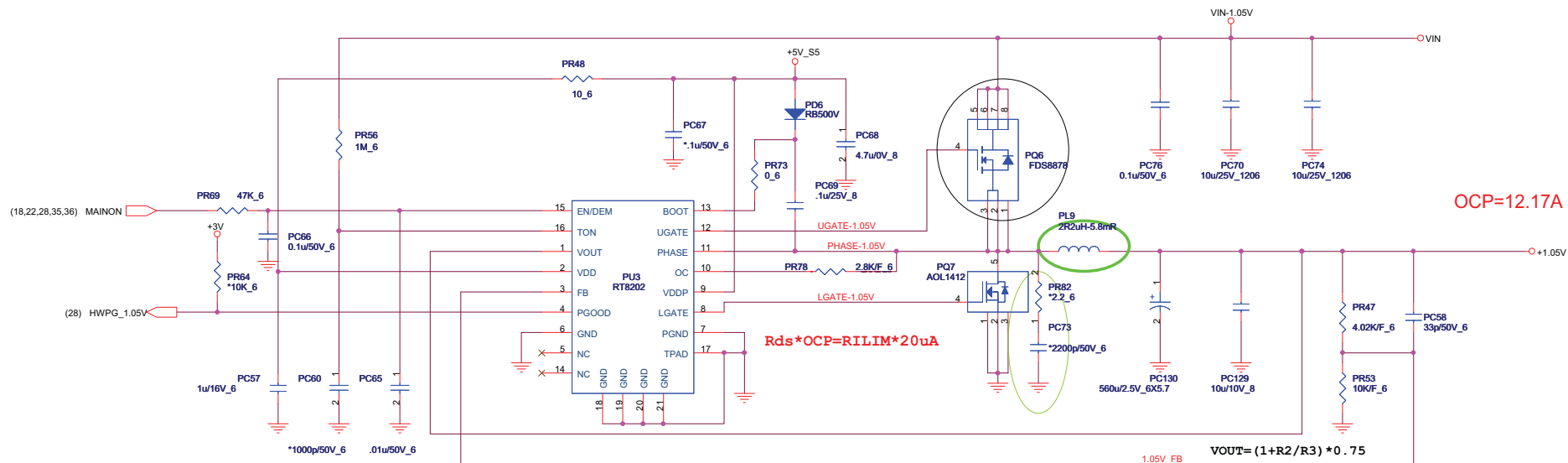


HP Amplifier









OCP=12.17A

$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$Rds * OCP = RILIM * 20uA$$

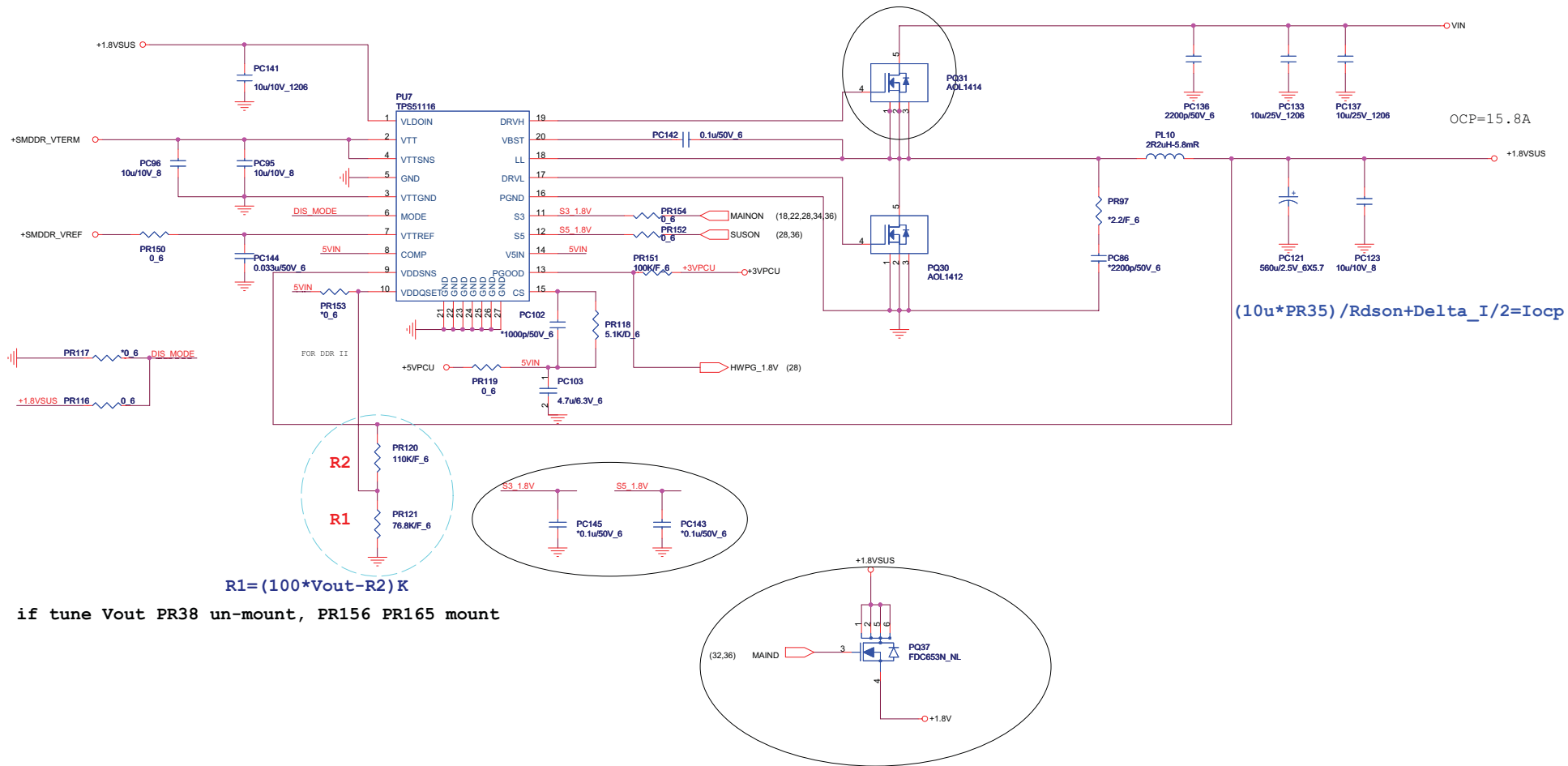
$$AO1412 \quad Rds = 4.6m\Omega$$

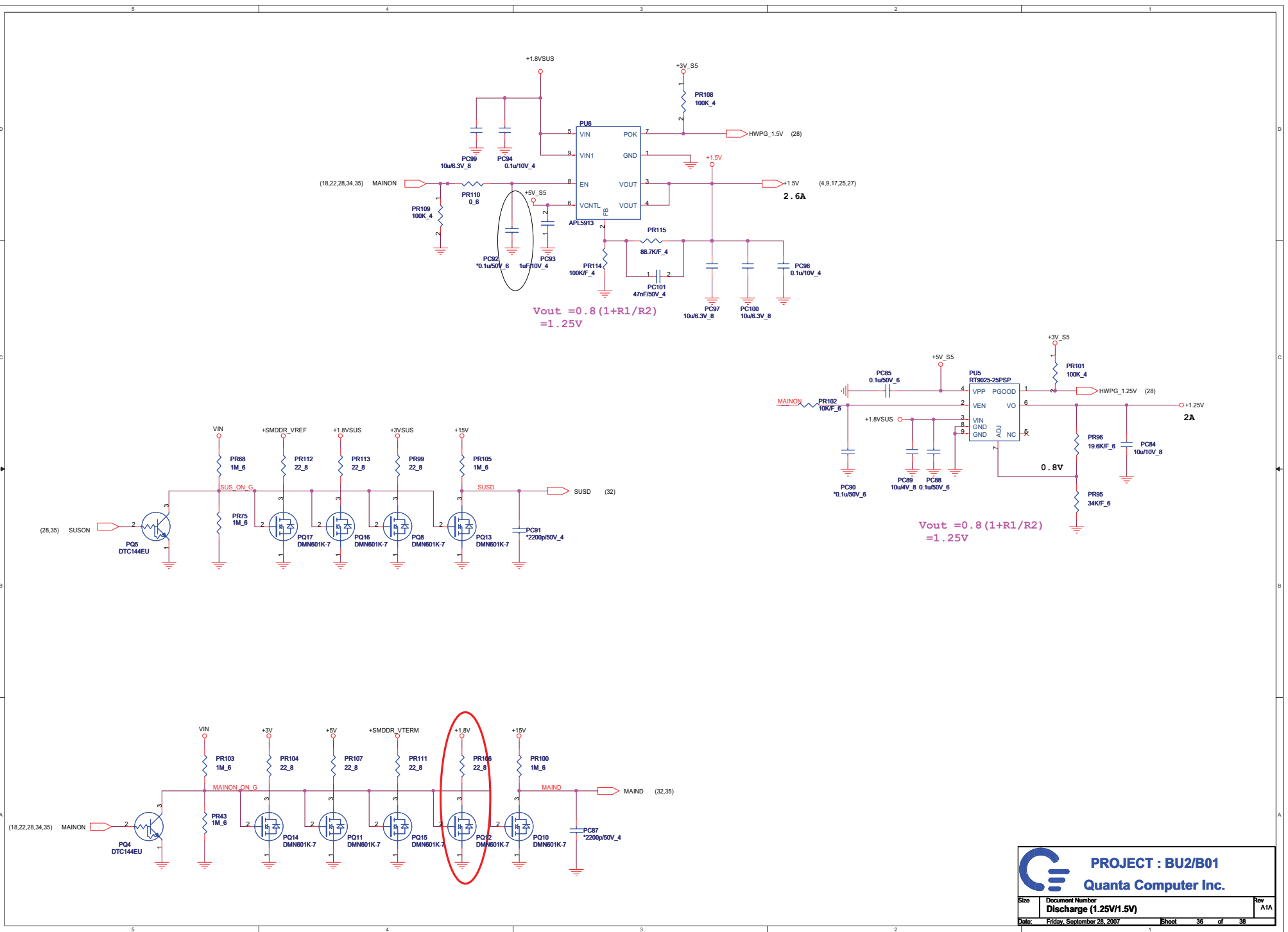
$$12.17A \quad OCP \quad --- \quad OC = 2.8K \quad (CS22803F914)$$



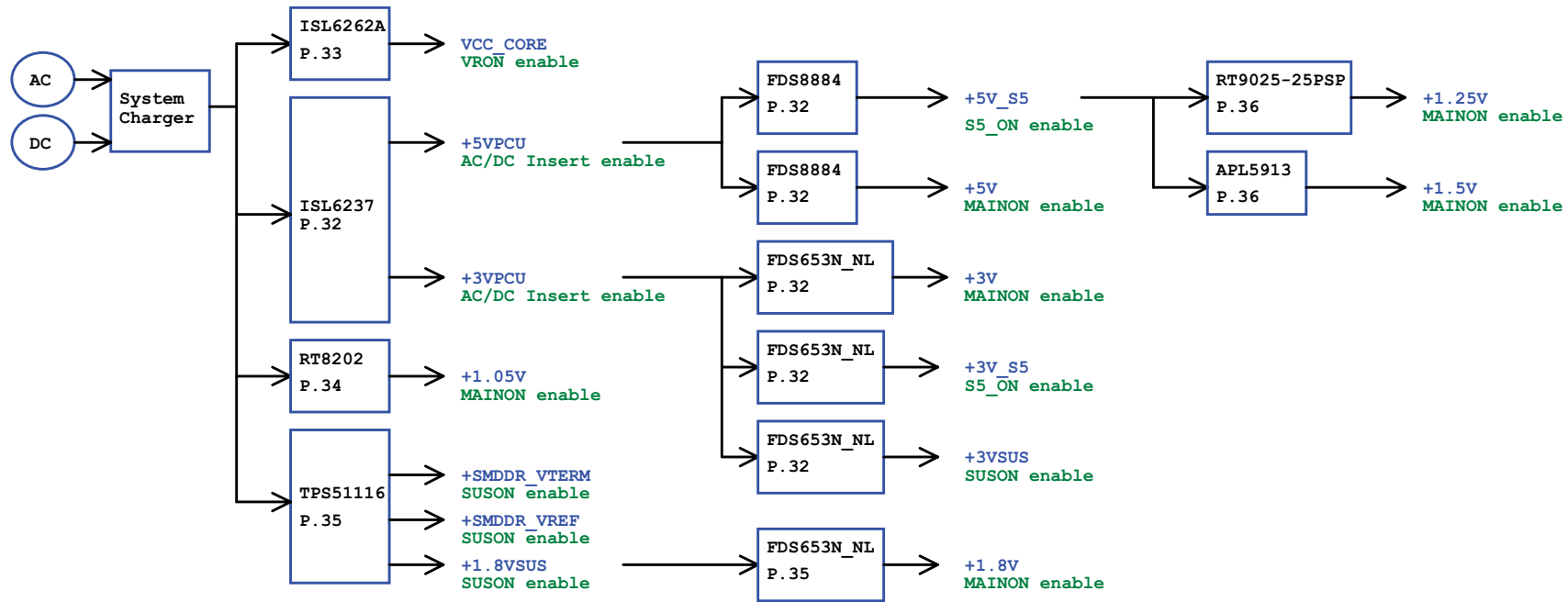
PROJECT : BU2/B01
Quanta Computer Inc.

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Power Tree Table



Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+1.8VSUS	GMCH, DDR
+SMDDR_VREF	GMCH, DDR
+SMDDR_VTERM	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T), Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	HDMI, Cardreader (OZ129T)
+1.25V	CLK, GMCH, ICH8M