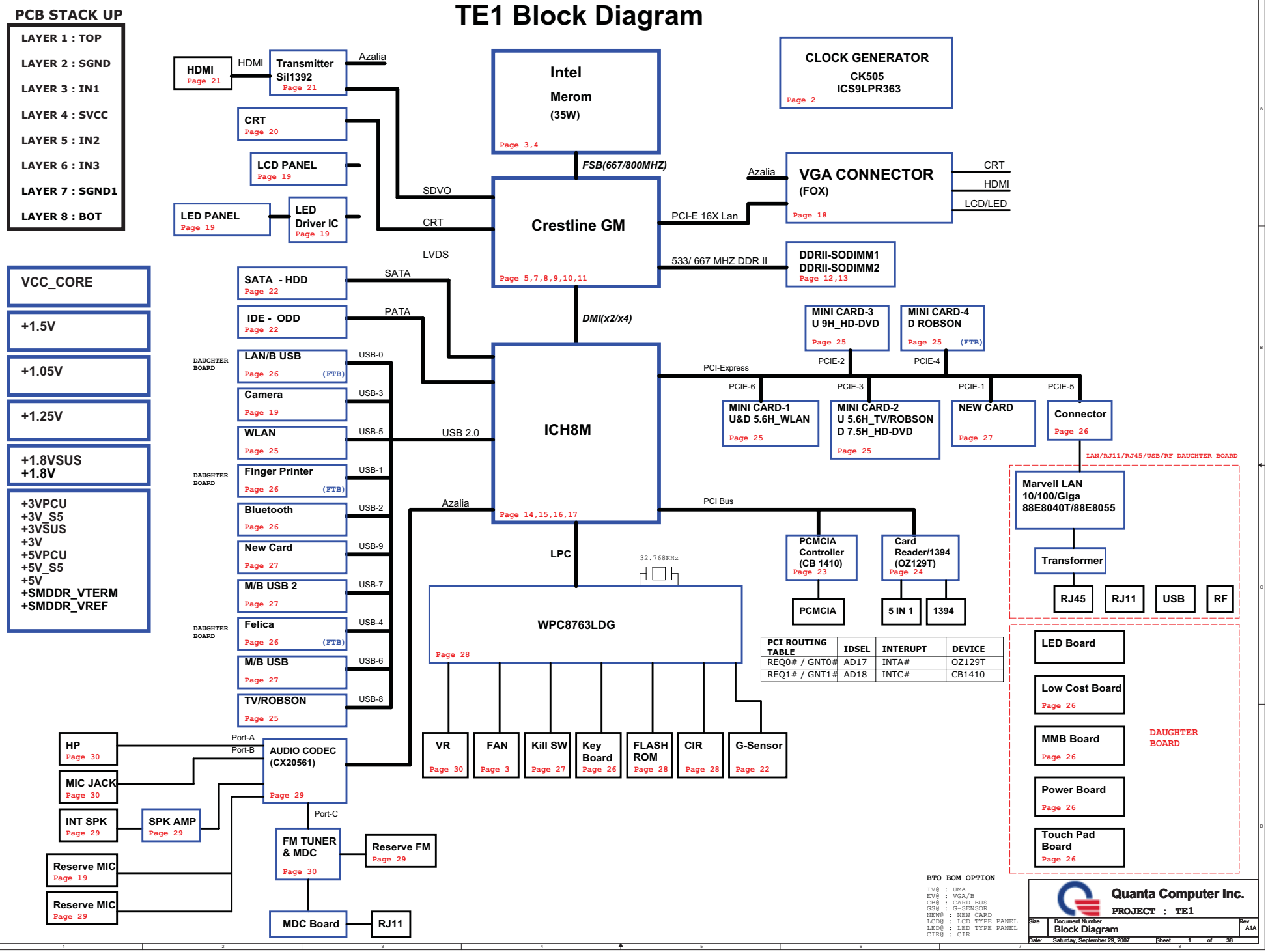
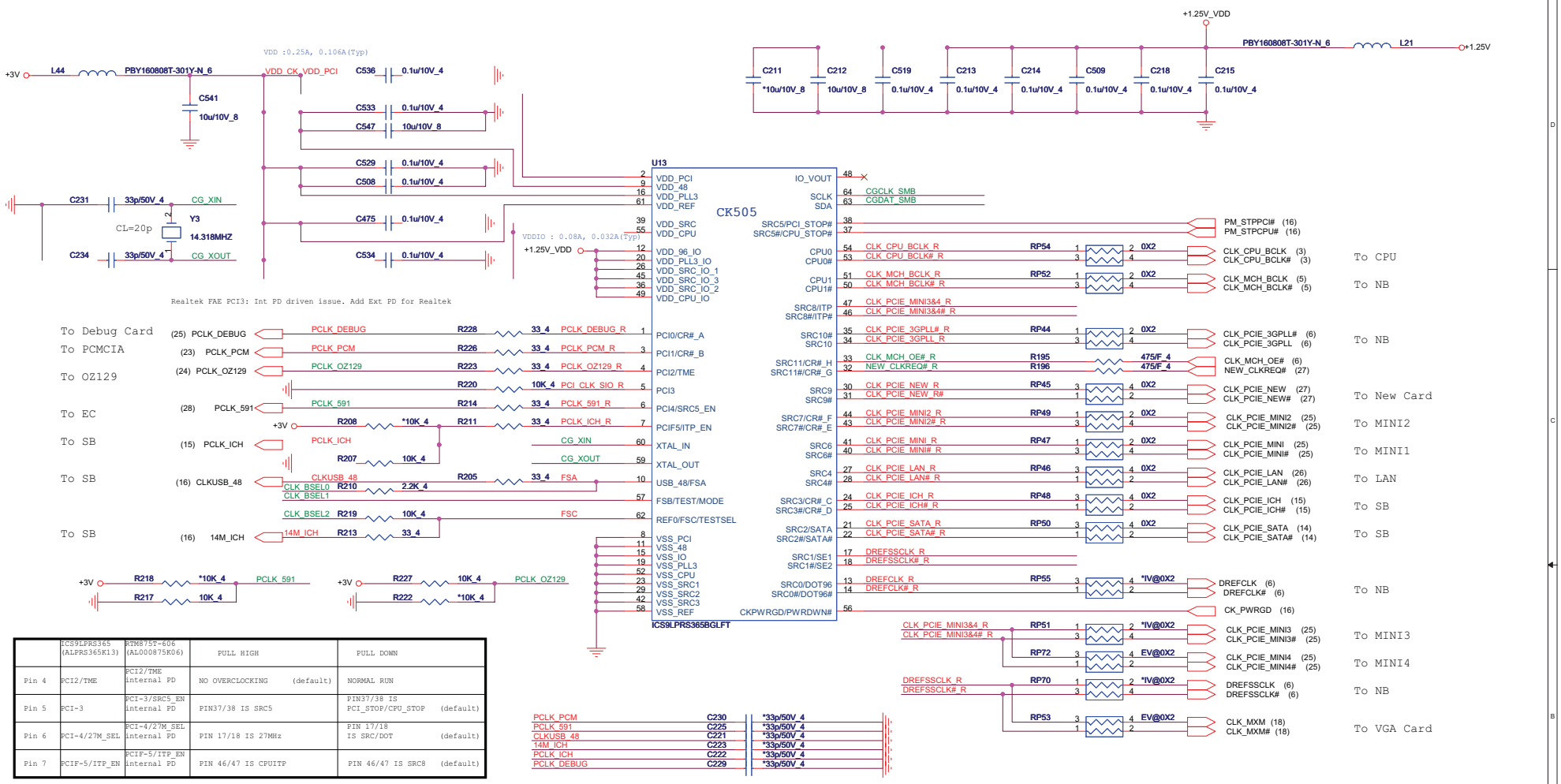
TE1 Block Diagram



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#	OZ129T
REQ1# / GNT1#	AD18	INTC#	CB1410

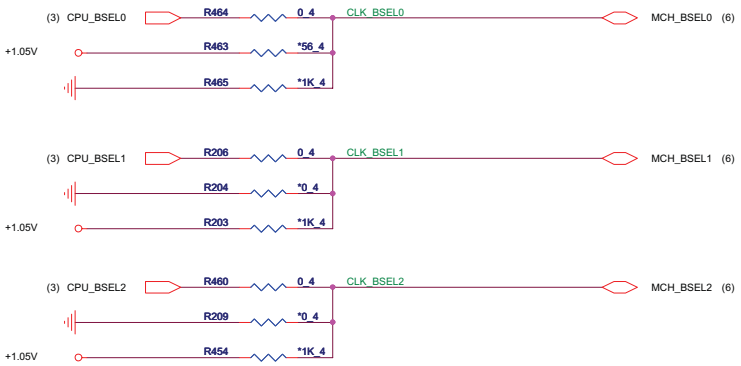
Clock Generator



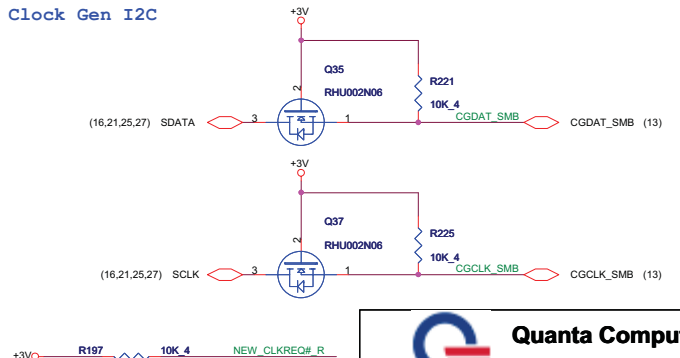
	ICS91PRS365 (ALPRS365K13)	RTM875T-606 (AL000875K06)	PULL HIGH	PULL DOWN
Pin 4	PCI2/TME	PCI2/TME internal PD	NO OVERCLOCKING (default)	NORMAL RUN
Pin 5	PCI-3	PCI-3/SRC5_EN internal PD	PIN37/38 IS SRC5	PIN37/38 IS PCI_STOP/CPU_STOP (default)
Pin 6	PCI-4/27M_SEL	PCI-4/27M_SEL internal PD	PIN 17/18 IS 27MHz	PIN 17/18 IS SRC/DOT (default)
Pin 7	PCIF-5/ITP_EN	PCIF-5/ITP_EN internal PD	PIN 46/47 IS CPUITP	PIN 46/47 IS SRC8 (default)

BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz



Clock Gen I2C



Quanta Computer Inc.

PROJECT : TE1

Size	Document Number	Rev
	CLK. GEN./ CK505	A1A

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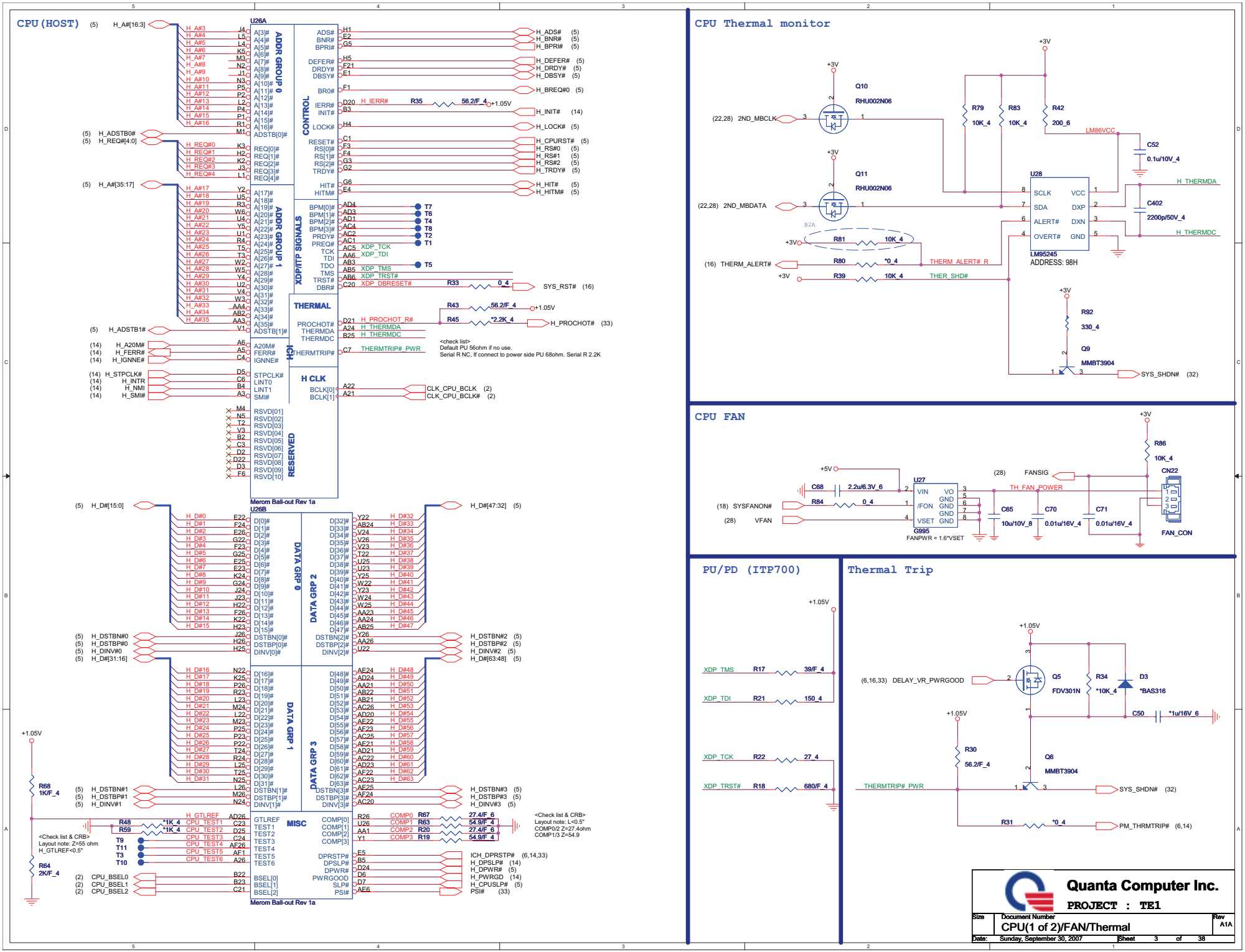
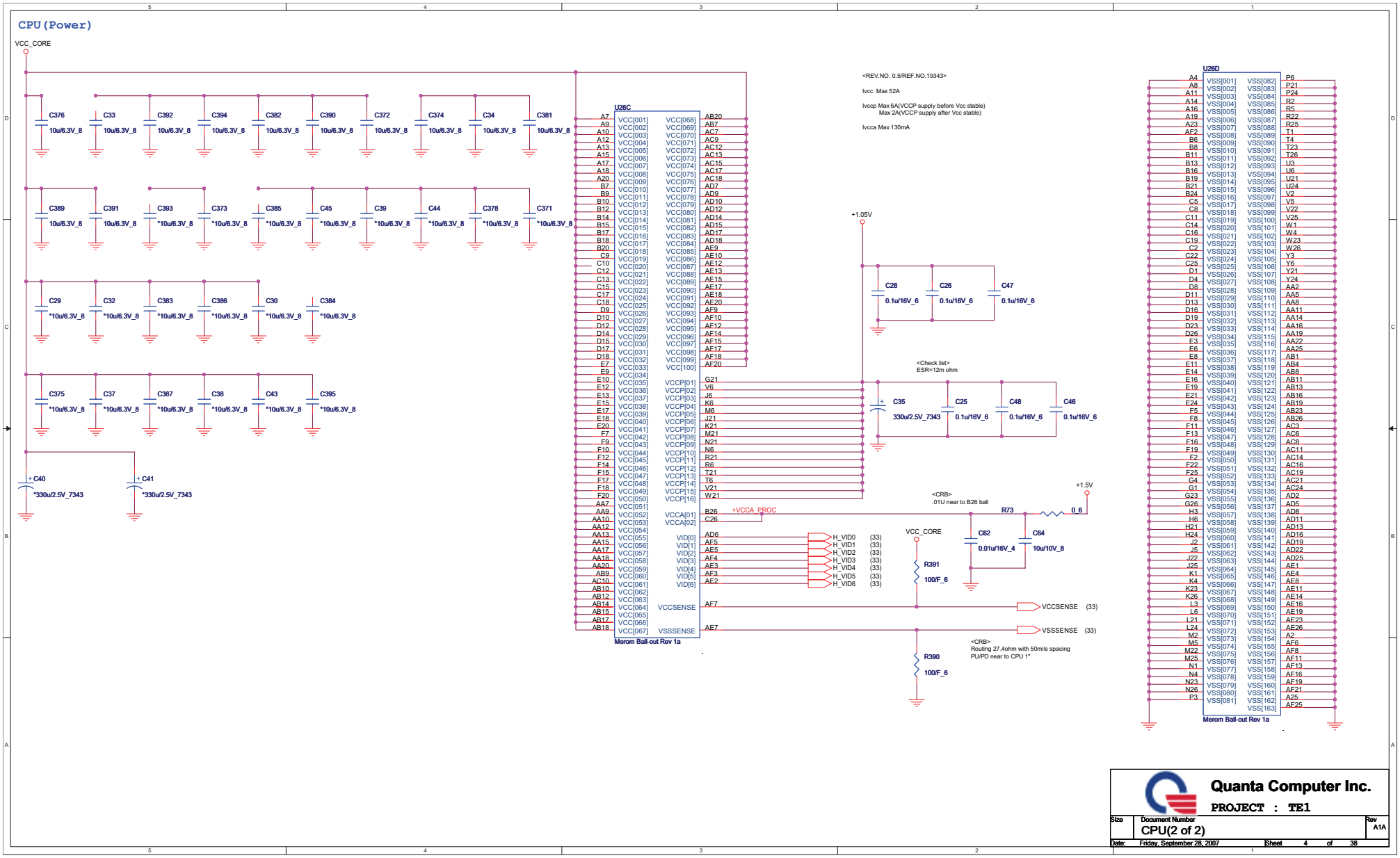




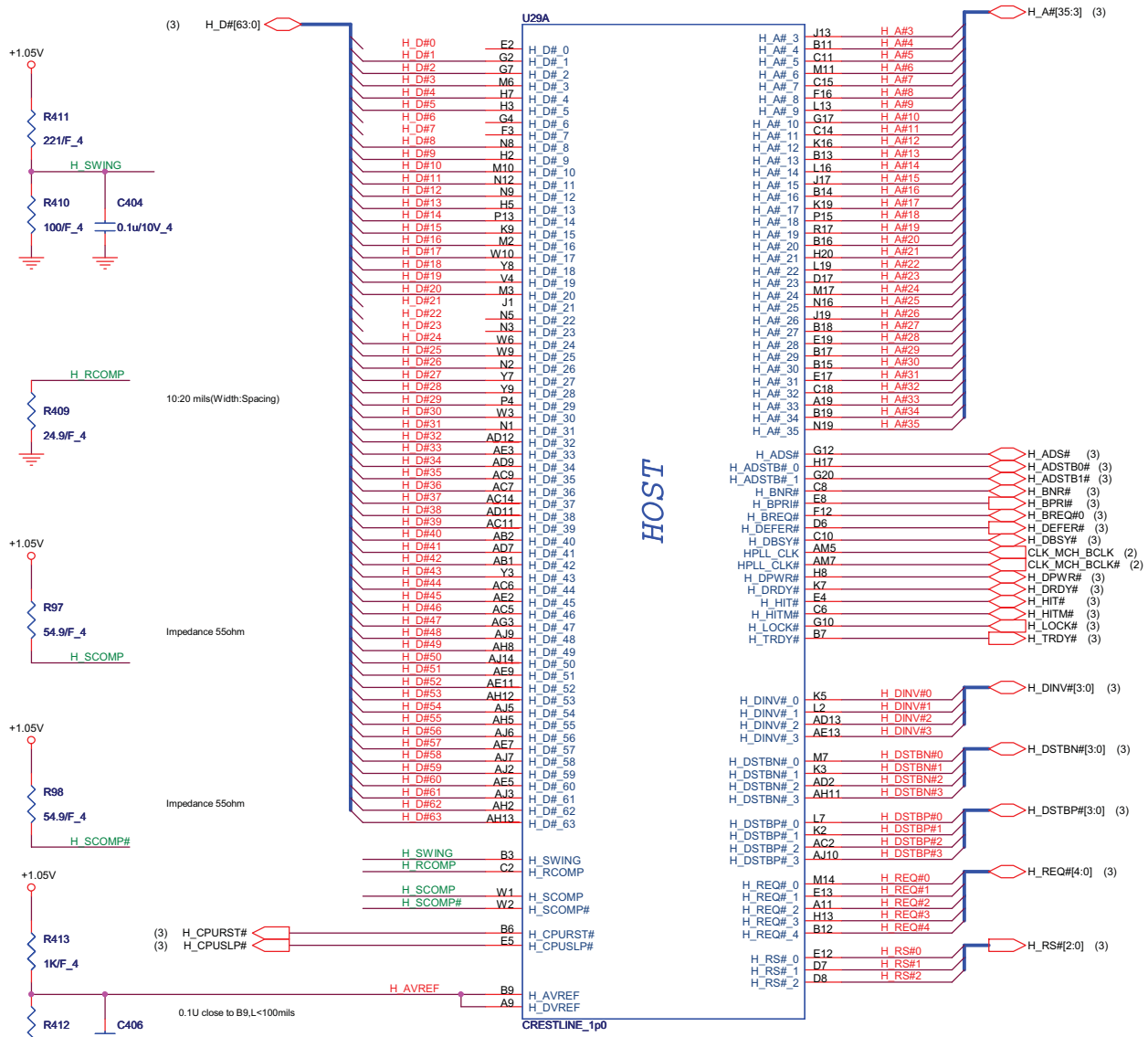
Quanta Computer Inc.

PROJECT : TE1

Size	Document Number	Rev
	CPU(2 of 2)	A1A

Date: Friday, September 28, 2007 Sheet 4 of 38

NB (HOST)



965GM : AJSLA5T0T20
965PM : AJSLA5U0T25
960GML : AJSLA5V0T09

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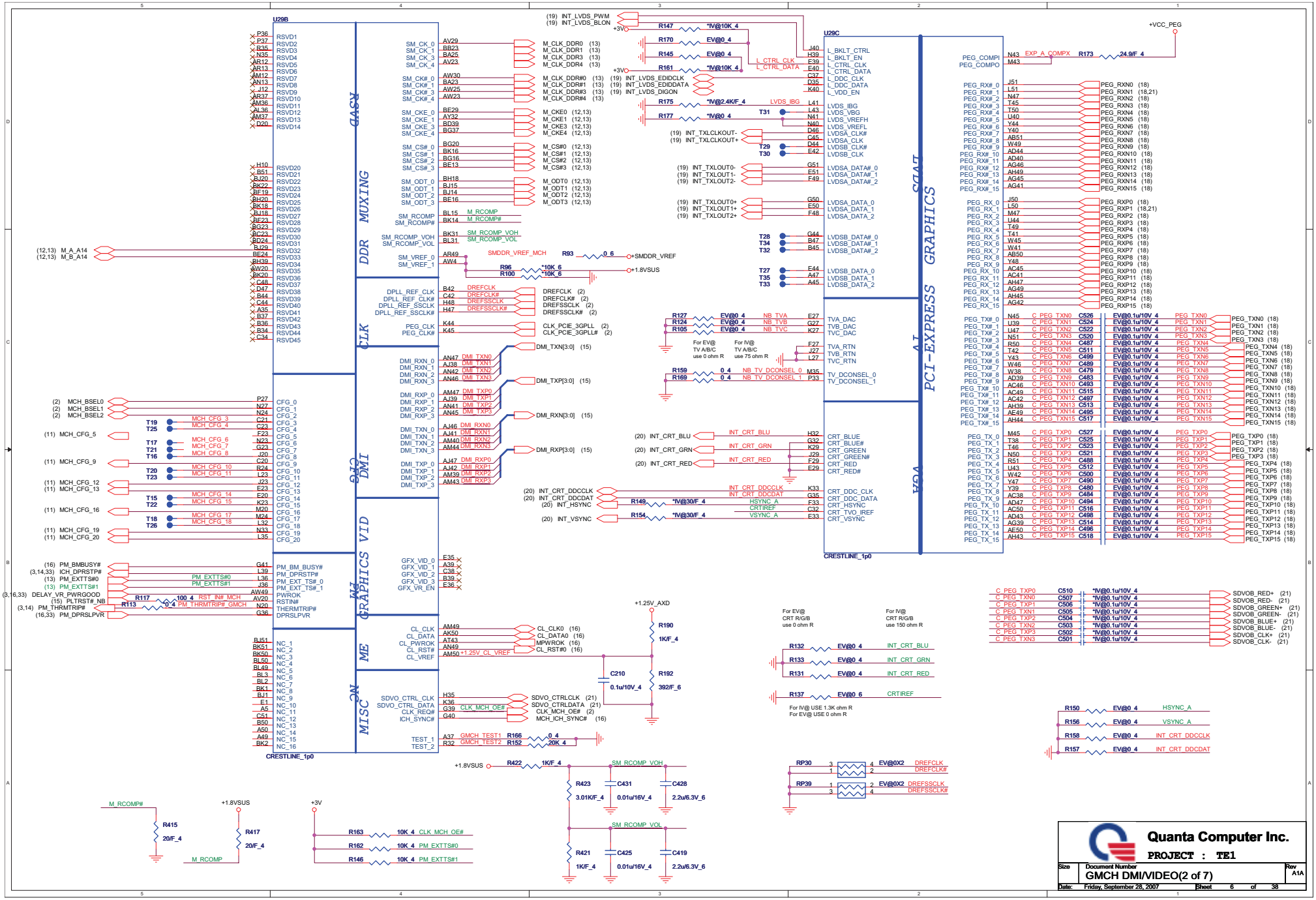
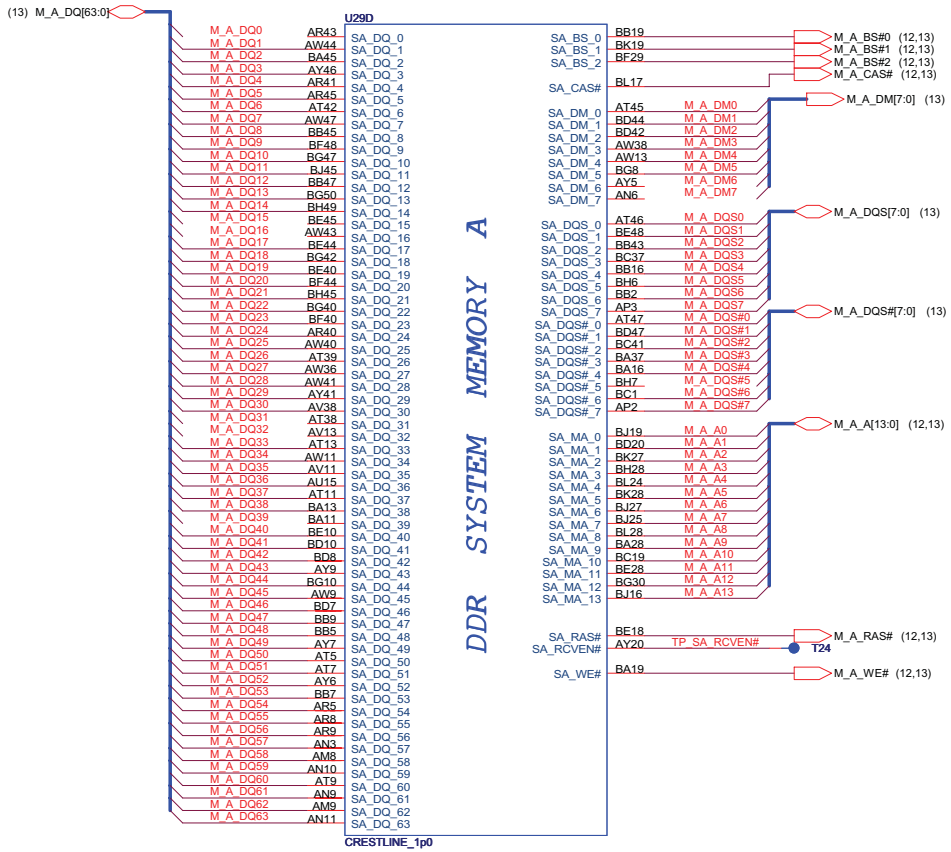
PROJECT : TE1

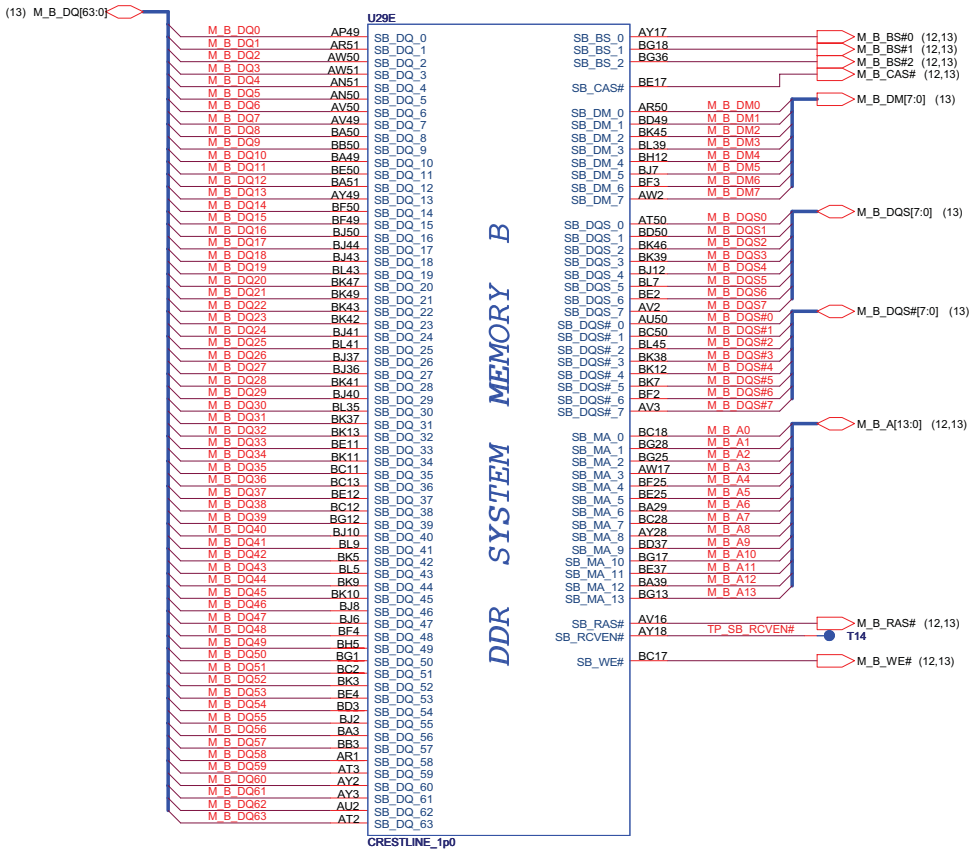
Size	Document Number	Rev
	GMCH HOST(1 of 7)	A1A

Date: Friday, September 28, 2007 Sheet 5 of 38



NB(Memory controller)





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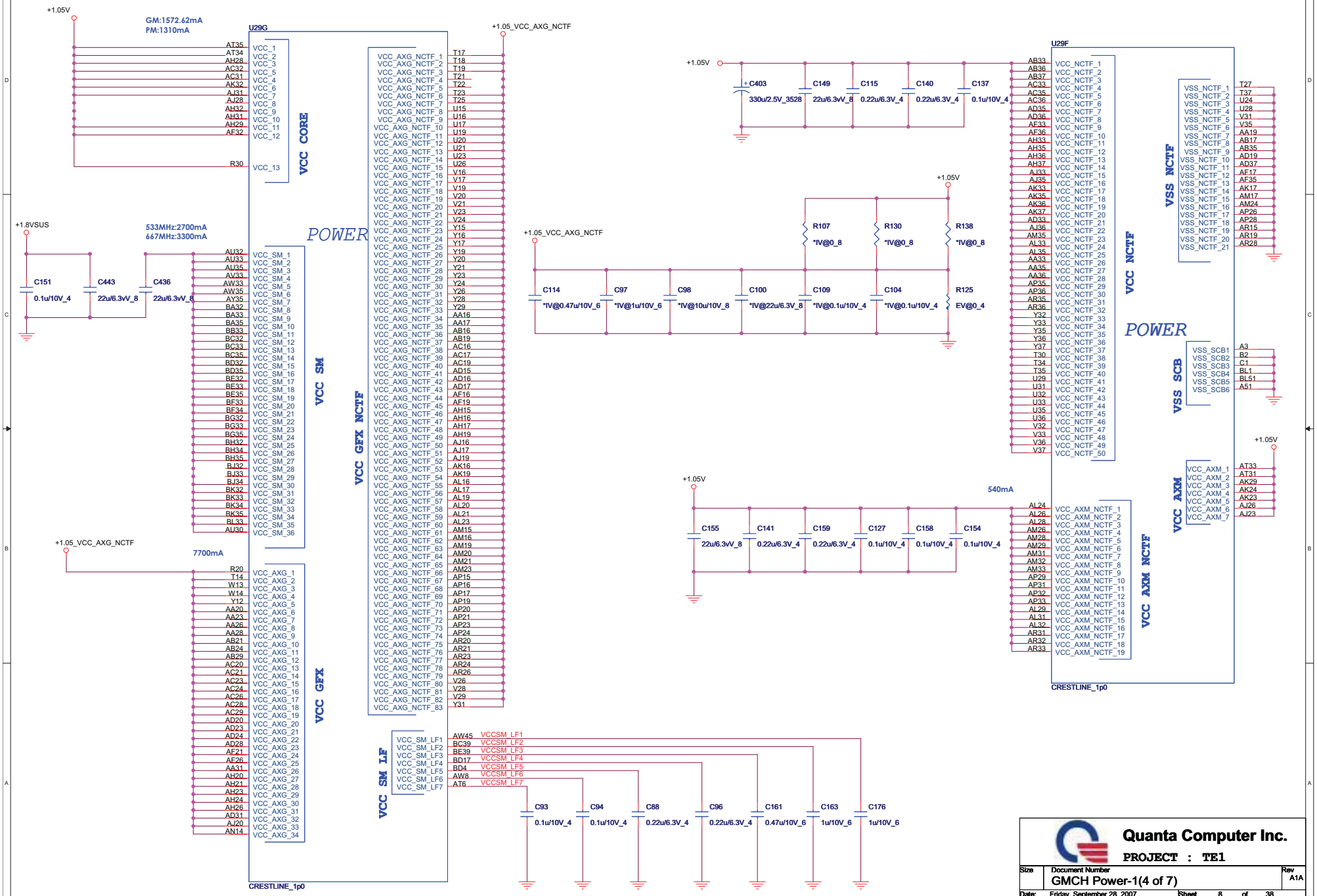
PROJECT : TE1

Size	Document Number	Rev
	MCH DDR(3 of 7)	A1A

Date: Friday, September 28, 2007 Sheet 7 of 38

NB(Power-1)

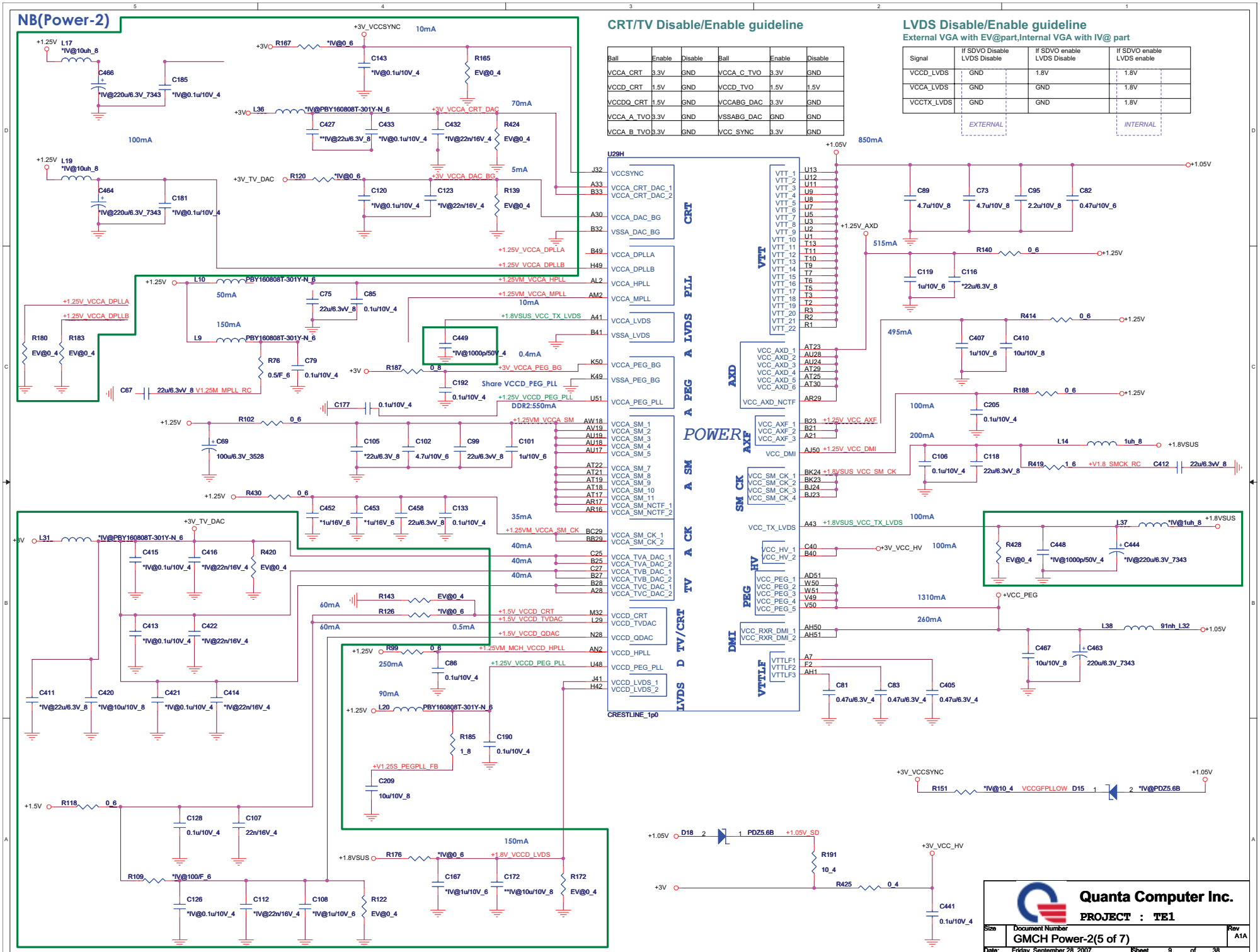


Quanta Computer Inc.

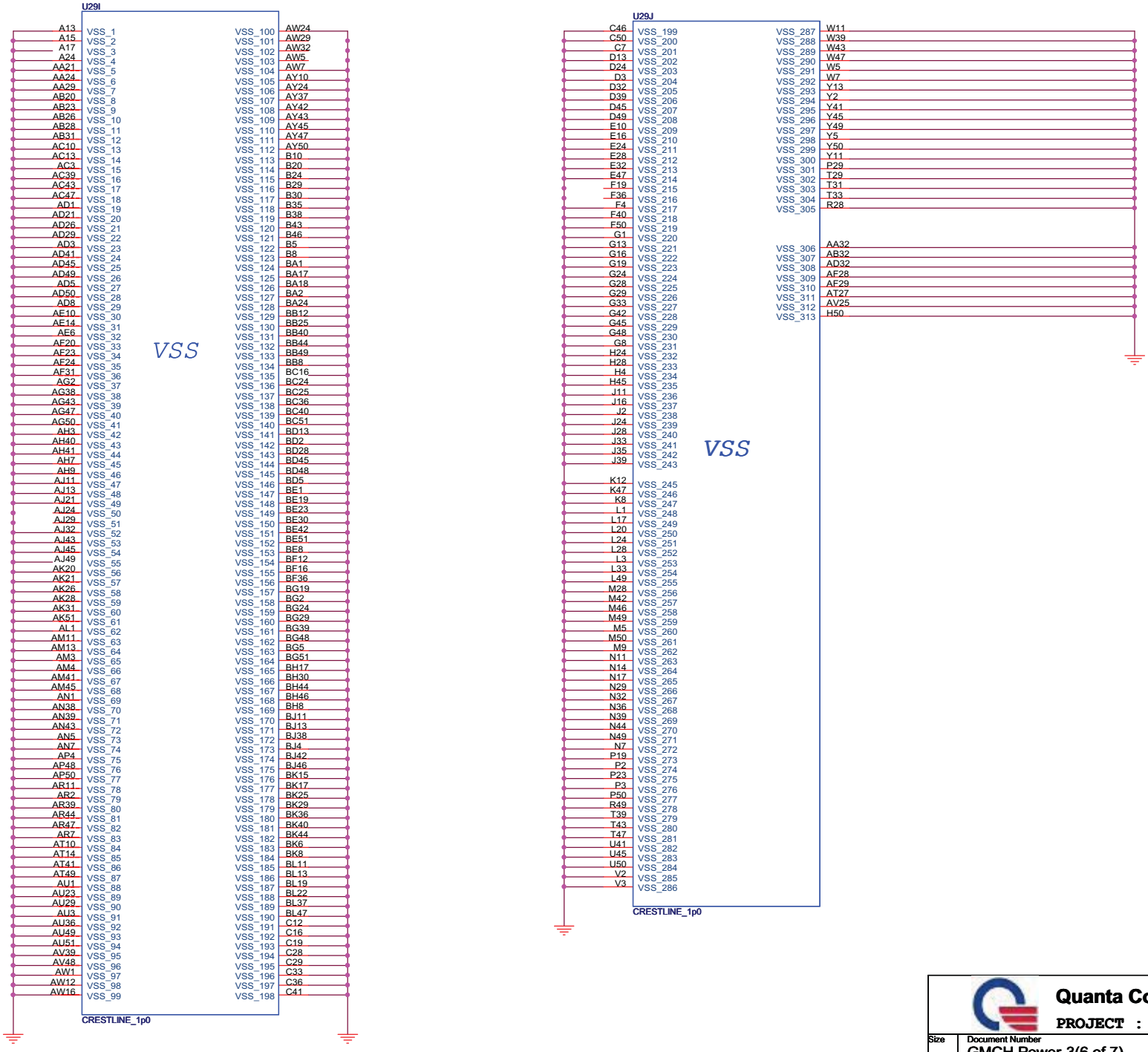
PROJECT : TE1

Size	Document Number	Rev
	GMCH Power-1(4 of 7)	A1A

Date: Friday, September 28, 2007 Sheet 8 of 38



NB(Power-3)



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PROJECT : TE1

Size	Document Number	Rev
	GMCH Power-3(6 of 7)	A1A

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Strap table(base on checklist Ver1.6)

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	Intel? Management Engine Crypto strap	0 = Intel? Management Engine Crypto Transport Layer.Security (TLS) cipher suite with no confidentiality 1= Intel Management Engine Crypto TLS Cipher Suite with confidentiality (default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE is operation(Default) 1 = SDVO and PCIE are operating simultaneously via the PEG port

DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)

DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane

XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

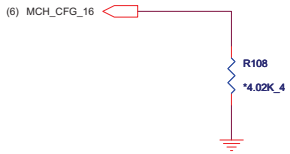
MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

SDVO Present

Strap define at External HDMI control page

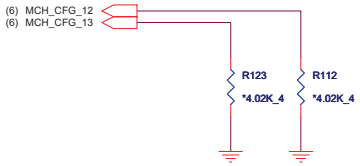
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE is operational(Default) High = SDVO andPCIE are operating simultaneously via the PEG port



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PROJECT : TE1

Size	Document Number	Rev
	GMCH Strap(7 of 7)	A1A

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DDR2 Dual channel A/B PU

M_A_A[13..0]
M_B_A[13..0]

M_A_A[13..0] (7,13)
M_B_A[13..0] (7,13)

DDRII A CHANNEL

+SMDDR_VTERM

C148 0.1u/10V_4 | C165 0.1u/10V_4 | C121 0.1u/10V_4 | C132 0.1u/10V_4 | C183 0.1u/10V_4 | C174 0.1u/10V_4 | C162 0.1u/10V_4 | C147 0.1u/10V_4 | C142 0.1u/10V_4 | C194 0.1u/10V_4 | C193 0.1u/10V_4 | C195 0.1u/10V_4 | C134 0.1u/10V_4

DDRII B CHANNEL

+SMDDR_VTERM

C202 0.1u/10V_4 | C171 0.1u/10V_4 | C124 0.1u/10V_4 | C139 0.1u/10V_4 | C125 0.1u/10V_4 | C196 0.1u/10V_4 | C203 0.1u/10V_4 | C169 0.1u/10V_4 | C160 0.1u/10V_4 | C144 0.1u/10V_4 | C178 0.1u/10V_4 | C199 0.1u/10V_4 | C152 0.1u/10V_4

Place one cap close to every 2 pull-up resistor terminated to SMDDR_VTERM

	M_A_A3	RP28	M_A_A1	+SMDDR_VTERM
	M_A_A9	RP34	M_A_A5	+SMDDR_VTERM
	M_A_A2	RP32	M_A_A4	+SMDDR_VTERM
(6,13) M_CKE1	M_A_A11	RP40		+SMDDR_VTERM
(6,13) M_CKE0	M_A_A8	RP38		+SMDDR_VTERM
(7,13) M_A_BS#2	M_A_A12	RP41		+SMDDR_VTERM
(7,13) M_A_BS#1	M_A_A0	RP25		+SMDDR_VTERM
(7,13) M_B_WE#	M_B_A10	RP26		+SMDDR_VTERM
	M_B_A3	RP29	M_B_A1	+SMDDR_VTERM
(7,13) M_B_BS#1	M_B_A0	RP27		+SMDDR_VTERM
	M_B_A7	RP35	M_B_A11	+SMDDR_VTERM
	M_B_A8	RP33	M_B_A5	+SMDDR_VTERM
	M_B_A2	RP31	M_B_A4	+SMDDR_VTERM
	M_B_A9	RP36	M_B_A12	+SMDDR_VTERM

	M_A_A7	RP37	M_A_A6	+SMDDR_VTERM
(6,13) M_CKE3	(7,13) M_B_BS#2	RP43		+SMDDR_VTERM
(6,13) M_ODT1	(6,13) M_CS#1	RP18		+SMDDR_VTERM
(6,13) M_ODT3	(7,13) M_B_BS#0	RP19		+SMDDR_VTERM
	M_A_A10	RP24	(7,13) M_A_BS#0	+SMDDR_VTERM
(7,13) M_A_CAS#	(7,13) M_A_WE#	RP21		+SMDDR_VTERM
(6,13) M_CS#0	(7,13) M_A_RAS#	RP23		+SMDDR_VTERM
(7,13) M_B_CAS#	(6,13) M_CS#3	RP22		+SMDDR_VTERM
	M_B_A6	RP42	(6,13) M_CKE4	+SMDDR_VTERM
(6,13) M_ODT2	(7,13) M_B_RAS#	RP20		+SMDDR_VTERM
(6,13) M_ODT0	M_A_A13	RP16		+SMDDR_VTERM
	M_B_A13	RP17	(6,13) M_CS#2	+SMDDR_VTERM

(6,13) M_A_A14 — R181 56_4
(6,13) M_B_A14 — R178 56_4
+SMDDR_VTERM

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PROJECT : TE1

Size	Document Number	Rev
	DDR RES. ARRAY	A1A

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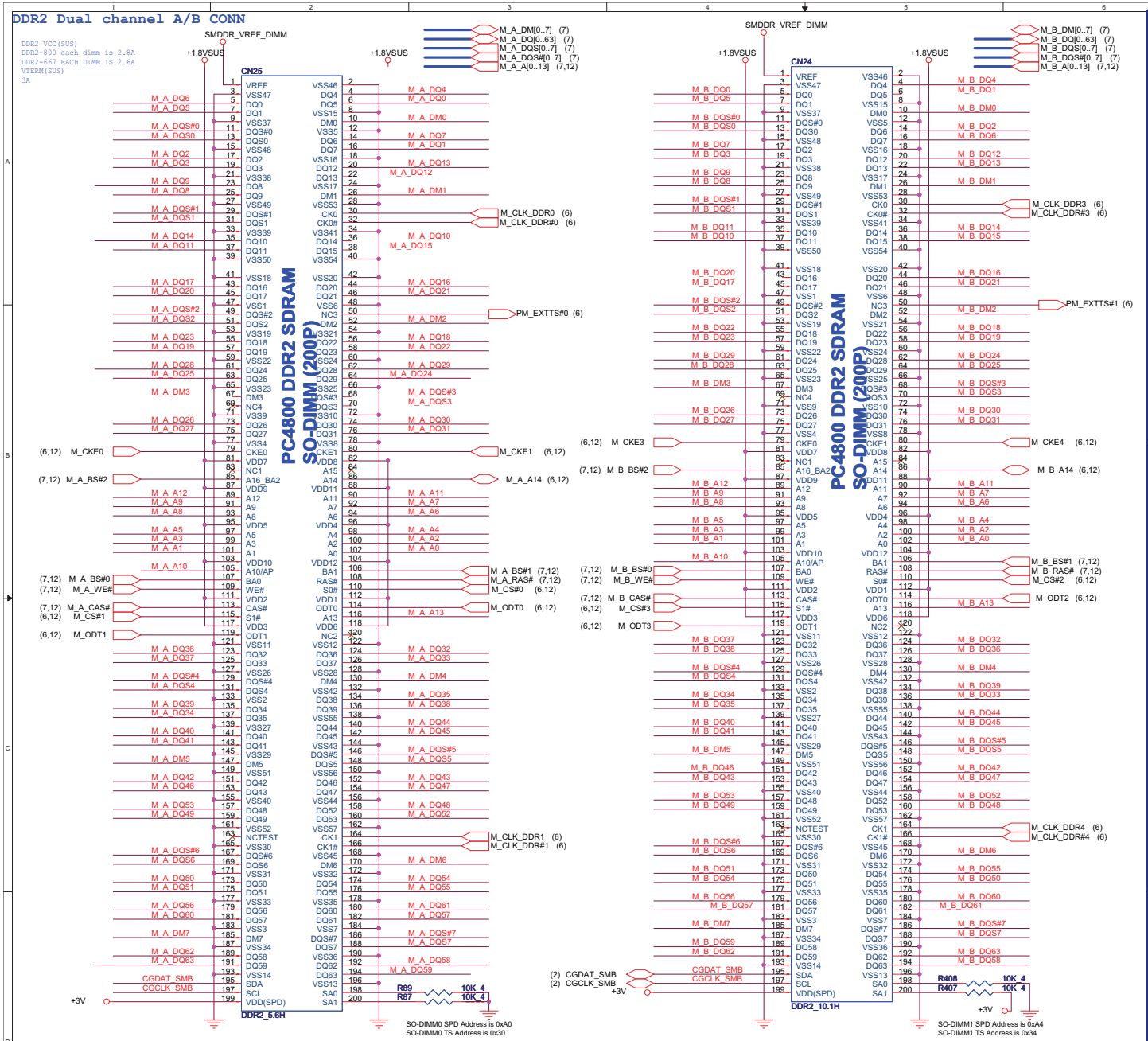
DDR2 Dual channel A/B CONN

DDR2 VCC(SUS)
DDR2-800 each dimm is 2.8A
DDR2-667 EACH DIMM IS 2.6A
VTERM(SUS)
3A



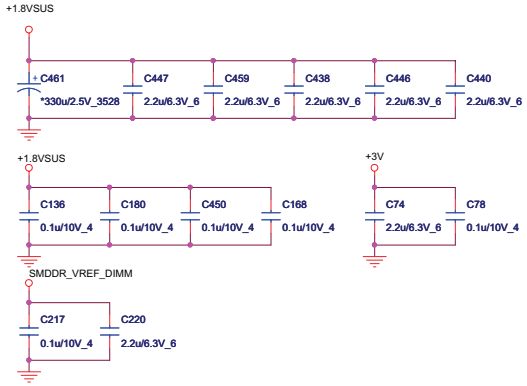
H: 5.6mm

CLOCK 0,1
CKE 0,1

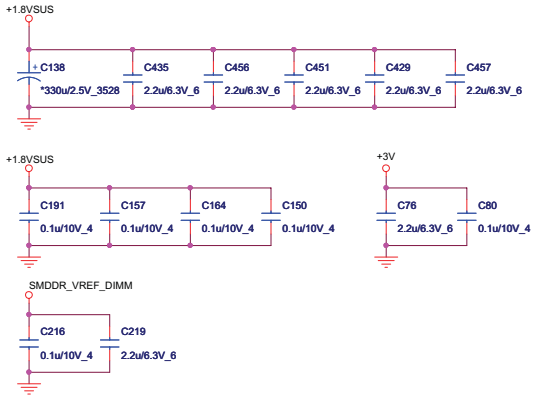
H: 10.1mm

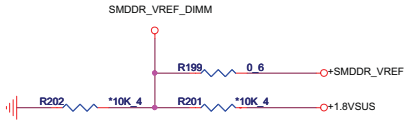
CLOCK 3,4
CKE 2,3

Close to DIMM0



Close to DIMM1





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PROJECT : TE1

Size	Document Number	Rev
	DDR SO-DIMM(200P)	A1A

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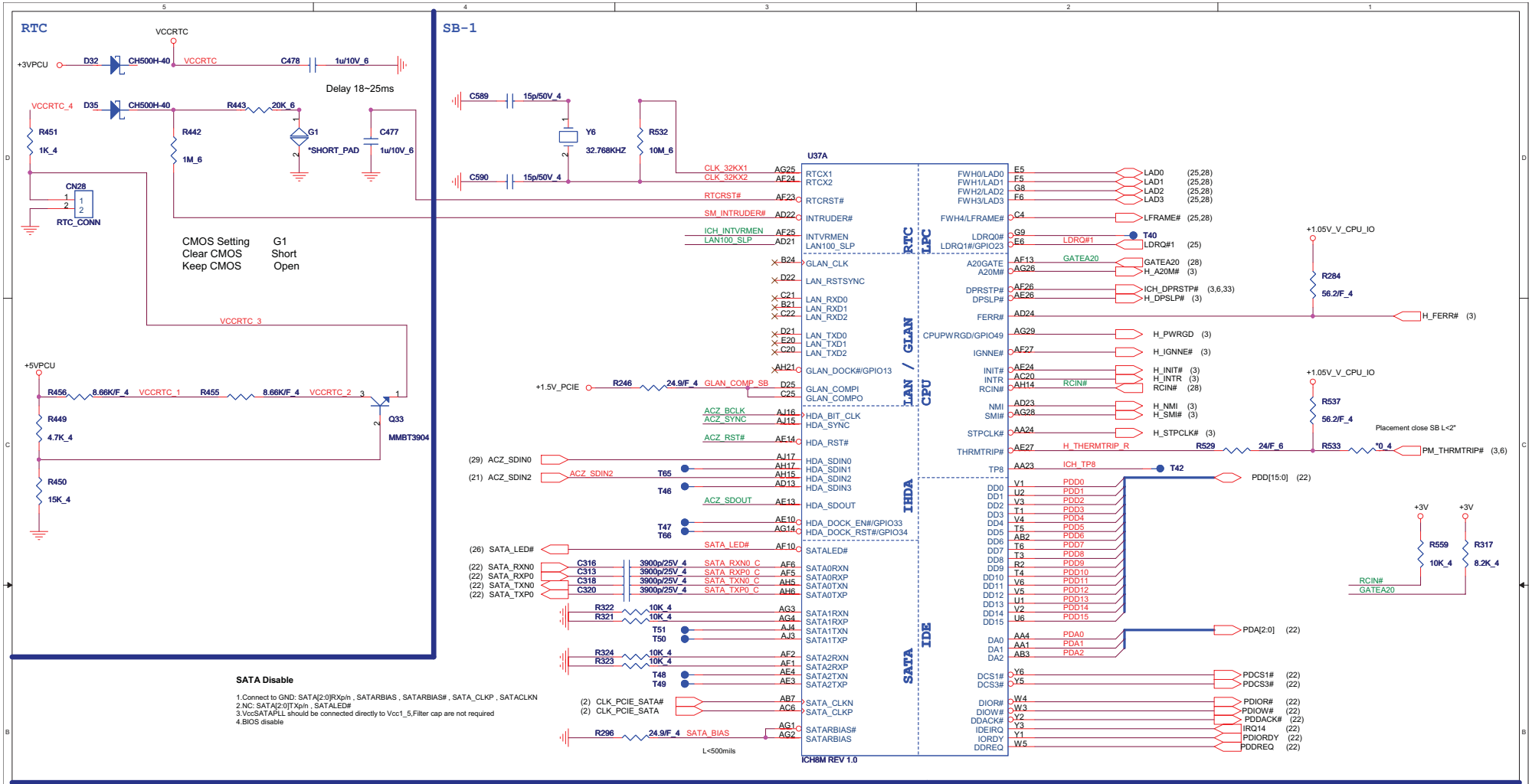
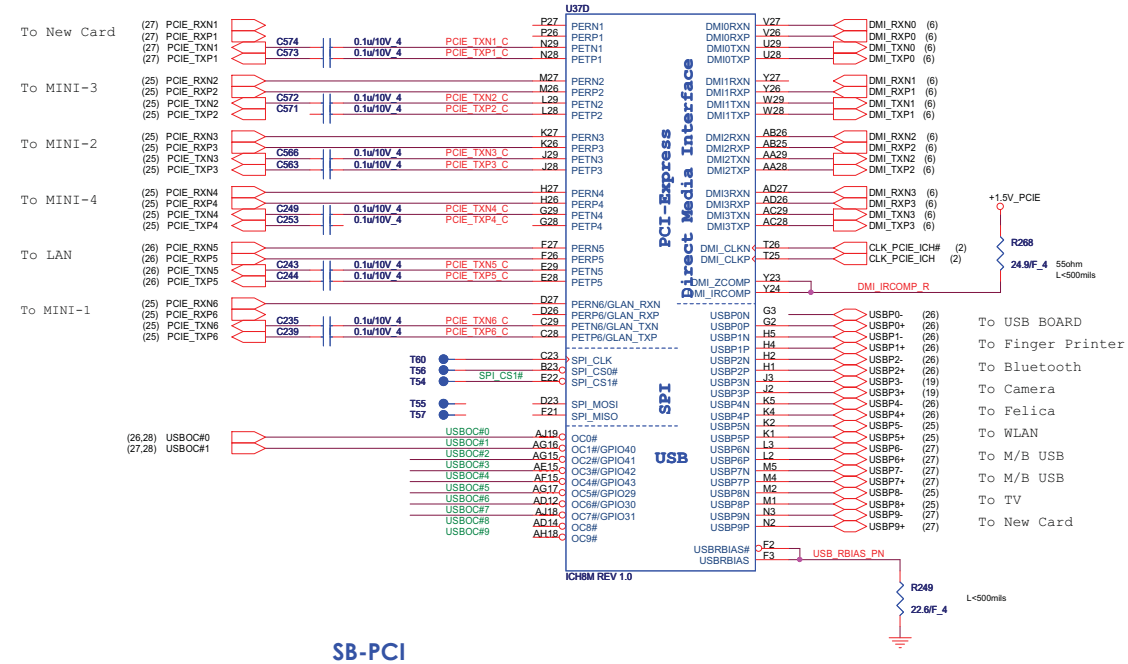


SB-PCIE/USB/DMI



A16 SWAP Override strap

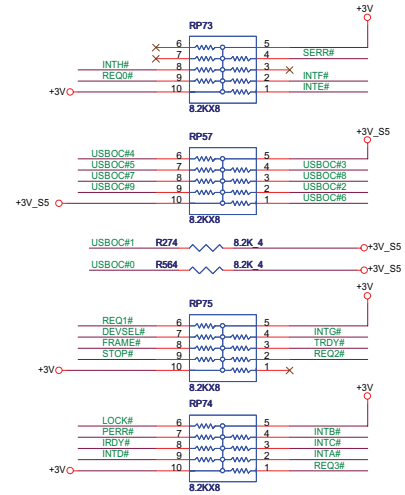
PCI_GNT#3	Low = A16 swap override enabled High = Default

GNT3# R469 *1K_4

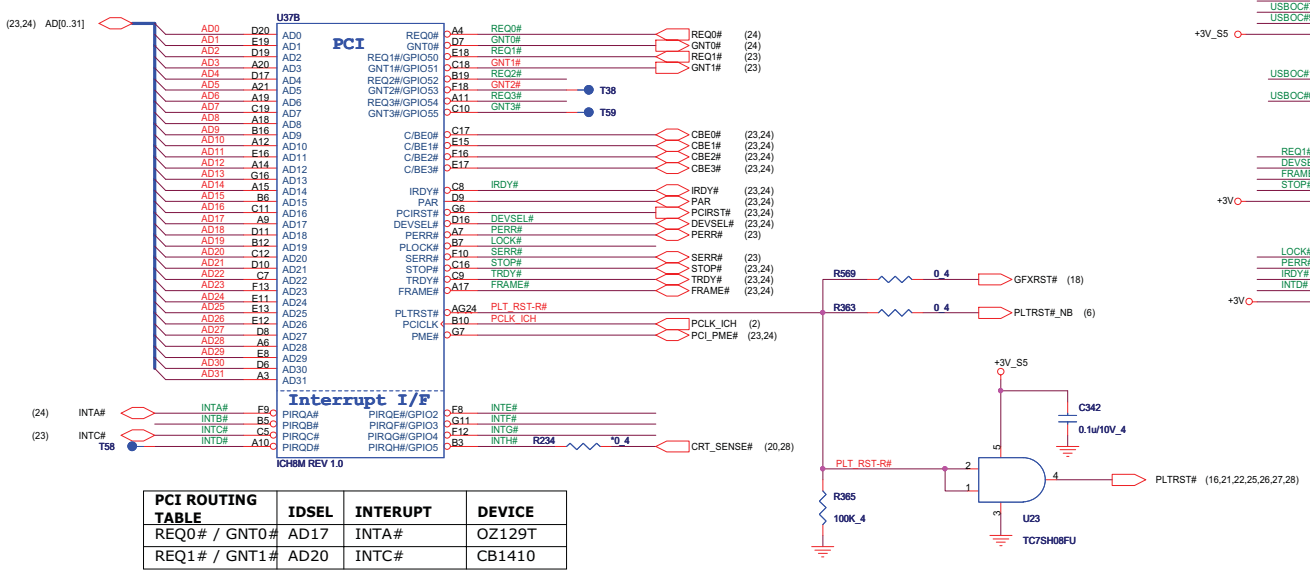
ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

SPI_CS1# R467 *1K_4
GNT0# R244 *1K_4



SB-PCI



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#	OZ129T
REQ1# / GNT1#	AD20	INTC#	CB1410

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PROJECT : TE1

Size	Document Number	Rev
	ICH8M PCIE(2 of 4)/ BIOS	A1A

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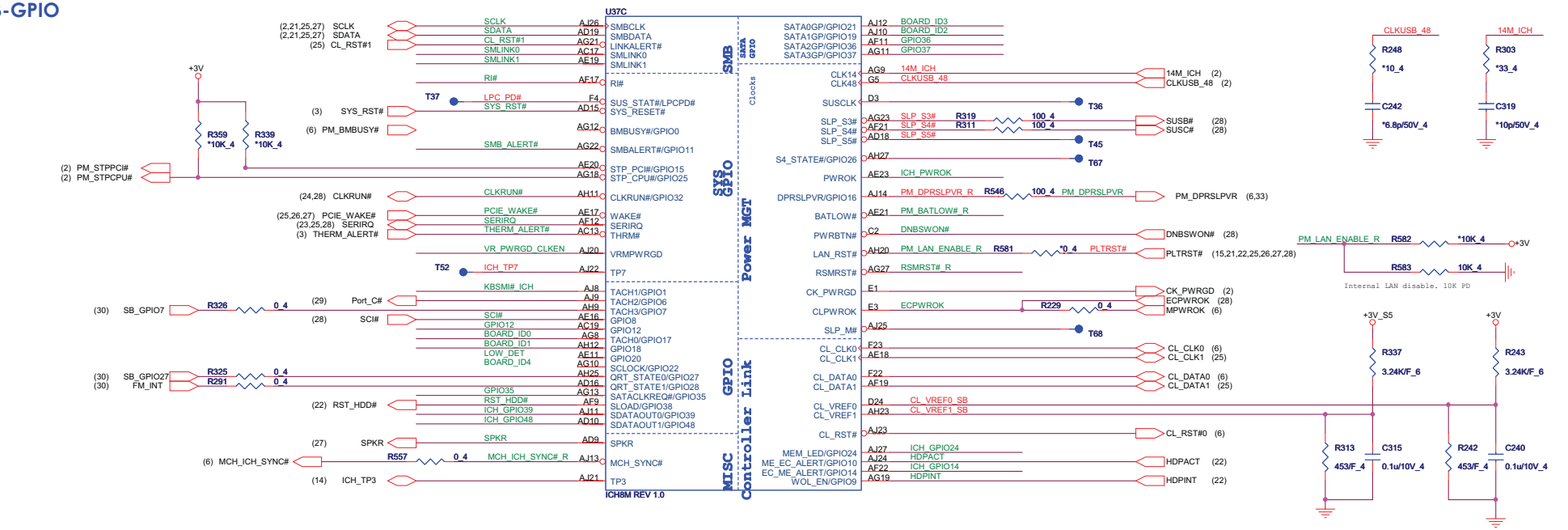
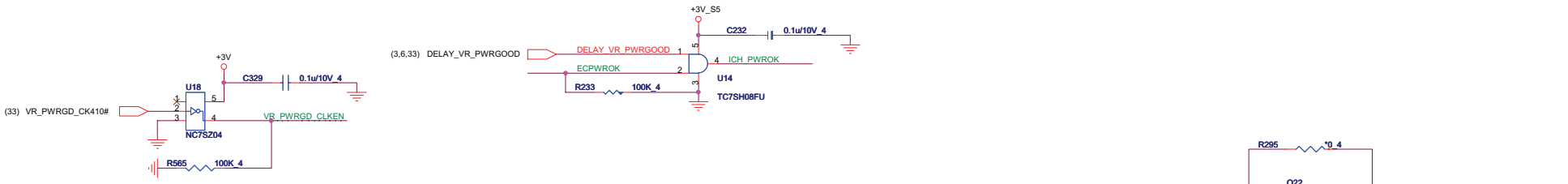
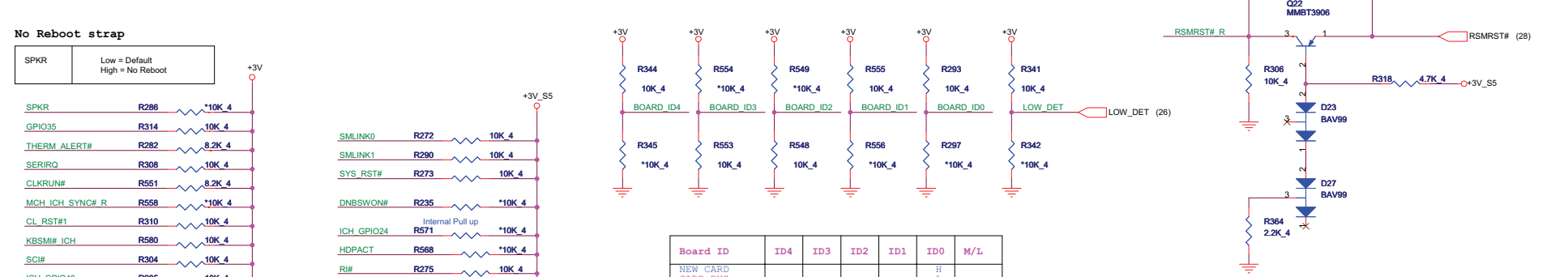
SB-GPIO





No Reboot strap

SPKR	Low = Default High = No Reboot



Board ID	ID4	ID3	ID2	ID1	ID0	M/L
NEW CARD CARD BUS					H L	
CCFL Panel LED Panel				H L		
W/ G-SENSOR W/O G-SENSOR			H L			
W/ TV W/O TV		H L				
W/ HDMI W/O HDMI	H L					
Main Strem Low Cost						H L

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PROJECT : TE1

Size	Document Number	Rev
	ICH8M GPIO(3 of 4)	A1A

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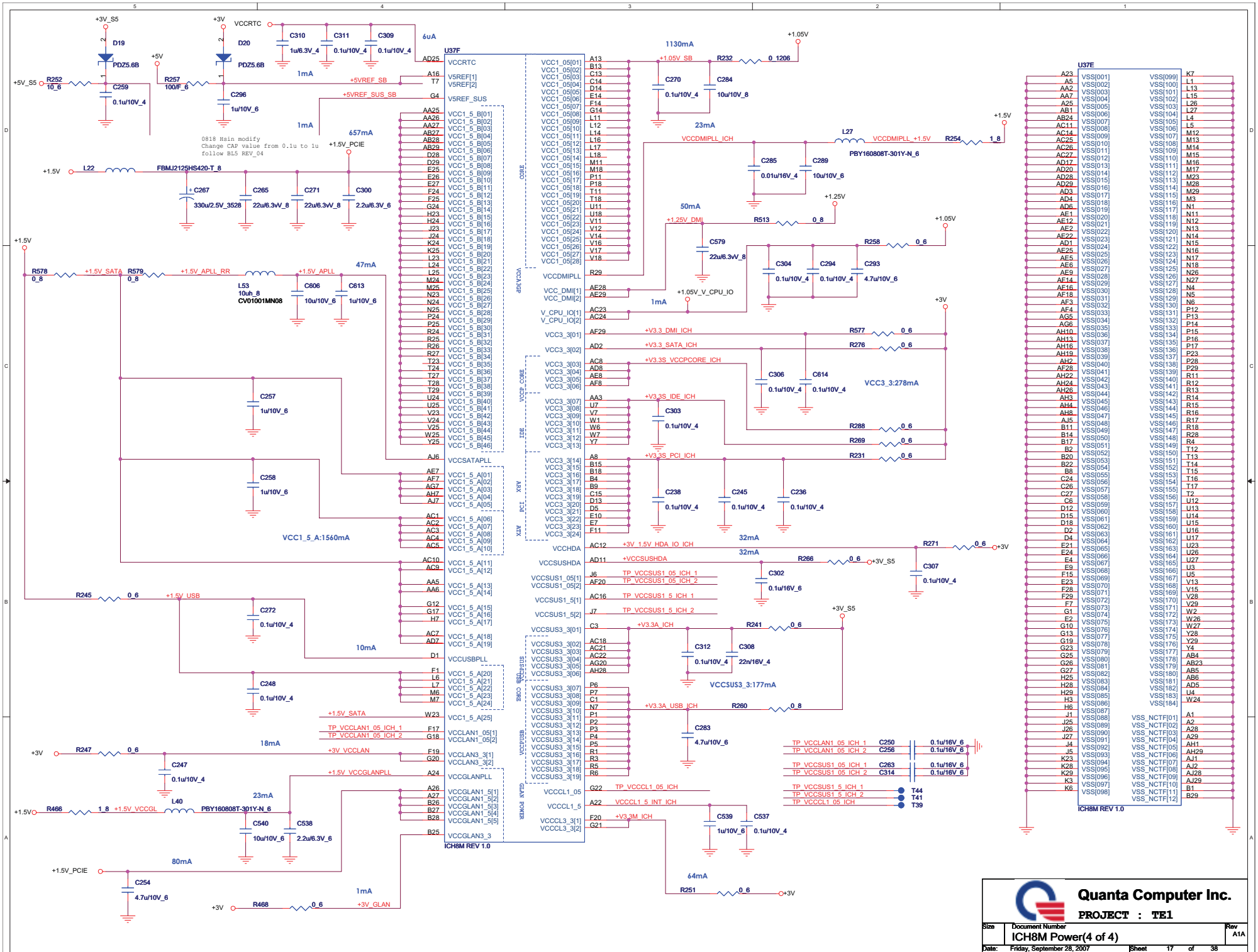
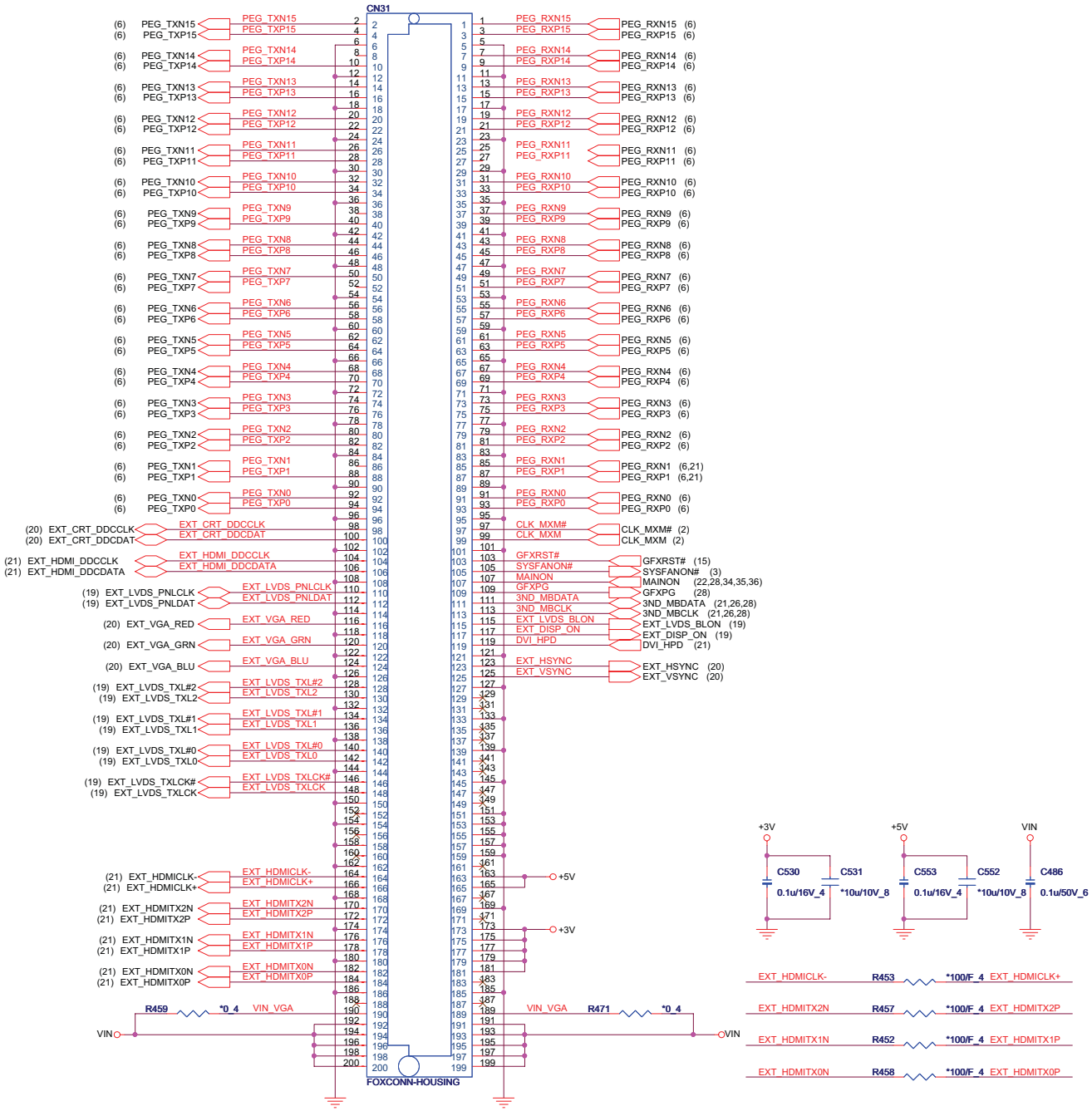


VGA/B conn



EXT_HDMICLK-	R453	*100/F_4	EXT_HDMICLK+	
EXT_HDMITX2N	R457	*100/F_4	EXT_HDMITX2P	
EXT_HDMITX1N	R452	*100/F_4	EXT_HDMITX1P	
EXT_HDMITX0N	R458	*100/F_4	EXT_HDMITX0P	

VIN(ALW)	4A
VDD_5V(RUN)	0.5A
VDD_3.3V(RUN)	2.5A

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PROJECT : TE1

Size	Document Number	Rev
	VGA CONNECTOR	A1A

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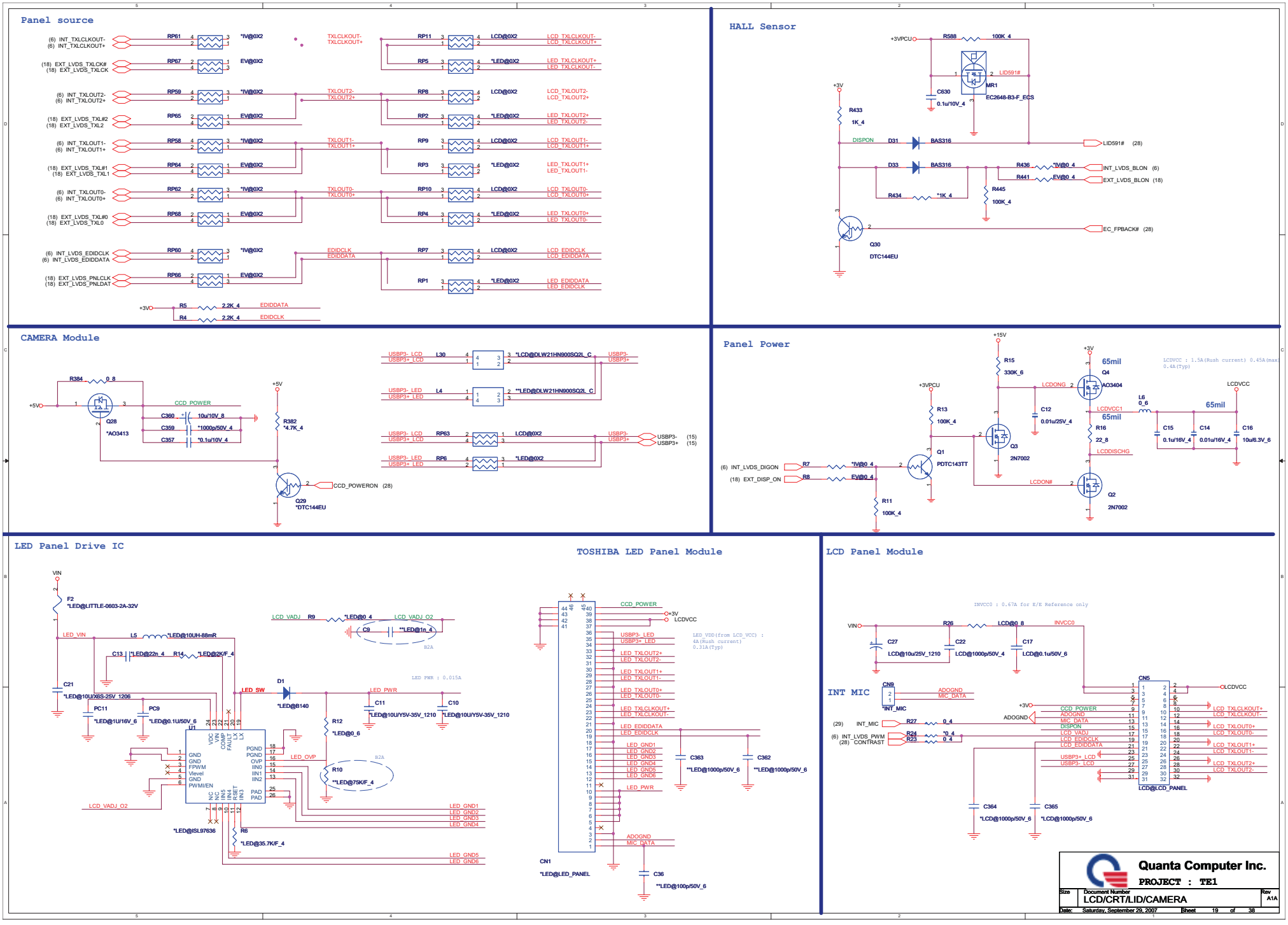
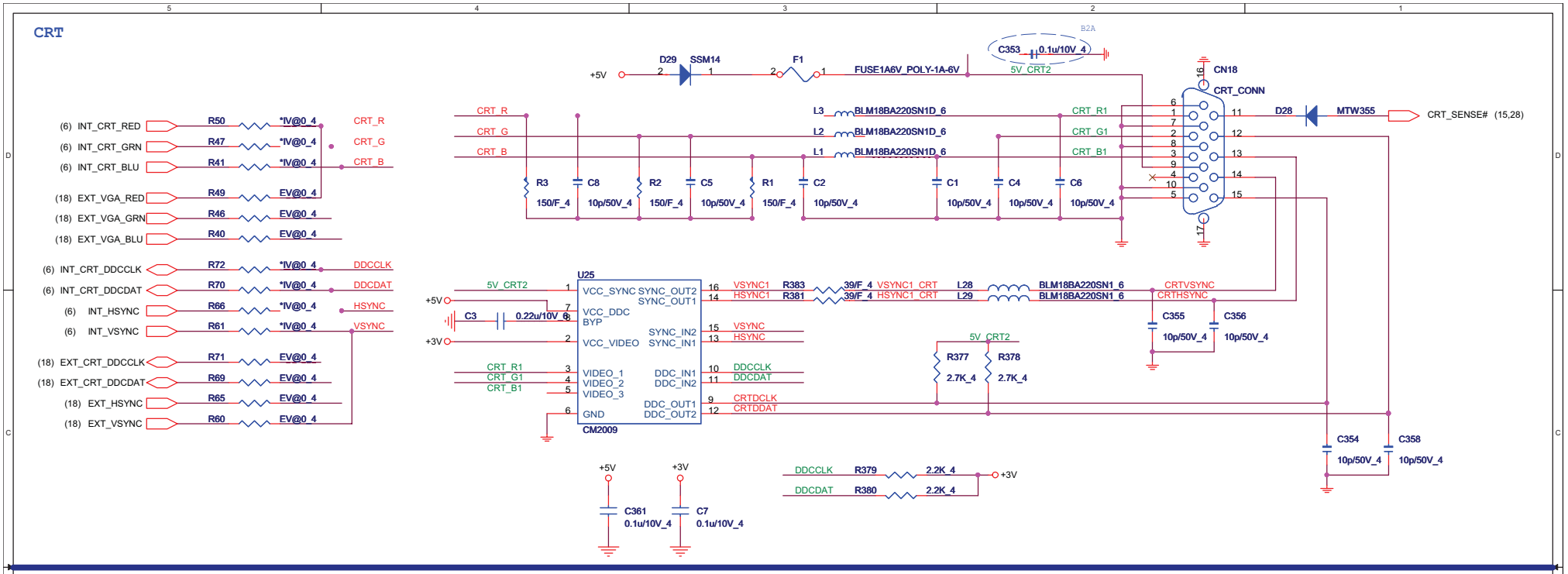
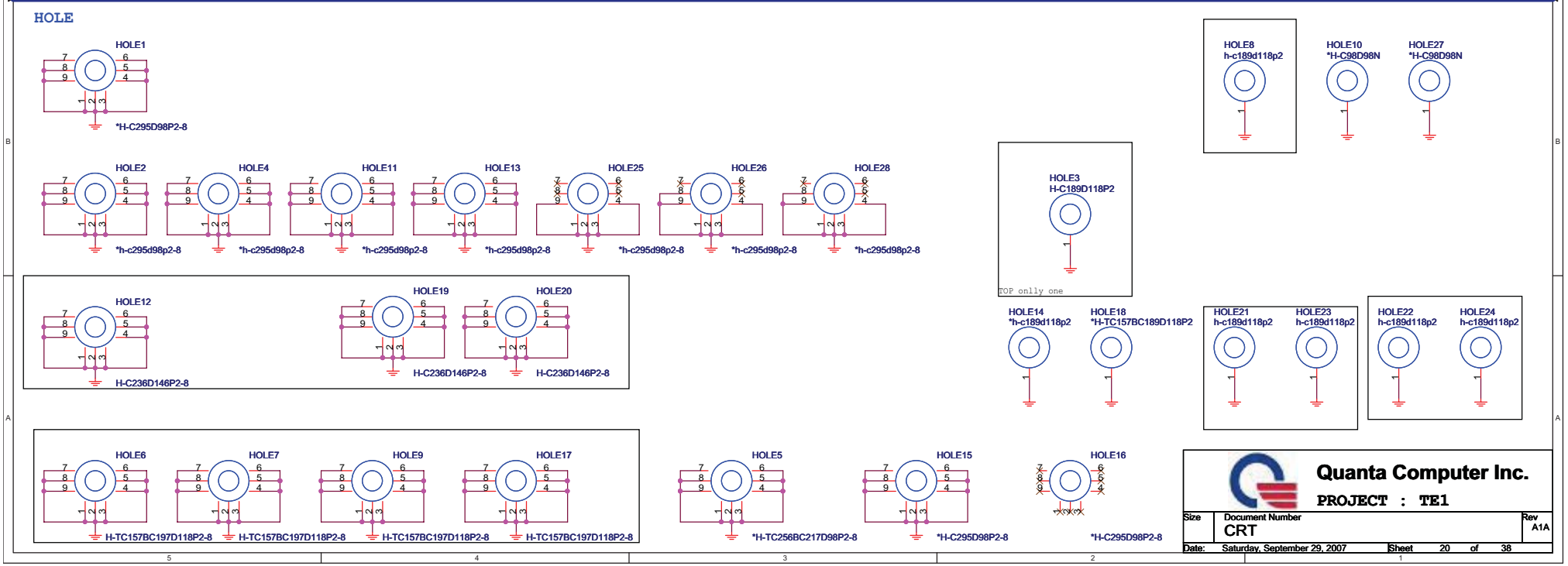


CRT



HOLE



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PROJECT : TE1

Size	Document Number	Rev
	CRT	A1A

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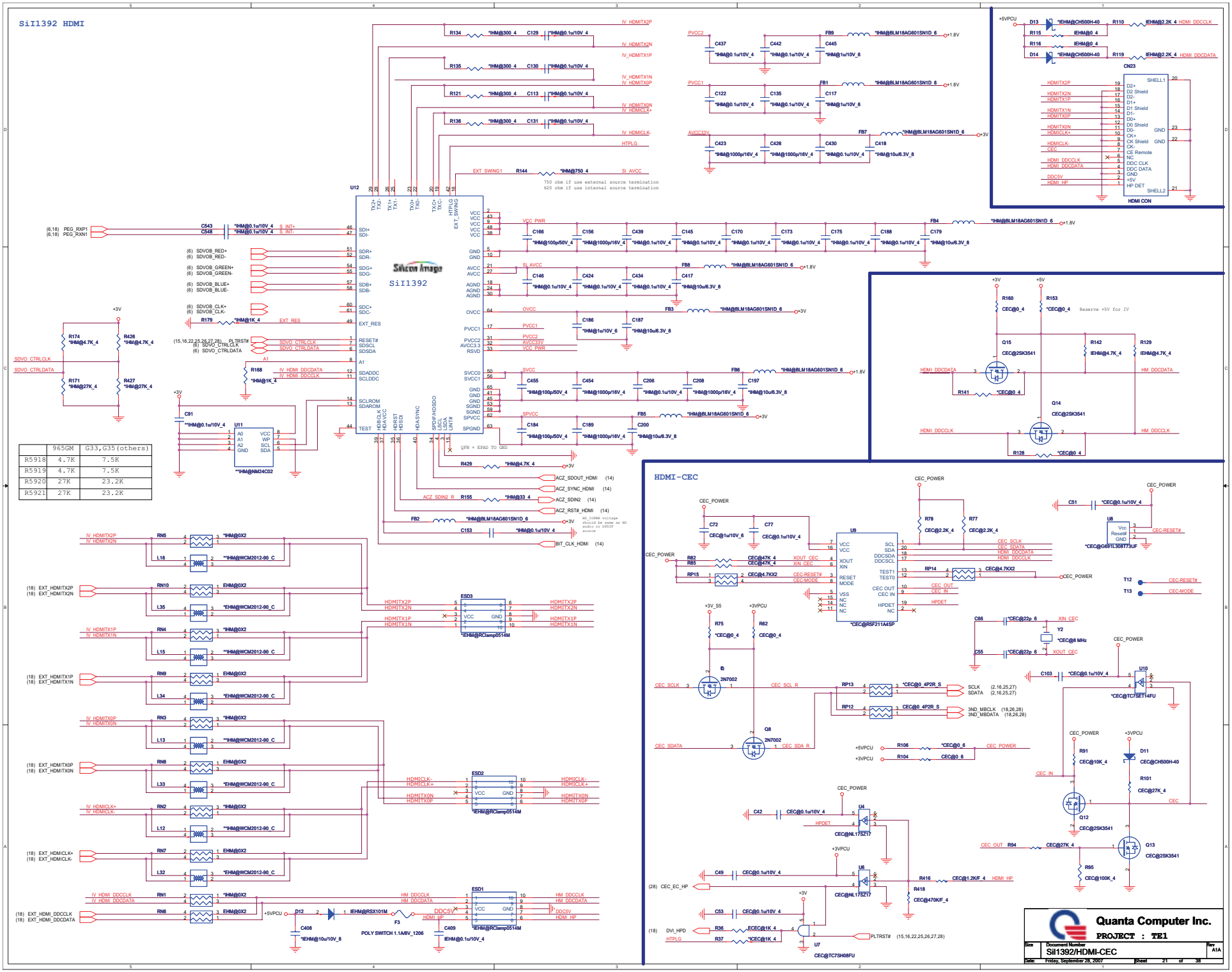


	965GM	G33,G35(others)
R5918	4.7K	7.5K
R5919	4.7K	7.5K
R5920	27K	23.2K
R5921	27K	23.2K

ODD

5VHDD(RUN) : 1A

CN36

(14) PDD[0..15] — PDD[0..15]

(14) PDDREQ — PDDREQ
(14) PDIOW# — PDIOW#
(14) PDIOR# — PDIOR#
(14) PDIORDY — PDIORDY
(14) PDDACK# — PDDACK#
(14) IRQ14 — IRQ14
(14) PDA1 — PDA1
(14) PDA0 — PDA0
(14) PDCS1# — PDCS1#
(14) PDA2 — PDA2
(14) PDCS3# — PDCS3#
(26) ODD_LED# — ODD_LED#

-IDERST, PDD7, PDD6, PDD5, PDD4, PDD3, PDD2, PDD1, PDD0, PDIOW#, PDIORDY, IRQ14, PDA1, PDA0, PDCS1#, ODD_LED#

PDD8, PDD9, PDD10, PDD11, PDD12, PDD13, PDD14, PDD15, PDDREQ, PDIOR#, PDDACK#, DIAG#, PDA2, PDCS3#

R256 *10K_4 +5V

+5V R236 470_6

C276 0.1u/10V_4 C260 1000p/50V_6 C277 0.1u/10V_4 C281 10u/10V_8 C251 *150u/6.3V_7343

ODD_CONN

+3V +5V Q38 DTC144EU R504 10K_4 -IDERST

(16) RST_HDD# R240 *0_4
(15,16,21,25,26,27,28) PLTRST# R239 0_4

+3V R264 4.7K_4 PDIORDY
+3V R259 8.2K_4 IRQ14

SATA HDD

5VODD(RUN) : 1.8A

CN19 Serial_ATA

GND23, GND1, RXP, RXN, GND2, TXN, TXP, GND3, 3.3V, 3.3V, 3.3V, GND, GND, GND, 5V, 5V, 5V, GND, RSVD, GND, 12V, 12V, 12V, GND24

SATA_TXP0 — SATA_TXP0 (14)
SATA_TXN0 — SATA_TXN0 (14)
SATA_RXN0 — SATA_RXN0 (14)
SATA_RXP0 — SATA_RXP0 (14)

+3.3VSATA R388 *0_8 +3V
C369 *4.7u/10V_8 C370 *0.1u/10V_4

+5VSATA R386 0_8 +5V
C23 0.1u/10V_4 C20 0.1u/10V_4 C24 10u/10V_8 C31 *150u/6.3V_7343

G SENSOR

(18,28,34,35,36) MAINON — +5V_S5

U30 *GS@G913-C
SHDN, VO, GND, VIN, SET

+3V_HDP C469 *GS@10u/10V_8
C472 *GS@0.1u/10V_4

ADDRESS: 32H

+3V_HDP Q32 *GS@2N7002 RP71 *GS@4.7KX2
(3,28) 2ND_MBDATA — KXP84_SDA

+3V_HDP Q31 *GS@2N7002
(3,28) 2ND_MBCLK — KXP84_SCL

+3V_HDP C474 *GS@0.1u/10V_4 C470 *GS@0.1u/10V_4

Close to Pin 7 and Pin 16

U31 *G691L308T73UF-SOT23
Vcc, Reset#, GND — +3V_HDP, G-RESET#

B2A
XIN_G C485 **GS@22p_6
Y4 **GS@8 MHz
XOUT_G C476 **GS@22p/50V_6

U33 *GS@LIS3L02AQ3

NC, Reserved, GND, VDD, Vouty, ST, Voutx

+3V_HDP C471 *GS@0.1u/10V_4

ACCELY, AXSTST, ACCELX, ACCELZ, FS, PD

+3V_HDP R437 **GS@10K_4
R440 *GS@10K_4

U34 *GS@R5F21174

VCC, VCC, ACCELX, ACCELY, ACCELZ, AXSTST, HDPACT, HDPPD, HDPINT, VSS
HDPSCL, HDPSDA, RESET, MODE, Reserved, GND, HD_PINT

KXP84_SCL, KXP84_SDA
G-RESET# R448 *GS@10K_4 R431 *GS@10K_4
XIN_G R444 *GS@10K_4
XOUT_G R438 *GS@10K_4

(16) HDPACT
(16) HDPINT
R432 *GS@1K_4
R435 *GS@47K/F_6

C492 *GS@33n/16V_4 C491 *GS@33n/16V_4 C481 *GS@33n/16V_4

Close Chipset

FS (Full Scale) selection

FS	0	1
	2g Full-Scale	6g Full-Scale

PD (Power Down) selection

PD	0	1
	Normal Mode	Power-down mode

HDPPD selection

HDPPD	0	1
	Normal Mode	Power-down mode

Quanta Computer Inc.

PROJECT : TE1

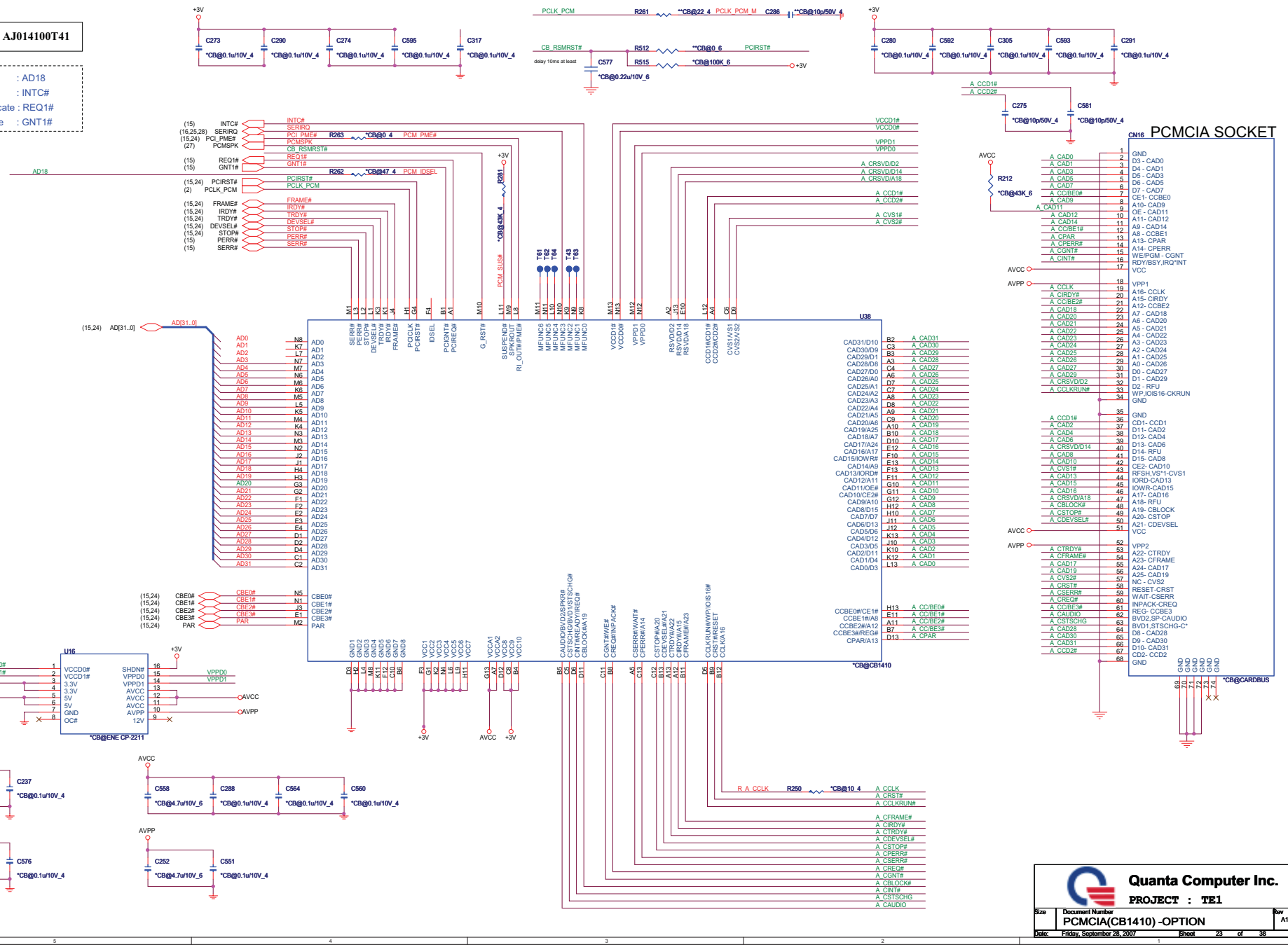
Size	Document Number	Rev
	SATA/PATA/G-SENSOR	A1A

Date: Sunday, September 30, 2007 Sheet 22 of 38

Cardbus

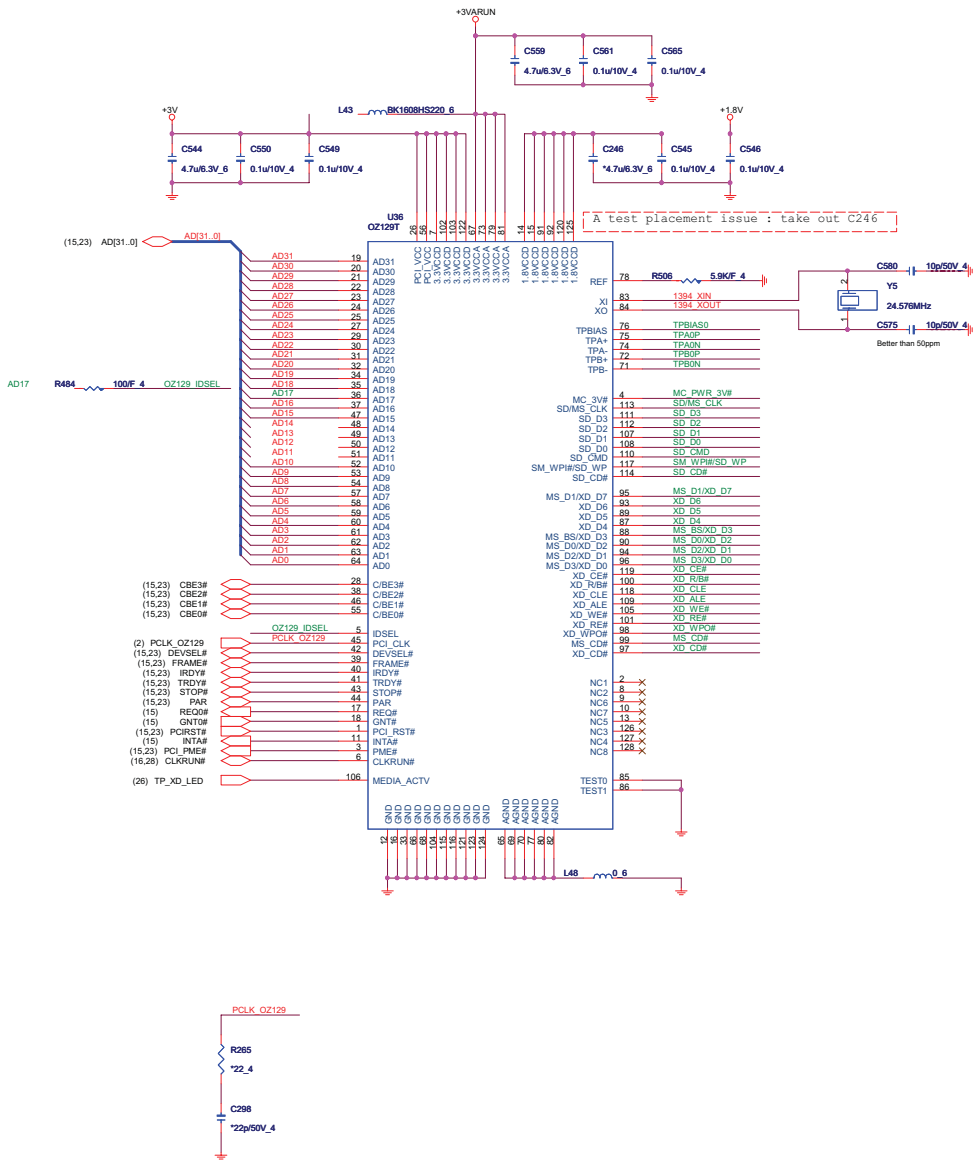
ENE1410	AJ014100T41

ID Select : AD18
Interrupt Pin : INTC#
Request Indicate : REQ1#
Grant Indicate : GNT1#

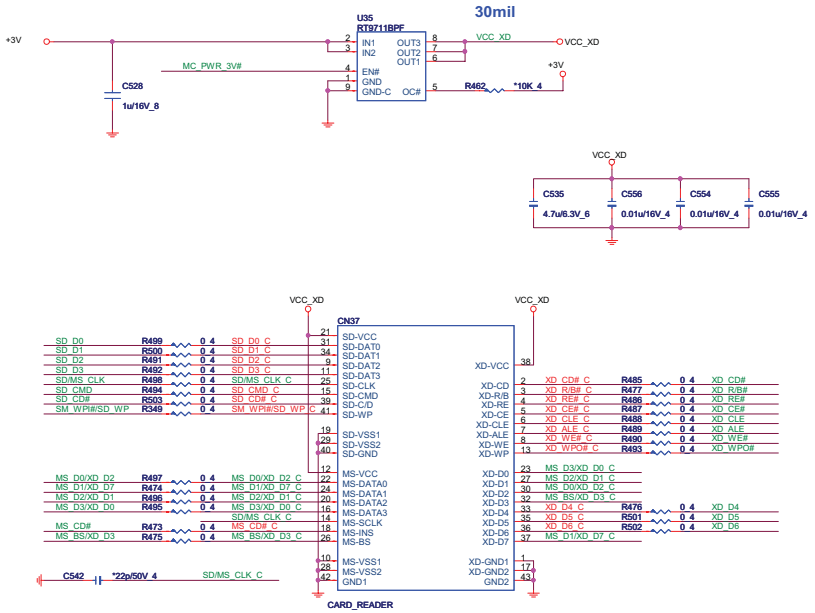


OZ129 for Cardreader+1394

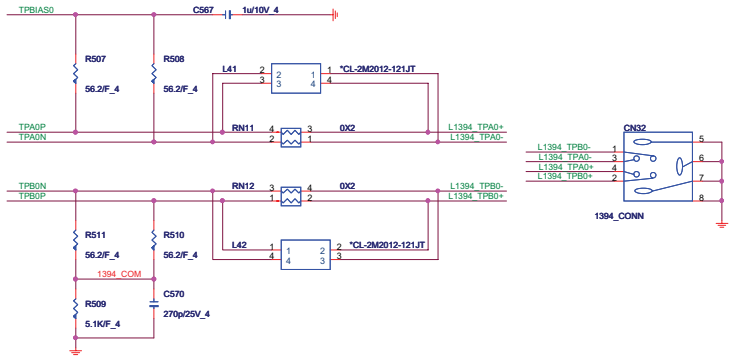
ID Select : AD17
Interrupt Pin : INTA#
Request Indicate : REQ0#
Grant Indicate : GNT0#



5 IN 1 Card reader



1394



Quanta Computer Inc.

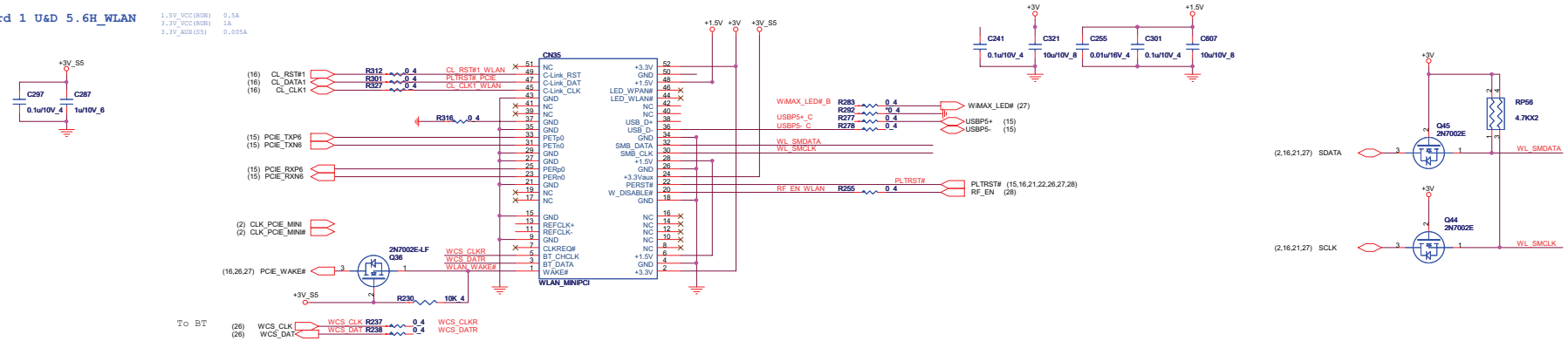
PROJECT : TE1

Size	Document Number	Rev
	OZ129T(5in1/1394)	A1A

Date: Friday, September 28, 2007 Sheet 24 of 38

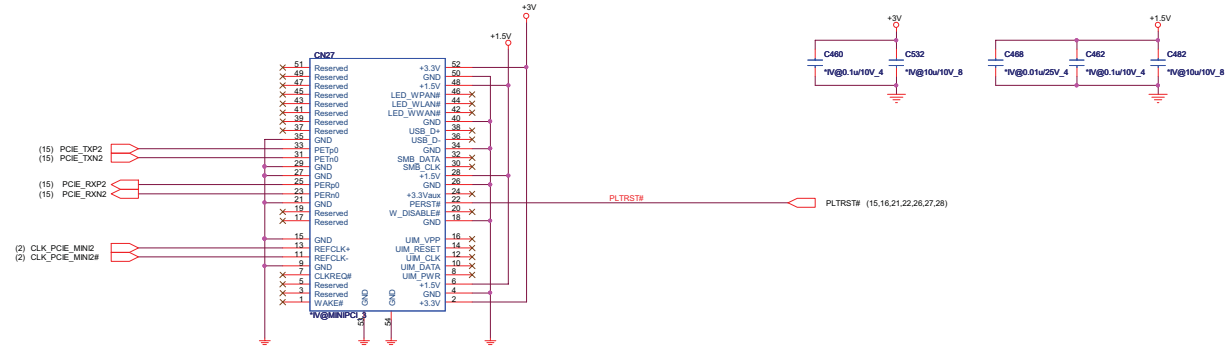
MINI Card 1 U&D 5.6H_WLAN

1.5V_VCC(RUN) 0.5A
3.3V_VCC(RUN) 1A
3.3V_AUX(S5) 0.005A



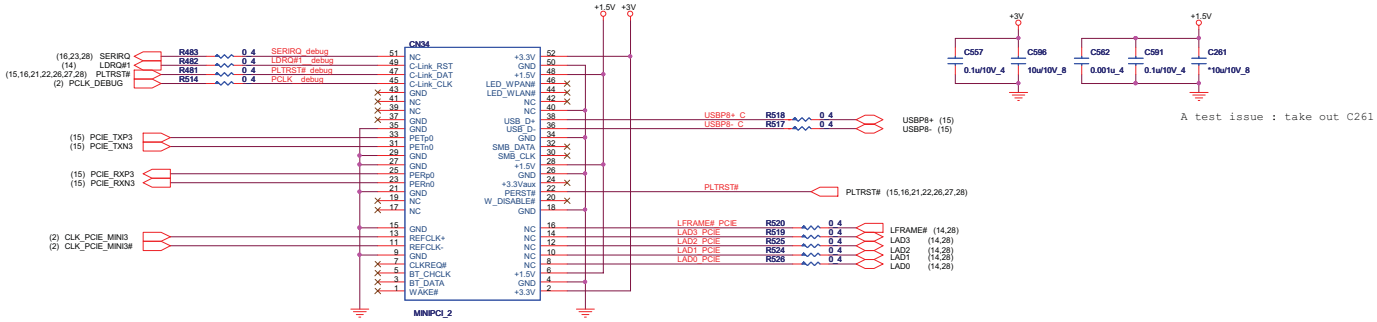
MINI Card 3 U 9H_HD-DVD

1.5V_VCC(RUN) 0.5A
3.3V_VCC(RUN) 1A



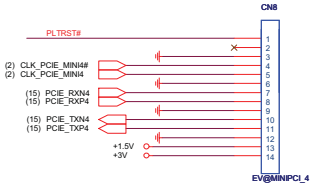
MINI Card 2
U 5.6H_TV/ROBOSON
D 7.5H_HD-DVD

1.5V_VCC(RUN) 0.5A
3.3V_VCC(RUN) 1A



A test issue : take out C261

MINI Card 4-D/Robson



Remark1:TV+Robson or HD-DVD+Robson or TV+HD-DVD for UMA SKU

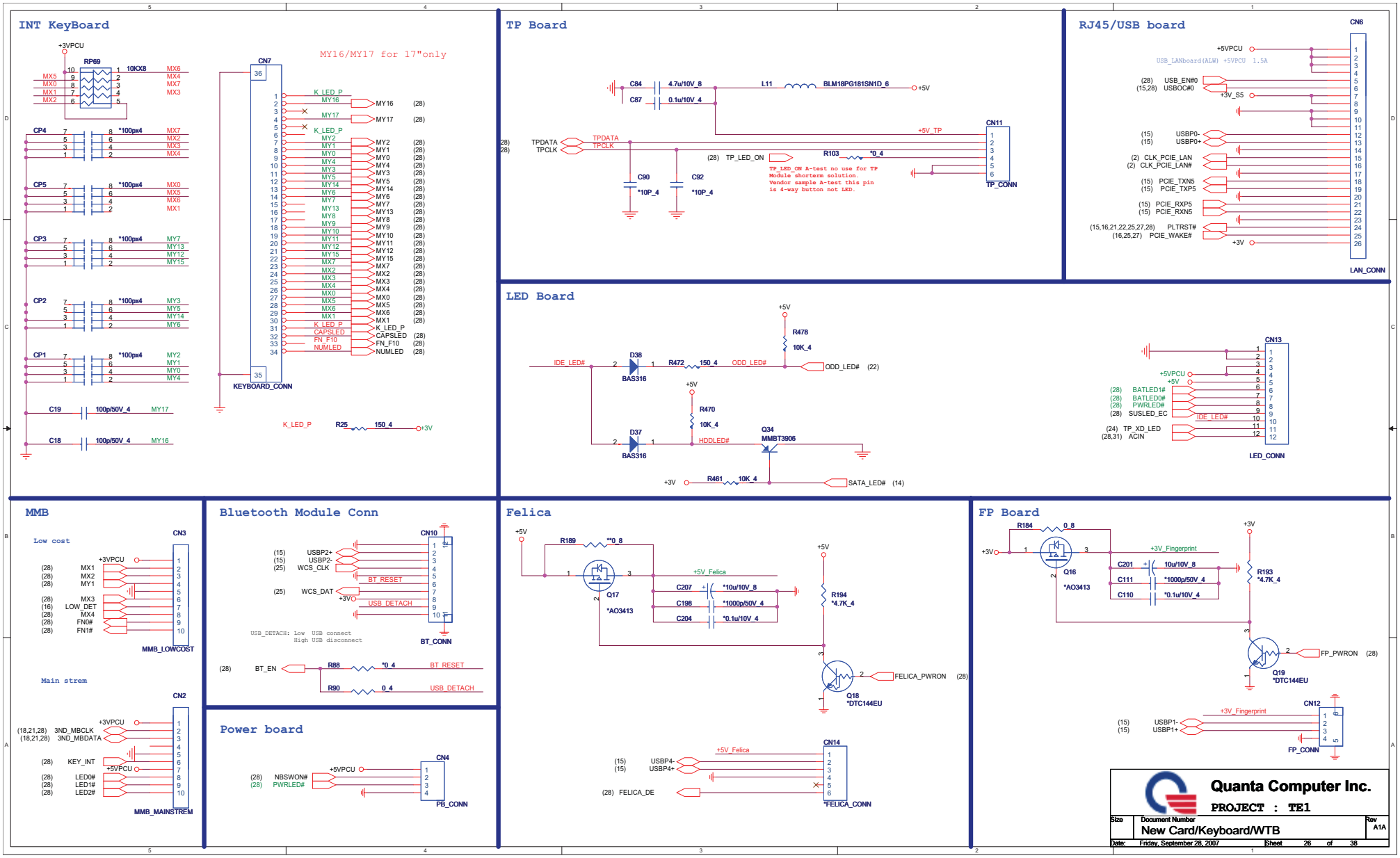
Remark2:TV is just for UMA(13")

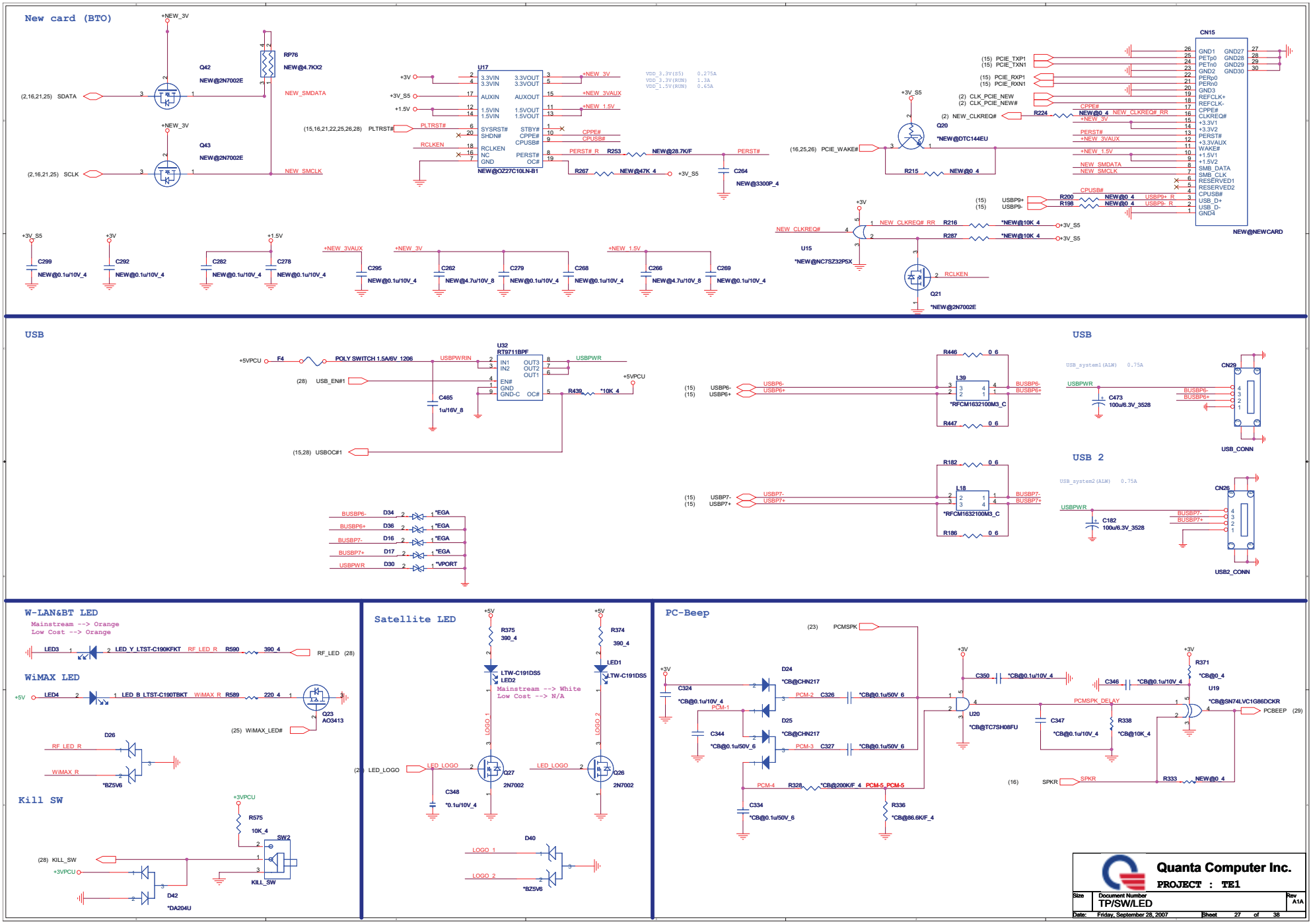
	UMA	Discrete
1	WLAN	WLAN
2	TV or Robson	HD-DVD
3	HD-DVD or Robson	N.C
4	N.C	Robson

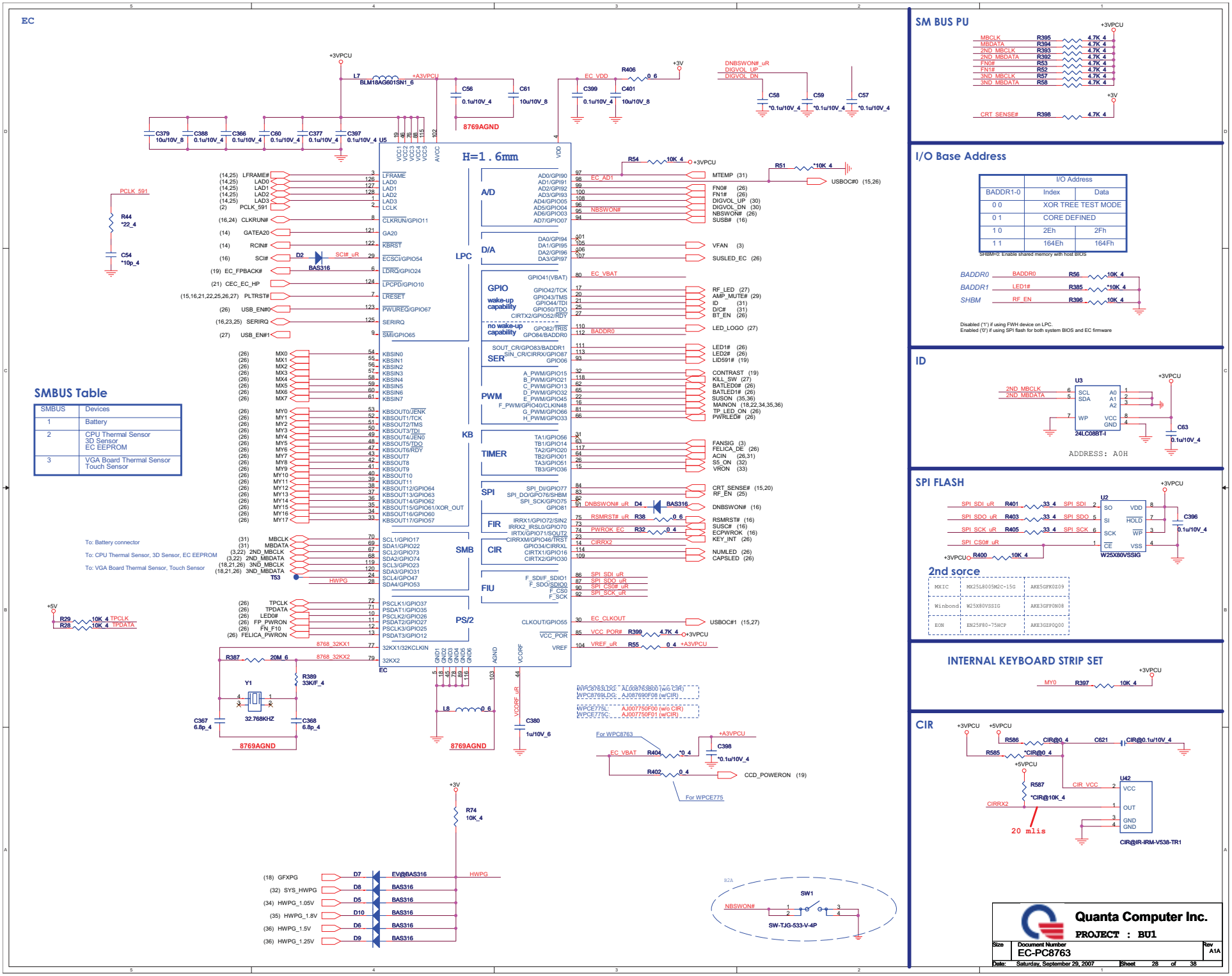
Quanta Computer Inc.
PROJECT : TE1

Size	Document Number	Rev
	MINI CARD	A1A

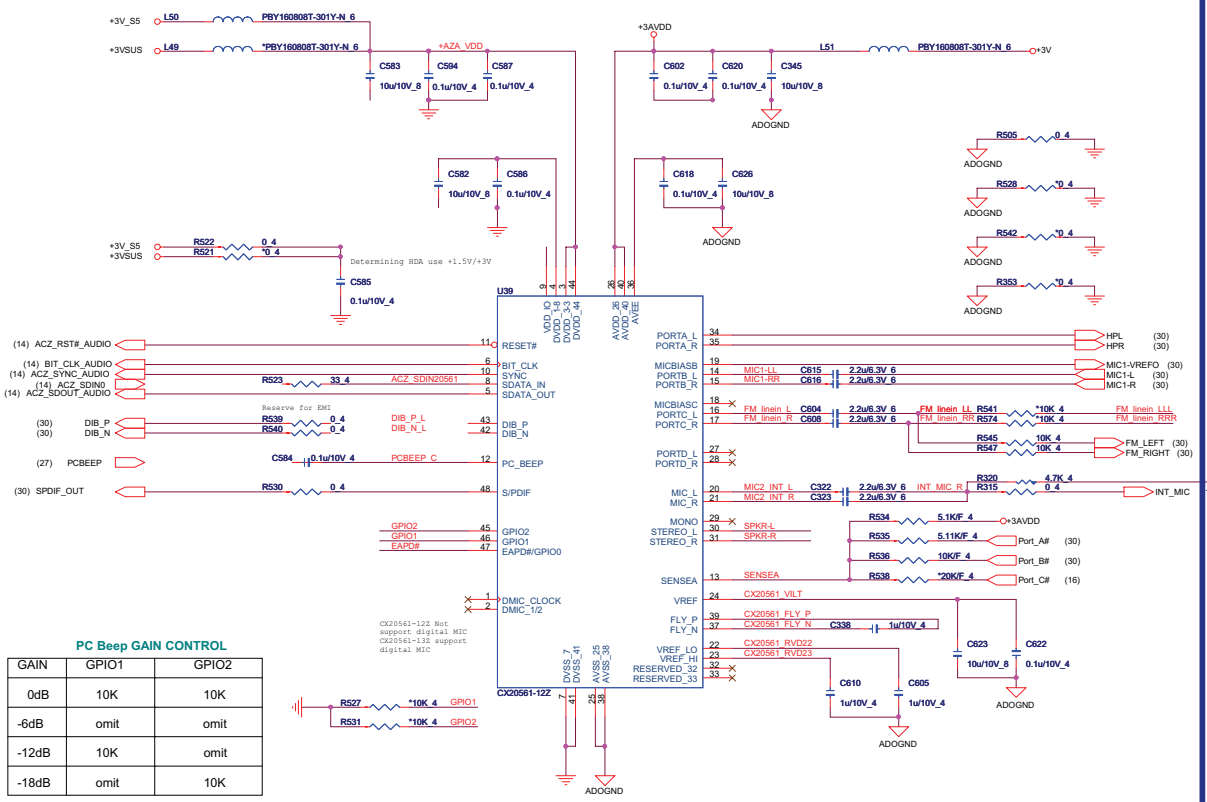
Date: Friday, September 28, 2007 Sheet 25 of 38







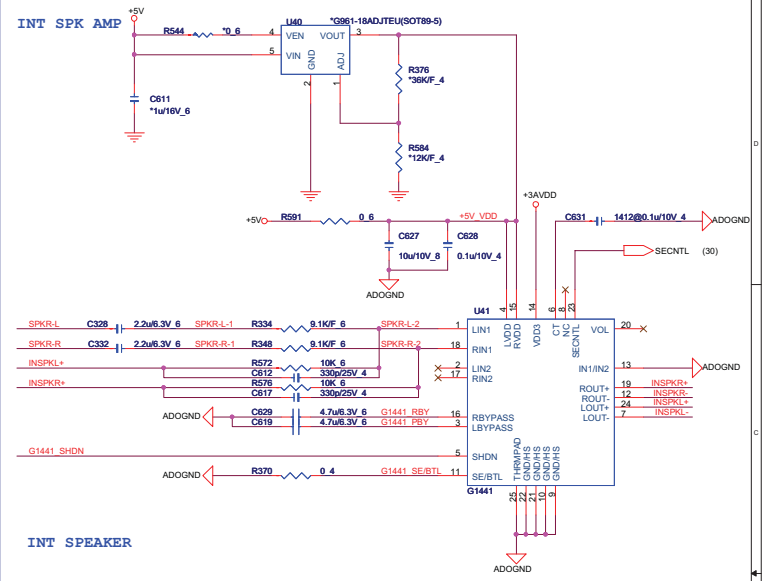
Codec (CX20561)



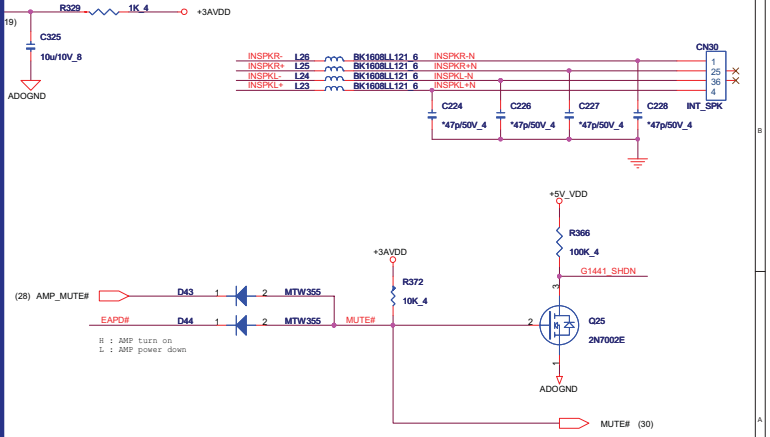
PC Beep GAIN CONTROL

GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

INT SPK AMP



INT SPEAKER



Reserve INTMIC

Reserve FM

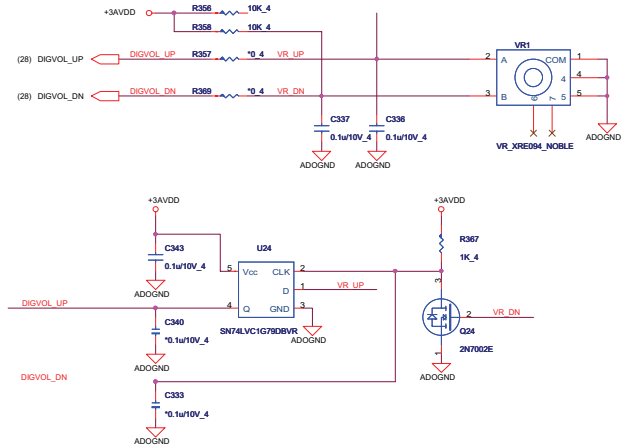
Quanta Computer Inc.

PROJECT : TE1

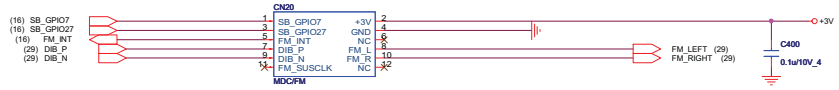
Size	Document Number	Rev
	Conexant CX205601	A1A

Date: Friday, September 28, 2007 Sheet 29 of 38

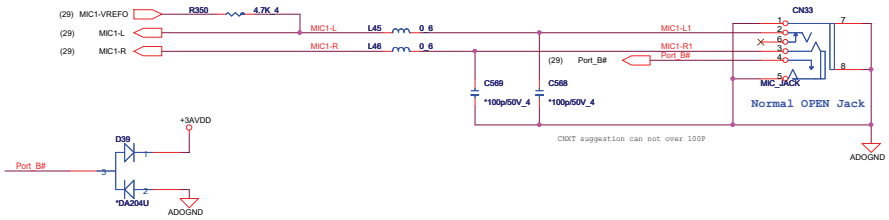
VR



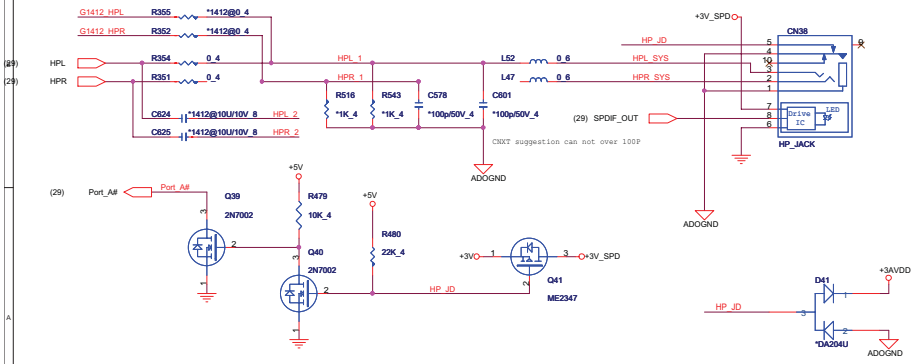
FM Tuner MDC



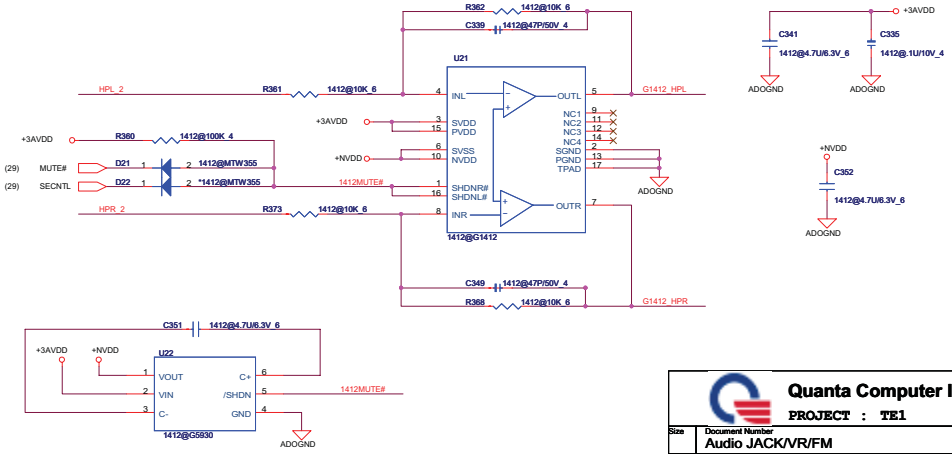
SYSTEM MIC



HP



HP Amplifier

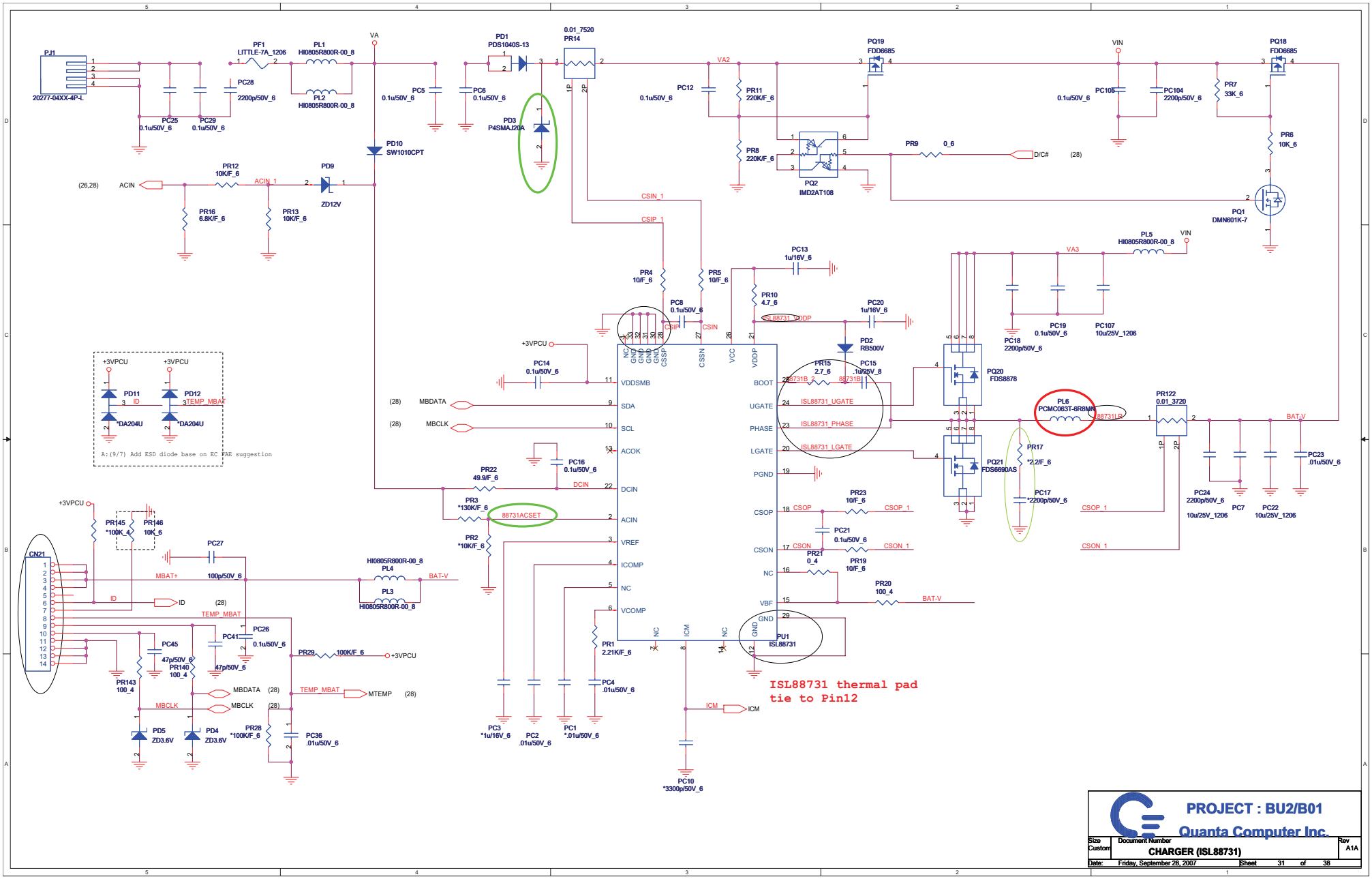


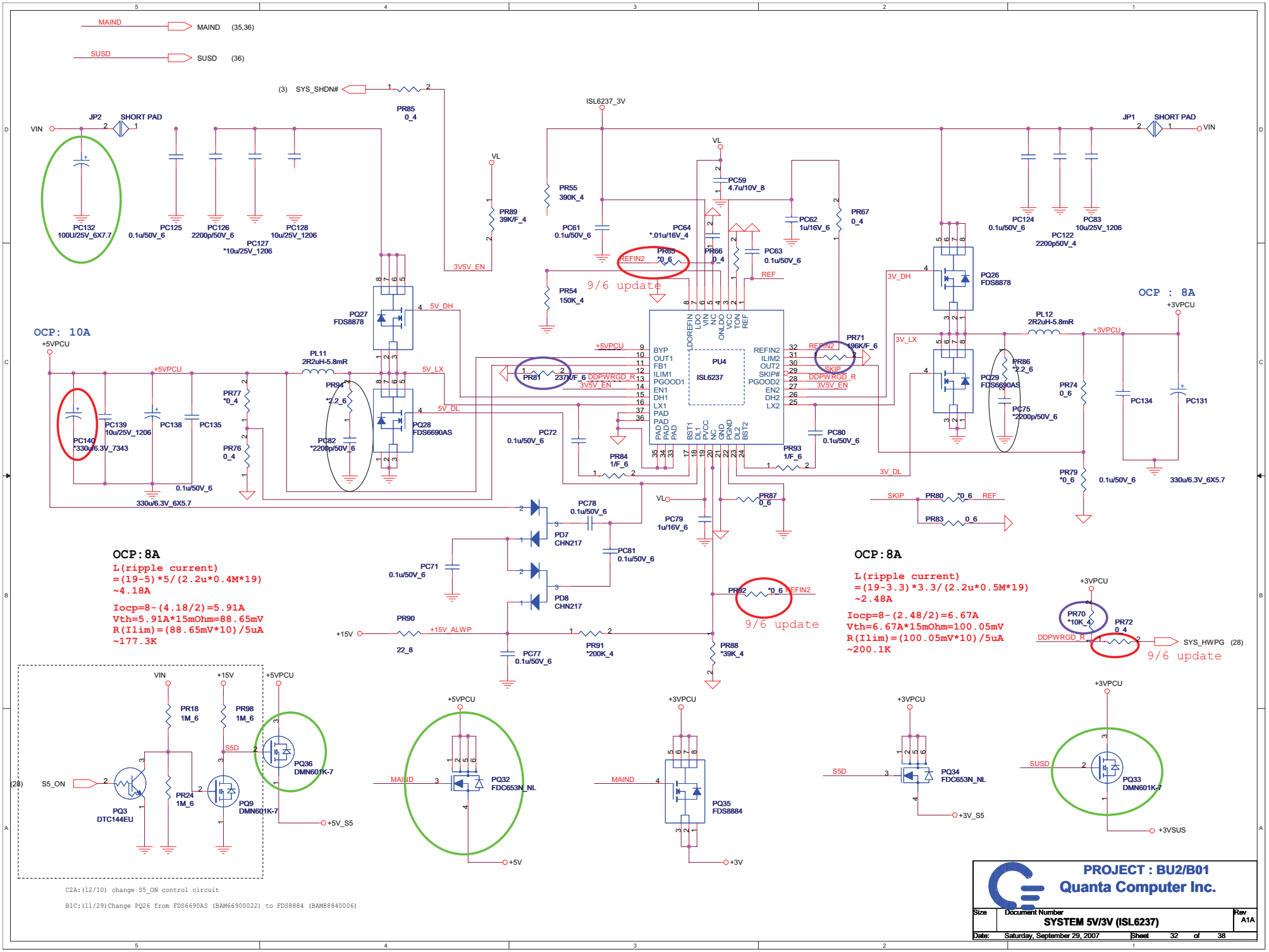
Quanta Computer Inc.

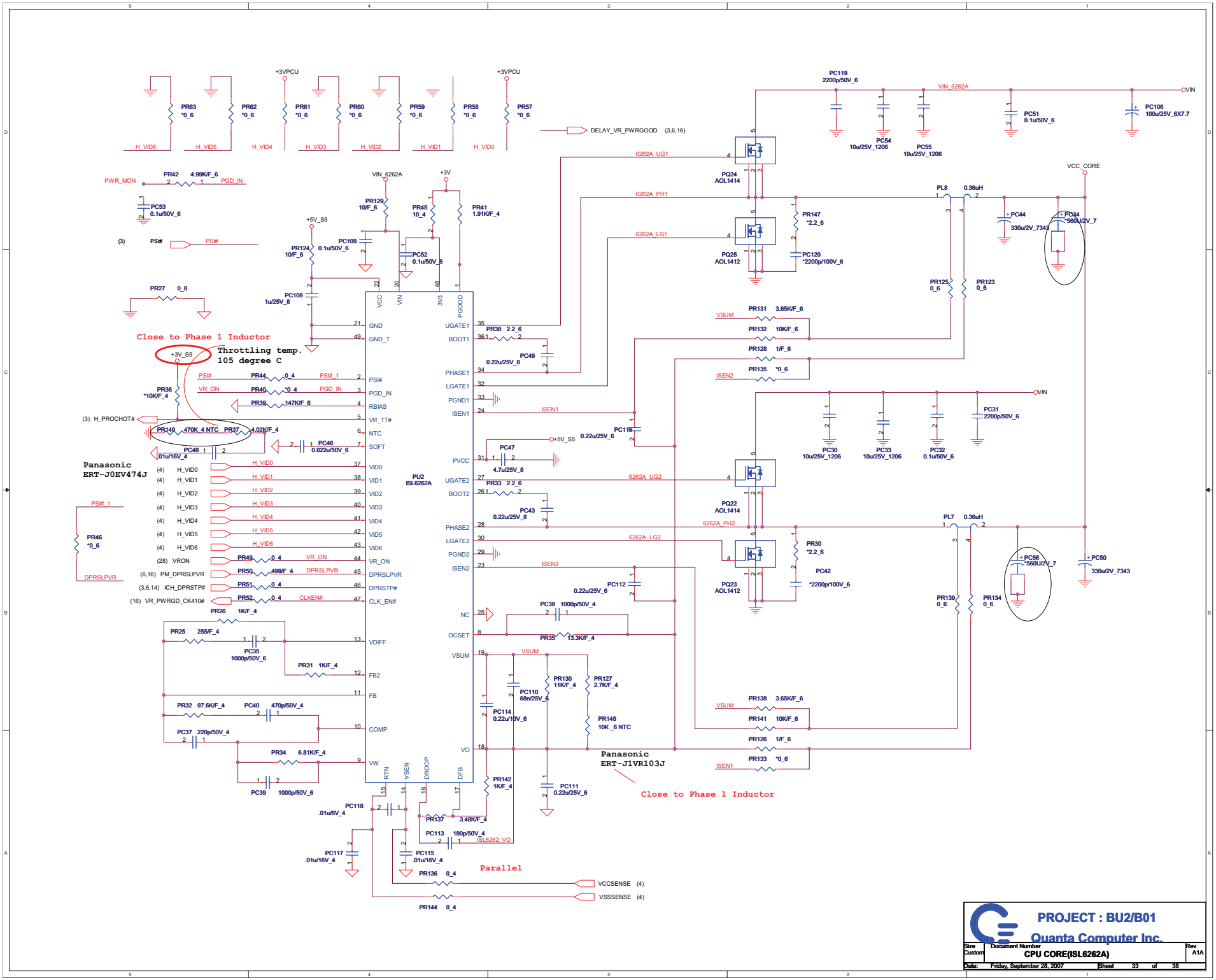
PROJECT : TE1

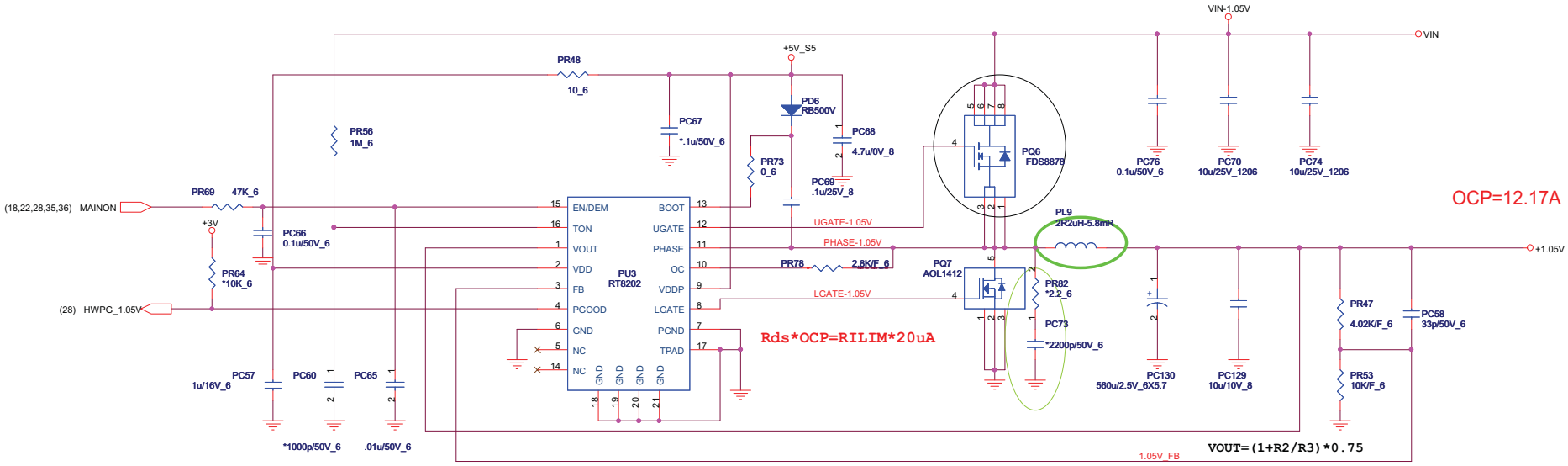
Size	Document Number	Rev
	Audio JACK/VR/FM	A1A

Date: Friday, September 28, 2007 Sheet 30 of 38









TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

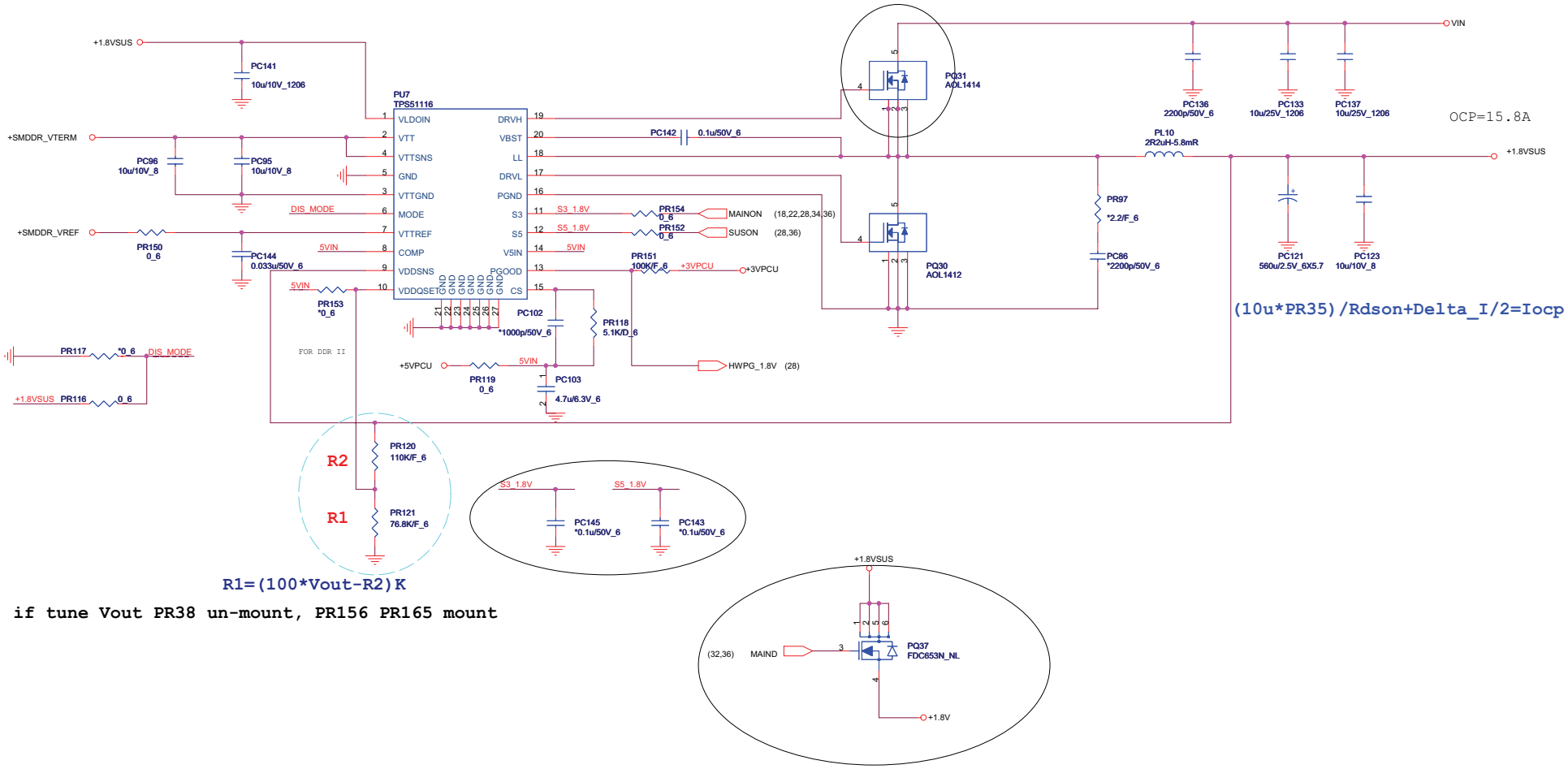
AO1412 Rds=4.6mOhm

12.17A OCP --- OC=2.8K(CS22803F914)

PROJECT : BU2/B01
Quanta Computer Inc.

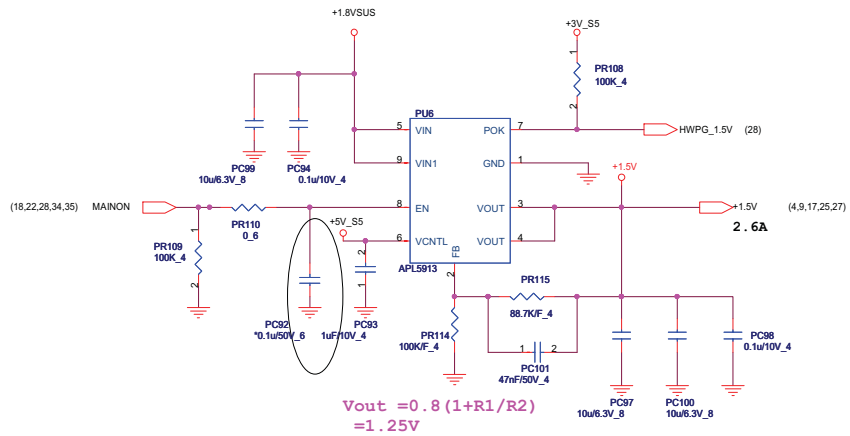
Size	Document Number	Rev
	VTT 1.05V (RT8202)	A1A

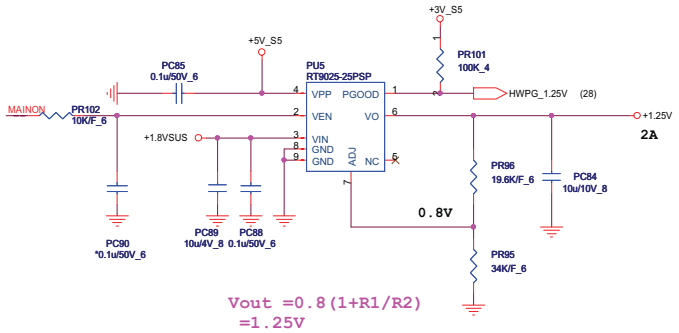
Date: Friday, September 28, 2007 Sheet 34 of 38

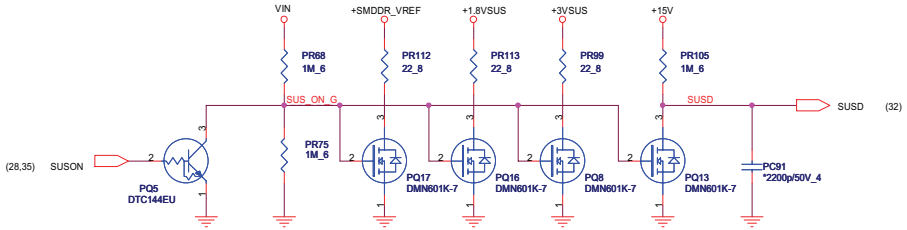


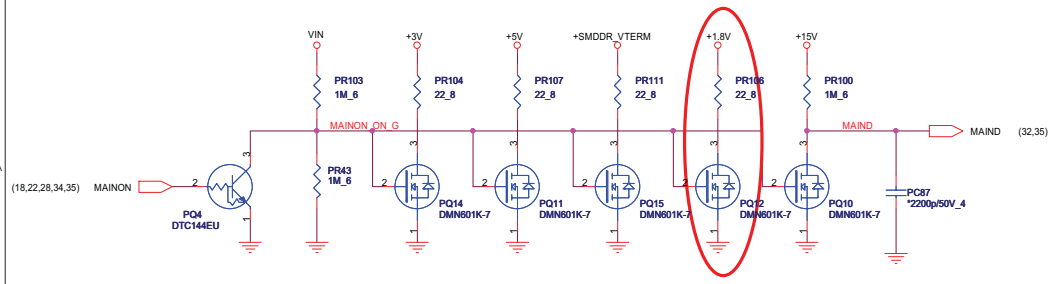
if tune Vout PR38 un-mount, PR156 PR165 mount

PROJECT : BU2/B01		
Quanta Computer Inc.		
Size	Document Number	Rev
	DDR 1.8V(TPS51116)	A1A
Date: Friday, September 28, 2007	Sheet 35 of 38	









PROJECT : BU2/B01

Quanta Computer Inc.

Size	Document Number	Rev
	Discharge (1.25V/1.5V)	A1A

Date: Friday, September 28, 2007 Sheet 36 of 38

Model	REV	DATE	CHANGE LIST	NOTE
TE1	01	20070824	FIRST RELEASED : 20070824	
	A1A	20070921	A-test RELEASED : 20070921	
	B2A		BA039040039 EOL, change to BA0390400H0	
			C353 change side to BOT	
			CH6102ME904 EOL change to CH6102M1909	
			Stuff SW1 of DHPTJG53336	
			Change U34 of AL021174C00 to AR0BU1R0000	
			PC82 apply * at Part Number	
			Always reserve Y4, C476 and C485 if Gsensor function on used	
			Stuff R81	
			Always reserve C9 and R10 from Power modify if LED panel on used.	

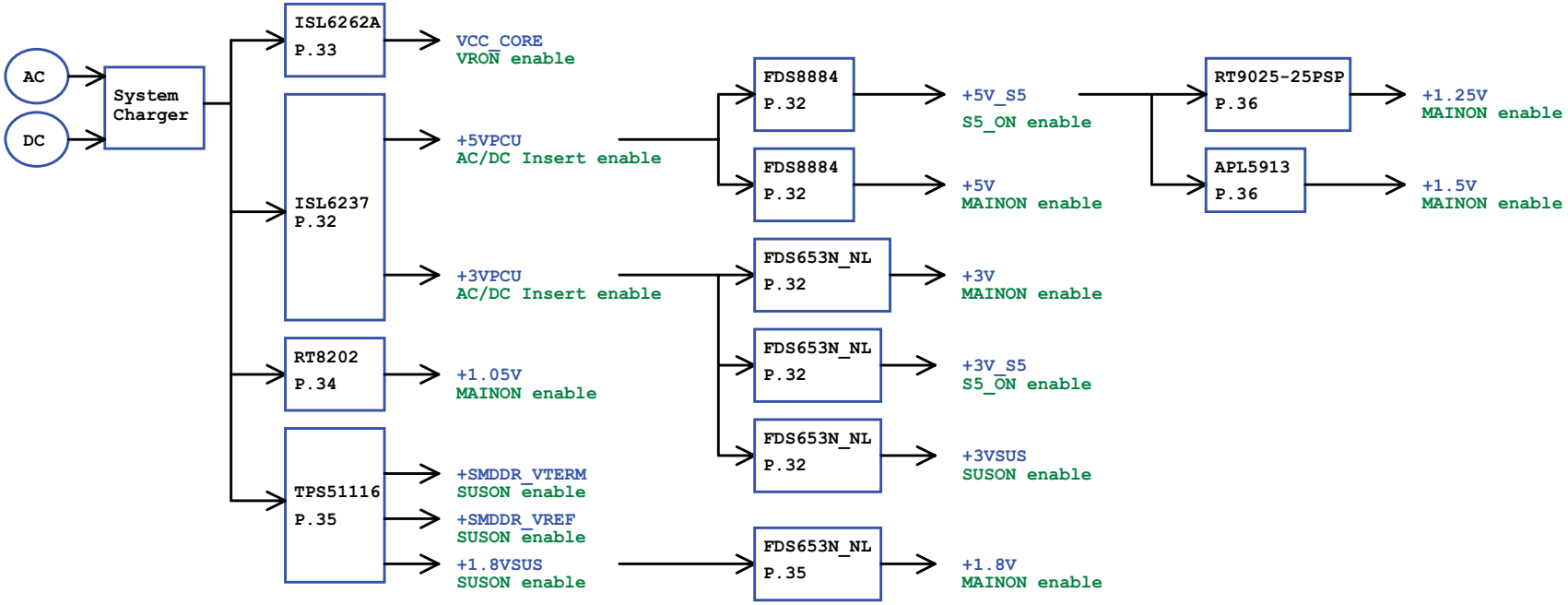
Quanta Computer Inc.

PROJECT : TE1

Size	Document Number	Rev
	Change list	1A

Date: Saturday, September 29, 2007 Sheet 37 of 38

Power Tree Table



Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+1.8VSUS	GMCH, DDR
+SMDDR_VREF	GMCH, DDR
+SMDDR_VTERM	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T) Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	HDMI, Cardreader (OZ129T)
+1.25V	CLK, GMCH, ICH8M

Quanta Computer Inc.
PROJECT : TE1

Size	Document Number	Rev
	Power Tree Table	1A

Date: Monday, September 10, 2007 Sheet 38 of 38