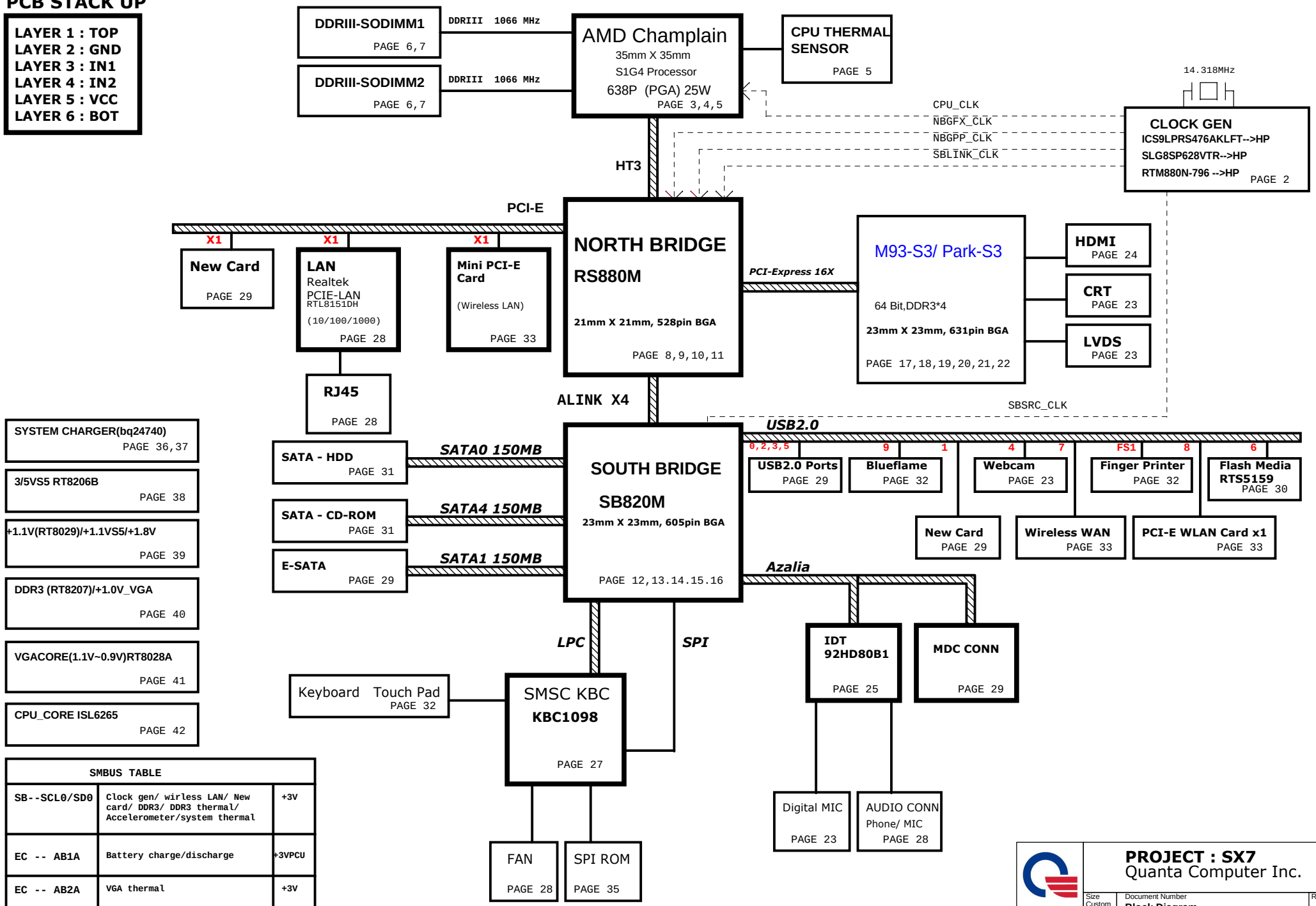
# SX7 SYSTEM DIAGRAM

AMD Smarter Choice

01

## PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT




| SMBUS TABLE | | |
|---|---|---|
| SB--SCL0/SD0 | Clock gen/ wirless LAN/ New card/ DDR3/ DDR3 thermal/ Accelerometer/system thermal | +3V |
| EC -- AB1A | Battery charge/discharge | +3VPCU |
| EC -- AB2A | VGA thermal | +3V |

NB5/RD2

**PROJECT : SX7**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Block Diagram | 3A |

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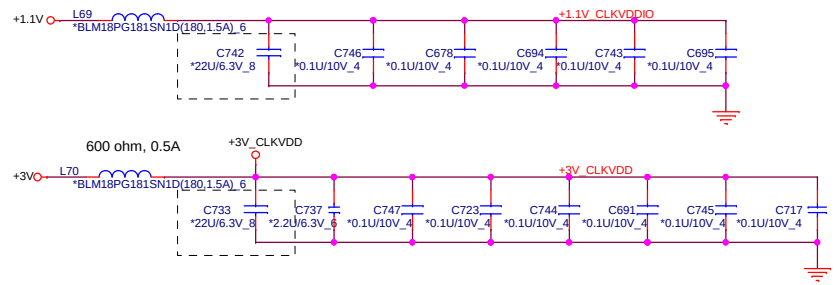
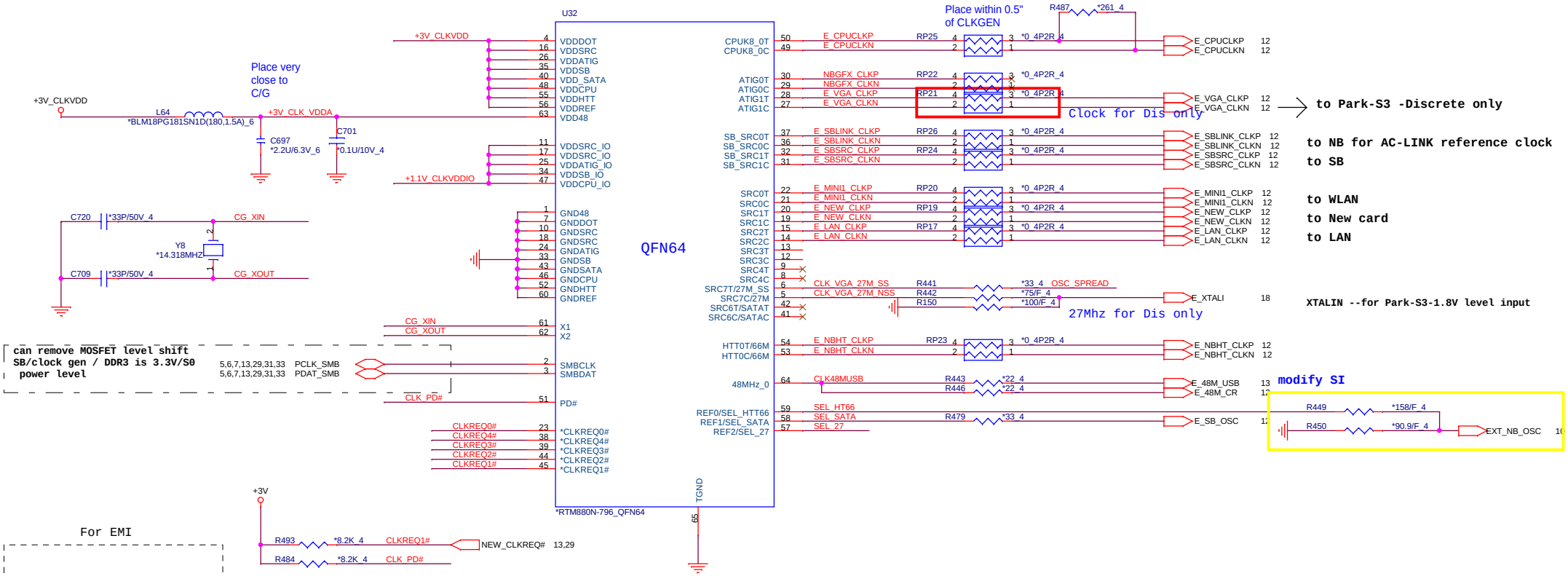
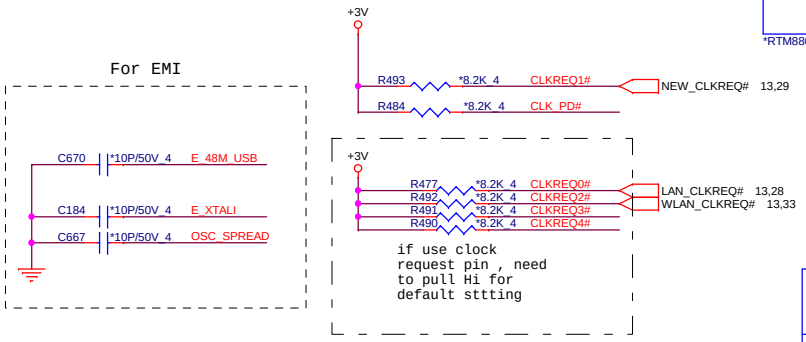
| CLOCKS name | Discrete | Clock pin function |
|---|---|---|
| NBGFX_CLKP<br>NBGFX_CLKN | NA | to NB for VGA reference clock |
| EXT_GFX_CLKP<br>EXT_GFX_CLKN | RP21 STUFF | to Park-S3 external reference clock -Discrete only |
| SBLINK_CLKP<br>SBLINK_CLKN | RP26 STUFF | to NB for AC-LINK reference clock |
| CLK_VGA_27M_SS<br>CLK_VGA_27M_NSS | R441, R442<br>STUFF | To Park-S3 27Mhz - Discrete only |




Need check the net name for the short pad

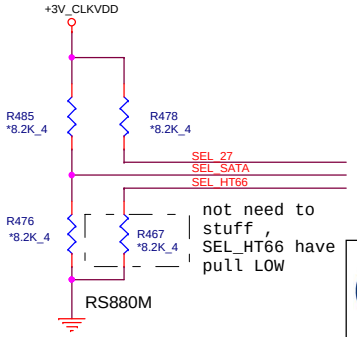



IDT ICS9LPRS480AKLFT--ALPRS480000
SLG SLG8SP628VTR--AL8SP628000
RTL RTM880N-796-- AL000880001

* default

| | | |
|---|---|---|
| SEL_HTT66 | 1 | 66 MHz 3.3V single ended HTT clock |
| | 0* | 100 MHz differential HTT clock |
| SEL_SATA | 1 | 100 MHz non-spreading differential SRC clock |
| | 0* | 100 MHz spreading differential SRC clock |
| SEL_27 | 1* | 27MHz non-spreading singled clock |
| | 0 | 100 MHz spreading differential SRC clock |




Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

NB5/RD2

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Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Clock Generator | 3A |

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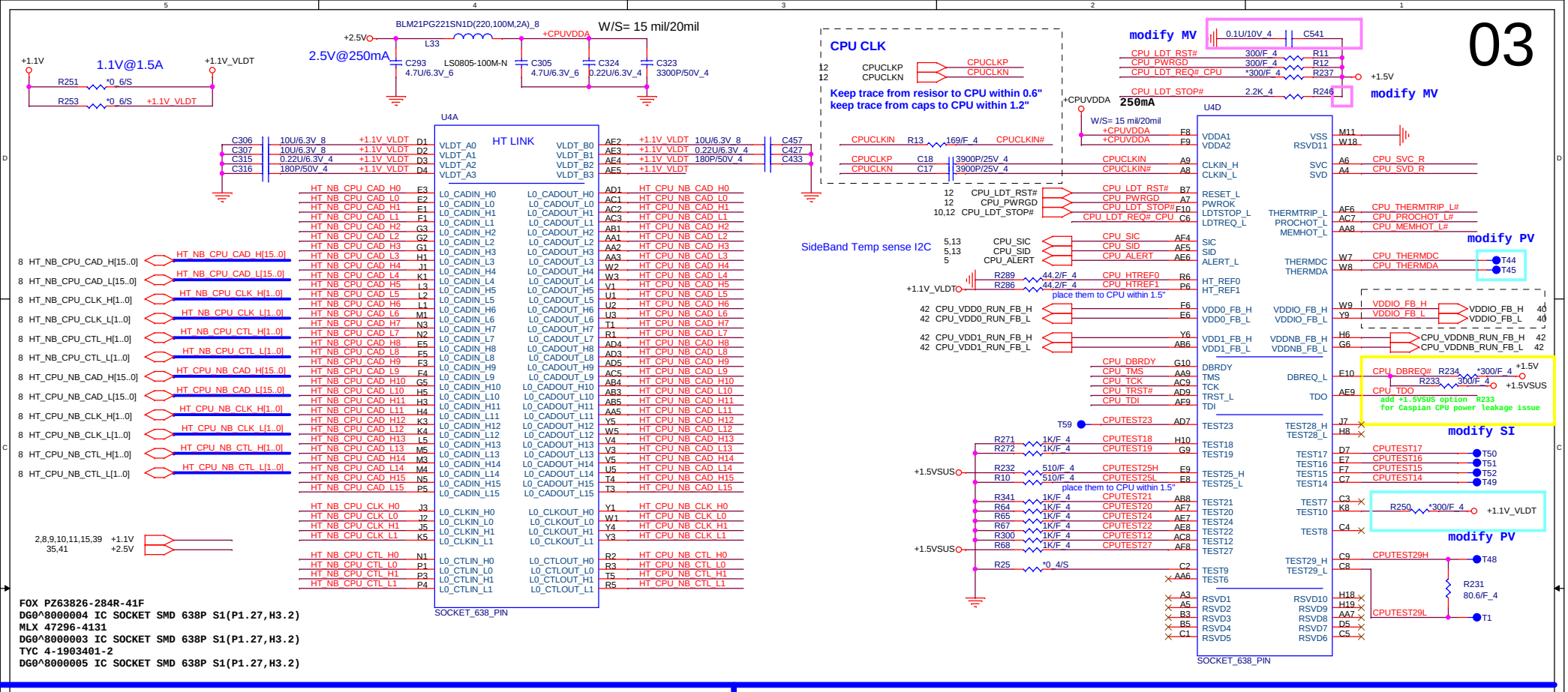
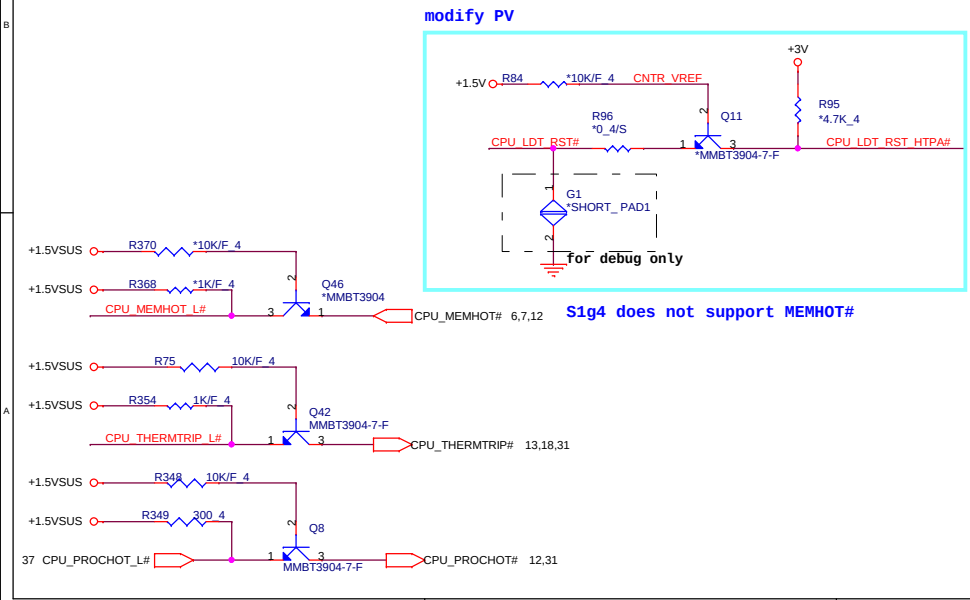
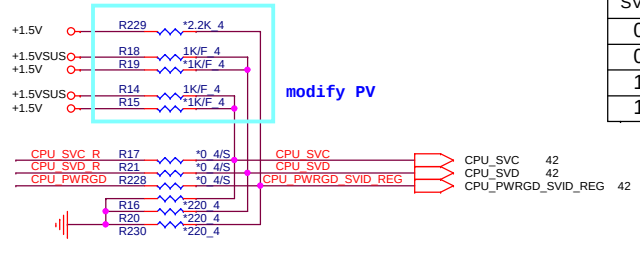



## Serial VID

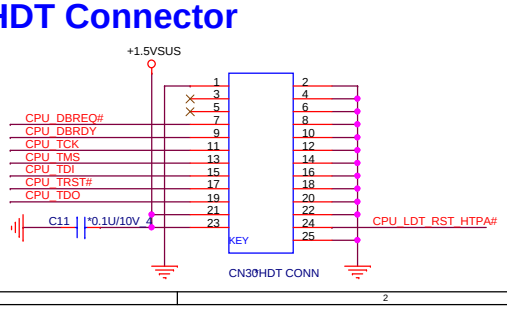
add +1.5VSUS option
R18 R14 for Caspian CPU
power leakge issue




VFIX MODE — VID Override Circuit

| SVC | SVD | Voltage Output |
|---|---|---|
| 0 | 0 | 1.1V |
| 0 | 1 | 1.0V |
| 1 | 0 | 0.9V |
| 1 | 1 | 0.8V |

## HDT Connector

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| Size | Document Number | Rev |
|---|---|---|
| Custom | S1G2 HT,CTL I/F 1/3 | 3A |

Date: Monday, March 15, 2010 Sheet 3 of 43

# Processor Memory Interface

04

0.9V@1.5A

PLACE THEM CLOSE TO CPU WITHIN 1"

modify PV

U4B

MEM:CMD/CTRL/CLK

SOCKET_638_PIN

U4C

MEM:DATA

SOCKET_638_PIN

Place close to socket

3,5,6,7,40,41,42 +1.5VSUS
6,40 +0.75VSMVREF
41 +0.9V

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NB5/RD2

| Size | Document Number | Rev |
|---|---|---|
| Custom | S1G2 DDRII MEMORY I/F 2/3 | 3A |

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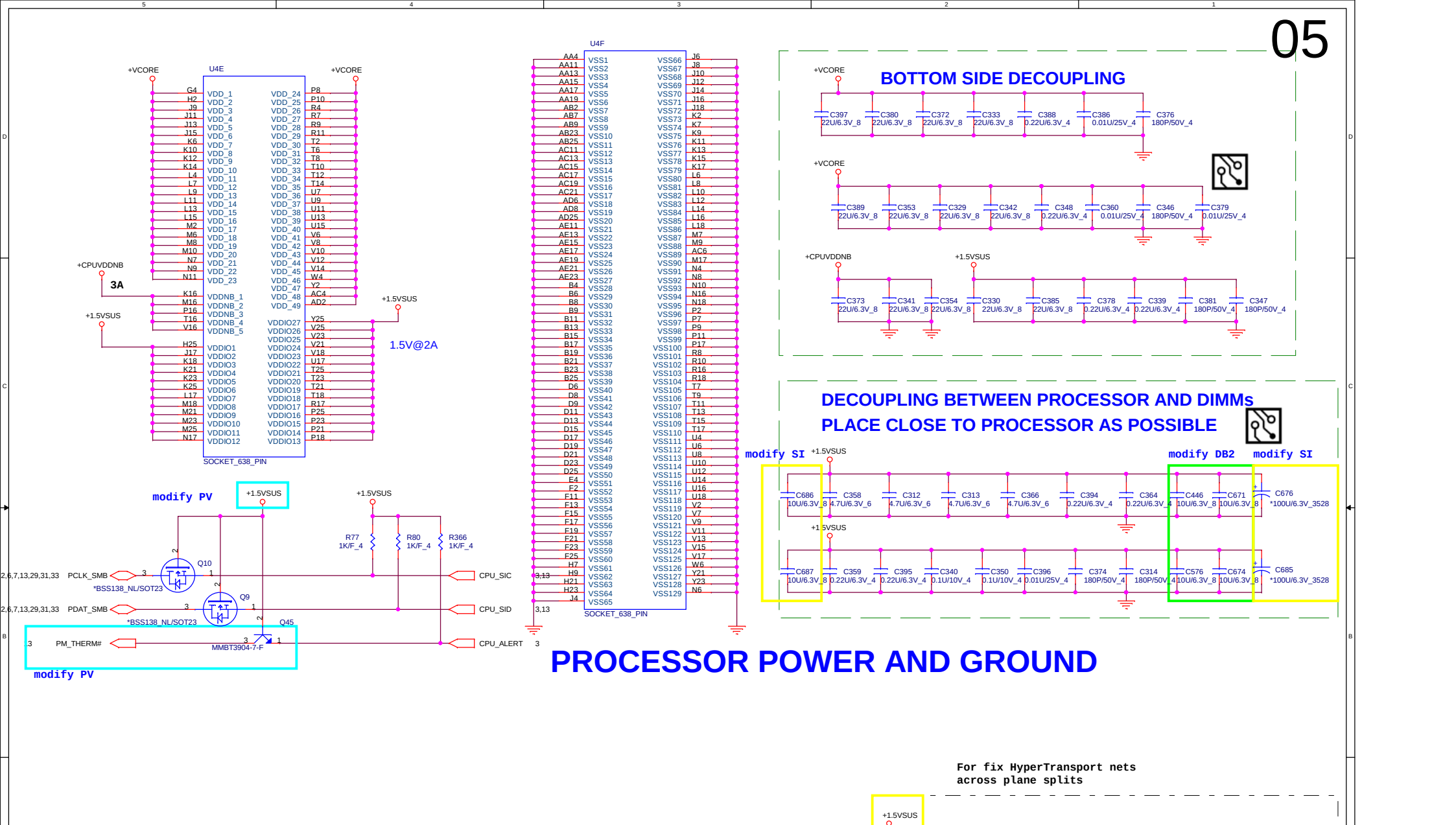


# PROCESSOR POWER AND GROUND

**PROJECT : SX7**
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| Size | Document Number | Rev |
|---|---|---|
| Custom | S1G2 PWR & GND 3/3 | 3A |

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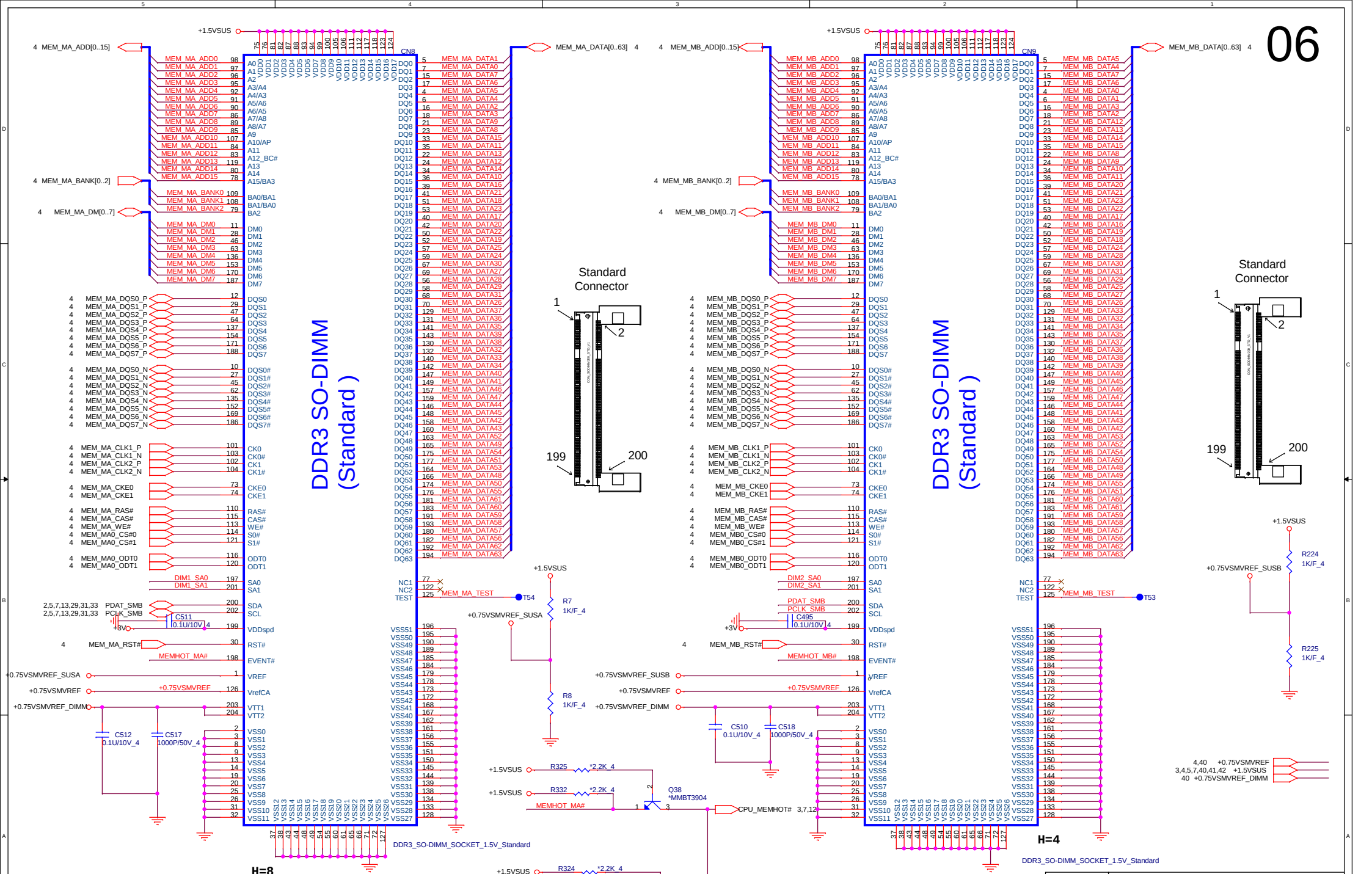


**PROJECT : SX7**
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NB5/RD2

| Size | Document Number | Rev |
|---|---|---|
| Custom | DDR2 SODIMMS: A/B CHANNEL | 3A |

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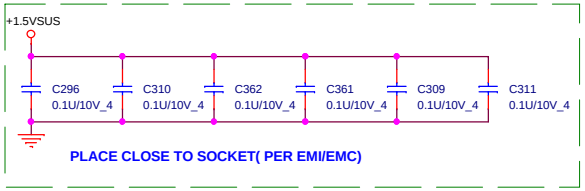
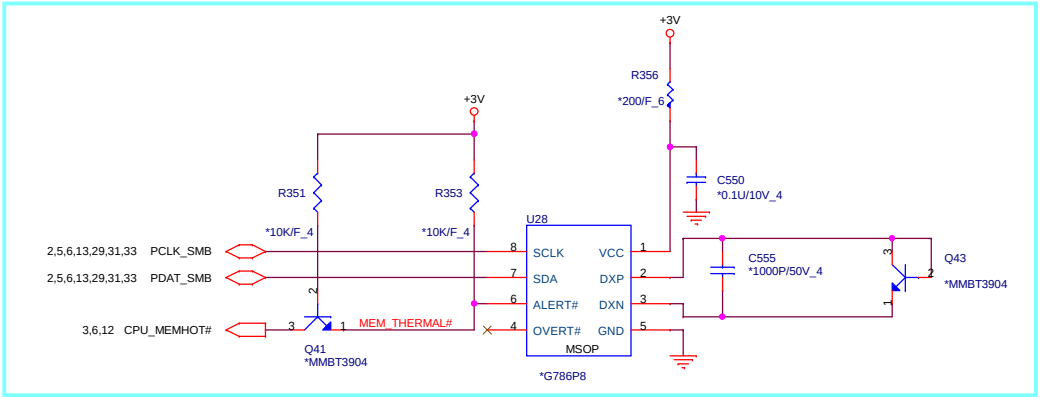



**modify PV**




**PROJECT : SX7**
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| Size | Document Number | Rev |
|---|---|---|
| Custom | DDR2 SODIMMS TERMINATIONS | 3A |

NB5/RD2

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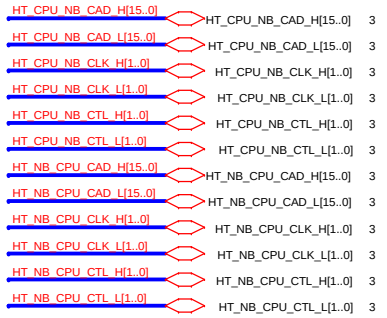
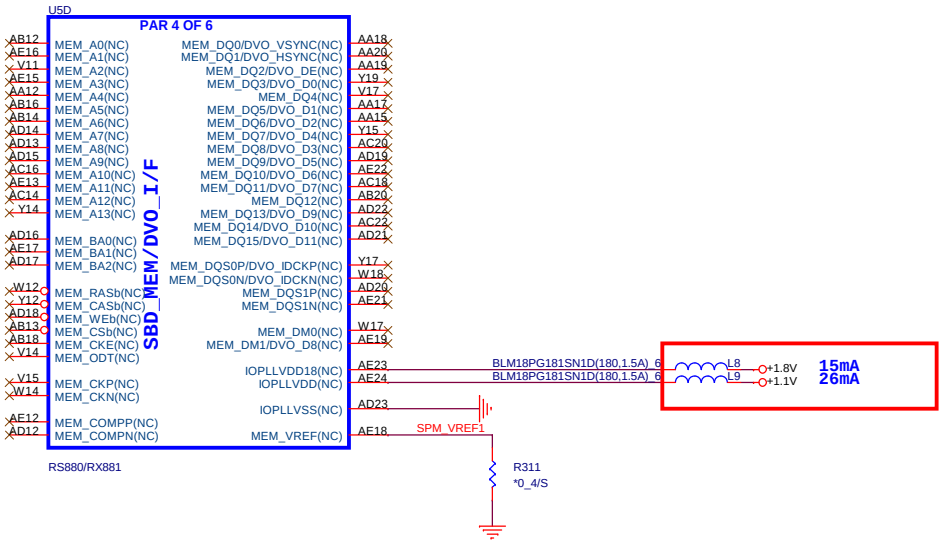



| signals | RS880M |
|---|---|
| HT_TXCALP | R430<br>301 ohm 1% |
| HT_TXCALN | |
| HT_RXCALP | R434<br>301 ohm 1% |
| HT_RXCALN | |

**This block is for UMA only , Discrete can remove all component**




**PROJECT : SX7**
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| Size | Document Number | Rev |
|---|---|---|
| Custom | RS880M-HT LINK I/F 1/5 | 3A |

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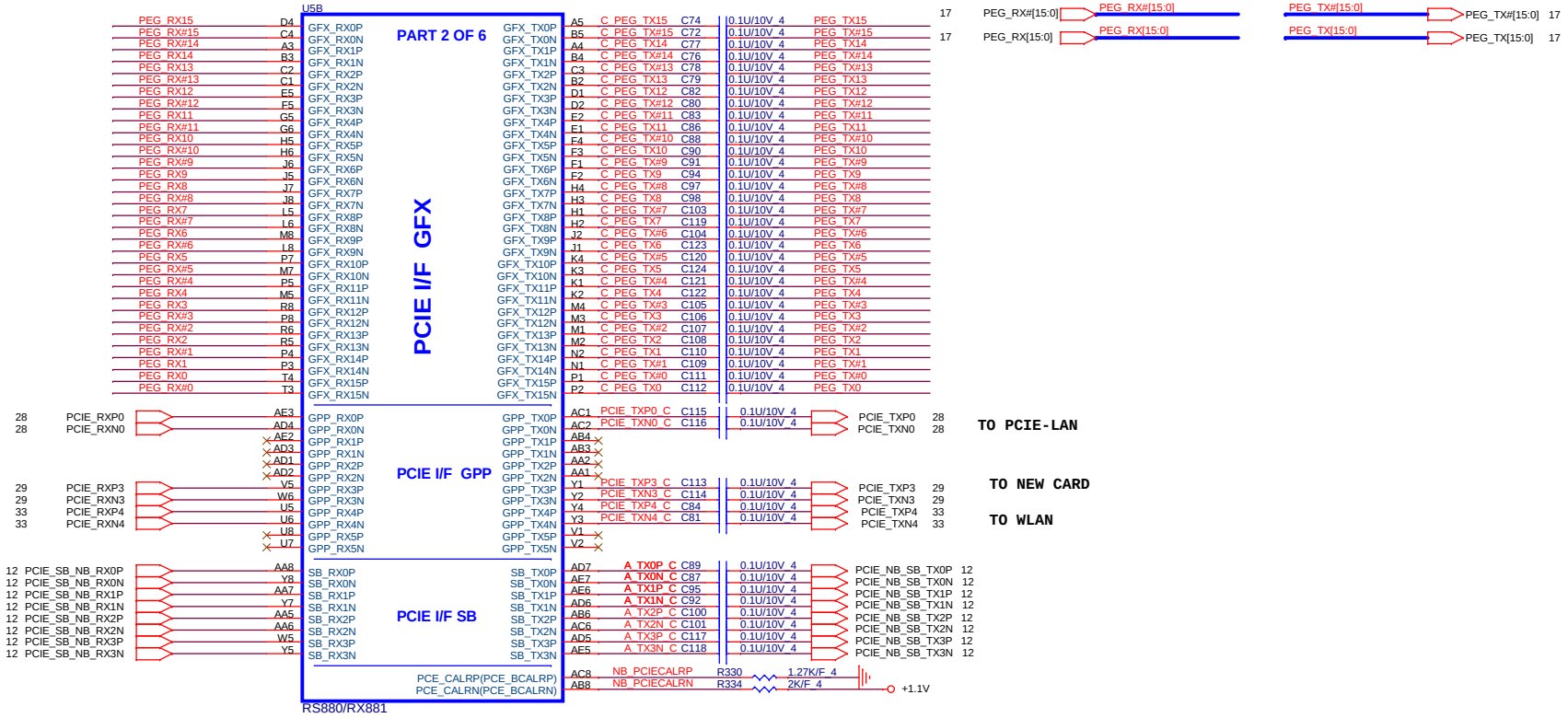
NB5/RD2




NB5/RD2

**PROJECT : SX7**
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| Size | Document Number | Rev |
|---|---|---|
| Custom | **RS880M-PCIE I/F 2/5** | 3A |

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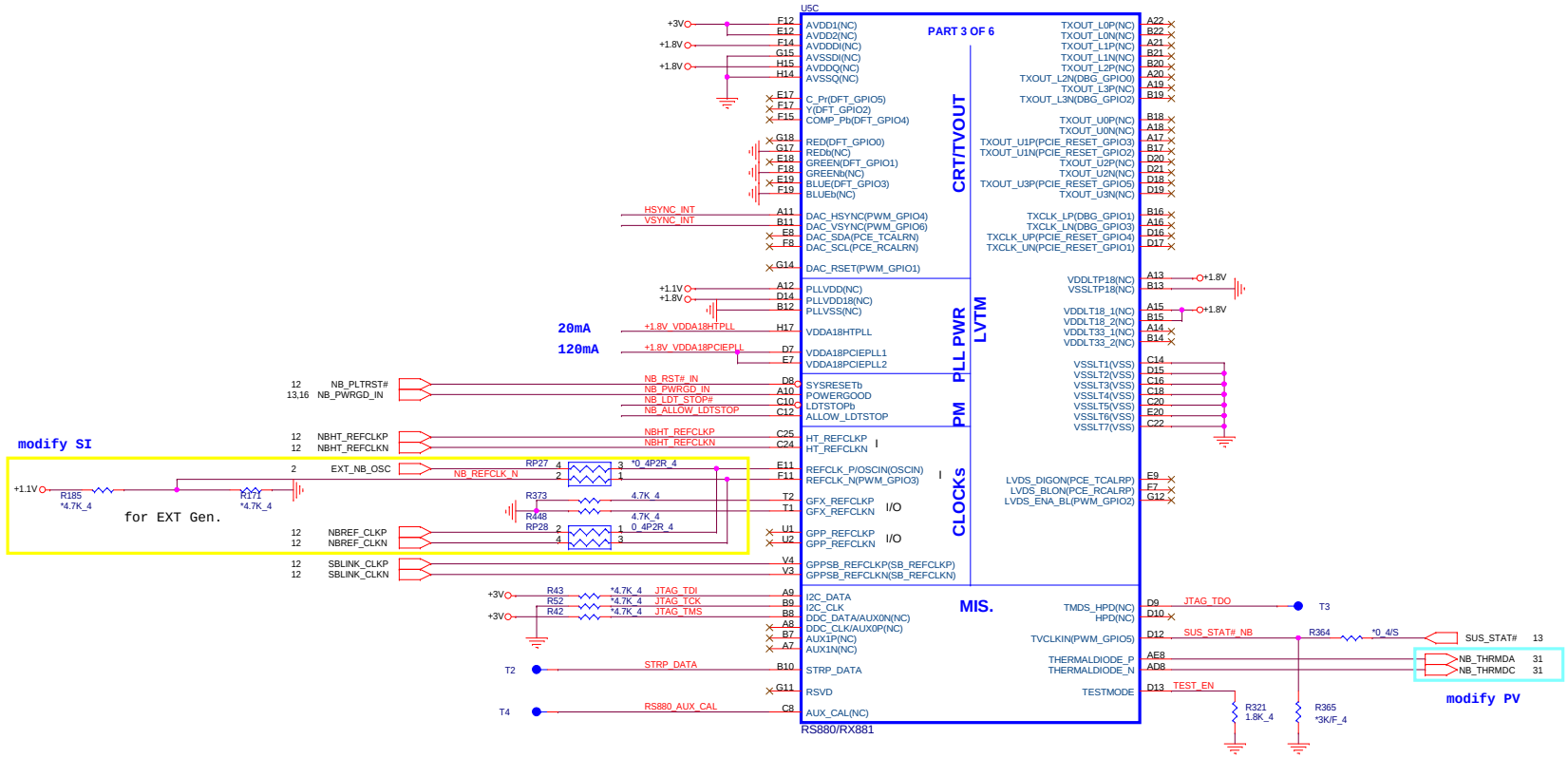
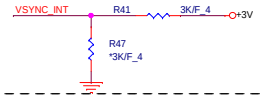


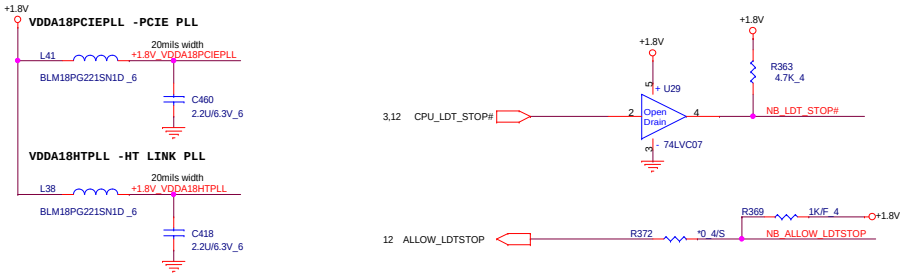

Enables Debug Bus acess
through memory I/O pads and GPIO.
0 : Enable RS880M , Default
1 : Disable RS880M
(RX881 use DAC_VSYNC)

**Discrete**




Indicates if memory Side port
is available or not
0: Reserved
1: Required setting. Select with a pull-up
resistor on the strap
( RX881 use DAC_HSYNC)

**Discrete**


NB5/RD2

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| Size | Document Number | Rev |
|---|---|---|
| Custom | RS880M-SYSTEM I/F 3/5 | 3A |

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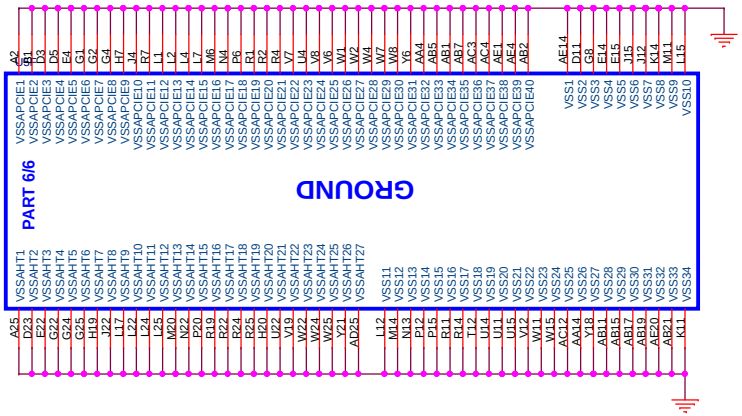
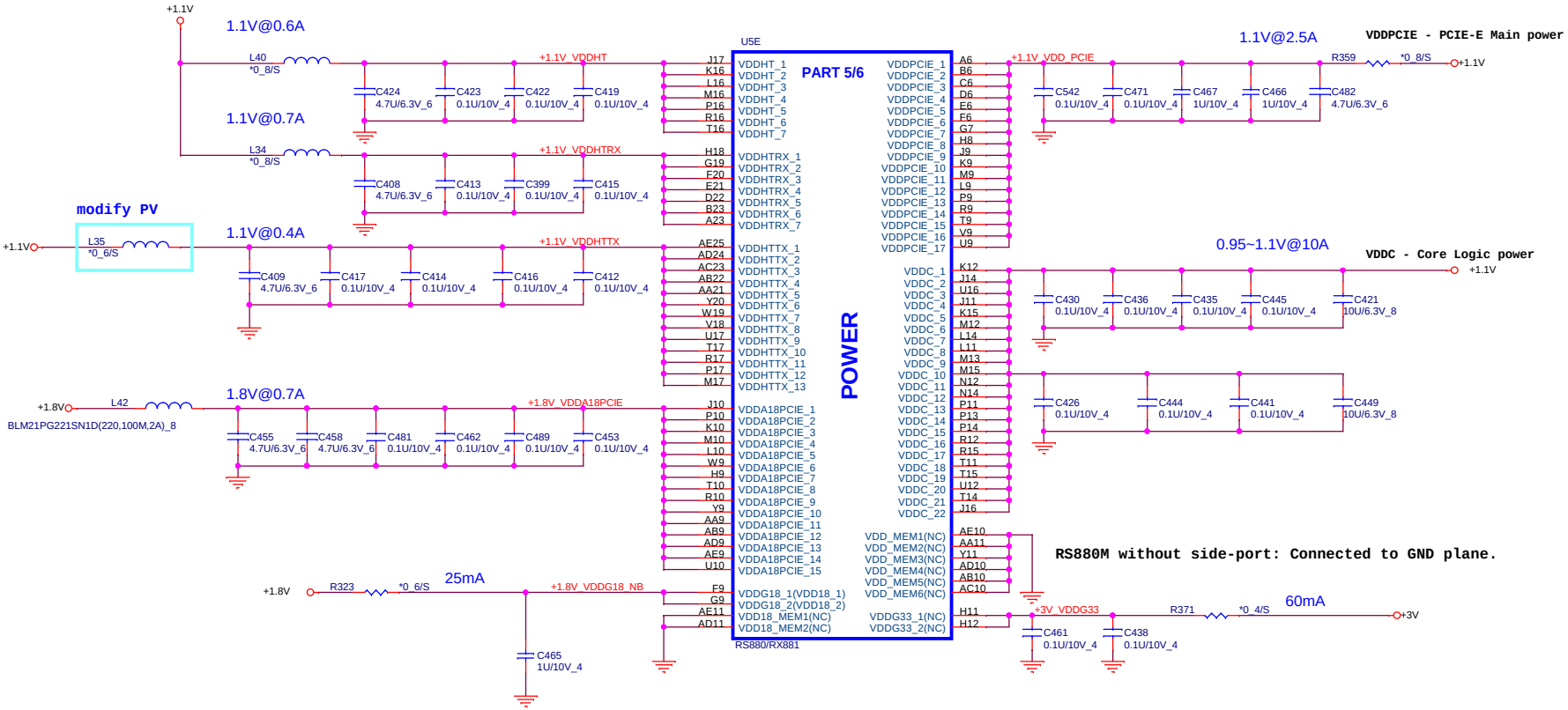



## RX881/RS880 POWER DIFFERENCE TABLE

| PIN NAME | RX881 | RS880 | PIN NAME | RX881 | RS880 |
|---|---|---|---|---|---|
| VDDHT | +1.1V | +1.1V | IOPLLVDD | +1.1V | +1.1V |
| VDDHTRX | +1.1V | +1.1V | AVDD | GND | +3.3V |
| VDDHTTX | +1.2V | +1.2V | AVDDDI | GND | +1.8V |
| VDDA18PCIE | +1.8V | +1.8V | AVDDQ | GND | +1.8V |
| VDDG18 | +1.8V | +1.8V | PLLVDD | GND | +1.1V |
| VDD18_MEM | GND | +1.8V | PLLVDD18 | GND | +1.8V |
| VDDPCIE | +1.1V | +1.1V | VDDA18PCIEPLL | +1.8V | +1.8V |
| VDDC | +1.1V | +1.1V | VDDA18HTPLL | +1.8V | +1.8V |
| VDD_MEM | GND | +1.8V/1.5V | VDDLTP18 | GND | +1.8V |
| VDDG33 | +3.3V | +3.3V | VDDLT18 | GND | +1.8V |
| IOPLLVDD18 | +1.8V | +1.8V | VDDLT33 | NC | NC |

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| Size | Document Number | Rev |
|---|---|---|
| Custom | RS880M-POWER5/5 | 3A |

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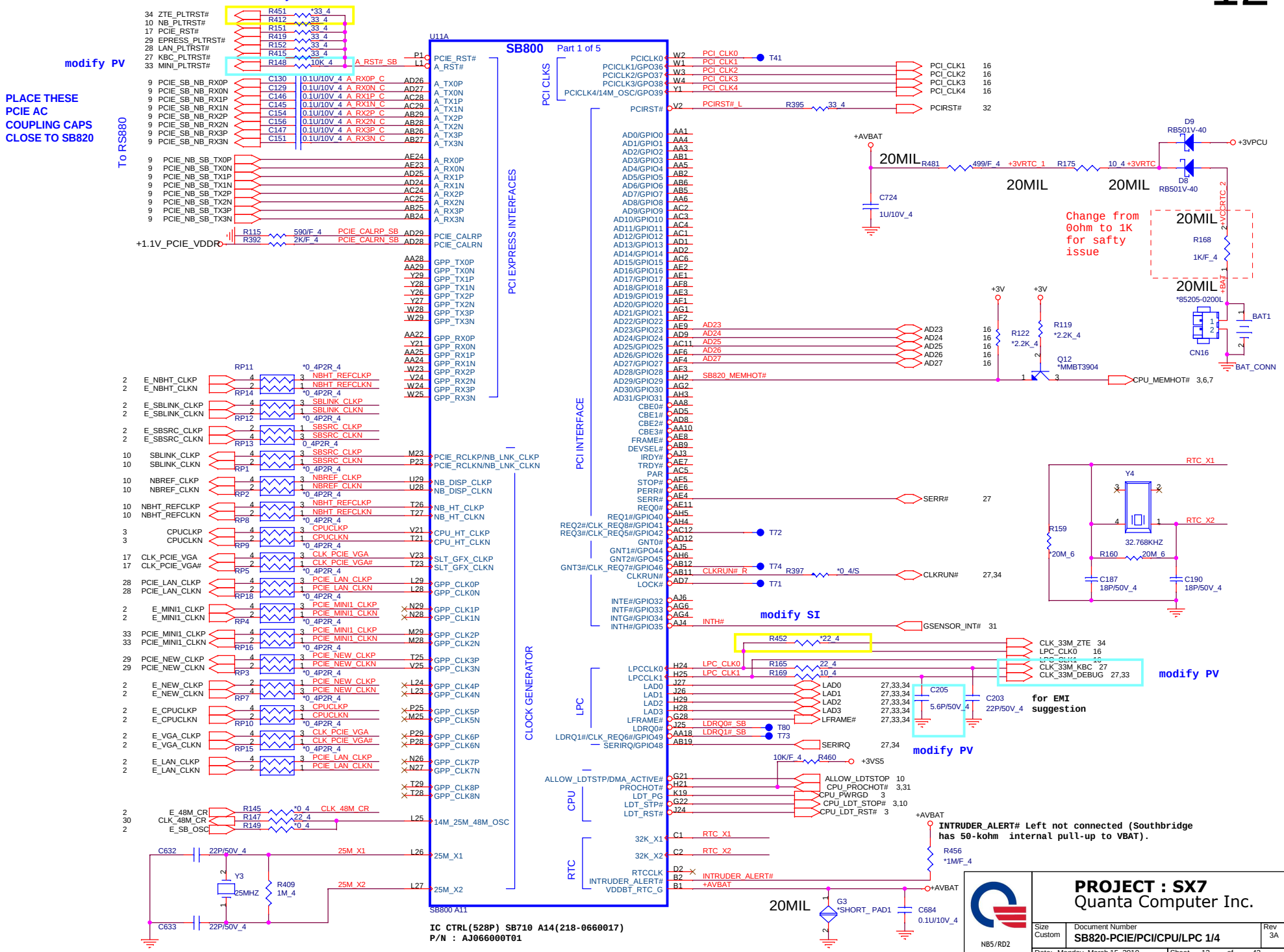
NB5/RD2


modify SI
modify PV
PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB820
To RS880
U11A
SB800
Part 1 of 5
PCI CLKS
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC
Change from 0ohm to 1K for safty issue
for EMI suggestion
INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).
SB800 A11
IC CTRL(528P) SB710 A14(218-0660017)
P/N : AJ066000T01
PROJECT : SX7
Quanta Computer Inc.
Size Custom
Document Number
SB820-PCIE/PCI/CPU/LPC 1/4
Rev 3A
Date: Monday, March 15, 2010
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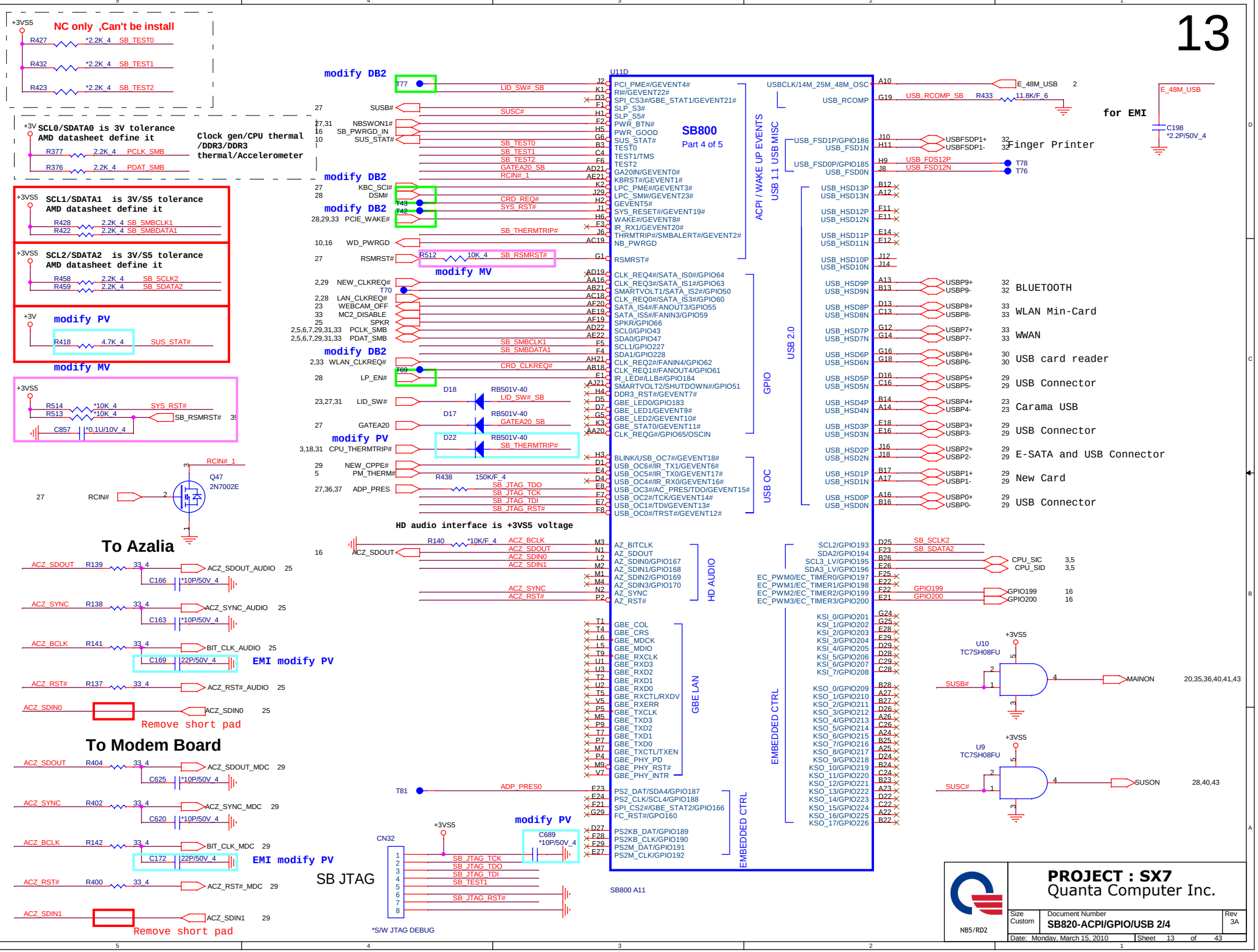
NB5/RD2


NC only ,Can't be install
R427 *2.2K_4 SB_TEST0
R432 *2.2K_4 SB_TEST1
R423 *2.2K_4 SB_TEST2
SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R377 2.2K_4 PCLK_SMB
R376 2.2K_4 PDAT_SMB
Clock gen/CPU thermal
/DDR3/DDR3
thermal/Accelerometer
SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it
R428 2.2K_4 SB_SMBCLK1
R422 2.2K_4 SB_SMBDATA1
SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R458 2.2K_4 SB_SCLK2
R459 2.2K_4 SB_SDATA2
modify PV
R418 4.7K_4 SUS_STAT#
modify MV
R514 *10K_4 SYS_RST#
R513 *10K_4 SB_RSMRST#
C857 *0.1U/10V_4
modify DB2
modify MV
modify PV
SB800
Part 4 of 5
U11D
ACPI / WAKE UP EVENTS
USB 1.1 USB MISC
USB 2.0
GPIO
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL
HD audio interface is +3VS5 voltage
To Azalia
ACZ_SDOUT R139 33_4 ACZ_SDOUT_AUDIO 25
C166 *10P/50V_4
ACZ_SYNC R138 33_4 ACZ_SYNC_AUDIO 25
C163 *10P/50V_4
ACZ_BCLK R141 33_4 BIT_CLK_AUDIO 25
C169 22P/50V_4
EMI modify PV
ACZ_RST# R137 33_4 ACZ_RST#_AUDIO 25
ACZ_SDIN0 ACZ_SDIN0 25
Remove short pad
To Modem Board
ACZ_SDOUT R404 33_4 ACZ_SDOUT_MDC 29
C625 *10P/50V_4
ACZ_SYNC R402 33_4 ACZ_SYNC_MDC 29
C620 *10P/50V_4
ACZ_BCLK R142 33_4 BIT_CLK_MDC 29
C172 22P/50V_4
EMI modify PV
ACZ_RST# R400 33_4 ACZ_RST#_MDC 29
ACZ_SDIN1 ACZ_SDIN1 29
Remove short pad
SB JTAG
CN32
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
C689 *10P/50V_4
modify PV
*S/W JTAG DEBUG
SB800 A11
Finger Printer
BLUETOOTH
WLAN Min-Card
WWAN
USB card reader
USB Connector
Carama USB
USB Connector
E-SATA and USB Connector
New Card
USB Connector
for EMI
E_48M_USB
C198 *2.2P/50V_4
U10 TC7SH08FU
U9 TC7SH08FU
MAINON 20,35,36,40,41,43
SUSON 28,40,43
PROJECT : SX7
Quanta Computer Inc.
Size Custom
Document Number SB820-ACPI/GPIO/USB 2/4
Rev 3A
Date: Monday, March 15, 2010
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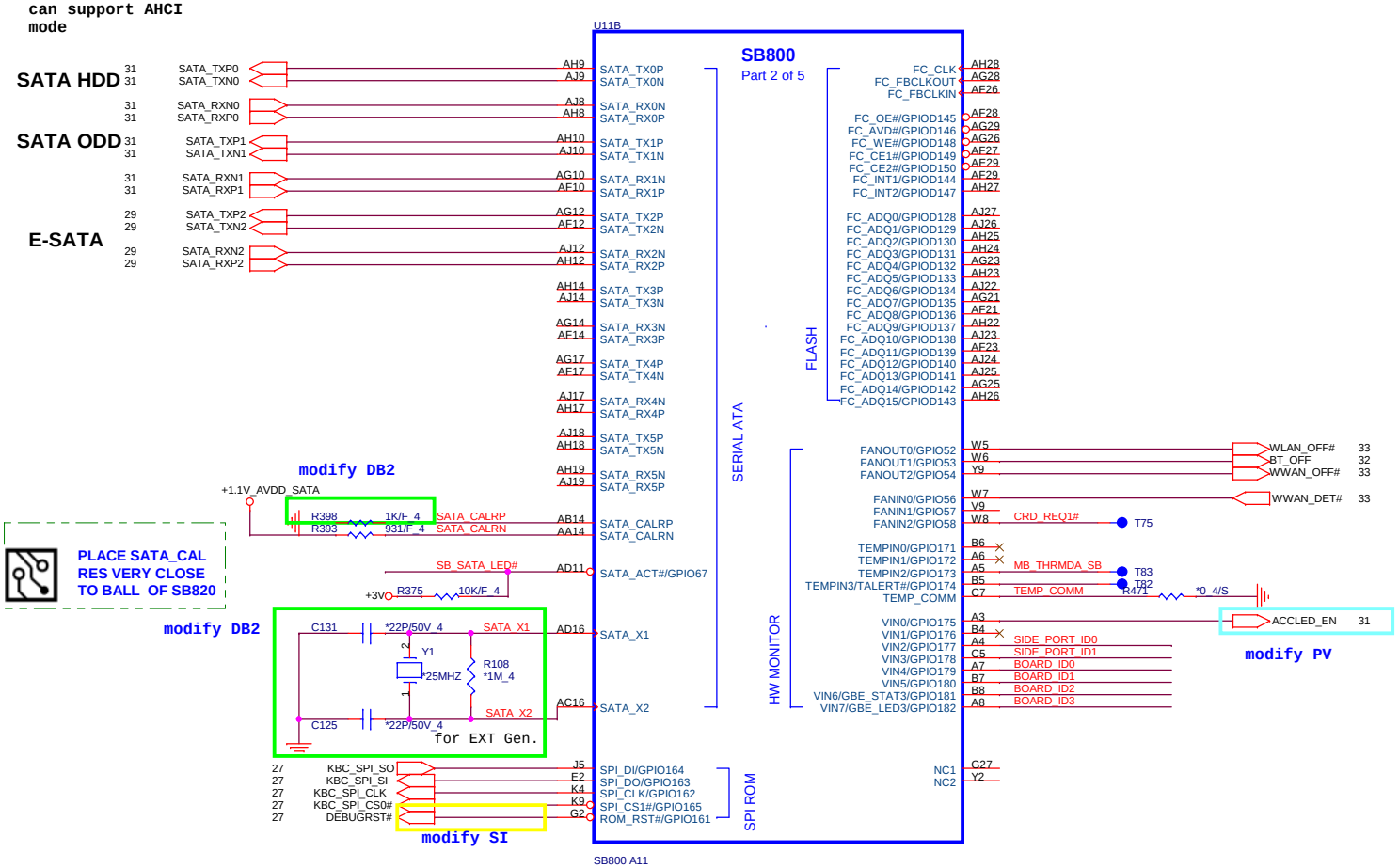
NB5/RD2

SATA PORT 0,1,2,3
can support AHCI
mode




| ID3 | ID2 | ID1 | ID0 | |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | SX7 UMA |
| 0 | 0 | 0 | 1 | SX7 UMA |
| 0 | 0 | 1 | 0 | SX7 Dis |
| 0 | 0 | 1 | 1 | SX7 Dis |
| 0 | 1 | 0 | 0 | SX7 UMA DF |
| 0 | 1 | 0 | 1 | SX7 UMA DF |
| 0 | 1 | 1 | 0 | SX7 Dis DF |
| 0 | 1 | 1 | 1 | SX7 Dis DF |

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Quanta Computer Inc.

NB5/RD2

| Size | Document Number | Rev |
|---|---|---|
| Custom | SB820-ACPI/GPIO/USB 2/4 | 3A |

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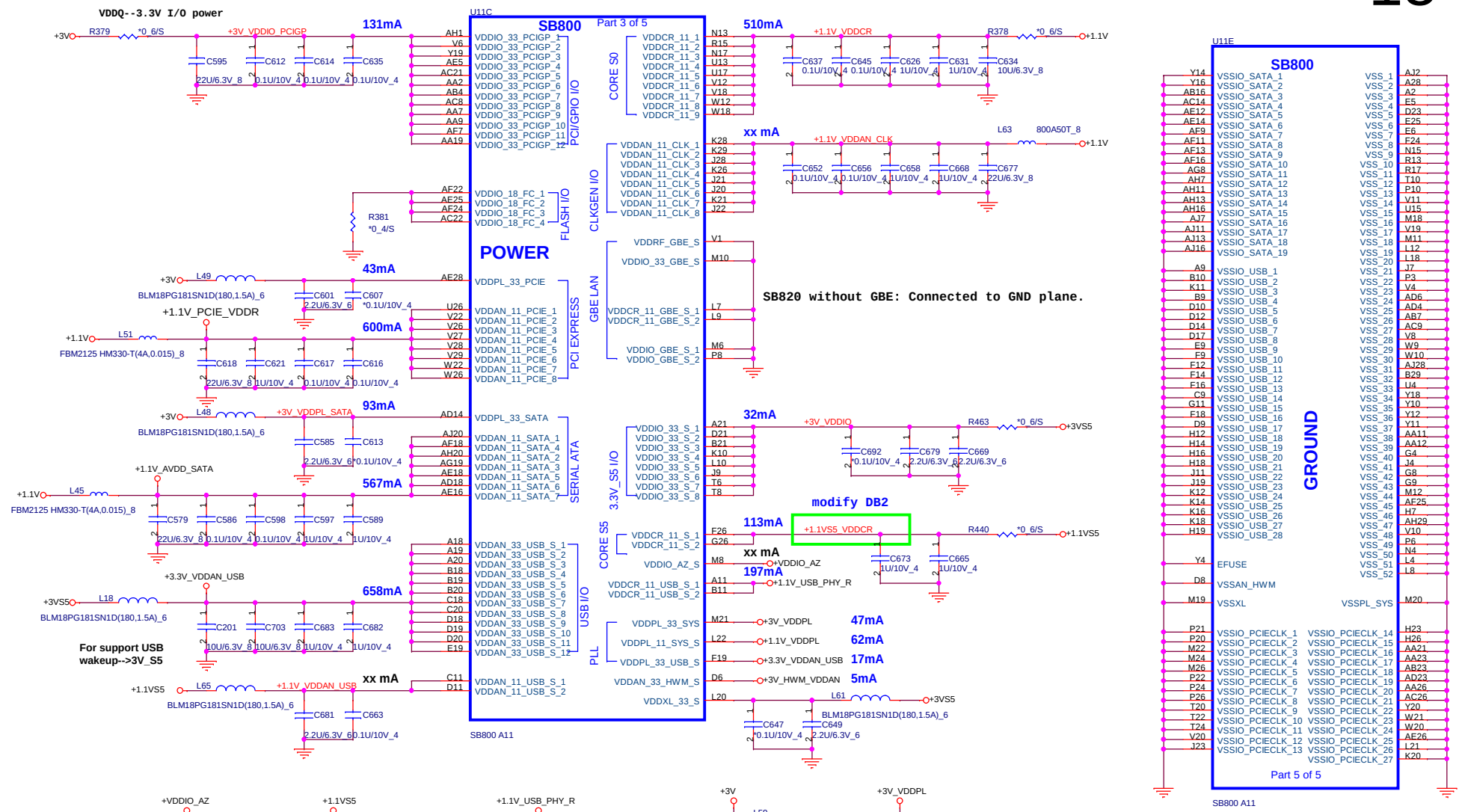
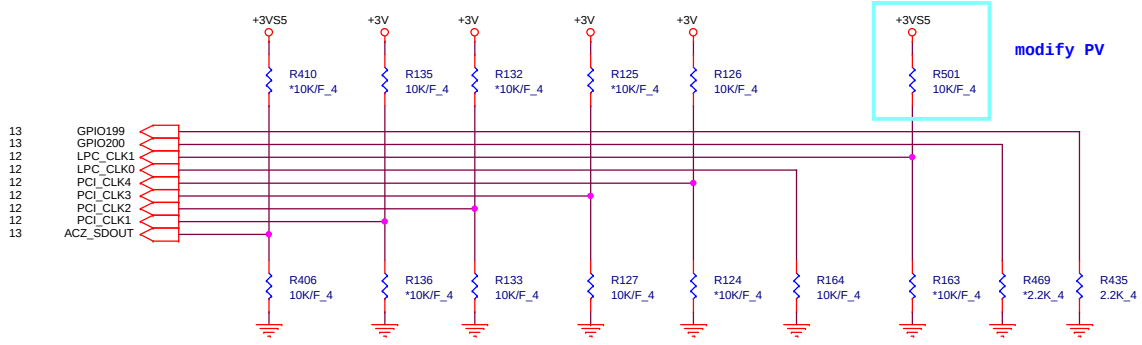
PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

# REQUIRED STRAPS



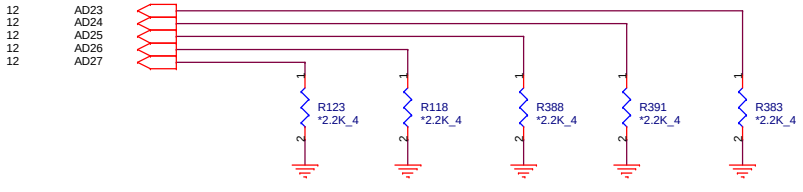

| | AZ_SDOUT | PCI_CLK1 | PCI_CLK2 | PCI_CLK3 | PCI_CLK4 | LPC_CLK0 | LPC_CLK1 | GPIO200 GPIO199 |
|---|---|---|---|---|---|---|---|---|
| PULL HIGH | LOW POWER MODE | ALLOW PCIE Gen2 DEFAULT | Watchdog Timer Enable | USE DEBUG STRAPS | non_Fusion CLOCK MODE DEFAULT | EC ENABLED | CLKGEN ENABLED DEFAULT | H, H=Reserved<br>H, L=SPI ROM DEFAULT |
| PULL LOW | PERFORMANCE MODE DEFAULT | FORCE PCIE Gen1 | Watchdog Timer Disable DEFAULT | IGNORE DEBUG STRAPS DEFAULT | Fusion CLOCK MODE | EC DISABLED DEFAULT | CLKGEN DISABLED | L, H=LPC ROM<br>L, L=FWH ROM |

modify DB2

internal have pull Hi 10K

# DEBUG STRAPS

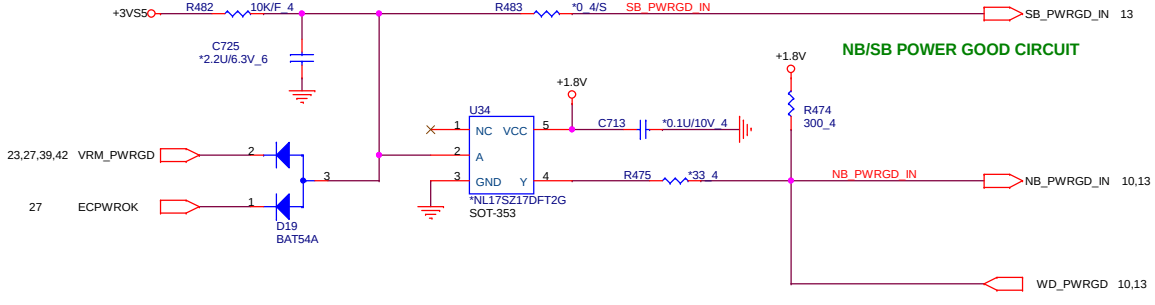
SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]




| | PCI_AD27 | PCI_AD26 | PCI_AD25 | PCI_AD24 | PCI_AD23 |
|---|---|---|---|---|---|
| PULL HIGH | USE PCI PLL DEFAULT | DISABLE ILA AUTORUN DEFAULT | USE FC PLL DEFAULT | USE DEFAULT PCIE STRAPS DEFAULT | DISABLE PCI MEM BOOT DEFAULT |
| PULL LOW | BYPASS PCI PLL | ENABLE ILA AUTORUN | BYPASS FC PLL | USE EEPROM PCIE STRAPS | ENABLE PCI MEM BOOT |

NB_PWRGD_IN:
RS880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)

## NB/SB POWER GOOD CIRCUIT




| | | |
|---|---|---|
| AL17SZ17000 | IC(5P) NL17SZ17DFT2G(SOT-353) | SOT-353 |
| ALUC1G17000 | IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) | SOT23-5 |

NB5/RD2

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Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | SB820-STRAPS | 3A |

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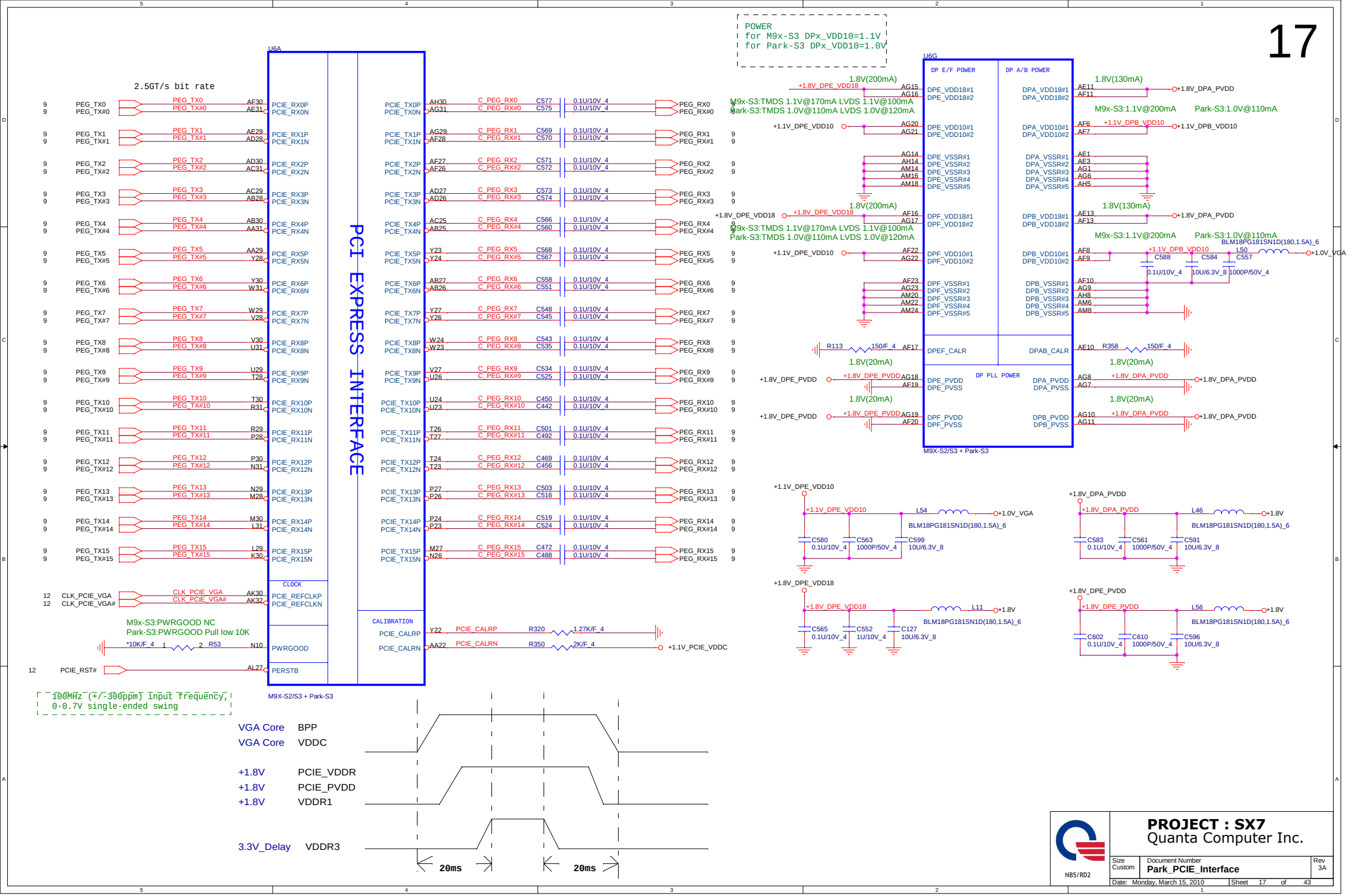


NB5/RD2

**PROJECT : SX7**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | **Park_PCIE_Interface** | 3A |

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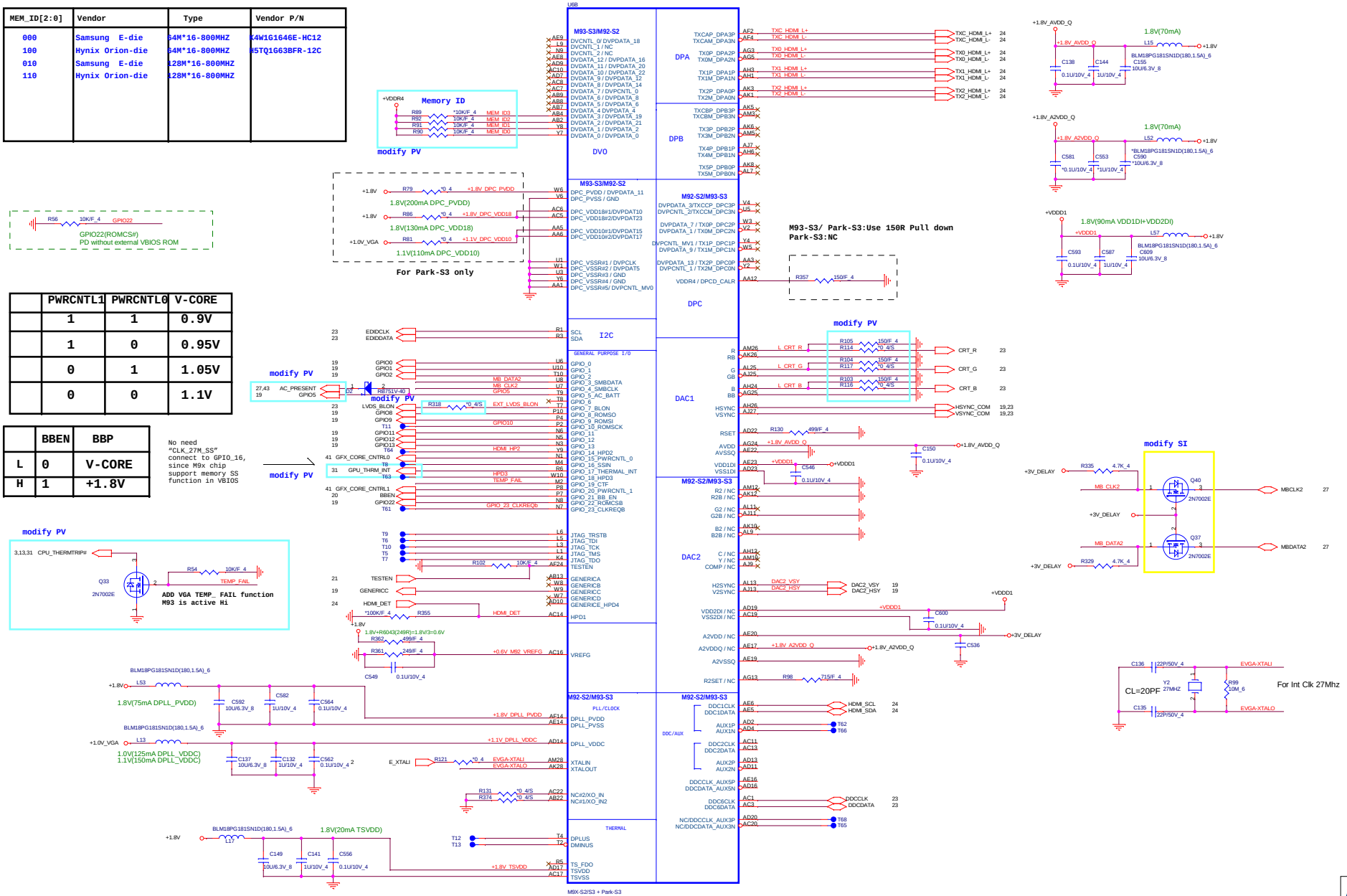
| MEM_ID[2:0] | Vendor | Type | Vendor P/N |
|---|---|---|---|
| 000 | Samsung E-die | 64M*16-800MHZ | K4W1G1646E-HC12 |
| 100 | Hynix Orion-die | 64M*16-800MHZ | H5TQ1G63BFR-12C |
| 010 | Samsung E-die | 128M*16-800MHZ | |
| 110 | Hynix Orion-die | 128M*16-800MHZ | |

| | PWRCNTL1 | PWRCNTL0 | V-CORE |
|---|---|---|---|
| | 1 | 1 | 0.9V |
| | 1 | 0 | 0.95V |
| | 0 | 1 | 1.05V |
| | 0 | 0 | 1.1V |

| | BBEN | BBP |
|---|---|---|
| L | 0 | V-CORE |
| H | 1 | +1.8V |

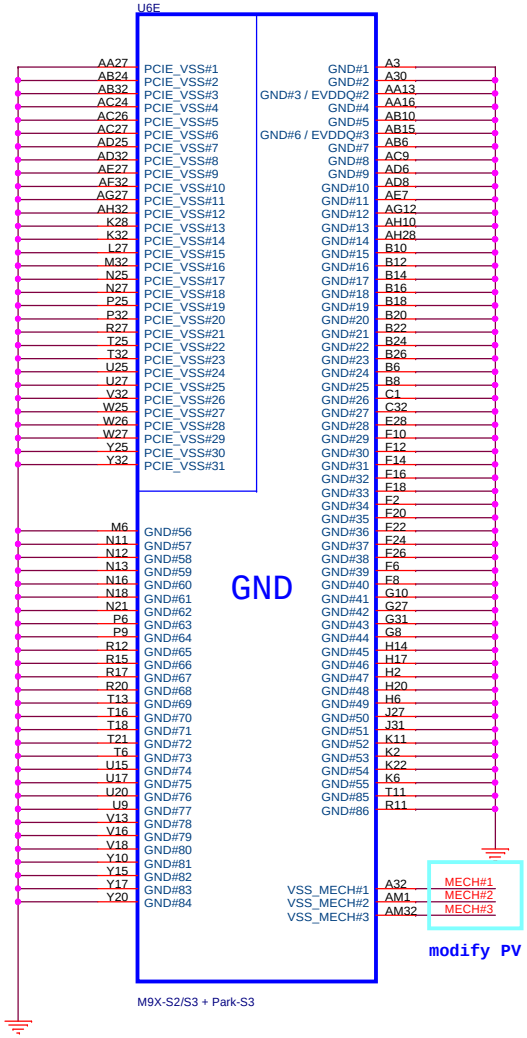
No need "CLK_27M_SS" connect to GPIO_16, since M9x chip support memory SS function in VBIOS

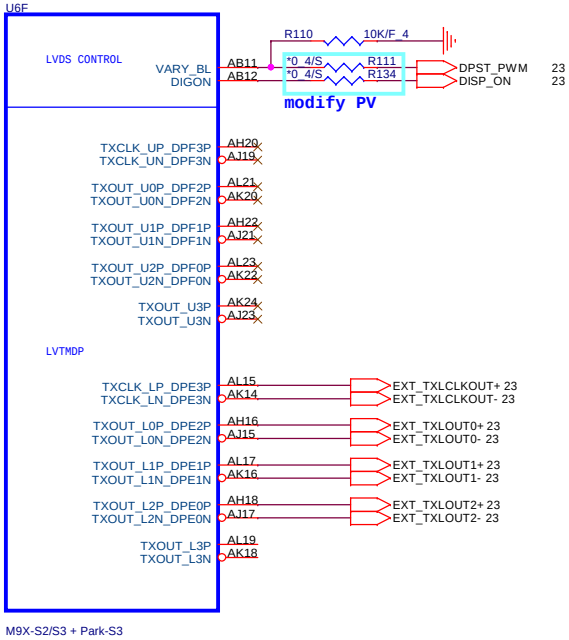



**PROJECT : SX7**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Park_Main | 3A |

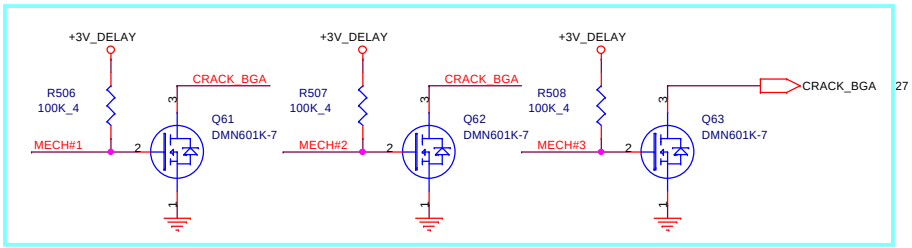
Date: Monday, March 15, 2010 Sheet 18 of 43





modify PV




## Pin Straps description

| Strap Name | | | Default Value |
|---|---|---|---|
| TX_PWRS_ENB | GPIO0 | **PCI Express Full TX Output Swing**<br>0: 50% Tx output swing for mobile mode<br>1: full Tx output swing (Default setting for Desktop) | 1 |
| TX_DEEMPH_EN | GPIO1 | **PCI Express Transmitter De-emphasis Enable**<br>0: Tx de-emphasis disabled for mobile mode<br>1: Tx de-emphasis enabled (Default setting for Desktop) | 1 |
| BIF_GEN2_EN_A | GPIO2 | 0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on.<br>1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on.<br>5.0 GT/s capability will be controlled by software. | 1 |
| RSVD<br>BIF_VGA_DIS<br>RSVD | GPIO8<br>GPIO9<br>GPIO21 | **Enable CLKREQ# Power Management**<br>0 - CLKREQ# power management capability is disabled<br>1 - CLKREQ# power management capability is enabled | 0<br>0<br>0 |
| BIOS_ROM_EN | GPIO22 | Enable external BIOS ROM device<br>0 - Disable external BIOS ROM device<br>1 - Enable external BIOS ROM device | 1 |
| AUD[0]<br>AUD(1) | VSYNC<br>HSYNC | AUD[1] AUD[0]<br>00 No Audio function<br>01 Audio for DisplayPort and HDMI if dongle is detected<br>10 Audio for DisplayPort only<br>11 Audio for both DisplayPort and HDMI | 1<br>1 |
| VIP_DEVICE_STRAP_ENA | V2SYNC | If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO | 0 |
| RSVD | GENERICC | | 0 |

## Memory Aperture size

| GPIO9<br>BIOSROM | | GPIO13<br>ROMIDCFG2 | GPIO12<br>ROMIDCFG1 | GPIO11<br>ROMIDCFG0 |
|---|---|---|---|---|
| 0 | 128M | 0 | 0 | 0 |
| 0 | 256M | 0 | 0 | 1 |
| 0 | 64M | 0 | 1 | 0 |
| 0 | 32M | 0 | 1 | 1 |
| 0 | 512M | 1 | 0 | 0 |
| 0 | 1G | 1 | 0 | 1 |
| 0 | 2G | 1 | 1 | 0 |
| 0 | 4G | 1 | 1 | 1 |

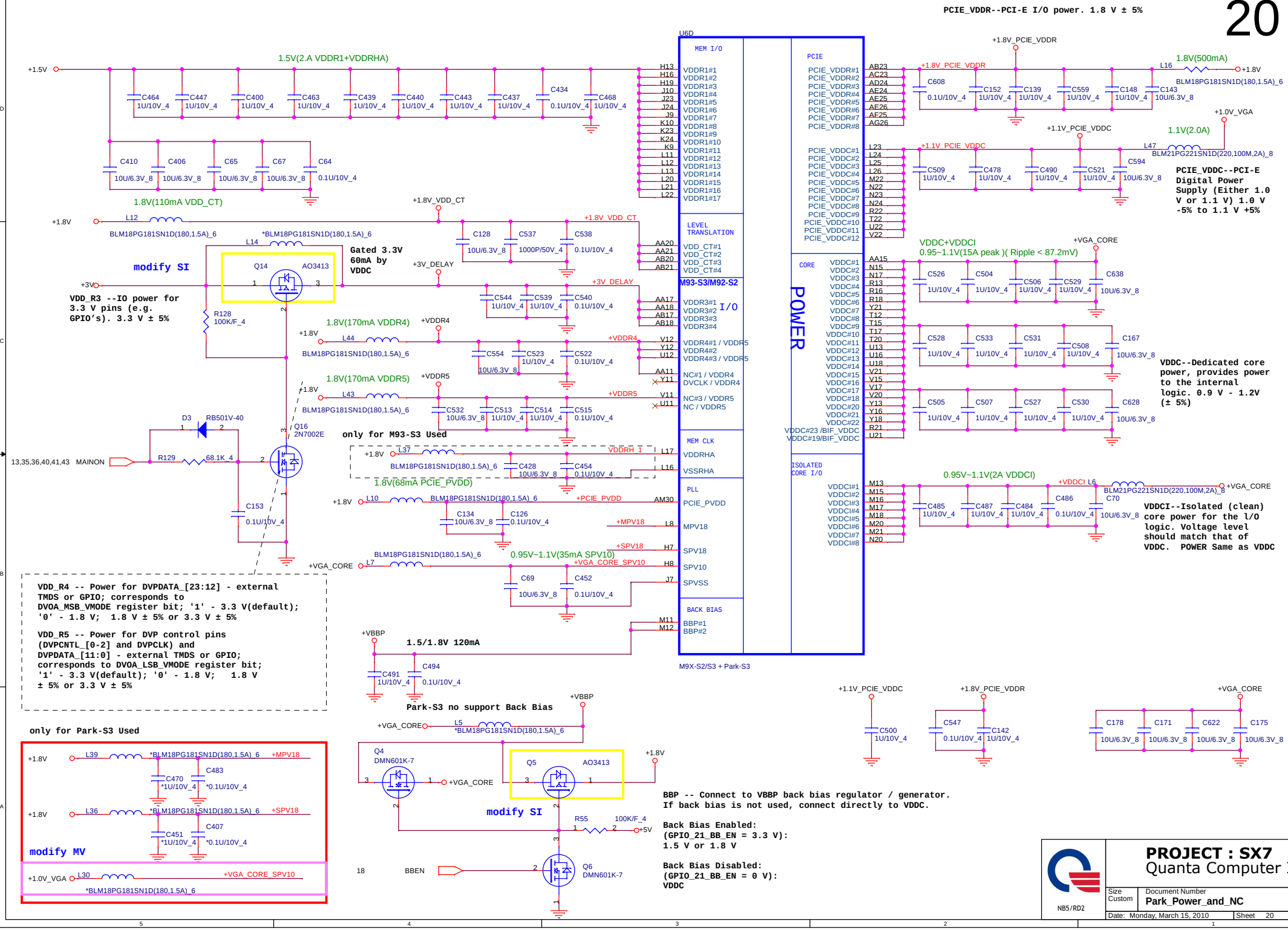
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

**PROJECT : SX7**
Quanta Computer Inc.

NB5/RD2

| Size | Document Number | Rev |
|---|---|---|
| Custom | Park_GND / LVDS/ Straps | 3A |

Date: Monday, March 15, 2010 Sheet 19 of 43

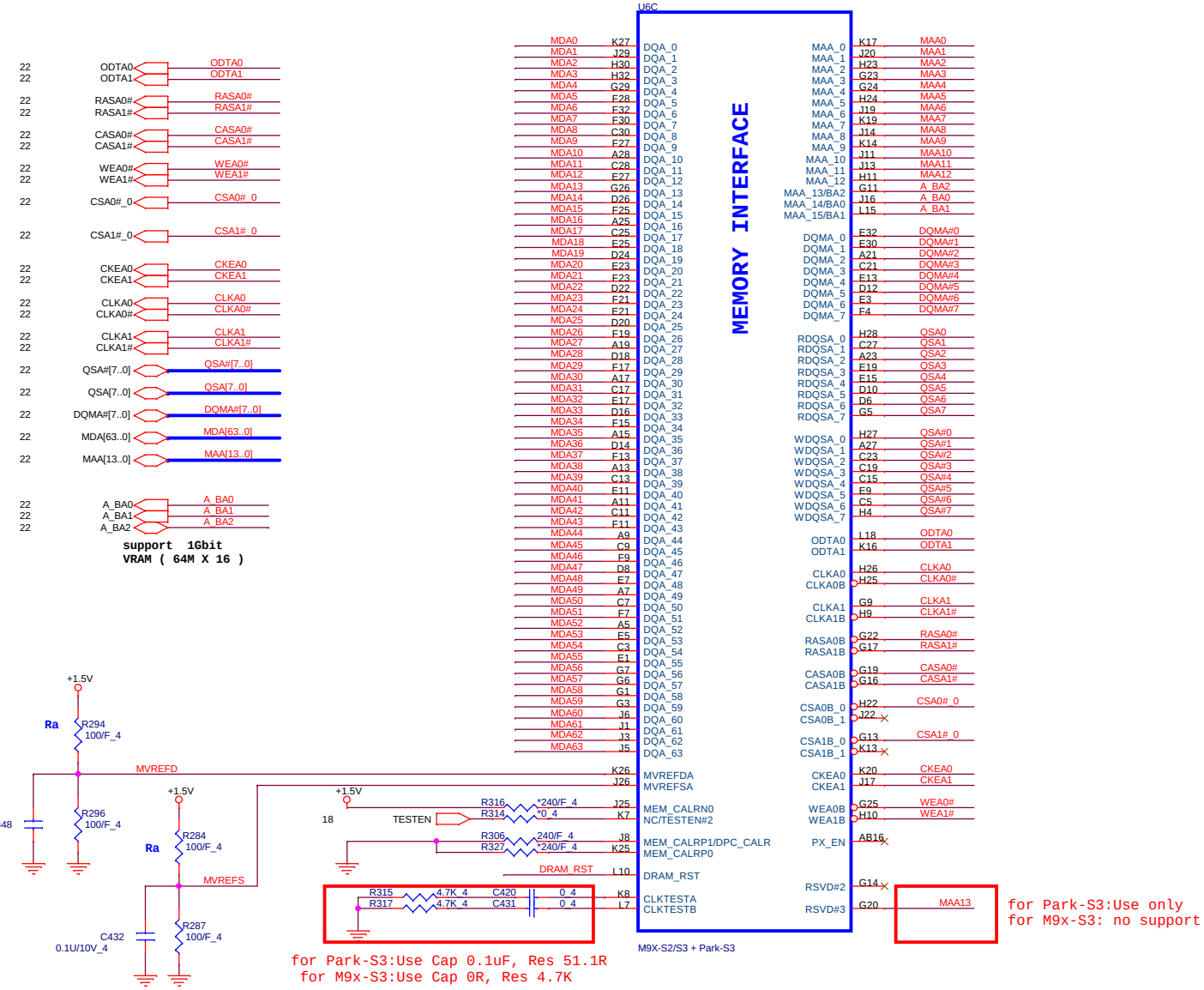



**PROJECT : SX7**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Park_Power_and_NC | 3A |

Date: Monday, March 15, 2010 Sheet 20 of 43

NB5/RD2

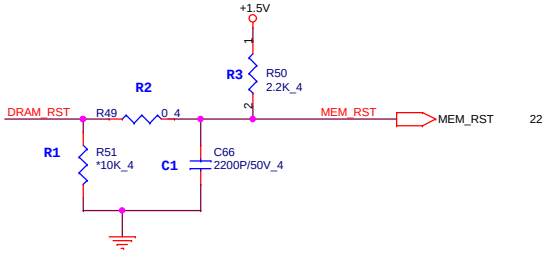



| | M9x-S2/S3 | Park-S3 |
|---|---|---|
| MEM_CALRN0(J25)<br>MEM_CALRP0(K25) | NC | 240R |
| MEM_CALRP1(J8) | 240R | 150R |
| TESTEN2#2(K7) | NC | 0R |
| R1 | NC | 10K |
| R2 | 0R | 51R |
| R3 | 2.2K | NC |
| C1 | 2.2nF | 68pF |

240R:CS12402FB03
150R:CS11502FB21

0R:CS00002JB38
680R:CS16802JB27

2.2nF:CH22206KB16
68pF:CH06806JB01




**PROJECT : SX7**
Quanta Computer Inc.

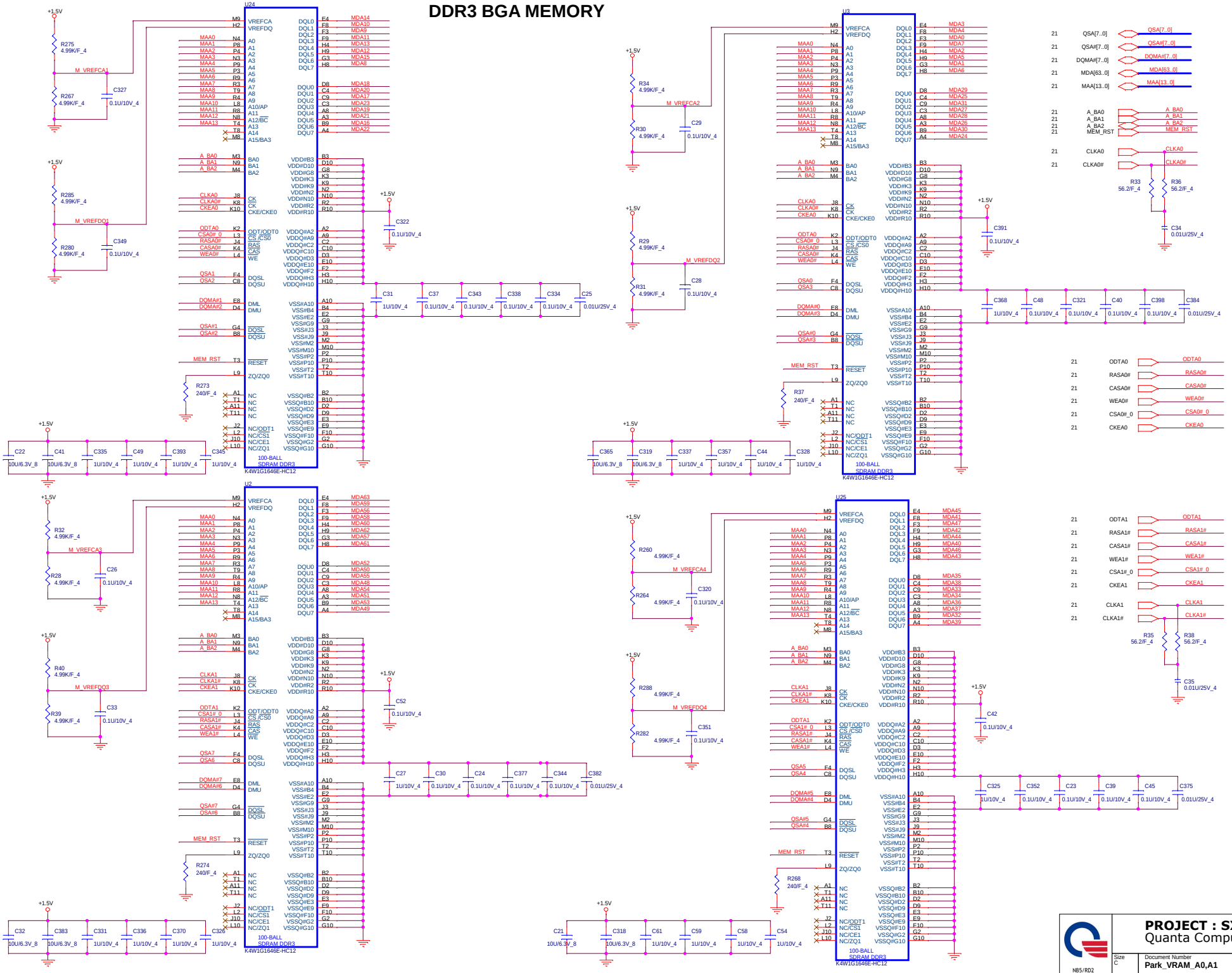
NB5/RD2

| Size | Document Number | Rev |
|---|---|---|
| Custom | Park_MEM_Interface | 3A |

Date: Monday, March 15, 2010 Sheet 21 of 43

# DDR3 BGA MEMORY



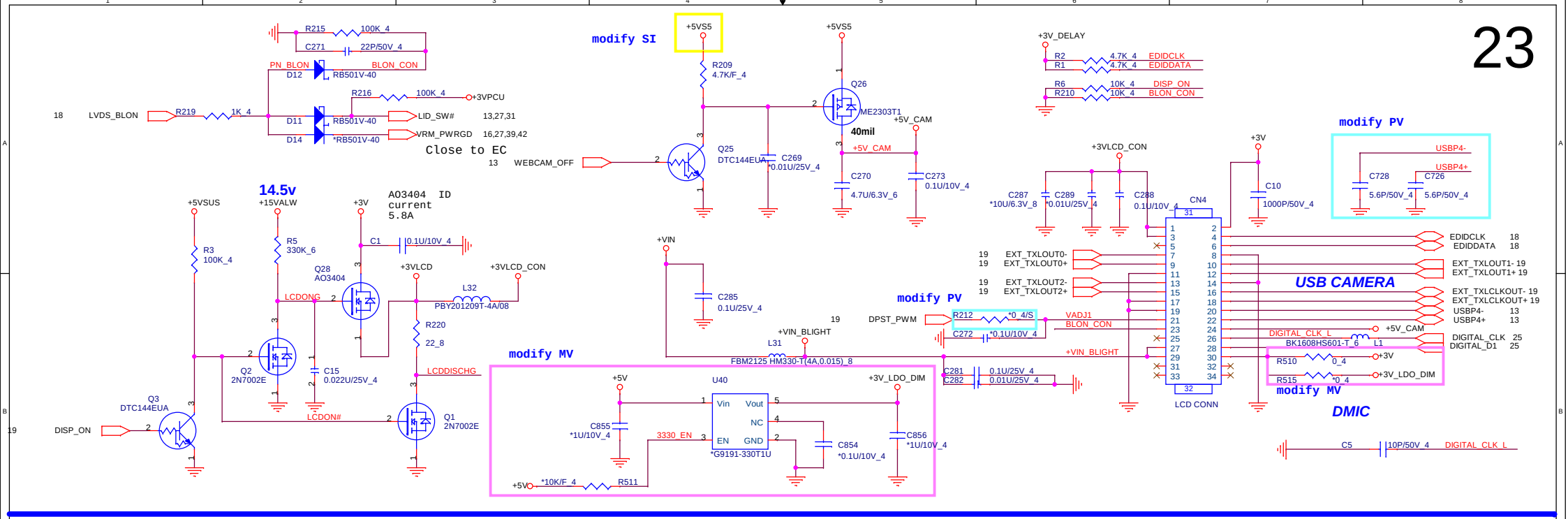



**PROJECT : SX7**
Quanta Computer Inc.

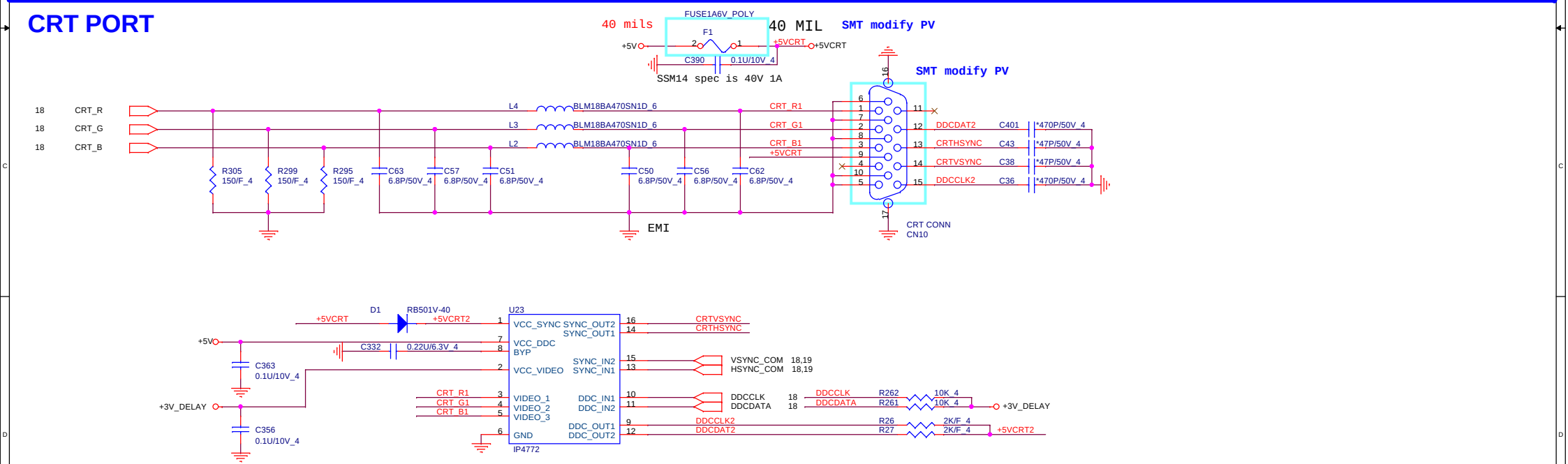
| Size | Document Number | Rev |
|---|---|---|
| C | Park_VRAM_A0,A1 | 3A |

Date: Monday, March 15, 2010 Sheet 22 of 43

NB5/RD2




# CRT PORT




2,3,5,6,7,10,11,12,13,14,15,16,20,25,27,28,29,30,31,32,33,34,35,37,43 +3V
12,27,31,32,33,36,37,38 +3VPCU
20,24,25,31,32,33,37,43 +5V
29,43 +5VSUS
38,43 +15VALW
36,38,39,40,41,42,43 +VIN

NB5/RD2

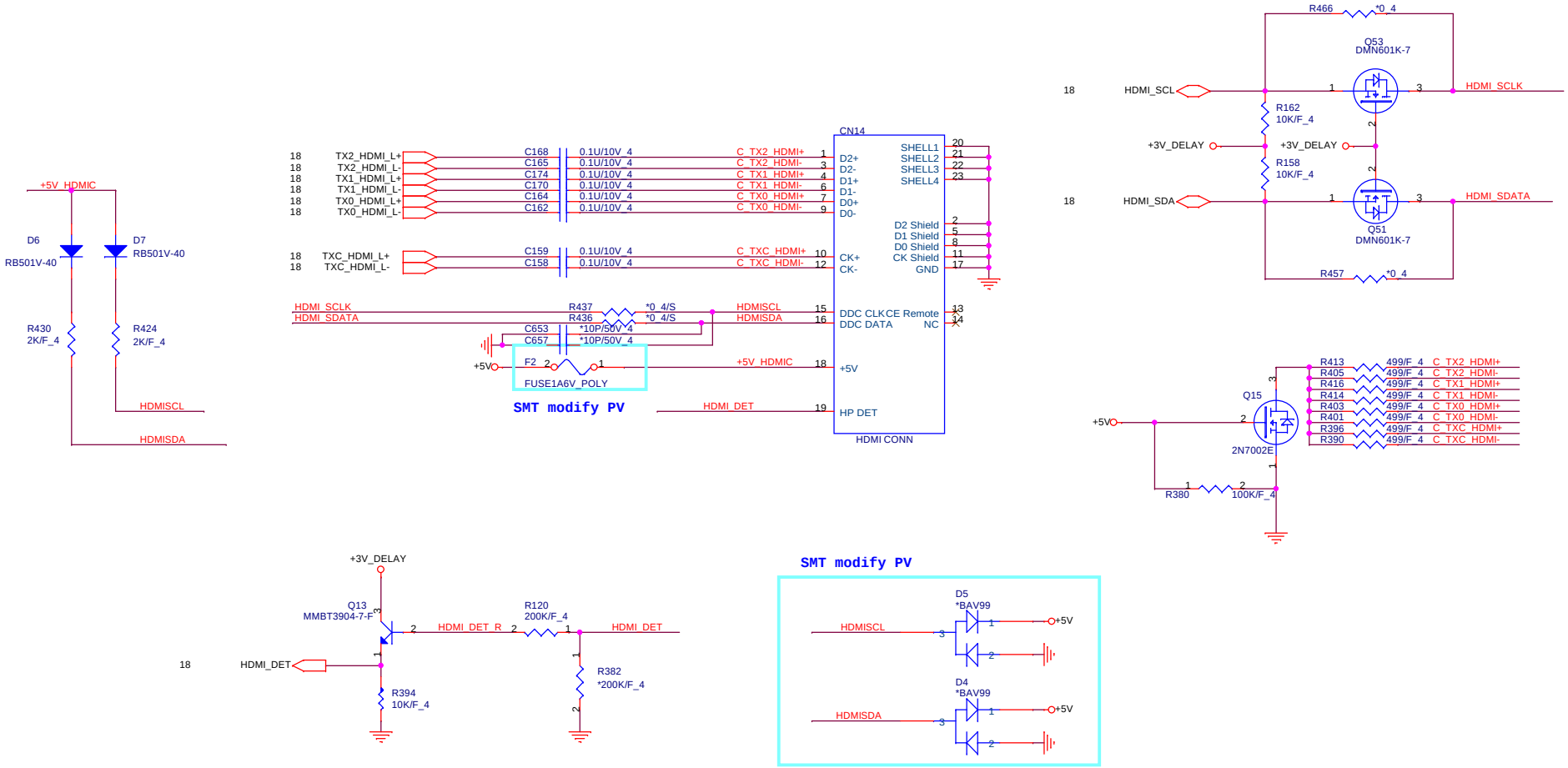
**PROJECT : SX7**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | LCD CONN/LID function | 3A |

Date: Monday, March 15, 2010 Sheet 23 of 43

# HDMI PORT






**PROJECT : SX7**
Quanta Computer Inc.

NB5/RD2

| Size | Document Number | Rev |
|---|---|---|
| Custom | **HDMI Conn** | 3A |

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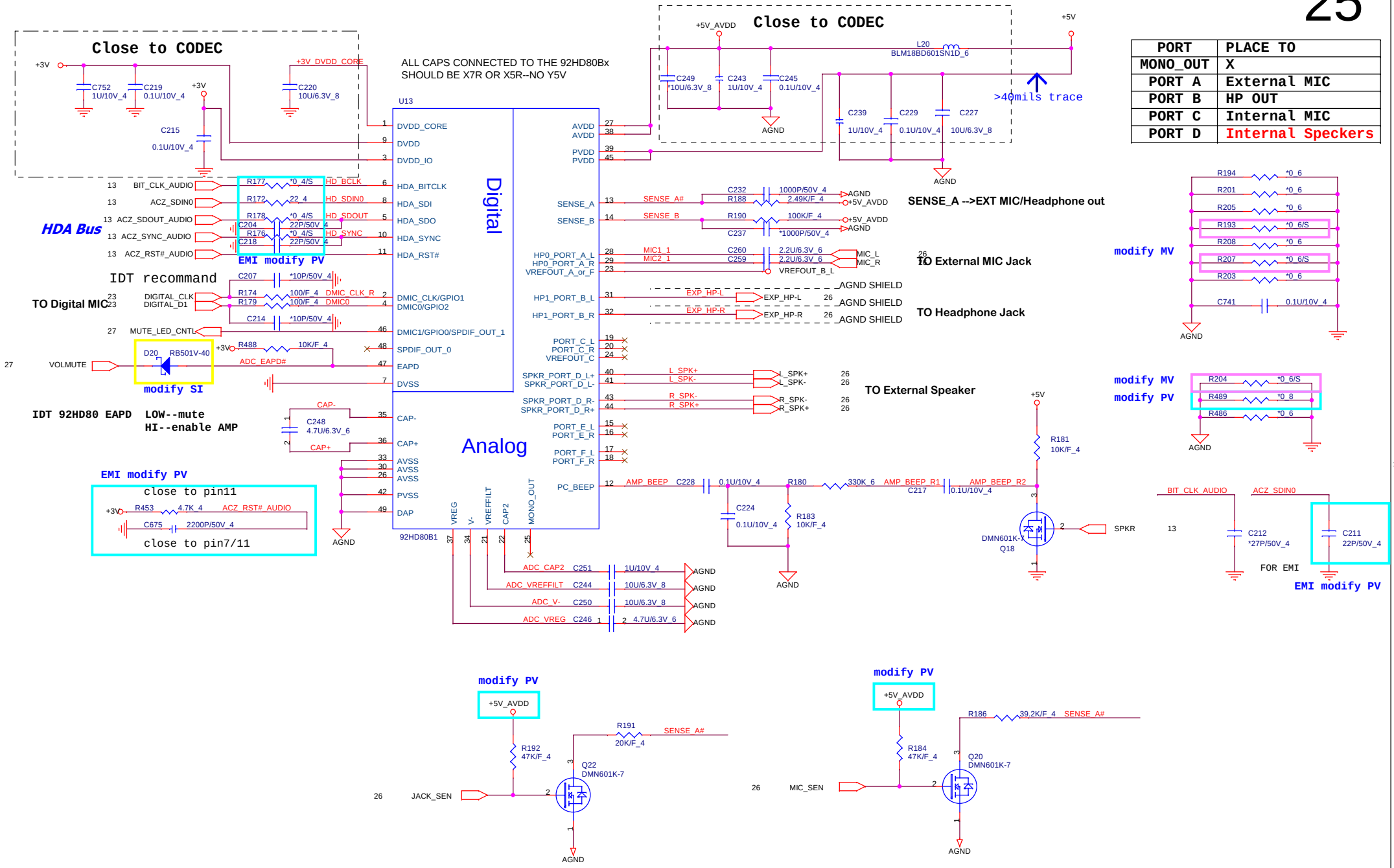
| PORT | PLACE TO |
|---|---|
| MONO_OUT | X |
| PORT A | External MIC |
| PORT B | HP OUT |
| PORT C | Internal MIC |
| PORT D | Internal Speckers |



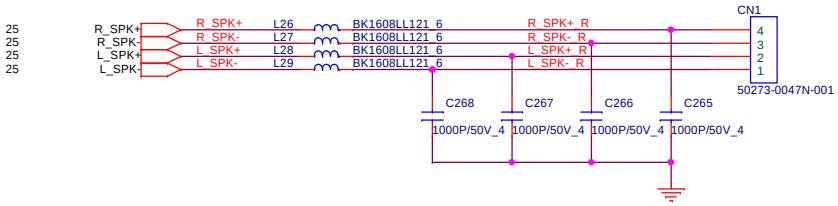

**PROJECT : SX7**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | IDT92HD80 | 3A |

Date: Monday, March 15, 2010 Sheet 25 of 43

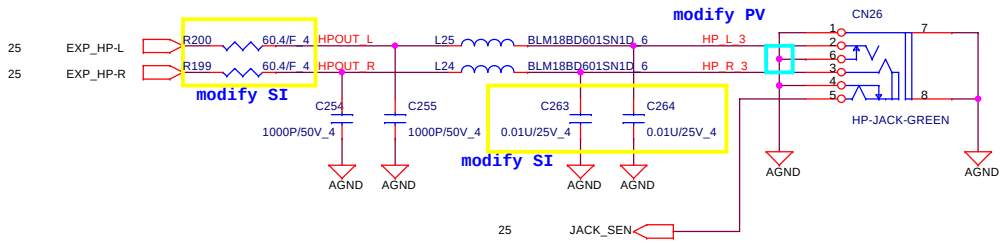
Note: JACK_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

## INT. SPEAKER



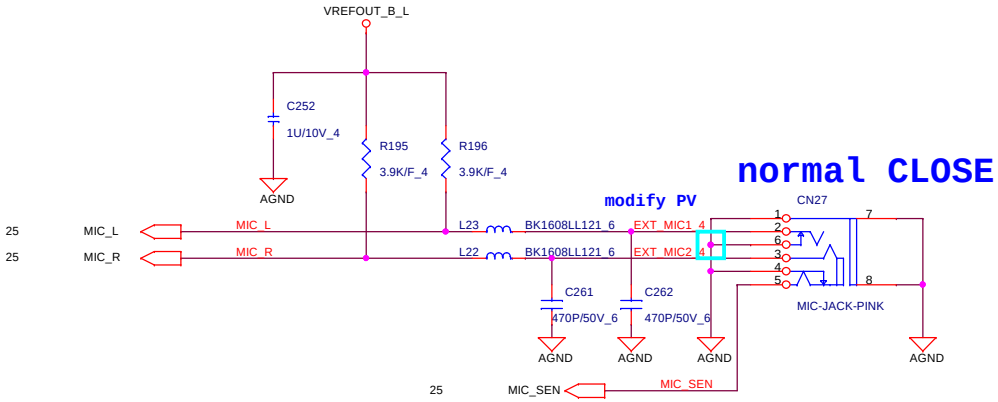

## Headphone Jack

**normal CLOSE**



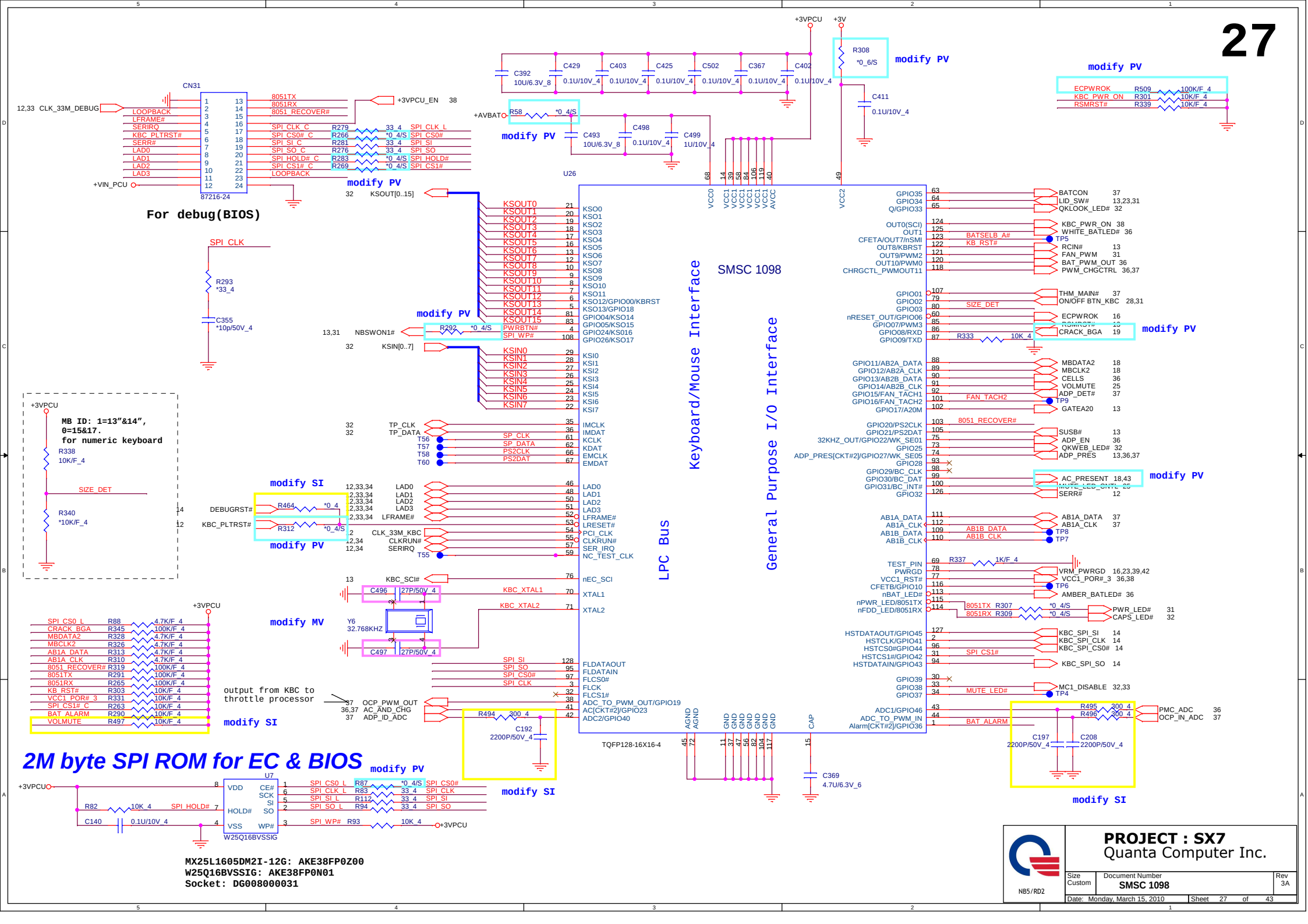

## EXT Mic Jack

**normal CLOSE**

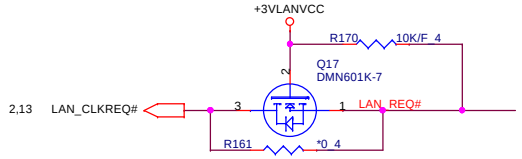


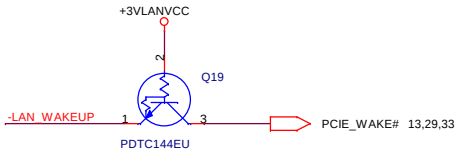

Note: MIC_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

| | | |
|---|---|---|
| NB5/RD2 | **PROJECT : SX7**<br>Quanta Computer Inc. | |
| Size<br>Custom | Document Number<br>**HP/MIC/SPK** | Rev<br>3A |
| | Date: Monday, March 15, 2010 | Sheet 26 of 43 |

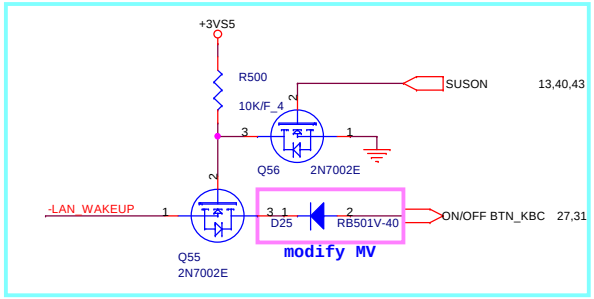

SMSC 1098
Keyboard/Mouse Interface
General Purpose I/O Interface
LPC Bus
U26
TQFP128-16X16-4
CN31
87216-24
For debug(BIOS)
modify PV
modify SI
modify MV
2M byte SPI ROM for EC & BIOS
U7
W25Q16BVSSIG
MX25L1605DM2I-12G: AKE38FP0Z00
W25Q16BVSSIG: AKE38FP0N01
Socket: DG008000031
MB ID: 1=13"&14",
0=15&17.
for numeric keyboard
output from KBC to throttle processor
PROJECT : SX7
Quanta Computer Inc.
Size Custom
Document Number SMSC 1098
Rev 3A
Date: Monday, March 15, 2010
Sheet 27 of 43
NB5/RD2

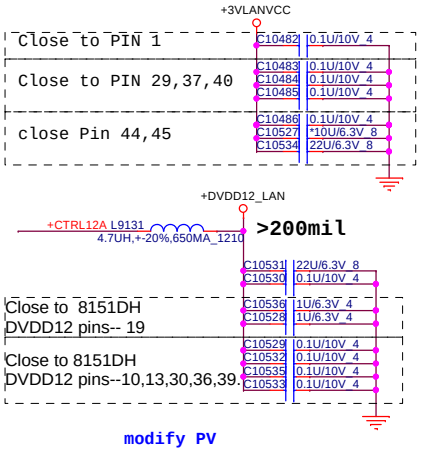
modify DB2

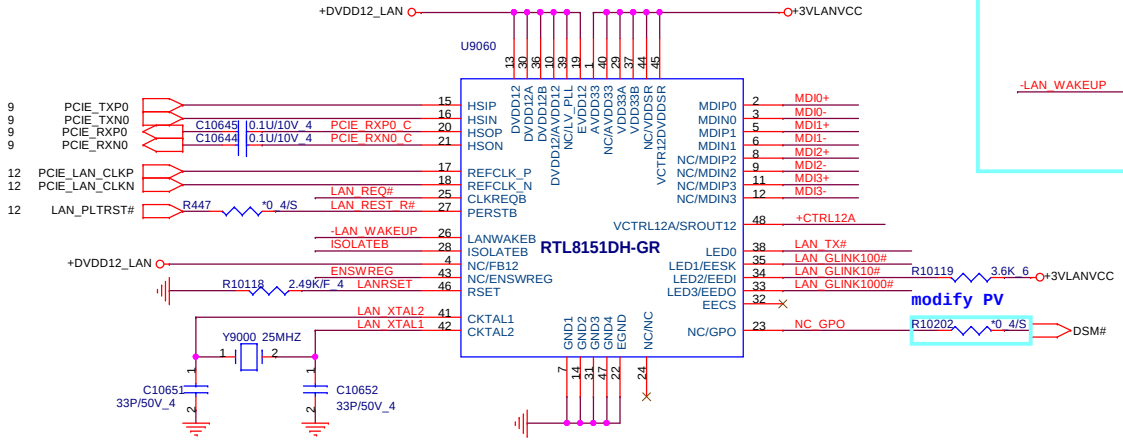


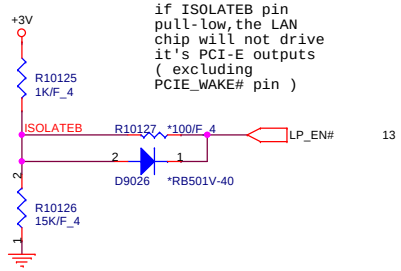

modify PV



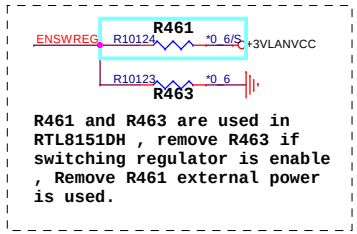




RTL8151DH-GR



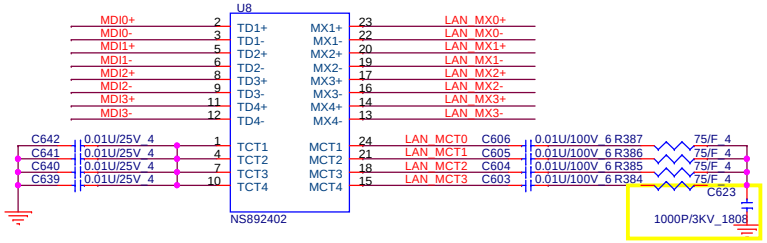

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs ( excluding PCIE_WAKE# pin )

modify PV




**R461 and R463 are used in RTL8151DH , remove R463 if switching regulator is enable , Remove R461 external power is used.**

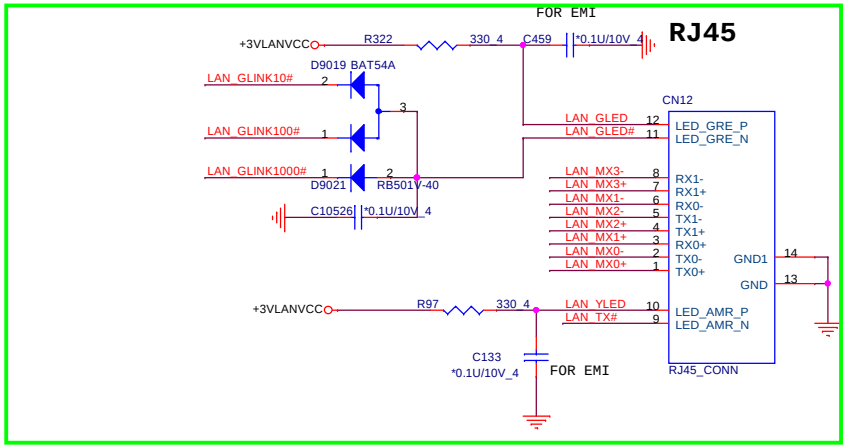
## Transformer for 10/100/1000




modify SI

## Lan Con.

modify DB2




43 +3VLANVCC
2,3,5,6,7,10,11,12,13,14,15,16,20,23,25,27,29,30,31,32,33,34,35,37,43 +3V

NB5/RD2

**PROJECT : SX7**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | LAN RTL8151/RJ45 | 3A |

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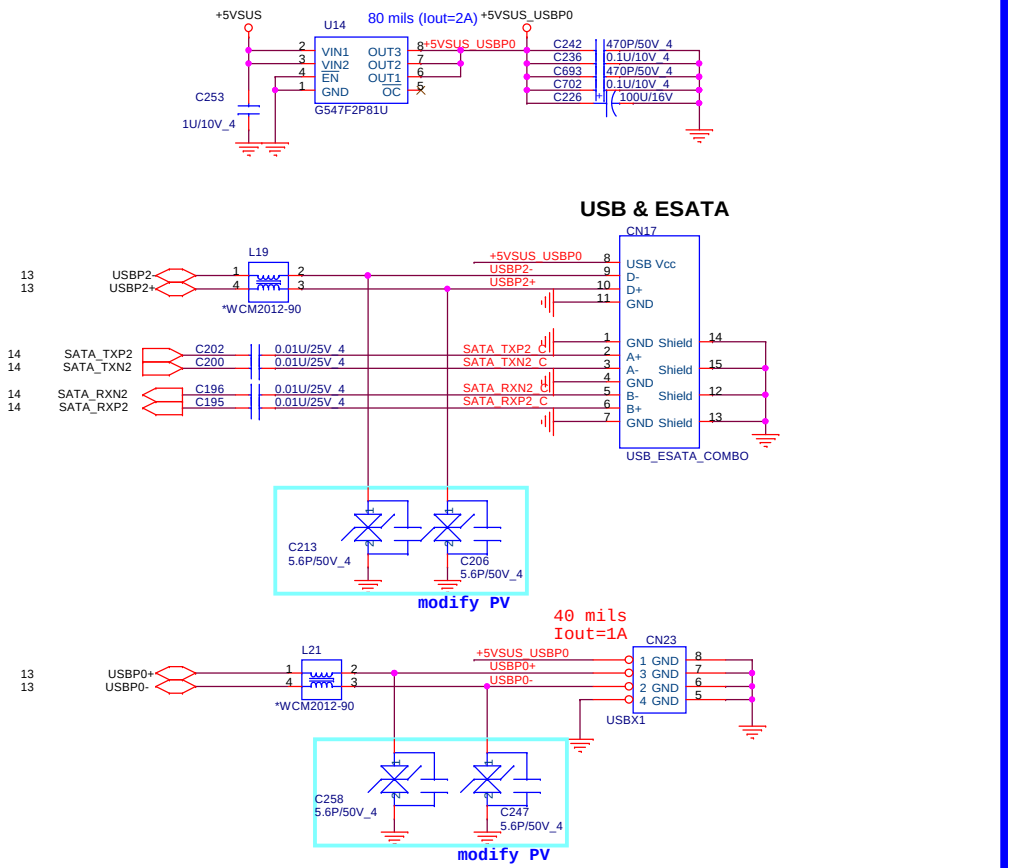
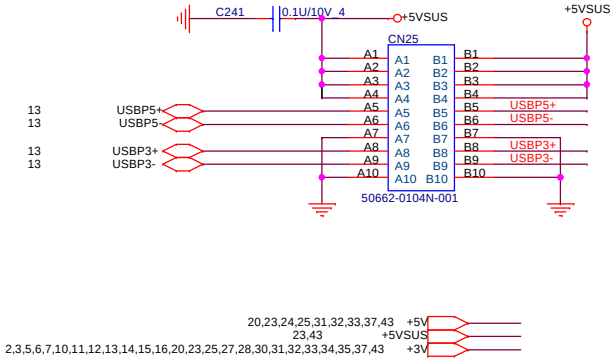
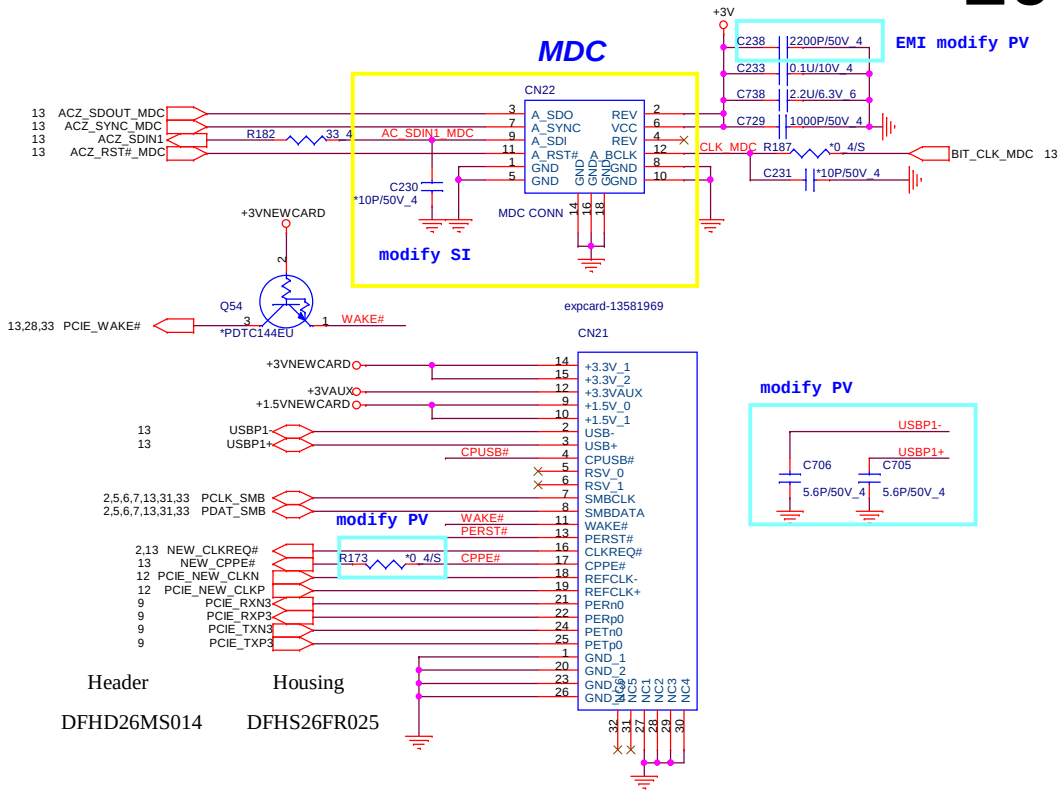
# LEFT SIDE USBX1 and E-SATA/USB COMBO



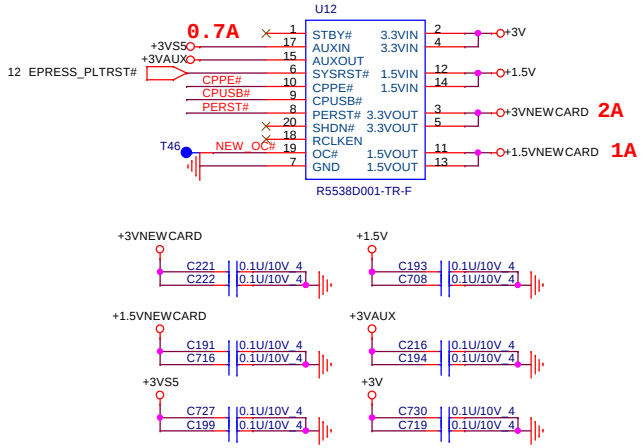

# RIGHT SIDE USBX2




# Modem CONN




## NEWCARD (PCIEXPRESS*1 + USB*1)




**PROJECT : SX7**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | EXTERNAL USB X2 | 3A |

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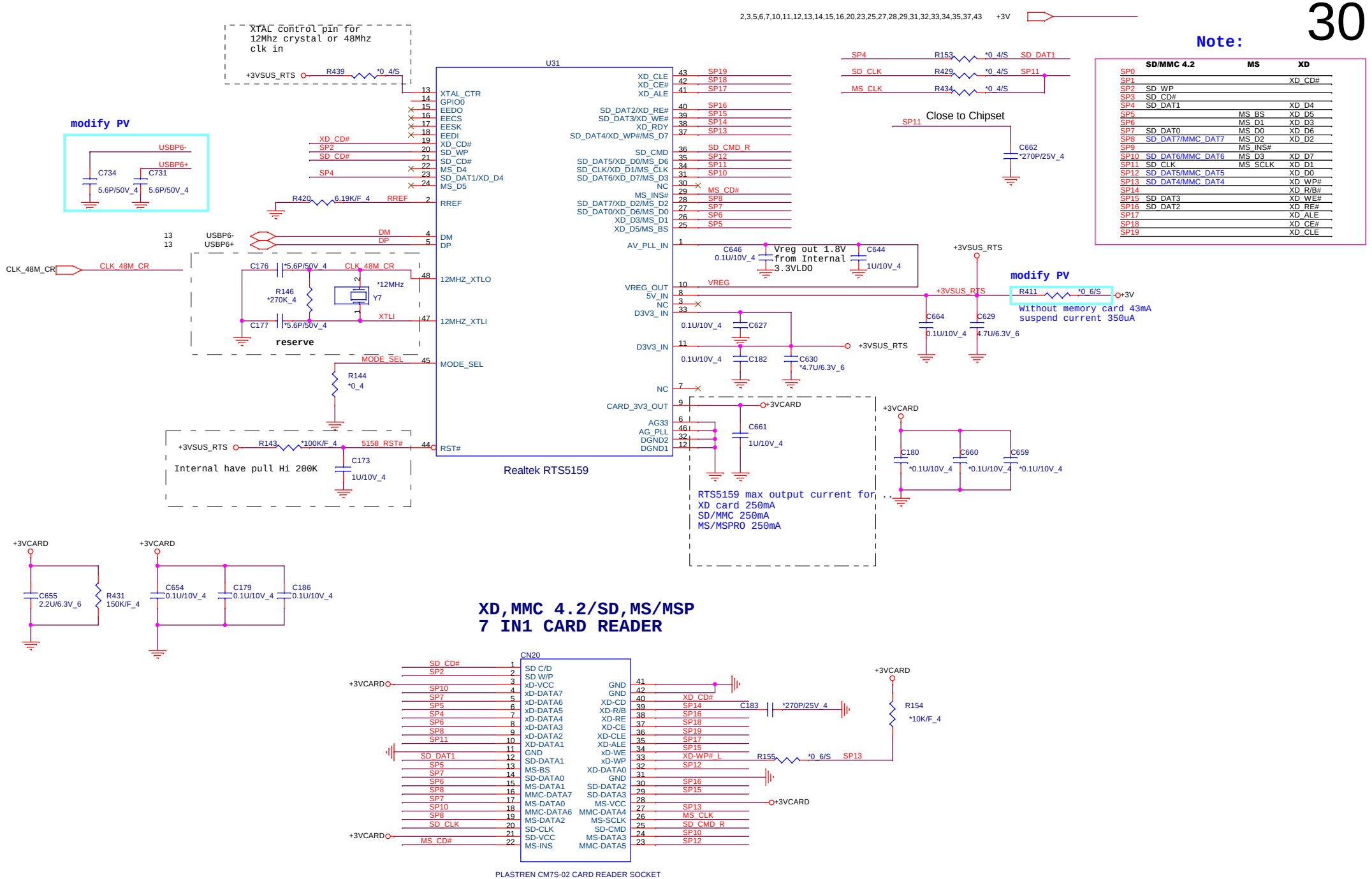
NB5/RD2




## Note:

| | SD/MMC 4.2 | MS | XD |
|---|---|---|---|
| SP0 | | | |
| SP1 | | | XD_CD# |
| SP2 | SD_WP | | |
| SP3 | SD_CD# | | |
| SP4 | SD_DAT1 | | XD_D4 |
| SP5 | | MS_BS | XD_D5 |
| SP6 | | MS_D1 | XD_D3 |
| SP7 | SD_DAT0 | MS_D0 | XD_D6 |
| SP8 | SD_DAT7/MMC_DAT7 | MS_D2 | XD_D2 |
| SP9 | | MS_INS# | |
| SP10 | SD_DAT6/MMC_DAT6 | MS_D3 | XD_D7 |
| SP11 | SD_CLK | MS_SCLK | XD_D1 |
| SP12 | SD_DAT5/MMC_DAT5 | | XD_D0 |
| SP13 | SD_DAT4/MMC_DAT4 | | XD_WP# |
| SP14 | | | XD_R/B# |
| SP15 | SD_DAT3 | | XD_WE# |
| SP16 | SD_DAT2 | | XD_RE# |
| SP17 | | | XD_ALE |
| SP18 | | | XD_CE# |
| SP19 | | | XD_CLE |

**PROJECT : SX7**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | RTS5159 & CR SOCKET | 3A |

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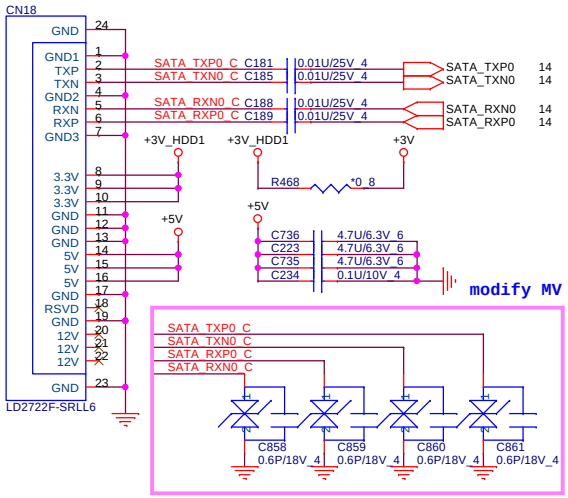
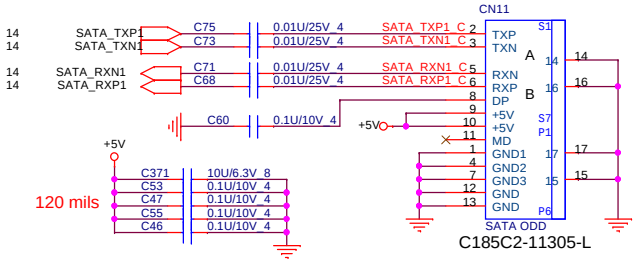
NB5/RD2

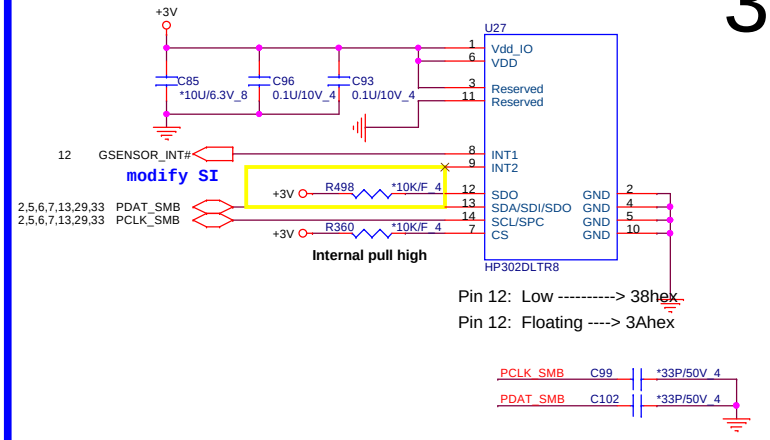
# SATA HDD CONNECTOR



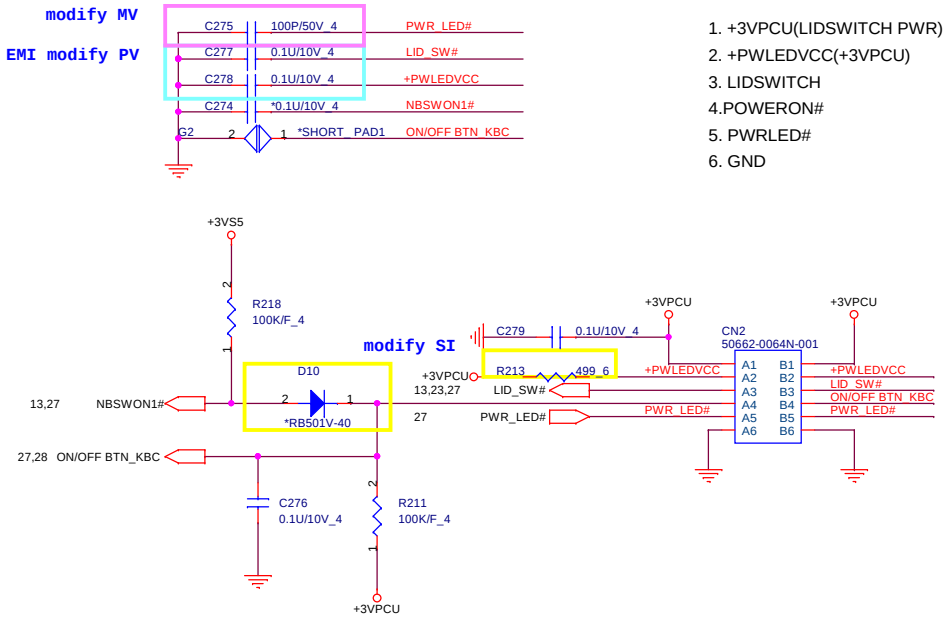

# SATA CD-ROM




# Accelerometer Sensor

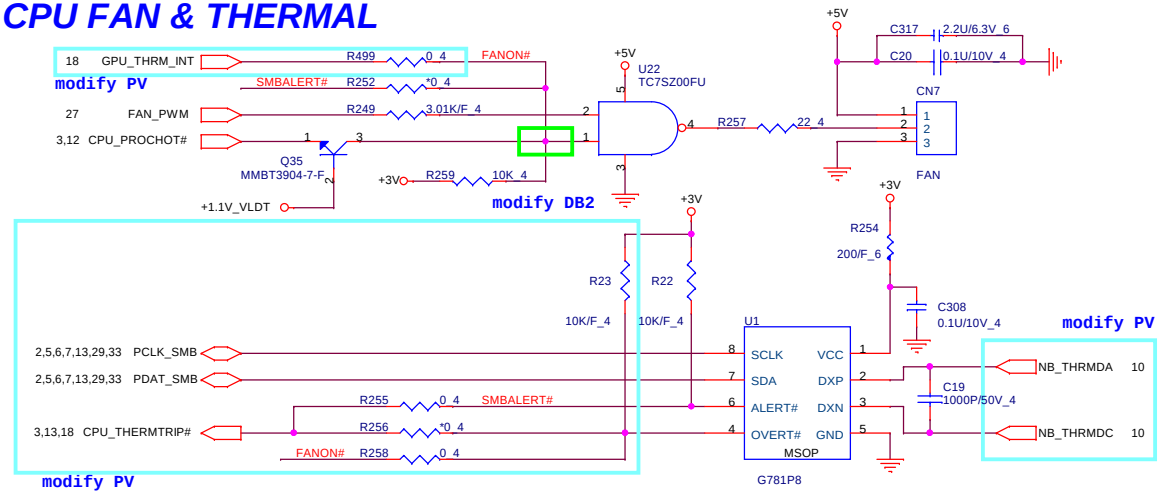



# POWER BOTTON CONNECT

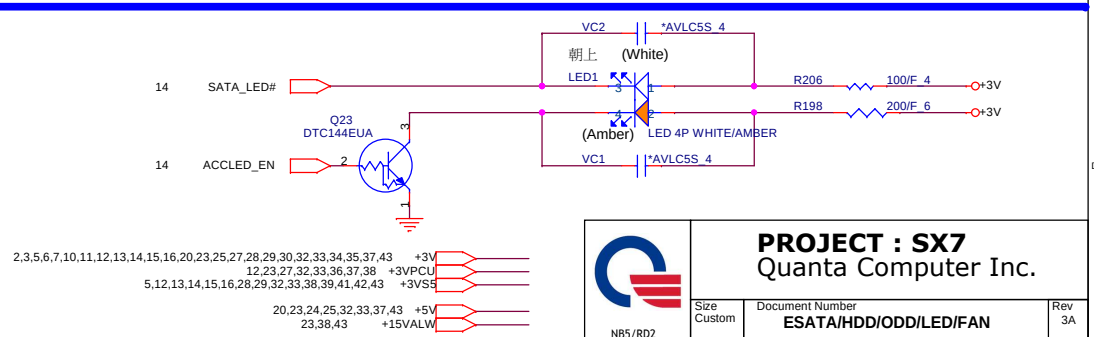



1. +3VPCU(LIDSWITCH PWR)
2. +PWLEDVCC(+3VPCU)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

# CPU FAN & THERMAL




# LED



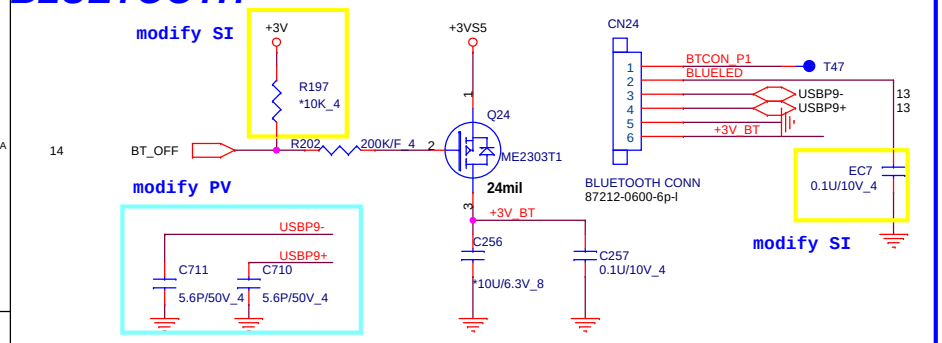

**PROJECT : SX7**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | ESATA/HDD/ODD/LED/FAN | 3A |

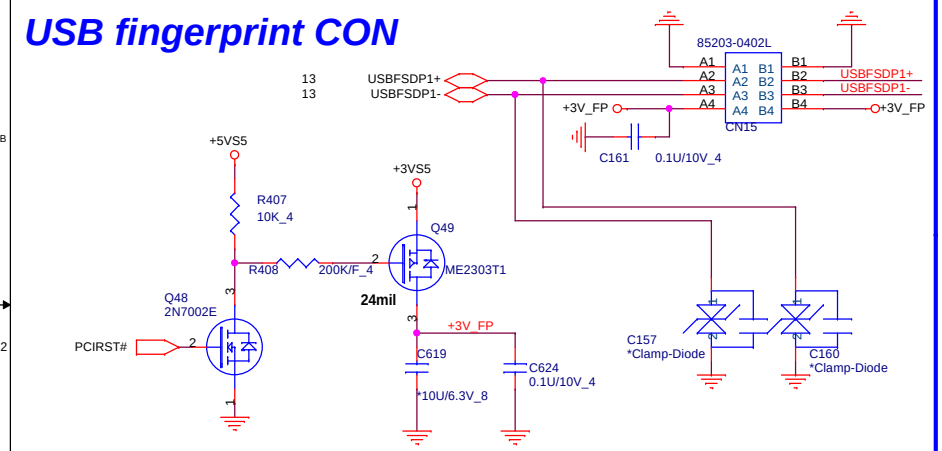
Date: Monday, March 15, 2010 | Sheet 31 of 43

NB5/RD2

# BLUETOOTH

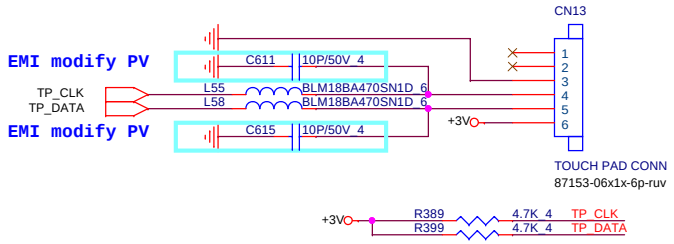



# USB fingerprint CON

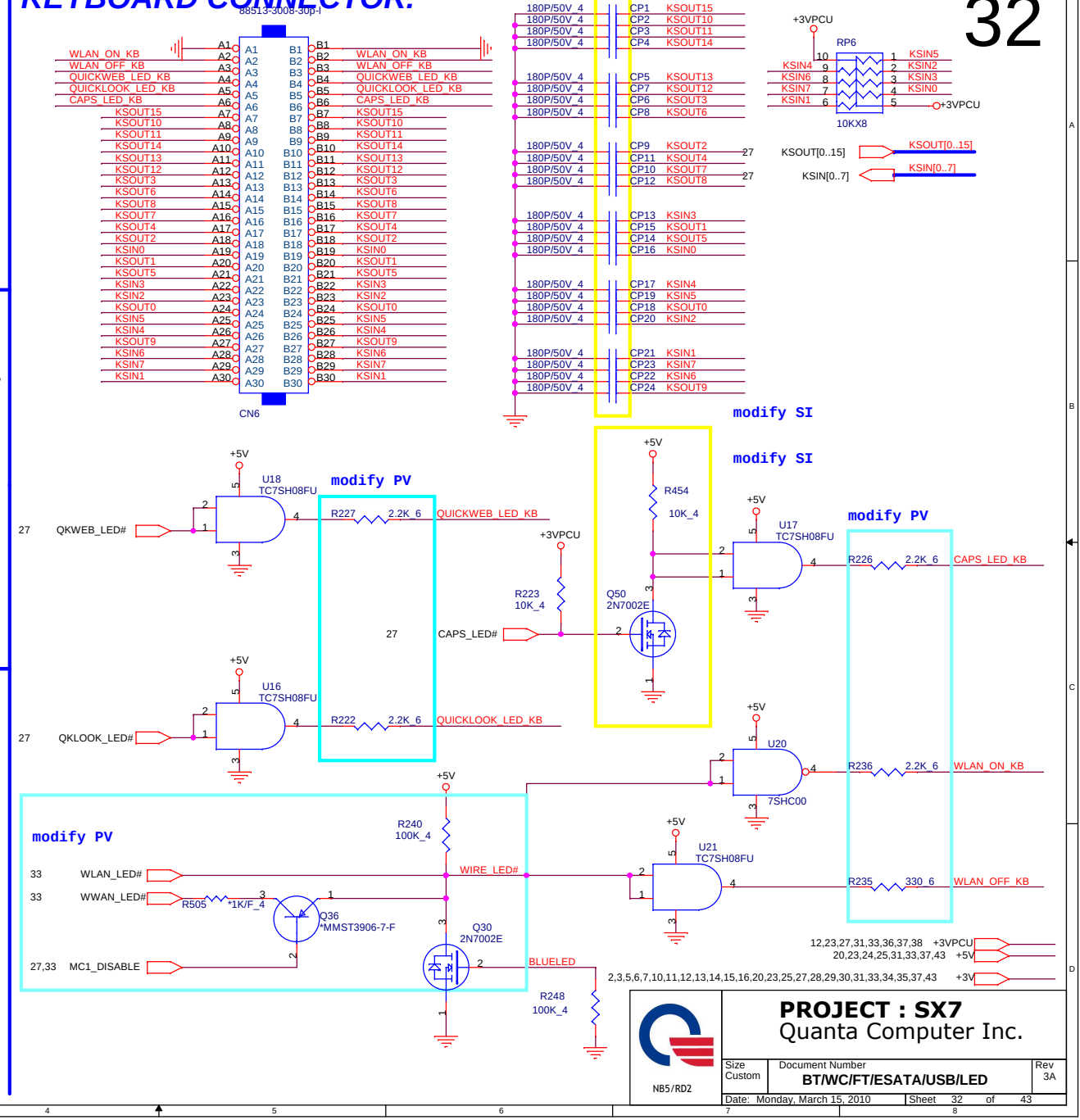



# TOUCH PAD CONNECTOR

| | |
|---|---|
| Pin1 | VDD |
| Pin2 | DATA |
| Pin3 | CLK |
| Pin4 | GND |
| Pin5 | X |
| Pin6 | X |




# KEYBOARD CONNECTOR.




**PROJECT : SX7**
Quanta Computer Inc.

NB5/RD2

| Size | Document Number | Rev |
|---|---|---|
| Custom | BT/WC/FT/ESATA/USB/LED | 3A |

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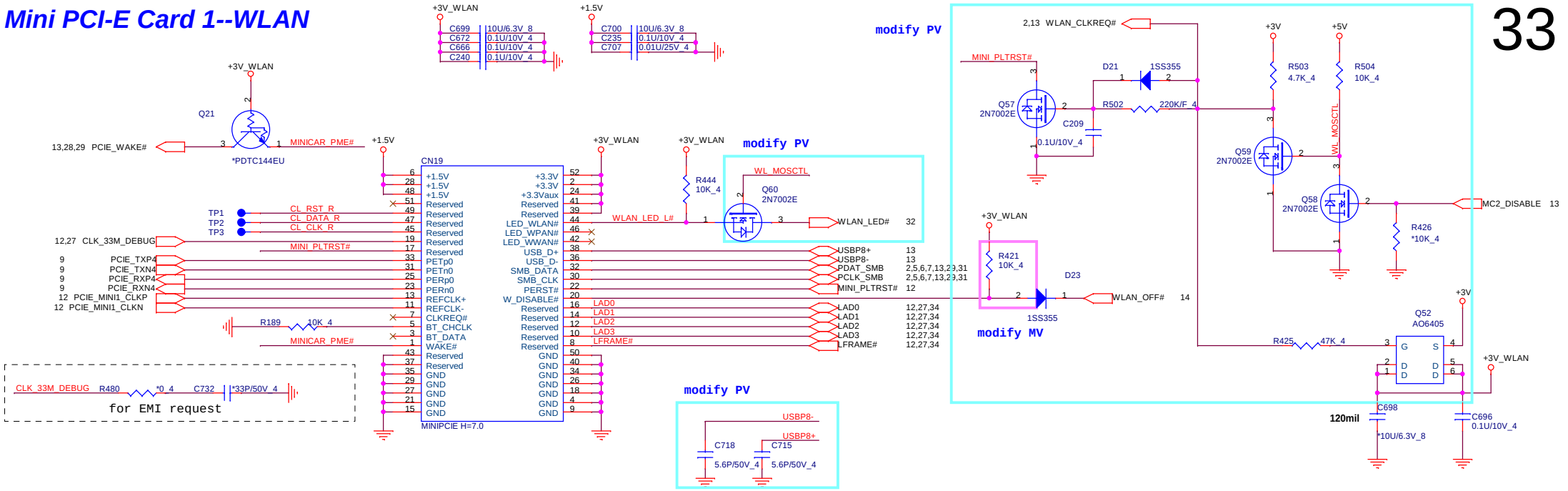
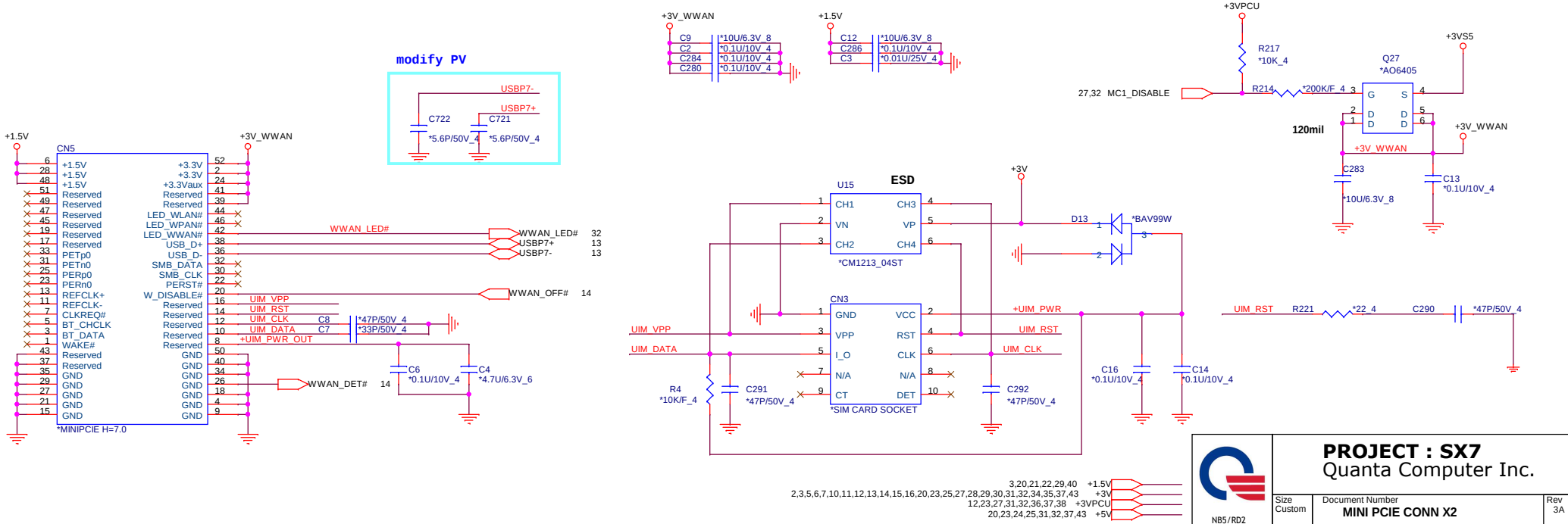
# Mini PCI-E Card 1--WLAN




# Mini PCI-E Card 2 --WWAN




**PROJECT : SX7**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | MINI PCIE CONN X2 | 3A |

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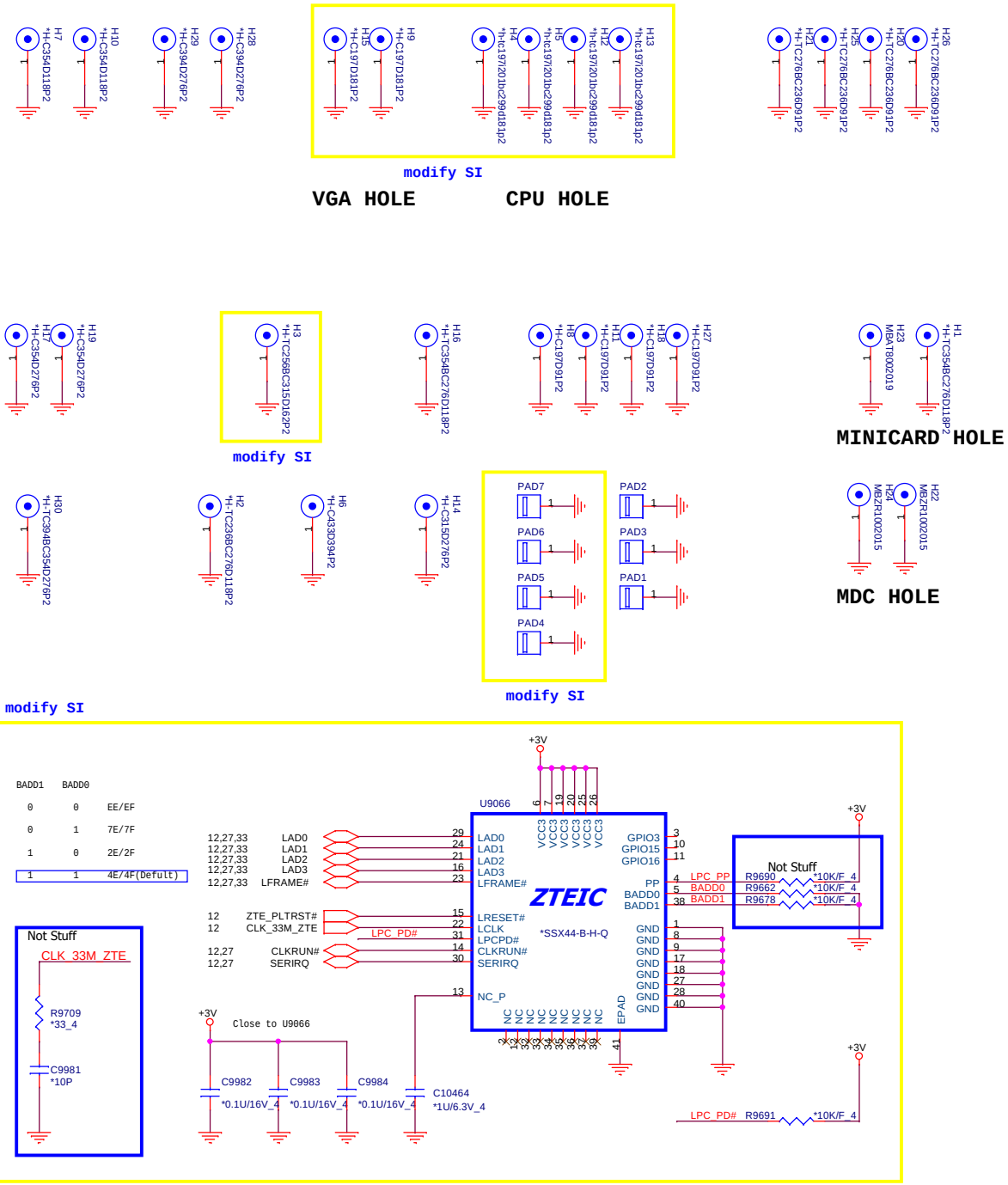
NB5/RD2




**PROJECT : SX7**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Hole, Nuts | 3A |

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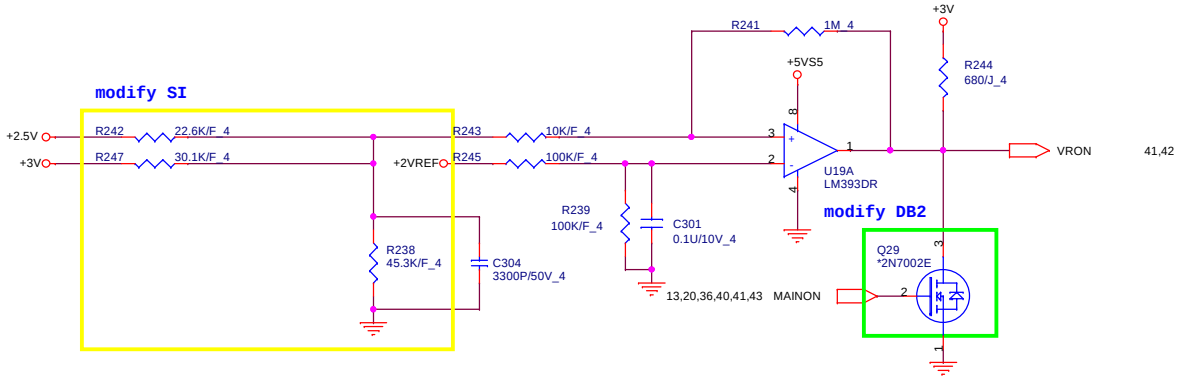
NB5/RD2




**PROJECT : SX7**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | **POWER Sequance** | 3A |

NB5/RD2

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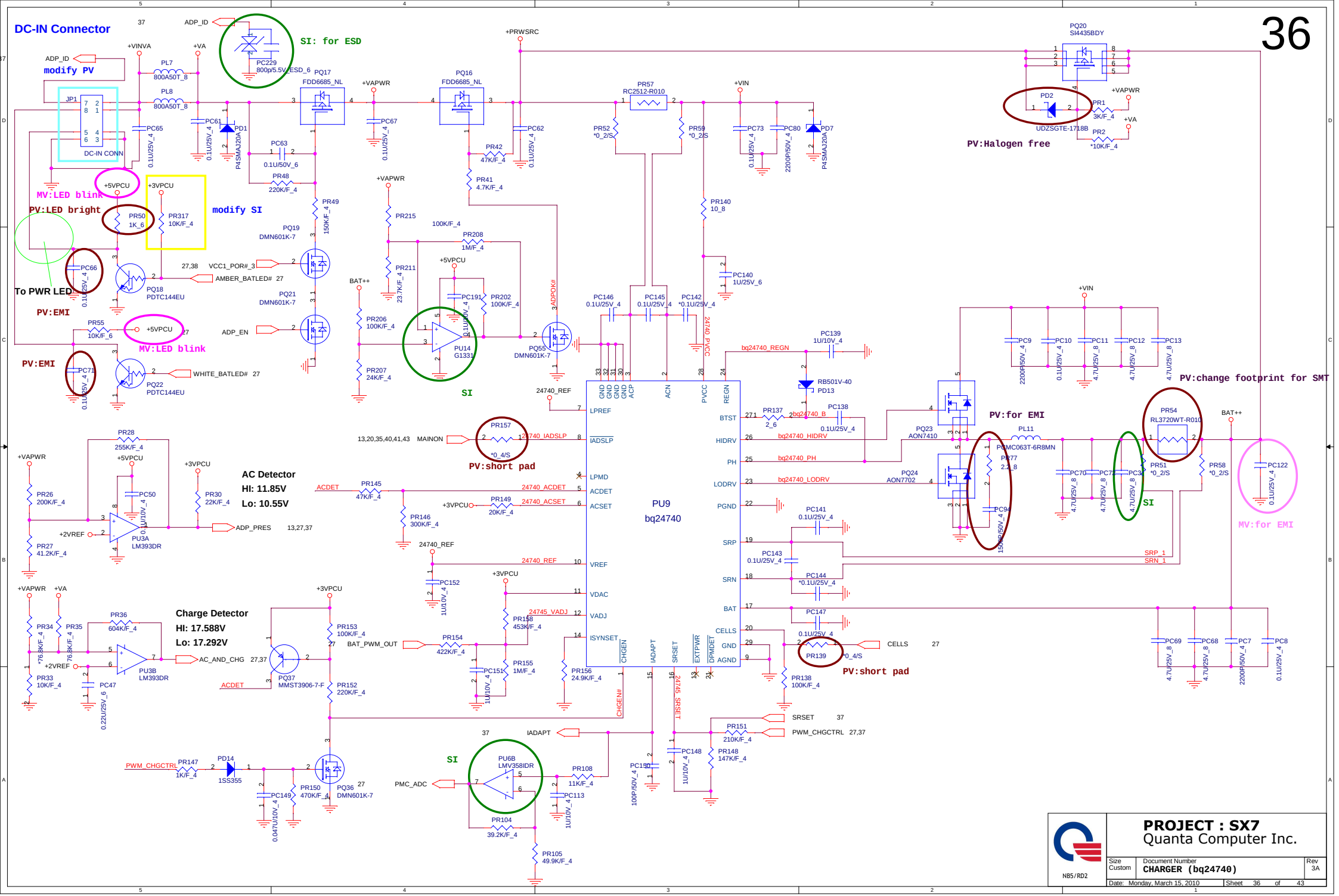
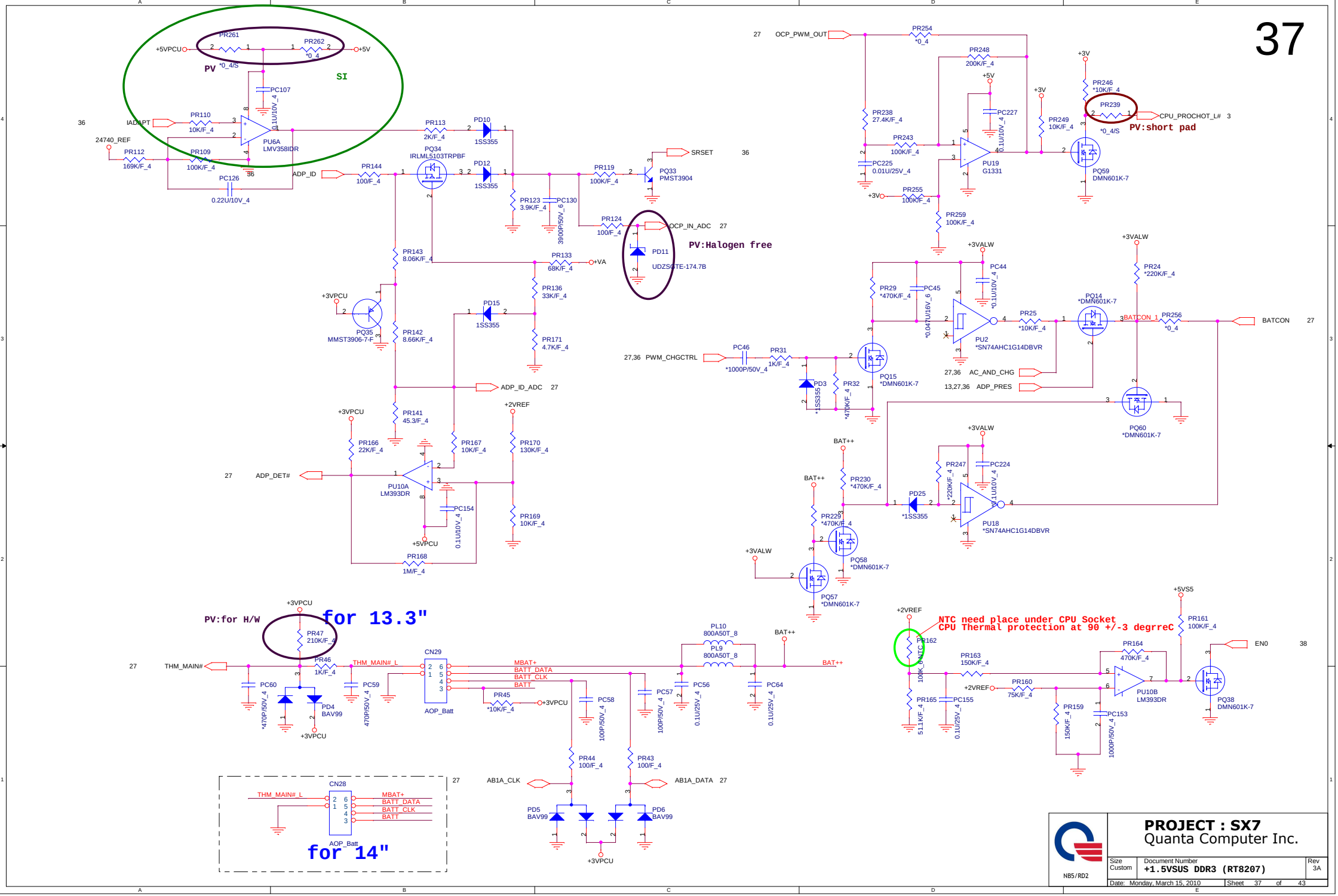

DC-IN Connector
SI: for ESD
modify PV
MV:LED blink
PV:LED bright
modify SI
To PWR LED
PV:EMI
PV:Halogen free
PV:change footprint for SMT
PV:for EMI
SI
MV:for EMI
PV:short pad
AC Detector
HI: 11.85V
Lo: 10.55V
Charge Detector
HI: 17.588V
Lo: 17.292V
PU9
bq24740
PU14
G1331
PU3A
LM393DR
PU3B
LM393DR
PU6B
LMV358IDR
PQ17
FDD6685_NL
PQ16
FDD6685_NL
PQ20
SI4435BDY
PQ55
DMN601K-7
PQ36
DMN601K-7
PQ37
MMST3906-7-F
PQ23
AON7410
PQ24
AON7702
PGMC063T-6R8MN
RL3720WT-R010
PROJECT : SX7
Quanta Computer Inc.
Size Custom
Document Number
CHARGER (bq24740)
Rev 3A
Date: Monday, March 15, 2010
Sheet 36 of 43
N85/RD2




**PROJECT : SX7**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | +1.5VSUS DDR3 (RT8207) | 3A |

N85/RD2

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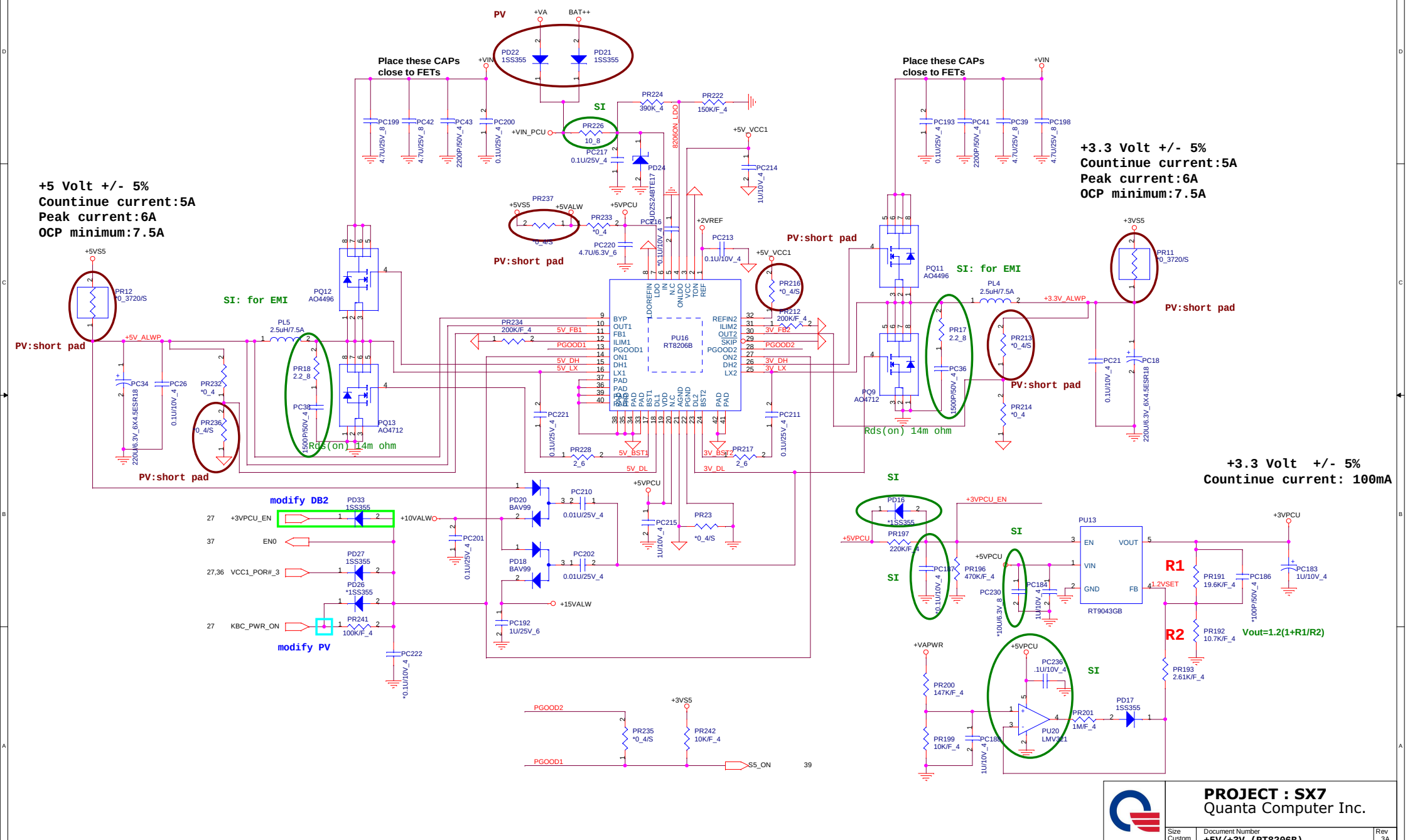
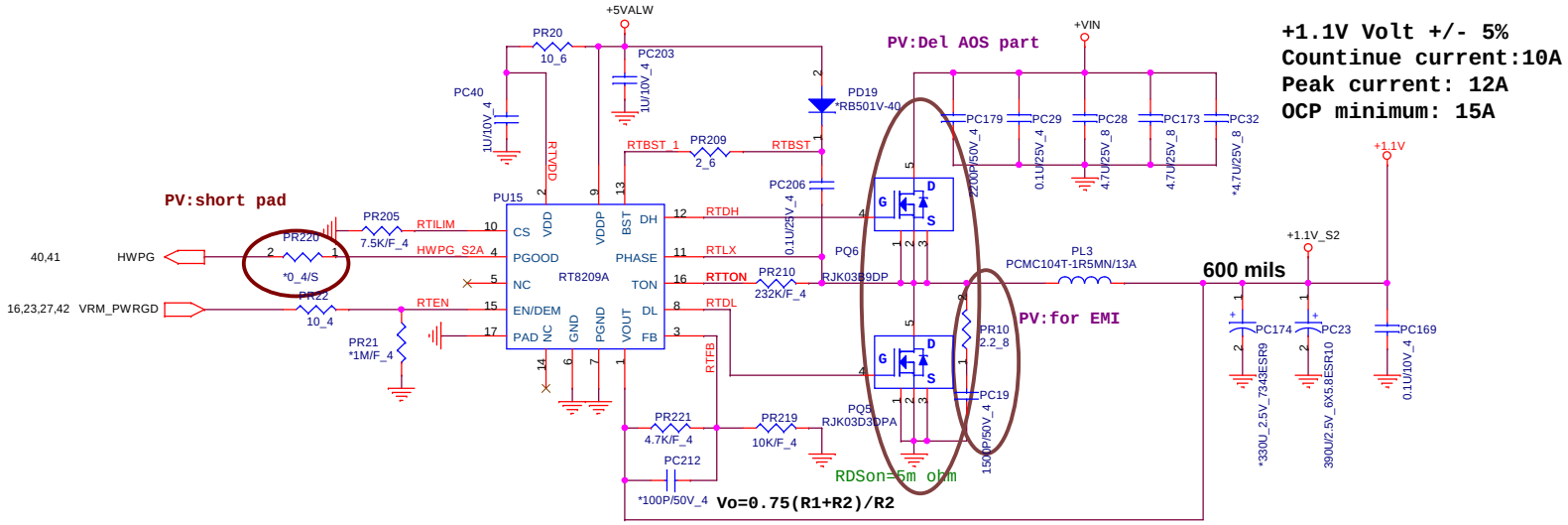
# DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

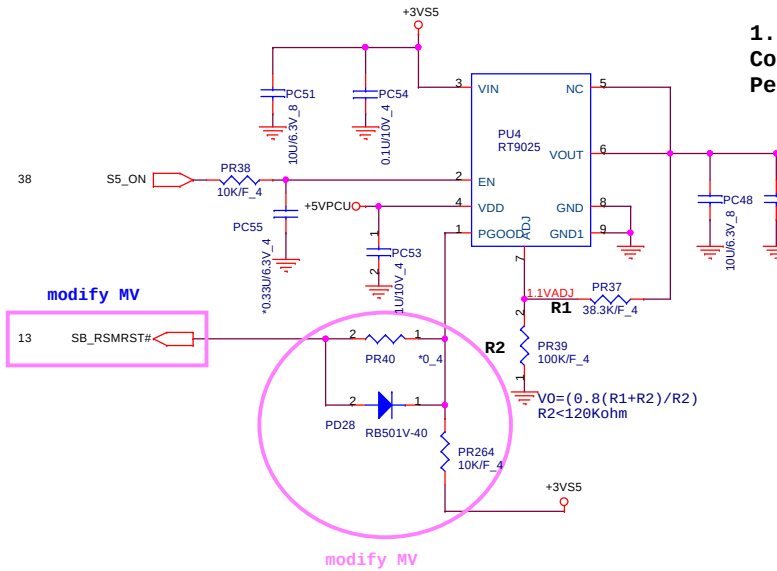


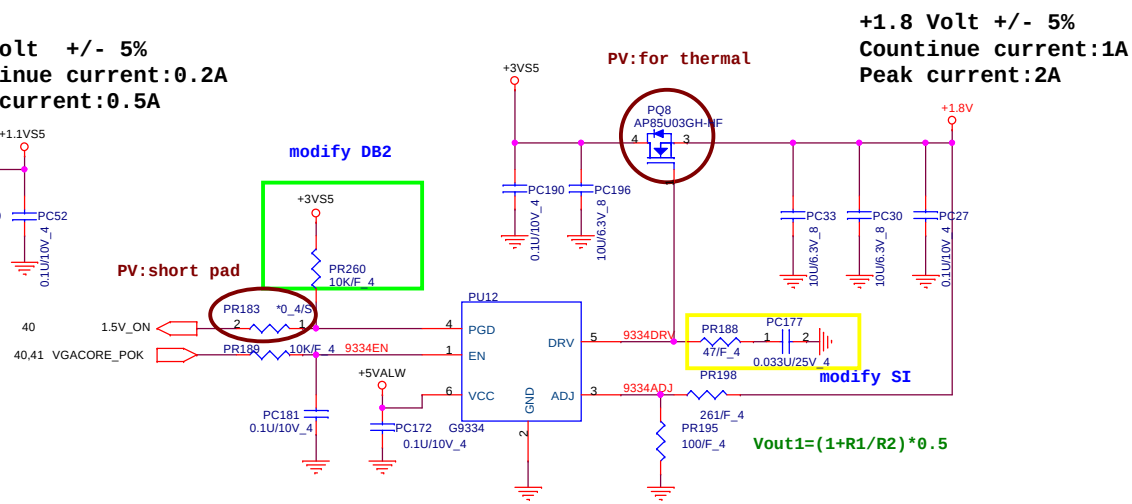



| | |
|---|---|
| **PROJECT : SX7** | |
| Quanta Computer Inc. | |
| Size: Custom | Document Number: +5V/+3V (RT8206B) | Rev: 3A |
| Date: Monday, March 15, 2010 | Sheet 38 of 43 |

N85/RD2




**PROJECT : SX7**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | VGA Core/+1.8VGFX/1.0VGFX | 3A |

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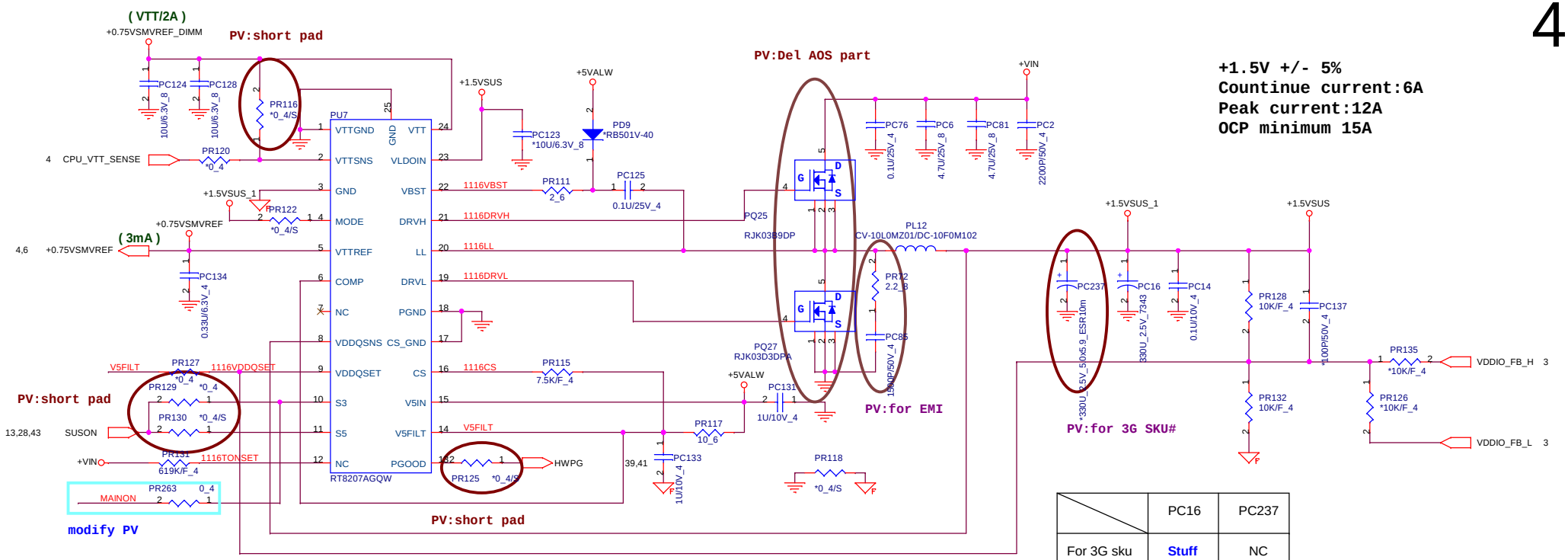
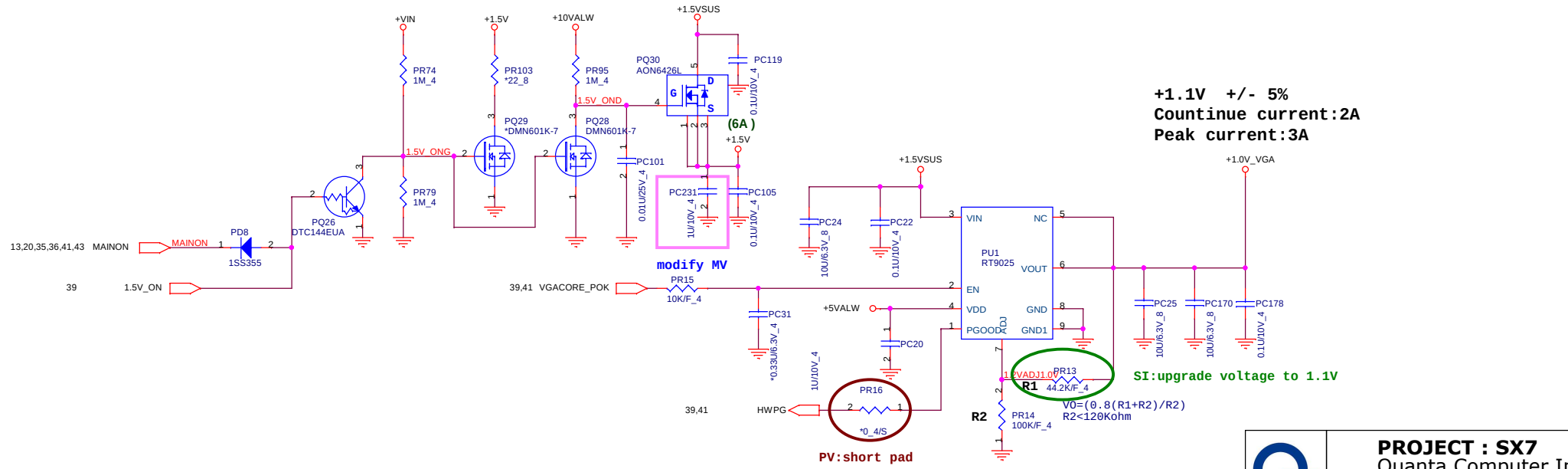
NB5/RD2




| | PC16 | PC237 |
|---|---|---|
| For 3G sku | **Stuff** | NC |
| non 3G sku | NC | **Stuff** |




**PROJECT : SX7**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | DDR3 (RT8207) | 3A |

NB5/RD2

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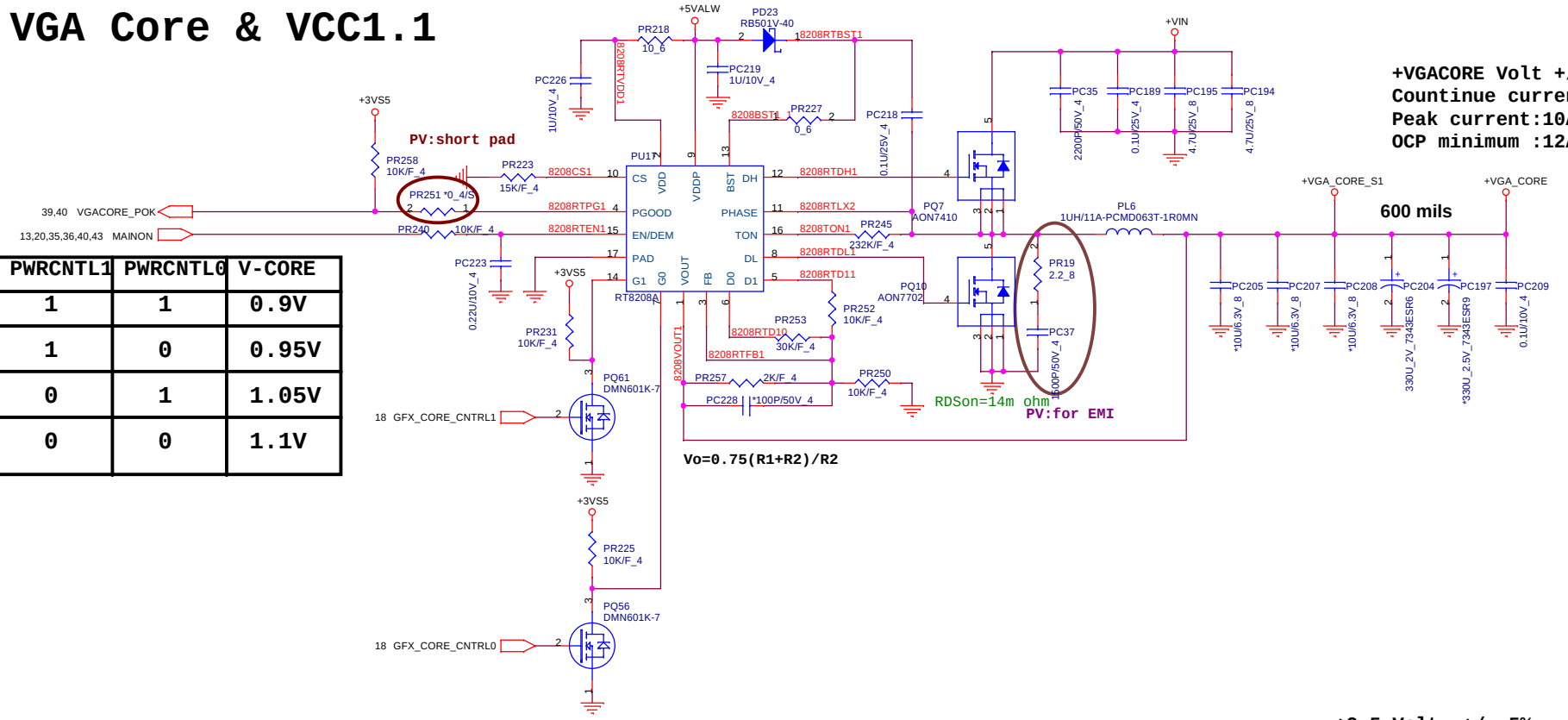
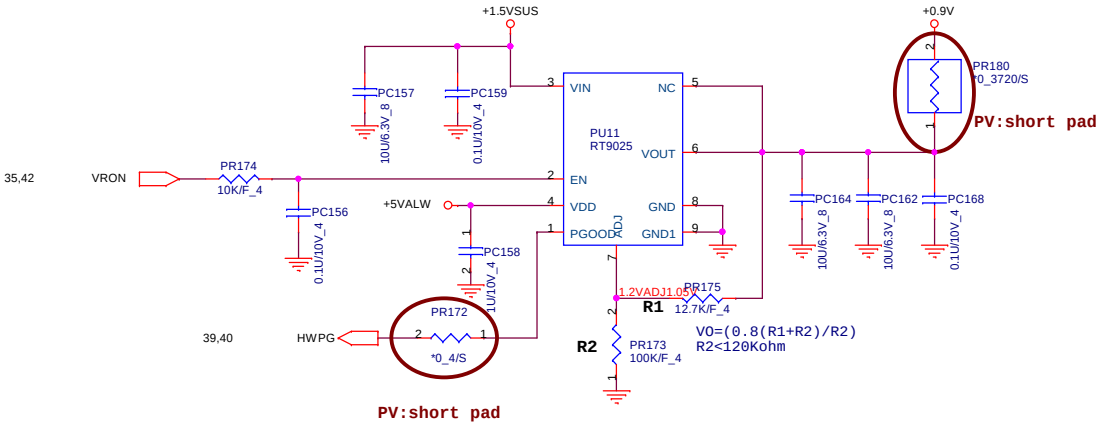
# VGA Core & VCC1.1

| | PWRCNTL1 | PWRCNTL0 | V-CORE |
|---|---|---|---|
| | 1 | 1 | 0.9V |
| | 1 | 0 | 0.95V |
| | 0 | 1 | 1.05V |
| | 0 | 0 | 1.1V |

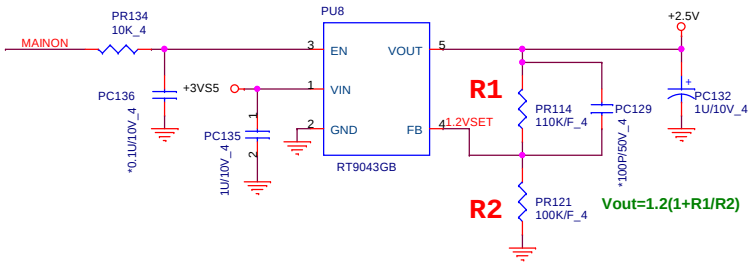



+VGACORE Volt +/- 5%
Countinue current:8A
Peak current:10A
OCP minimum :12A

+0.9V +/- 5%
Countinue current:1.5A
Peak current:2A




+2.5 Volt +/- 5%
Countinue current: 200mA
Peak current: 600mA




**PROJECT : SX7**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | VGA Core/+1.8VGFX/1.0VGFX | 3A |

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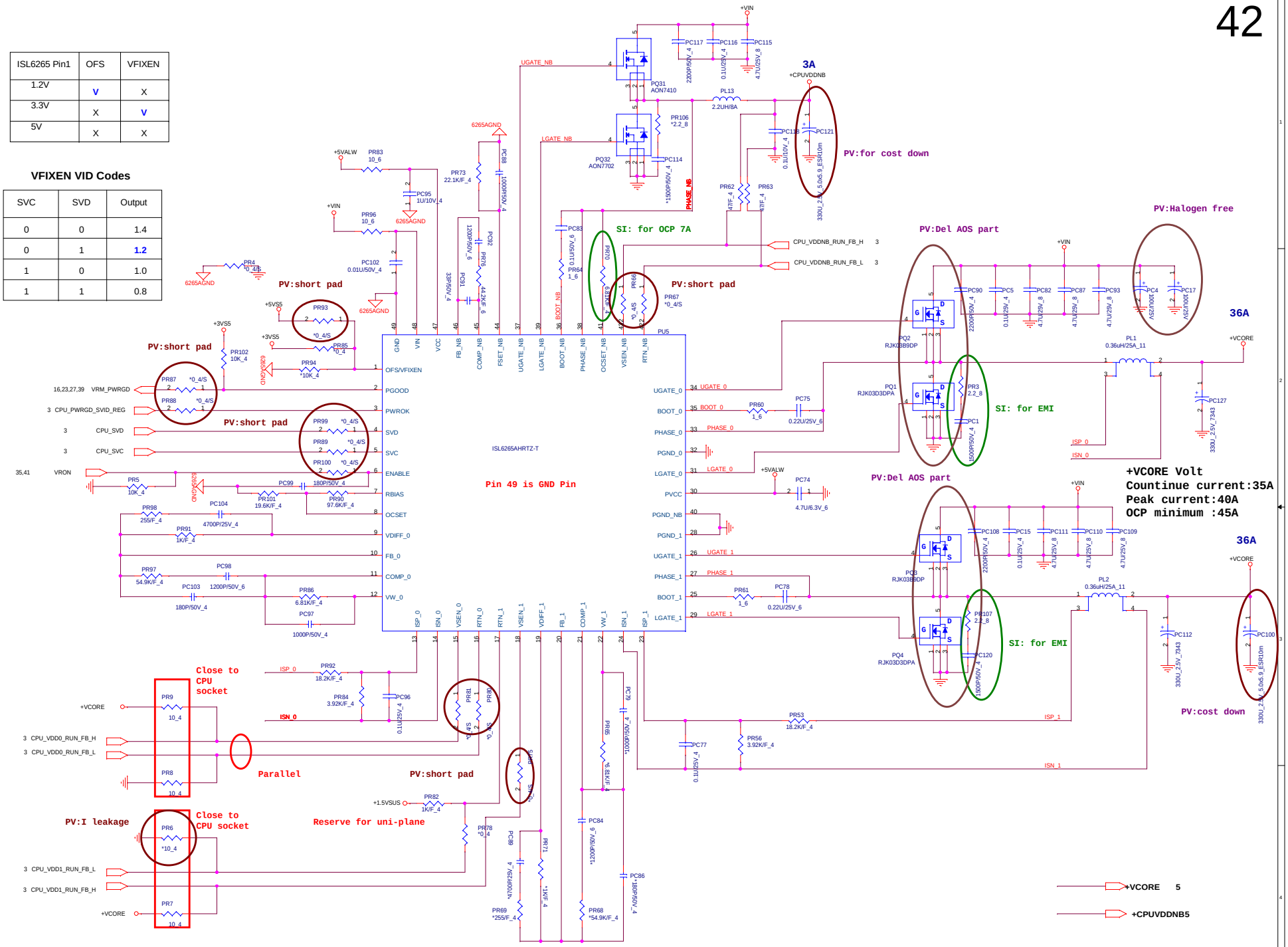
NB5/RD2

| ISL6265 Pin1 | OFS | VFIXEN |
|---|---|---|
| 1.2V | V | X |
| 3.3V | X | V |
| 5V | X | X |

**VFIXEN VID Codes**

| SVC | SVD | Output |
|---|---|---|
| 0 | 0 | 1.4 |
| 0 | 1 | 1.2 |
| 1 | 0 | 1.0 |
| 1 | 1 | 0.8 |




**PROJECT : SX7**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| C | CPU_CORE(ISL6265) | 3A |

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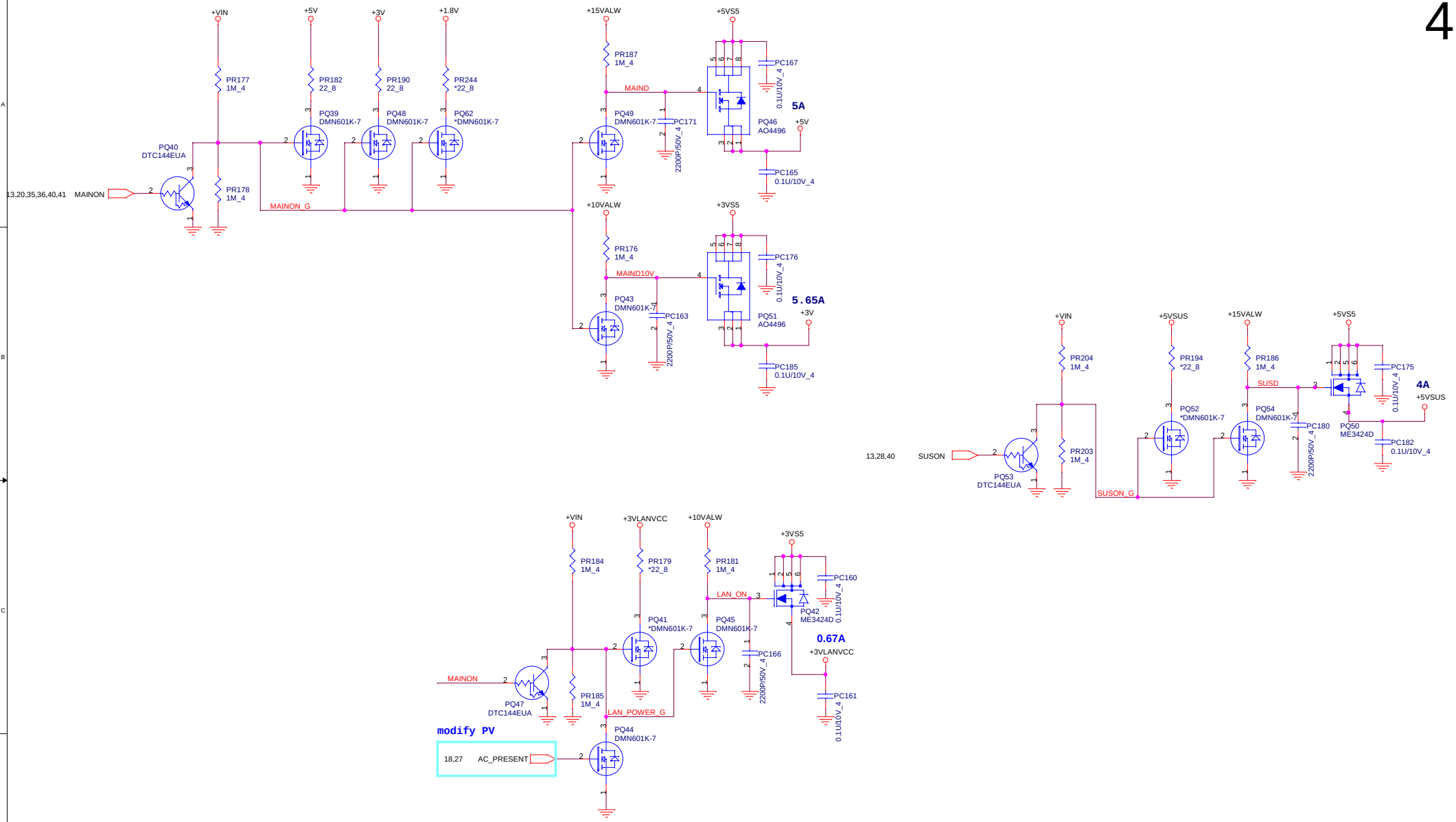


**PROJECT : SX7**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | DISCHARGE/3VS5/5VS5/LAN | 3A |

N85/RD2

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