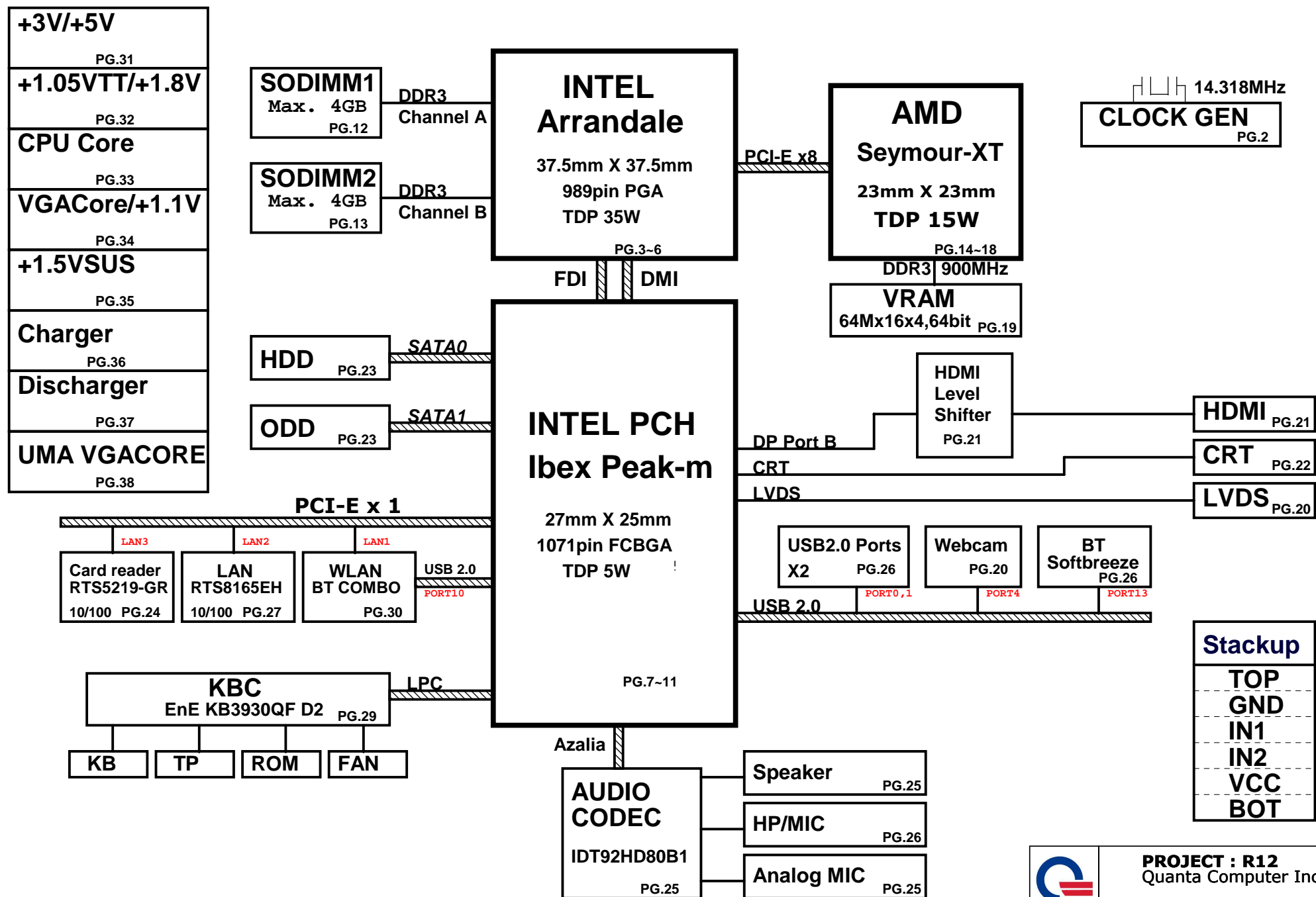


R12 INTEL UMA/DISCRETE SYSTEM DIAGRAM



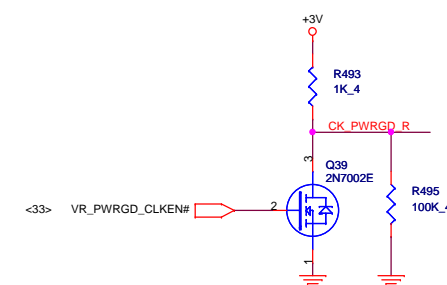
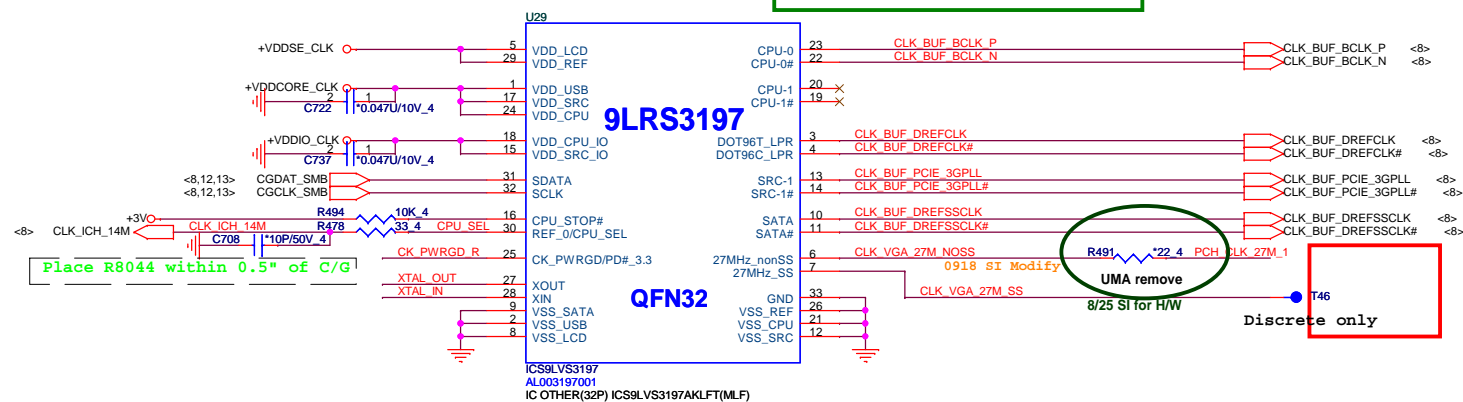
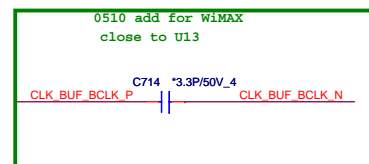
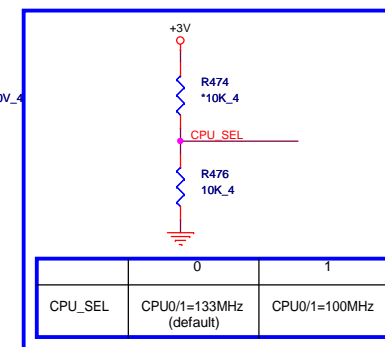
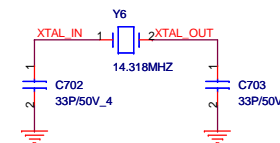
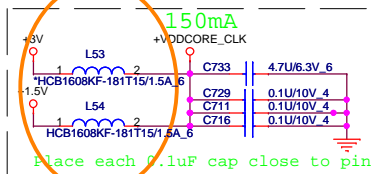
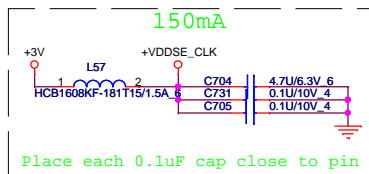
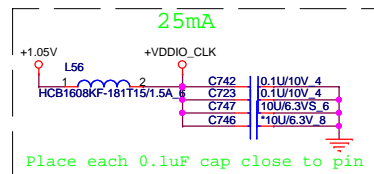
PROJECT : R12
Quanta Computer Inc.

Size
Custom

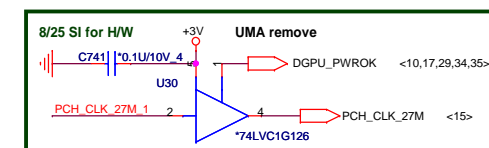
Document Number
BLOCK DIAGRAM

Rev
1A

Date: Tuesday, September 14, 2010 Sheet 1 of 39



Vender	Part	Part Number	Part Description
ICS	ICS9LVS3197	AL003197000	IC OTHER(32P) ICS9LVS3197AKLFT(MLF)
Realtek	RTM890N-632	AL000890000	IC OTHER(32P) RTM890N-632-GRT(QFN)
Silego	SLG8LV595VTR	AL000595000	IC OTHER(32P)SLG8LV595VTR(QFN)



+1.05V <7,8,9,11,39>

+1.5V <5,30>

+3V <3,7,8,9,10,11,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36>

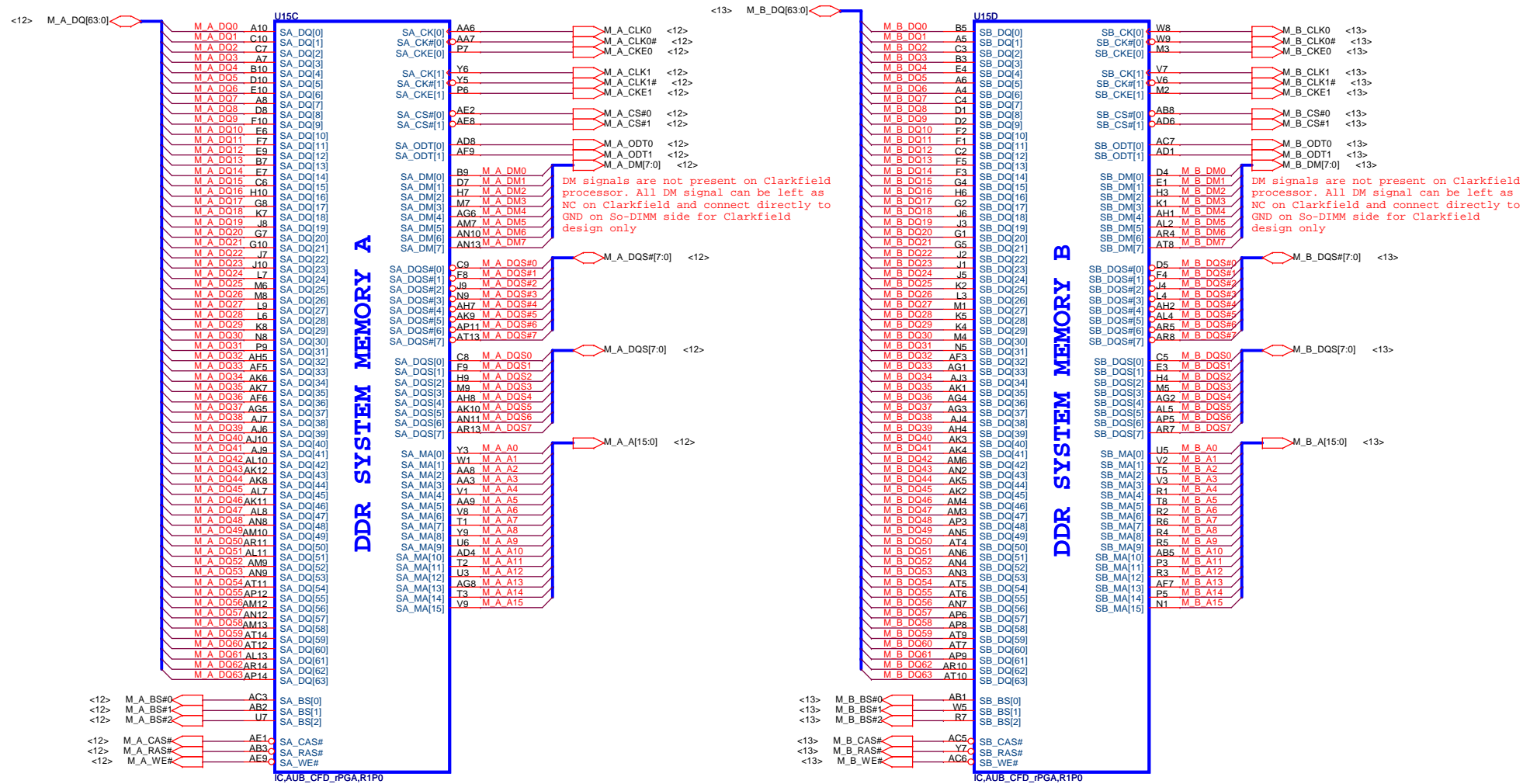


PROJECT : R12
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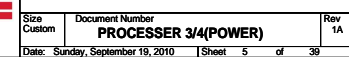
Size	Document Number	Rev
Custom	Clock Gen(9LRS3197)	1A
Date:	Sunday, September 19, 2010	Sheet 2 of 39

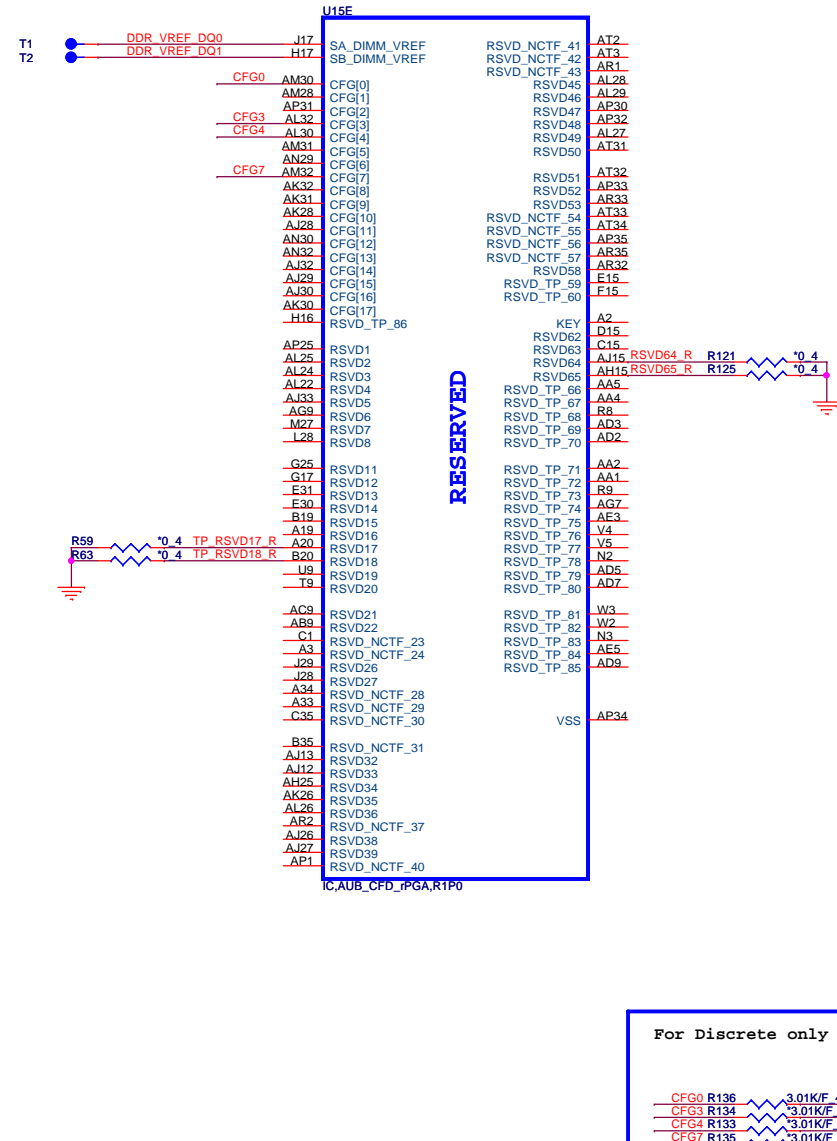
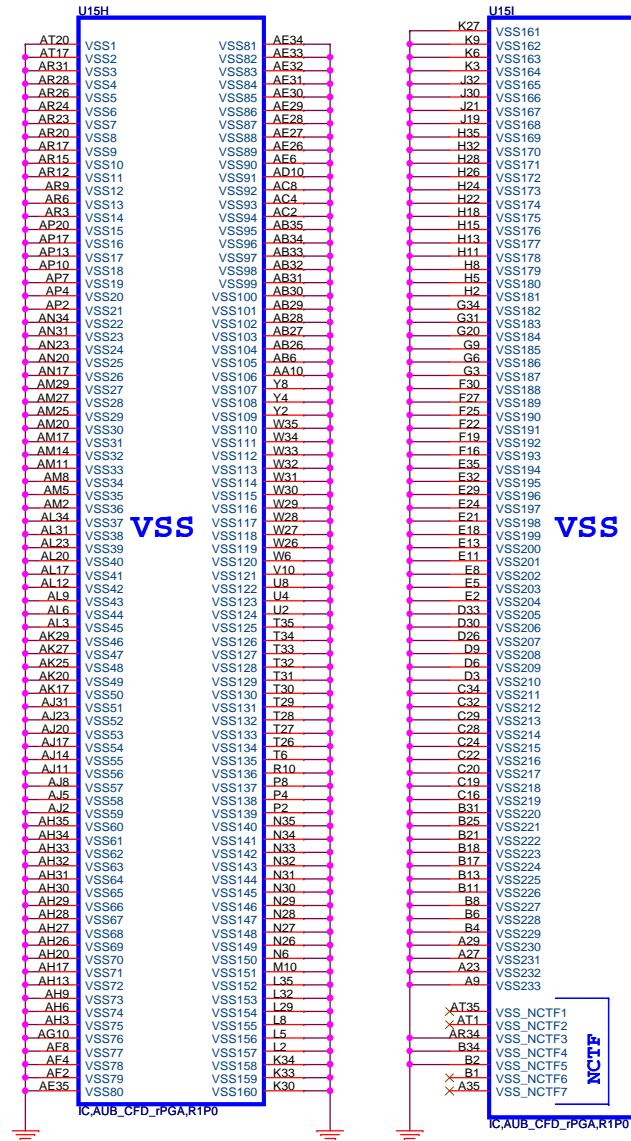
03

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

For Discrete only

CFG0 R136 3.01K/F 4
CFG1 R137 3.01K/F 4
CFG2 R138 3.01K/F 4
CFG3 R139 3.01K/F 4

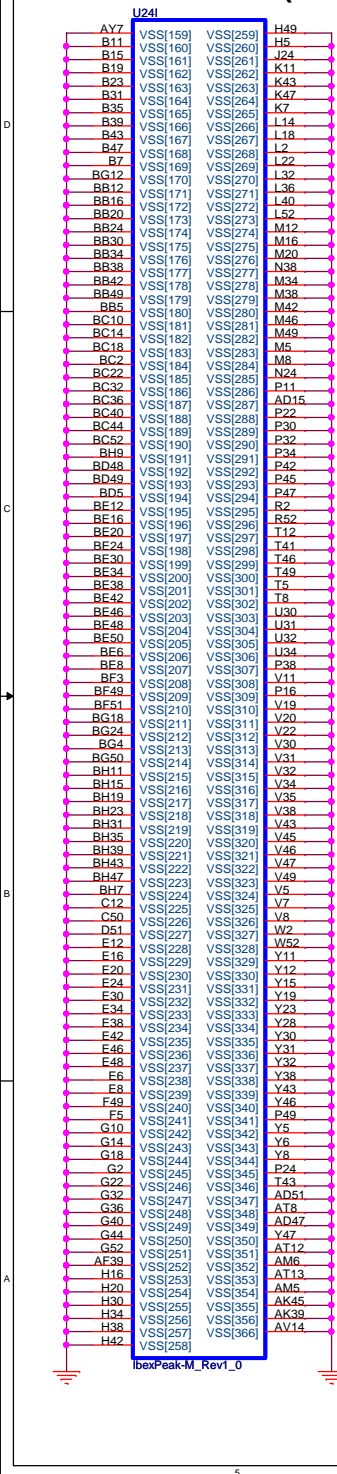
CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

PROJECT : R12
Quanta Computer Inc.

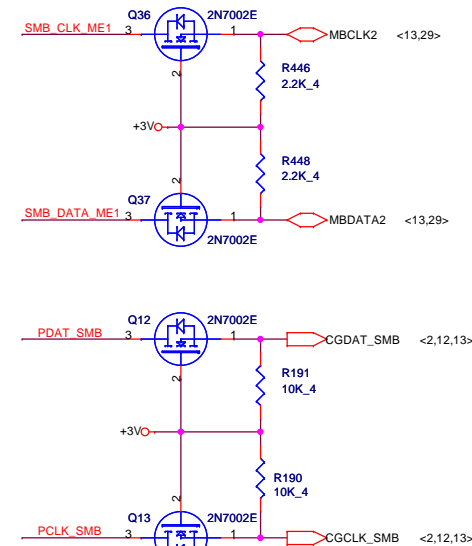
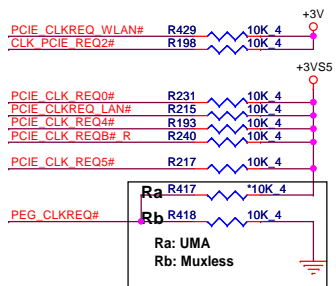
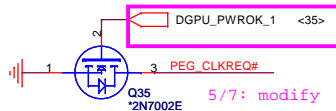
Size Custom Document Number
PROCESSOR 4/4 (GND)

Date: Sunday, September 19, 2010 | Sheet 6 of 39

Size Custom	Document Number PCH 1/5 (SATA,HDA,LPC)
Date: Sunday, September 19, 2010	Sheet 7 of 39

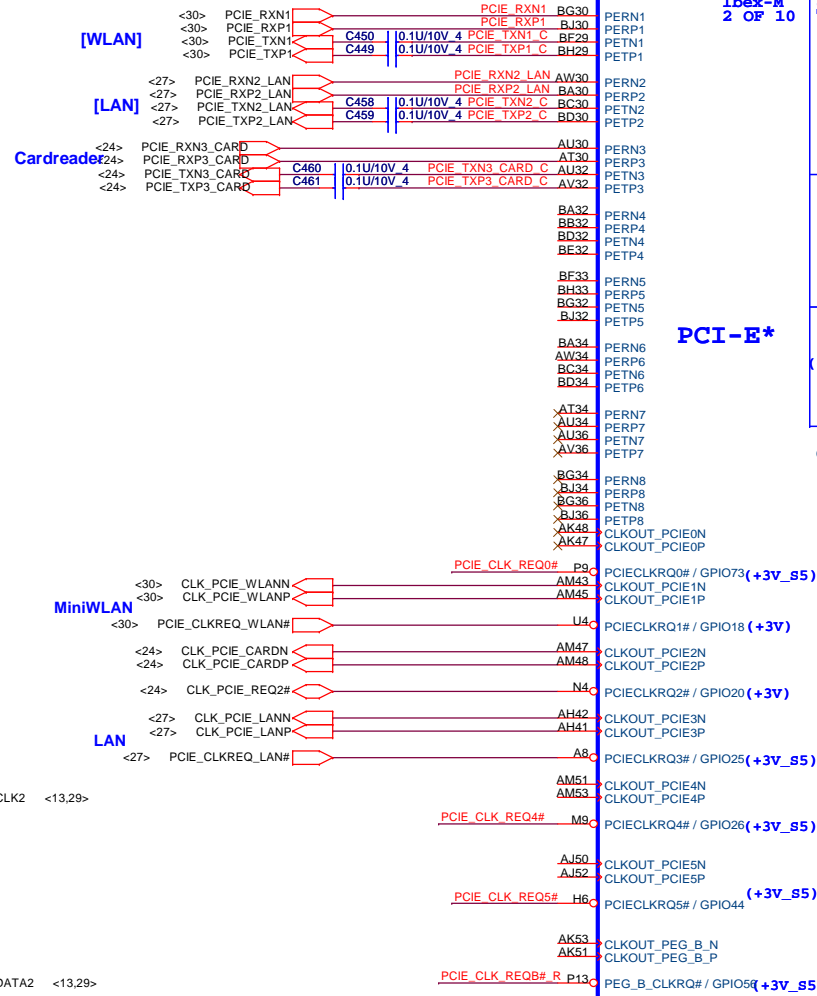


PEG Clock detect (SG only)



IBEX PEAK-M (PCI-E,SMBUS,CLK)

U24B



SMBus

(+3V_S5) SMBALERT# / GPIO11

SMBCLK

(+3V_S5) SML0ALERT# / GPIO69

SML0DATA

(+3V_S5) SML1ALERT# / GPIO74

(+3V_S5) SML1CLK / GPIO58

(+3V_S5) SML1DATA / GPIO75

Controller

Link

PEG

(+3V_S5) PEG_A_CLKREQ# / GPIO47

CLKOUT_PEG_A_N

CLKOUT_PEG_A_P

CLKOUT_DMI_N

CLKOUT_DMI_P

CLKOUT_DP_N / CLKOUT_BCLK1_N

CLKOUT_DP_P / CLKOUT_BCLK1_P

CLKIN_DMI_N

CLKIN_DMI_P

CLKIN_BCLK_N

CLKIN_BCLK_P

CLKIN_DOT_96N

CLKIN_DOT_96P

CLKIN_SATA_N / CKSSCD_N

CLKIN_SATA_P / CKSSCD_P

REFCLK14IN

CLKIN_PCIOLOOPBACK

XTAL25_IN

XTAL25_OUT

XCLK_RCOMP

(+3V) CLKOUTFLEX0 / GPIO64

(+3V) CLKOUTFLEX1 / GPIO65

(+3V) CLKOUTFLEX2 / GPIO66

(+3V) CLKOUTFLEX3 / GPIO67

Clock Flex

CLKOUT_FLEX0

CLKOUT_FLEX1

CLKOUT_FLEX2

CLKOUT_FLEX3

CLKOUT_FLEX4

CLKOUT_FLEX5

CLKOUT_FLEX6

CLKOUT_FLEX7

CLKOUT_FLEX8

CLKOUT_FLEX9

CLKOUT_FLEX10

CLKOUT_FLEX11

CLKOUT_FLEX12

CLKOUT_FLEX13

CLKOUT_FLEX14

CLKOUT_FLEX15

CLKOUT_FLEX16

CLKOUT_FLEX17

CLKOUT_FLEX18

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CLKOUT_FLEX202

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CLKOUT_FLEX208

CLKOUT_FLEX209

CLKOUT_FLEX210

CLKOUT_FLEX211

CLKOUT_FLEX212

CLKOUT_FLEX213

CLKOUT_FLEX214

CLKOUT_FLEX215

CLKOUT_FLEX216

CLKOUT_FLEX217

CLKOUT_FLEX218

CLKOUT_FLEX219

CLKOUT_FLEX220

CLKOUT_FLEX221

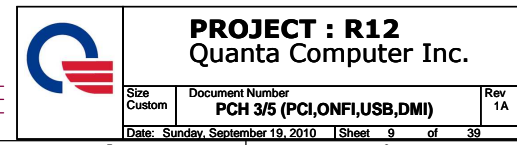
CLKOUT_FLEX222

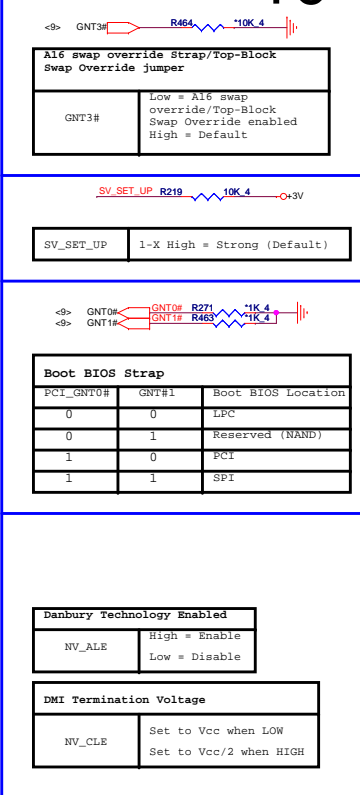
CLKOUT_FLEX223

CLKOUT_FLEX224

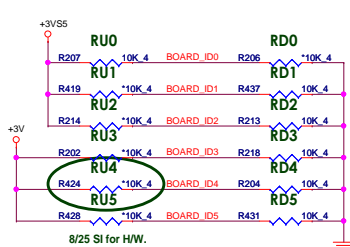
CLKOUT_FLEX225




IBEX PEAK-M (PCI,USB,NVRAM)










Board ID	ID0 GPIO24	ID1 GPIO45	ID2 GPIO57	ID3 GPIO34	ID4 GPIO35	ID5 GPIO38
UMA/DIS	0=UMA 1=DIS.					
Reserve		0=No 1=Yes				
Reserve			0=No 1=Yes			
Reserve				0=No 1=Yes		
Reserve					0=No 1=Yes	
Reserve						0=No 1=Yes





<7.25> AC2_SPKR  *IK_4  R430  +3V

<7.29> GPIO3_E  R253  *100K_4  +3V5S

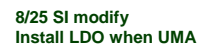
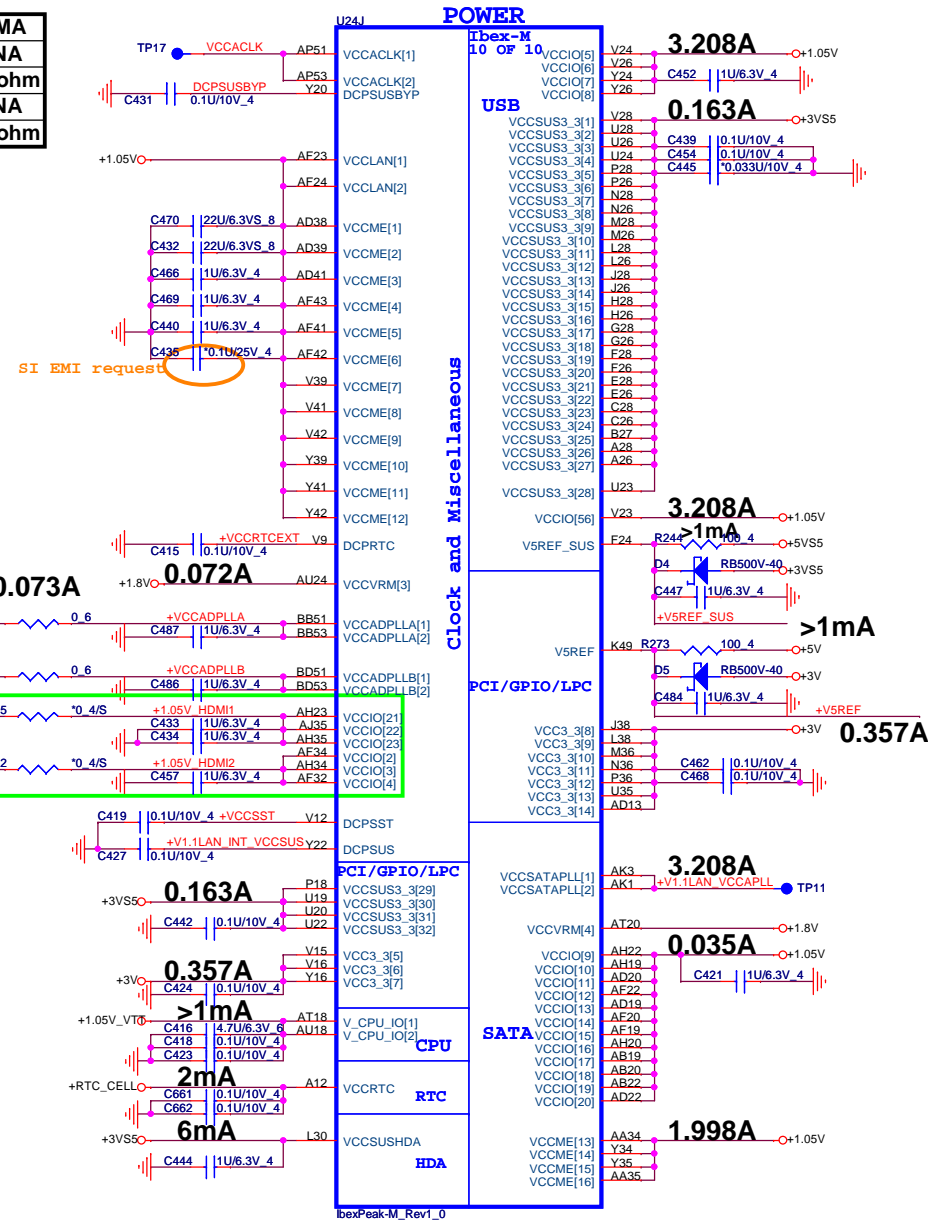
<3.5,11,29,32,33,38> +1.05V_V1T 

12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36<3.5,11,32> +1.8V 

<3.7,8.9,11,26,31,32,34,35,36,38> +3V 

+3V5S 

	DIS	UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm

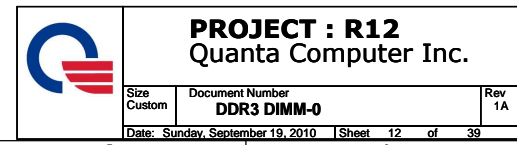


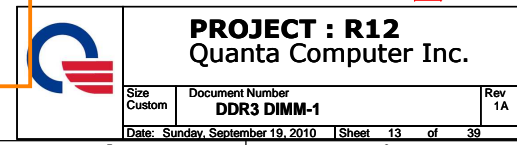
	<2,7,8,9,39>	+1.05V	
	<3,5,10,29,32,33,38>	+1.05V_VTT	
		<5,32>	+1.8V
<2,3,7,8,9,10,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36>			+3V
	<3,7,8,9,10,26,31,32,34,35,36,38>		+3V5S
	<17,21,22,23,25,28,30,36>		+5V
	<20,26,31,32,33,34,35,36,38,39>		+5V5S

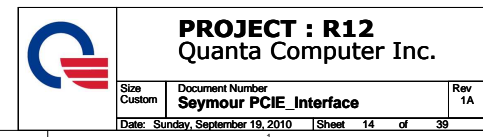


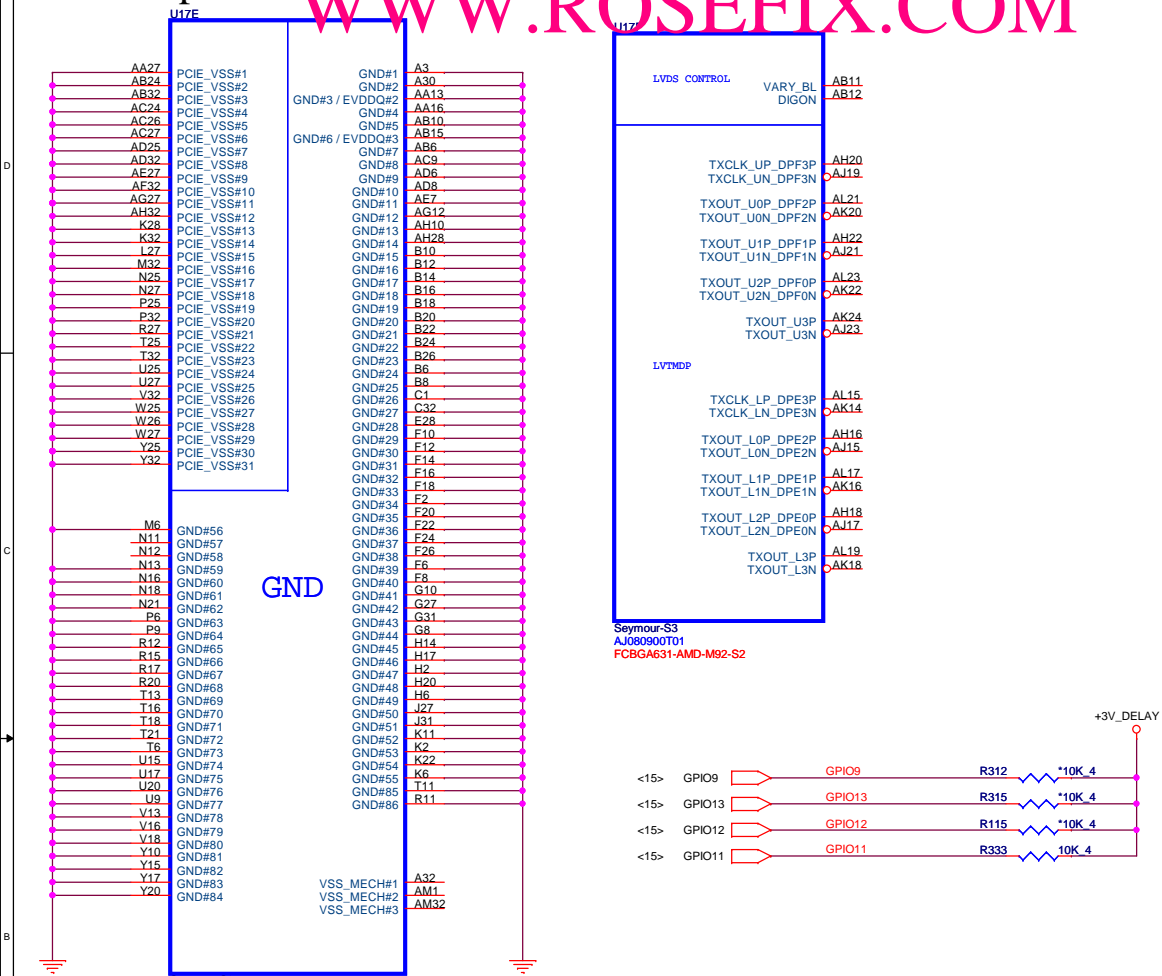
PROJECT : R12
Quanta Computer Inc.

Size Custom	Document Number PCH 5/5 (POWER)	Rev 1A
Date: Sunday, September 19, 2010		Sheet 11 of 39

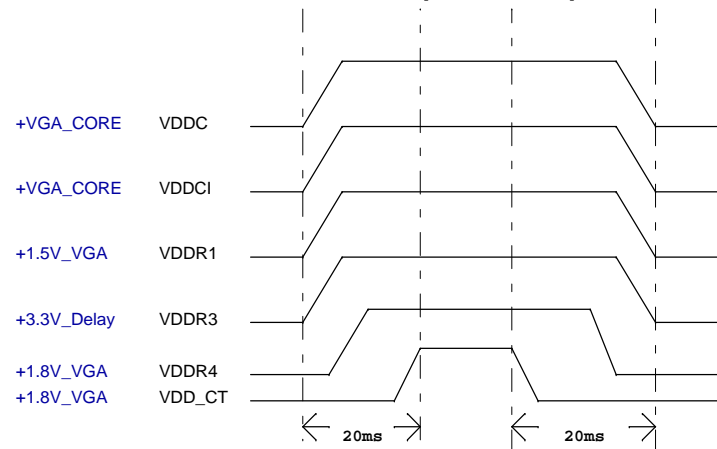








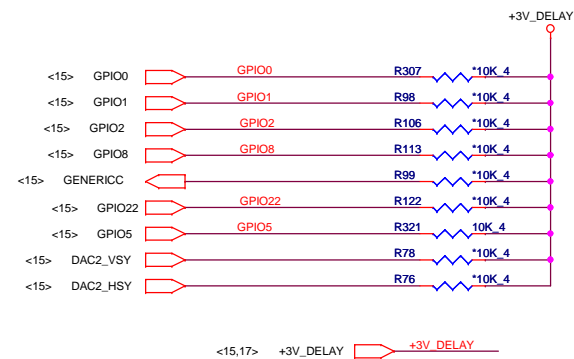
Power Up/Down Sequence



Memory Aperture size

GPIO9	GPIO13	GPIO12	GPIO11
BIOSROM	ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0
0	256M	0	1
0	64M	0	0
0	32M	0	1
0	512M	1	0
0	1G	1	0
0	2G	1	0
0	4G	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO21_BB_EN	



PROJECT : R12
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PROJECT : R12
Quanta Computer Inc.

1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)
2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

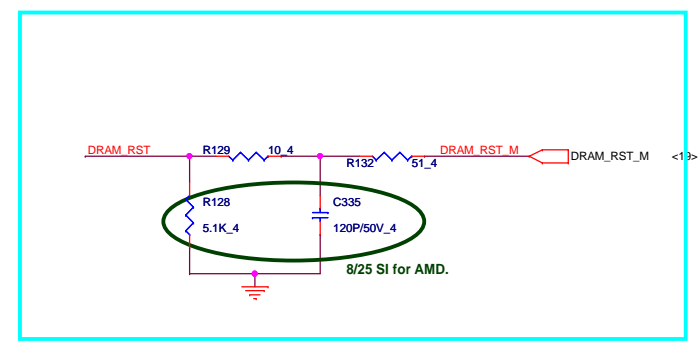
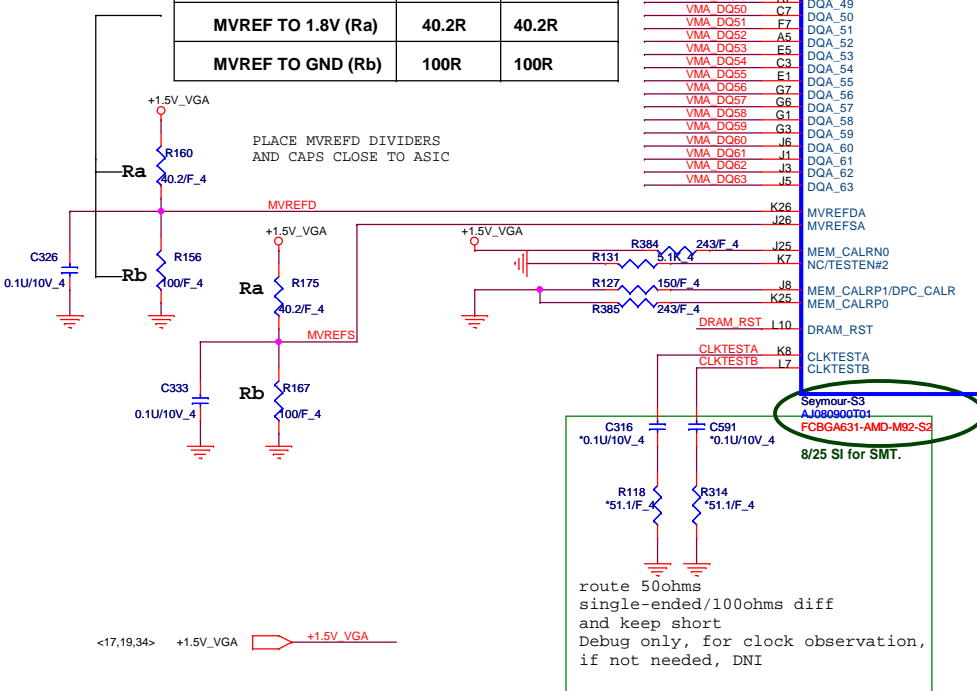
Rev
4A

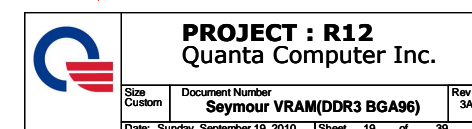
39

MAA_0	K17	VMA MA0
MAA_1	J20	VMA MA1
MAA_2	H23	VMA MA2
MAA_3	G23	VMA MA3
MAA_4	G24	VMA MA4
MAA_5	H24	VMA MA5
MAA_6	J19	VMA MA6
MAA_7	K19	VMA MA7
MAA_8	L14	VMA MA8
MAA_9	K14	VMA MA9
MAA_10	J11	VMA MA10
MAA_11	J13	VMA MA11
MAA_12	H11	VMA MA12
MAA_13/BA0	G16	VMA BA2
MAA_14/BA2	J16	VMA BA0
MAA_15/BA1	L15	VMA BA1
DQMA_0	E32	VMA DM0
DQMA_1	A30	VMA DM1
DQMA_2	E21	VMA DM2
DQMA_3	C21	VMA DM3
DQMA_4	E13	VMA DM4
DQMA_5	D12	VMA DM5
DQMA_6	E3	VMA DM6
DQMA_7	F4	VMA DM7
RDQSO_0	H28	VMA RDQSO
RDQSO_1	A27	VMA RDQST
RDQSO_2	C27	VMA RDQST
RDQSO_3	E19	VMA RDQSO3
RDQSO_4	E15	VMA RDQSO4
RDQSO_5	D10	VMA RDQSO5
RDQSO_6	G5	VMA RDQSO6
RDQSO_7	D6	VMA RDQSO7
WDQSO_0	A27	VMA WDQSO
WDQSO_1	H27	VMA WDQSO2
WDQSO_2	C23	VMA WDQSO2
WDQSO_3	C19	VMA WDQSO3
WDQSO_4	C15	VMA WDQSO4
WDQSO_5	E9	VMA WDQSO5
WDQSO_6	C5	VMA WDQSO6
WDQSO_7	H4	VMA WDQSO7
ODTA0	L18	VMA ODT0
ODTA1	K16	VMA ODT1
CLKA0	H26	VMA CLK0
CLKA0B	H25	VMA CLK0#
CLKA1	G9	VMA CLK1
CLKA1B	H9	VMA CLK1#
RASA0B	G22	VMA RAS0#
RASA1B	G17	VMA RAS1#
CASA0B	G19	VMA CAS0#
CASA1B	G16	VMA CAS1#
CSA0B_0	H22	VMA CS0#
CSA0B_1	J22	
CSA1B_0	G13	VMA CS1#
CSA1B_1	K13	
CKEA0	K20	VMA CKEO
CKEA1	J17	VMA CKET
WEA0B	G25	VMA WEO#
WEA1B	H10	VMA WE1#
PX_EN	AB16	PX_EN
RSVD#0	G14	
RSVD#3	G20	VMA MA13

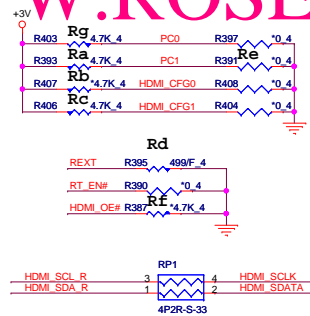
MEMORY INTERFACE

support 1Gbit VRAM (64M X 16)		
DIVIDER RESISTORS	GDDR5	DDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R





Signals		PDT	PIM	CHR
PC1	Ra	4.7K	4.7K	NC
HDMI_CFG0	Rb	NC	NC	NC
HDMI_CFG1	Rc	4.7K	NC	NC
REXT	Rd	499	4.7K	1.2K
PC1	Re	NC	NC	4.7K
HDMI_OE#	Rf	NC	NC	4.7K
PC0	Rg	4.7K	4.7K	4.7K



Vender	Part	Part Number	Part Description
PDT	PS8101	AL008101000	IC OTHER(48P) PS8101QFN48GTR(QFN)
PIM	PI3VDP411LSRZBE	ALP411LS004	IC OTHER(48P) PI3VDP411LSRZBE(TQFN)
CHR	CH7318C	AL007318002	IC OTHER(48P) CH7318C-BF-TR(QFN)

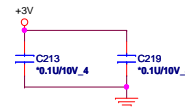
9/16 : PIM: need use ALP411LS000 or ALP411LS004 for capella

CHR : need Na R1182, add R1027 for capella

EQUALIZATION SETTING

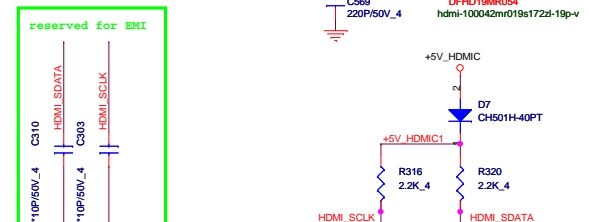
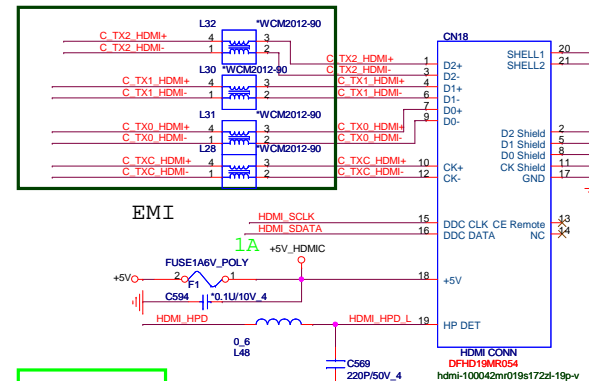
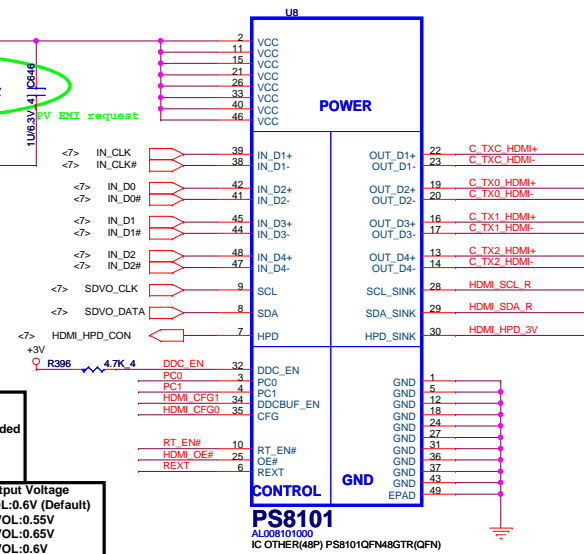
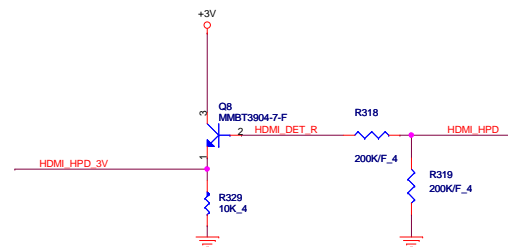
PC1:PC0=0:0 8dB
 PC1:PC0=0:1 4dB Recommended
 PC1:PC0=1:0 12dB
 PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level Input/output Voltage
 CFG1:CFG0=0:0 VIL:-0.4V VOL:-0.6V (Default)
 CFG1:CFG0=0:1 VIL:-0.36V VOL:-0.55V
 CFG1:CFG0=1:0 VIL:-0.44V VOL:-0.65V
 CFG1:CFG0=1:1 VIL:-0.36V VOL:-0.6V



8/25 SI for EMI reserve.

C TX2 HDMI+	R504	100F 4	C TX2 HDMI-
C TX1 HDMI+	R505	100F 4	C TX1 HDMI-
C TX0 HDMI+	R506	100F 4	C TX0 HDMI-
C TXC HDMI+	R507	100F 4	C TXC HDMI-

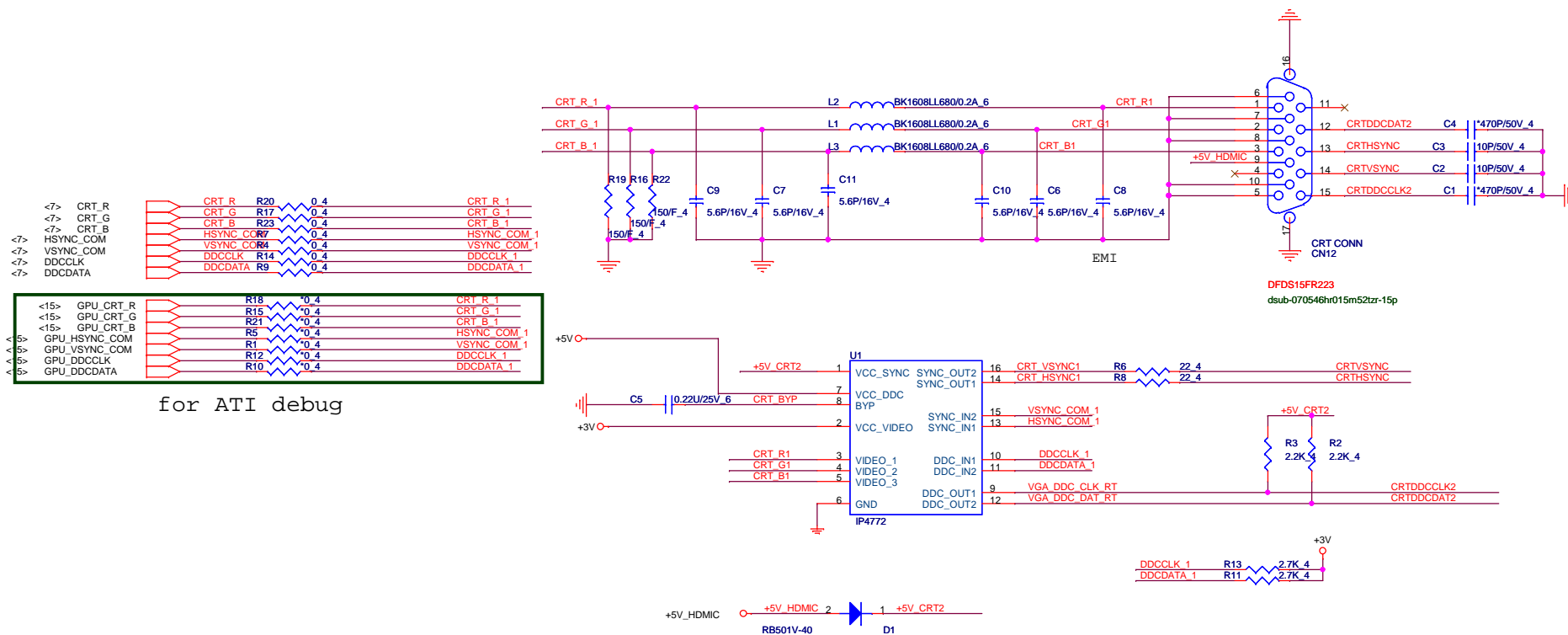


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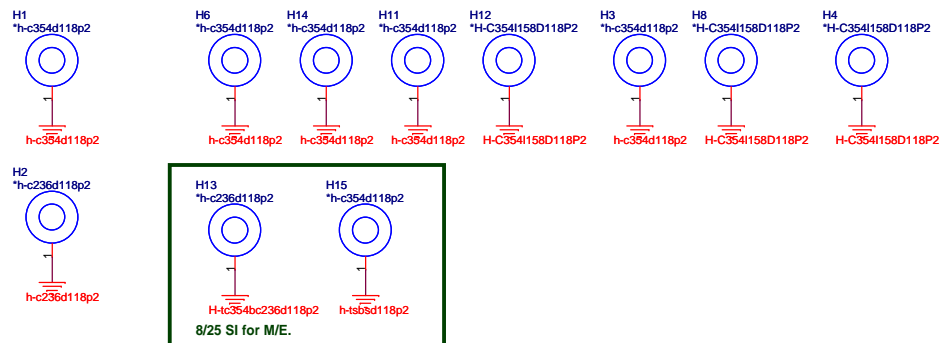
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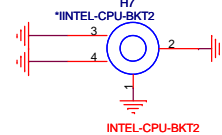
CRT PORT



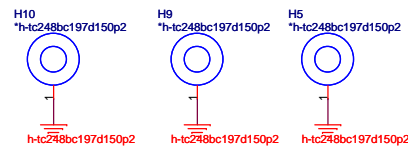
HOLE



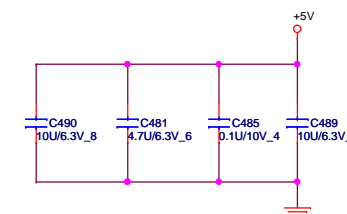
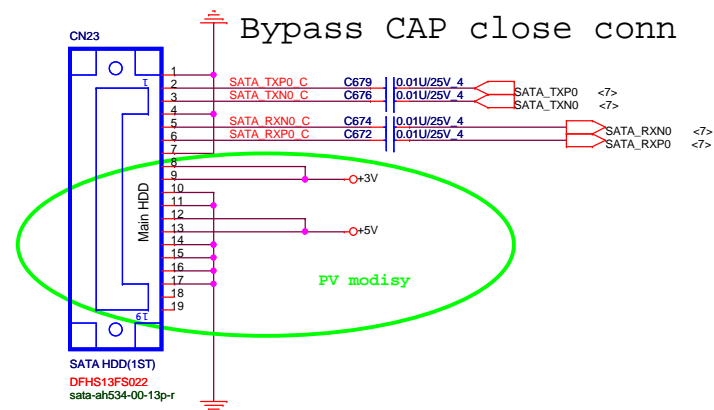
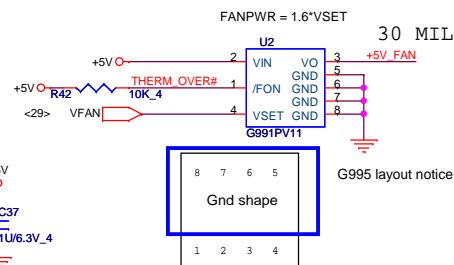
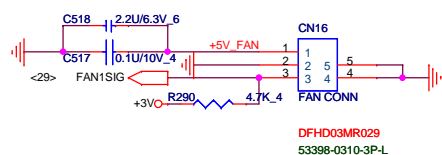
CPU



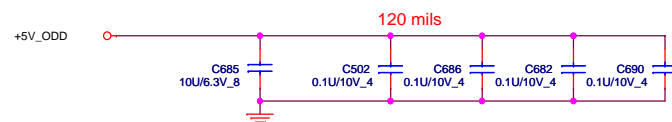
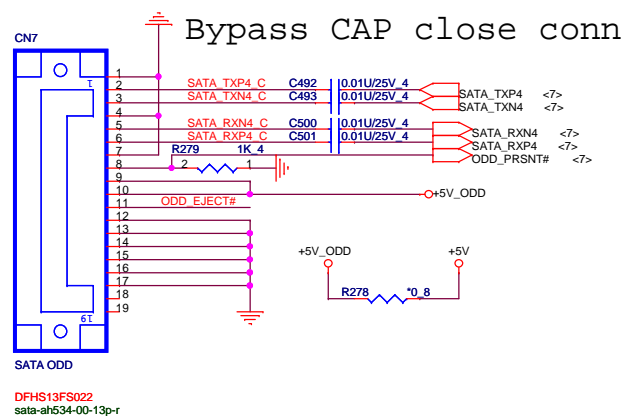
VGA



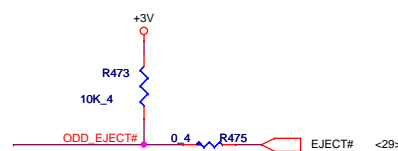
PROJECT : R12
Quanta Computer Inc.



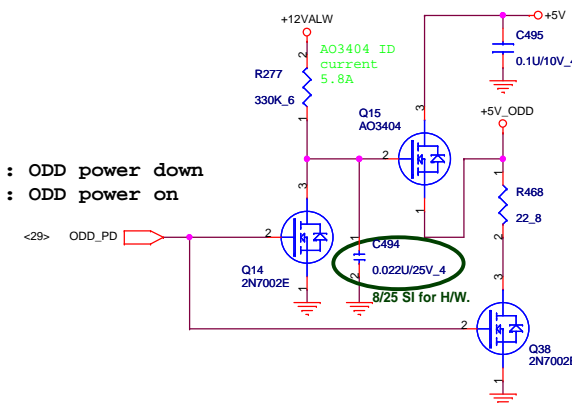
SATA ODD CONNECTOR



follow INTEL DG change eject PU to +3V.

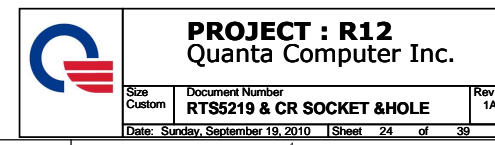


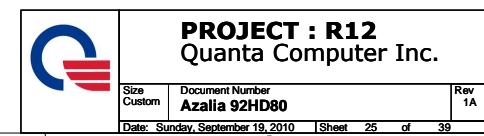
High : ODD power down
Low : ODD power on

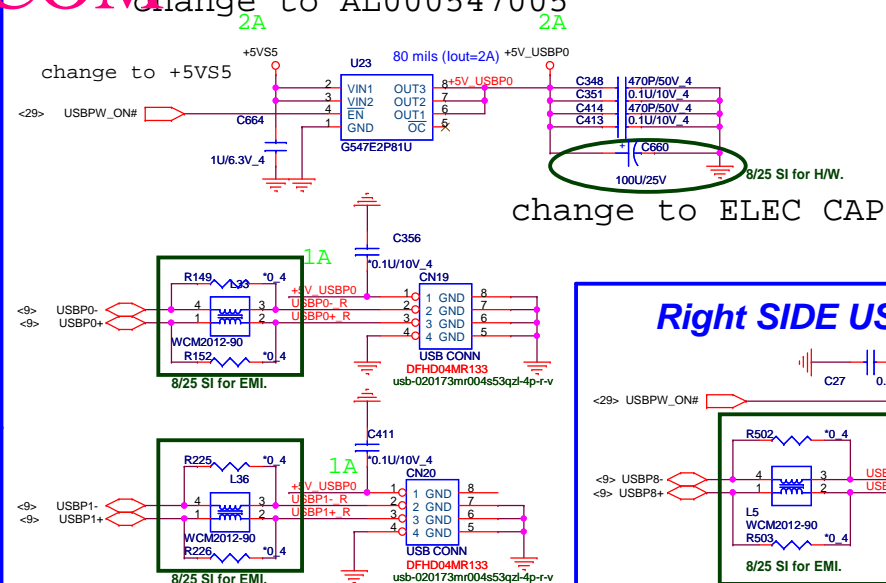
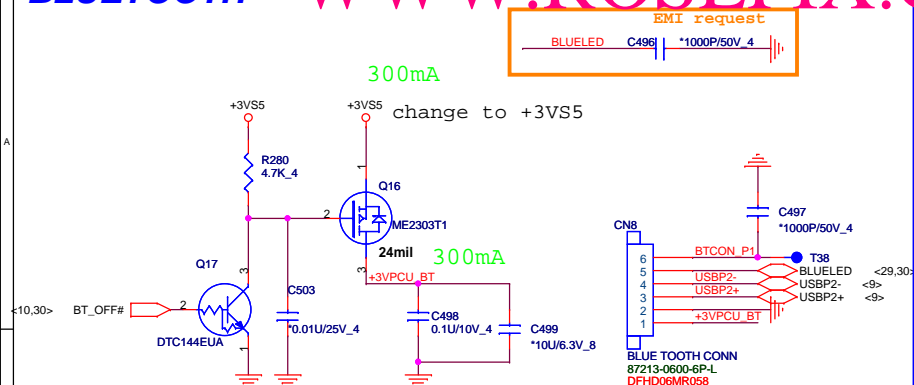


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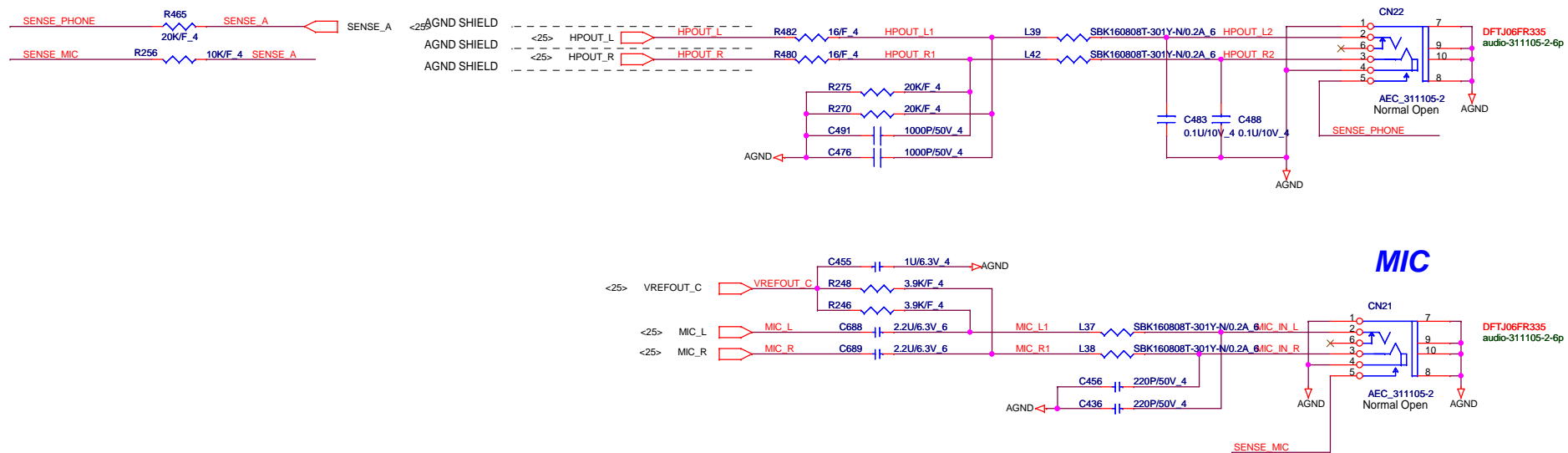
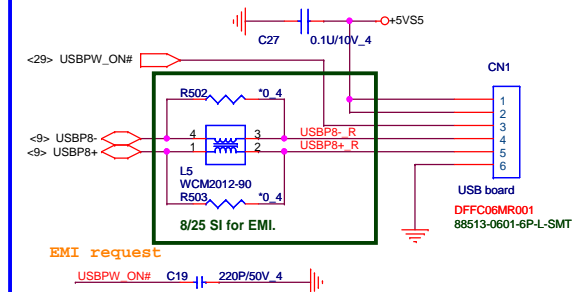
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Right SIDE USBX1



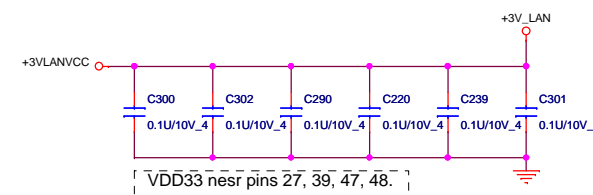
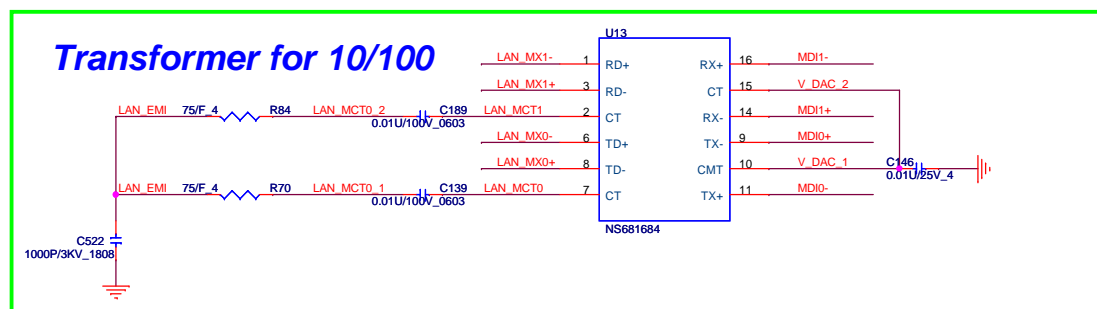
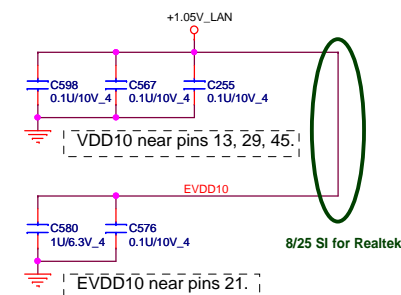
Line out

MIC



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FOR EMI

C214 1000P/50V

+3VLANVCC R85 330 4

LAN_GLED+ 12

LAN_GLED# 11

LAN_MX1- 8

LAN_MX1+ 6

LAN_MX0- 5

LAN_MX0+ 4

LAN_MX0+ 3

LAN_MX0+ 2

FOR EMI

C114 1000P/50V

+3VLANVCC R68 330 4

LAN_YLED 10

LAN_TX# 9

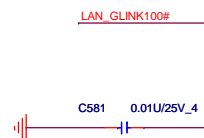
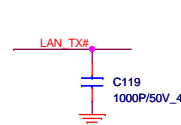
RJ45 CONN

CN17

LED_AMBE+ LED_AMBE-

RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+

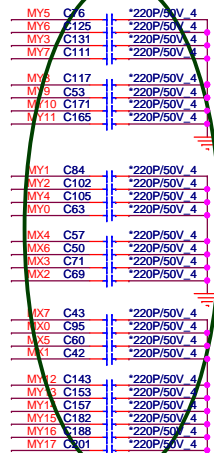
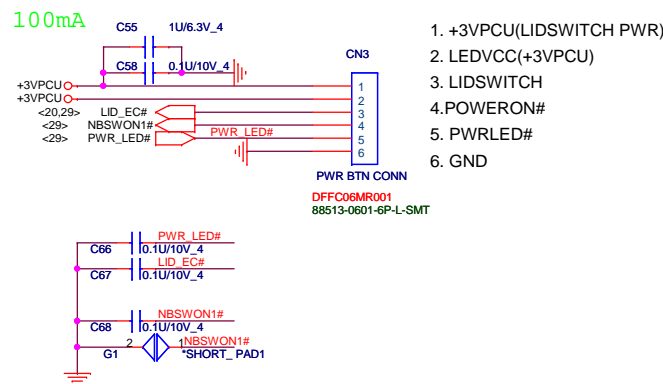
LED_WHITE LED_WHITE



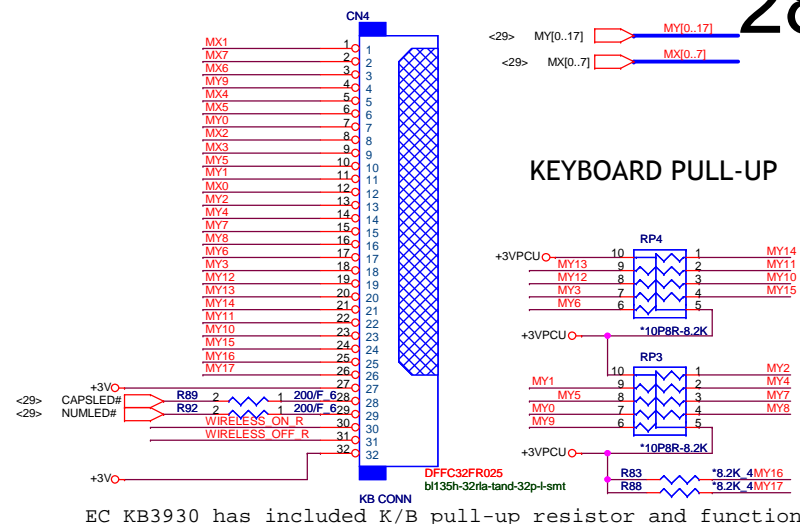
PROJECT : R12
Quanta Computer Inc.

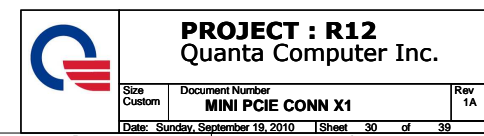
Size Custom	Document Number RTL8165EH	Rev 1
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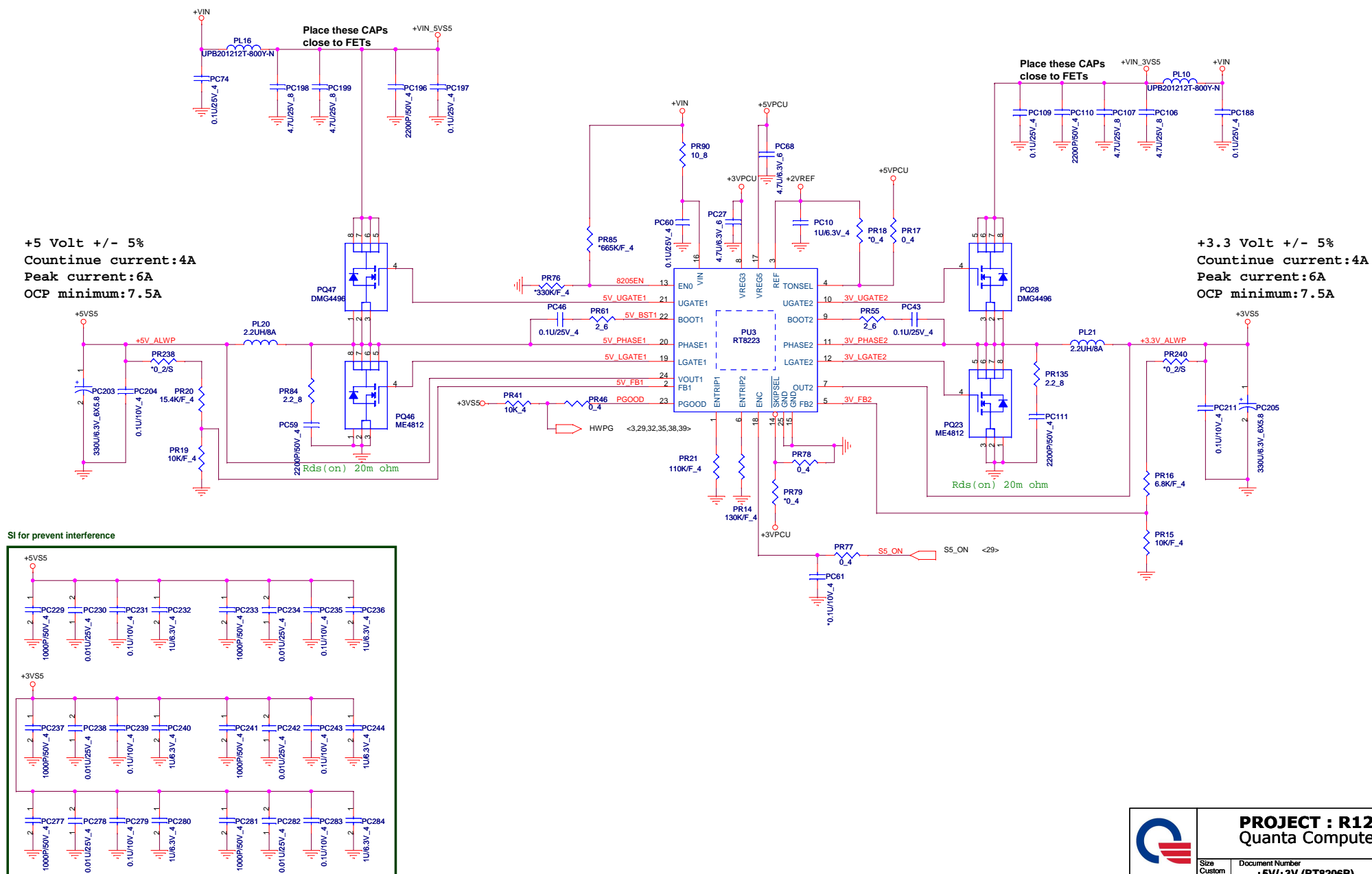
POWER BOTTOM CONNECT

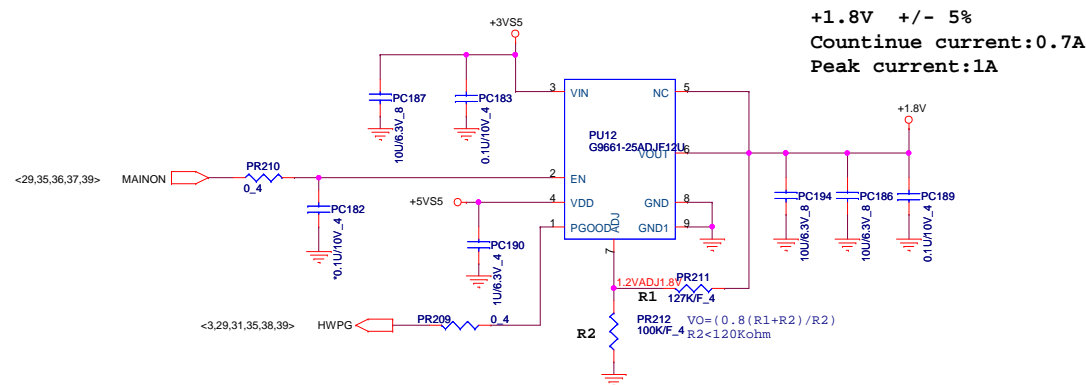
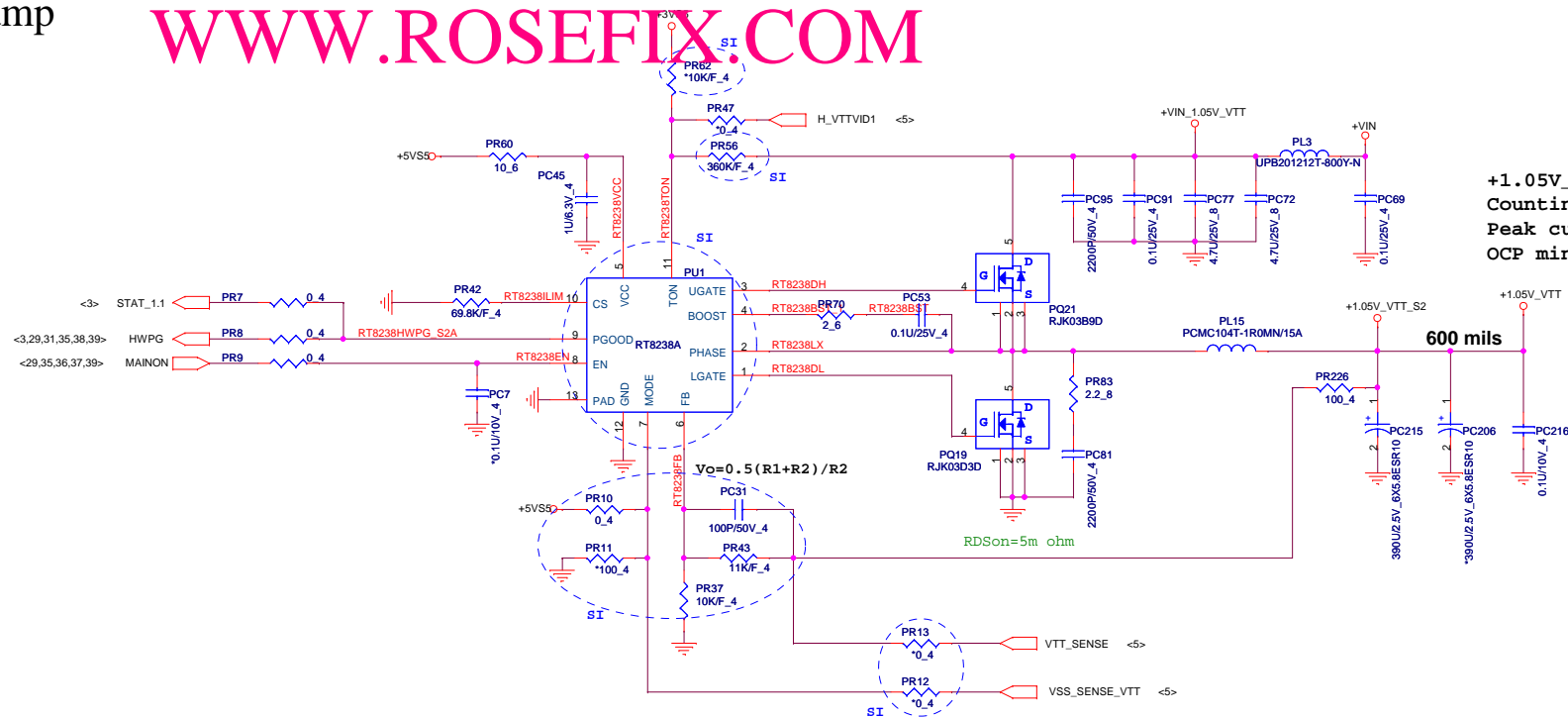


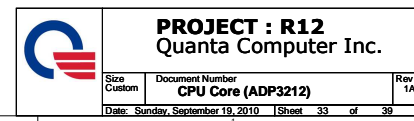
8/25 SI for H/W.

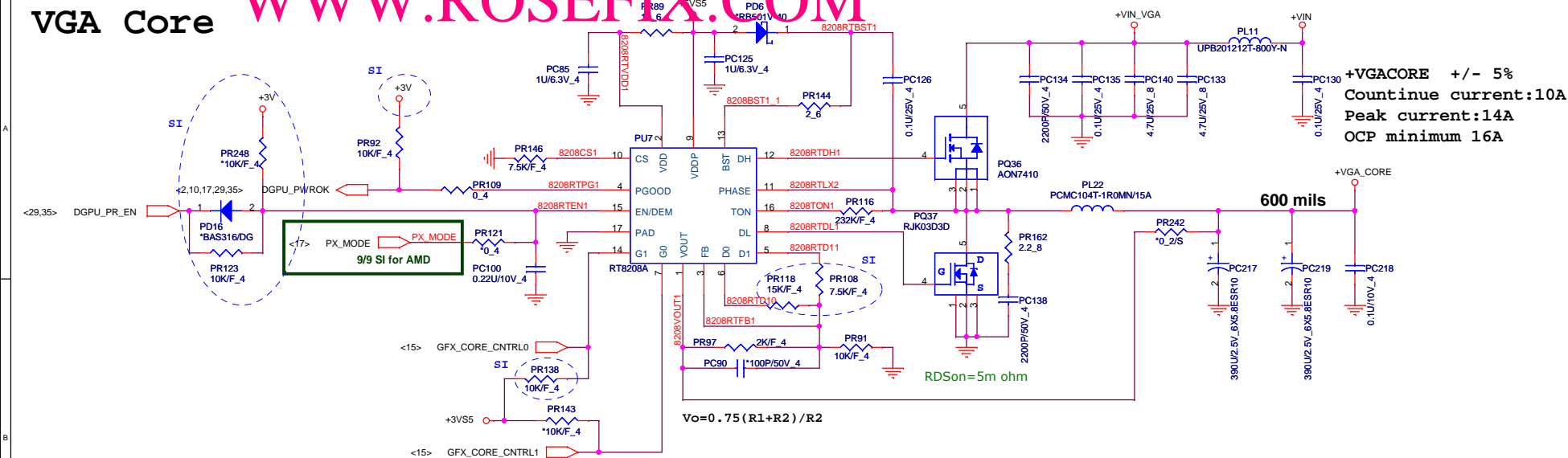




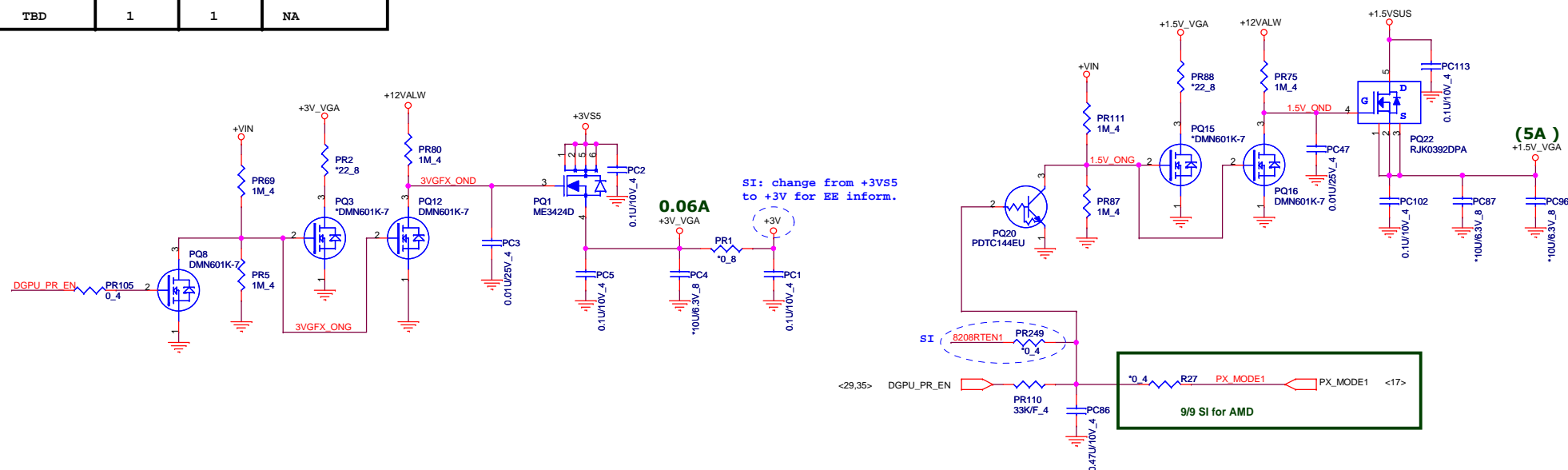








Seymour-XT	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V (Default)
TBD	1	1	NA

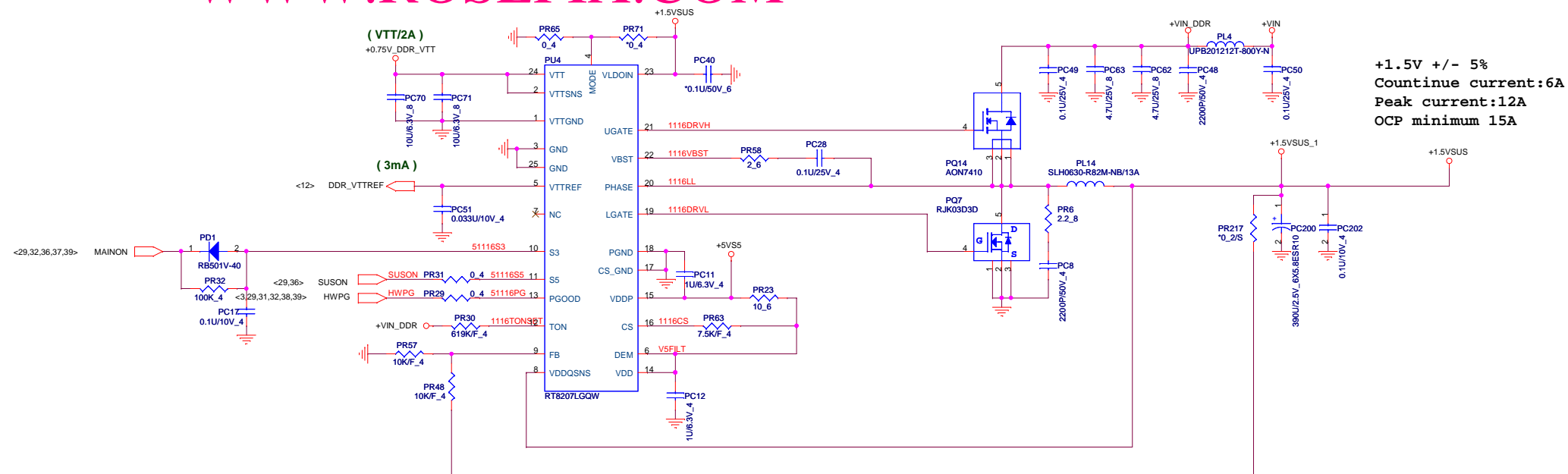


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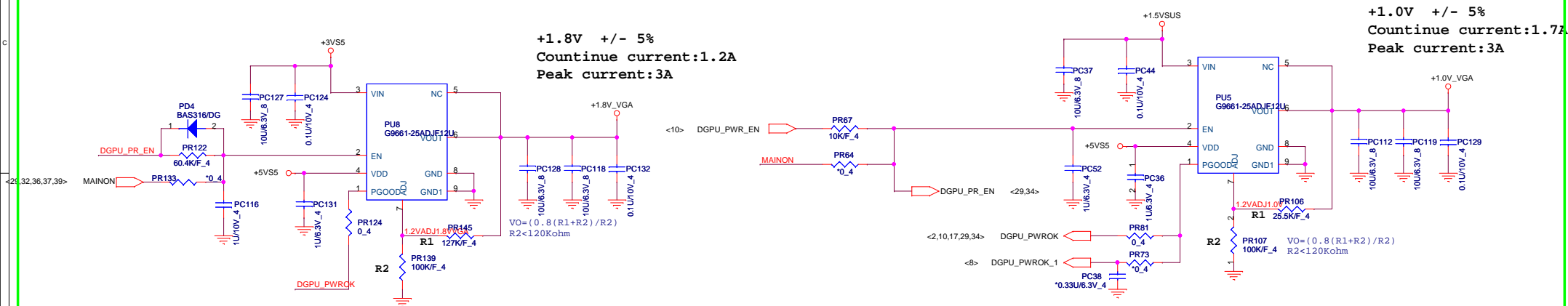
Size Custom	Document Number +VGACORE (RT8208/1.8V)
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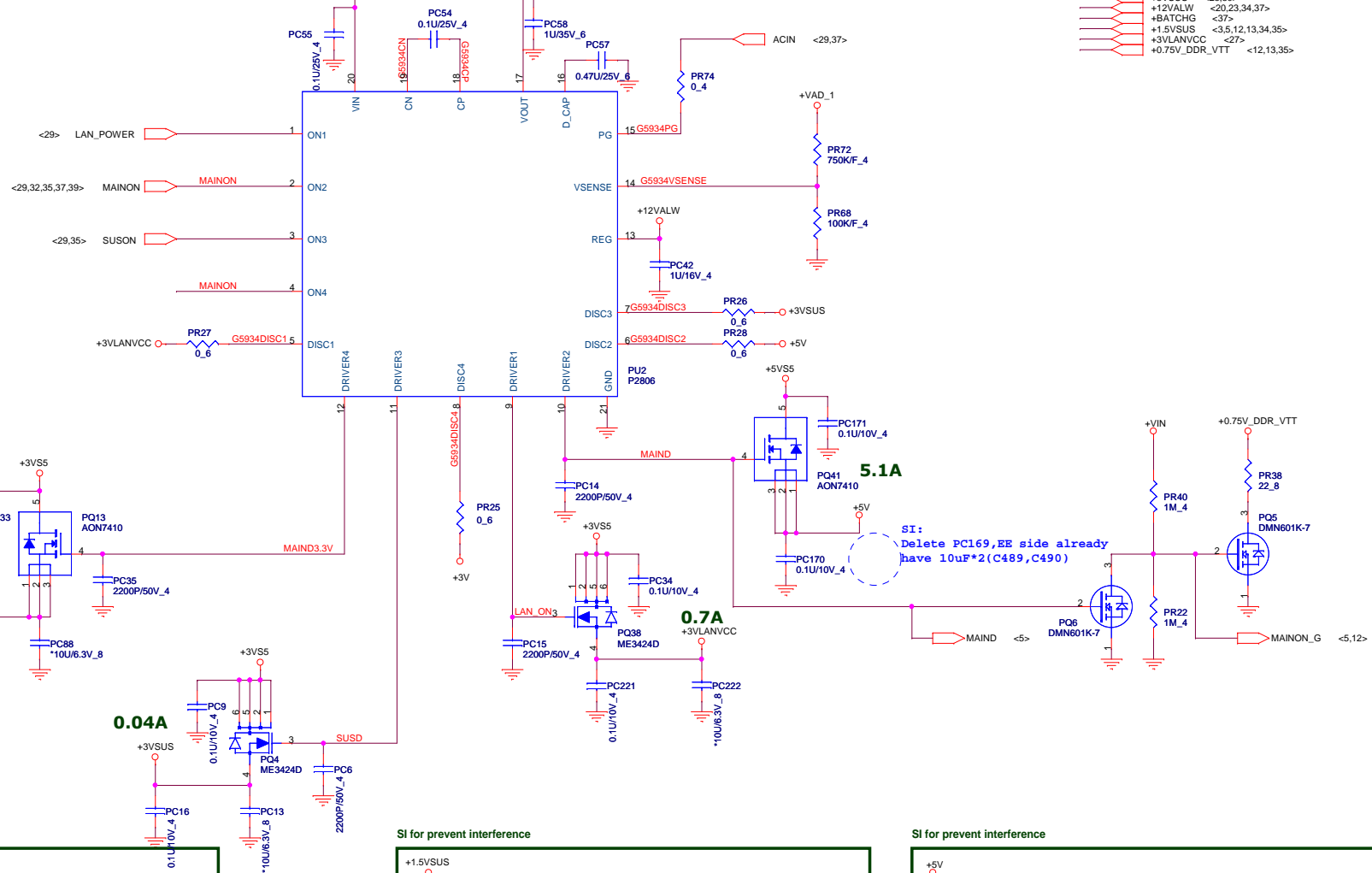
	Re
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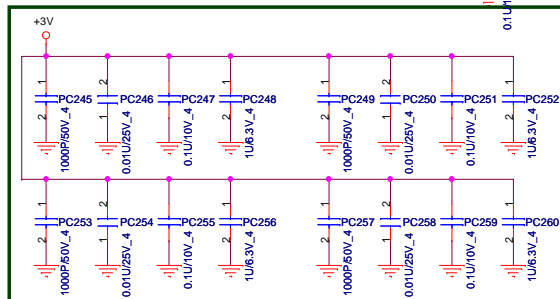


SG & Discrete Only

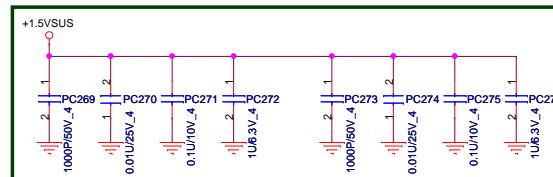




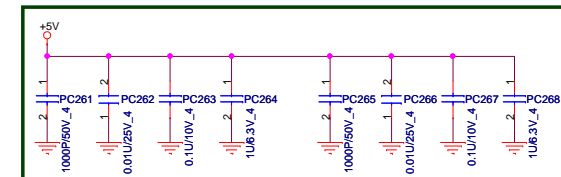
SI for prevent interference



SI for prevent interference



SI for prevent interference



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