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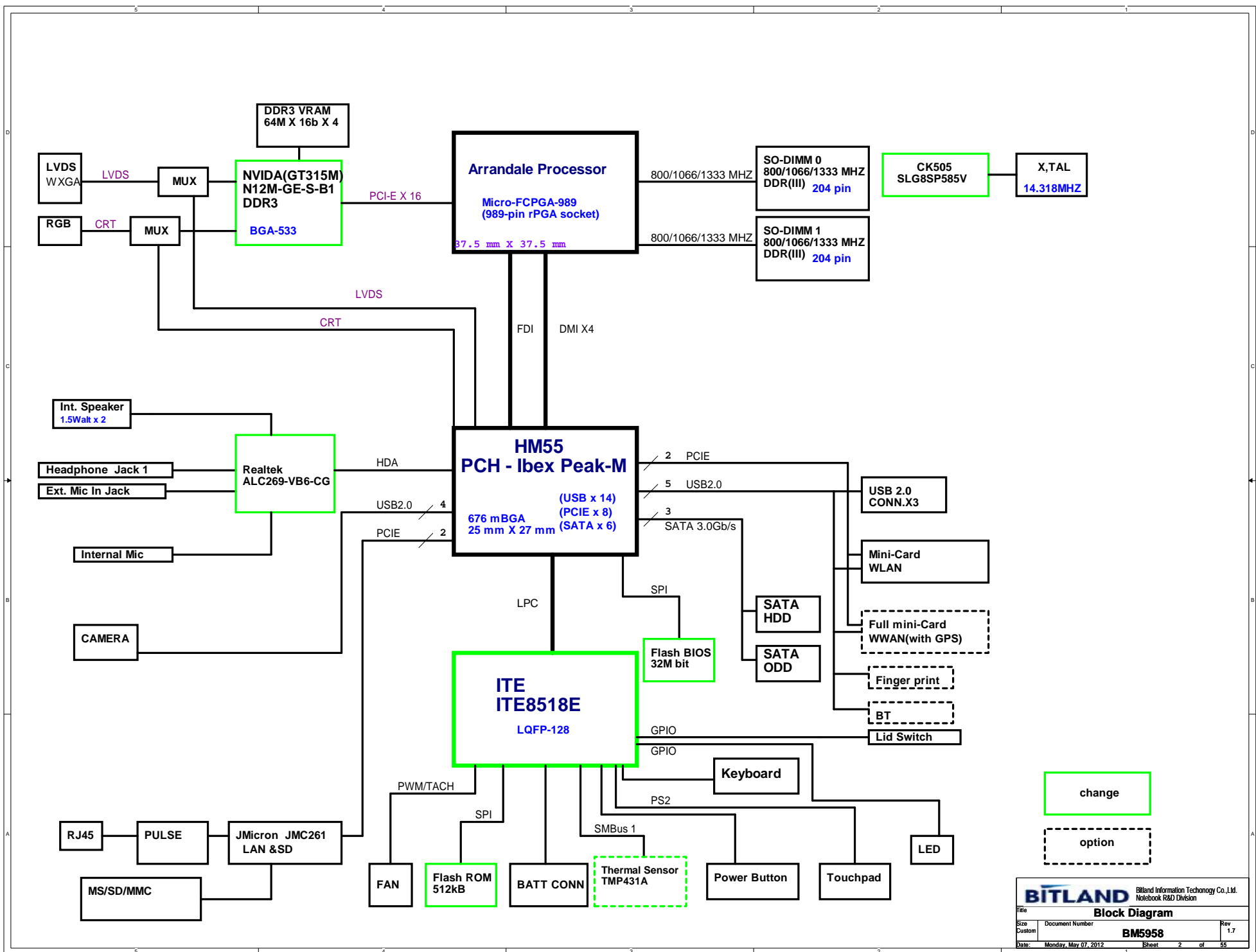
BM5958 M/B Schematics Document

Intel Arrandale Processor with Ibexpeak(HM55) + DDRIII

2012-5-7

REV:1.71

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Block Diagram		
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1

Voltage Rails

Power Plane	Description	S1	S3	S5
DC_IN	Adapter power supply (19V)	N/A	N/A	N/A
DCBATOUT	AC or battery power rail for power circuit.	N/A	N/A	N/A
+V_CORE	Core voltage for CPU	ON	OFF	OFF
+0_75V	0.75VRUN LDO power rail for DDR terminator	ON	OFF	OFF
+1.05VRUN	1.05V switched power rail	ON	OFF	OFF
+5VRUN	5V switched power rail	ON	OFF	OFF
+1_5VSUS	1.5V power rail for DDR	ON	ON	OFF
+1.5VRUN	1.5V switched power rail	ON	OFF	OFF
+1.8VRUN	1.8V power rail for system	ON	OFF	OFF
+1.5V_CPU	1.5V switched power rail	ON	OFF	OFF
+1.1VTT	VTI switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VSUS	3.3V power rail for SB	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF
+3VRUN	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VSUS	5V switched power rail	ON	ON	OFF
PEX_VDD	PEX LDO power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON
NV_VDD	Core voltage for GPU	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADT7421	1001 100X b
MEDIA CONSOLE	1010 000X b	NB9M THERMAL SENSOR	

EC SM Bus2 address

HM55 SM Bus address

Device	Address
Clock Generator (SLG8SP587V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+SUS	+RUN	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

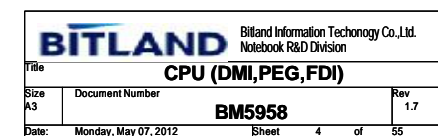
Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

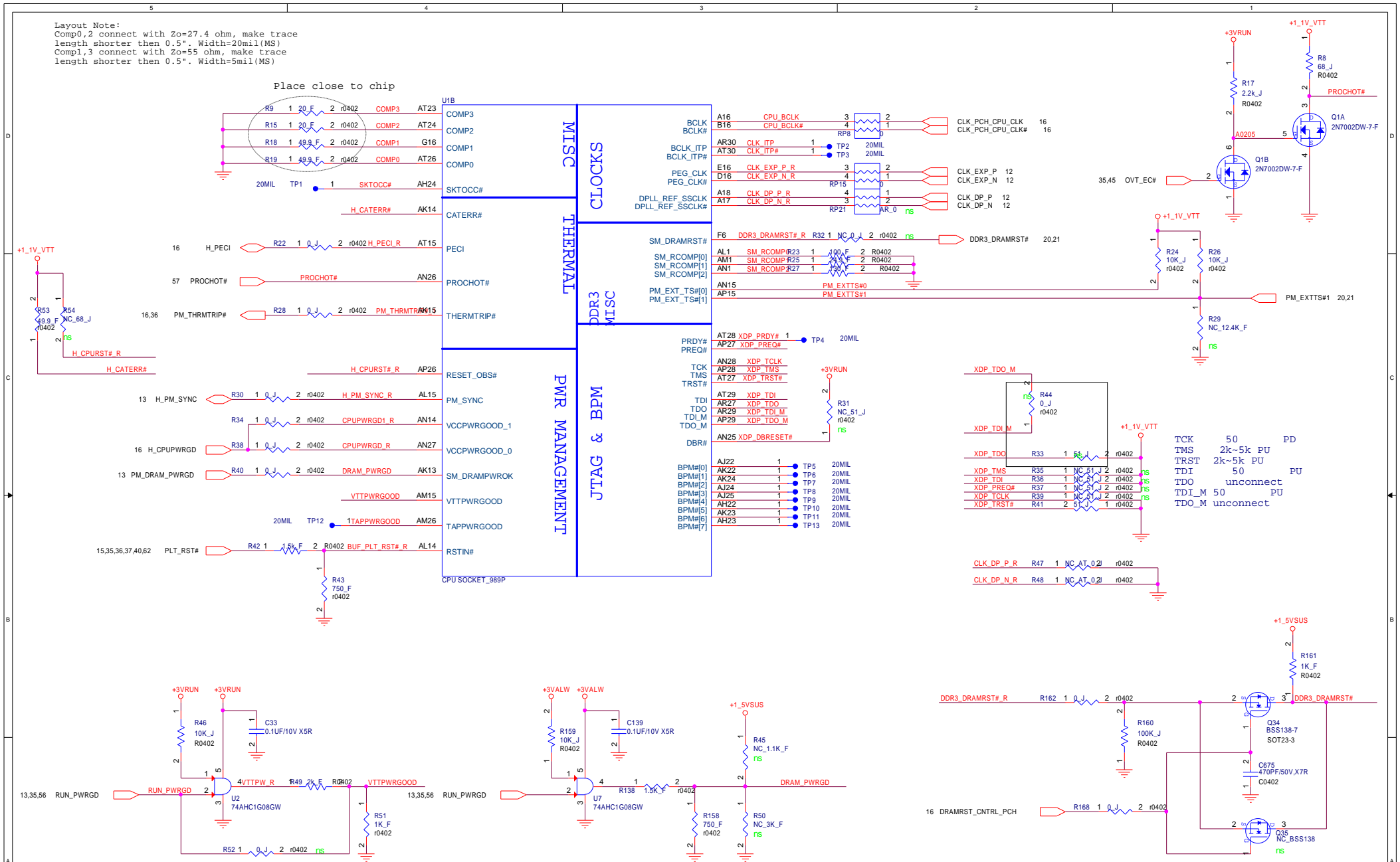
BOARD ID Table

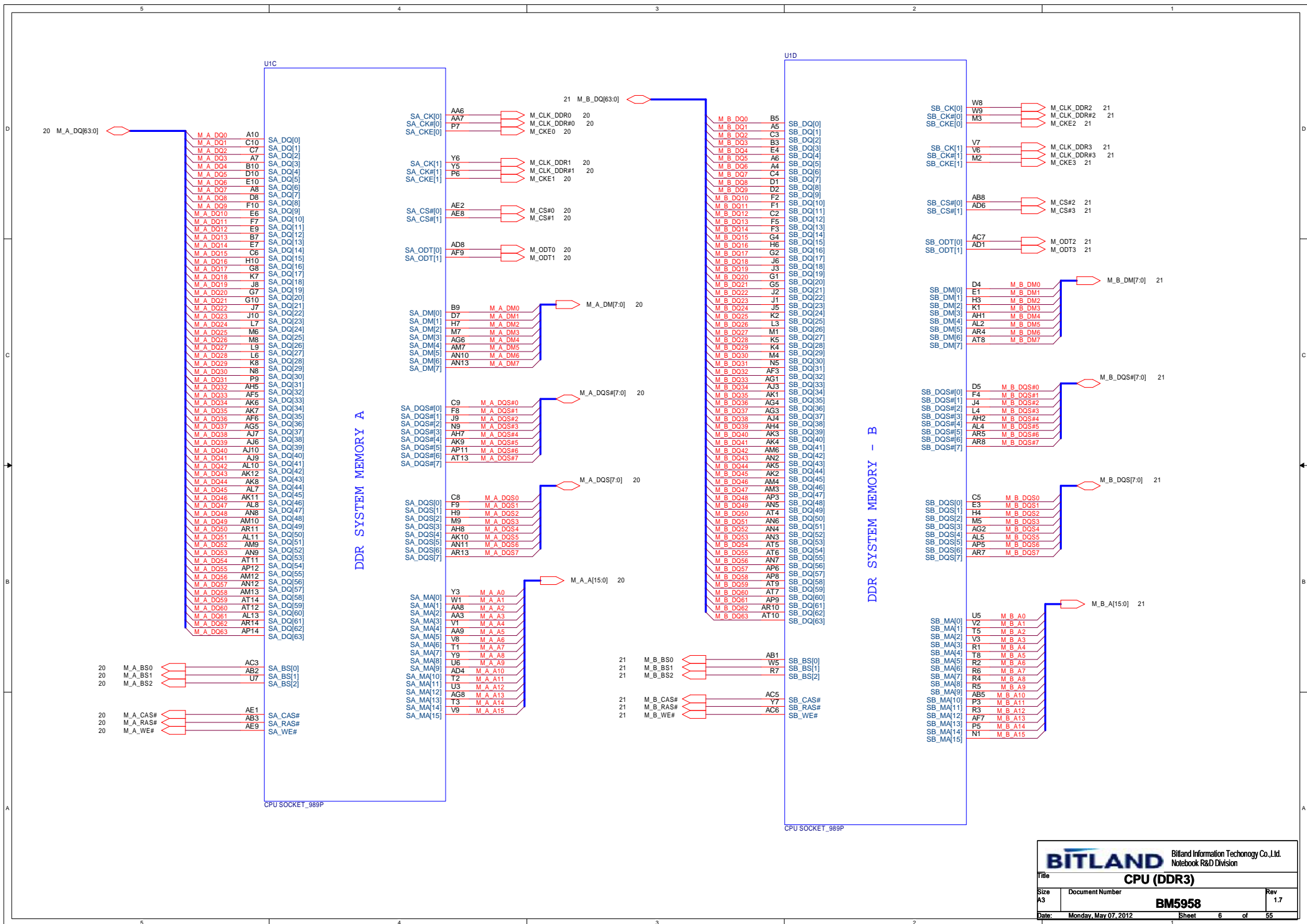
Board ID	PCB Revision
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1	1.0
2	1.1
3	1.2
4	1.3
5	
6	
7	

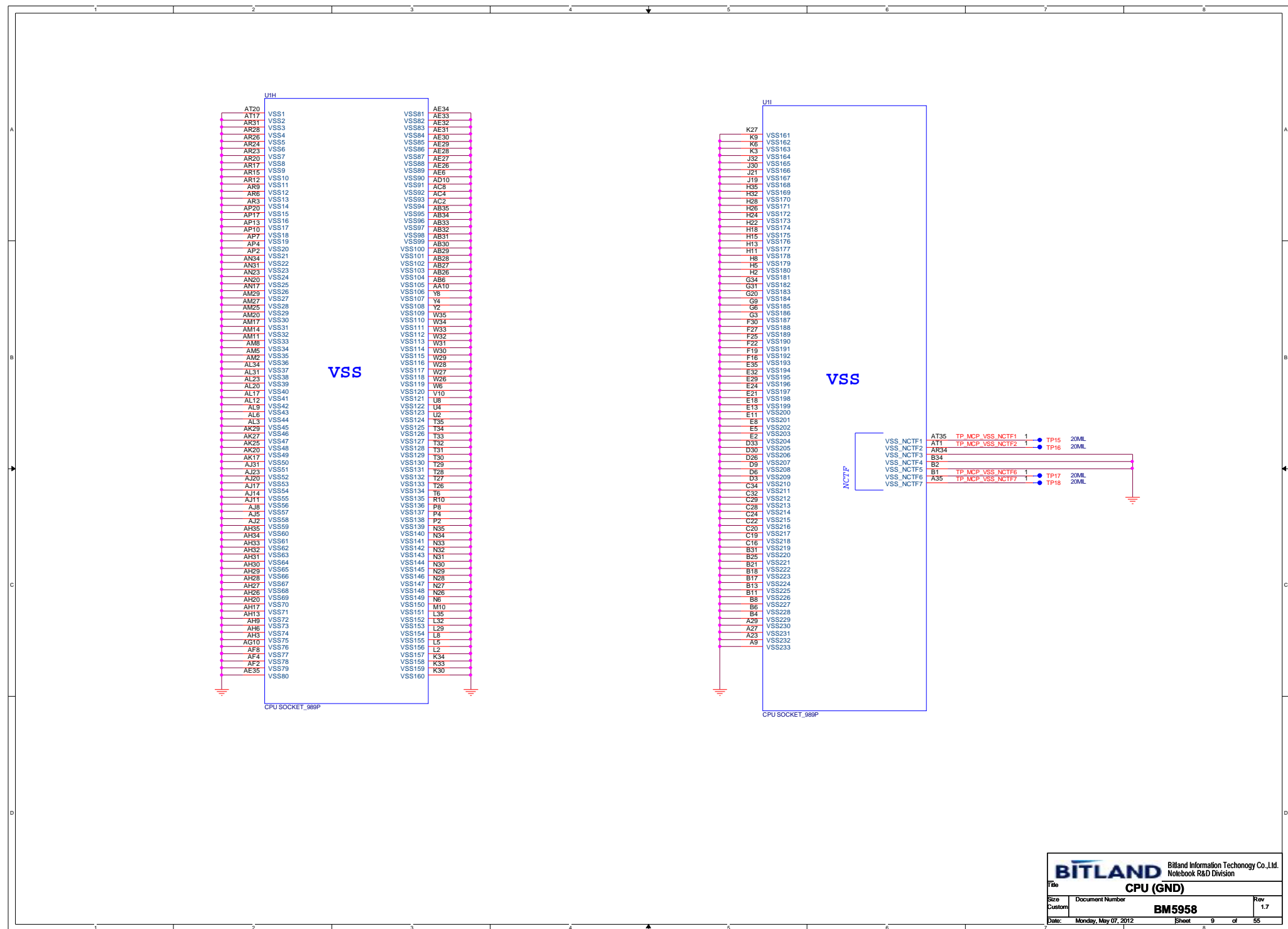
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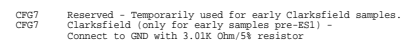
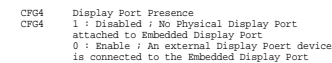
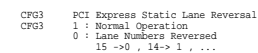
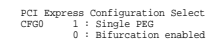


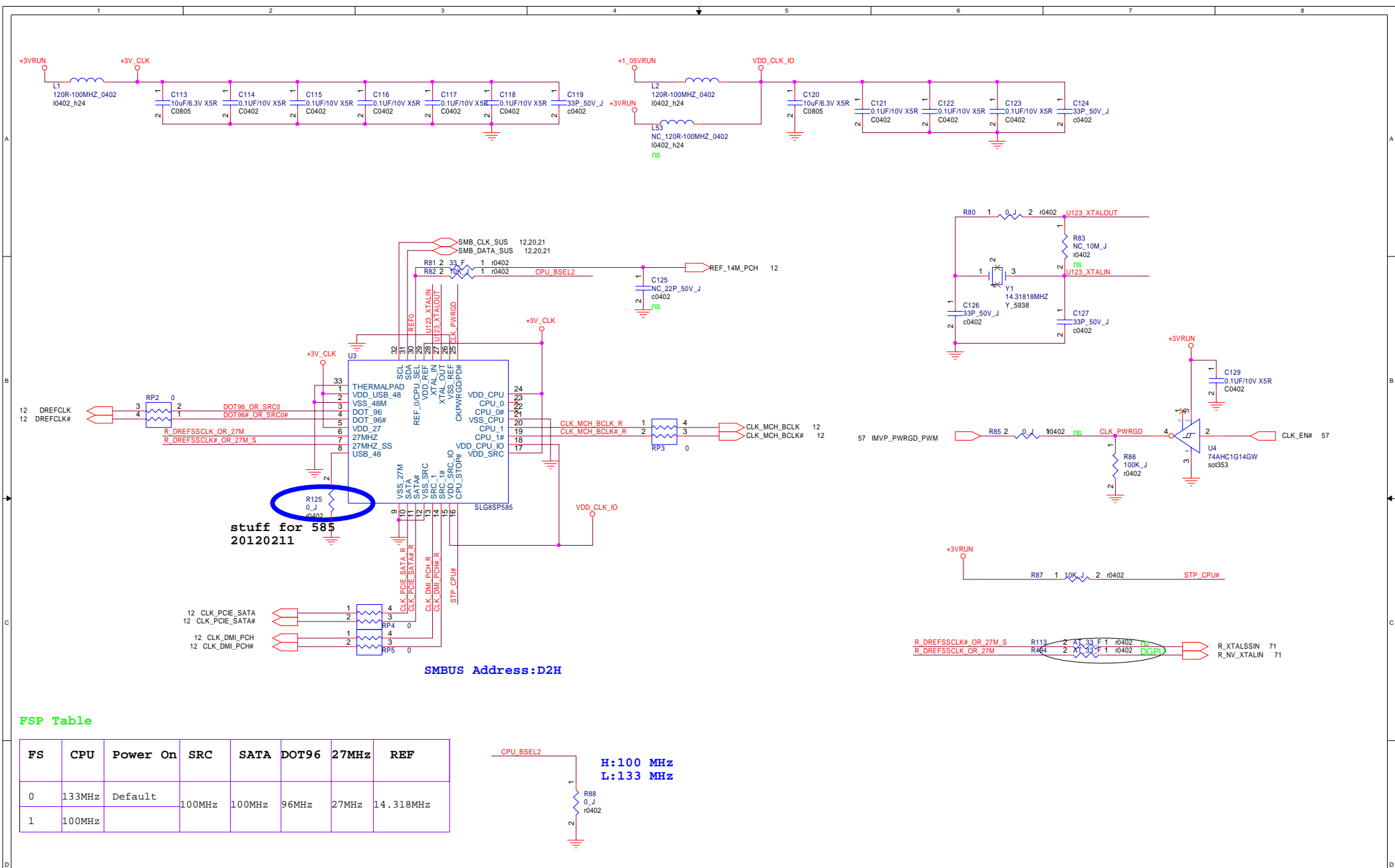
Layout Note:
Comp0,2 connect with $Z_0=27.4$ ohm, make trace
length shorter then 0.5". Width=20mil(MS)
Comp1,3 connect with $Z_0=55$ ohm, make trace
length shorter then 0.5". Width=5mil(MS)

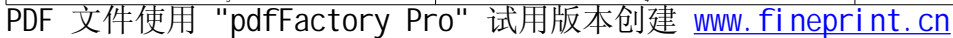




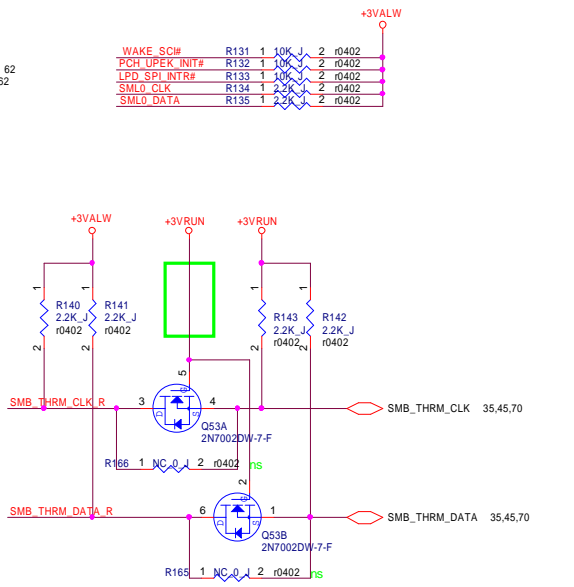






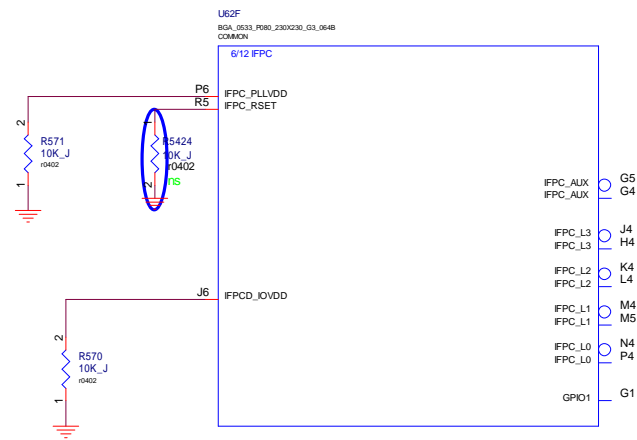
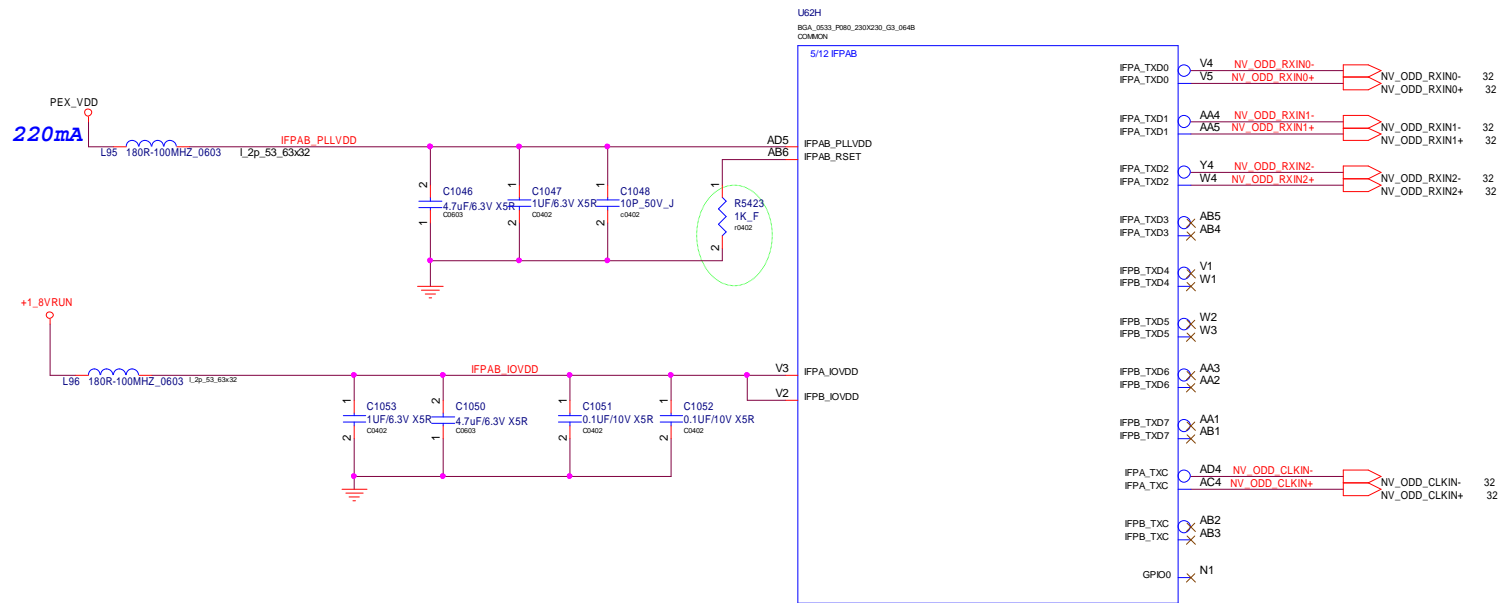


Port	Function
Port1	LAN
Port2	Express Card
Port3	WLAN
Port4	Un-used
Port5	Un-used
Port6	Un-used
Port7	Un-used
Port8	Un-used

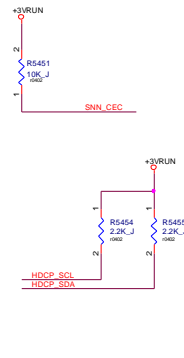




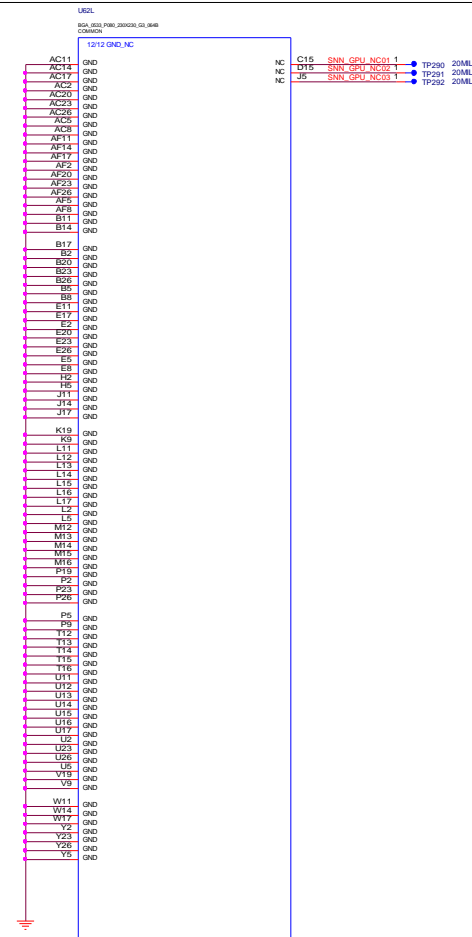


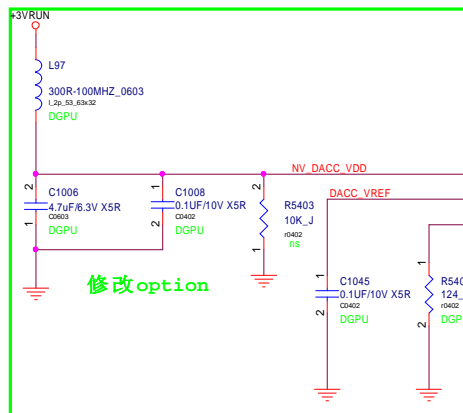


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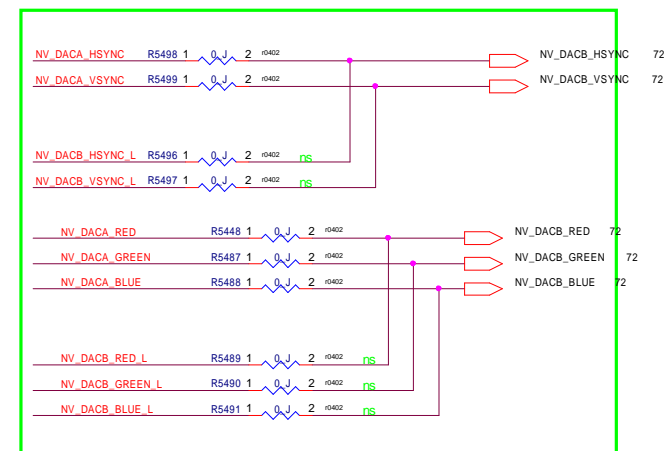
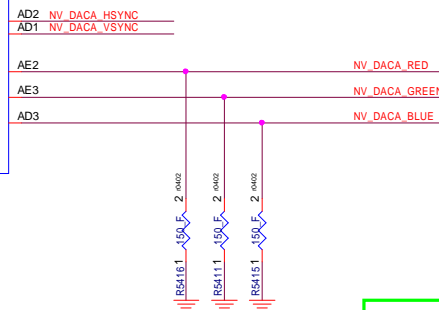
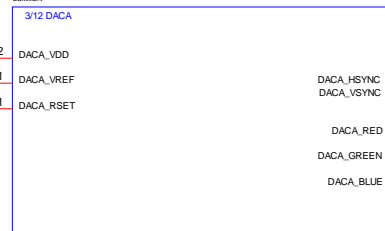
Node	Build_30sec_RxT1_30D	Build_30sec_RxT2_30D	Dropping technique value for other drop plans
Element Product line	40,2% (5 to 60)	40	-100 %
Multi Level	40,2% (5 to 60)	40,2% (5 to 60)	See build-in-out string



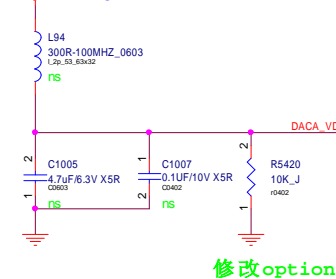


DAC A

U62D
BGA_0533_P080_230X230_Q3_0648
COMMON

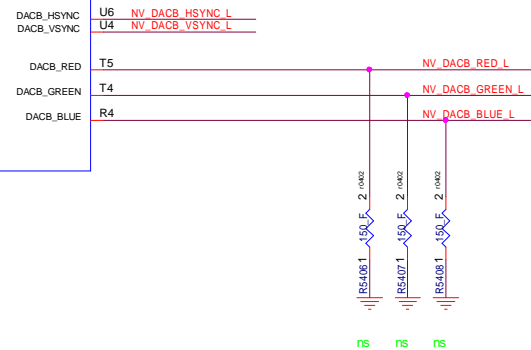


+3V RUN 120mA

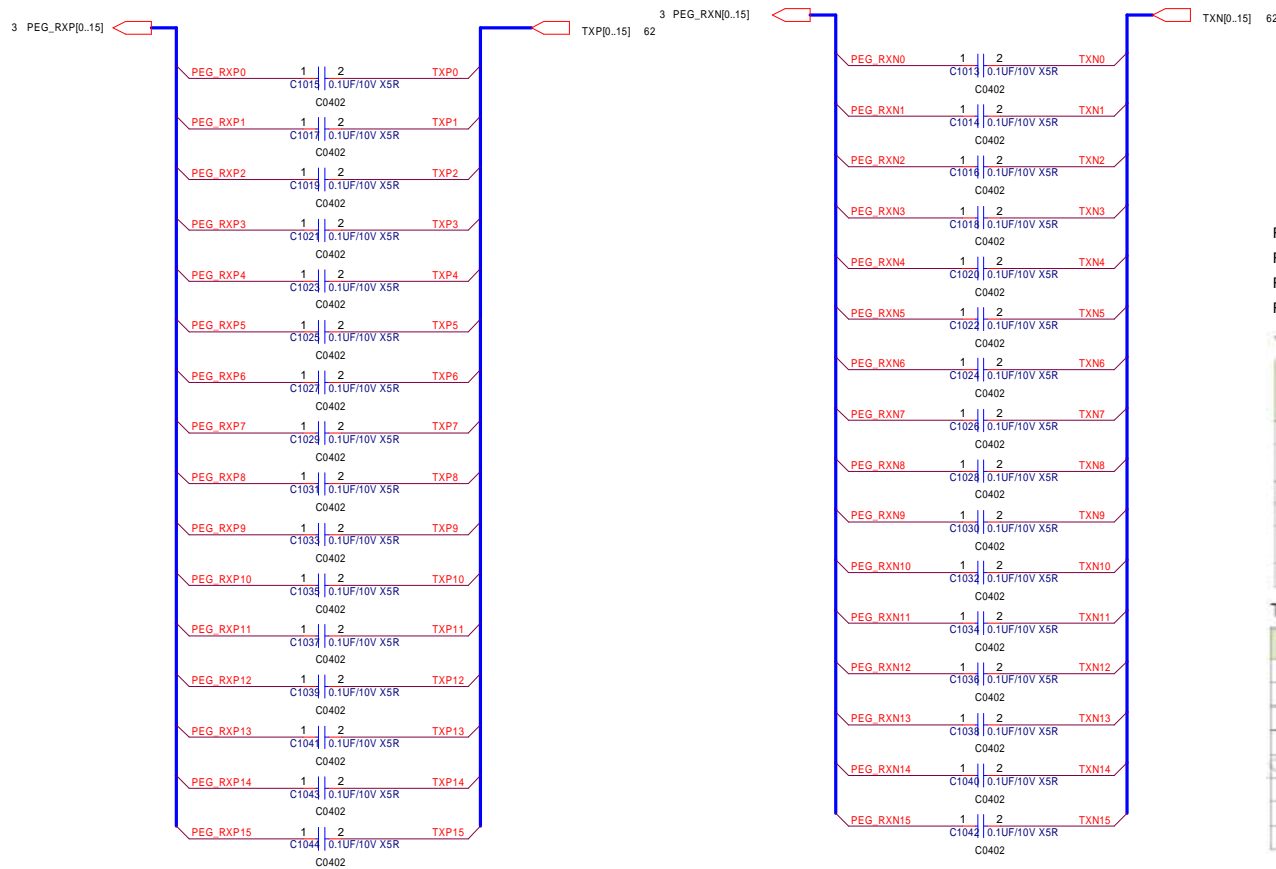


DAC B

U62C
BGA_0533_P080_230X230_Q3_0648
COMMON



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STRAP0: USER[3:0]
 STRAP1: 3GIO_PADCFG_LUT_ADR[3:0]
 STRAP2: PCI_DEVID[3:0]

ROM_SCLK: PCIDEVID_EXT.SUB_VENDOR,SLOT_CLK,PEX_PLL_EN
 ROM_SI: RAMCFG[3:0]
 ROM_SO: XCLK_277,TVMODE[2:0] ** G98
 ROM_SO: XCLK_417,FB_0_BAR_SIZE,SMB_ALT_ADDR,VGA_DEVICE **GT218

Table 15.2 Multi-Level Mode Strapping

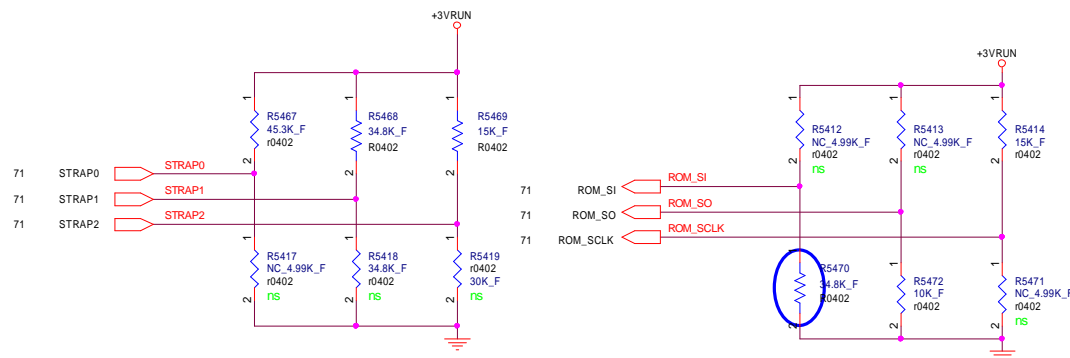
Physical Strapping Pin	Power Rail	Logical Strapping Bit 1	Logical Strapping Bit 2	Logical Strapping Bit 3	Logical Strapping Bit 0
ROM_SO	VDD03	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	VDD03	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN, TE BM
ROM_SI	VDD03	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
STRAP0	VDD03	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	VDD03	3GIO_PADC_CFG_ADR[3]	3GIO_PADC_CFG_ADR[2]	3GIO_PADC_CFG_ADR[1]	3GIO_PADC_CFG_ADR[0]
STRAP2	VDD03	USER[3]	USER[2]	USER[1]	USER[0]

Table 15.3 Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD	Pull-down to GND
5k	1000	0000
10k	1001	0001
15k	1010	0010
20k	1011	0011
25k	1100	0100
30k	1101	0101
35k	1110	0110
45k	1111	0111

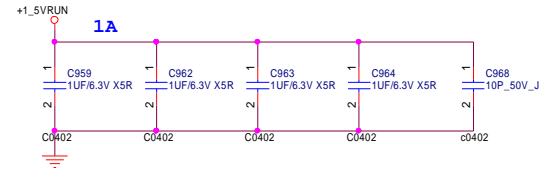
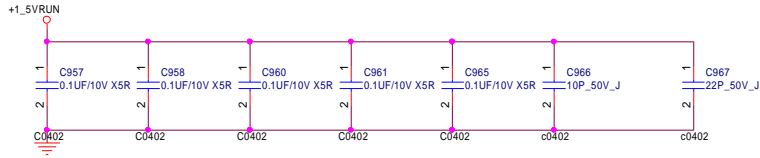
Configuration	FB Width	Vendor	Strap	FWVDV/FWVDD2	Manufacturer Part Number	Speed (MHz)	Memory Base Code Alert
128Mx16 DDR3	64 bit	Hynix	Dx6	1.5 V, 1.5 V	H8TQG638FR-12C	800	Use material datasheet after date code "1008."
Single Rank (500 Mhz)	64 bit	Samsung	Dx7	1.5 V, 1.5 V	K4W2G1644C-PC12	800	Use material datasheet after date code "1025"

samsung: R5470 0x7 45k pull down
 hynix: R5470 0x6 35k pull down

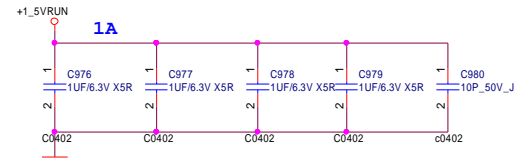
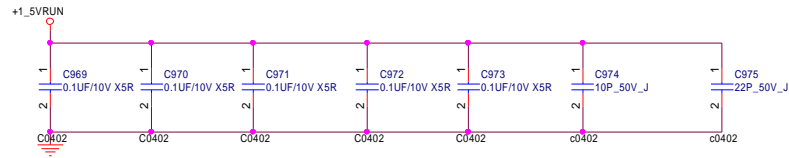


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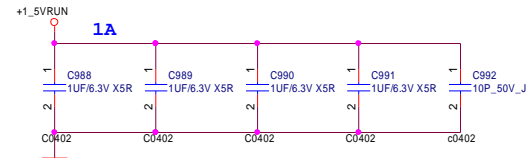
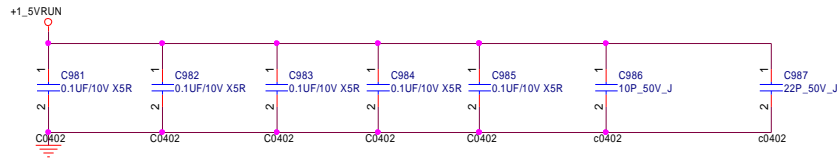
Place around the VRAM U63



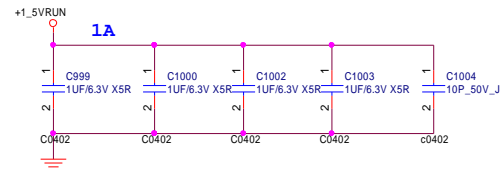
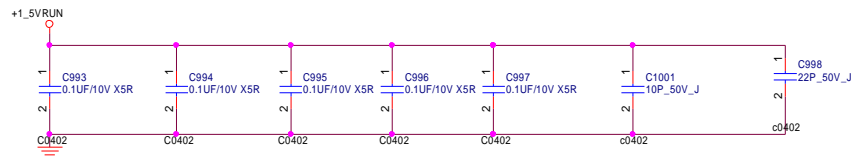
Place around the VRAM U64



Place around the VRAM U65



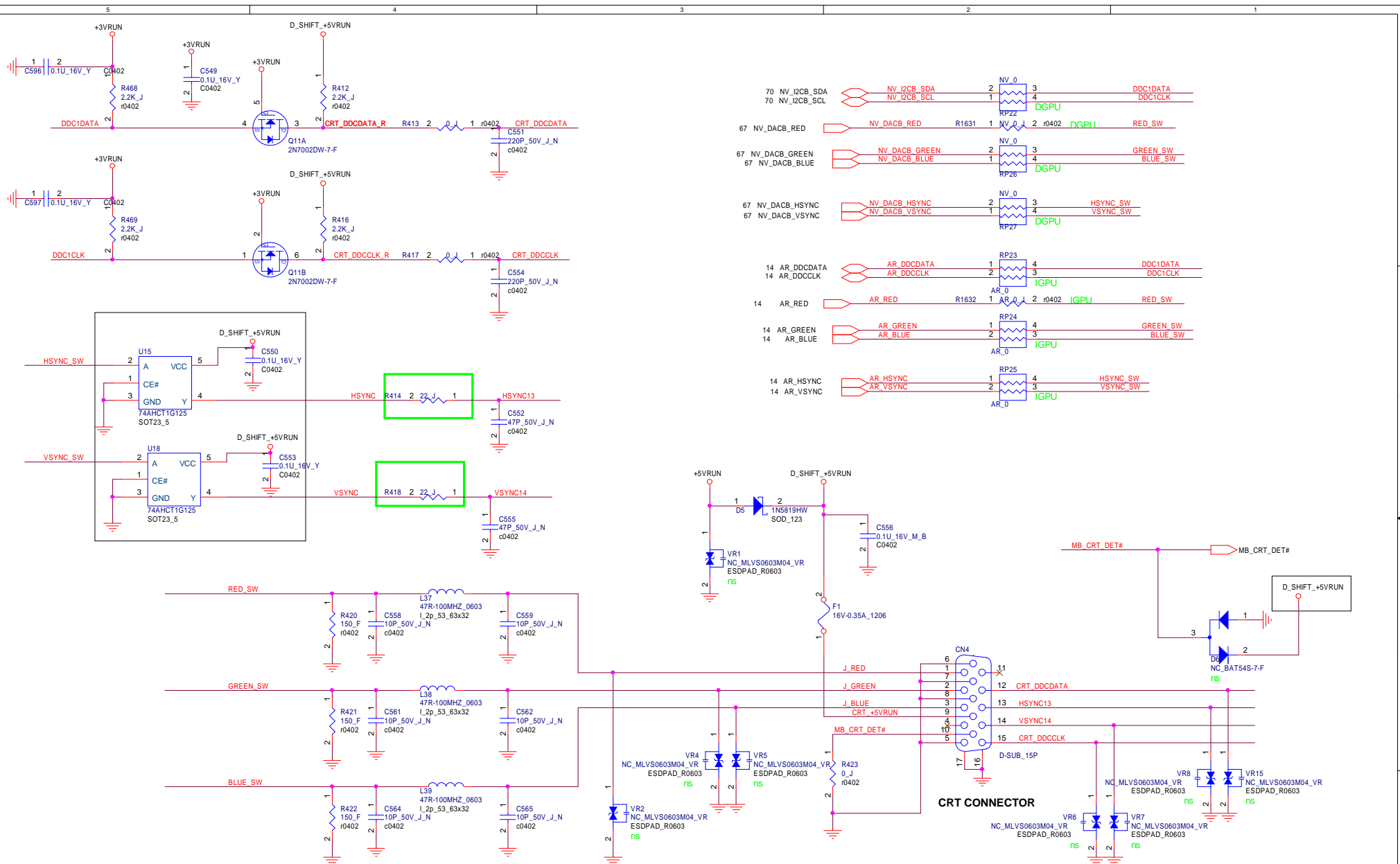
Place around the VRAM U66

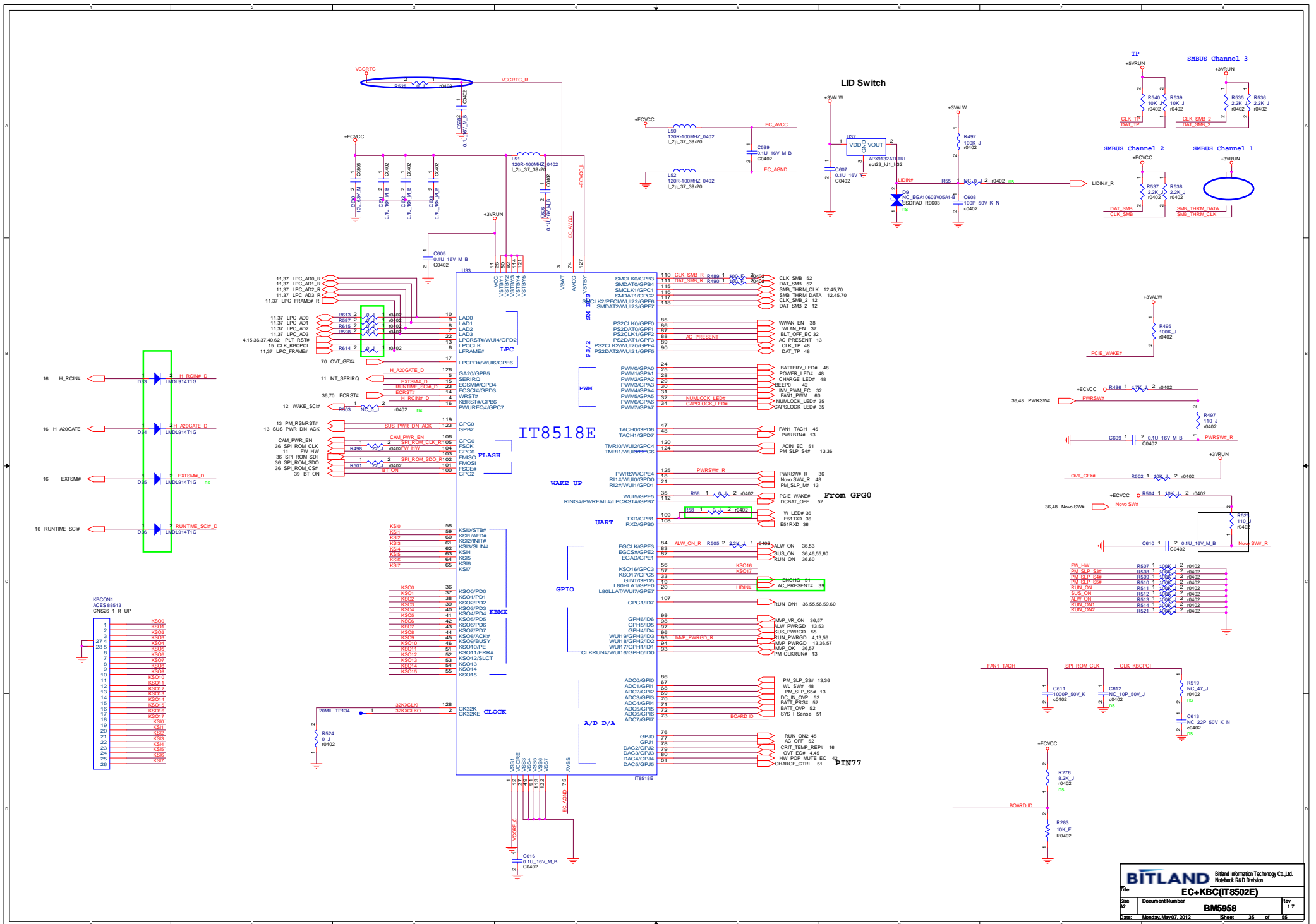


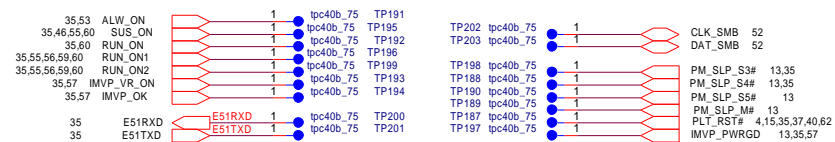
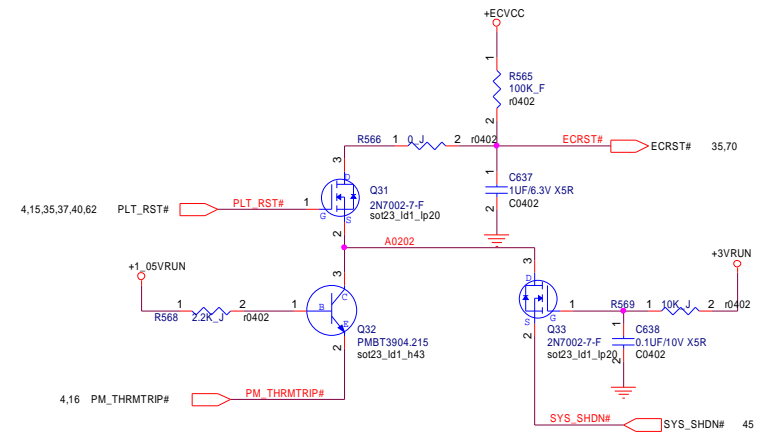
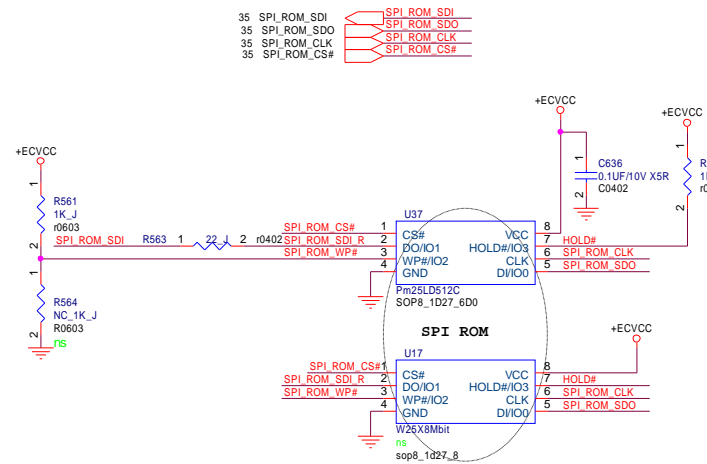
PLACE 0.1UF CAPS UNDER THE MEMORY DEVICE.

PLACE 1UF CAPACITORS CLOSE TO THE MEMORY DEVICE.

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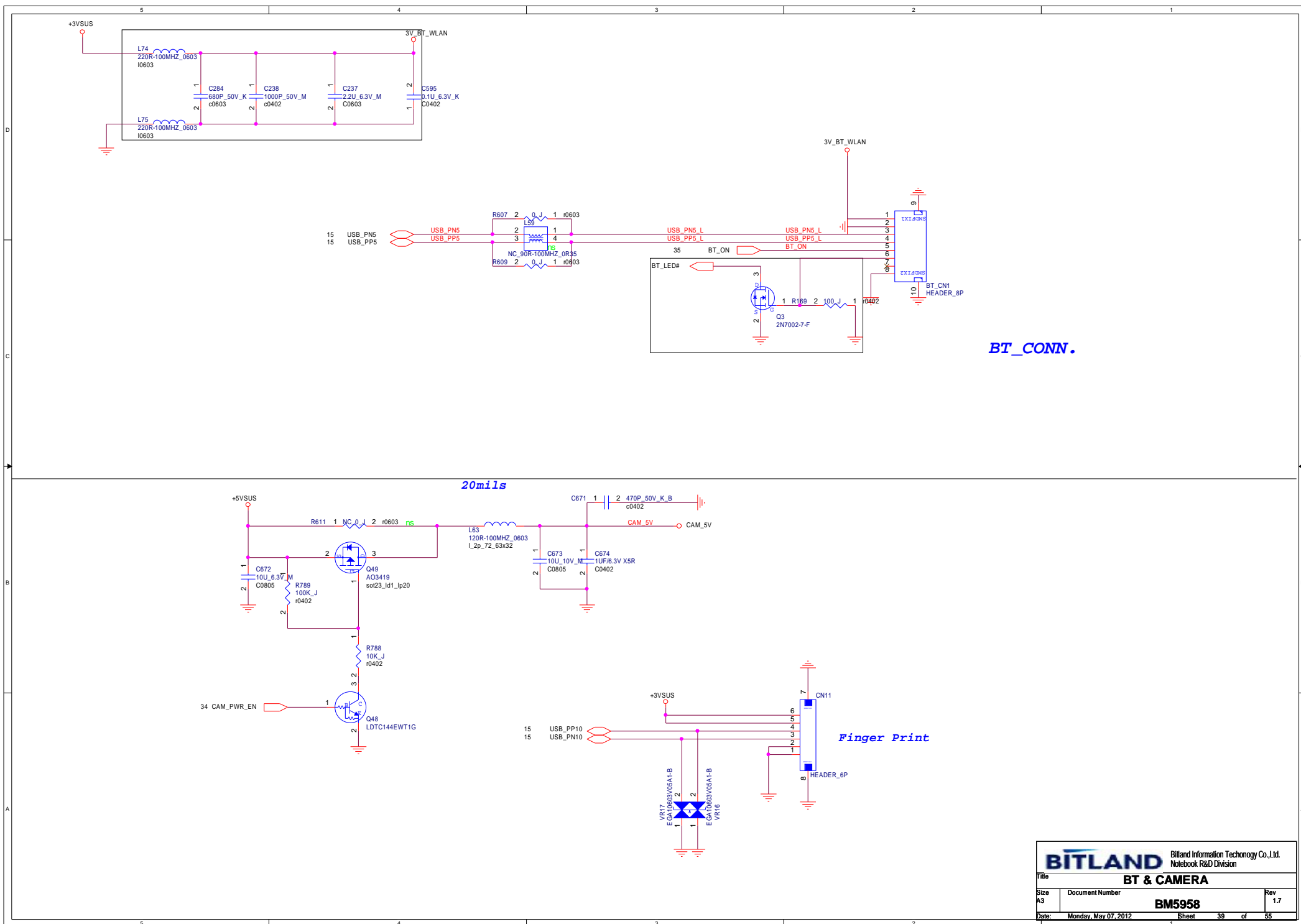





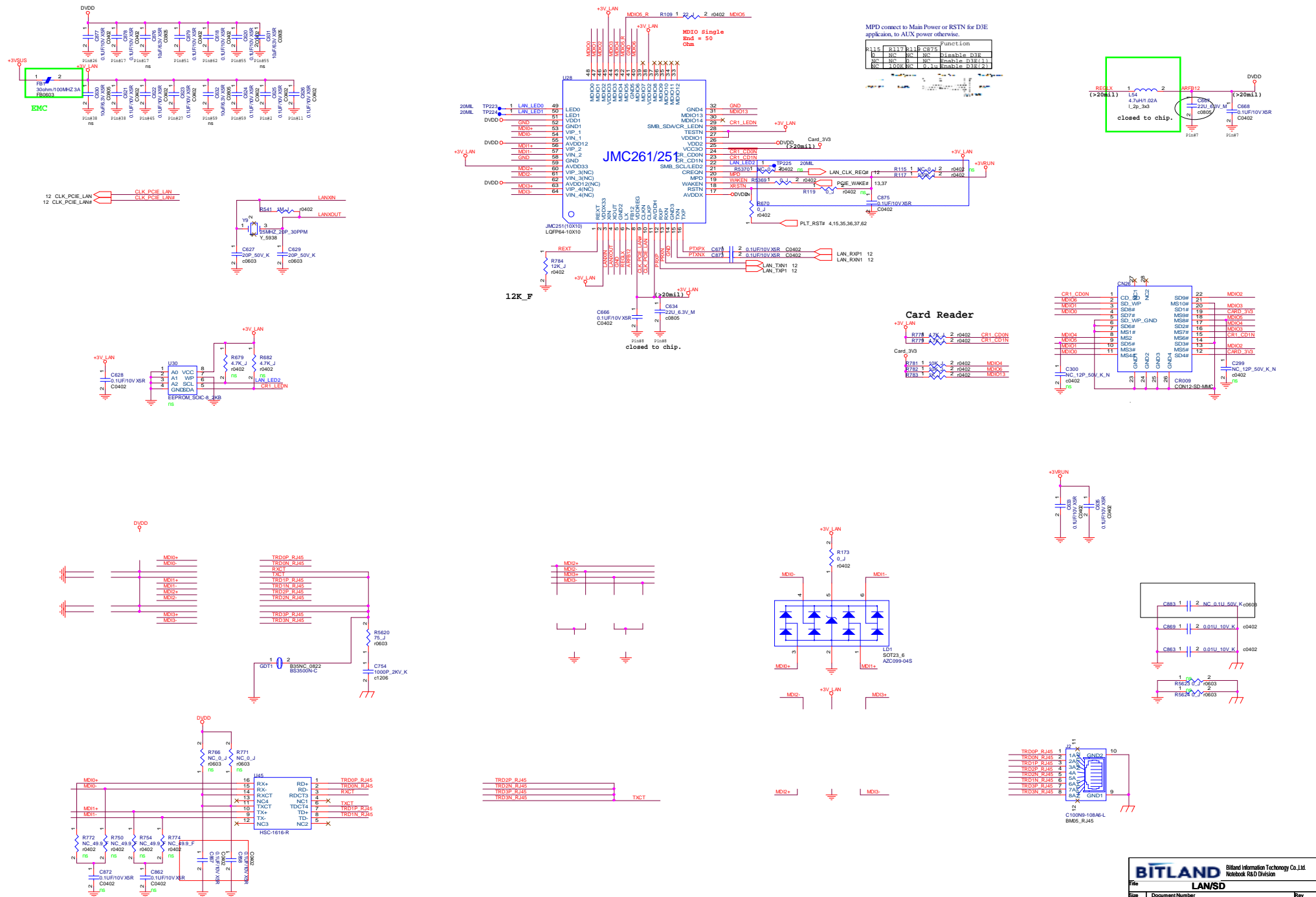


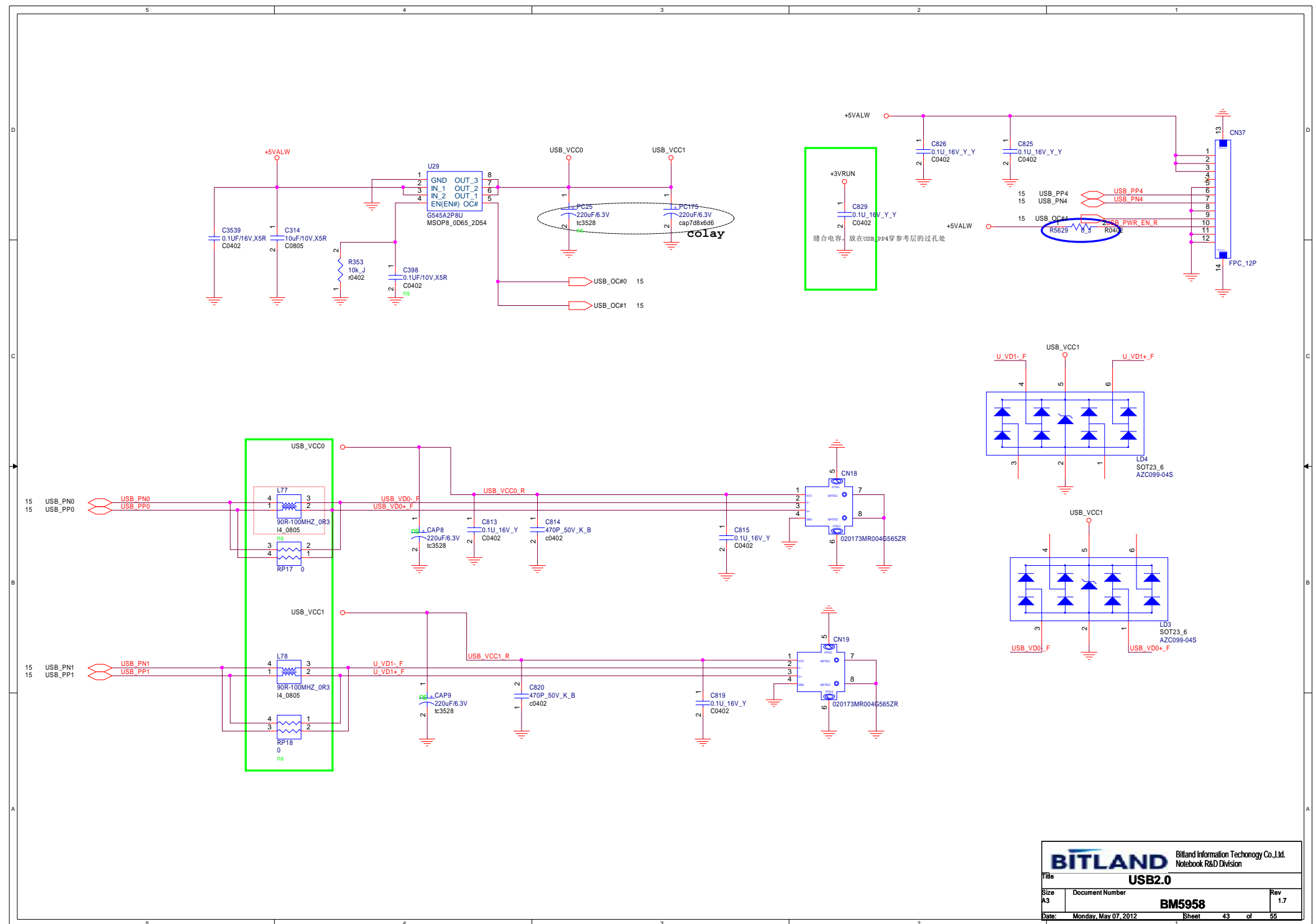
these TP could near the MB outline.

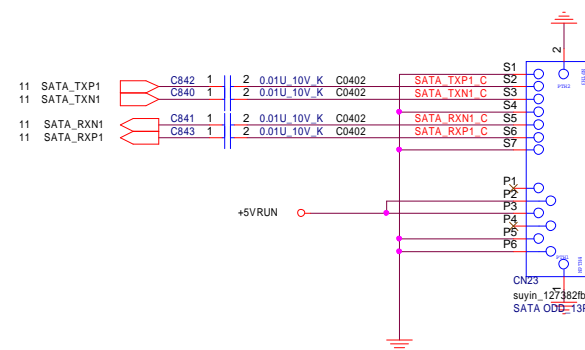
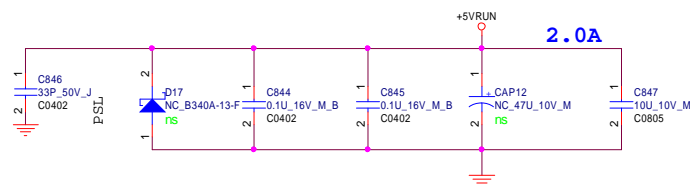
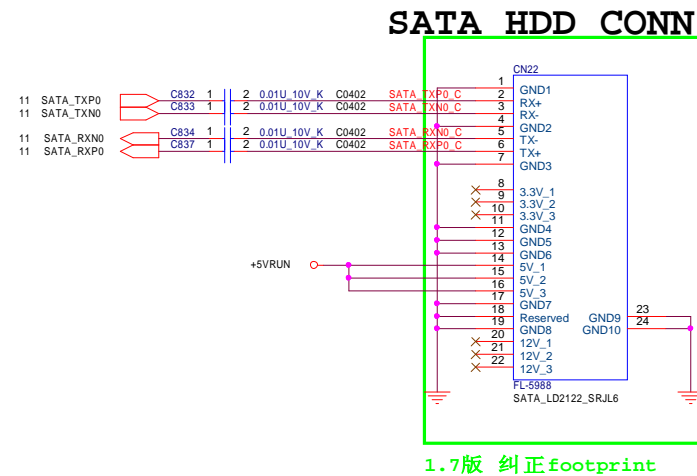
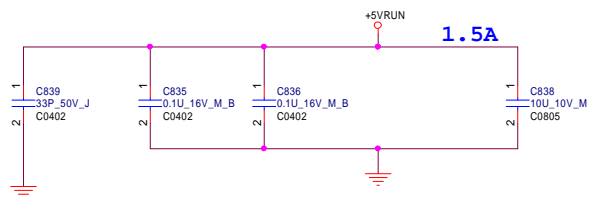
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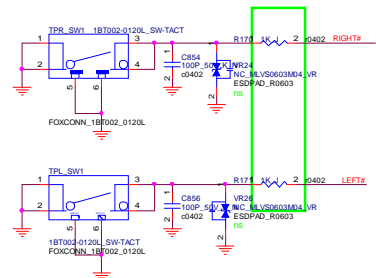
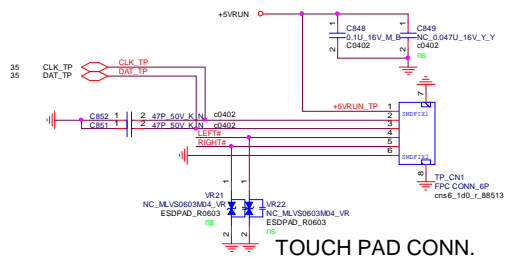
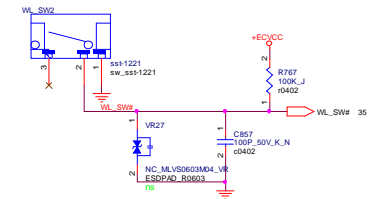
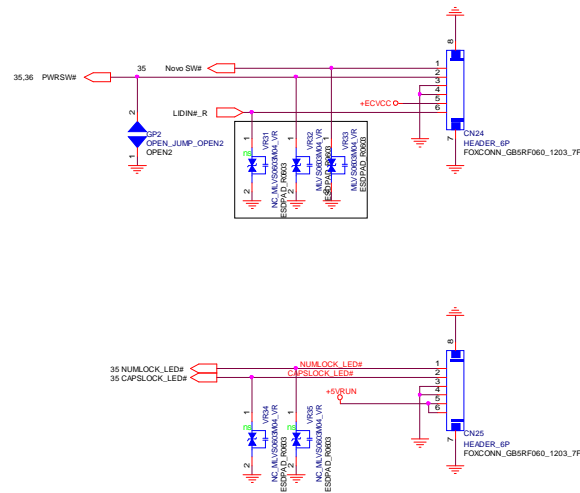
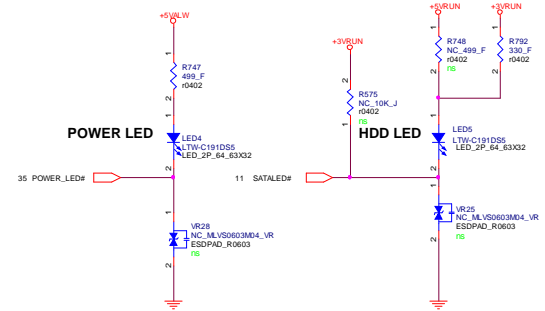
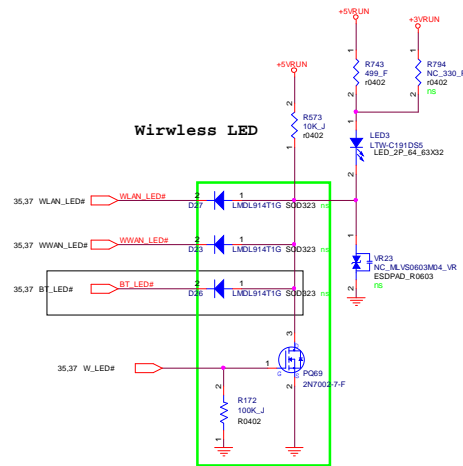
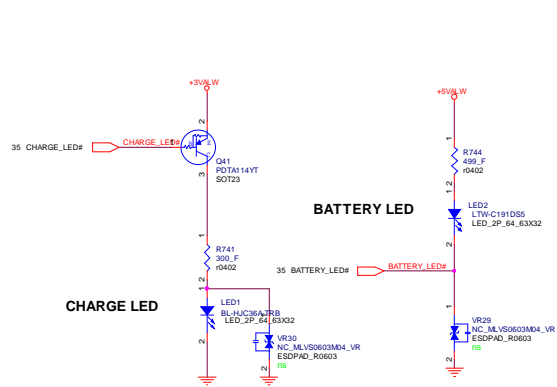


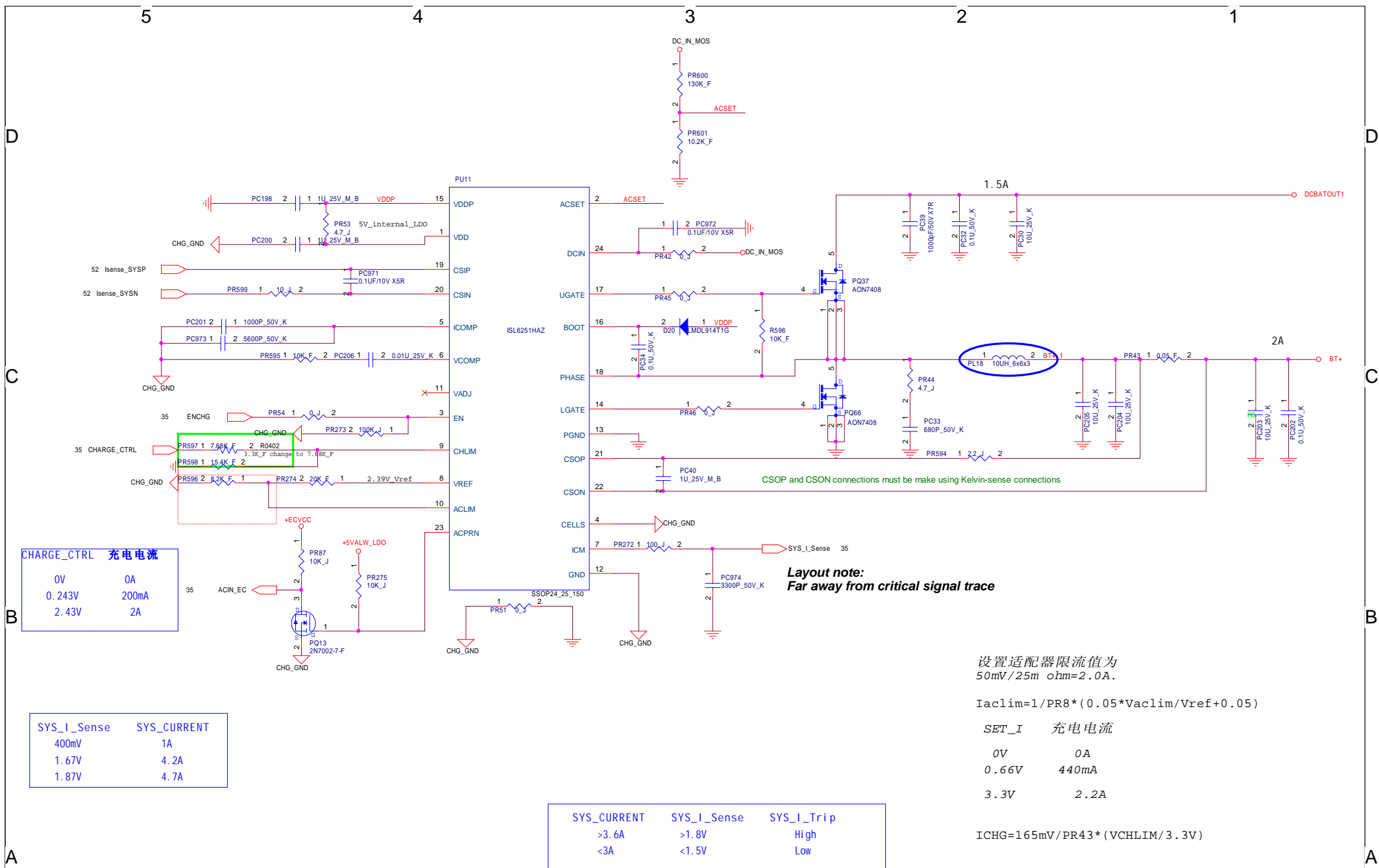
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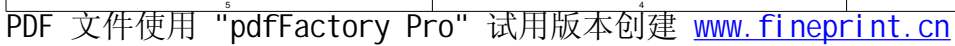




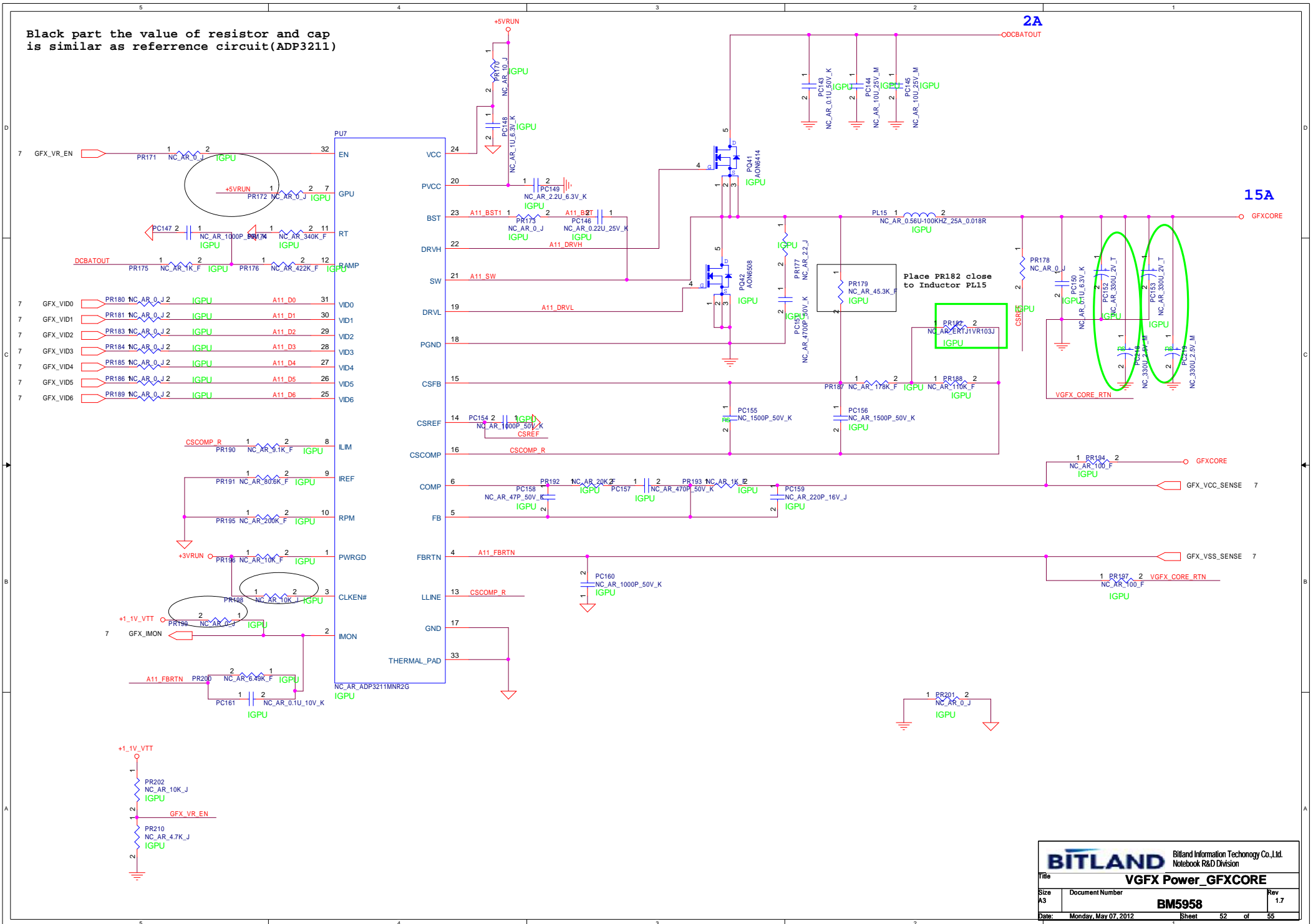


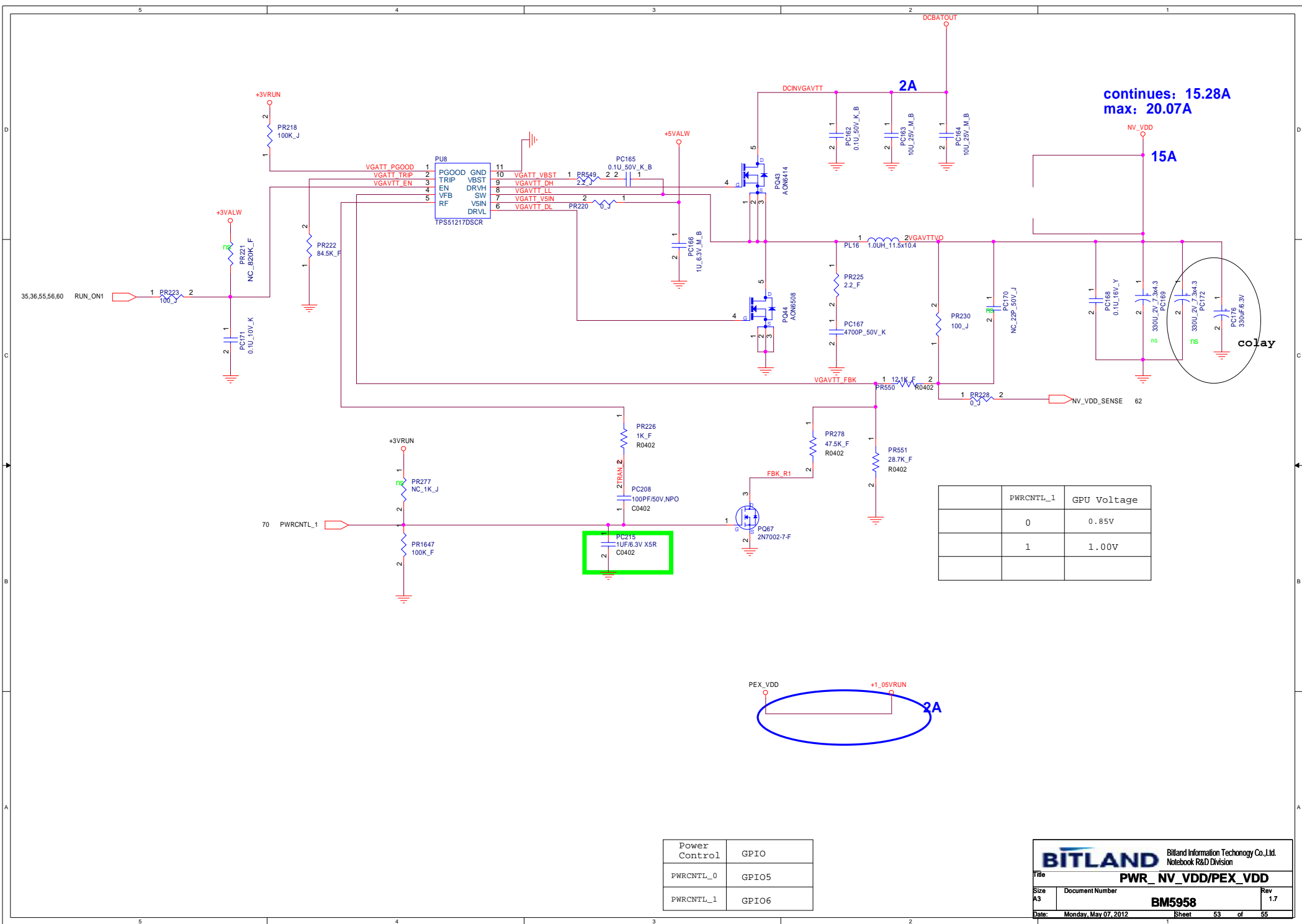


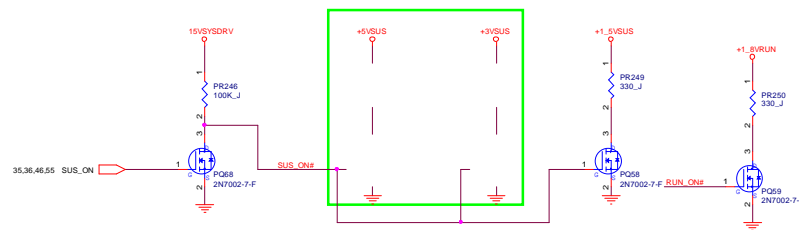
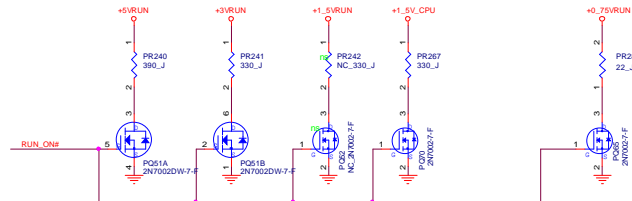
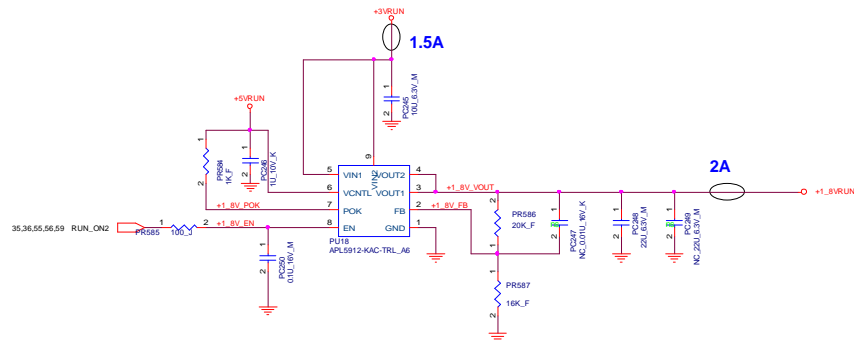


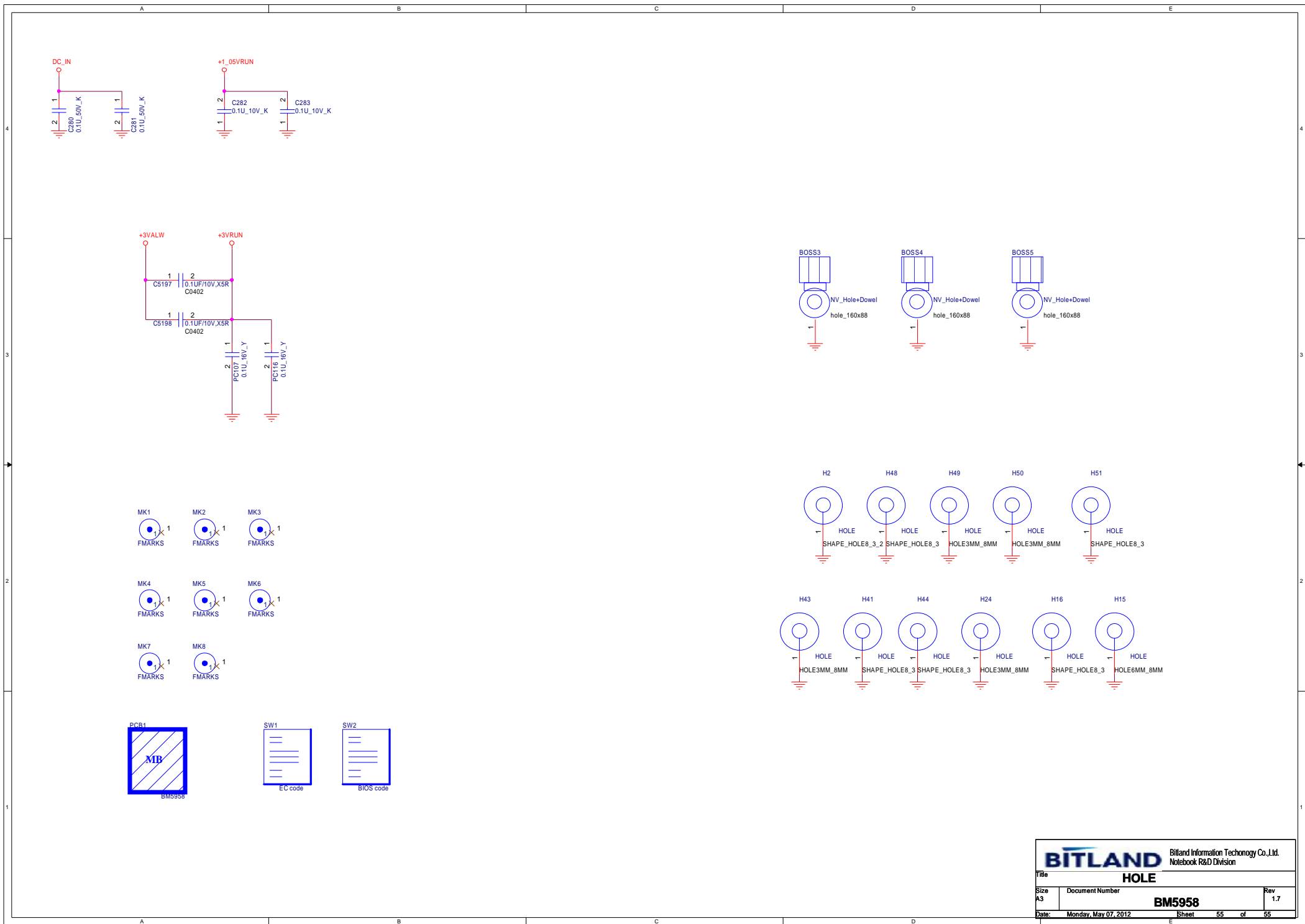


Black part the value of resistor and cap is similar as reference circuit(ADP3211)









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