120mΩ, 1.3A Power Switch with Programmable Current Limit

General Description

The RT9728 is a cost effective, low voltage, single P-MOSFET high side power switch IC for USB application with a programmable current limit feature. Low switch-on resistance (typ.120mΩ) and low supply current (typ. 120μA) are realized in this IC.The RT9728 can offer a programmable current limit threshold between 75mA and 1.3A (typ.) via an external resistor. The ±10% current limit accuracy can be realized for all current limit settings. Besides, a flag output is available to indicate fault conditions to the local USB controller. Furthermore, the chip also integrates an embedded delay function to prevent mis-operation from happening due to high inrush current. The RT9728 is an ideal solution for USB power supply and can support flexible applications since it is functional for various current limit requirements. It is available in WDFN-6L 2x2 package.

Ordering Information

RT9728□□□

- Pin 1 Orientation***
  (2) : Quadrant 2, Follow EIA-481-D
  (For RT9728GQW Only)
- Package Type
  QW : WDFN-6L 2x2 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
  Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

***Empty means Pin1 orientation is Quadrant 1

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

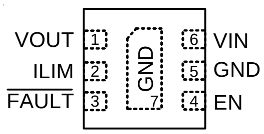
- ±10% Current Limit Accuracy @ 1.3A
- Adjustable Current Limit : 75mA to 1.3A (typ.)
- Meets USB Current Limiting Requirements
- Operating Voltage Range : 2.5V to 5.5V
- Reverse Input – Output Voltage Protection
- Built-in Soft-Start
- 120mΩ High Side MOSFET
- 120μA Supply Current
- RoHS Compliant and Halogen Free

Applications

- USB Bus/Self Powered Hubs
- USB Peripheral Ports
- ACPI Power Distribution
- Battery Power Equipment
- 3G/3.5G Data Card, Set-Top Boxes

Pin Configuration

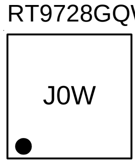
(TOP VIEW)



WDFN-6L 2x2

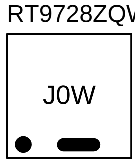
Marking Information

RT9728GQW



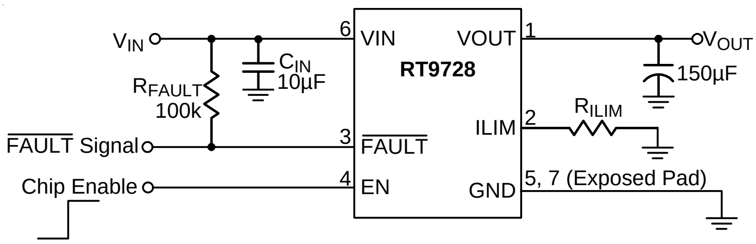
J0 : Product Code
W : Date code

RT9728ZQW

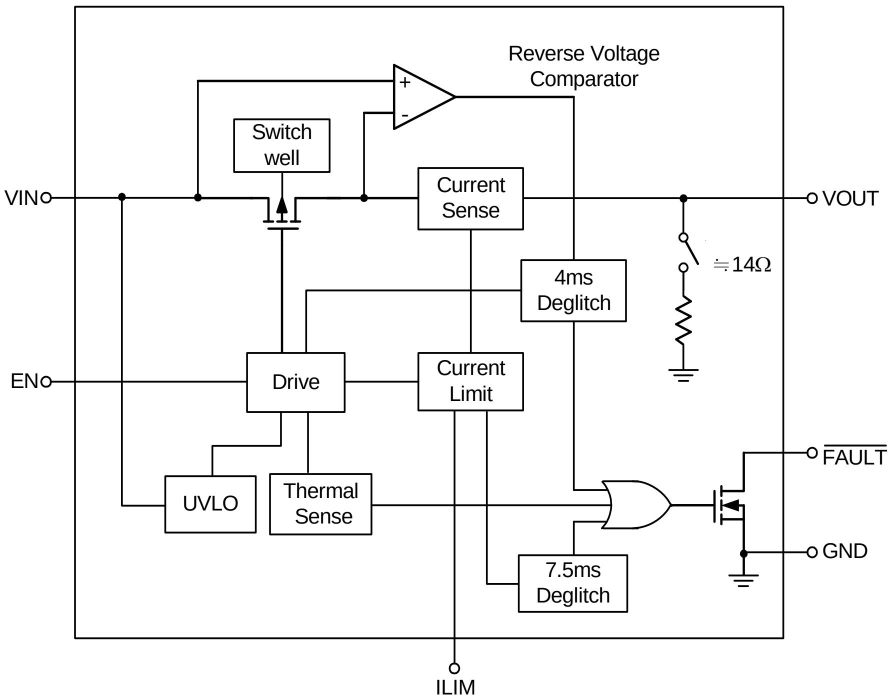


J0 : Product Code
W : Date Code

Typical Application Circuit



Functional Block Diagram



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VOUT	Power switch output.
2	ILIM	External resistor used to set current limit threshold. Recommended 19.1kΩ ≤ R_{ILIM} ≤ 232kΩ.
3	$\overline{\text{FAULT}}$	Active-low open-drain output. Asserted during over current, over temperature, or reverse voltage conditions.
4	EN	Chip enable (Active High).
5, 7 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
6	VIN	Supply input voltage.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- –0.3V to 6V
- Other Pin Voltage ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-6L 2x2 ---------- 0.606W
- Package Thermal Resistance (Note 2)
  WDFN-6L 2x2, θ_{JA} ---------- 165°C/W
  WDFN-6L 2x2, θ_{JC} ---------- 7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 2.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.6V, 19.1kΩ ≤ R_{ILIM} ≤ 232kΩ, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
EN Threshold Voltage	Logic-High	V_{IH}			1.1	--	--	V
	Logic- Low	V_{IL}			--	--	0.66	
Current-Limit Threshold Resistor Range		R_{ILIM}			19.1	--	232	kΩ
Under Voltage Lockout Threshold		UVLO	V_{IN} rising		--	2.35	--	V
			V_{IN} falling		--	2.10	--	
Shutdown Current		I_{SHDN}	V_{IN} = 5.5V, No Load on V_{OUT}, V_{EN} = 0V		--	1	3	μA
Quiescent Current		I_Q	V_{IN} = 5.5V, No Load on V_{OUT}	R_{ILIM} = 20kΩ	--	120	170	μA
				R_{ILIM} = 210kΩ	--	120	170	
Reverse Leakage Current		I_{REV}	V_{OUT} = 5.5V, V_{IN} = 0V		--	1	3	μA
Thermal Shutdown Temperature		T_{SD}			--	160	--	°C
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	I_{SW} = 0.2A		--	120	--	mΩ
Current Limit		I_{LIM}	R_{ILIM} = 20kΩ		1166	1295	1425	mA
			R_{ILIM} = 49.9kΩ		468	520	572	
			R_{ILIM} = 210kΩ		110	130	150	
			I_{LIM} shorted to V_{IN}		50	75	100	
Reverse Voltage Comparator Trip Point (V_{OUT} – V_{IN})					--	135	--	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
$\overline{FAULT}$ Output Low Voltage	V_{OL}	$I_{\overline{FAULT}}$ = 1mA	--	180	--	mV
$\overline{FAULT}$ Off State Leakage		$V_{\overline{FAULT}}$ = 5.5V	--	1	--	μA
$\overline{FAULT}$ Deglitch		$\overline{FAULT}$ assertion or de-assertion due to over current condition	5	7.5	10	ms
		$\overline{FAULT}$ assertion or de-assertion due to reverse voltage condition	2	4	6	

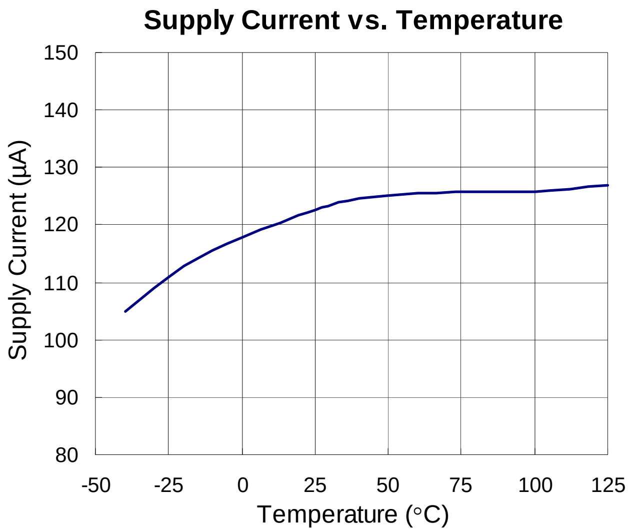
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

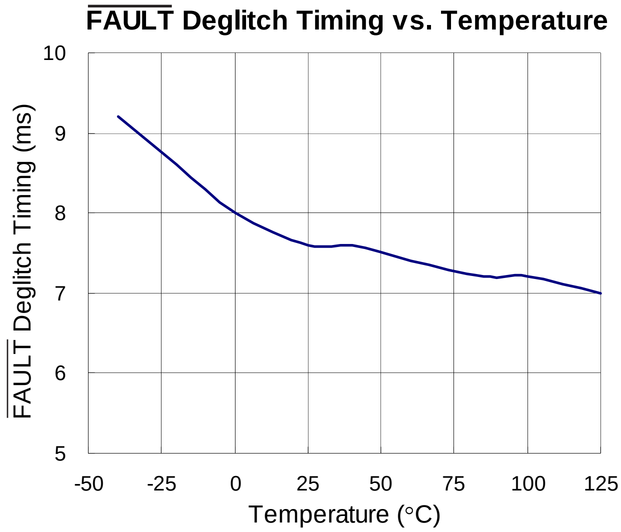
Note 2. θ_{JA} is measured at T_A = 25°C on a low effective thermal conductivity single-layer test board per JEDEC 51-3. θ_{JC} is measured at the exposed pad of the package.

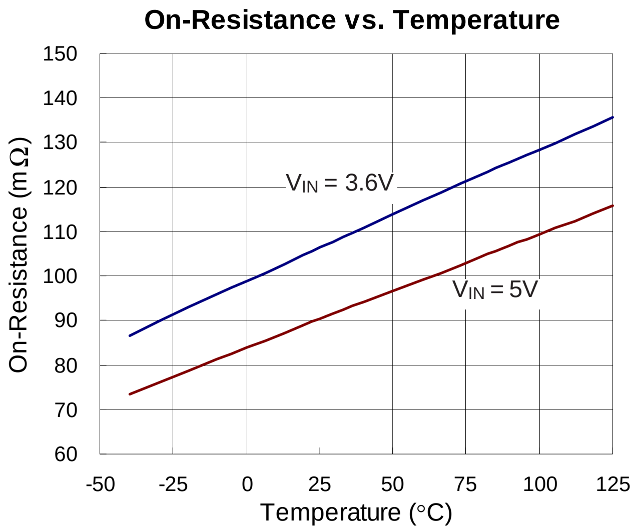
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

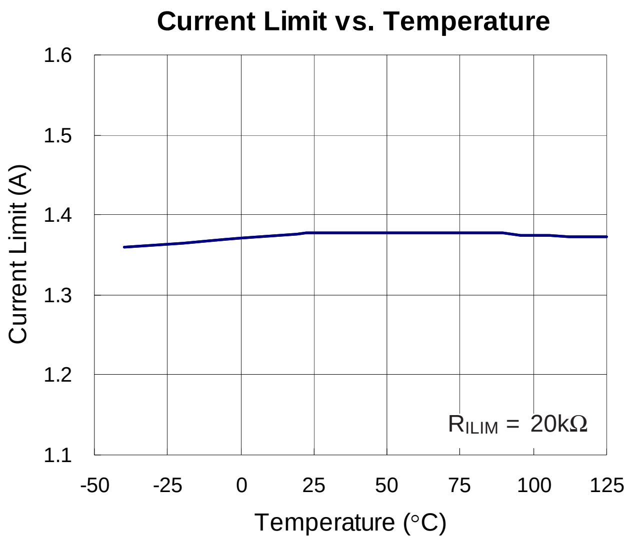
Note 4. The device is not guaranteed to function outside its operating conditions.

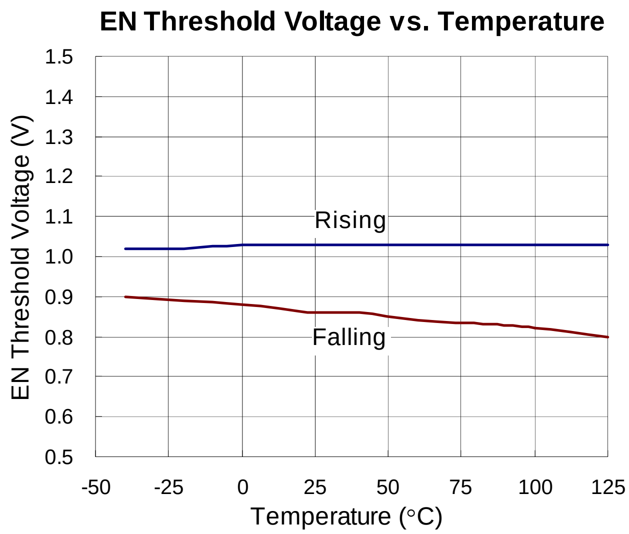
Typical Operating Characteristics

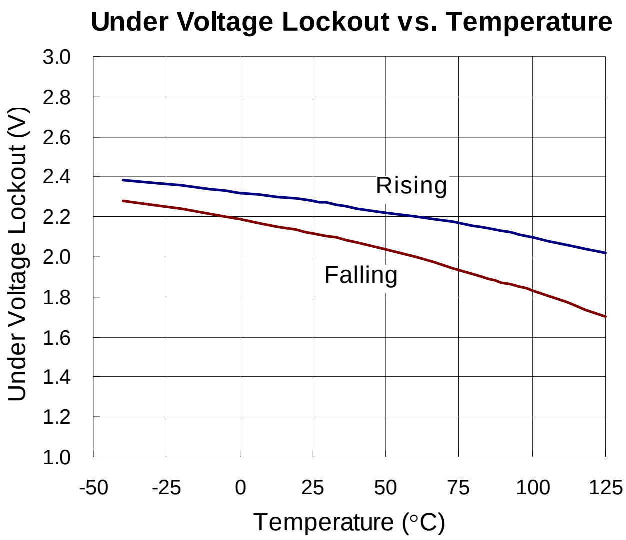




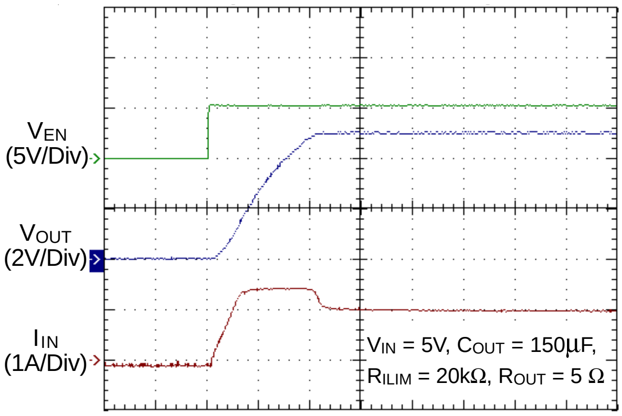






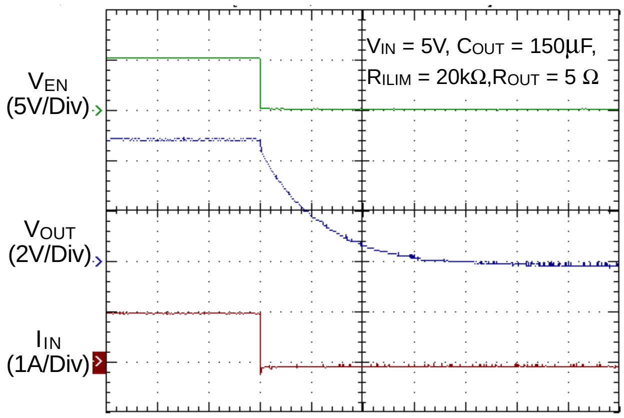


Power On from EN



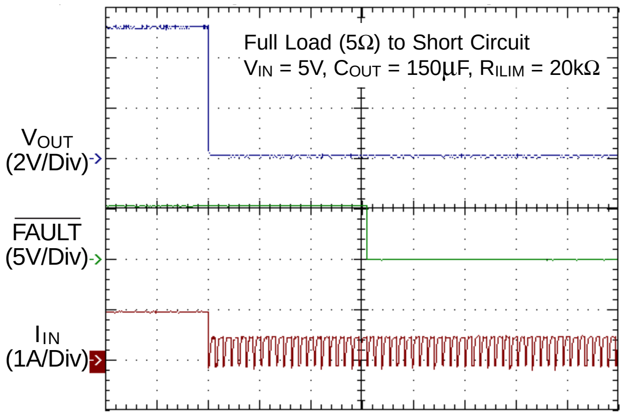
Time (500µs/Div)

Power Off from EN



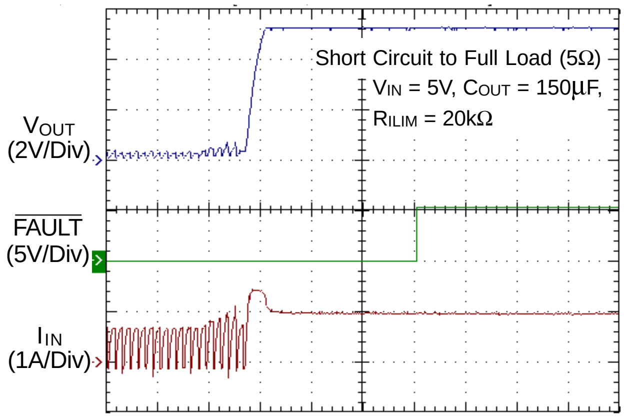
Time (500µs/Div)

Current Limit



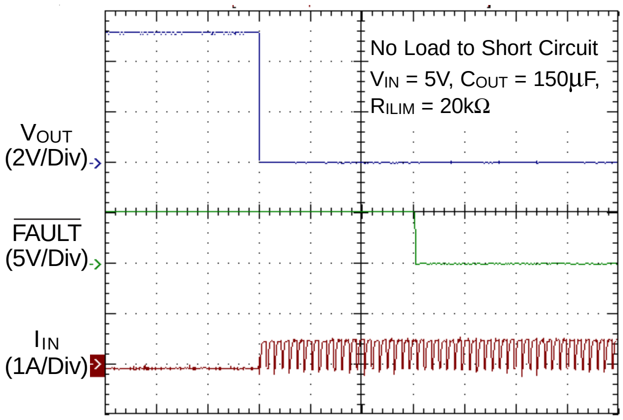
Time (2.5ms/Div)

Current Limit



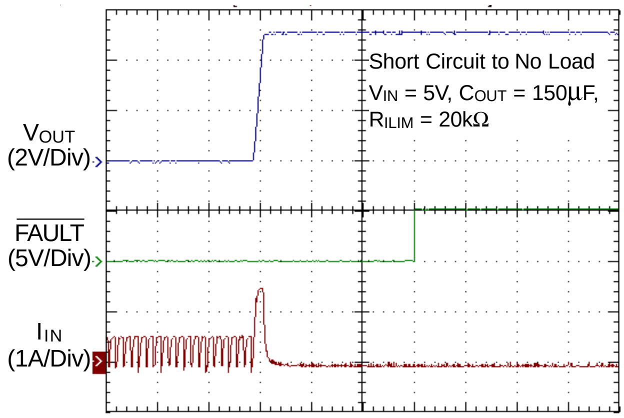
Time (2.5ms/Div)

Current Limit

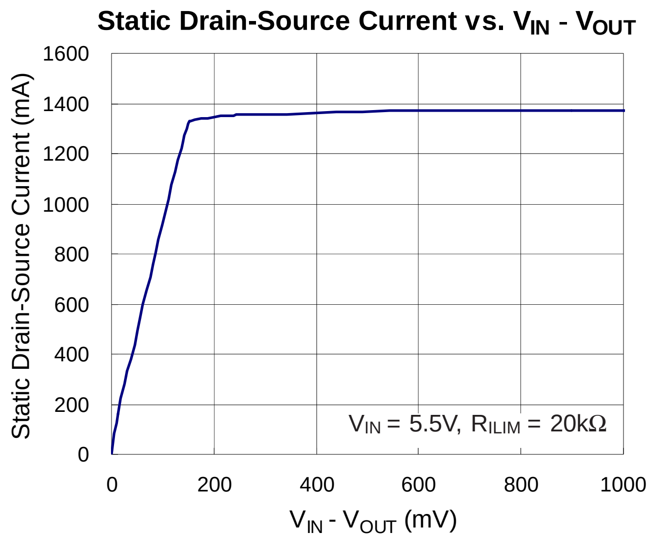


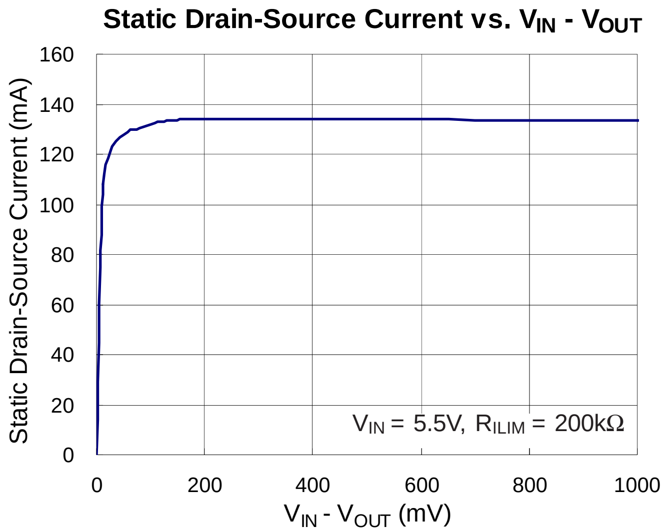
Time (2.5ms/Div)

Current Limit



Time (2.5ms/Div)


Static Drain-Source Current vs. VIN - VOUT
Static Drain-Source Current (mA)
1600
1400
1200
1000
800
600
400
200
0
0
200
400
600
800
1000
VIN - VOUT (mV)
VIN = 5.5V, RILIM = 20kΩ


Static Drain-Source Current vs. VIN - VOUT
Static Drain-Source Current (mA)
160
140
120
100
80
60
40
20
0
0
200
400
600
800
1000
VIN - VOUT (mV)
VIN = 5.5V, RILIM = 200kΩ

Application Information

The RT9728 is a single P-MOSFET high side power switch with active high enable input, optimized for self powered and bus powered Universal Serial Bus (USB) applications. The switch's low $R_{DS(ON)}$ meets USB voltage drop requirements and a flag output is available to indicate fault conditions to the local USB controller.

Current Limiting and Short Circuit Protection

When a heavy load or short circuit situation occurs while the switch is enabled, large transient current may flow through the device. The RT9728 includes a current limit circuitry to prevent these large currents from damaging the MOSFET switch and the hub downstream ports. The RT9728 provides an adjustable current limit threshold between 120mA and 1.3A (typ.) via an external resistor, R_{ILIM}, between 19.1kΩ and 232kΩ. However, if the ILIM pin is connected to V_{IN}, the current limit threshold will be 75mA (typ.). Once the current limit threshold is exceeded, the device enters constant current mode until either thermal shutdown occurs or the fault is removed. The table1 shows a recommended current limit value vs. R_{ILIM} resistor.

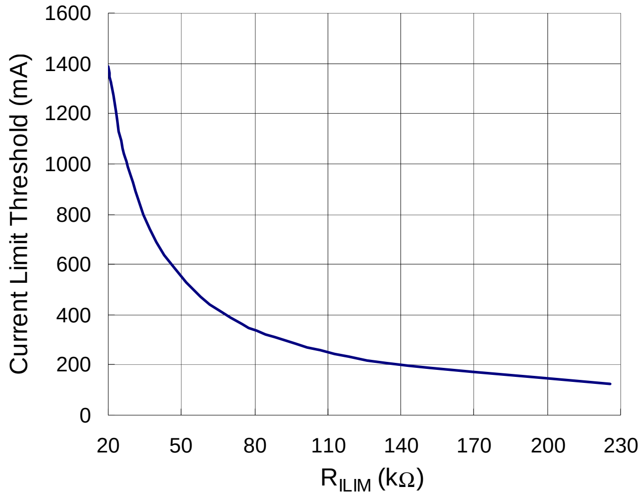


Figure 1. Current Limit Threshold vs. R_{ILIM}

Table 1. Recommended R_{ILIM} Resistor Selections

Desired Nominal Current Limit (mA)	Ideal Resistor (kΩ)	Closet 1% Resistor (kΩ)	Actual Limits (Include R Tolerance)		
			IOS Min (mA)	IOS Nom (mA)	IOS Max (mA)
75	Short Ilim to VIN		50.0	75.0	100.0
120	226.1	226.0	101.3	120.0	142.1
200	134.0	133.0	173.7	201.5	233.9
300	88.5	88.7	262.1	299.4	342.3
400	65.9	66.5	351.1	396.7	448.7
500	52.5	52.3	443.9	501.6	562.4
600	43.5	43.2	535.1	604.6	674.1
700	37.2	37.4	616.0	696.0	776.0
800	32.4	32.4	708.7	800.8	892.9
900	28.7	28.7	797.8	901.5	1005.2
1000	25.8	26.1	875.4	989.1	1102.8
1100	23.4	23.2	982.1	1109.7	1237.3
1200	21.4	21.5	1057.9	1195.4	1332.9
1300	19.7	19.6	1158.0	1308.5	1459.0

Fault Flag

The RT9728 provides a $\overline{FAULT}$ signal pin which is an N-Channel open drain MOSFET output. This open drain output goes low when current exceeds current limit threshold. The $\overline{FAULT}$ output is capable of sinking a 1mA load to typically 180mV above ground. The $\overline{FAULT}$ pin requires a pull-up resistor ; this resistor should be large in value to reduce energy drain. A 100kΩ pull-up resistor works well for most applications. In case of an over current condition, $\overline{FAULT}$ will be asserted only after the flag response delay time, t_D, has elapsed. This ensures that $\overline{FAULT}$ is asserted upon valid over current conditions and that erroneous error reporting is eliminated. For example, false over current conditions may occur during hot-plug events when extremely large capacitive loads are connected, which induces a high transient inrush current that exceeds the current limit threshold. The $\overline{FAULT}$ response delay time, t_D, is typically 7.5ms.

Supply Filter/Bypass Capacitor

A 10μF low-ESR ceramic capacitor connected from V_{IN} to GND and located close to the device is strongly recommended to prevent input voltage drooping during hot-plug events. However, higher capacitor values may be used to further reduce the voltage droop on the input. Without this bypass capacitor, an output short may cause sufficient ringing on the input (from source lead inductance) to destroy the internal control circuitry. Note that the input transient voltage must never exceed 6V as stated in the Absolute Maximum Ratings.

Output Filter Capacitor

A low-ESR 150μF aluminum electrolytic capacitor connected between V_{OUT} and GND is strongly recommended to meet the USB standard maximum droop requirement for the hub, V_{BUS}. Standard bypass methods should be used to minimize inductance and resistance between the bypass capacitor and the downstream connector to reduce EMI and decouple voltage droop caused by hot-insertion transients in downstream cables. Ferrite beads in series with V_{BUS}, the ground line and the 0.1μF bypass capacitors at the power connector pins are recommended for EMI and ESD protection. The bypass capacitor itself should have a low dissipation factor to allow decoupling at higher frequencies.

Chip Enable Input

The RT9728 will be disabled when the EN pin is in a logic low condition. During this condition, the internal circuitry and MOSFET are turned off, reducing the supply current to 1μA typical. The maximum guaranteed voltage for a logic-low at the EN pin is 0.66V. A minimum guaranteed voltage of 1.1V at the EN pin will turn off the RT9728. Floating the input may cause unpredictable operation. EN should not be allowed to go negative with respect to GND.

Under Voltage Lockout

Under Voltage Lockout (UVLO) prevents the MOSFET switch from turning on until input voltage exceeds approximately 2.3V. If input voltage drops below approximately 2.1V, UVLO turns off the MOSFET switch and $\overline{FAULT}$ will be asserted accordingly. The under voltage lockout detection functions only when the switch is enabled.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-6L 2x2 packages, the thermal resistance, θ_{JA}, is 165°C/W on a standard JEDEC 51-3 single layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (165°C/W) = 0.606W for WDFN-6L 2x2 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

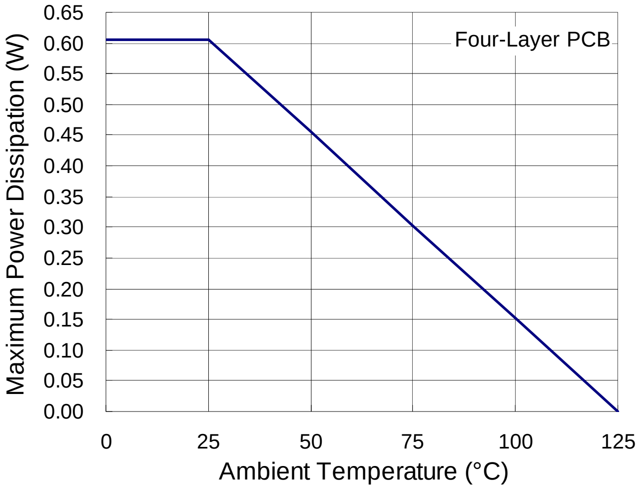
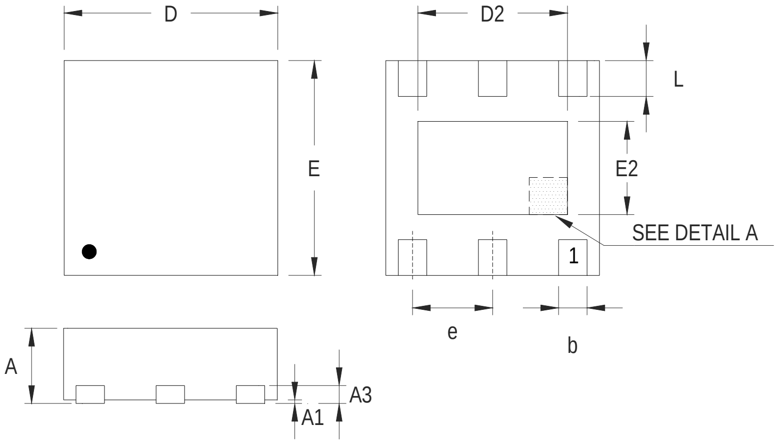
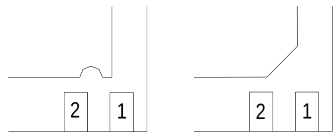


Figure 2. Derating Curve of Maximum Power Dissipation

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.350	0.008	0.014
D	1.950	2.050	0.077	0.081
D2	1.000	1.450	0.039	0.057
E	1.950	2.050	0.077	0.081
E2	0.500	0.850	0.020	0.033
e	0.650		0.026	
L	0.300	0.400	0.012	0.016

W-Type 6L DFN 2x2 Package

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