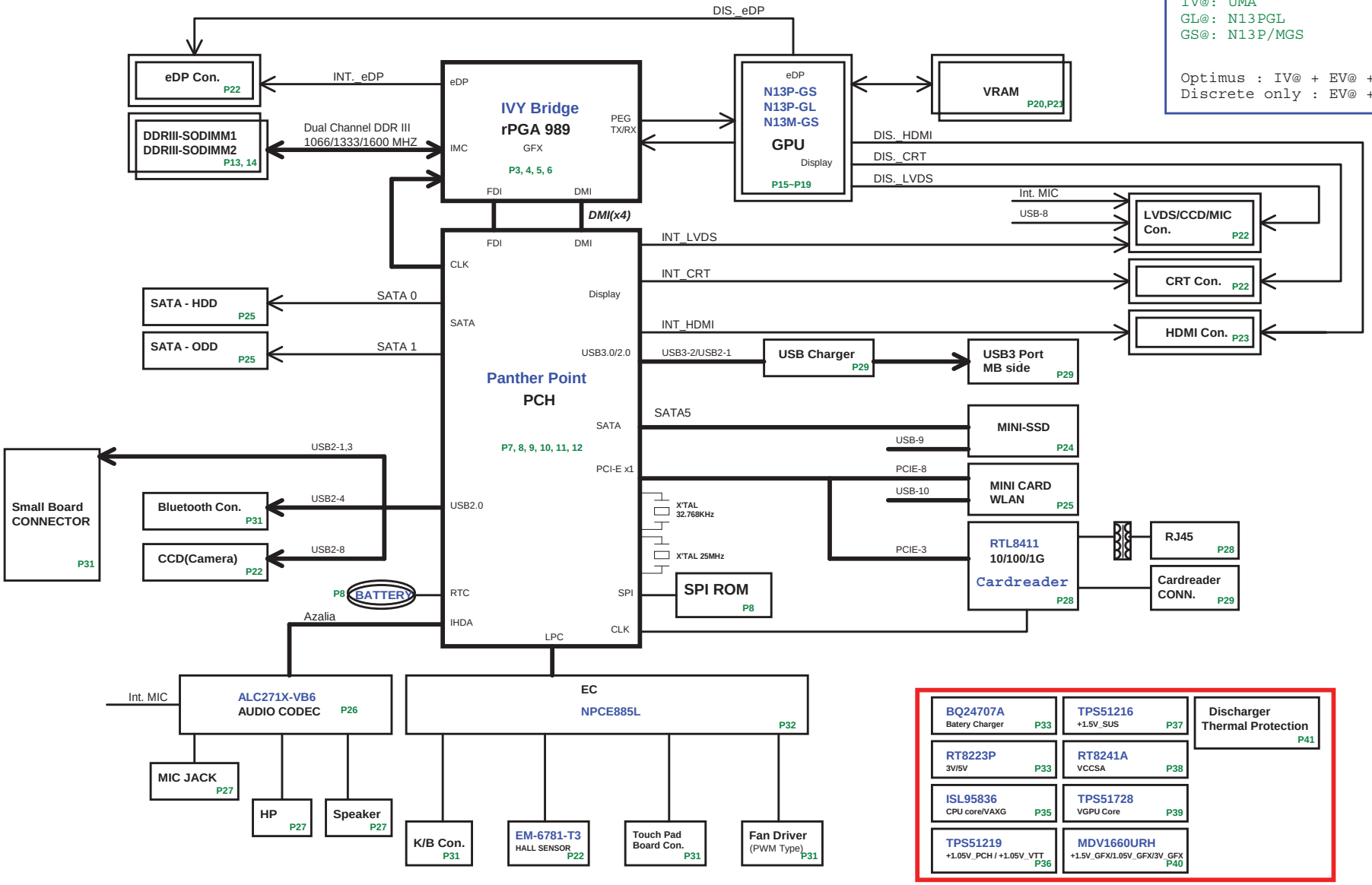
ZQTA/ZQSA CRV SYSTEM BLOCK DIAGRAM

BOM

```
IV@ : iGPU
EV@ : dGPU
OP@ : Optimus
DO@ : Discrete only
SP@ : Special
SNP@: N13PGS/GL
IV@: UMA
GL@: N13PGL
GS@: N13P/MGS

Optimus : IV@ + EV@ + OP@
Discrete only : EV@ + DO@
```



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	Block Diagram	1A

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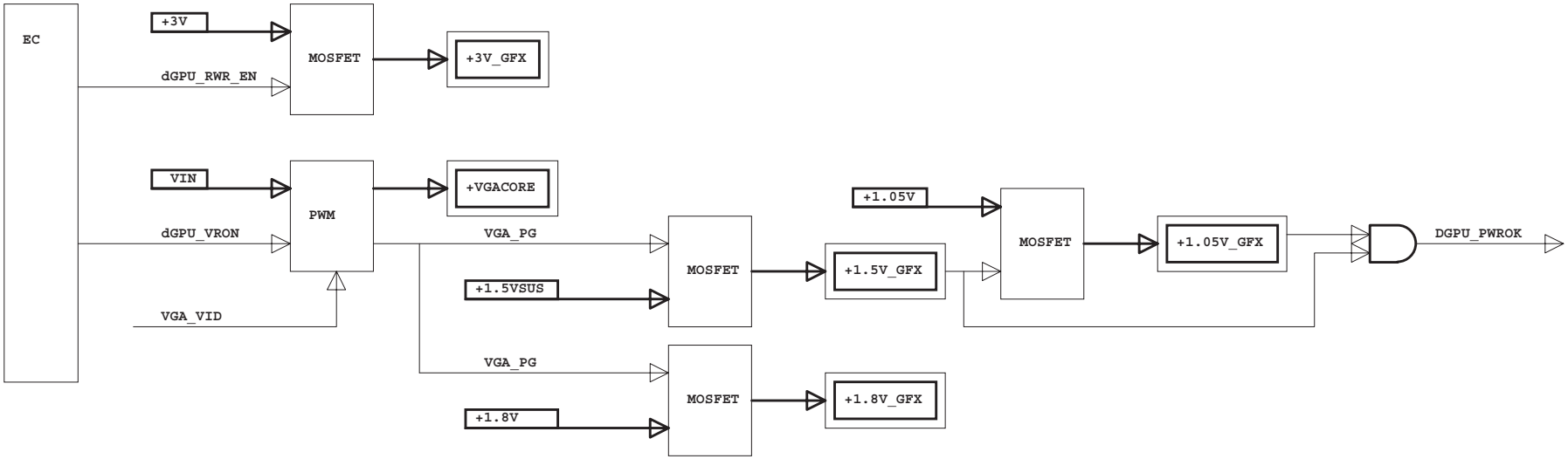
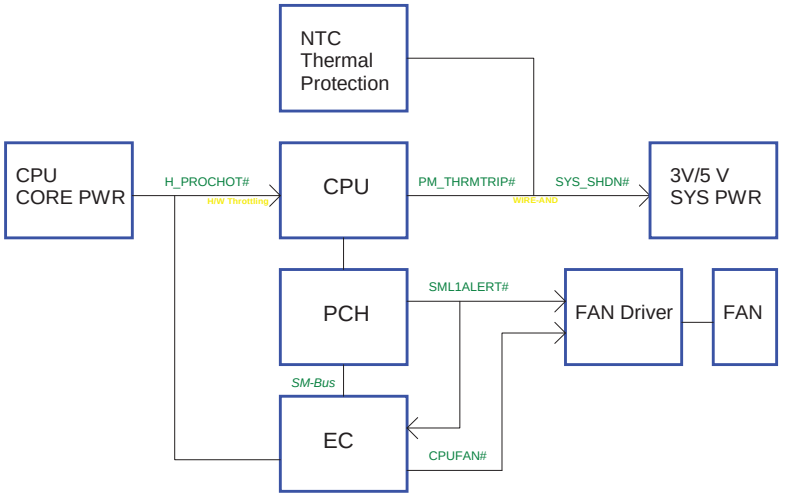
VGA power up sequence



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	VRON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER/IVY/SNB bridge VCCIO	MAINON	S0
+VCCSA	+0.9V	CPU POWER	HWPG_VTT	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
			MAINON	S0

Thermal Follow Chart



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IVY Bridge Processor (DMI,PEG,FDI)

For Sandy Bridge processor only implementation:
PROC_SELECT can be left NC.

For IVY/Sandy processor compatibility:
Needs a pull-up resistor to PCH VccDFTERM rail (1.8V) through a 2.2 K±5% pull-up resistor.
Connect to the DF_TVS of PCH though a 1K±5% series resistor.

U16A

DMI
Intel(R) FDI
PCI EXPRESS* - GRAPHICS
eDP

PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

Ivy Bridge_rPGA_2DPC_Rev0p61

HPD disable
This signal can be left as no connect if entire eDP interface is disabled.

DG 1.0 :
The recommended AC cap value is changed to 220nF for compatibility with PCIe Gen3 on future platforms.
For Gen2 only designs, it is acceptable to continue to use the 100nF capacitor.

IVY Bridge Processor (CLK,MISC,JTAG)

U16B

MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM

Intel recommended UNCOREPWRGOOD routing on one layer

apply C5205 for nosie

Ivy Bridge_rPGA_2DPC_Rev0p61

wo eDP and dGPU
Connect DPLL_REF_SSCLK on Processor to GND through 1K ± 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K ± 5% resistor

	EV	UMA/OPT.
Ra	NA	0 ohm
Rb	1K	NA
Rc	1K	NA

CRB 1.0 : SM_RCOMP[2..0] W:20mils, S:15mils, L 500mils

For XDP

CRB 1.0 : change to +3V(S0)

FDI Disabling (Discrete Only)

9/26 add

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

DP & PEG Compensation

Routed within 25 mils

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Routed within 500 mils

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms

PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up(CPU)

9/27 modify

Q4 FDV301N
Q5 MMBT3904
Q30 *2N7002K

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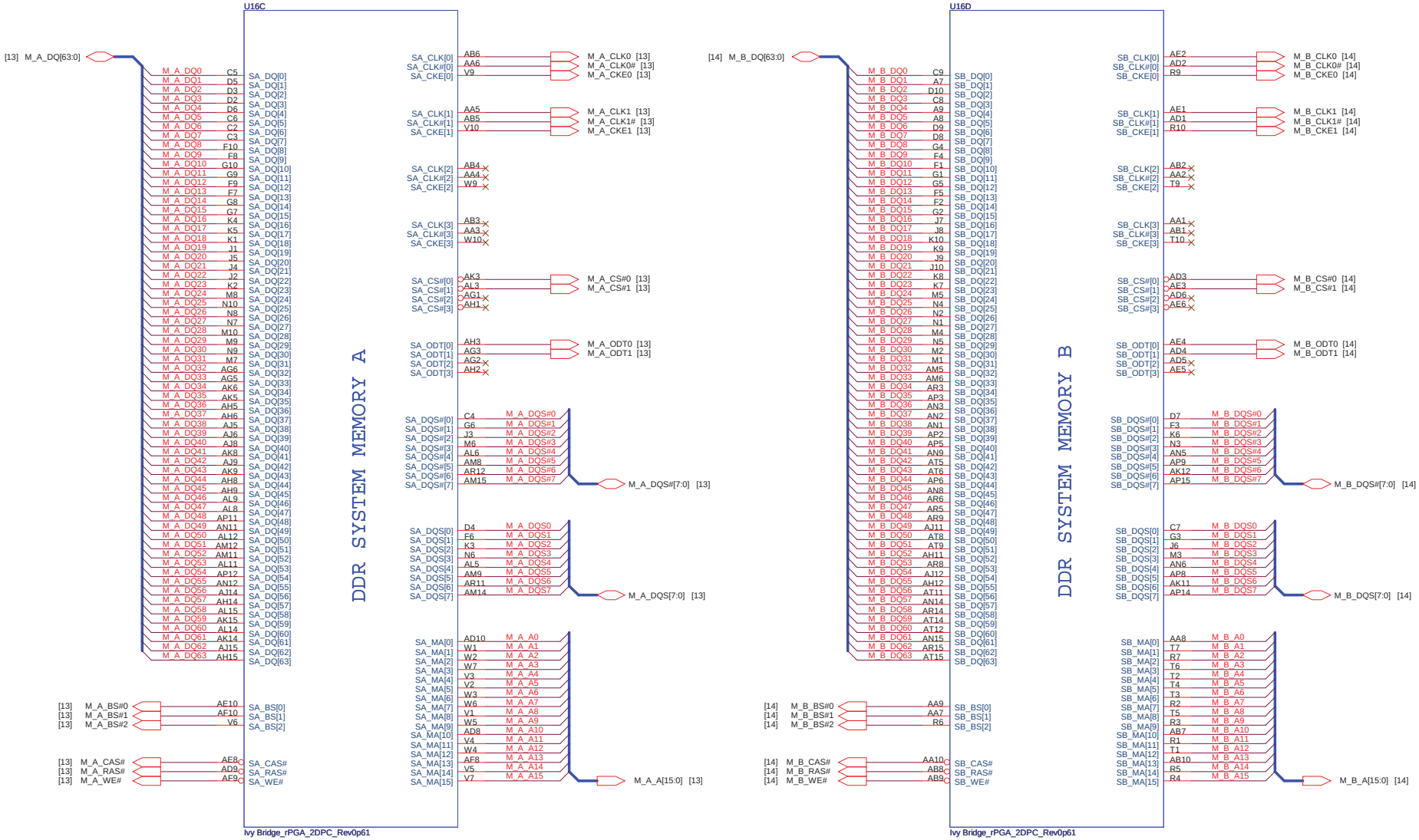
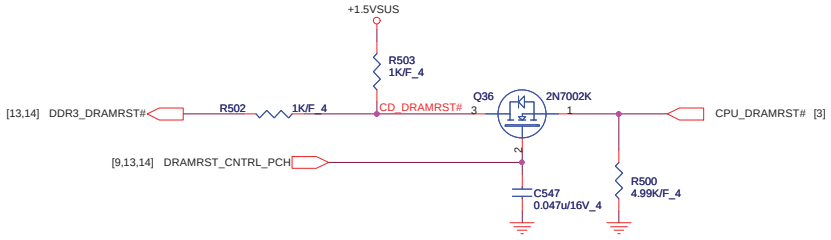
IVY Bridge Processor (DDR3)





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IVY Processor (POWER)

IVY Bridge Processor (GRAPHIC POWER)

POWER

0929 change value by CRB

CPU Core Power
IVY 45W:TDC 52A

IVY SPEC
22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4
total : 10uF x 10 , RSVD x 1
total : 22uF x 16 , RSVD x 3
tatal : 470u x 4, RSVD x2

SNB : Spec	Cose down
470uF/4mohm x 4	330uF x2
22uF x 16	22uF x 4
10uF x 10	10uF x 20 reserved x 5

CPU VTT
IVY 45W:8.5A

SNB : Spec	Cose down
330uF/6mohm x 2	330uF x1
22uF x 12	22uF x 2
22uF x 7 (Non-stuff)	10uF x 10 reserved x 4

CPU VGT
IVY 45W:TDC 38A

Spec	Cose down
470uF/4mohm x 2	330uF x1
22uF x 12	22uF x 4
	10uF x 10

IVY SPEC
22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

U16F

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

IVY SPEC
22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

U16G

GRAPHICS

SENSE LINES

VREF

DDR3 - 1.5V RAILS

SA RAIL

1.8V RAIL

MISC

	DIS. VGA	UMA/ Optimus
Ra	0 ohm	NA

CPU VCCPL
IVY 45W:1.5A

Spec	Real
330uF/7mohm x 1	10uF x 1
10uF x 1	1uF x 2
1uF x 2	

IVY SPEC
330uF x1, 10uF_8 x1, 1uF_4 x2
Socket BOT edge.

10uF (Reserved)

4.5A

10 mil

For M3 solution need Rb4, Rd1 W/O M3 then NC ball B4 and D1

IVY SPEC
330uF x1, 10uF_8 x6 Socket BOT edge.

Voltage selection for VCCIO:
this pin must be pulled high on the motherboard

On CRB
H_SNB_IVB#_PWRCTRL = low, 1.0V
H_SNB_IVB#_PWRCTRL = high/NC, 1.05V

Trace Route to Power IC area.

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

Remove PU resistor 54.9/F, stuff at IMVP7 page

Place PU resistor close to CPU

SVID DATA

Remove PU resistor 130/F, stuff at IMVP7 page

Place PU resistor close to CPU

SVID ALERT

IVY SPEC
330uF x1, 10uF_8 x1 Socket BOT edge, 10uF_8 x2 Socket BOT cavity.

CPU SA
IVY 45W: 6A

Spec	Real
330uF/7mohm x 1	10uF x 3
10uF x 3	

CPU MCH
IVY 45W: 5A

Spec	
330uF/6mohm x 1	
10uF x 6	
Real	
10uF x 8	

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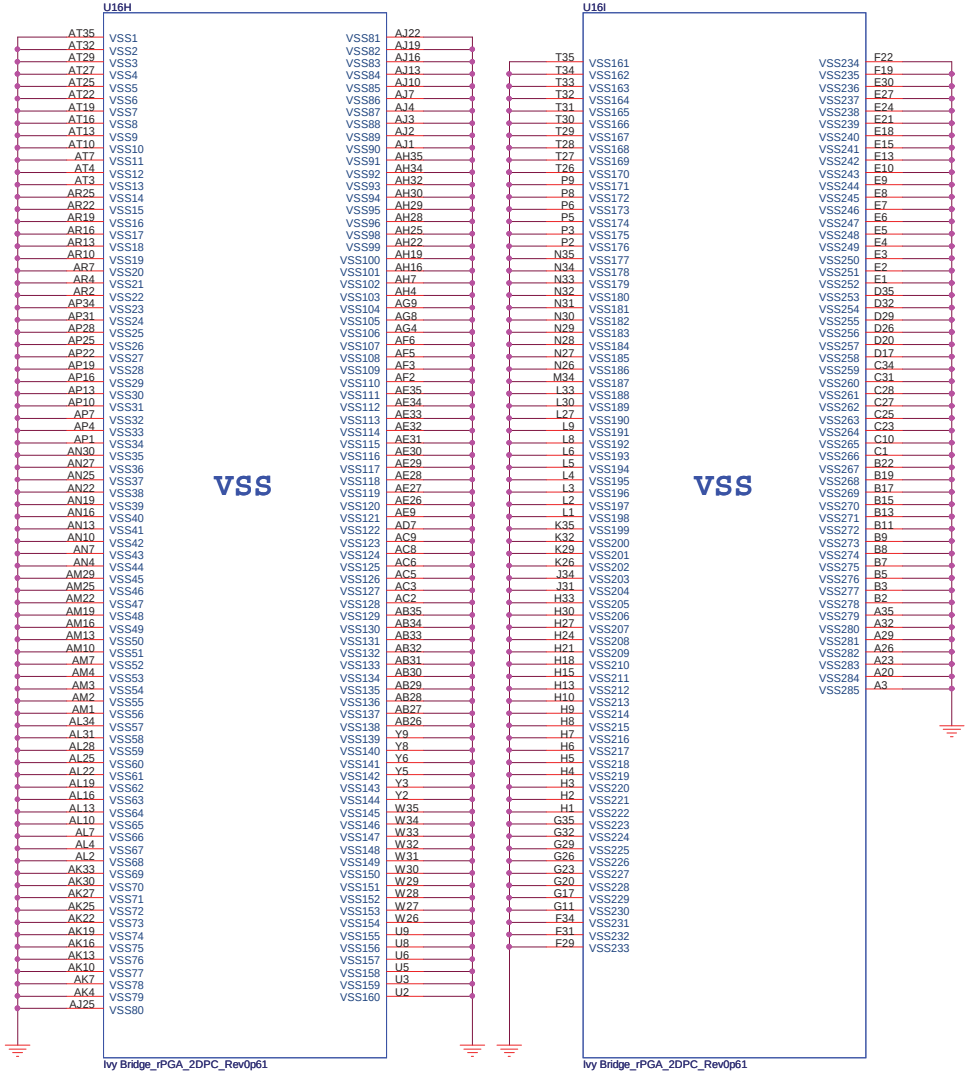
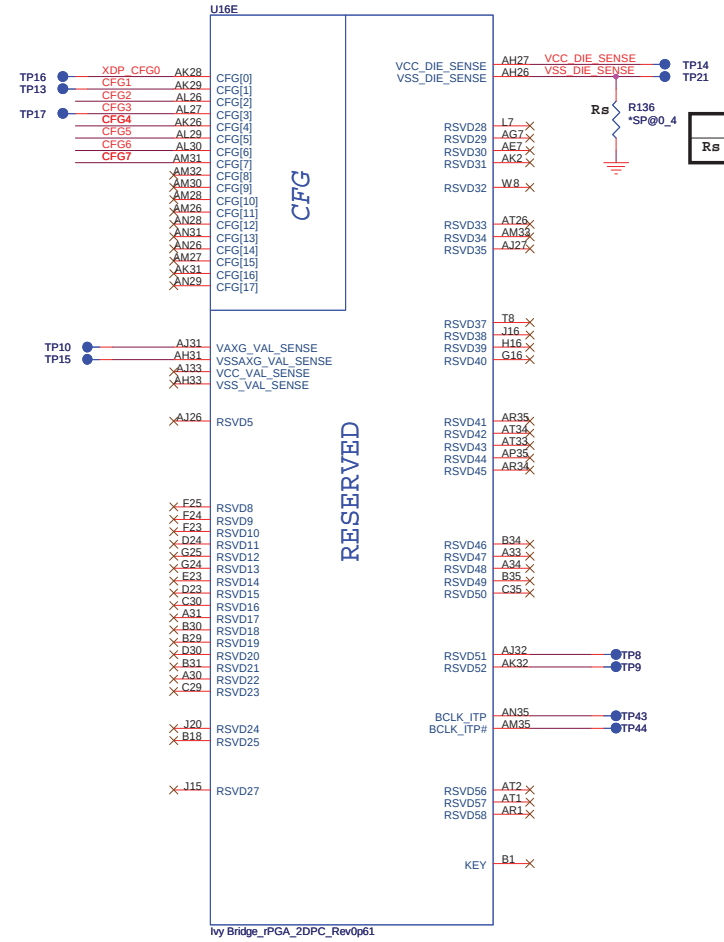
IVY Bridge Processor (GND)



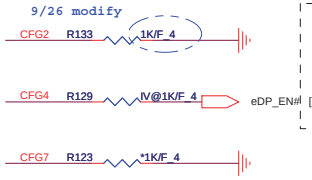
IVY Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	**Lane Reversed**
CFG4 (DP Presence Strap)	**Disable; No physical DP attached to eDP**	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	**PEG train immediately following xxRESETB de assertion**	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

CFG5 R130 *1K/F_4
CFG6 R127 *1K/F_4

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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[3,5,8,9,11,22,32,35,36,40,41] +1.05V
[3,8,9,10,11,15,28,30,31,34,35,36,41,42] +3V_S5

CPT/PPT (DMI,FDI,PM)

U20C

DMI: DMI0RXN, DMI1RXN, DMI2RXN, DMI3RXN, DMI0RXP, DMI1RXP, DMI2RXP, DMI3RXP, DMI0TXN, DMI1TXN, DMI2TXN, DMI3TXN, DMI0TXP, DMI1TXP, DMI2TXP, DMI3TXP, DMI_ZCOMP, DMI_IRCOMP, DMI2RBIAS

FDI: FDI_RXN0..7, FDI_RXP0..7, FDI_INT, FDI_FSYNC0, FDI_FSYNC1, FDI_LSYNC0, FDI_LSYNC1

System Power Management: DSWVRMEN, DPWROK, WAKE#, CLKRUN# / GPIO32, SUS_STAT# / GPIO61, SUSCLK / GPIO62, SLP_S5# / GPIO63, SLP_S4#, SLP_S3#, SLP_A#, SLP_SUS#, PMSYNCH, SLP_LAN# / GPIO29, SUSACK#, SYS_RESET#, SYS_PWROK, PWROK, APWROK, DRAMPWROK, RSMRST#, SUSWARN#/SUSPWRDNACK/GPIO30, PWRBTN#, ACPRESENT / GPIO31, BATLOW# / GPIO72, RI#

PANTHER POINT

CPT/PPT (LVDS,DDI)

U20D

LVDS: L_BKLTEN, L_VDD_EN, L_BKLTCTL, L_DDC_CLK, L_DDC_DATA, L_CTRL_CLK, L_CTRL_DATA, LVD_IBG, LVD_VBG, LVD_VREFH, LVD_VREFL, LVDSA_CLK#, LVDSA_CLK, LVDSA_DATA#0..3, LVDSA_DATA0..3, LVDSB_CLK#, LVDSB_CLK, LVDSB_DATA#0..3, LVDSB_DATA0..3

CRT: CRT_BLUE, CRT_GREEN, CRT_RED, CRT_DDC_CLK, CRT_DDC_DATA, CRT_HSYNC, CRT_VSYNC, DAC_IREF, CRT_IRTN

Digital Display Interface: SDVO_TVCLKINN/P, SDVO_STALLN/P, SDVO_INTN/P, SDVO_CTRLCLK, SDVO_CTRLDATA, DDPB_AUXN/P, DDPB_HPD, DDPB_0N/P..3N/P, DDPC_CTRLCLK, DDPC_CTRLDATA, DDPC_AUXN/P, DDPC_HPD, DDPC_0N/P..3N/P, DDPD_CTRLCLK, DDPD_CTRLDATA, DDPD_AUXN/P, DDPD_HPD, DDPD_0N/P..3N/P

PANTHER POINT

The required series-resistors are:
- Direct Connect - 33 Ω
- Docking Topology - 20 Ω

R place close to PCH

0 : Port not detected

INT. HDMI

PCH Pull-high/low(CLG)

CRB 1.0 change R8315 to 1K

wo S3 leakage, remove R

System PWR_OK(CLG)

IMVP_PWRGD PU +3V
PWROK_EC PD
so AND gate output dont need PD again

to PCH Pin12, XDP and EE debug

U24 TC7SH08FU

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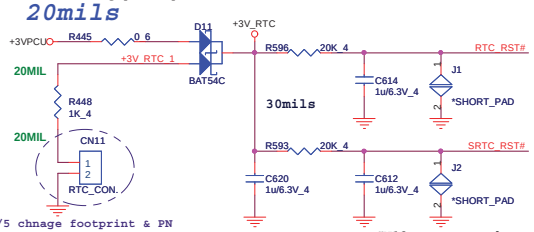
RTC Circuitry(RTC)

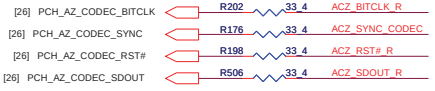
20mils



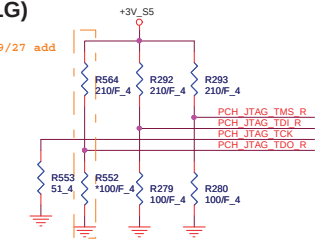
10/5 chnage footprint & PN

CN13 battery
DFWF02MS118 AHL03003022
AHL03003024

HDA Bus(CLG)

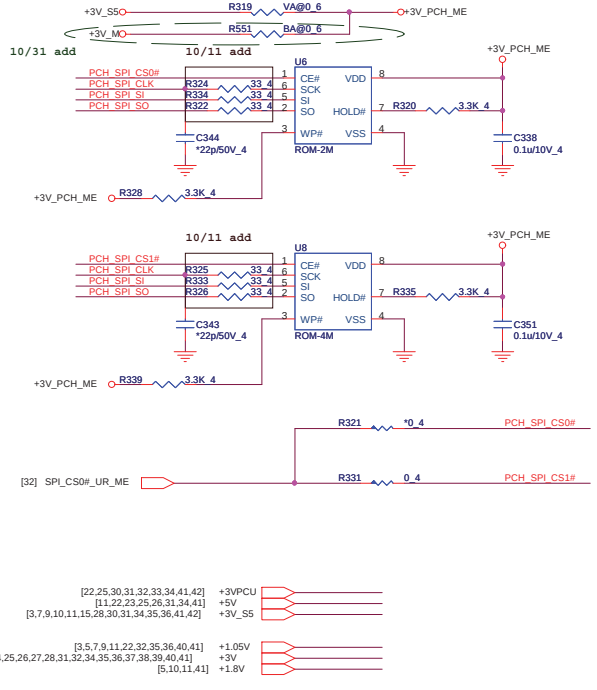


PCH JTAG Debug (CLG)



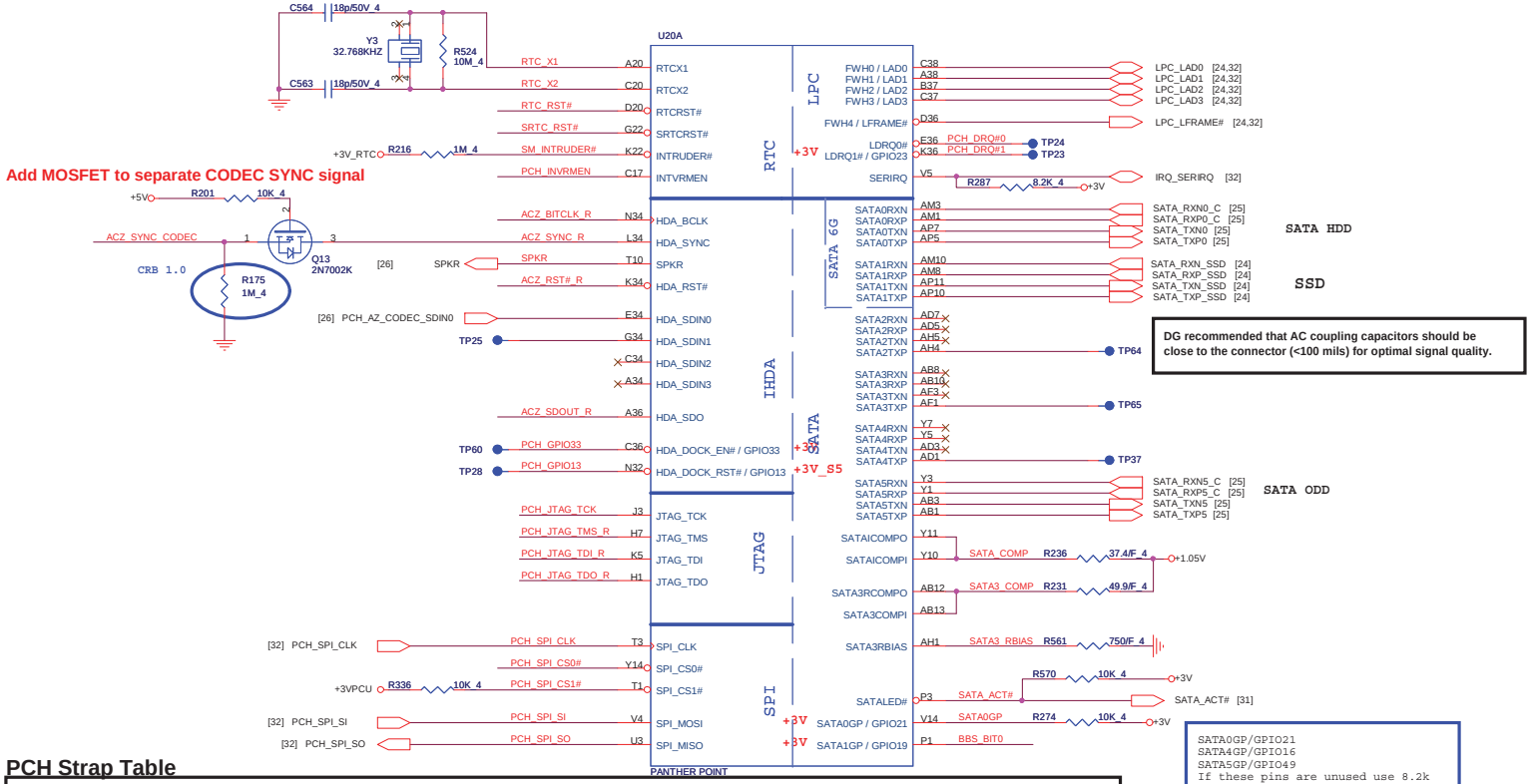
PCH Dual SPI (CLG) (Default for WIN8)

W25Q32BVSSIG / AKE391P0N00------>4MB
W25Q16BVSSIG / AKE38FP0N01------>2MB
for BA W25Q64BVSSIG / AKE3EFP0N00------>8MB



PCH2 (CLG)

CPT/PPT (HDA,JTAG,SATA)

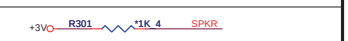


DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

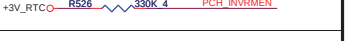
SATA0GP/GPIO21
SATA4GP/GPIO16
SATA5GP/GPIO49
If these pins are unused use 8.2k to 10k pull-up to +Vcc3_3 or 8.2k to 10k pull-down to ground

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	RSMRST	0 = effect (default)(weak pull-down 20K) 1 = overridden
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss (weak pull-down 20K) 1 = Set to Vcc
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD	RSMRST	0 = Disable (Default) 1 = Enable
DSWVREN	DEEP S4/S5 well On Die DSW VR Enable	DSW	High = Enable (Default) Low = Disable
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)



Used as GPIO only. at chklist 1.2

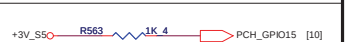


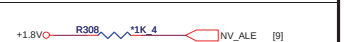
Default weak pull-up on GNT0/1#
[Need external pull-down for LPC BIOS]

ME_WR default EC setting folating

for future CPU, Sandy Bridge NC
DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhm ±5% - R8361 change to 0 or not??

Needs to be pulled High for Huron River platform. chklist 1.2





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CPT/PPT (PCI,USB,NVRAM)

CPT/PPT (PCI-E,SMBUS,CLK)

PLTRST#(CLG)

PCI/USBOC# Pull-up(CLG)

CLK_REQ/Strap Pin(CLG)

SMBus(EC)

SMBus(PCH)

	dGPU_PW_CTRL# (GPIO68) CTL : dGPU_VRON	SKU_ID1 (GPIO64)	SKU_ID0 (GPIO16)	VGA H/W Signal	Setup Menu	
UMA Only	1	0	0	UMA	Hidden	UMA boot
dGPU Only	0	0	1	GPU	Hidden	GPU boot
Switchable (Mux)				UMA+dGPU	dGPU/SG	UMA boot
Optimize (Muxless)	0	1	1	UMA	UMA/SG	UMA boot

dGPU_PW_CTRL#
1 = GPU power is control by H/W (pure Discrete SKU)
0 = GPU power is control by PCH GPIO (Discrete, SG or Optimize)
--->(Default)

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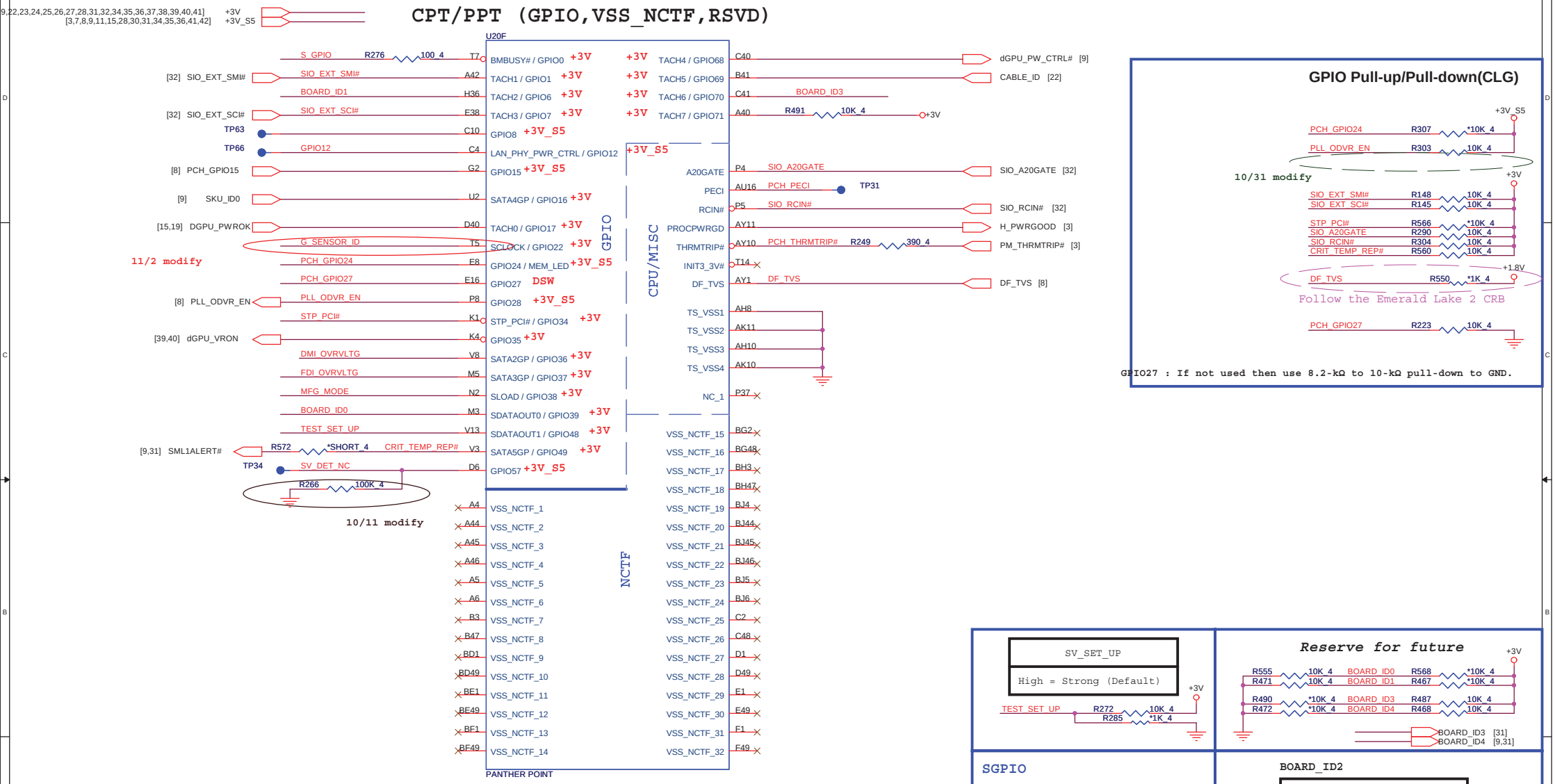
CPT/PPT (GPIO,VSS_NCTF,RSVD)



GPIO Pull-up/Pull-down(CLG)

GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

SATA2GP : strap for reserved at chklist 1.2
SATA3GP : strap for reserved at chklist 1.2
NOTE: The internal pull-down is disabled after PLTRST# deasserts.
NOTE: This signal should not be pulled high when strap is sampled.

SV_SET_UP
High = Strong (Default)

TEST_SET_UP R272 10K_4 R285 *1K_4 +3V

Reserve for future

R555 10K_4 BOARD_ID0 R568 *10K_4
R471 10K_4 BOARD_ID1 R467 *10K_4
R490 *10K_4 BOARD_ID3 R487 10K_4
R472 *10K_4 BOARD_ID4 R468 10K_4
BOARD_ID3 [31]
BOARD_ID4 [9,31]

SGPIO

S_GPIO R302 1K_4 R289 *1K_4 +3V

BOARD_ID2

8 Layer ------->High *
6 Layer ------->Low

R167 *10K_4 R172 10K_4 BOARD_ID2 [9]

R305 100K_4 FDI_OVRVLTG R291 *1K_4 +3V

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

DMI_OVRVLTG R286 *200K/F_4 +3V

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

G_SENSOR_ID R288 SP@10K_4 R275 SP@1K_4 +3V

BIOS RECOVERY	High = W/O G_SENSOR Low = W G_SENSOR

MFG-TEST

MFG_MODE R569 10K_4 R557 *1K_4 +3V

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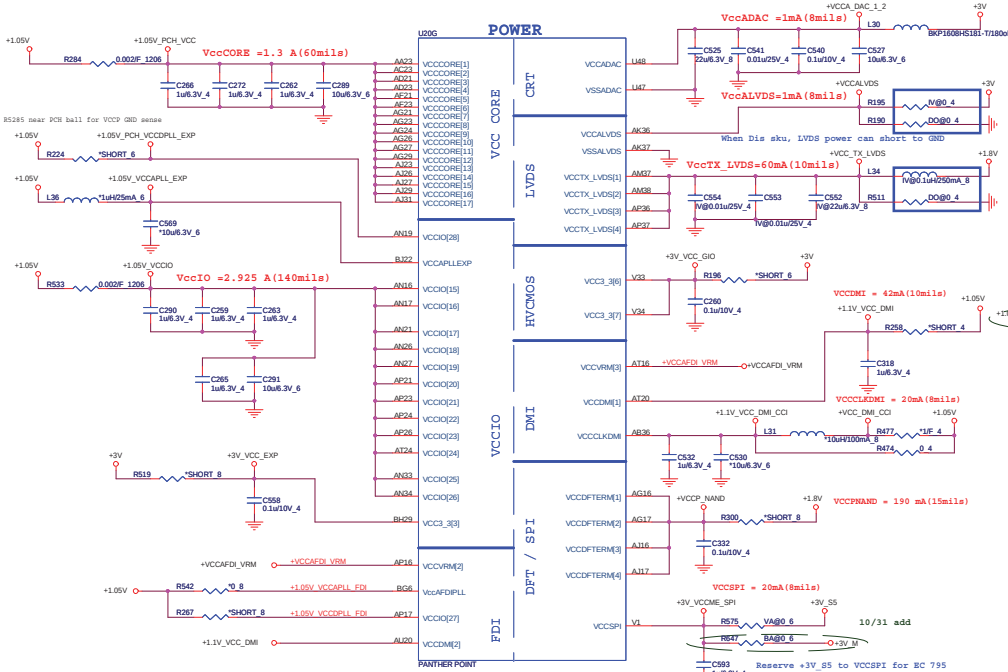
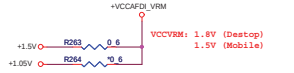
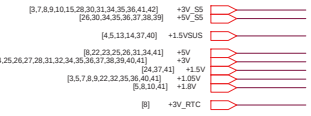
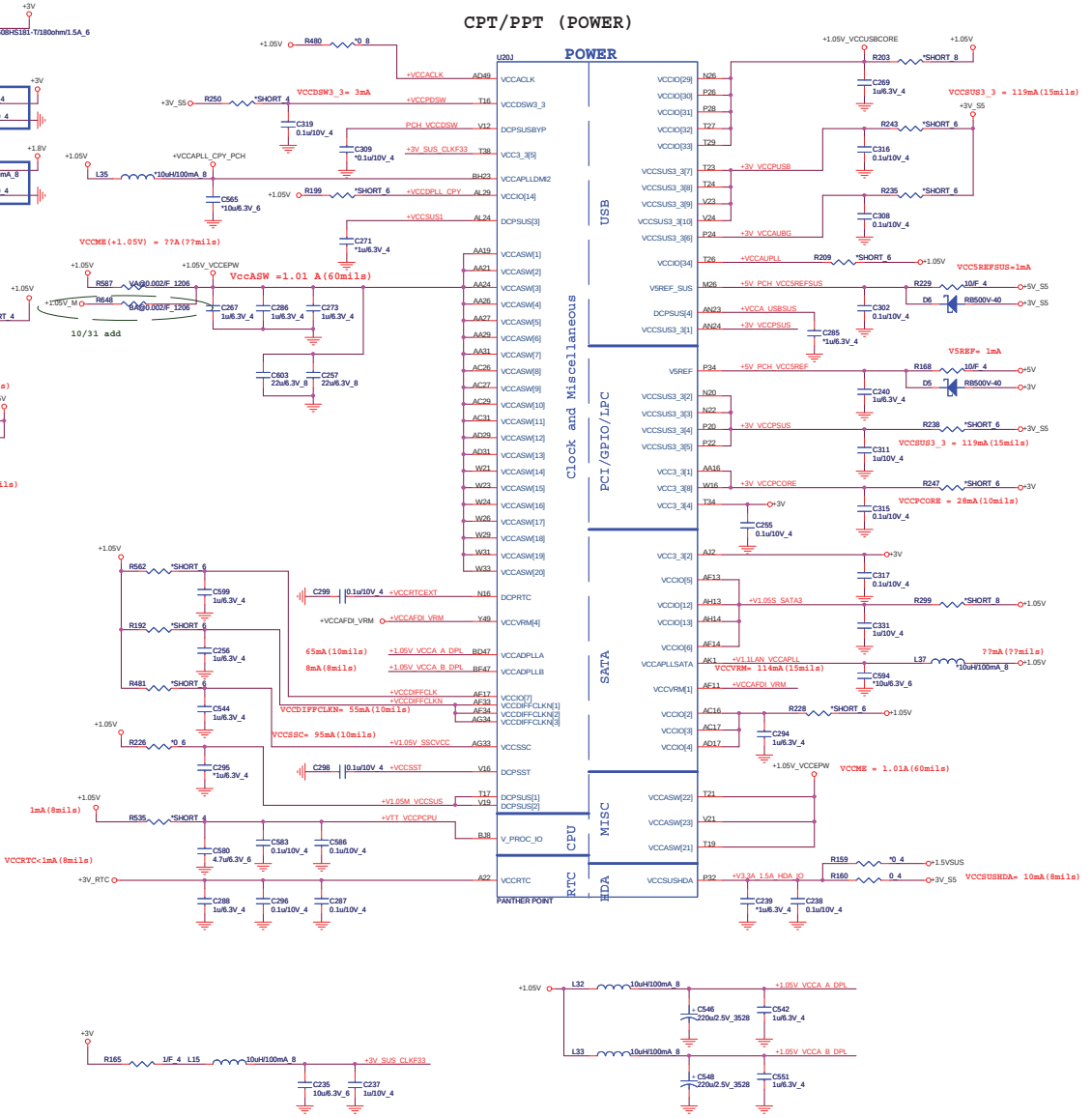
CPT/PPT (POWER)









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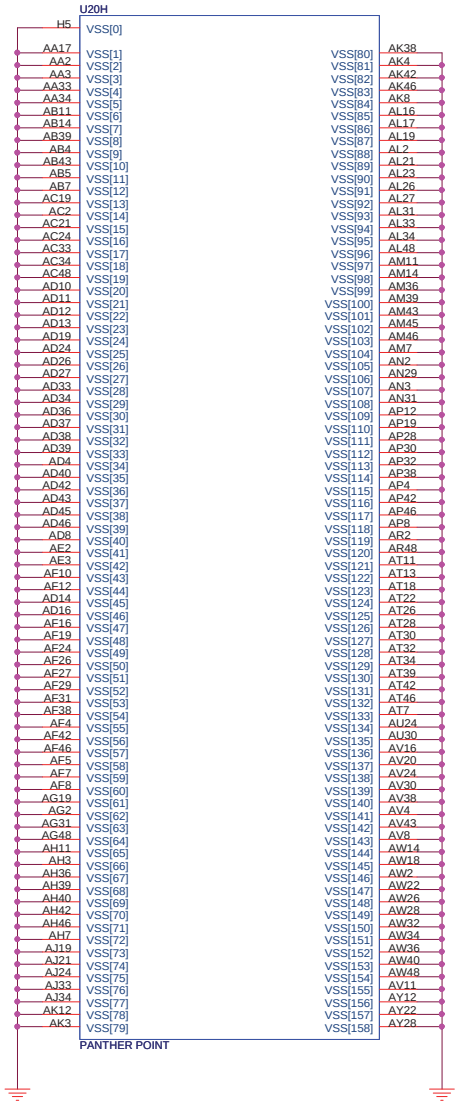
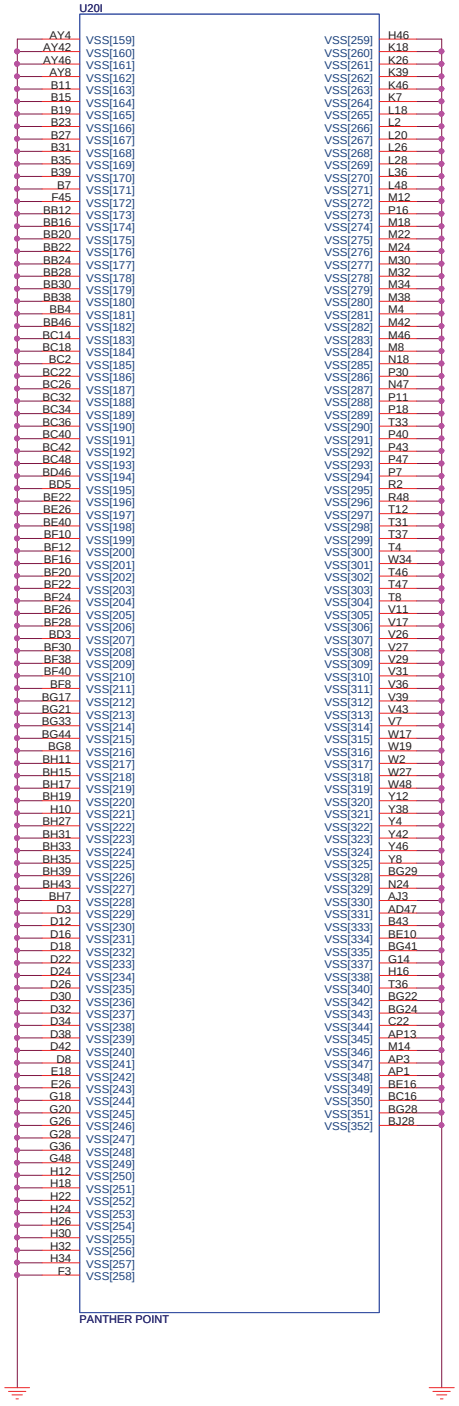
PCH6 (CLG)

IBEX PEAK-M (GND)





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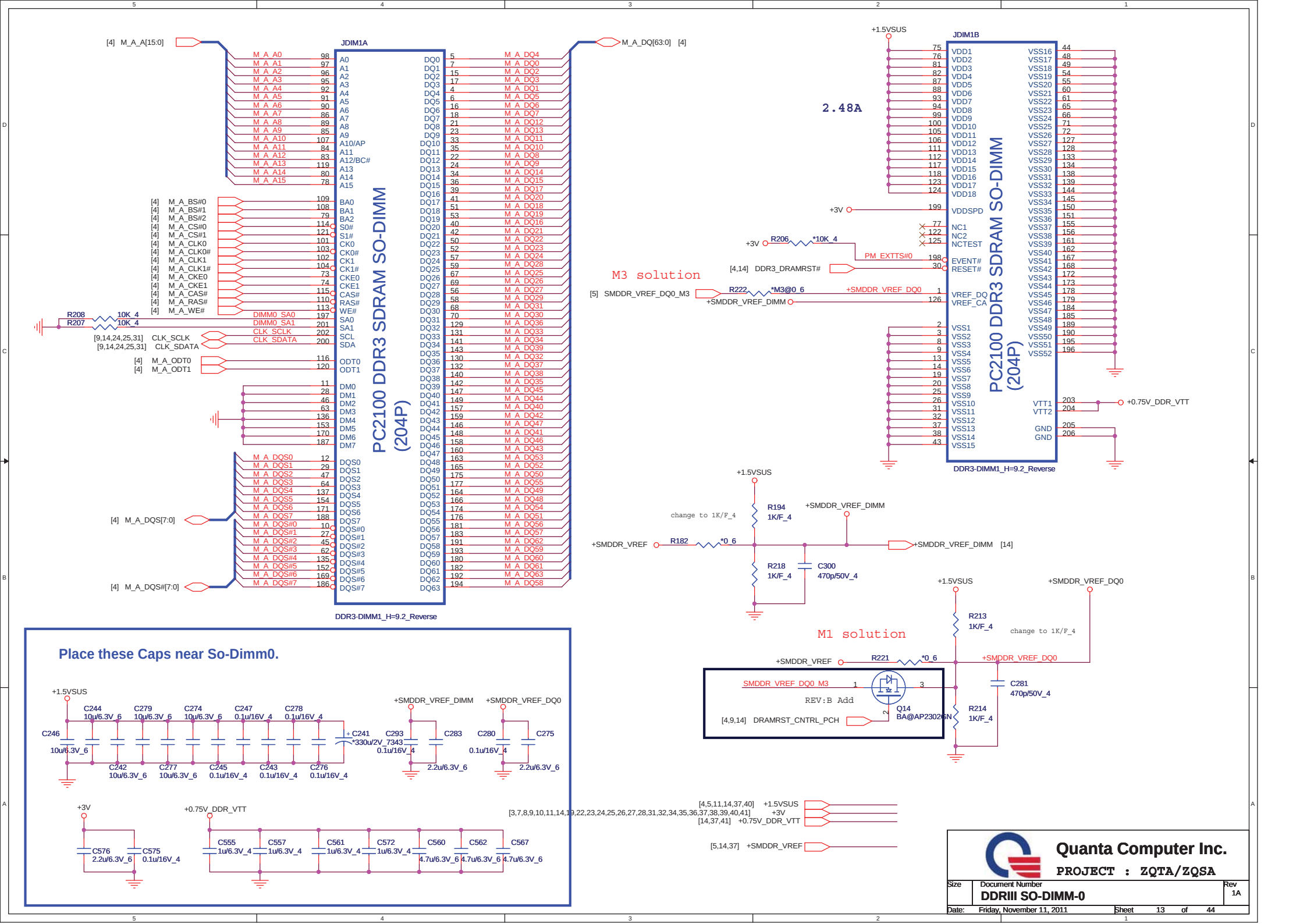
JDIM1A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=9.2_Reverse
JDIM1B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=9.2_Reverse
2.48A
M3 solution
M1 solution
change to 1K/F_4
REV:B Add
Place these Caps near So-Dimm0.
Quanta Computer Inc.
PROJECT : ZQTA/ZQSA
DDRIII SO-DIMM-0
Friday, November 11, 2011
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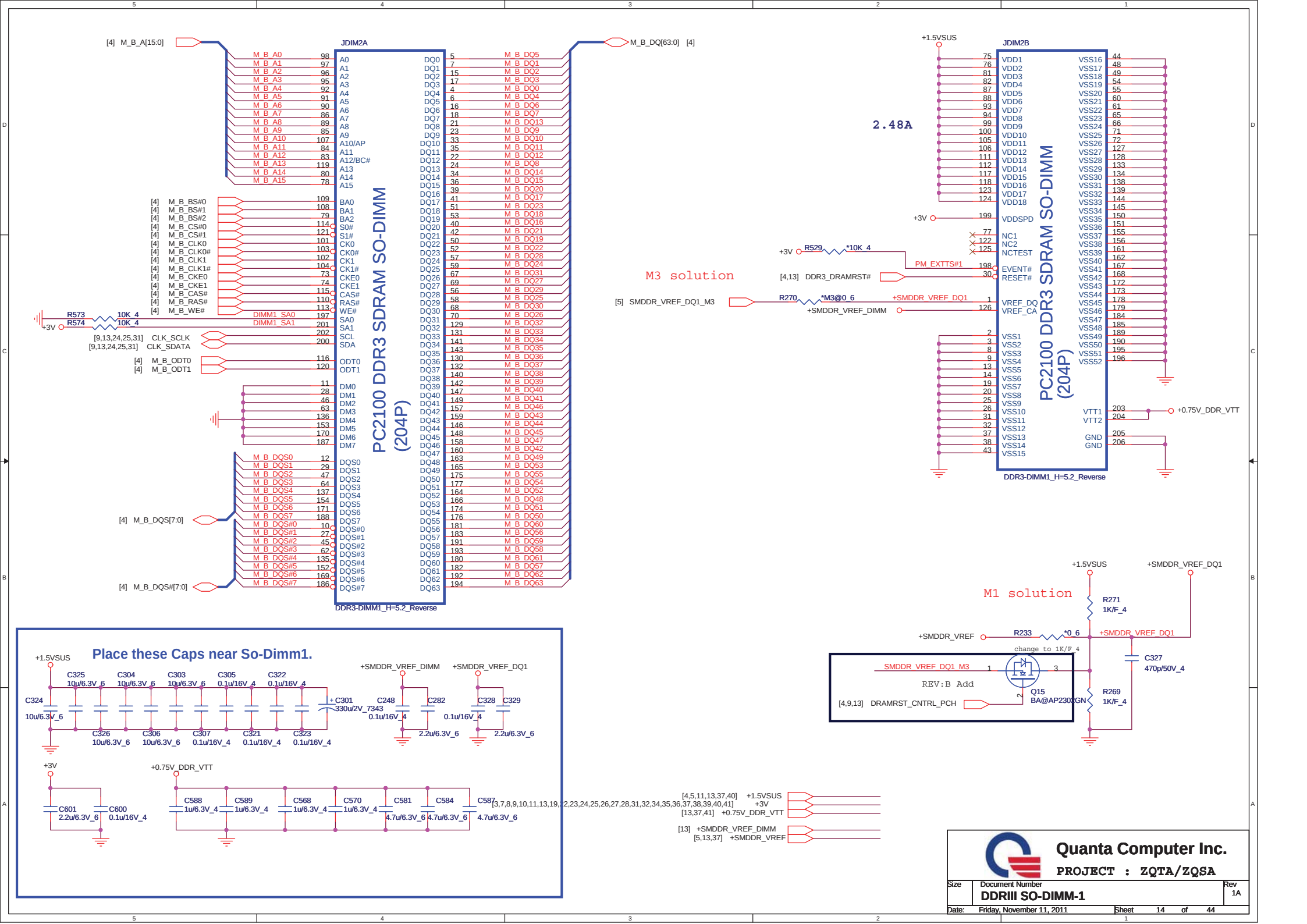
JDIM2A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=5.2_Reverse
JDIM2B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=5.2_Reverse
2.48A
M3 solution
M1 solution
Place these Caps near So-Dimm1.
Quanta Computer Inc.
PROJECT : ZQTA/ZQSA
DDRIII SO-DIMM-1
Friday, November 11, 2011

N13P-GL	AJ0N13P0T02
N13P-GS	AJ0N13P0T07
N13M-GS	AJ0N13M0T08

IV@:iGPU
EV@:dGPU
OP@:Optimus
DO@:Discrete only
SP@:Special

1000mA

+1.05V_GFX

To be placed no further from the GPU than bewteen the PS and GPU

C435	EV@22u/6.3V_8	
C441	EV@22u/6.3V_8	
C388	EV@10u/6.3V_6	
C392	EV@10u/6.3V_6	
C74	EV@4.7u/6.3V_6	PLACE UNDER BGA
C91	EV@1u/6.3V_4	PLACE NEAR BALLS
C98	EV@1u/6.3V_4	

+1.05V_GFX

To be placed no further from the GPU than bewteen the PS and GPU

C443	EV@22u/6.3V_8	
C432	EV@22u/6.3V_8	
C114	EV@10u/6.3V_6	
C109	EV@10u/6.3V_6	
C52	EV@4.7u/6.3V_6	PLACE UNDER BGA
C86	EV@1u/6.3V_4	PLACE NEAR BALLS
C78	EV@1u/6.3V_4	

2500mA

U15A

[PEG Interface]

AG19	PEX_IOVDD_1	PEX_RX0	AN12	PEG_TX15
AG21	PEX_IOVDD_2	PEX_RX0_N	AM12	PEG_TX#15
AG22	PEX_IOVDD_3	PEX_RX1	AN14	PEG_TX14
AG24	PEX_IOVDD_4	PEX_RX1_N	AM14	PEG_TX#14
AH21	PEX_IOVDD_5	PEX_RX2	AP14	PEG_TX13
AH25	PEX_IOVDD_6	PEX_RX2_N	AP15	PEG_TX#13
		PEX_RX3	AN15	PEG_TX12
AG13	PEX_IOVDDQ_1	PEX_RX3_N	AM15	PEG_TX#12
AG15	PEX_IOVDDQ_2	PEX_RX4	AN17	PEG_TX11
AG16	PEX_IOVDDQ_3	PEX_RX4_N	AM17	PEG_TX#11
AG18	PEX_IOVDDQ_4	PEX_RX5	AP17	PEG_TX10
AG25	PEX_IOVDDQ_5	PEX_RX5_N	AP18	PEG_TX#10
AH15	PEX_IOVDDQ_6	PEX_RX6	AN18	PEG_TX9
AH18	PEX_IOVDDQ_7	PEX_RX6_N	AM18	PEG_TX#9
AH26	PEX_IOVDDQ_8	PEX_RX7	AN20	PEG_TX8
AH27	PEX_IOVDDQ_9	PEX_RX7_N	AM20	PEG_TX#8
AJ27	PEX_IOVDDQ_10	PEX_RX8	AP20	PEG_TX7
AK27	PEX_IOVDDQ_11	PEX_RX8_N	AP21	PEG_TX#7
AL27	PEX_IOVDDQ_12	PEX_RX9	AN21	PEG_TX6
AM28	PEX_IOVDDQ_13	PEX_RX9_N	AM21	PEG_TX#6
AN28	PEX_IOVDDQ_14	PEX_RX10	AN23	PEG_TX5
		PEX_RX10_N	AM23	PEG_TX#5
		PEX_RX11	AP23	PEG_TX4
		PEX_RX11_N	AP24	PEG_TX#4
		PEX_RX12	AN24	PEG_TX3
		PEX_RX12_N	AM24	PEG_TX#3
		PEX_RX13	AN26	PEG_TX2
		PEX_RX13_N	AM26	PEG_TX#2
		PEX_RX14	AP26	PEG_TX1
		PEX_RX14_N	AP27	PEG_TX#1
		PEX_RX15	AN27	PEG_TX0
		PEX_RX15_N	AM27	PEG_TX#0

PEG_TX15 [3]	PEX_TX0	AK14	R_PEG_RX15	C133	EV@0.22u/6.3V_4
PEG_TX#15 [3]	PEX_TX0_N	AJ14	R_PEG_RX#15	C138	EV@0.22u/6.3V_4
PEG_TX14 [3]	PEX_TX1	AH14	R_PEG_RX14	C140	EV@0.22u/6.3V_4
PEG_TX#14 [3]	PEX_TX1_N	AG14	R_PEG_RX#14	C145	EV@0.22u/6.3V_4
PEG_TX13 [3]	PEX_TX2	AK15	R_PEG_RX13	C128	EV@0.22u/6.3V_4
PEG_TX#13 [3]	PEX_TX2_N	AJ15	R_PEG_RX#13	C130	EV@0.22u/6.3V_4
PEG_TX12 [3]	PEX_TX3	AL16	R_PEG_RX12	C120	EV@0.22u/6.3V_4
PEG_TX#12 [3]	PEX_TX3_N	AK16	R_PEG_RX#12	C123	EV@0.22u/6.3V_4
PEG_TX11 [3]	PEX_TX4	AK17	R_PEG_RX11	C112	EV@0.22u/6.3V_4
PEG_TX#11 [3]	PEX_TX4_N	AJ17	R_PEG_RX#11	C119	EV@0.22u/6.3V_4
PEG_TX10 [3]	PEX_TX5	AH17	R_PEG_RX10	C106	EV@0.22u/6.3V_4
PEG_TX#10 [3]	PEX_TX5_N	AG17	R_PEG_RX#10	C111	EV@0.22u/6.3V_4
PEG_TX9 [3]	PEX_TX6	AK18	R_PEG_RX9	C100	EV@0.22u/6.3V_4
PEG_TX#9 [3]	PEX_TX6_N	AJ18	R_PEG_RX#9	C105	EV@0.22u/6.3V_4
PEG_TX8 [3]	PEX_TX7	AL19	R_PEG_RX8	C99	EV@0.22u/6.3V_4
PEG_TX#8 [3]	PEX_TX7_N	AK19	R_PEG_RX#8	C95	EV@0.22u/6.3V_4
PEG_TX7 [3]	PEX_TX8	AK20	R_PEG_RX7	C93	EV@0.22u/6.3V_4
PEG_TX#7 [3]	PEX_TX8_N	AJ20	R_PEG_RX#7	C89	EV@0.22u/6.3V_4
PEG_TX6 [3]	PEX_TX9	AH20	R_PEG_RX6	C87	EV@0.22u/6.3V_4
PEG_TX#6 [3]	PEX_TX9_N	AG20	R_PEG_RX#6	C84	EV@0.22u/6.3V_4
PEG_TX5 [3]	PEX_TX10	AK21	R_PEG_RX5	C81	EV@0.22u/6.3V_4
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PEG_TX4 [3]	PEX_TX11	AL22	R_PEG_RX4	C76	EV@0.22u/6.3V_4
PEG_TX#4 [3]	PEX_TX11_N	AK22	R_PEG_RX#4	C71	EV@0.22u/6.3V_4
PEG_TX3 [3]	PEX_TX12	AK23	R_PEG_RX3	C64	EV@0.22u/6.3V_4
PEG_TX#3 [3]	PEX_TX12_N	AJ23	R_PEG_RX#3	C62	EV@0.22u/6.3V_4
PEG_TX2 [3]	PEX_TX13	AH23	R_PEG_RX2	C55	EV@0.22u/6.3V_4
PEG_TX#2 [3]	PEX_TX13_N	AG23	R_PEG_RX#2	C54	EV@0.22u/6.3V_4
PEG_TX1 [3]	PEX_TX14	AK24	R_PEG_RX1	C61	EV@0.22u/6.3V_4
PEG_TX#1 [3]	PEX_TX14_N	AJ24	R_PEG_RX#1	C59	EV@0.22u/6.3V_4
PEG_TX0 [3]	PEX_TX15	AL25	R_PEG_RX0	C57	EV@0.22u/6.3V_4
PEG_TX#0 [3]	PEX_TX15_N	AK25	R_PEG_RX#0	C56	EV@0.22u/6.3V_4

AC6	NC_1		
AJ28	NC_2		
AJ4	NC_3		
AJ5	NC_4		
AL11	NC_5		
C15	NC_6		
D19	NC_7		
D20	NC_8		
D23	NC_9		
D26	NC_10		
H31	NC_11		
T8	NC_12		
V32	NC_13		

PEX_REFCLK	AL13	CLK_PCIE_VGA		CLK_PCIE_VGA [9]	
PEX_REFCLK_N	AK13	CLK_PCIE_VGA#		CLK_PCIE_VGA# [9]	
PEX_TSTCLK_OUT	AJ26	PEX_TSTCLK	R53	*EV@200_4	
PEX_TSTCLK_OUT_N	AK26	PEX_TSTCLK#			
PEX_WAKE	AJ11			TP5	
PEX_RST_N	AJ12	PEGX_RST#			
PEX_CLKREQ_N	AK12	PEX_CLKREQ#	R390	EV@1K_4	+3V_GFX
PEX_TERMP	AP29	PEX_TERMP	R372	EV@2.49K/F_4	
TESTMODE	AK11	TESTMODE	R393	EV@10K/F_4	
PEX_PLLVDD	AG26	PEX_PLLVDD			
PEX_PLL_HVDD	AH12				
PEX_SVDD_3V3	AG12				
3.3V_AUX_NC	P8				
VDD_SENSE	L4				
GND_SENSE	L5				

10/11 change to 1k

+3V_GFX

J8	VDD33_1		
K8	VDD33_2		
L8	VDD33_3		
M8	VDD33_4		

+3V_GFX PLACE CLOSE TO BGA

C154	EV@4.7u/6.3V_6
C159	EV@1u/10V_6
C143	EV@0.1u/10V_4
C142	EV@0.1u/10V_4
C144	EV@0.1u/10V_4
C141	EV@0.1u/10V_4

PLACE CLOSE TO GPU BALLS

C47	EV@4.7u/6.3V_6	PLACE NEAR BGA CLOSE TO CAPS
C48	EV@1u/6.3V_4	PLACE UNDER BGA
C63	EV@0.1u/10V_4	PLACE NEAR BALLS

R46 GSS@0_6 +1.05V_GFX
L3 GL@160808-120

C124	EV@0.1u/10V_4	+3V_GFX
C459	EV@4.7u/6.3V_6	
C447	EV@4.7u/6.3V_6	

12~16 mils width PLACE NEAR BGA

EV@N13x

N13P

GPUVCC_SENSE [39]
GPUVSS_SENSE [39]

for N13P/M-GS	for N13P-GL
Stuff--> R	Reserve--> R
Reserve -->L	Stuff--> L

10/31 modify

[10,19] DGPU_PWROK — R649 *EV@10K/F_4 — R384 EV@10K/F_4 — +3V_GFX

R589 10K/F_4 — +3V_S5 — CLK_PEGA_REQ# [9]

Q39 EV@DTC144EUA

PEX_CLKREQ# — Q22 EV@PDTC143TT

10/11 chnage type

+3V_GFX 10/5 modify

C390 EV@0.1u/10V_4

[9,24,28,32] PLTRST#
[9] DGPU_HOLD_RST#
U14 EV@MC74VHC1G08DFT2G
PEGX_RST#
R374 EV@100K_4

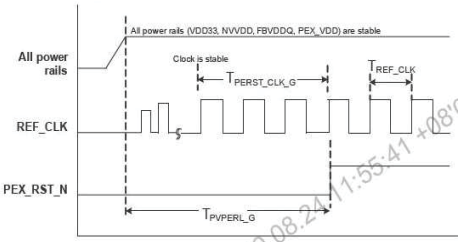
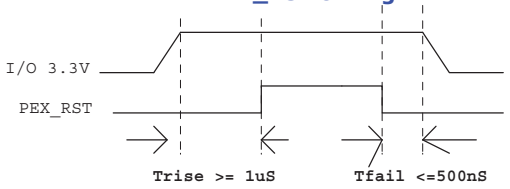


Figure 3-18. PEX_RST_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T_{PVPERL_G}	$T_{PVPERL\_G} \geq 1us$	
$T_{PERST\_CLK\_G}$	$T_{PERST\_CLK\_G} \geq 1T_{REF\_CLK}$	

PEX_RST timing



[16,17,19,40] +1.05V_GFX
[17,18,19,39,40] +3V_GFX
[3,7,8,9,10,11,28,30,31,34,35,36,41,42] +3V_S5
[3,7,8,9,10,11,13,14,19,22,23,24,25,26,27,28,31,32,34,35,36,37,38,39,40,41] +3V

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	DGPU 1/5 (PEG)	1A
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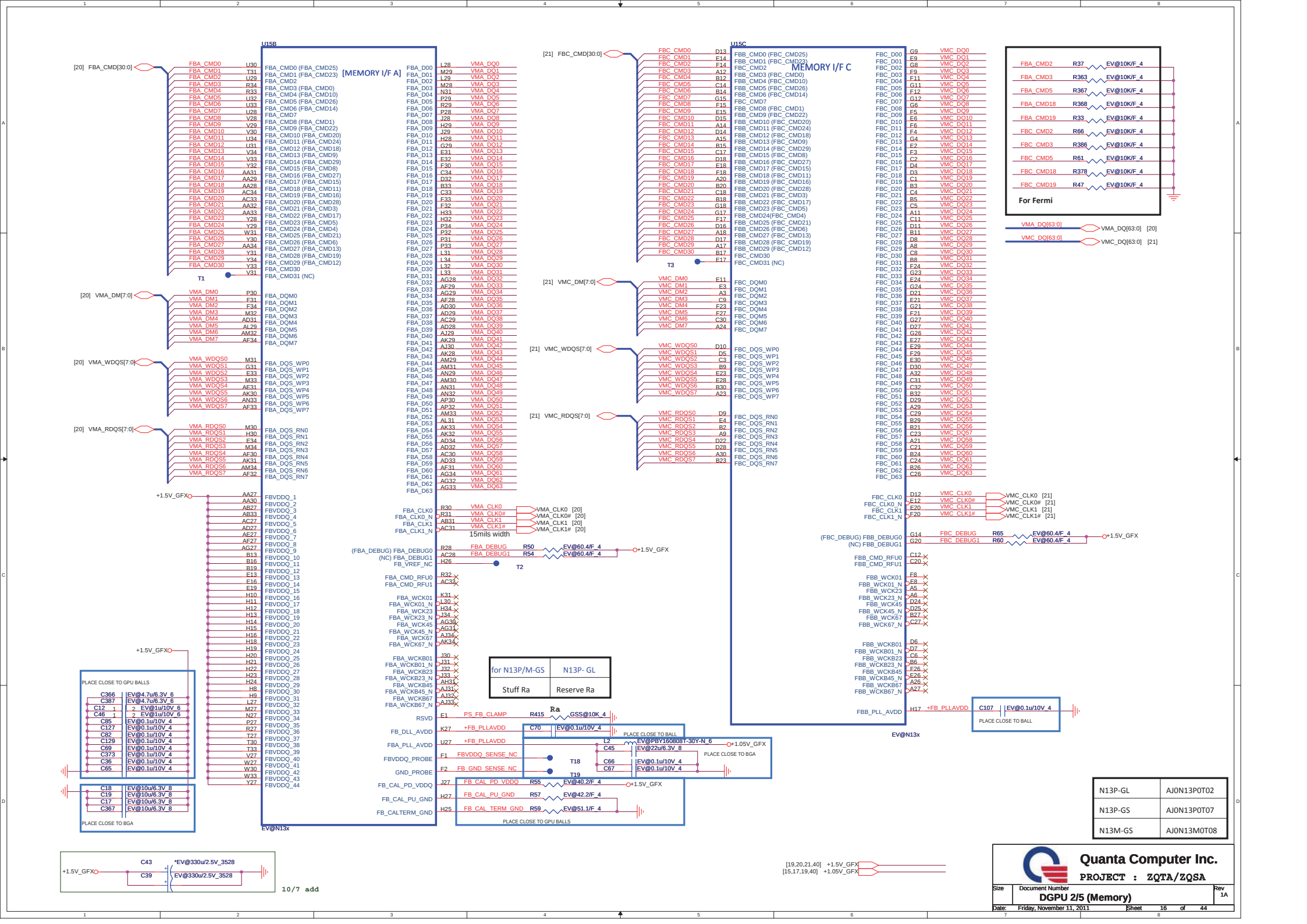
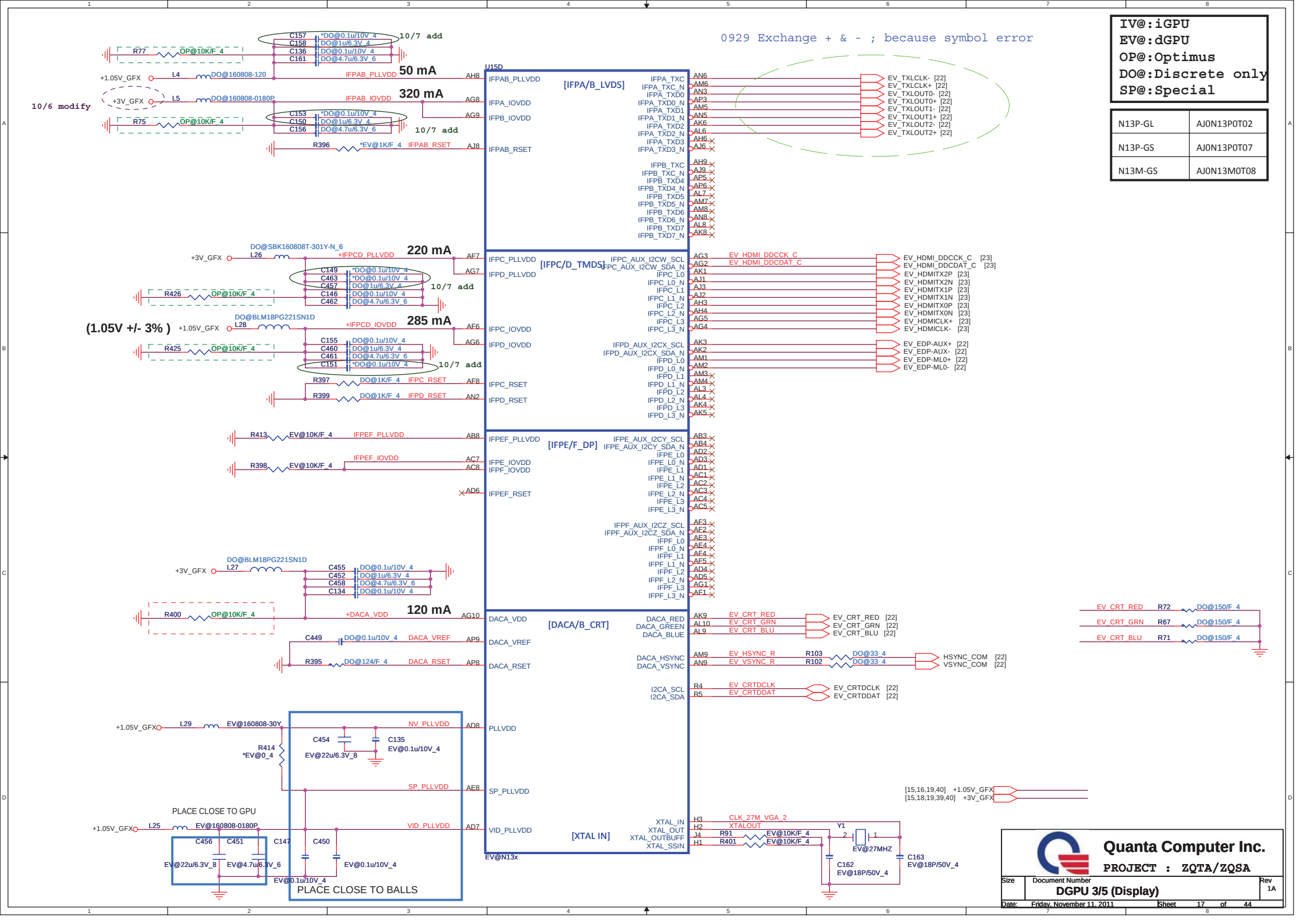


N13P-GL	AJ0N13P0T02
N13P-GS	AJ0N13P0T07
N13M-GS	AJ0N13M0T08



N13P-GL	AJ0N13P0T02
N13P-GS	AJ0N13P0T07
N13M-GS	AJ0N13M0T08

Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB_1	FB_0	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1110
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0010
STRAP4	RESERVED	PCI SPEED CHANGE GEN3	PCI_MAX SPEED	DP_PLL_VDD33	0011

N13P-GL	AJ0N13P0T02
N13P-GS	AJ001070T00
N13M-GS	AJ001170T00

[15,17,19,39,40] +3V_GFX

STRAP2
N13P-GL (1001) ---> 10k PU
N13P-GS (1011) ---> 20K PU

STRAP1
N13P-GL (0111) ---> 45.3k PD
N13P-GS (0110) ---> 34.8K PD

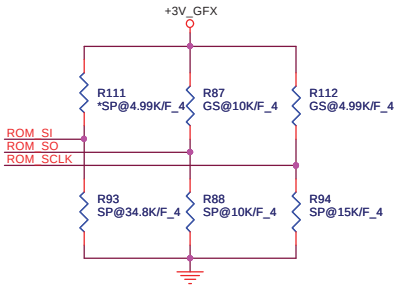
STRAP3
Optimus ---> 4.99k PD
Discrete only ---> 15K PD

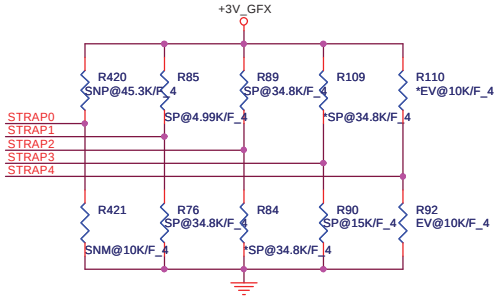
Resistor P/N
4.99K---> CS24992FB26
10K ---> CS31002FB26
15K ---> CS31502FB24
20K ---> CS32002FB29
34.8K---> CS33482FB22
45.3K ---> CS34532FB18

U15E

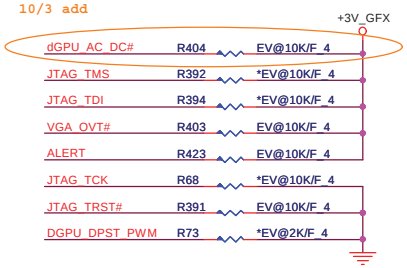
[MIOA]

[MIOB]



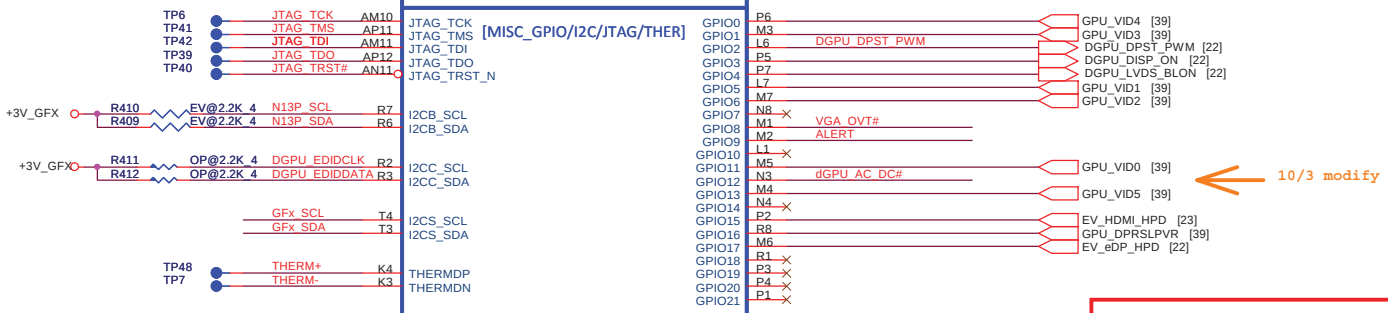


10/3 add



N13P-GS/-GL Straping table

ROM_SI	ROM_SO	ROM_SCLK
1G Hynix 64Mx16 -->15K PD	N13P-GL --> 10K PD	N13P-GL (0010) ---> 15k PD
1G Micron 64Mx16 -->20K PD	N13P-GS --> 10K PU	N13P-GS (1000) ---> 4.99K PU
2G Hynix 128Mx16 -->35K PD (Default)		
2G Micron 128Mx16 -->45K PD		



10/3 modify

N13M-GS Straping table

Pin Name	Strap Mapping	Value
ROM_SCLK	SMB_ALT_ADDR	0
ROM_SI	SUB_VENDOR	0
ROM_SO	VGA_DEVICE	0
STRAP[3..0]	RAM_CFG[3..0]	0010(Hynix 64Mx16) 0110(Hynix 128Mx16)
STRAP[4]	PCIE_MAX_SPEED	0

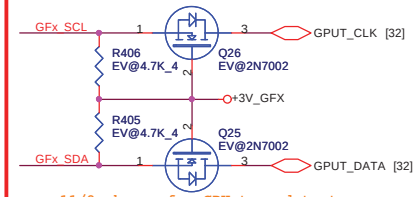
Remark :
0 -> 10K PD
1 -> 10K PU

[22] DGPU_EDIDCLK
[22] DGPU_EDIDDATA
DGPU_EDIDCLK
DGPU_EDIDDATA

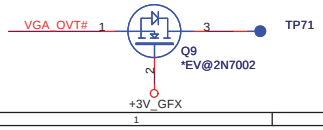
R422	
N13P-GS/GL	40.2K
N13M-GS	NC

for N13P/M-GS	for N13P- GL
Reserve R108	Stuff R108

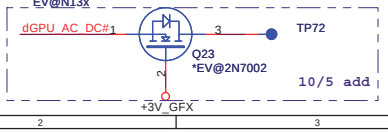
GFx SMBus Isolation **

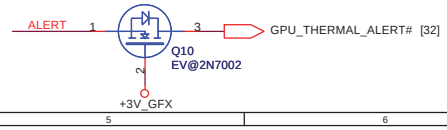


11/8 change for GPU temp detect



EV@N13x





Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	DGPU 4/5 (MIO/GPIO)	1A

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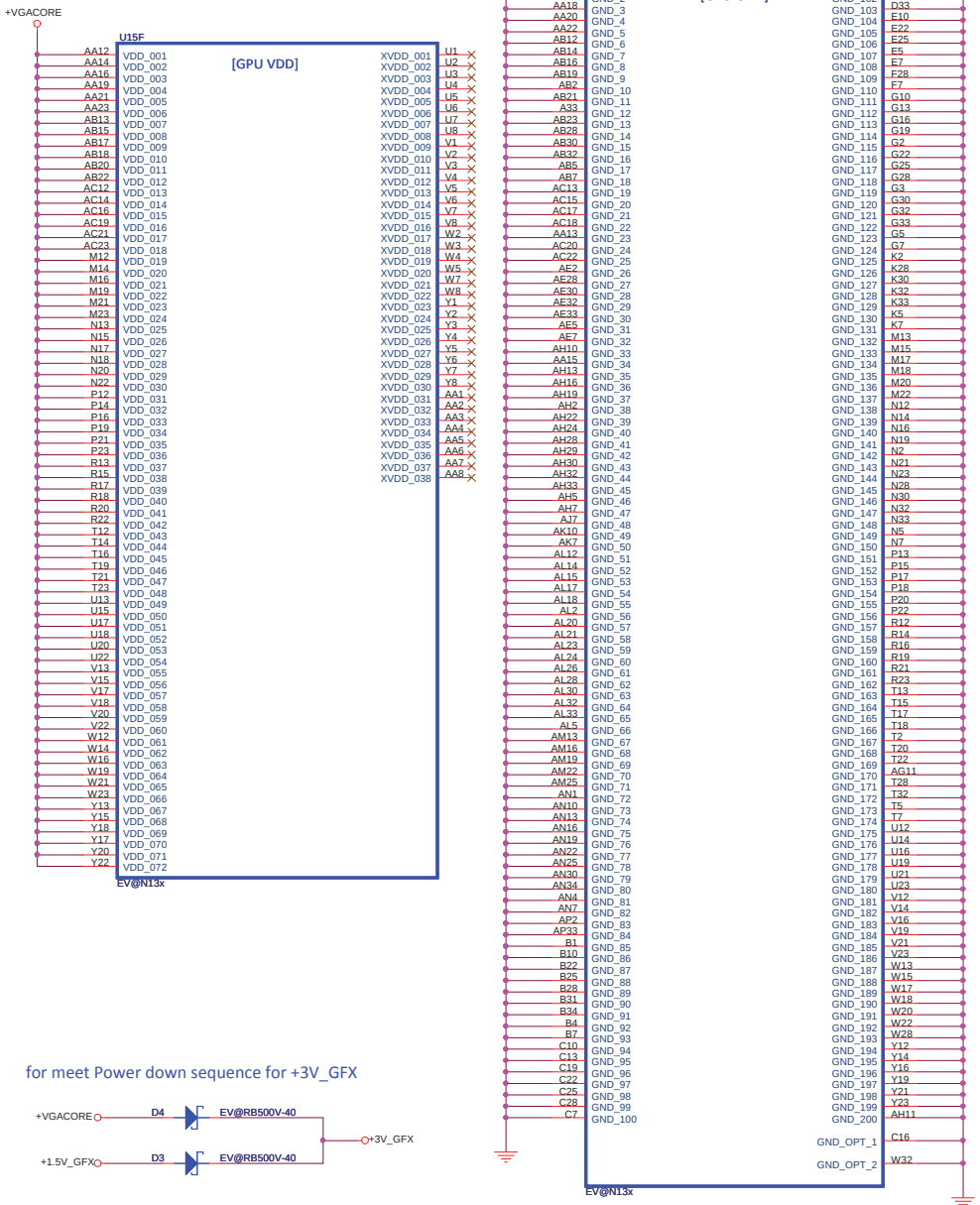
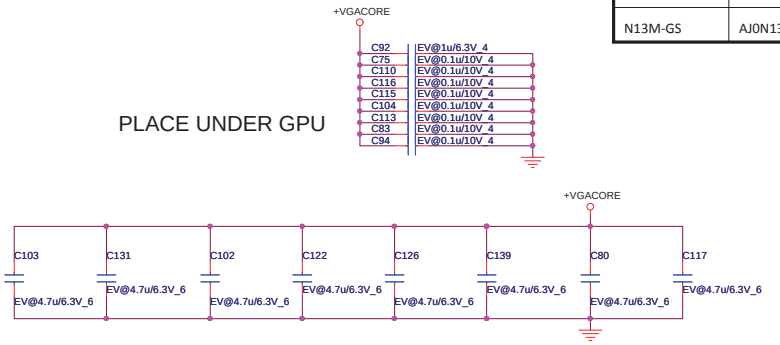
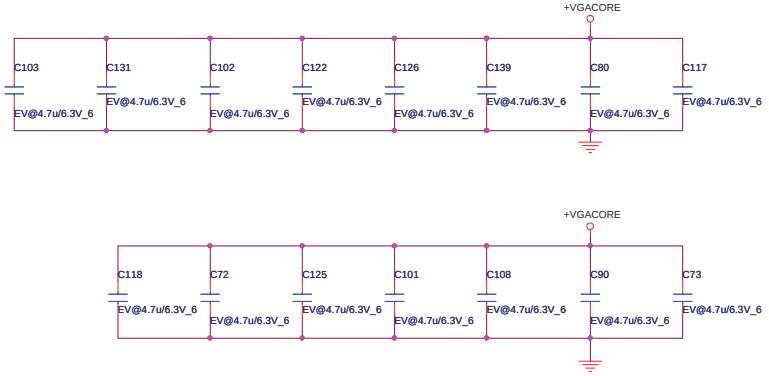
N13P-GL	AJ0N13P0T02
N13P-GS	AJ0N13P0T07
N13M-GS	AJ0N13M0T08

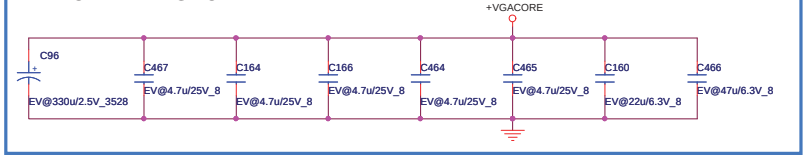


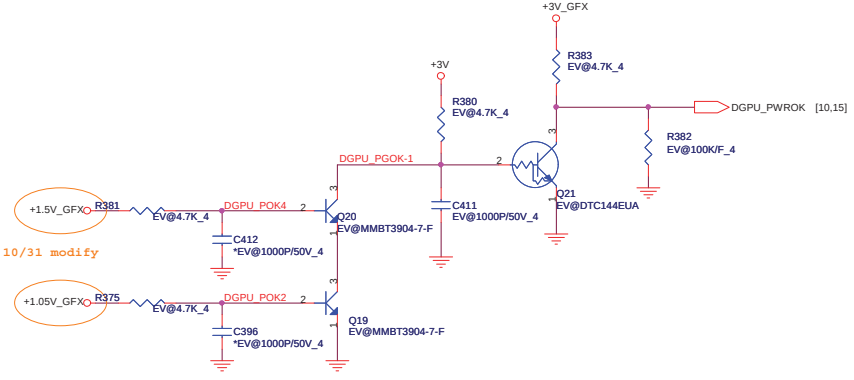
PLACE UNDER GPU



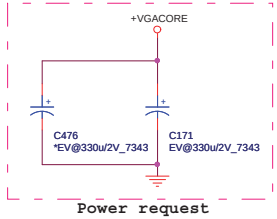


PLACE NEAR GPU





for meet Power down sequence for +3V_GFX



Power request

ESR

9/27 add

[31,39] +VGACORE
[15,16,17,40] +1.05V_GFX
[16,20,21,40] +1.5V_GFX
[15,17,18,39,40] +3V_GFX
[3,7,8,9,10,11,13,14,22,23,24,25,26,27,28,31,32,34,35,36,37,38,39,40,41] +3V

Quanta Computer Inc.

PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	DGPU 5/5 (Power/Ground)	1A

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HYNIX 900MHz 1G AKD5LZWTW02
HYNIX 900MHz 2G AKD5MGWTW00

CHANNEL A: 256MB/512MB DDR3

[16] VMA_DQ[63..0]
[16] VMA_DM[7..0]
[16] VMA_WDQS[7..0]
[16] VMA_RDQS[7..0]

VRAM2 / VRAM5 / VRAM1 / VRAM6

10/12 SWAP Pin

Should be 240 Ohms +-1%

R43 EV@243/F_4
R364 EV@243/F_4
R34 EV@243/F_4
R373 EV@243/F_4

96-BALL SDRAM DDR3
EV@VRAM_DDR3

+1.5V_GFX

R371 EV@162/F_4 (VMA_CLK0 / VMA_CLK0#)

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R366 EV@1.33K/F_4 — VREFC_VMA1 — R365 EV@1.33K/F_4 — C376 EV@0.1u/10V_4
R39 EV@1.33K/F_4 — VREFD_VMA1 — R38 EV@1.33K/F_4 — C34 EV@0.1u/10V_4

[16] FBA_CMD17 — FBA_CMD17 — TP1
[16] FBA_CMD1 — FBA_CMD1 — TP2
10/14 modify

R41 EV@162/F_4 (VMA_CLK1 / VMA_CLK1#)

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R36 EV@1.33K/F_4 — VREFC_VMA3 — R35 EV@1.33K/F_4 — C24 EV@0.1u/10V_4
R370 EV@1.33K/F_4 — VREFD_VMA3 — R369 EV@1.33K/F_4 — C380 EV@0.1u/10V_4

C30 C27 C374 C25 EV@1u/10V_4
C369 C379 C382 C23 C29 C32 EV@10u/6.3V_8 / EV@1u/10V_4
C416 C26 C375 C28 C37 C33 C31 C371 EV@10u/6.3V_8 / EV@1u/10V_4
C386 C368 EV@10u/6.3V_8
C381 C35 C377 C378 C370 EV@0.1u/10V_4
C44 C88 EV@10u/6.3V_8
C372 C385 C383 EV@0.1u/10V_4

[16,19,21,40] +1.5V_GFX

Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	DGPU Memory 1/2 (DDR3)	1A
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HYNIX 900MHz 1G AKD5LZWTW02
HYNIX 900MHz 2G AKD5MGWTW00

[16] VMC_DQ[63..0]
[16] VMC_DM[7..0]
[16] VMC_WDQS[7..0]
[16] VMC_RDQS[7..0]

CHANNEL B: 256MB/512MB DDR3

VRAM8 / VRAM4 / VRAM3 / VRAM7

10/12 SWAP Pin

+1.5V_GFX

Should be 240 Ohms +-1%

R385 SNP@243/F_4 (VRAM8)
R64 SNP@243/F_4 (VRAM4)
R52 SNP@243/F_4 (VRAM3)
R379 SNP@243/F_4 (VRAM7)

96-BALL SDRAM DDR3
SNP@VRAM _DDR3

R388 SNP@162/F_4 (VMC_CLK0 / VMC_CLK0#)

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R62 SNP@1.33K/F_4, R63 SNP@1.33K/F_4, C121 SNP@0.1u/10V_4 (VREFC_VMC1)
R74 SNP@1.33K/F_4, R70 SNP@1.33K/F_4, C148 SNP@0.1u/10V_4 (VREFD_VMC1)

R49 SNP@162/F_4 (VMC_CLK1 / VMC_CLK1#)

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R56 SNP@1.33K/F_4, R58 SNP@1.33K/F_4, C79 SNP@0.1u/10V_4 (VREFC_VMC3)
R376 SNP@1.33K/F_4, R377 SNP@1.33K/F_4, C403 SNP@0.1u/10V_4 (VREFD_VMC3)

[16,19,20,40] +1.5V_GFX

C137 C384 C68 C423 SNP@1u/10V_4
C152 SNP@10u/6.3V_8, C448 SNP@10u/6.3V_8, C446 SNP@1u/10V_4, C394 C58 C429 SNP@1u/10V_4
C21 C445 C132 C393 C397 C399 C442 C50 SNP@0.1u/10V_4
C53 C410 C51 C22 C97 C426 C391 C389 SNP@1u/10V_4

[16] FBC_CMD17 — FBC_CMD17 — TP3
[16] FBC_CMD1 — FBC_CMD1 — TP4

Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	DGPU Memory 2/2 (DDR3)	1A
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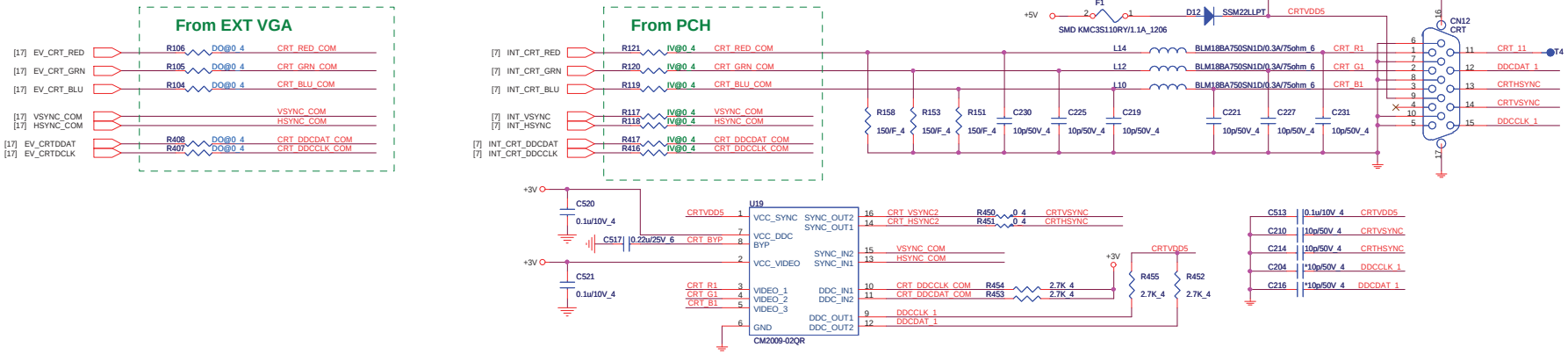
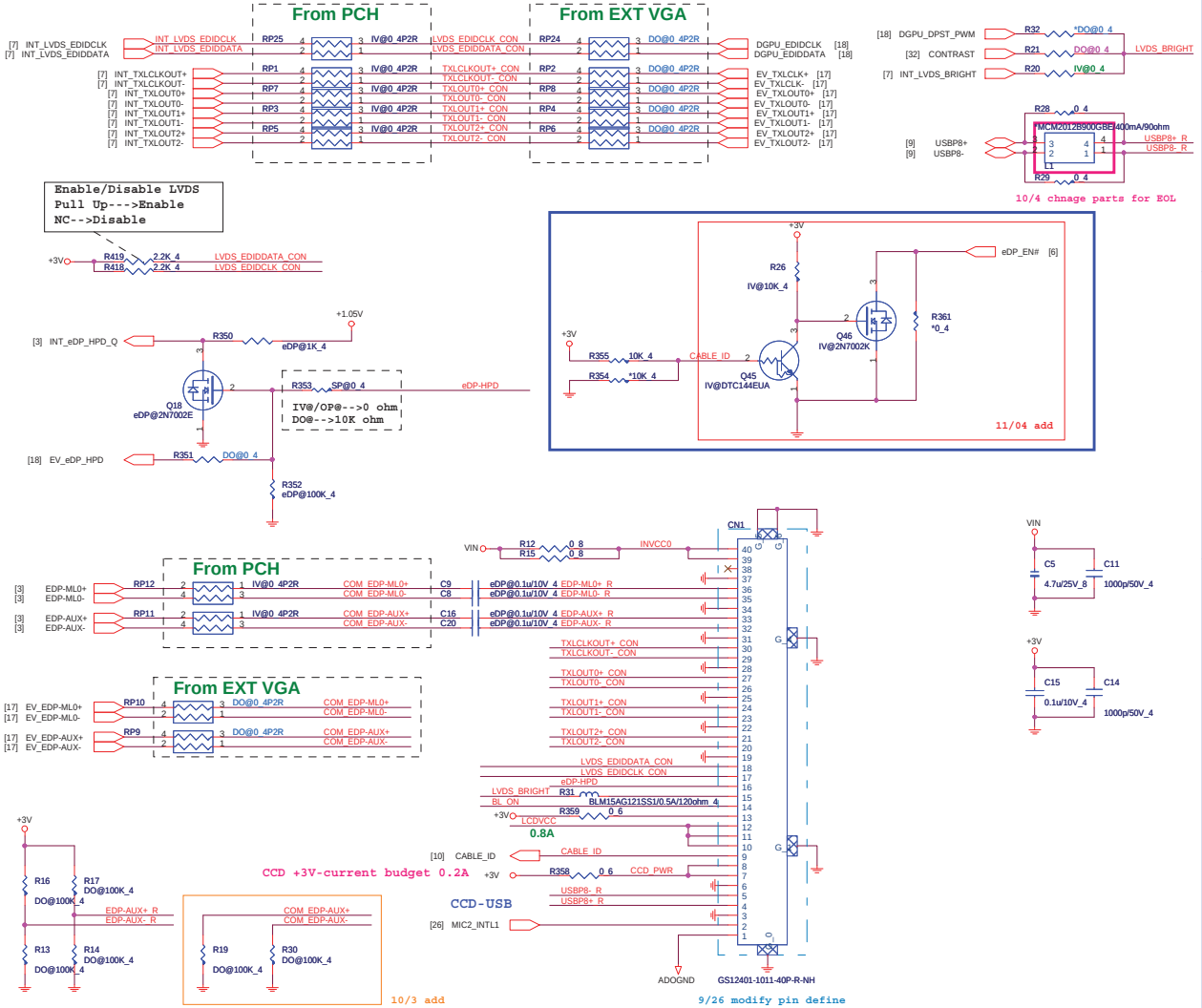
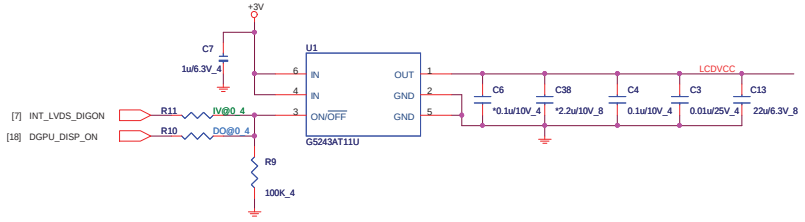
CRT



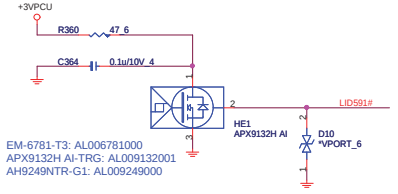
LVDS & eDP



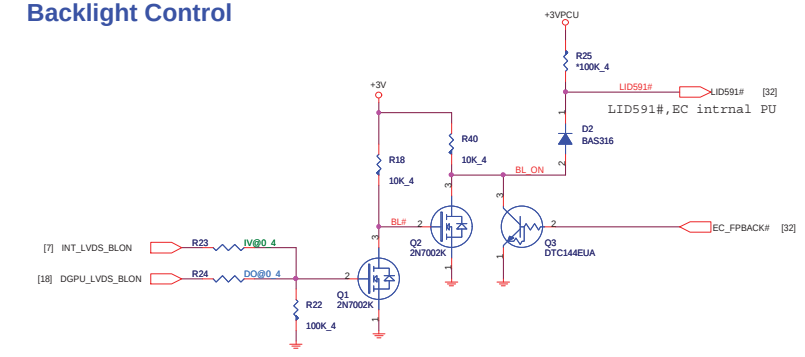
LCD Power



Lid Switch (Hall sensor)



Backlight Control



Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	1A
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HDMI

From PCH

[7] INT_HDMITX2N — C270 0.1u/10V_4 — INT_HDMITX2N_C
[7] INT_HDMITX2P — C284 0.1u/10V_4 — INT_HDMITX2P_C
[7] INT_HDMITX1N — C258 0.1u/10V_4 — INT_HDMITX1N_C
[7] INT_HDMITX1P — C261 0.1u/10V_4 — INT_HDMITX1P_C
[7] INT_HDMITX0N — C264 0.1u/10V_4 — INT_HDMITX0N_C
[7] INT_HDMITX0P — C268 0.1u/10V_4 — INT_HDMITX0P_C
[7] INT_HDMICLK+ — C254 0.1u/10V_4 — INT_HDMICLK+_C
[7] INT_HDMICLK- — C251 0.1u/10V_4 — INT_HDMICLK-_C

DO@--->499 ohm
P/N:CS14992FB24
IV@/OP@--->680 ohm
P/N:CS16802JB27

R512 SP@680_4 R515 SP@680_4 R522 SP@680_4 R520 SP@680_4 R518 SP@680_4 R516 SP@680_4 R525 SP@680_4 R523 SP@680_4

+5V — R517 *100K/F_4 — Q38 2N7002E

From EXT VGA

[17] EV_HDMITX2N — RP14 — DO@0_4P2R — INT_HDMITX2N
[17] EV_HDMITX2P — INT_HDMITX2P
[17] EV_HDMITX1N — RP15 — DO@0_4P2R — INT_HDMITX1N
[17] EV_HDMITX1P — INT_HDMITX1P
[17] EV_HDMITX0N — RP16 — DO@0_4P2R — INT_HDMITX0N
[17] EV_HDMITX0P — INT_HDMITX0P
[17] EV_HDMICLK- — RP17 — DO@0_4P2R — INT_HDMICLK-
[17] EV_HDMICLK+ — INT_HDMICLK+

IV@:iGPU
EV@:dGPU
OP@:Optimus
DO@:Discrete only
SP@:Special

HDMI connector

CN13 HDMI CONN

INT_HDMITX2P_C — D2+
INT_HDMITX2N_C — D2 Shield
INT_HDMITX1P_C — D2-
INT_HDMITX1N_C — D1+
INT_HDMITX0P_C — D1 Shield
INT_HDMITX0N_C — D1-
INT_HDMICLK+_C — D0+
D0 Shield
INT_HDMICLK-_C — D0-
CK+
CK Shield
CK-
CE Remote
NC
HDMI_DDCCLK_MB — DDC CLK
HDMI_DDCDATA_MB — DDC DATA
GND
+5V
HP DET
SHELL1 SHELL2

+5V — SMD KMC3S110RY/1.1A_1206 F2 — HDMI_5V_R — D19 SSM22LLPT — HDMI_5V
C545 470p/50V_4
HDMI_MB_HP — R178 0_4 — HP_DET_CN
R179 100K_4

9/22 change parts

HDMI-detect

+3V — R174 10K_4
+3V — R181 10K_4
R185 IV@0_4 — HDMI_HP [7]
R189 DO@0_4 — EV_HDMI_HPD [18]
[32] HDMI_HPD_EC#
+5V — R180 *10K_4 — HDMI_MB_HP
Q12 2N7002E
Q11 2N7002E

I2C

UMA	R239 R245	CS22202JB18
DIS	R239 R245	CS24702JB38

From EXT VGA

[17] EV_HDMI_DDCCK_C — R493 DO@0_4 — HDMI_DDCCLK_COM
[17] EV_HDMI_DDCDAT_C — R508 DO@0_4 — HDMI_DDCDATA_COM

From PCH

[7] HDMI_DDCCLK_SW — R501 IV@0_4 — HDMI_DDCCLK_COM
[7] HDMI_DDCDATA_SW — R504 IV@0_4 — HDMI_DDCDATA_COM

+5V — D20 RB501V-40 — R494 2.2K_4 — HDMI_DDCCLK_MB
+3V — R489 SP@2.2K_4 — Q35 BSN20
+5V — D21 RB501V-40 — R509 2.2K_4 — HDMI_DDCDATA_MB
+3V — R510 SP@2.2K_4 — Q37 BSN20

EMI

INT_HDMITX2P_C — R212 *100/F_4 — INT_HDMITX2N_C
INT_HDMITX1P_C — R200 *100/F_4 — INT_HDMITX1N_C
INT_HDMITX0P_C — R204 *100/F_4 — INT_HDMITX0N_C
INT_HDMICLK+_C — R193 *100/F_4 — INT_HDMICLK-_C

[3,7,8,9,10,11,13,14,19,22,24,25,26,27,28,31,32,34,35,36,37,38,39,40,41] +3V
[8,11,22,25,26,31,34,41] +5V

Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	HDMI (PS8101)	1A

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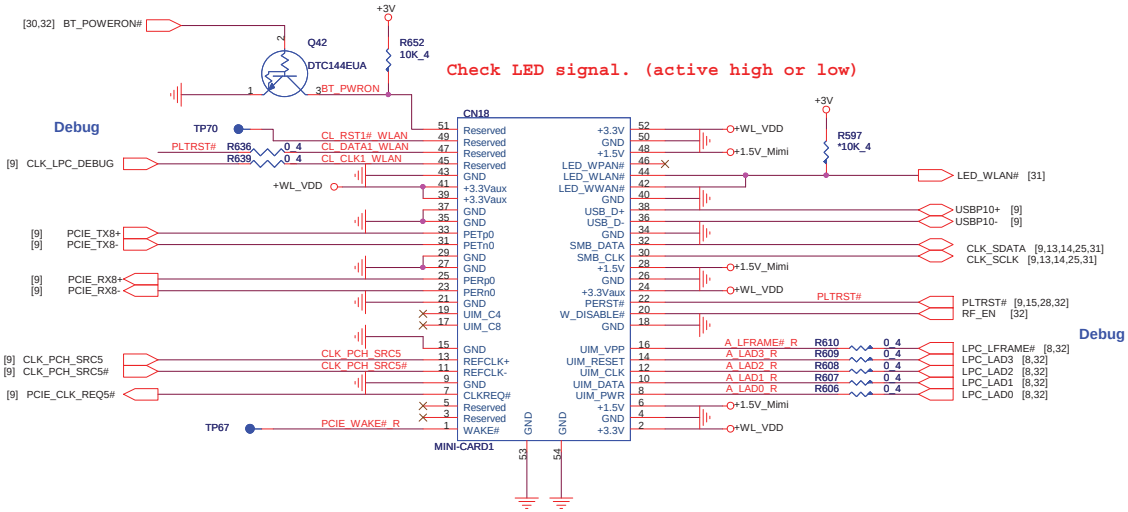
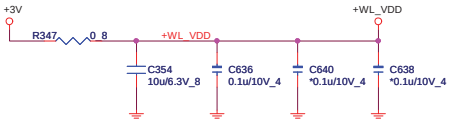
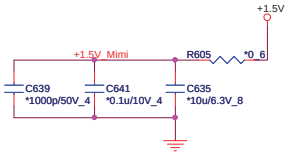
MINI-CARD WLAN(MPC)

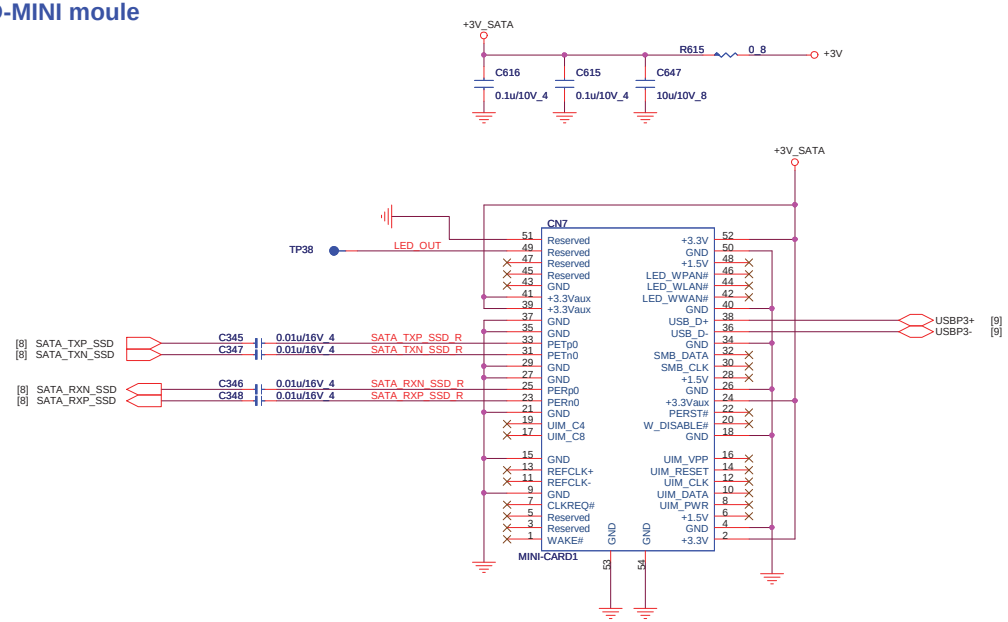
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA







SSD-MINI moule



Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	MINI PCI-E / SSD	1A
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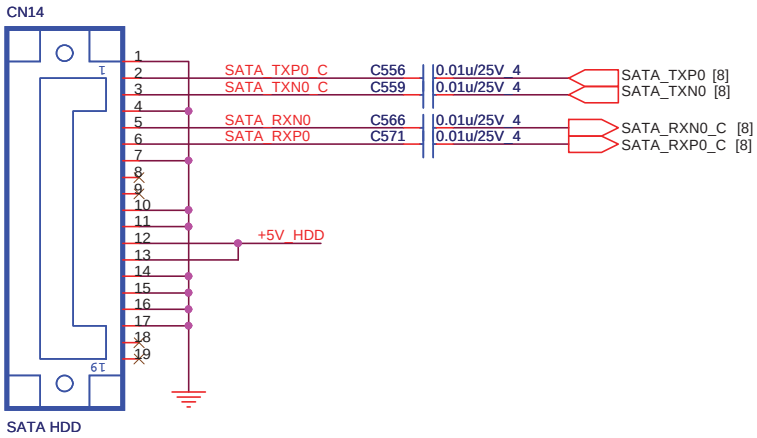
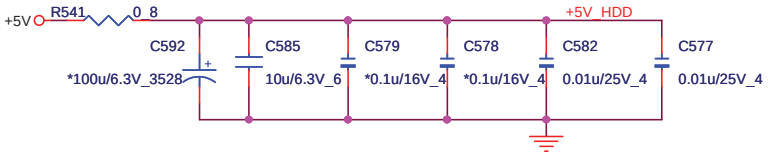
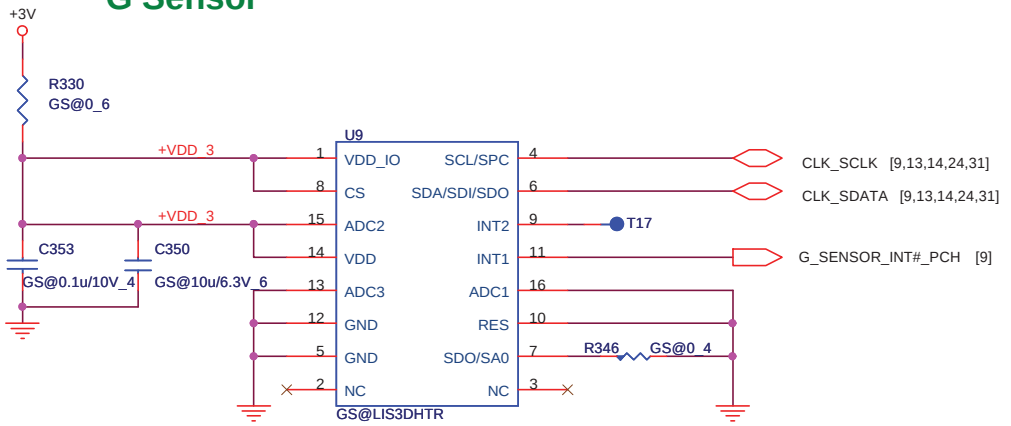
MAIN SATA HDD(HDD)



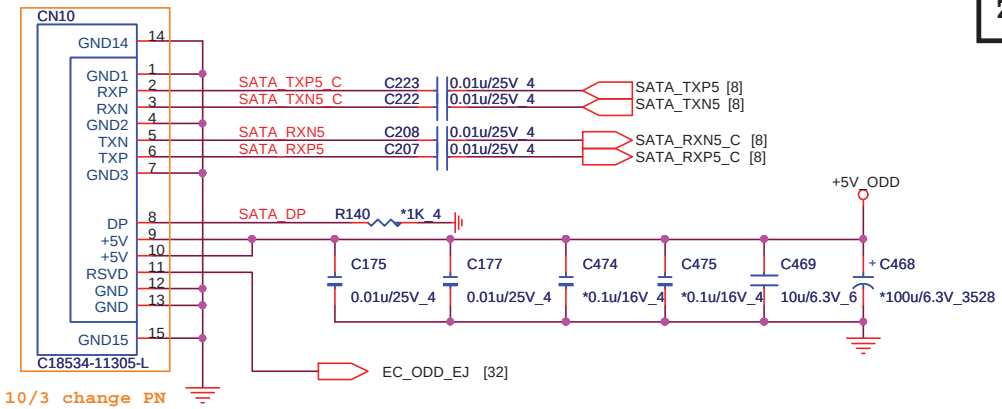


G Sensor



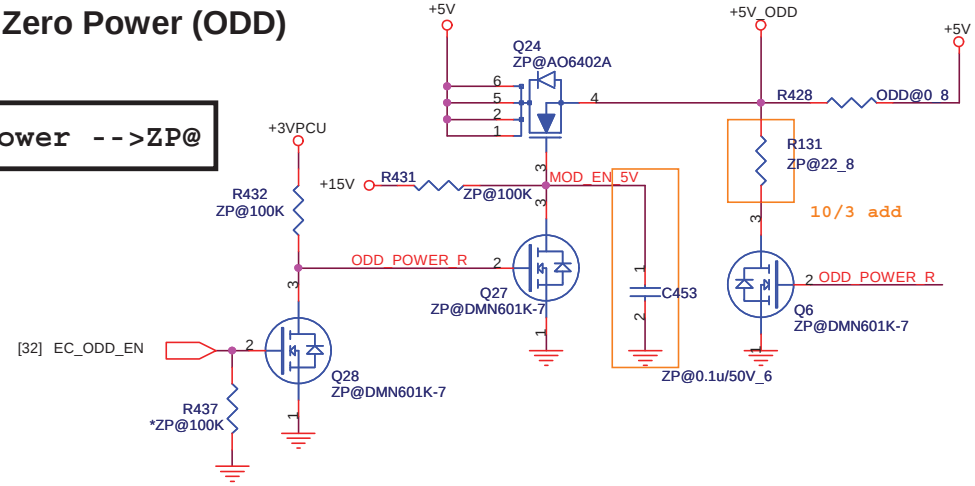
G-Sensor -->GS@

ODD (ODD)



Zero Power (ODD)

Zero Power -->ZP@



Quanta Computer Inc.		
PROJECT : ZQTA/ZQSA		
Size	Document Number: SATA-HDD/ODD/G Sensor	Rev 1A
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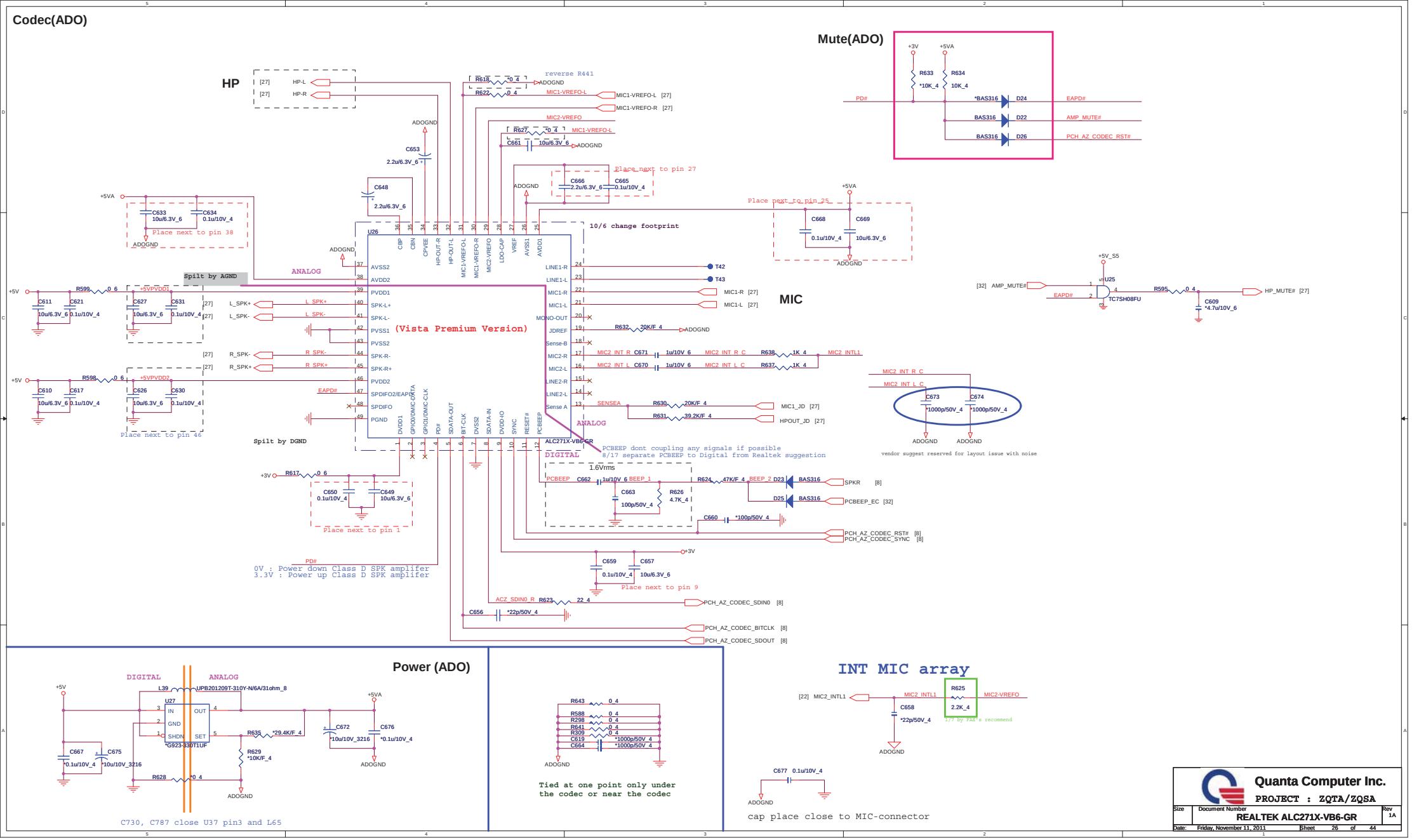
Codec(ADO)



Quanta Computer Inc.			
PROJECT : ZQTA/ZQSA			
Size	Document Number		Rev
	REALTEK ALC271X-VB6-GR		1A
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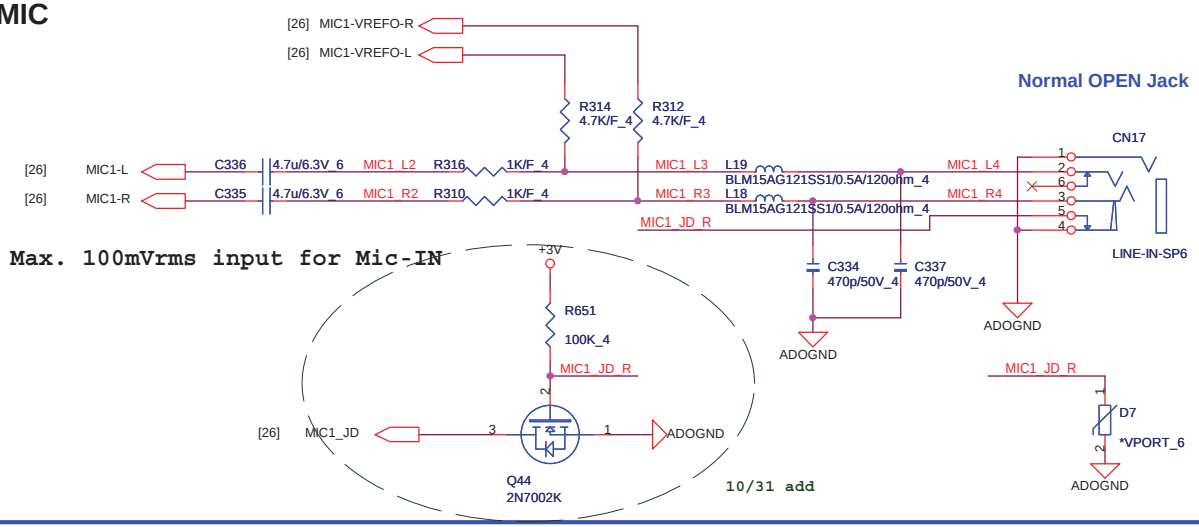
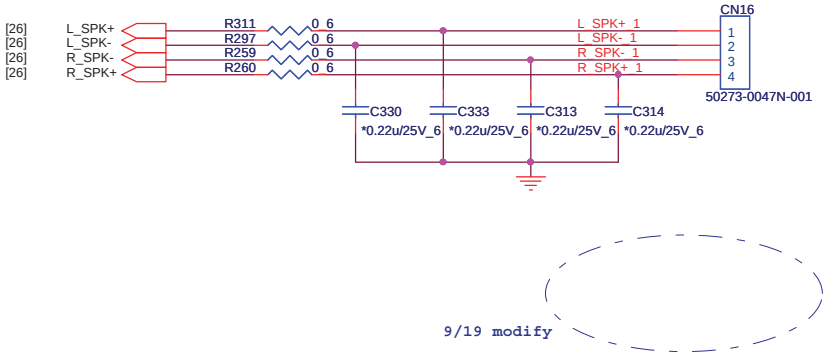
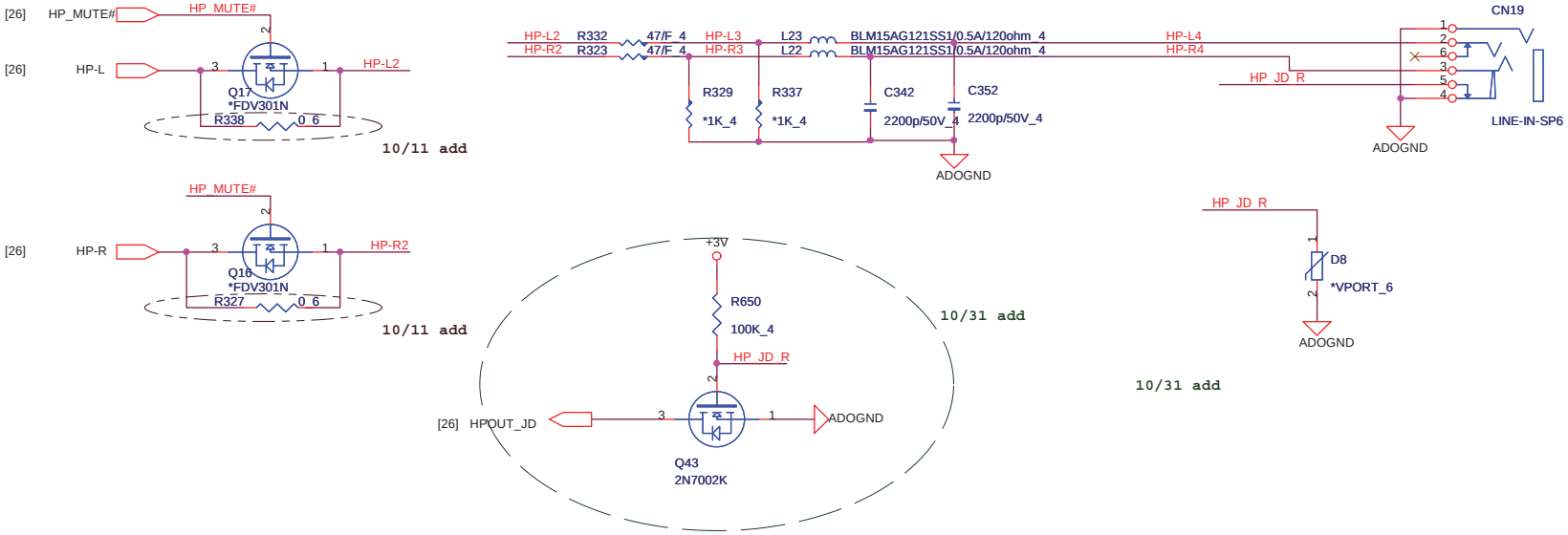
MIC



Internal Speaker



HP



Quanta Computer Inc.		
PROJECT : ZQTA/ZQSA		
Size	Document Number: AUDIO JACK CONN	Rev 1A
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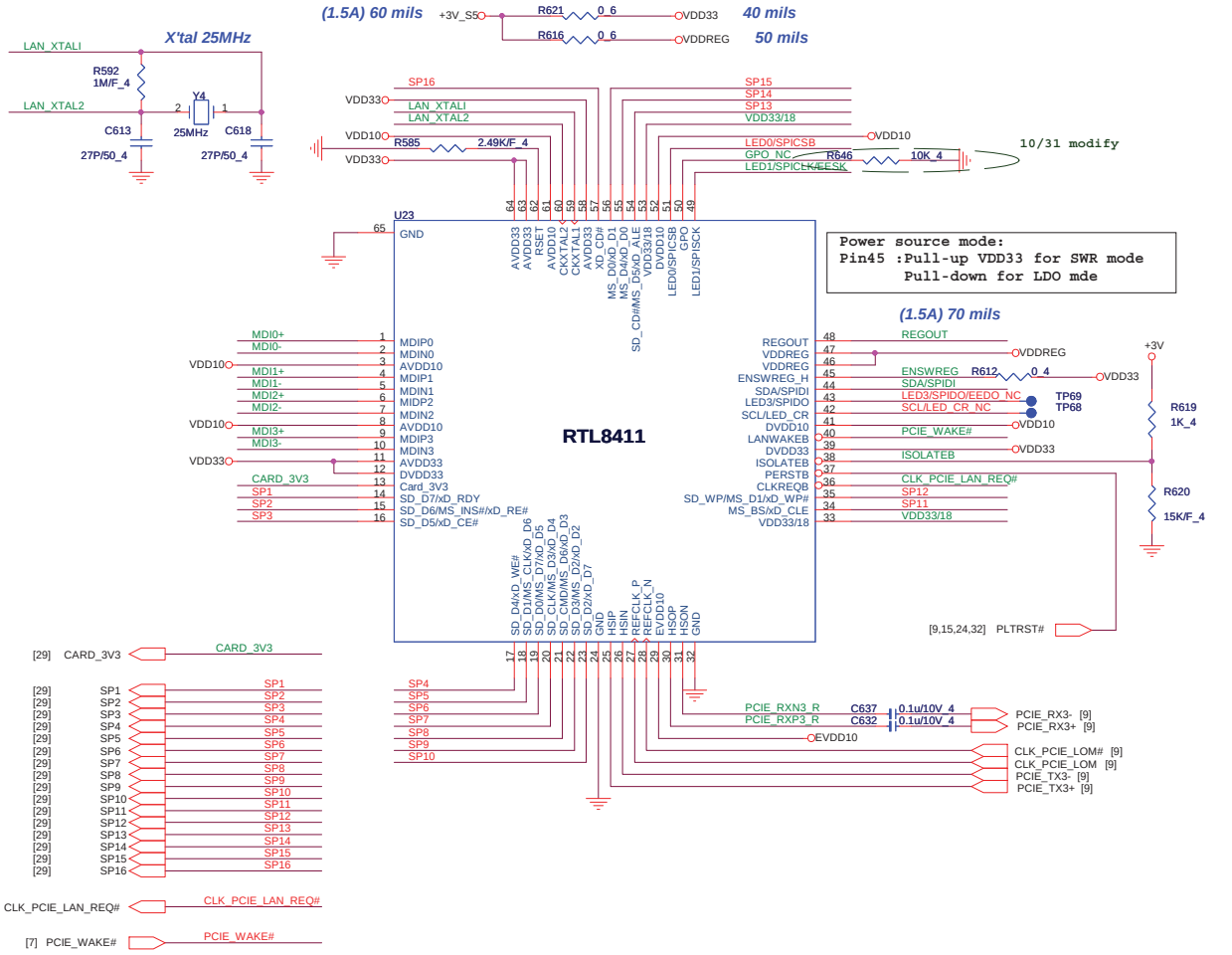
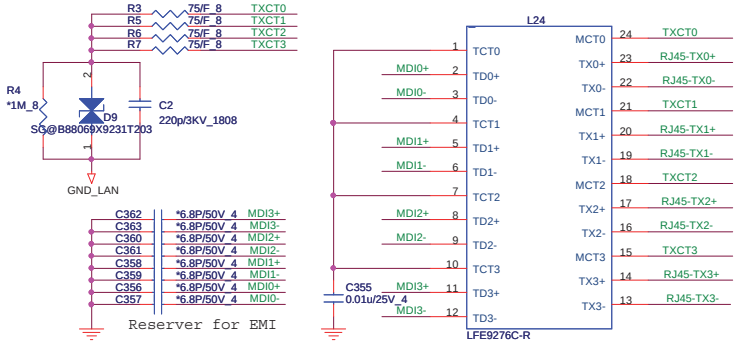
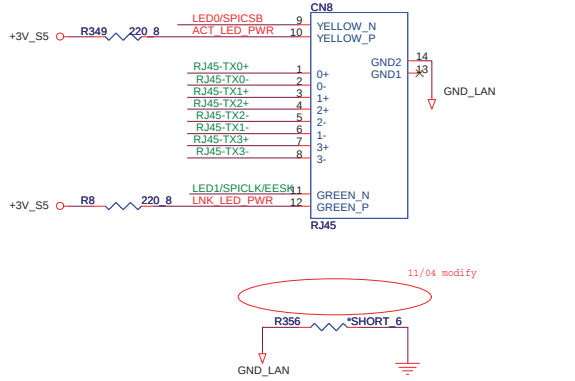
LAN/Card reader



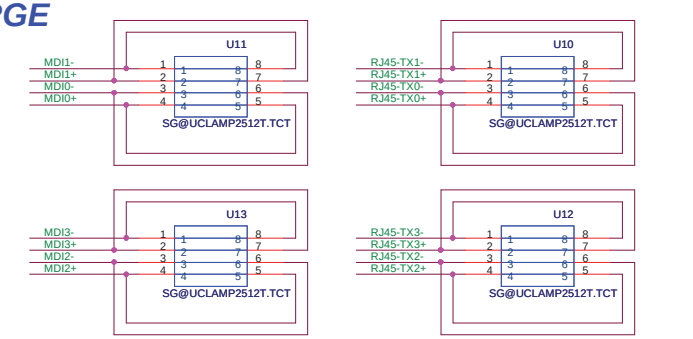
Transformer

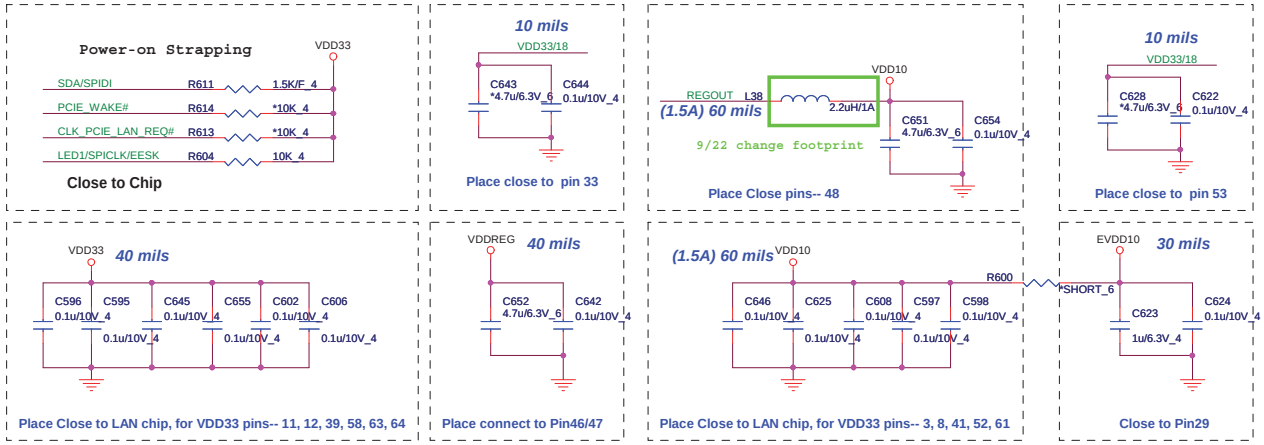


RJ45



SURGE





[3,7,8,9,10,11,15,30,31,34,35,36,41,42] +3V_S5

Quanta Computer Inc.

PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	LAN-RTL8411/CARD READER	1A

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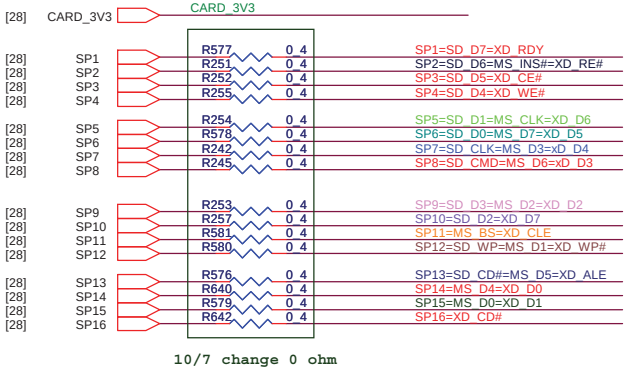
CARD READER CONNECTOR

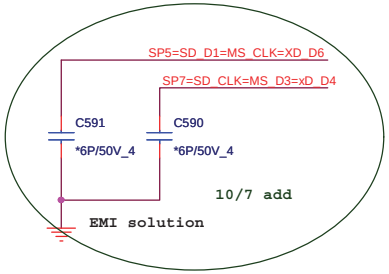
XD,MMC 4.2/SD,MS/MSP 7 IN1 CARD READER

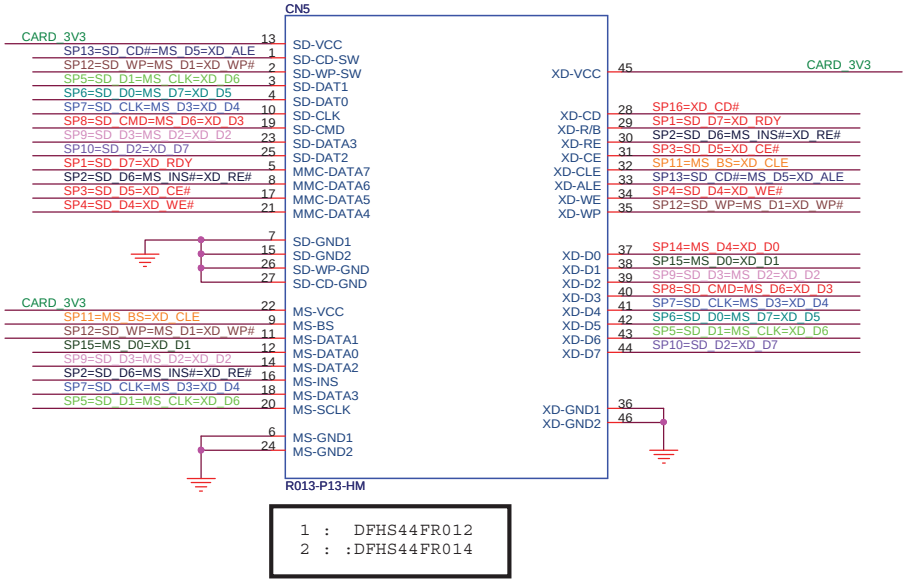
Share Pin

SP1	SD_D7		xD_RDY
SP2	SD_D6	MS_INS#	xD_RE#
SP3	SD_D5		xD_CE#
SP4	SD_D4		xD_WE#
SP5	SD_D1	MS_CLK	xD_D6
SP6	SD_D0	MS_D7	xD_D5
SP7	SD_CLK	MS_D3	xD_D4
SP8	SD_CMD	MS_D6	xD_D3
SP9	SD_D3	MS_D2	xD_D2
SP10	SD_D2		xD_D7
SP11		MS_BS	xD_CLE
SP12	SD_WP	MS_D1	xD_WP#
SP13	SD_CD#	MS_D5	xD_ALE
SP14		MS_D4	xD_D0
SP15		MS_D0	xD_D1
SP16			xD_CD#

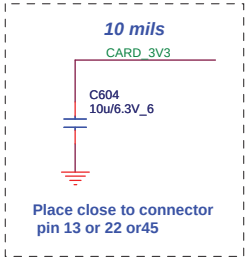


10/7 change 0 ohm





1 : DFHS44FR012
2 : :DFHS44FR014

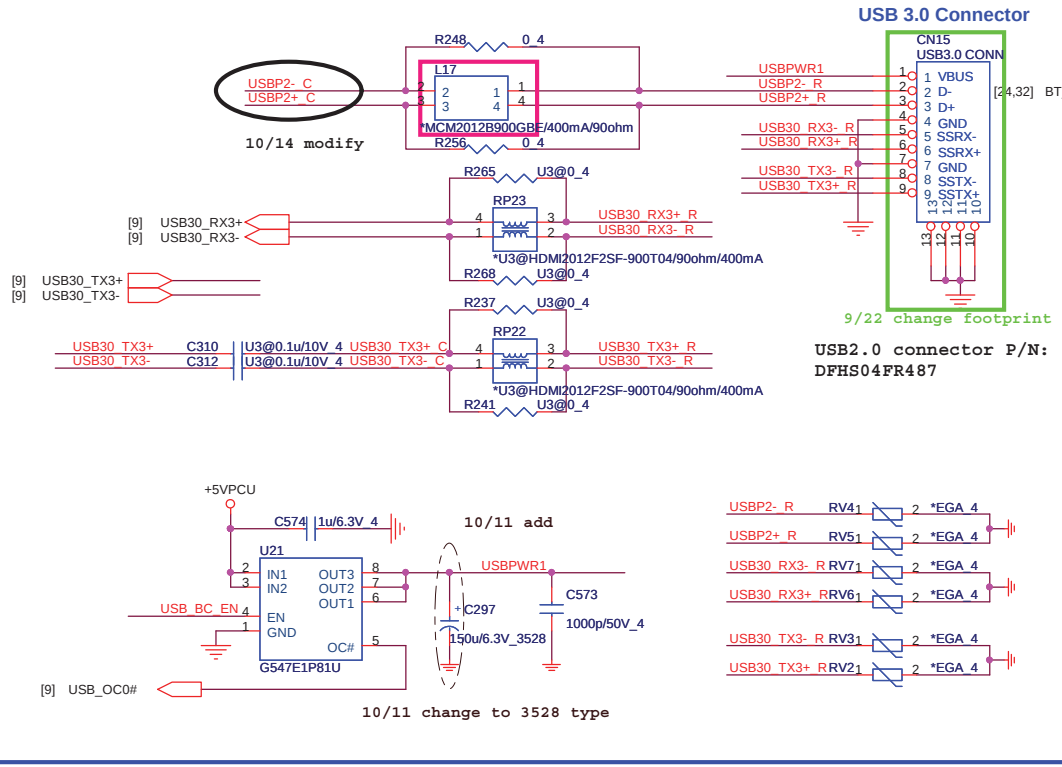


Quanta Computer Inc.

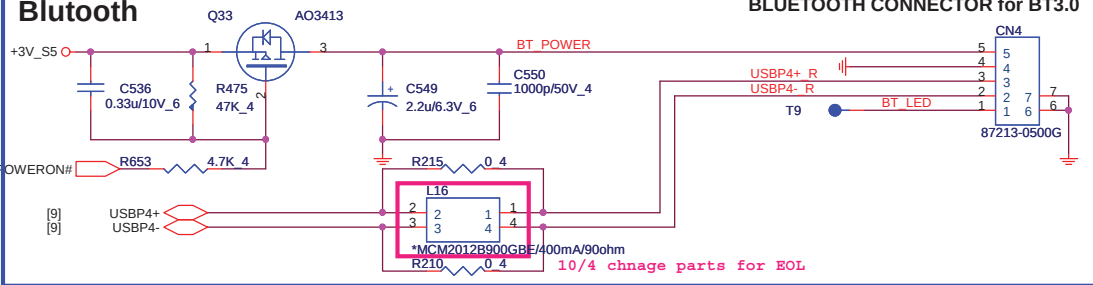
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	CARD READER CONNECTOR	1A
Date: Friday, November 11, 2011	Sheet 29 of 44	

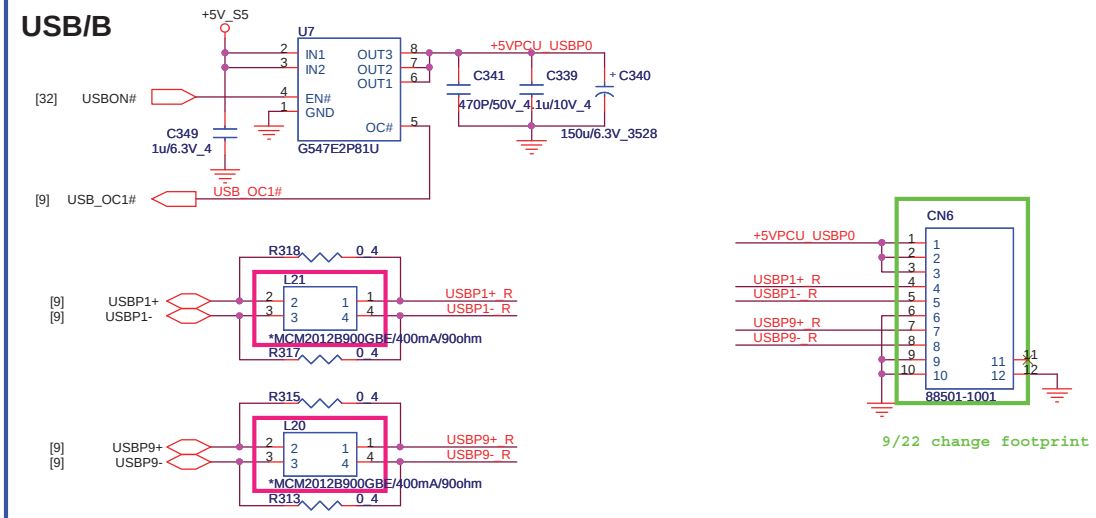
USB3.0/2.0



Blutooth



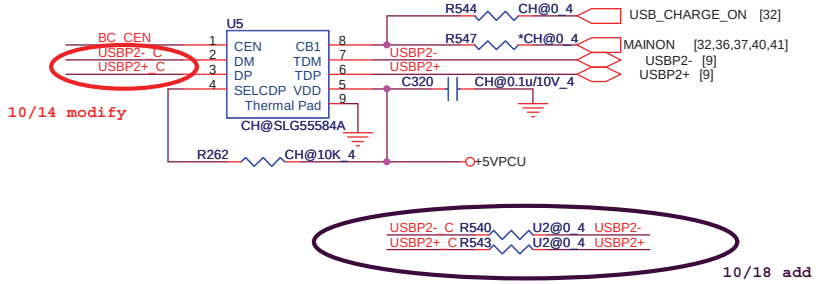
USB/B

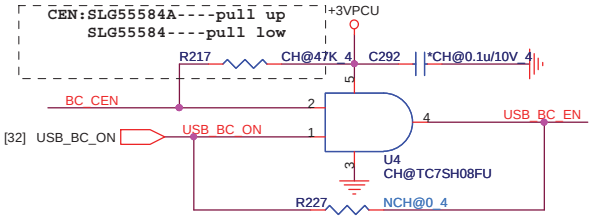


USB Charger to 3.0

CB	SELCDP	Funcion
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)

USB Charger -->CH@
None Charger--> NCH@





Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	USB/ BT/CHARGER	1A
Date: Friday, November 11, 2011	Sheet 30 of 44	

K/B

9/14 modify

CN2

KB CONN

10/11 modify

+VGACORE

+3VPCU

RP13 10K_10P8R

CPU FAN

10/5 add

FANPWR = 1.6*VSET

G995P1U

FAN_CONN.

53398-0310-3P-L

DFHD03MR026

LED

Power

PWRLED#

SUSLED#

LED_AMBER/BLUE

Power Botton

Blue

BEBL0089Z00

LTST-C190TBKT/BLUE

Battery

BATLED0#

BATLED1#

HDD

SATA_ACT#

HDD_LED

WLAN

AMBER

LED_WLAN#

WLAN_LED

TOUCHPAD & Switch CONN.

Model EA/EG/BA---->SW3,SW4

VA/VG--------->SW5,SW6

50mil

10/5 modify

11/04 modify

11/1 modify pin define

SP@SWITCH

For BA WLAN function

BA@SWITCH

*BA@EGA-0402

Quanta Computer Inc.

PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	KB/FAN/TP+FP/LED	1A

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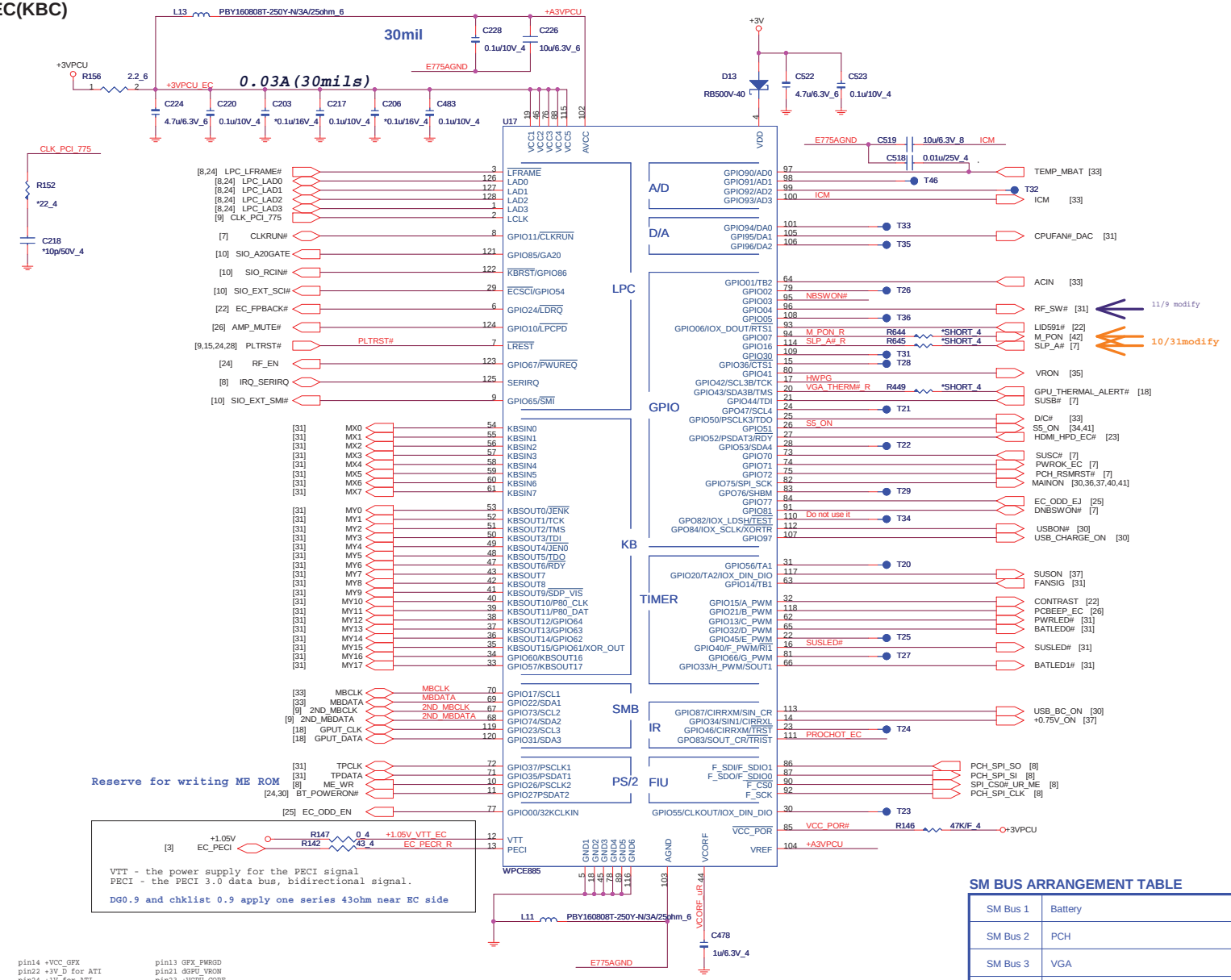
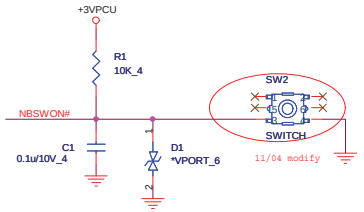
EC(KBC)



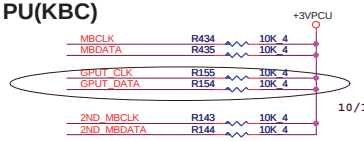
SM BUS ARRANGEMENT TABLE

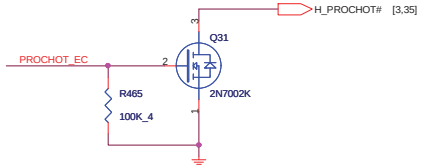
SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	VGA
SM Bus 4	HDMI

Power on bottom

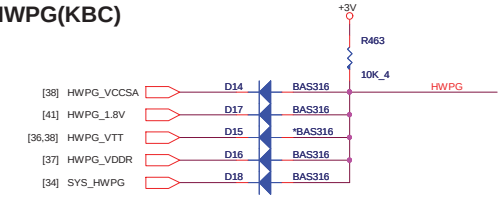


SM BUS PU(KBC)





HWPG(KBC)



Quanta Computer Inc.			
PROJECT : ZQTA/ZQSA			
Size	Document Number		Rev
	WPCE885 & FLASH		1A
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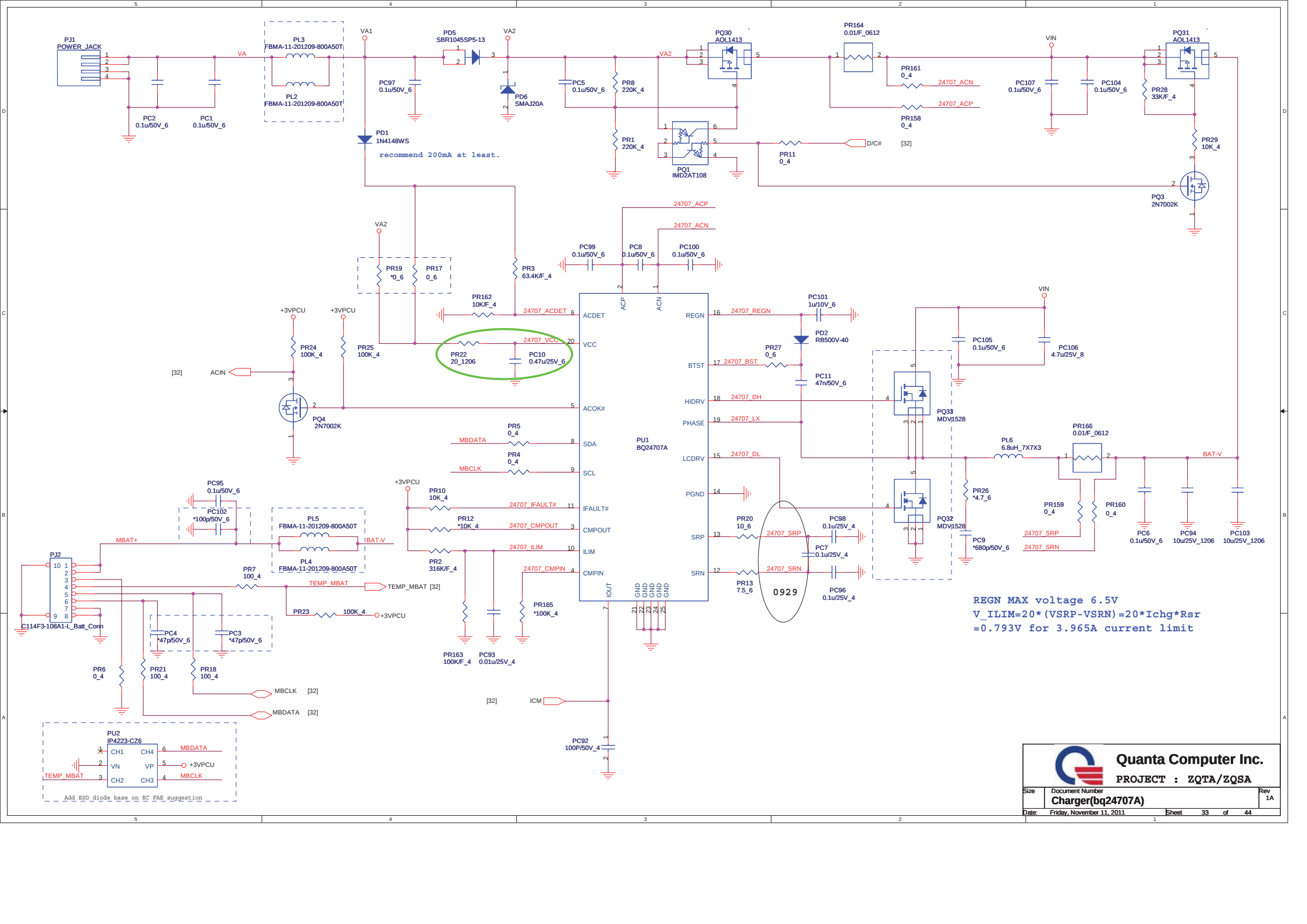
PJ1
POWER_JACK
VA
PC2
0.1u/50V_6
PC1
0.1u/50V_6
PL3
FBMA-11-201209-800A50T
PL2
FBMA-11-201209-800A50T
VA1
PD1
1N4148WS
recommend 200mA at least.
PC97
0.1u/50V_6
PD5
SBR1045SP5-13
VA2
PD6
SMAJ20A
PC5
0.1u/50V_6
PR8
220K_4
PR1
220K_4
PQ30
AOL1413
PQ1
IMD2AT108
PR164
0.01/F_0612
PR161
0_4
PR158
0_4
24707_ACN
24707_ACP
PR11
0_4
D/C#
[32]
VIN
PC107
0.1u/50V_6
PC104
0.1u/50V_6
PQ31
AOL1413
PR28
33K/F_4
PR29
10K_4
PQ3
2N7002K
PR19
*0_6
PR17
0_6
PR3
63.4K/F_4
PC99
0.1u/50V_6
PC8
0.1u/50V_6
PC100
0.1u/50V_6
PR162
10K/F_4
24707_ACDET
PR22
20_1206
24707_VCC
PC10
0.47u/25V_6
PR24
100K_4
PR25
100K_4
+3VPCU
[32]
ACIN
PQ4
2N7002K
PR5
0_4
MBDATA
PR4
0_4
MBCLK
PU1
BQ24707A
ACDET
ACP
ACN
VCC
ACOK#
SDA
SCL
IFAULT#
CMPOUT
ILIM
CMPIN
IOUT
REGN
BTST
HIDRV
PHASE
LCDRV
PGND
SRP
SRN
GND
24707_REGN
24707_BST
24707_DH
24707_LX
24707_DL
24707_SRP
24707_SRN
PC101
1u/10V_6
PD2
RB500V-40
PR27
0_6
PC11
47n/50V_6
PR20
10_6
PC98
0.1u/25V_4
PC7
0.1u/25V_4
PR13
7.5_6
PC96
0.1u/25V_4
0929
PC105
0.1u/50V_6
PC106
4.7u/25V_8
PQ33
MDV1528
PQ32
MDV1528
PL6
6.8uH_7X7X3
PR166
0.01/F_0612
BAT-V
PR26
*4.7_6
PC9
*680p/50V_6
PR159
0_4
PR160
0_4
PC6
0.1u/50V_6
PC94
10u/25V_1206
PC103
10u/25V_1206
PC95
0.1u/50V_6
PC102
*100p/50V_6
PL5
FBMA-11-201209-800A50T
PL4
FBMA-11-201209-800A50T
MBAT+
IBAT-V
PJ2
C114F3-108A1-L_Batt_Conn
PR7
100_4
TEMP_MBAT
TEMP_MBAT [32]
PR23
100K_4
+3VPCU
PC4
*47p/50V_6
PC3
*47p/50V_6
PR6
0_4
PR21
100_4
PR18
100_4
MBCLK [32]
MBDATA [32]
PR10
10K_4
24707_IFAULT#
PR12
*10K_4
24707_CMPOUT
24707_ILIM
PR2
316K/F_4
24707_CMPIN
PR165
*100K_4
PR163
100K/F_4
PC93
0.01u/25V_4
[32]
ICM
PC92
100P/50V_4
PU2
IP4223-CZ6
CH1
CH2
CH3
CH4
VN
VP
Add ESD diode base on EC FAE suggestion
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
Quanta Computer Inc.
PROJECT : ZQTA/ZQSA
Size
Document Number
Charger(bq24707A)
Rev
1A
Date: Friday, November 11, 2011
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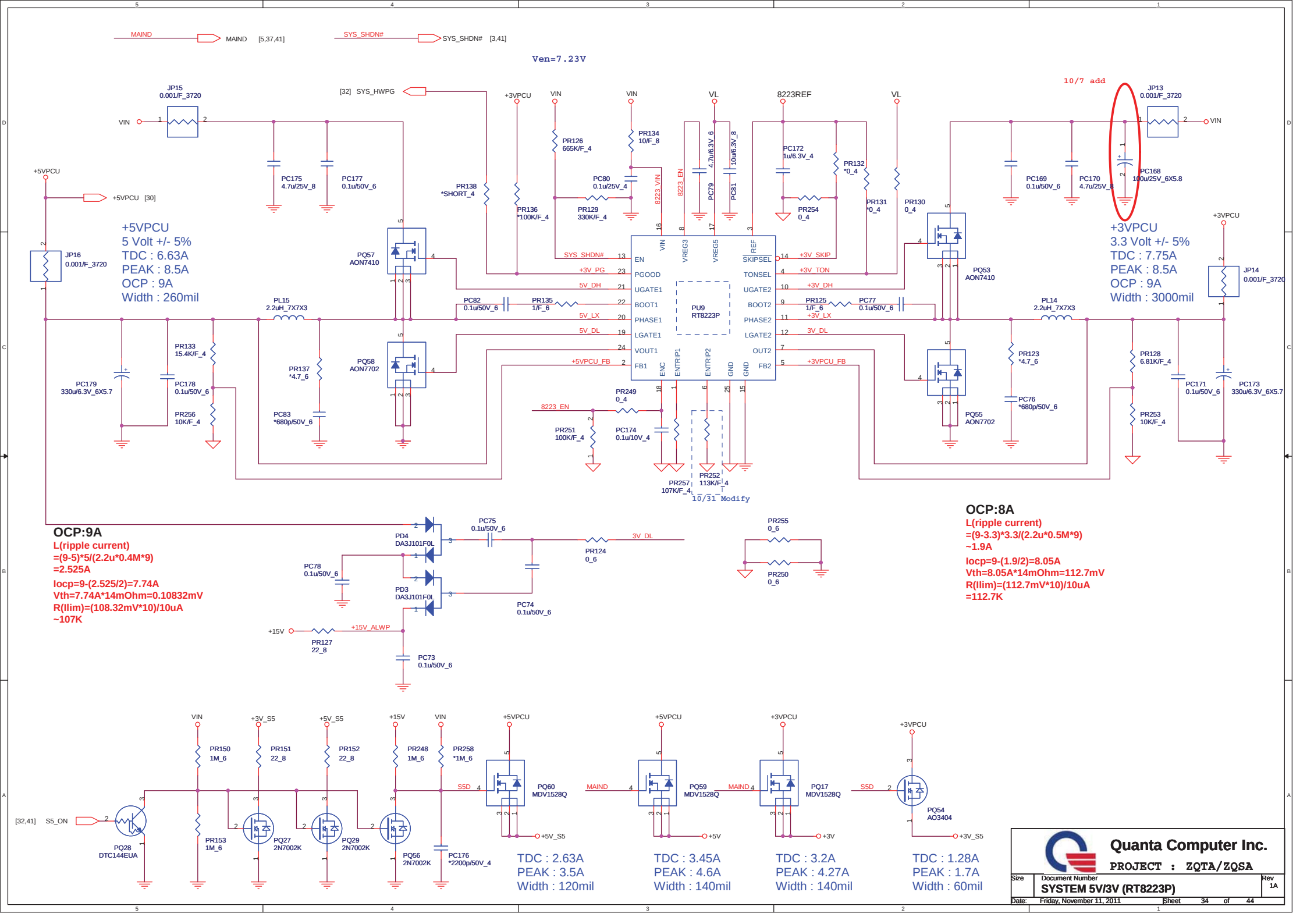
MAIND
MAIND [5,37,41]
SYS_SHDN#
SYS_SHDN# [3,41]
Ven=7.23V
10/7 add
+5VPCU
5 Volt +/- 5%
TDC : 6.63A
PEAK : 8.5A
OCP : 9A
Width : 260mil
+3VPCU
3.3 Volt +/- 5%
TDC : 7.75A
PEAK : 8.5A
OCP : 9A
Width : 3000mil
PU9
RT8223P
10/31 Modify
OCP:9A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
=2.525A
Iocp=9-(2.525/2)=7.74A
Vth=7.74A*14mOhm=0.10832mV
R(Ilim)=(108.32mV*10)/10uA
~107K
OCP:8A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
~1.9A
Iocp=9-(1.9/2)=8.05A
Vth=8.05A*14mOhm=112.7mV
R(Ilim)=(112.7mV*10)/10uA
=112.7K
TDC : 2.63A
PEAK : 3.5A
Width : 120mil
TDC : 3.45A
PEAK : 4.6A
Width : 140mil
TDC : 3.2A
PEAK : 4.27A
Width : 140mil
TDC : 1.28A
PEAK : 1.7A
Width : 60mil
Quanta Computer Inc.
PROJECT : ZQTA/ZQSA
SYSTEM 5V/3V (RT8223P)
Size
Document Number
Rev 1A
Date: Friday, November 11, 2011
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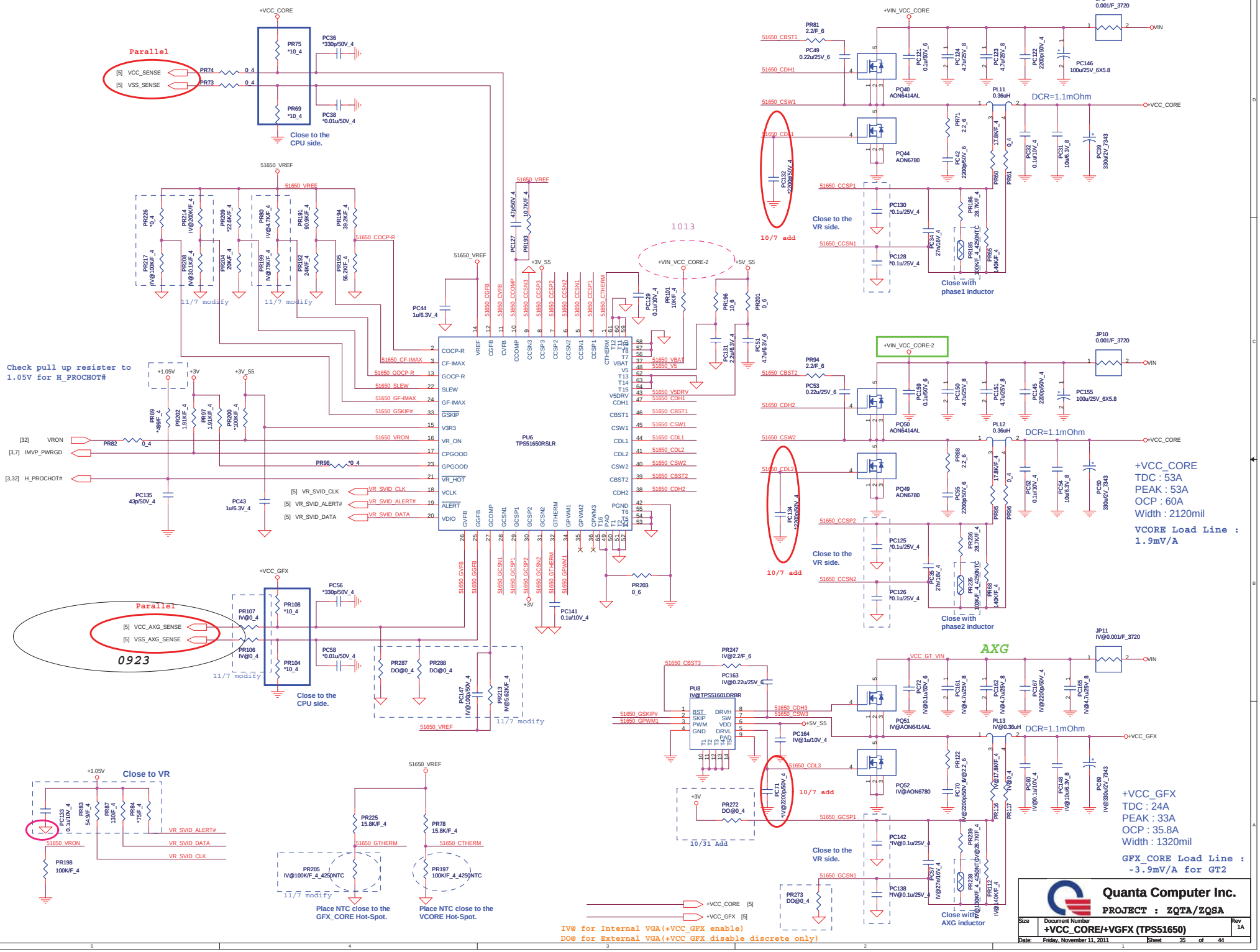
Parallel
[5] VCC_SENSE
[5] VSS_SENSE
PR74 0_4
PR73 0_4
PR75 *10_4
PR69 *10_4
PC36 *330p/50V_4
PC38 *0.01u/50V_4
+VCC_CORE
Close to the CPU side.
51650_VREF
PR226 *0_4
PR214 IV@200K/F_4
PR209 *22.6K/F_4
PR80 IV@4.7K/F_4
PR191 90.9K/F_4
PR184 39.2K/F_4
PR217 IV@100K/F_4
PR208 IV@30.1K/F_4
PR204 20K/F_4
PR199 IV@75K/F_4
PR192 24K/F_4
PR185 55.2K/F_4
51650_COCP-R
11/7 modify
PC44 1u/6.3V_4
PC127 47p/50V_4
PR193 10.7K/F_4
+3V_S5
1013
+VIN_VCC_CORE-2
+5V_S5
PC129 0.1u/10V_4
PR101 10K/F_4
PR196 10_6
PR201 0_6
PC131 2.2u/6.3V_4
PC51 4.7u/6.3V_6
Check pull up resister to 1.05V for H_PROCHOT#
+1.05V
+3V
+3V_S5
PR89 *499/F_4
PR202 1.91K/F_4
PR97 1.91K/F_4
PR200 *100K/F_4
[32] VRON
[3,7] IMVP_PWRGD
[3,32] H_PROCHOT#
PR82 0_4
PR98 *0_4
PC135 43p/50V_4
PC43 1u/6.3V_4
[5] VR_SVID_CLK
[5] VR_SVID_ALERT#
[5] VR_SVID_DATA
PU6
TPS51650RSLR
COCP-R
CF-IMAX
GOCP-R
SLEW
GF-IMAX
GSKIP
V3R3
VR_ON
CPGOOD
GPGOOD
VR_HOT
VCLK
ALERT
VDIO
PR203 0_6
PC141 0.1u/10V_4
+VCC_GFX
Parallel
[5] VCC_AXG_SENSE
[5] VSS_AXG_SENSE
0923
PR107 IV@0_4
PR106 IV@0_4
PR108 *10_4
PR104 *10_4
PC56 *330p/50V_4
PC58 *0.01u/50V_4
Close to the CPU side.
PR287 DO@0_4
PR288 DO@0_4
PC147 IV@100K/F_4
PR213 IV@5.62K/F_4
Close to VR
PC133 0.1u/10V_4
PR83 54.9K/F_4
PR87 130K/F_4
PR84 *75K/F_4
VR_SVID_ALERT#
VR_SVID_DATA
VR_SVID_CLK
51650_VRON
PR198 100K/F_4
PR225 15.8K/F_4
PR78 15.8K/F_4
51650_GTHERM
51650_CTHERM
PR205 IV@100K/F_4_4250NTC
PR197 100K/F_4_4250NTC
Place NTC close to the GFX_CORE Hot-Spot.
Place NTC close to the VCORE Hot-Spot.
+VCC_CORE [5]
+VCC_GFX [5]
IV@ for Internal VGA(+VCC_GFX enable)
DO@ for External VGA(+VCC_GFX disable discrete only)
+VIN_VCC_CORE
PR81 2.2/F_6
PC49 0.22u/25V_6
51650_CBST1
51650_CDH1
51650_CSW1
51650_CDL1
PQ40 AON6414AL
PQ44 AON6780
PC132 *2200p/50V_4
10/7 add
PL11 0.36uH
DCR=1.1mOhm
PR71 2.2_6
PC42 2200p/50V_6
PR60 17.8K/F_4
PR61 0_4
PC32 0.1u/10V_4
PC31 10u/6.3V_8
PC39 330u/2V_7343
JP8 0.001/F_3720
VIN
+VCC_CORE
51650_CCSP1
51650_CCSN1
PC130 *0.1u/25V_4
PC128 *0.1u/25V_4
PC134 27n/10V_4
PR185 100K/F_4_4250NTC
PR65 140K/F_4
Close to the VR side.
Close with phase1 inductor
PR94 2.2/F_6
PC53 0.22u/25V_6
51650_CBST2
51650_CDH2
51650_CSW2
51650_CDL2
PQ50 AON6414AL
PQ49 AON6780
PC134 *2200p/50V_4
10/7 add
PL12 0.36uH
DCR=1.1mOhm
PR88 2.2_6
PC35 2200p/50V_6
PR65 17.8K/F_4
PR66 0_4
PC52 0.1u/10V_4
PC54 10u/6.3V_8
PC50 330u/2V_7343
JP10 0.001/F_3720
51650_CCSP2
51650_CCSN2
PC125 *0.1u/25V_4
PC126 *0.1u/25V_4
PC36 27n/10V_4
PR235 100K/F_4_4250NTC
PR63 140K/F_4
Close to the VR side.
Close with phase2 inductor
+VCC_CORE
TDC : 53A
PEAK : 53A
OCP : 60A
Width : 2120mil
VCORE Load Line : 1.9mV/A
AXG
PR247 IV@2.2/F_6
PC163 IV@0.22u/25V_6
51650_CBST3
51650_CDH3
51650_CSW3
51650_CDL3
PU8 IV@TPS51601DRBR
51650_GSKIP#
51650_GPWM1
PQ51 IV@AON6414AL
PQ52 IV@AON6780
PC164 IV@1u/10V_4
PC71 *IV@2200p/50V_4
10/7 add
PR272 DO@0_4
10/31 Add
PL13 IV@0.36uH
DCR=1.1mOhm
PR122 IV@2.2_6
PC70 IV@2200p/50V_4
PR116 IV@17.8K/F_4
PR117 IV@0_4
PC60 IV@0.1u/10V_4
PC148 IV@10u/6.3V_8
PC69 IV@330u/2V_7343
JP11 IV@0.001/F_3720
51650_GCSP1
51650_GCSN1
PC142 *IV@0.1u/25V_4
PC138 *IV@0.1u/25V_4
PC57 IV@27n/10V_4
PR239 IV@28.7K/F_4
PR238 IV@100K/F_4_4250NTC
PR113 IV@140K/F_4
PR273 DO@0_4
Close to the VR side.
Close with AXG inductor
+VCC_GFX
TDC : 24A
PEAK : 33A
OCP : 35.8A
Width : 1320mil
GFX_CORE Load Line : -3.9mV/A for GT2
Quanta Computer Inc.
PROJECT : ZQTA/ZQSA
Size
Document Number
+VCC_CORE/+VGFX (TPS51650)
Rev 1A
Date: Friday, November 11, 2011
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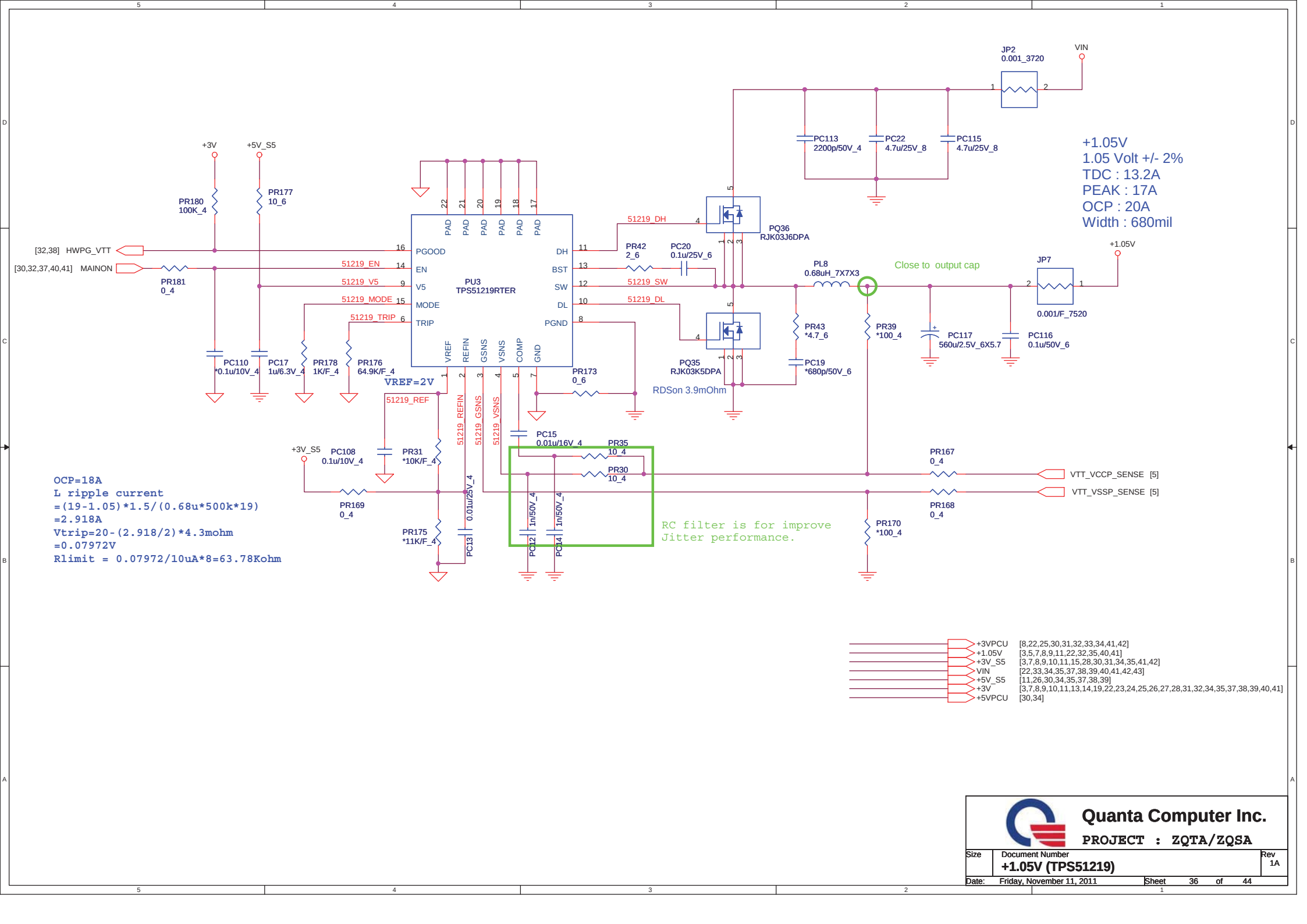
JP2
0.001_3720
VIN
PC113
2200p/50V_4
PC22
4.7u/25V_8
PC115
4.7u/25V_8
+1.05V
1.05 Volt +/- 2%
TDC : 13.2A
PEAK : 17A
OCP : 20A
Width : 680mil
+3V
+5V_S5
PR180
100K_4
PR177
10_6
[32,38] HWPG_VTT
[30,32,37,40,41] MAINON
PR181
0_4
PU3
TPS51219RTER
PGOOD
EN
V5
MODE
TRIP
DH
BST
SW
DL
PGND
PAD
51219_EN
51219_V5
51219_MODE
51219_TRIP
51219_DH
51219_SW
51219_DL
PR42
2_6
PC20
0.1u/25V_6
PQ36
RJK03J6DPA
PQ35
RJK03K5DPA
PL8
0.68uH_7X7X3
Close to output cap
JP7
+1.05V
0.001/F_7520
PR43
*4.7_6
PC19
*680p/50V_6
PR39
*100_4
PC117
560u/2.5V_6X5.7
PC116
0.1u/50V_6
RDSon 3.9mOhm
PC110
*0.1u/10V_4
PC17
1u/6.3V_4
PR178
1K/F_4
PR176
64.9K/F_4
VREF=2V
VREF
REFIN
GSNS
VSNS
COMP
GND
PR173
0_6
51219_REF
51219_REFIN
51219_GSNS
51219_VSNS
PC15
0.01u/16V_4
PR35
10_4
PR30
10_4
+3V_S5
PC108
0.1u/10V_4
PR31
*10K/F_4
PR169
0_4
PR175
*11K/F_4
PC13
0.01u/25V_4
PC12
1n/50V_4
PC14
1n/50V_4
PR167
0_4
PR168
0_4
PR170
*100_4
VTT_VCCP_SENSE [5]
VTT_VSSP_SENSE [5]
OCP=18A
L ripple current
=(19-1.05)*1.5/(0.68u*500k*19)
=2.918A
Vtrip=20-(2.918/2)*4.3mohm
=0.07972V
Rlimit = 0.07972/10uA*8=63.78Kohm
RC filter is for improve
Jitter performance.
+3VPCU [8,22,25,30,31,32,33,34,41,42]
+1.05V [3,5,7,8,9,11,22,32,35,40,41]
+3V_S5 [3,7,8,9,10,11,15,28,30,31,34,35,41,42]
VIN [22,33,34,35,37,38,39,40,41,42,43]
+5V_S5 [11,26,30,34,35,37,38,39]
+3V [3,7,8,9,10,11,13,14,19,22,23,24,25,26,27,28,31,32,34,35,37,38,39,40,41]
+5VPCU [30,34]
Quanta Computer Inc.
PROJECT : ZQTA/ZQSA
Size
Document Number
+1.05V (TPS51219)
Rev
1A
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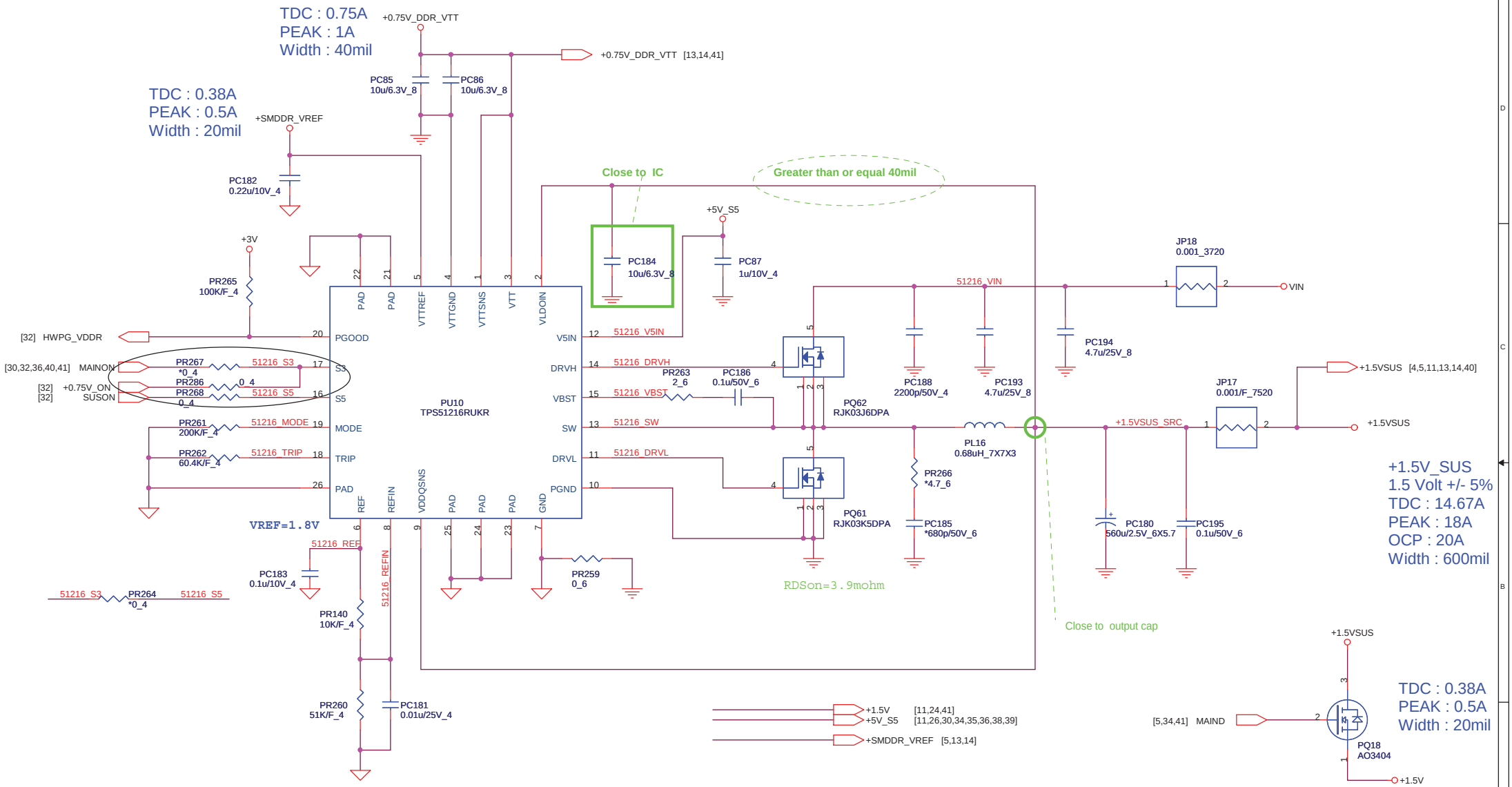

OCP=20A
L ripple current
=(19-1.5)*1.5/(0.68u*400k*19)
=5.079A
Vtrip=20-(5.079/2)*4.3mohm
=0.07508V
Rlimit=0.07508/10uA*8=60.063Kohm

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	DDR 1.5V(TPS51216)	1A
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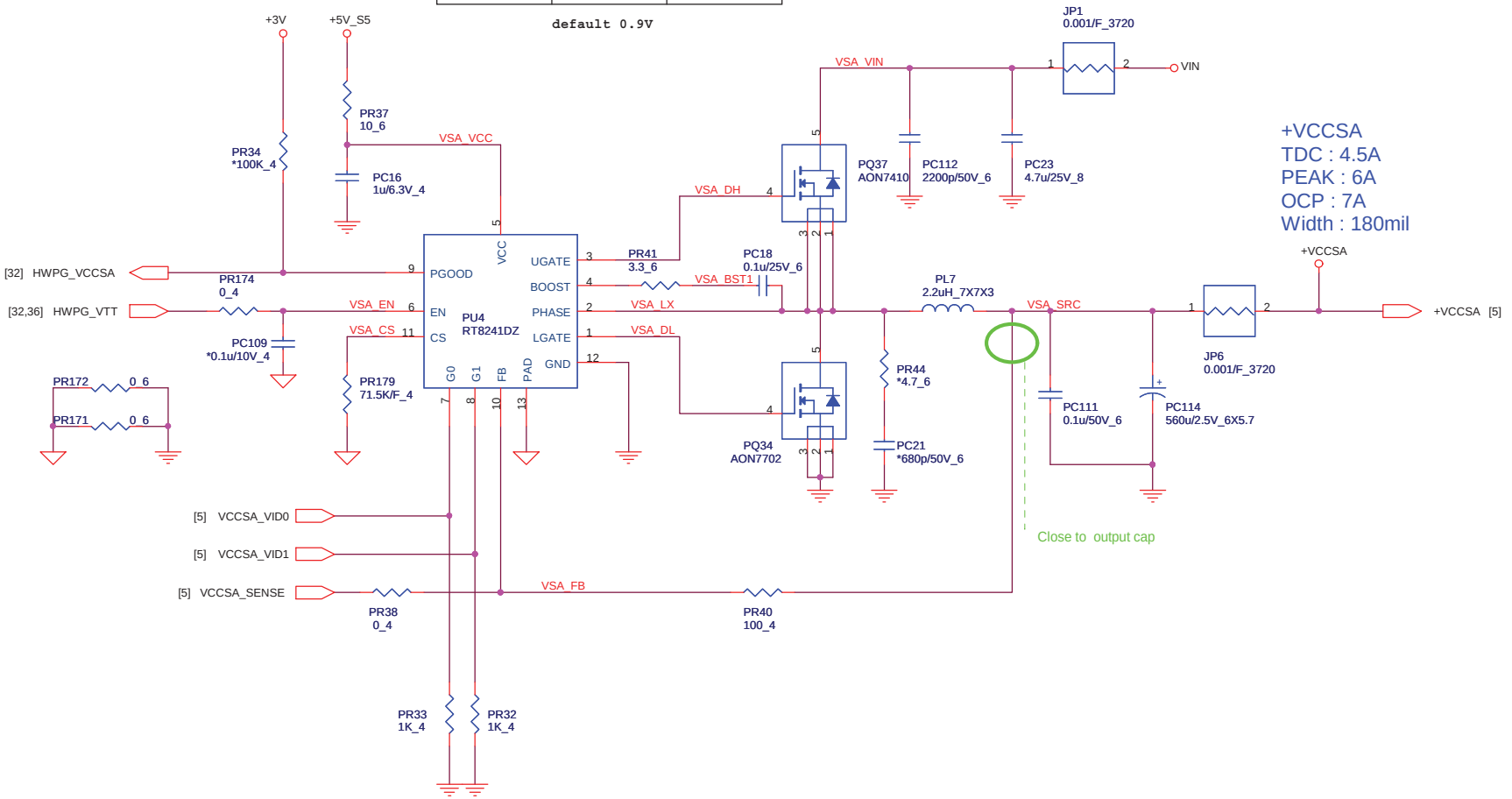
G0	G1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

default 0.9V



+VCCSA
TDC : 4.5A
PEAK : 6A
OCP : 7A
Width : 180mil

OCP=7A
Iripple=(19-0.9)*0.9/(2.2u*300K*19)
=1.299A
Rth=14mohm*8*(7-0.65)/10uA
=71.125K
Ipeak=8.299A

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PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	VCCSA(RT8241DZ)	1A
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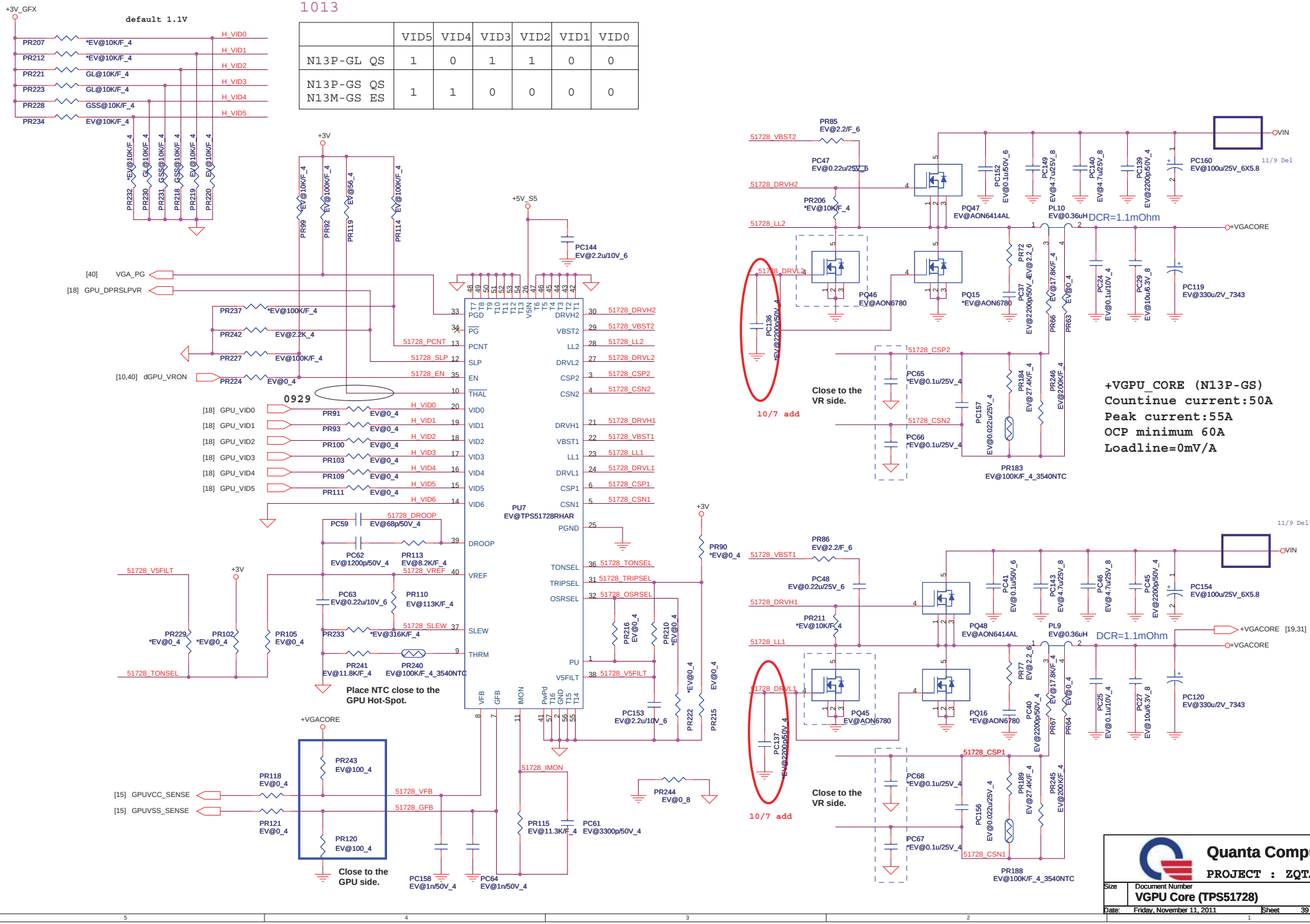
1013

	VID5	VID4	VID3	VID2	VID1	VID0
N13P-GL QS	1	0	1	1	0	0
N13P-GS QS N13M-GS ES	1	1	0	0	0	0



Quanta Computer Inc.

PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	VGPU Core (TPS51728)	1A

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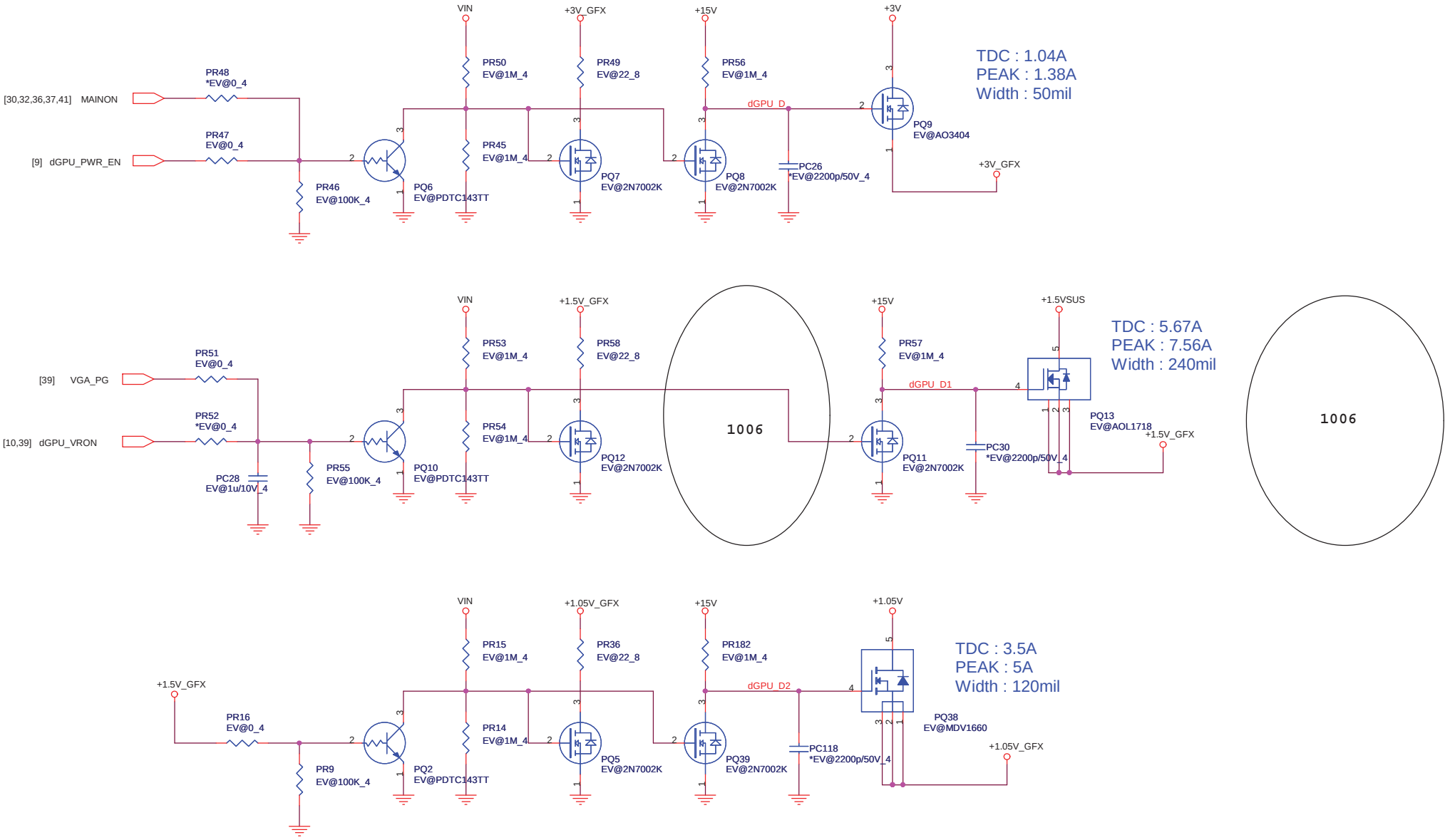

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PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	GPU_PWR	1A
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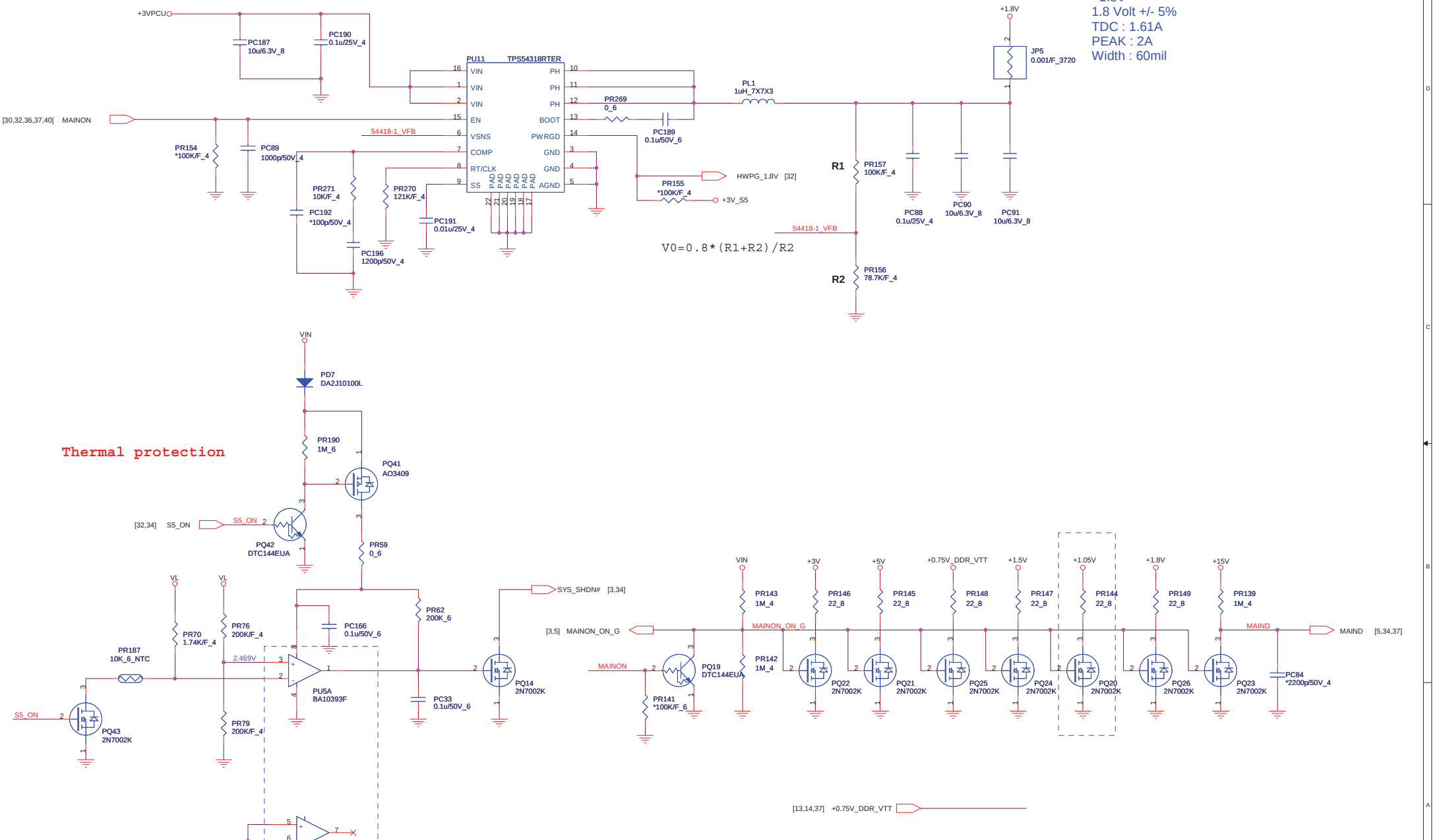
+1.8V
1.8 Volt +/- 5%
TDC : 1.61A
PEAK : 2A
Width : 60mil
+3VPCU
PC187 10u/6.3V_8
PC190 0.1u/25V_4
PU11 TPS54318RTER
VIN
PH
BOOT
PWRGD
GND
AGND
EN
VSNS
COMP
RT/CLK
SS
PAD
[30,32,36,37,40] MAINON
PR154 *100K/F_4
PC89 1000p/50V_4
54418-1_VFB
PR271 10K/F_4
PR270 121K/F_4
PC192 *100p/50V_4
PC196 1200p/50V_4
PC191 0.01u/25V_4
PR269 0_6
PC189 0.1u/50V_6
PL1 1uH_7X7X3
HWPG_1.8V [32]
PR155 *100K/F_4
+3V_S5
+1.8V
JP5 0.001/F_3720
R1
PR157 100K/F_4
PC88 0.1u/25V_4
PC90 10u/6.3V_8
PC91 10u/6.3V_8
54418-1_VFB
R2
PR156 78.7K/F_4
V0=0.8*(R1+R2)/R2
Thermal protection
VIN
PD7 DA2J10100L
PR190 1M_6
PQ41 AO3409
[32,34] S5_ON
S5_ON
PQ42 DTC144EUA
PR59 0_6
VL
PR70 1.74K/F_4
PR76 200K/F_4
PR187 10K_6_NTC
2.469V
PC166 0.1u/50V_6
PR62 200K_6
PU5A BA10393F
PC33 0.1u/50V_6
PR79 200K/F_4
PQ43 2N7002K
PU5B BA10393F
SYS_SHDN# [3,34]
PQ14 2N7002K
[3,5] MAINON_ON_G
MAINON
PQ19 DTC144EUA
PR141 *100K/F_6
PR142 1M_4
PR143 1M_4
PR146 22_8
PR145 22_8
PR148 22_8
PR147 22_8
PR144 22_8
PR149 22_8
PR139 1M_4
+3V
+5V
+0.75V_DDR_VTT
+1.5V
+1.05V
+15V
PQ22 2N7002K
PQ21 2N7002K
PQ25 2N7002K
PQ24 2N7002K
PQ20 2N7002K
PQ26 2N7002K
PQ23 2N7002K
MAIND
MAIND [5,34,37]
PC84 *2200p/50V_4
[13,14,37] +0.75V_DDR_VTT
For EC control thermal protection (output 3.3V)
Quanta Computer Inc.
PROJECT : ZQTA/ZQSA
Size
Document Number
+1.8V/Discharge/Thermal
Rev 1A
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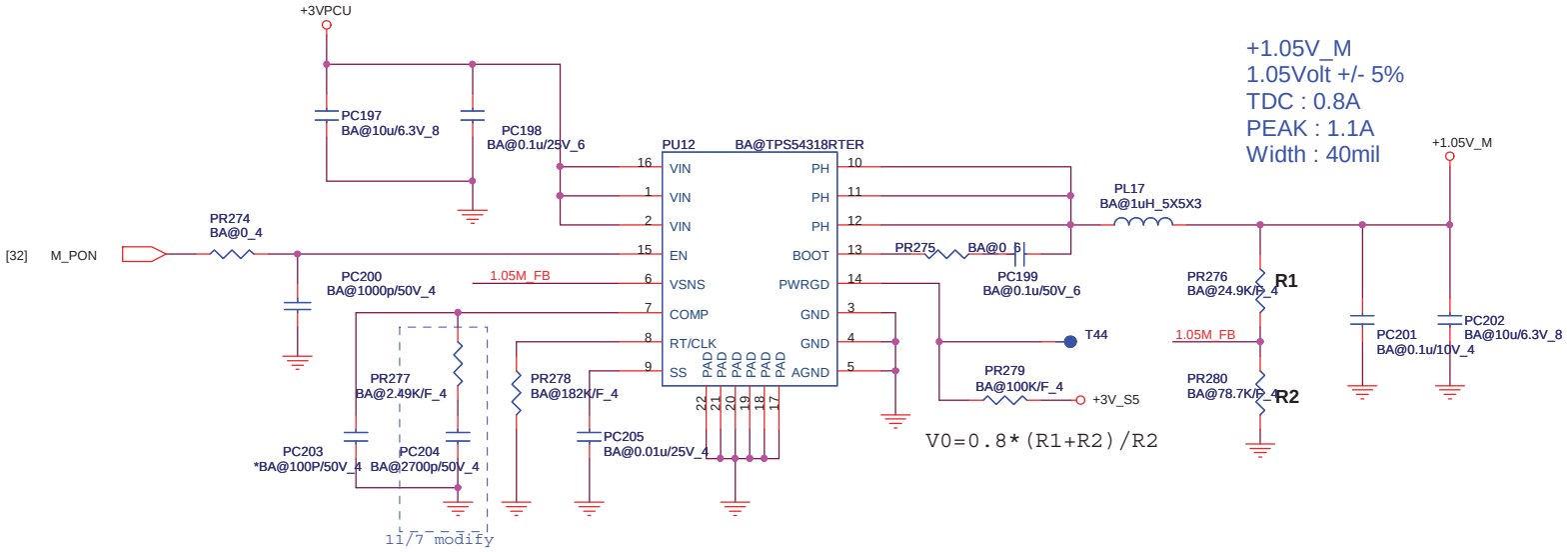

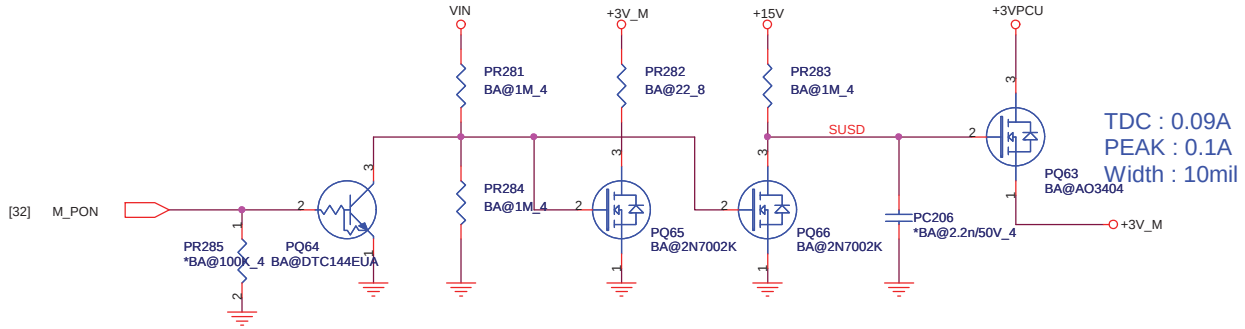

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PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	+1.05V_M/+3V_M	1A
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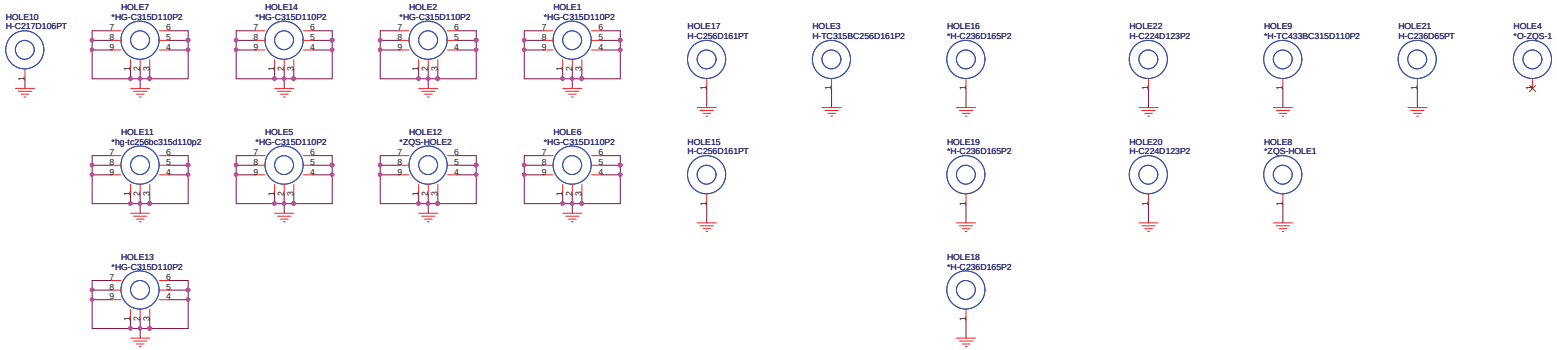
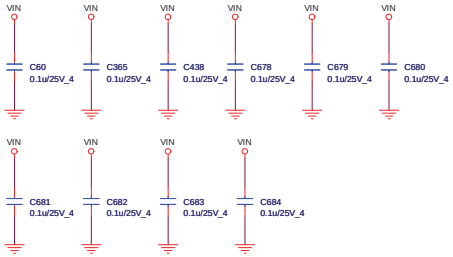
Hole





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PROJECT : ZQTA/ZQSA

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	Hole	1A

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Model	date	CHANGE LIST
ZASA/ZSQTA	9/26	page3 : add R511,R525,R527,R528,R529 for Discrete Only &PCH_JTAG_TDO net change pull-up from +3V_S5 to +1.05 rail
	9/27	Update power circuit Page19 : add C3777,C3778
	9/30	Page18 : add Q3508 for U7 GPU_THERMAL_ALERT net Page31 : Del CN1
	10/3	Page18 : add dGPU_ACDC# net to U7 GPIO04 & add R347 Page22 : add R557,R554 to pull-down & R548,R547 stuff for Discrete only Page25 : add R3693,C116 for ODD zero power circuit
	10/4	Page31 : CN8 add board id3 & board id4 net for touch pad ID control
	10/5	Page31 : CN8.2,CN8.3 add CLK_SDATA & CLK_SCLK net for touch pad & add R278,R279 Page15 : U41 Power rail change to +3V_GFX Page24 : Del Q16 no't support wake up function Page18 : add Q3509 for dGPU_ACDC# net Page31 : add L35,R3694,R3695 for touch pad 5V & 3V option & add R297,R295 Fan PWR option
	10/6	Page17 : IFPAB_PLLVDD rail change from +1.8V_GFX to +3V_GFX Page27 : U6 change footprint Page39 : PWR engineer add PQ3006,PQ3005 Page40 : PWR engineer Del PR193,PQ51,PQ54
	10/7	Page16 :add C3779,C3780 Page29 :add C542,C530 for EMI solution & C544 change to 4.7u 0603 type Page35 :PWR engineer add PC3037,PC3038,PC3039 Page35 :PWR engineer add PC3035,PC3036
	10/11	Page8 :add R376,R381,R393,R407,R421,R434 for Dual SPI ROM Page9 :U13 power rail change to +3V Page10 :SV_DET_NC net add R250 to pull-down Page27 :add R133,R235 Page30 :C443 change to 3528 type & add C366,R340 Page31 :CN2.27 pin change to +VGACORE Page32 :add R330,R328 pull-up +3VPCU for GPUT_CLK,GPUT_DATA net
	10/14	Page20 :add C3781,C3782,R3569,R3570,R3571,R3576 Page21 :add C3783,C3784,R3577,R3578,R3579,R3581

Quanta Computer Inc. PROJECT : ZQTA/ZQSA Size: Document Number: Change list; Rev: 1A Date: Friday, November 11, 2011; Sheet 44 of 44	DOC NO.	PROJECT MODEL :	ZQTA/ZQSA	APPROVED BY:	DATE:
		PART NUMBER:		DRAWING BY:	REVISON: