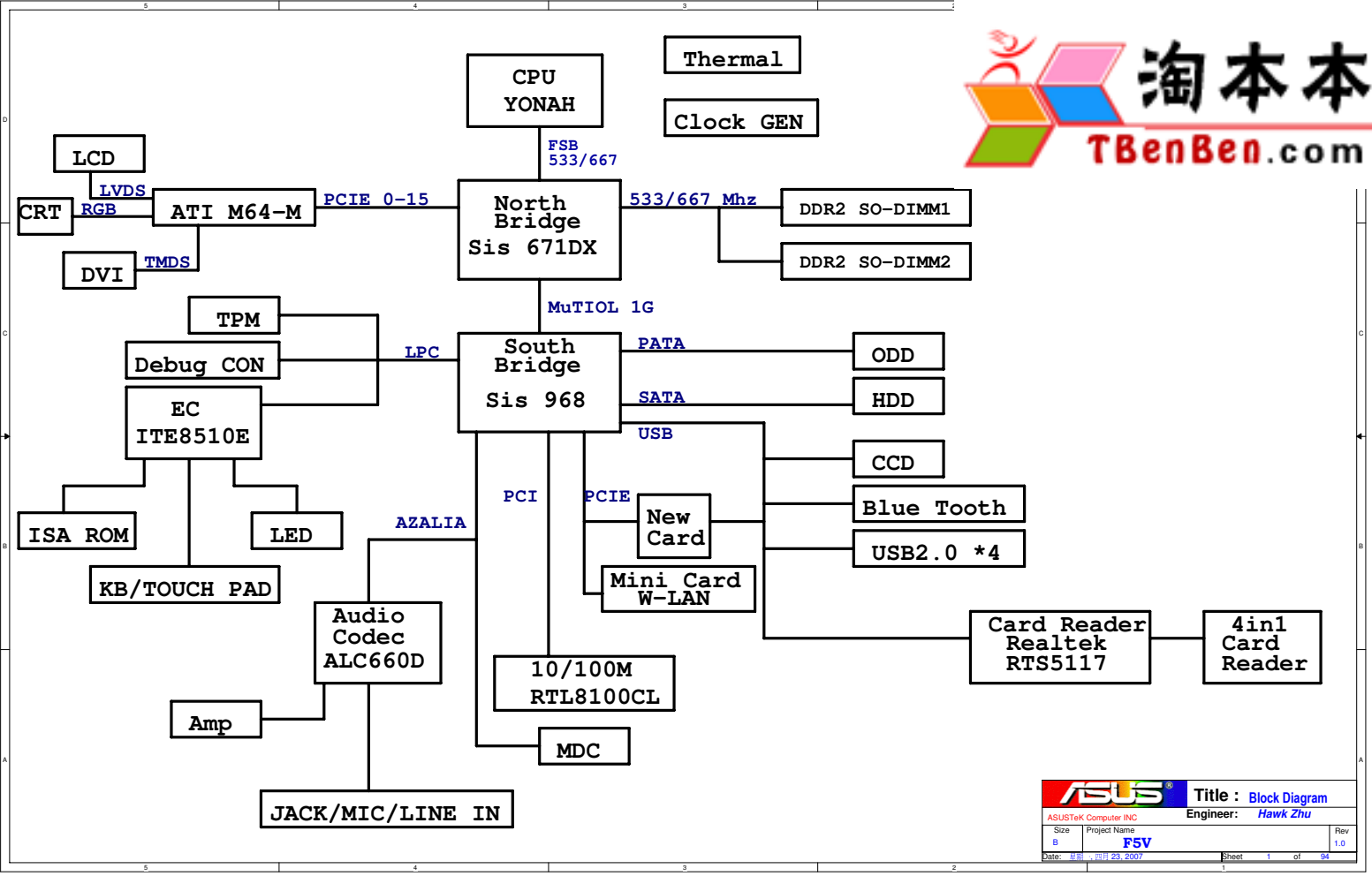
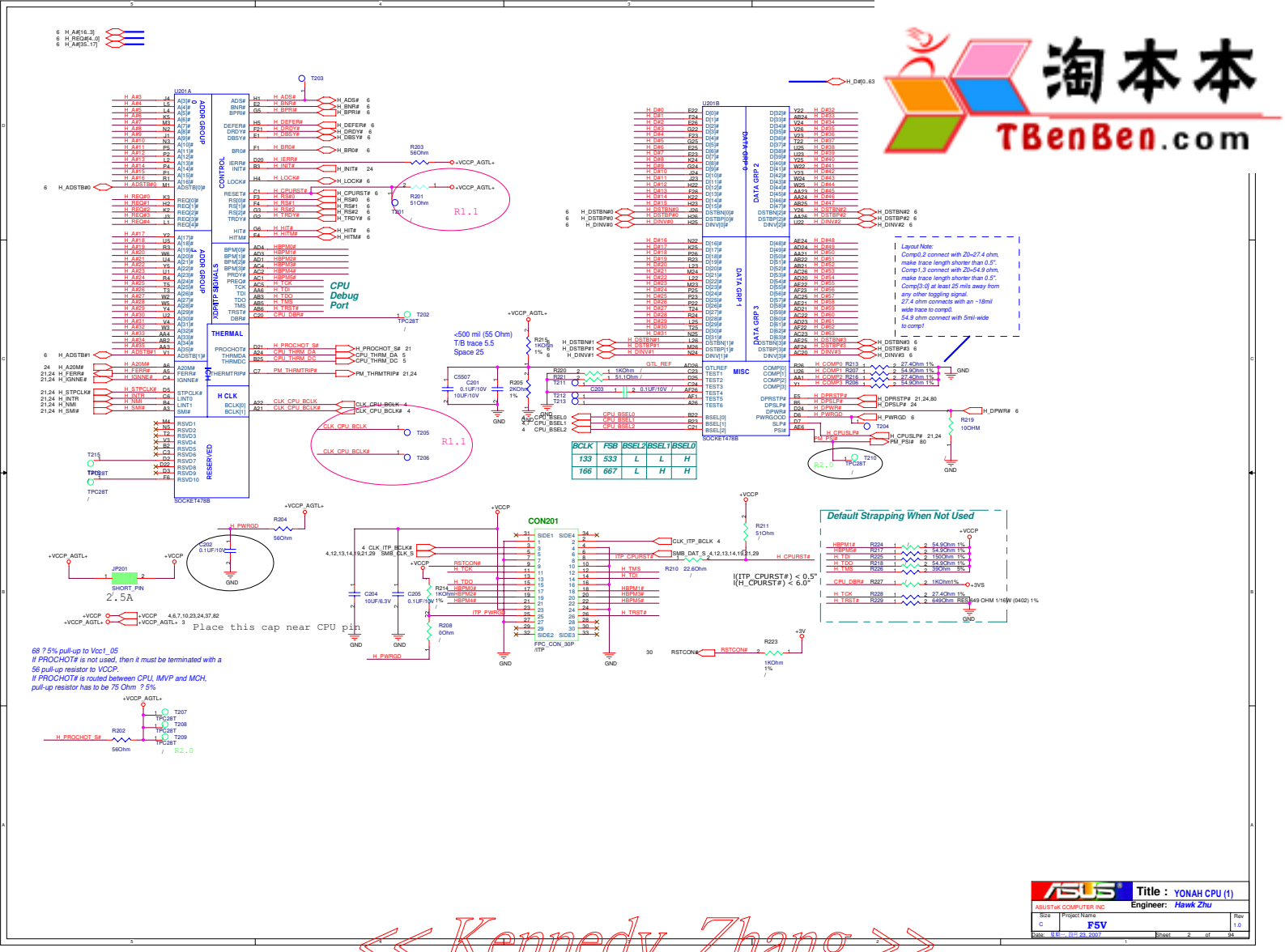
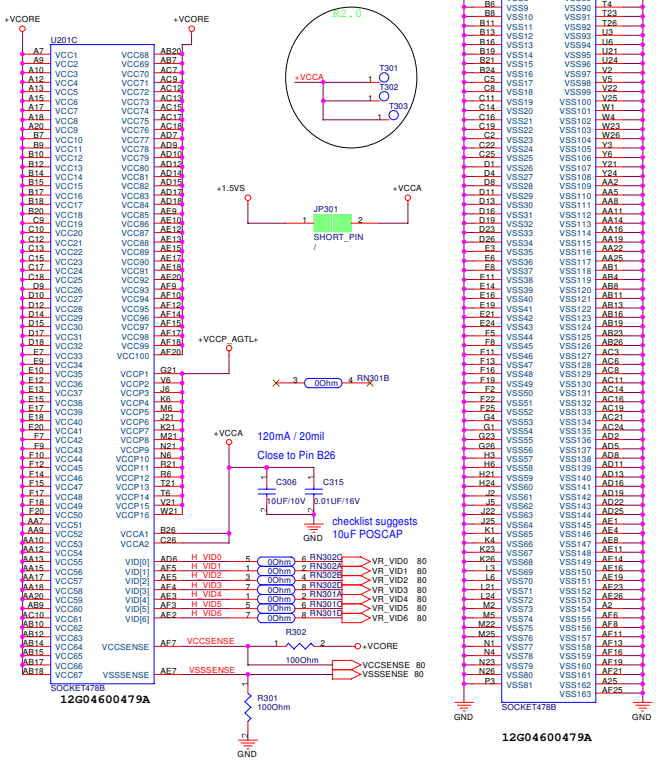


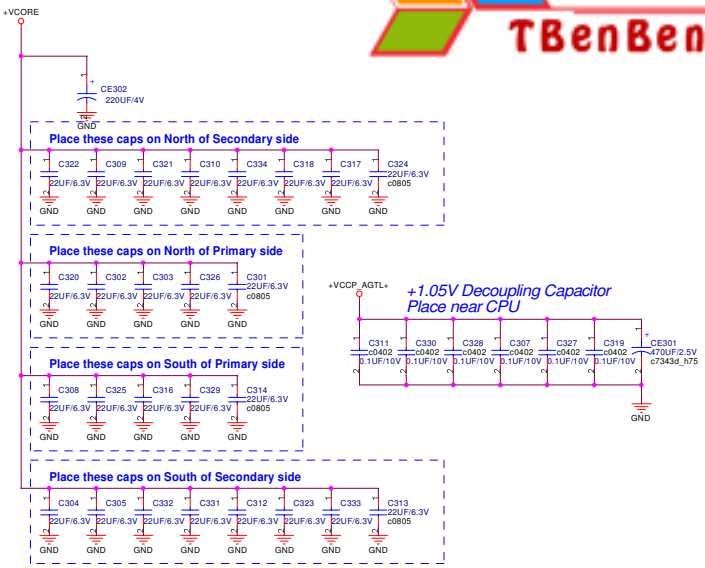

CPU Debug Port
Layout Note:
Comp0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
Comp1,3 connect with Z0=54.9 ohm, make trace length shorter than 0.5".
Comp[3:0] at least 25 mils away from any other toggling signal.
27.4 ohm connects with an ~18mil wide trace to comp0.
54.9 ohm connect with 5mil-wide to comp1
<500 mil (55 Ohm)
T/B trace 5.5
Space 25
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
CON201
Default Strapping When Not Used
Place this cap near CPU pin
68 ? 5% pull-up to Vcc1_05
If PROCHOT# is not used, then it must be terminated with a 56 pull-up resistor to VCCP.
If PROCHOT# is routed between CPU, IMVP and MCH, pull-up resistor has to be 75 Ohm ? 5%
Title : YONAH CPU (1)
Engineer: Hawk Zhu
ASUSTeK COMPUTER INC
F5V
Kennedy_Zhang

YUNAH FSB667			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

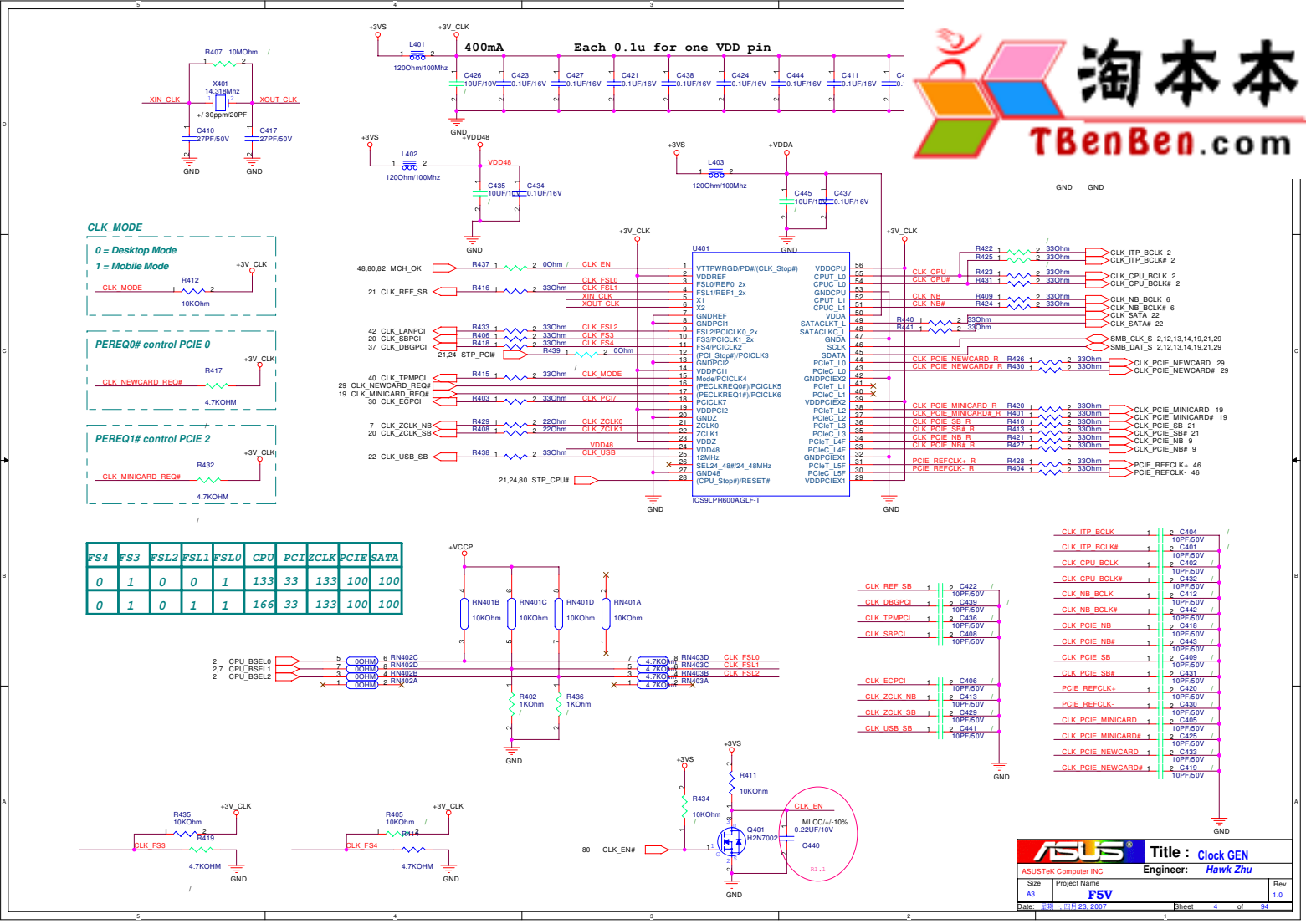
YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A



Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27.4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.



Title : Yonah CPU (2)		
ASUSTeK COMPUTER INC	Engineer: Hawk Zhu	
Size: A3	Project Name: F5V	Rev: 1.0
Date: 星期 , 四月 23, 2007	Sheet 3 of 94	



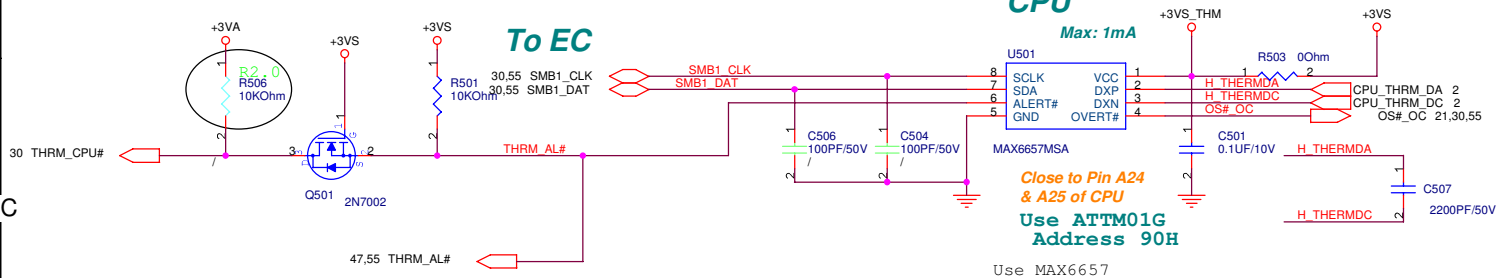
FS4	FS3	FSL2	FSL1	FSL0	CPU	PCI	ZCLK	PCIE	SATA
0	1	0	0	1	133	33	133	100	100
0	1	0	1	1	166	33	133	100	100

Thermal Sensor

To EC

CPU

Max: 1mA



Close to Pin A24 & A25 of CPU

Use ATTM01G
Address 90H

Use MAX6657
Address 98H

Route H_THERMDA and H_THERMDC on the same layer

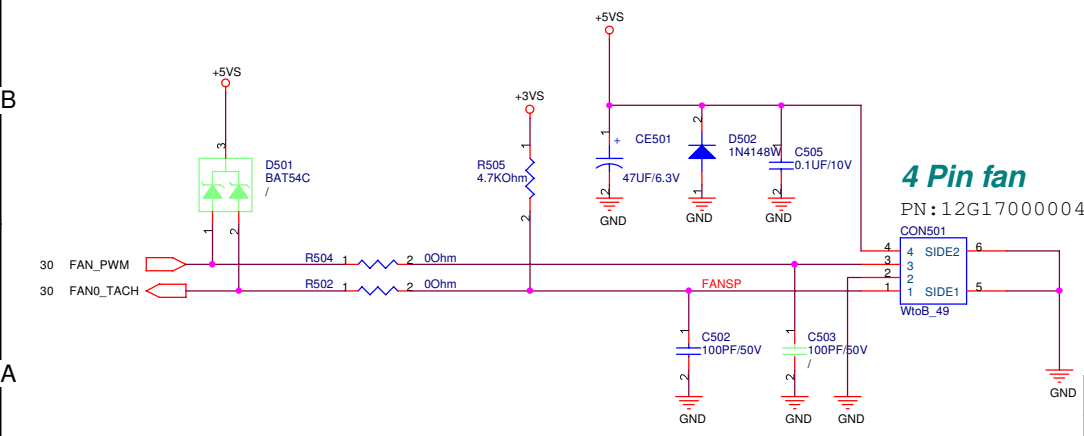
----------OTHER SIGNALS
20 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
20 mils
----------OTHER SIGNALS

Avoid FSB,Power

DC FAN Control

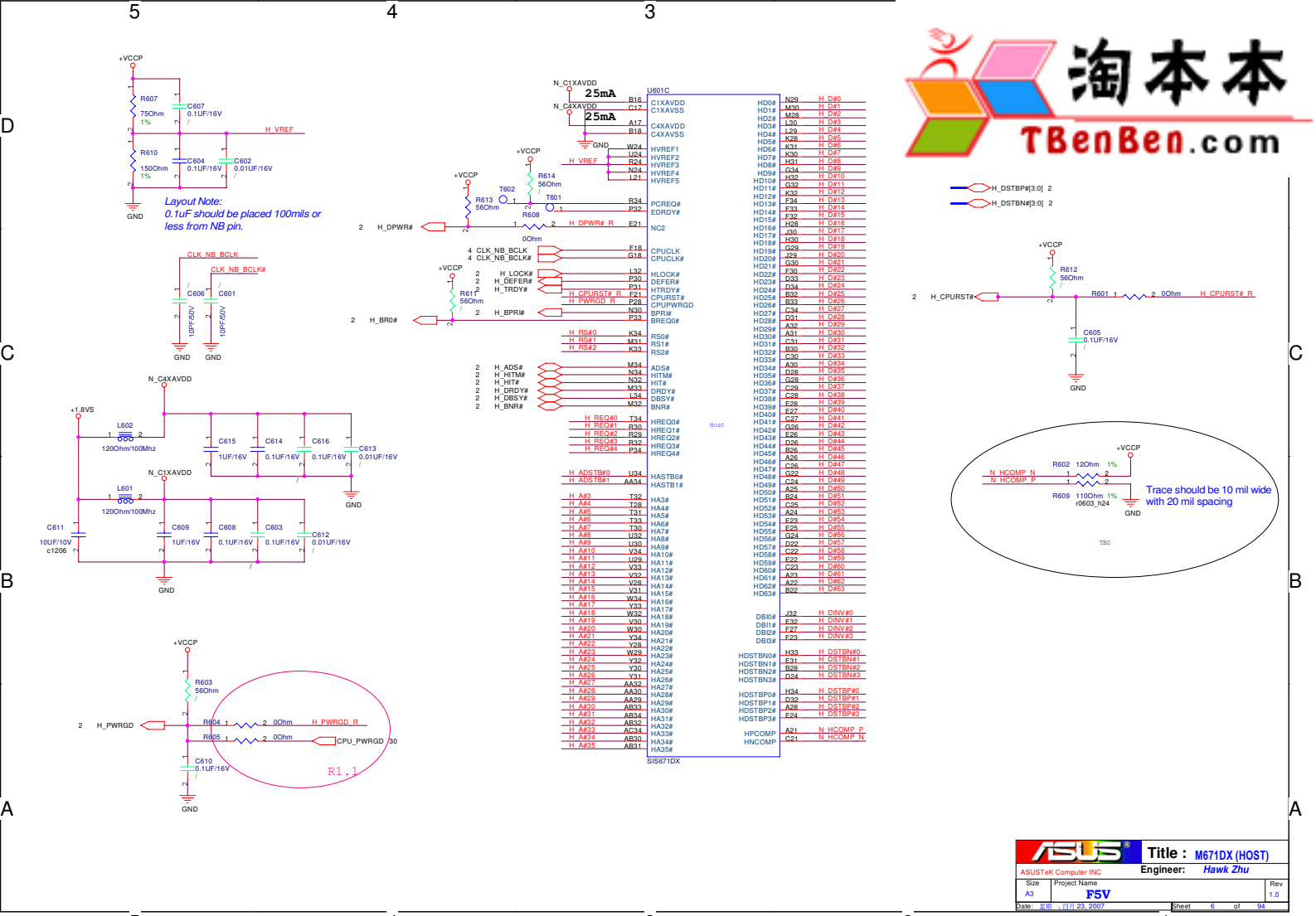
4 Pin fan

PN:12G17000004B



ASUSTeK Computer INC	Title : Thermal Sensor		
	Engineer: Hawk Zhu		
Size: A4	Project Name: F5V		Rev: 1.0
Date: 星期 , 四月 23, 2007	Sheet 5 of 94		

<< Kennedy_Zhang >>



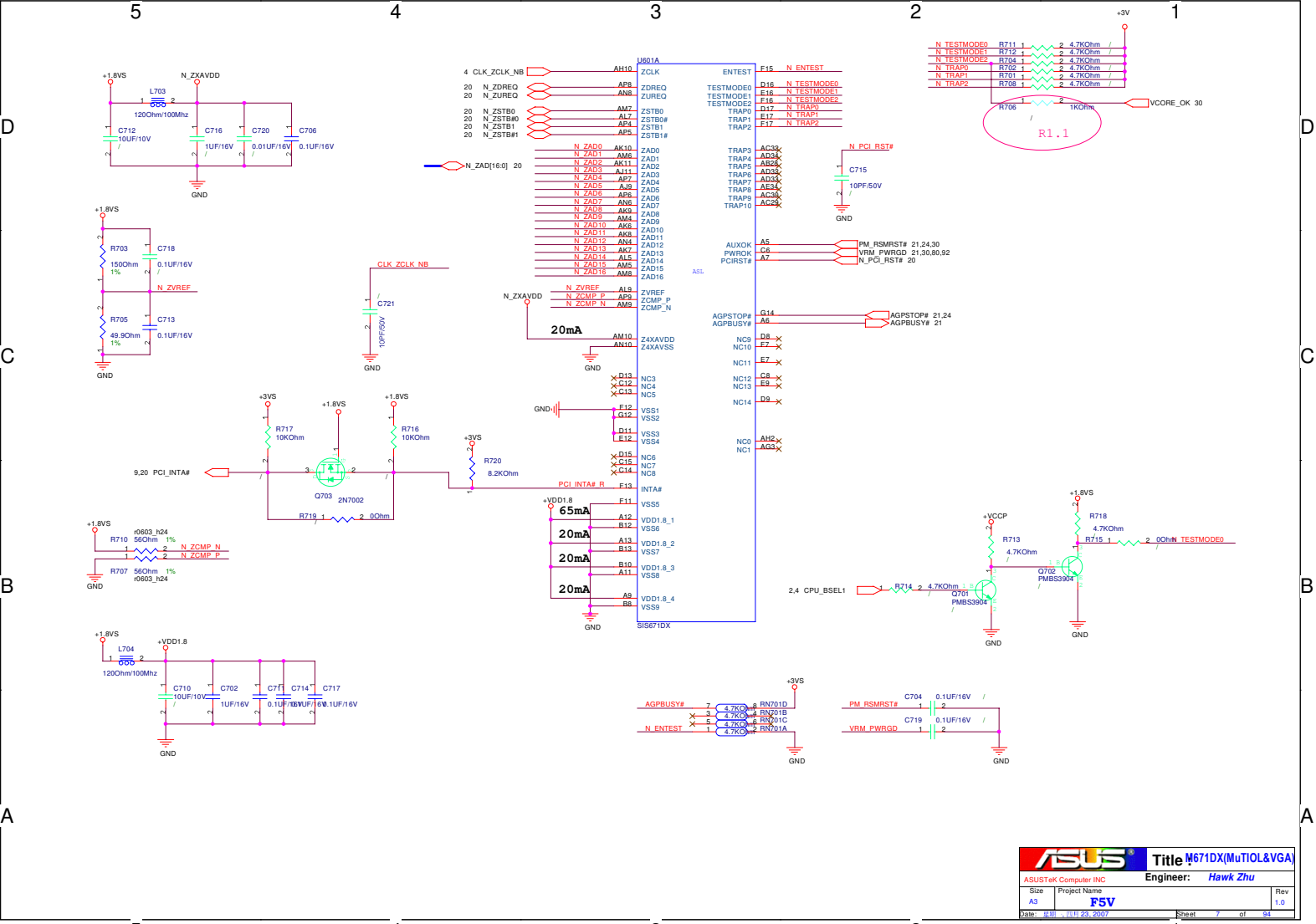
ASUSTeK Computer INC

Title : M671DX (HOST)

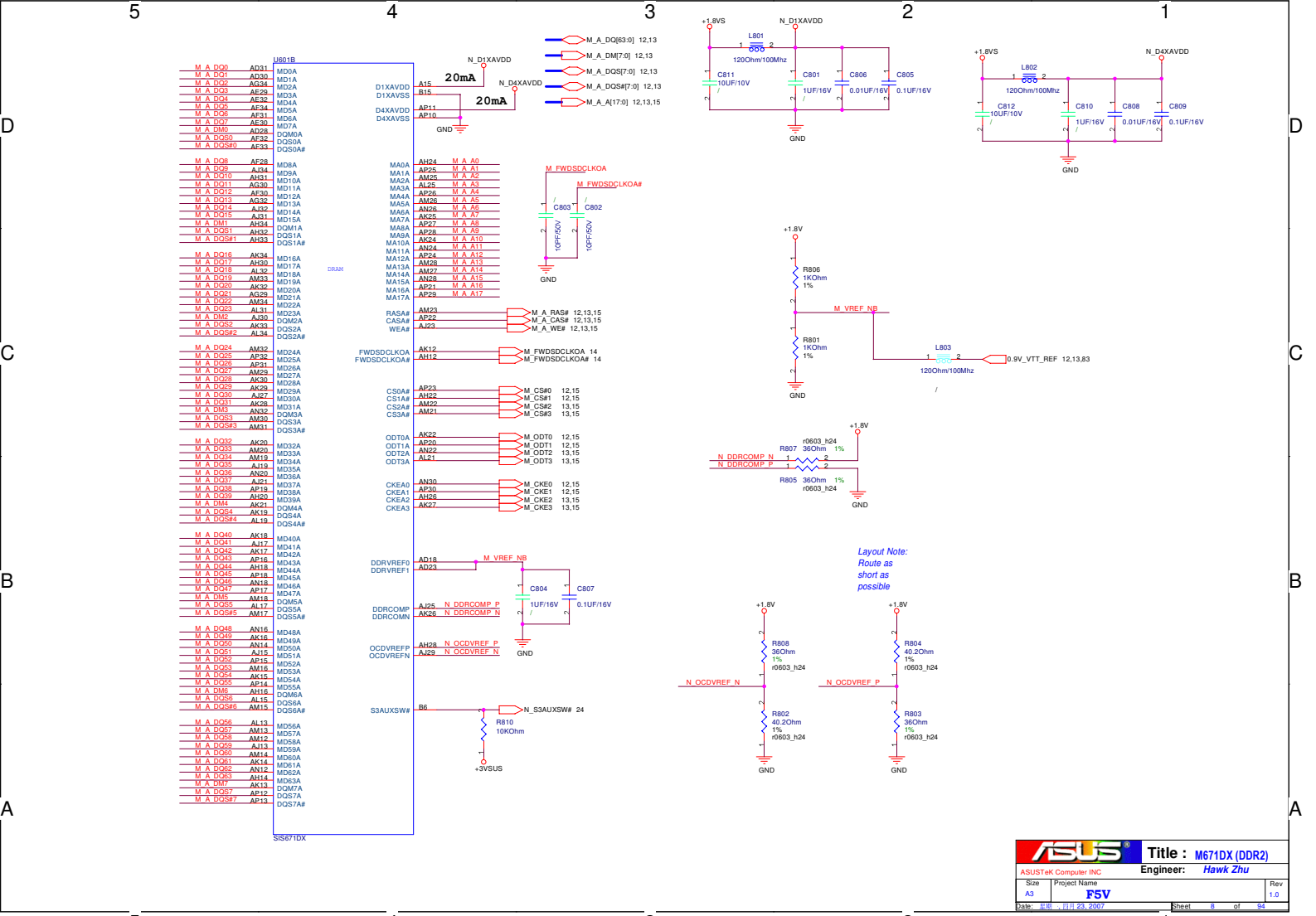
Engineer: Hawk Zhu

Size	Project Name	Rev
A3	F5V	1.0

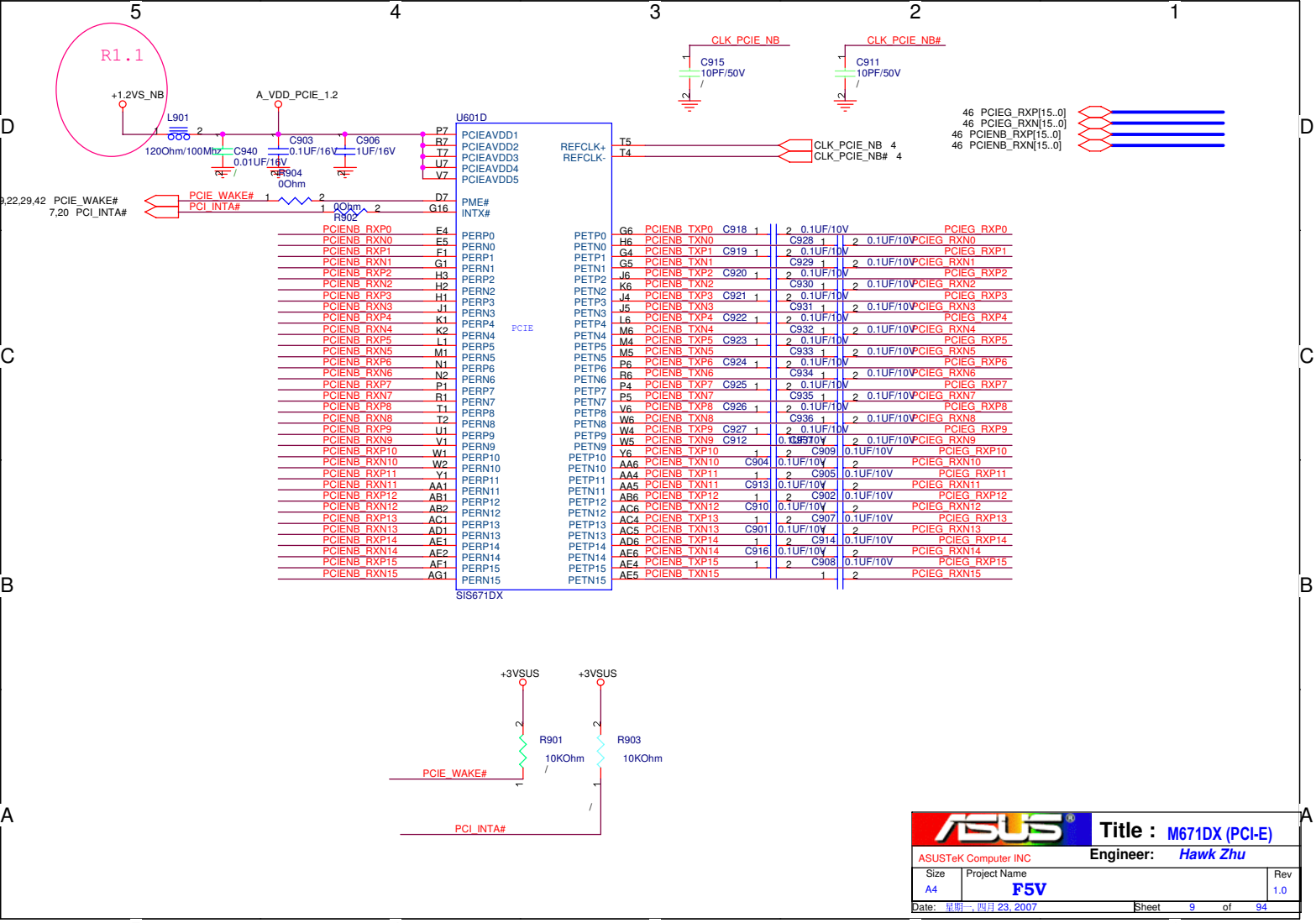
Date: 星期 , 四月 23, 2007 Sheet 6 of 94



Title	M671DX(MuTIOL&VGA)
ASUSTeK Computer INC	Engineer: Hawk Zhu
Size: A3	Project Name: F5V
Rev: 1.0	
Date: 星期一, 四月 23, 2007	Sheet 7 of 94

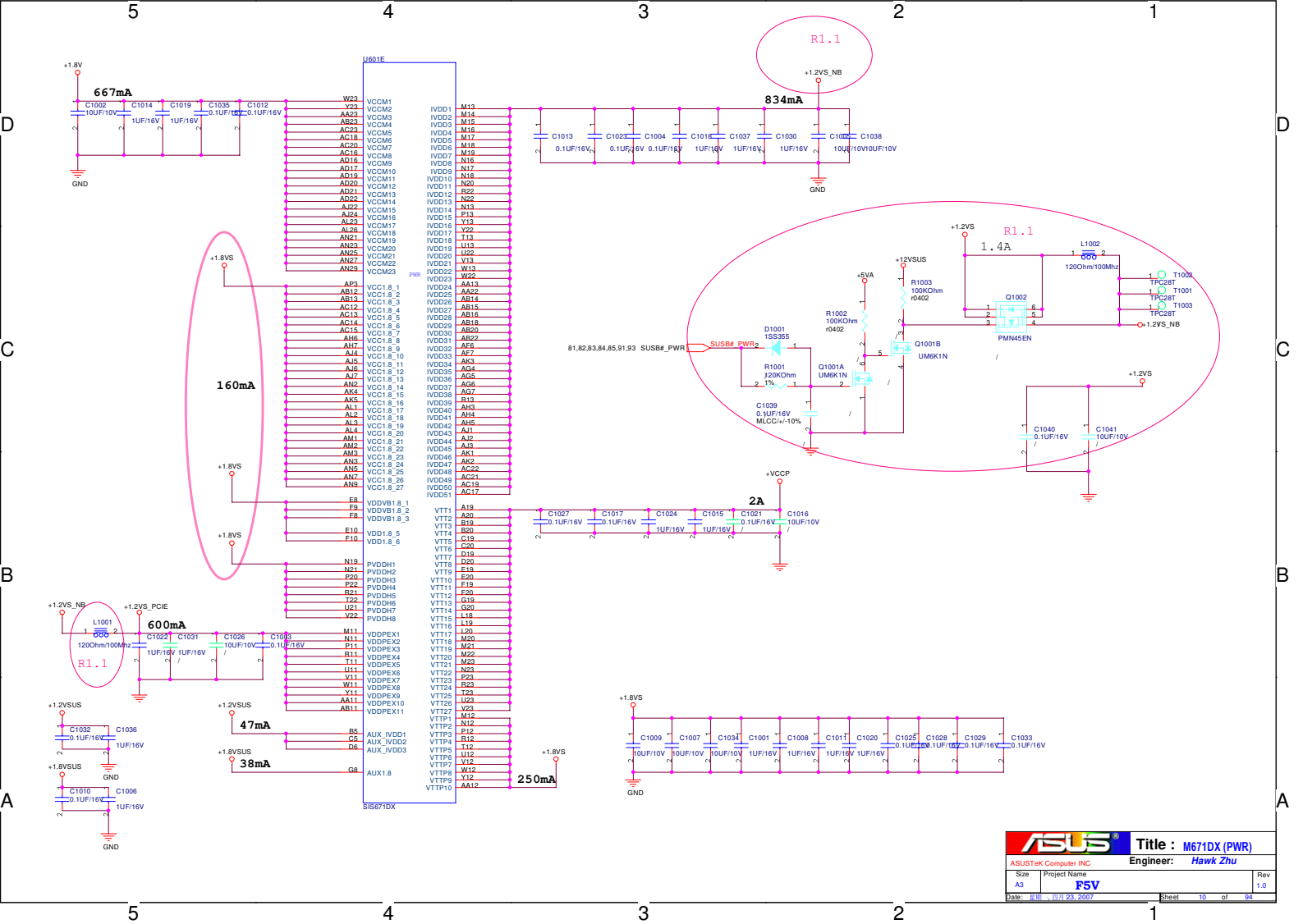


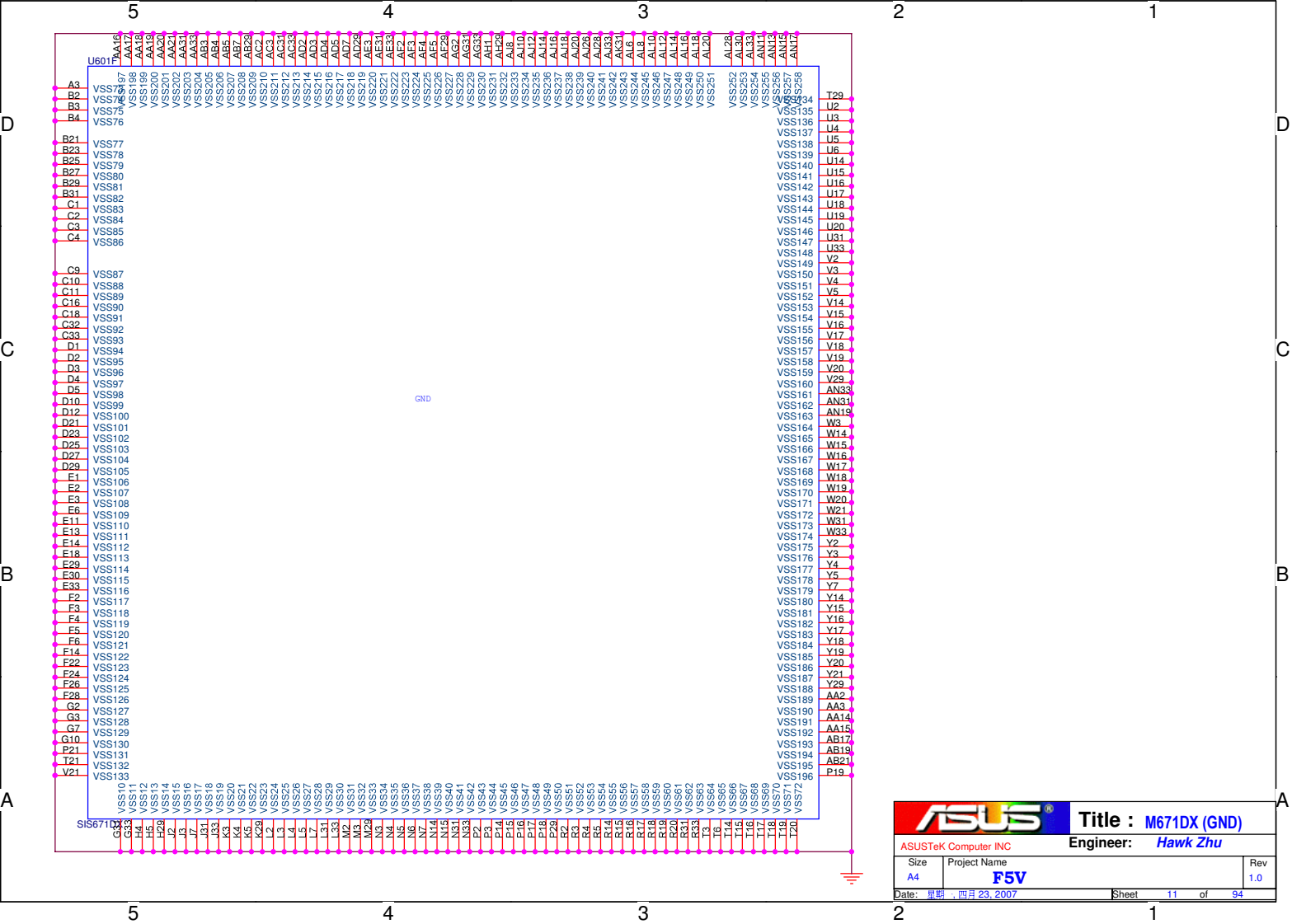
Title :	M671DX (DDR2)
ASUSTeK Computer INC	Engineer: Hawk Zhu
Size: A3	Project Name: F5V
Rev: 1.0	
Date: 星期 , 四月 23, 2007	Sheet 8 of 94



Title :	M671DX (PCI-E)	
ASUSTeK Computer INC	Engineer:	Hawk Zhu
Size: A4	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 9 of 94	

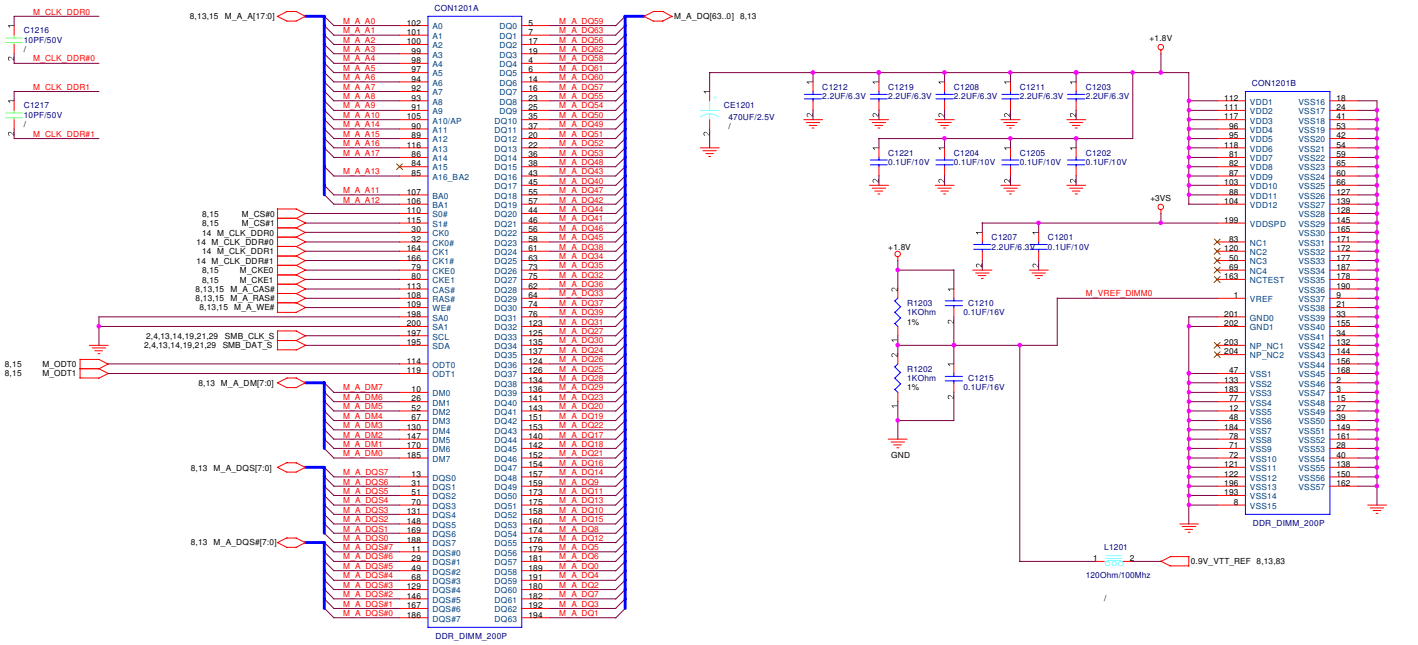
<< Kennedy_Zhang >>





ASUSTeK Computer INC	Title : M671DX (GND)		
	Engineer: Hawk Zhu		
Size: A4	Project Name: F5V		Rev: 1.0
Date: 星期 ，四月 23, 2007	Sheet 11 of 94		

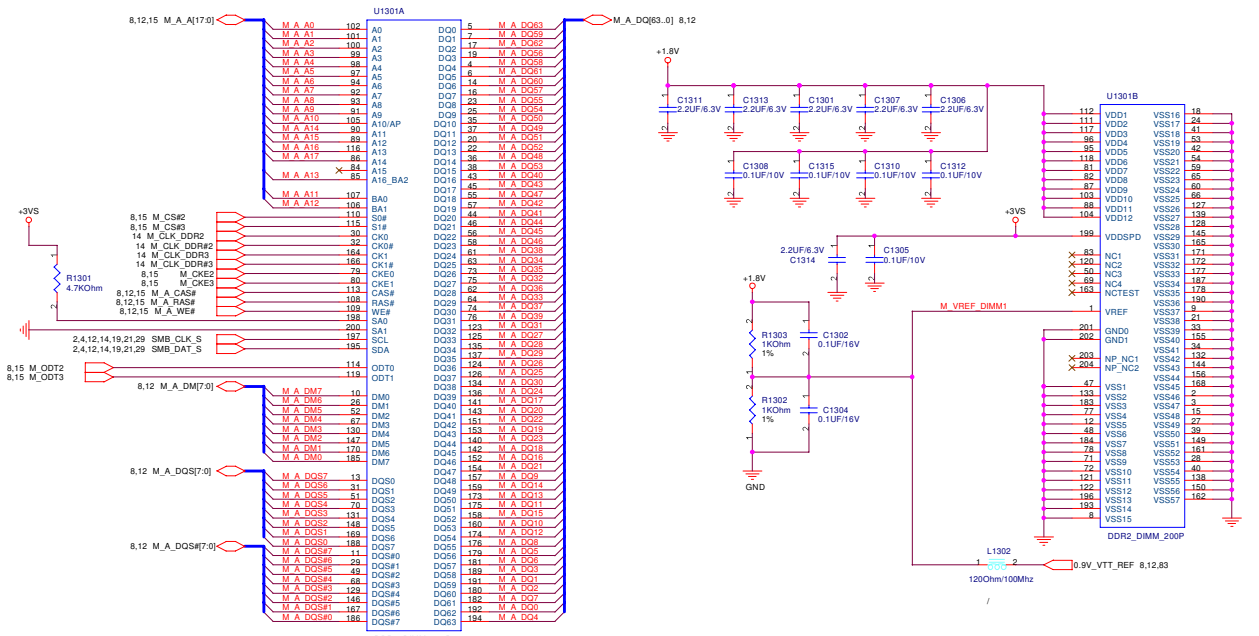
TOP



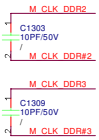
PN:12G025122006

ASUSTeK Computer INC	Title : DDR2 SO-DIMM1		
	Engineer: Hawk Zhu		
Size: A3	Project Name: F5V		Rev: 1.0
Date: 星期 , 四月 23, 2007		Sheet 12 of 94	

<< Kennedy_Zhang >>

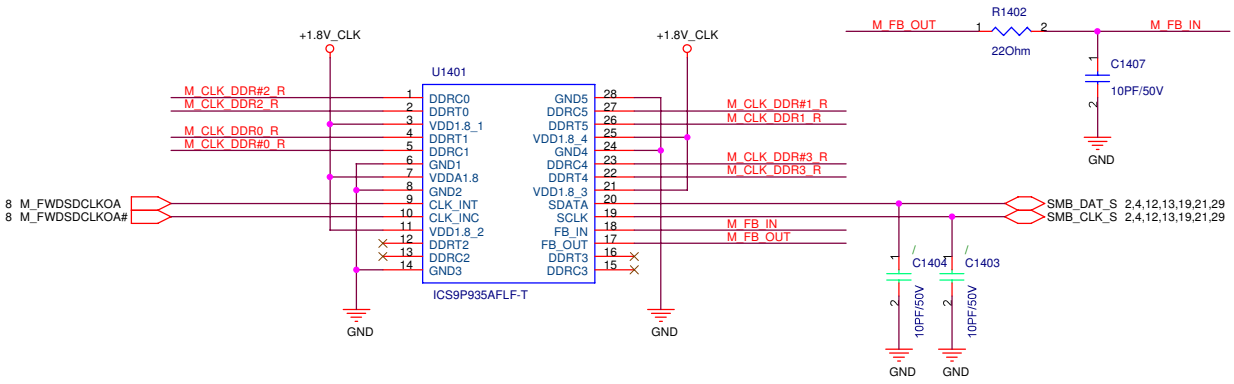


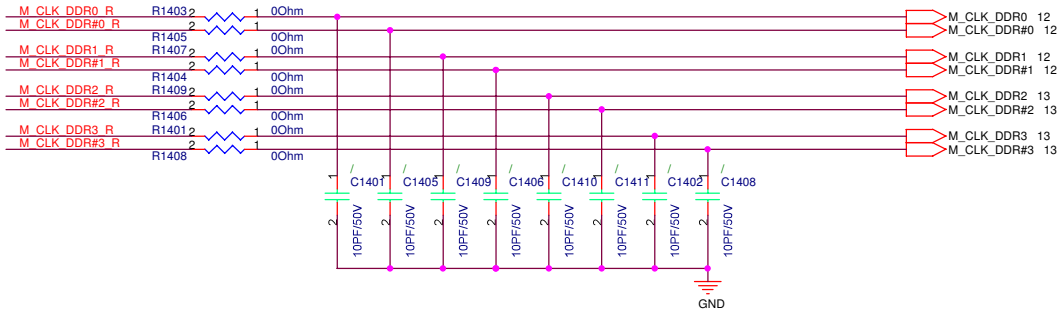
PN:12G025C22002

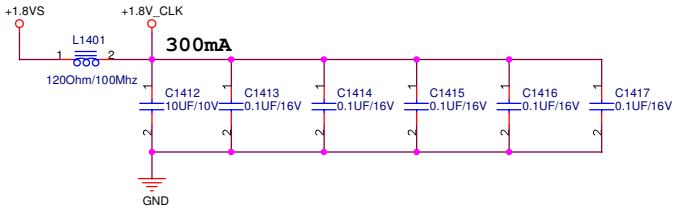


ASUSTeK Computer INC	Title : DDR2 SO-DIMM2	
	Engineer: Hawk Zhu	
Size: A3	Project Name: F5V	Rev: 1.0
Date: 星期 , 四月 23, 2007	Sheet 13 of 94	

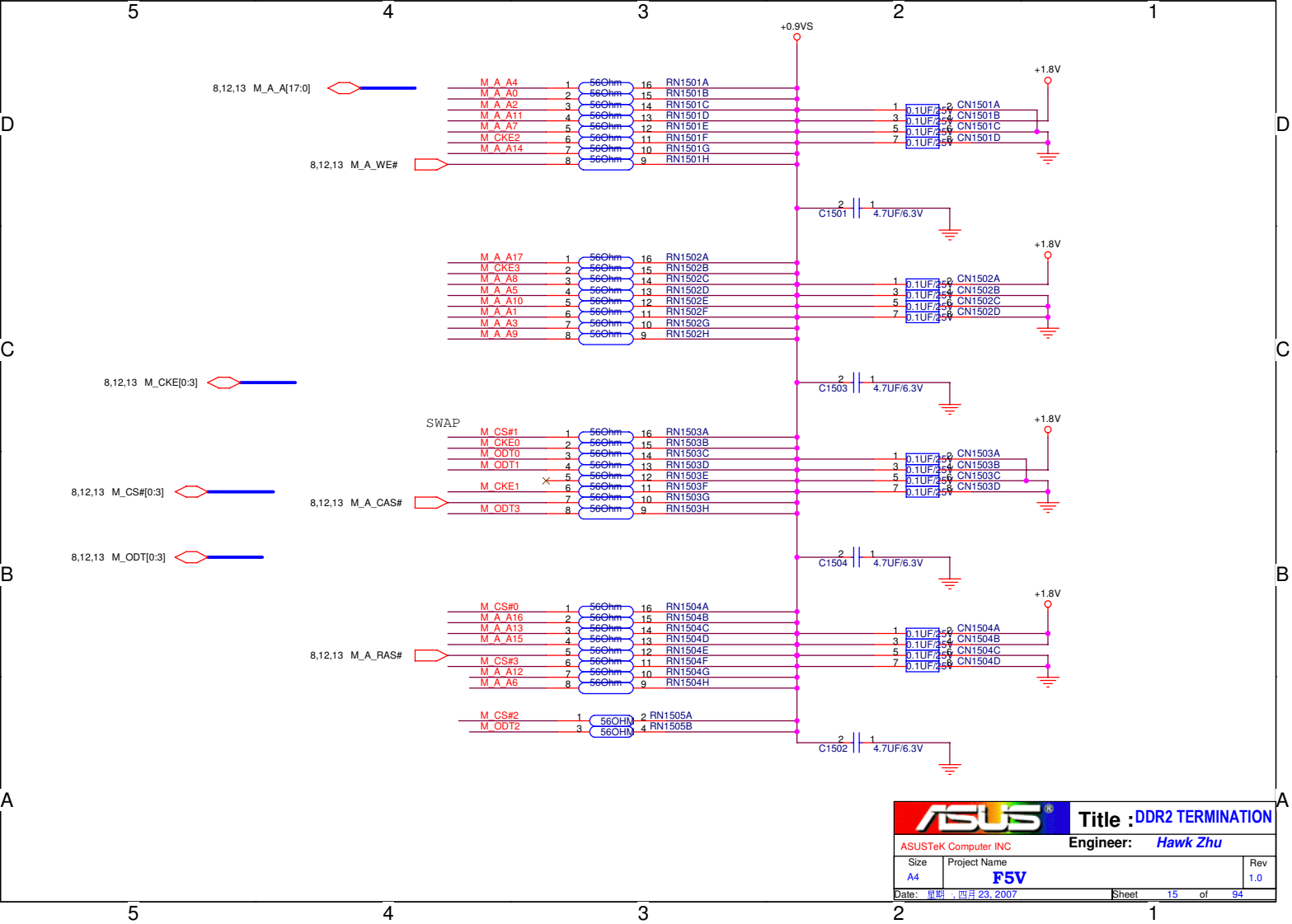
<< Kennedy_Zhang >>



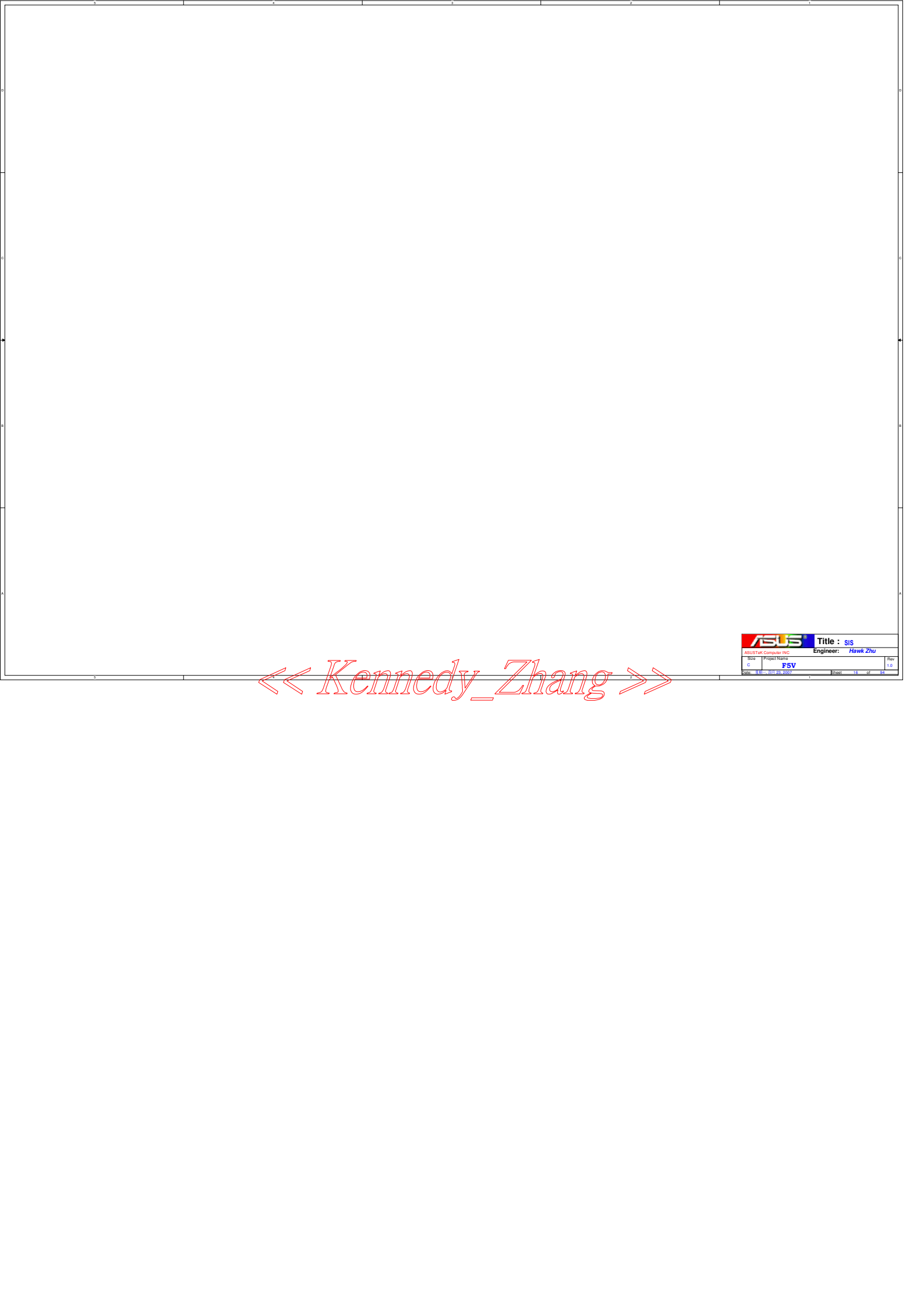




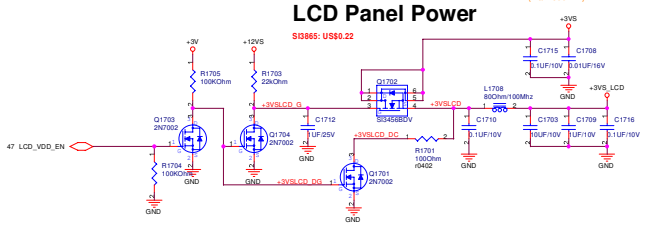
ASUSTeK Computer INC	Title : DDR2 BUFFER	
	Engineer: Hawk Zhu	
Size: A4	Project Name: F5V	Rev: 1.0
Date: 星期 , 四月 23, 2007	Sheet 14 of 94	



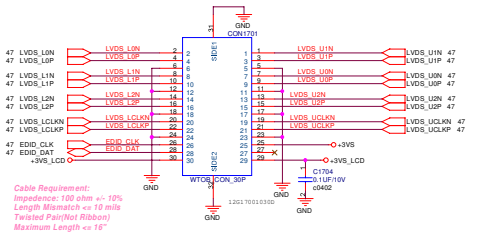
<< Kennedy_Zhang >>

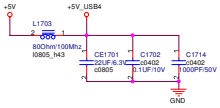

Title : SIS
ASUSTeK Computer INC
Engineer: Hawk Zhu
Size
C
Project Name
F5V
Rev
1.0
Date: 星期二, 四月 23, 2007
Sheet 18 of 94
<< Kennedy_Zhang >>

LCD Panel Power



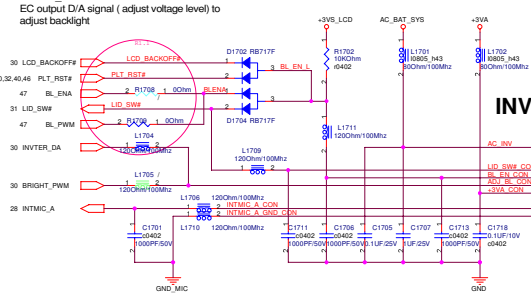
LCD LVDS Interface



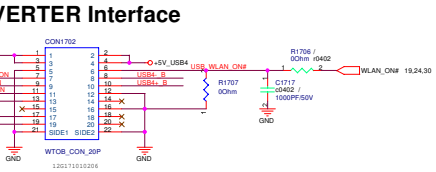


LCD Backlight Control

BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn
On/Off backlight
EC
INVTER_DA:
EC output D/A signal (adjust voltage level) to
adjust backlight

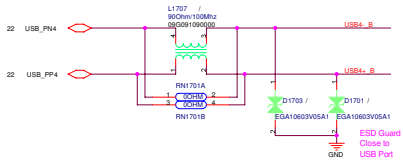


INVERTER Interface

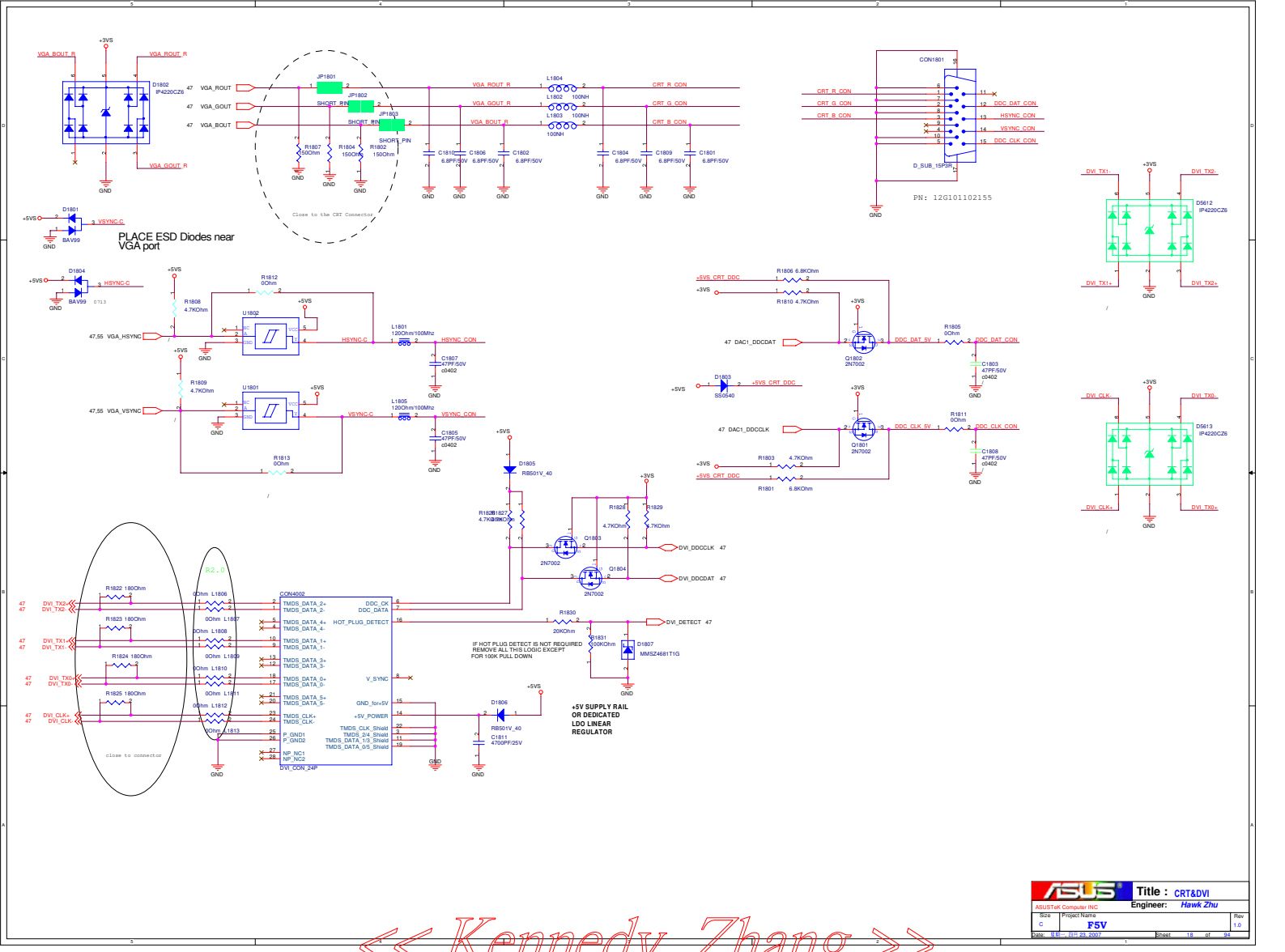


700V rms@5 mA rms
(Min. 3 mA rms)6 mA
rms(Max. 6.5 mA
rms)

USB4 For CMOS Camera



Title : LVDS
ASUSTeK Computer INC
Engineer: Hawk Zhu
Size C
Project Name F5V
Rev 1.0
Date: 星期二, 四月 23, 2007
Sheet 17 of 94



ASUSTeK Computer INC

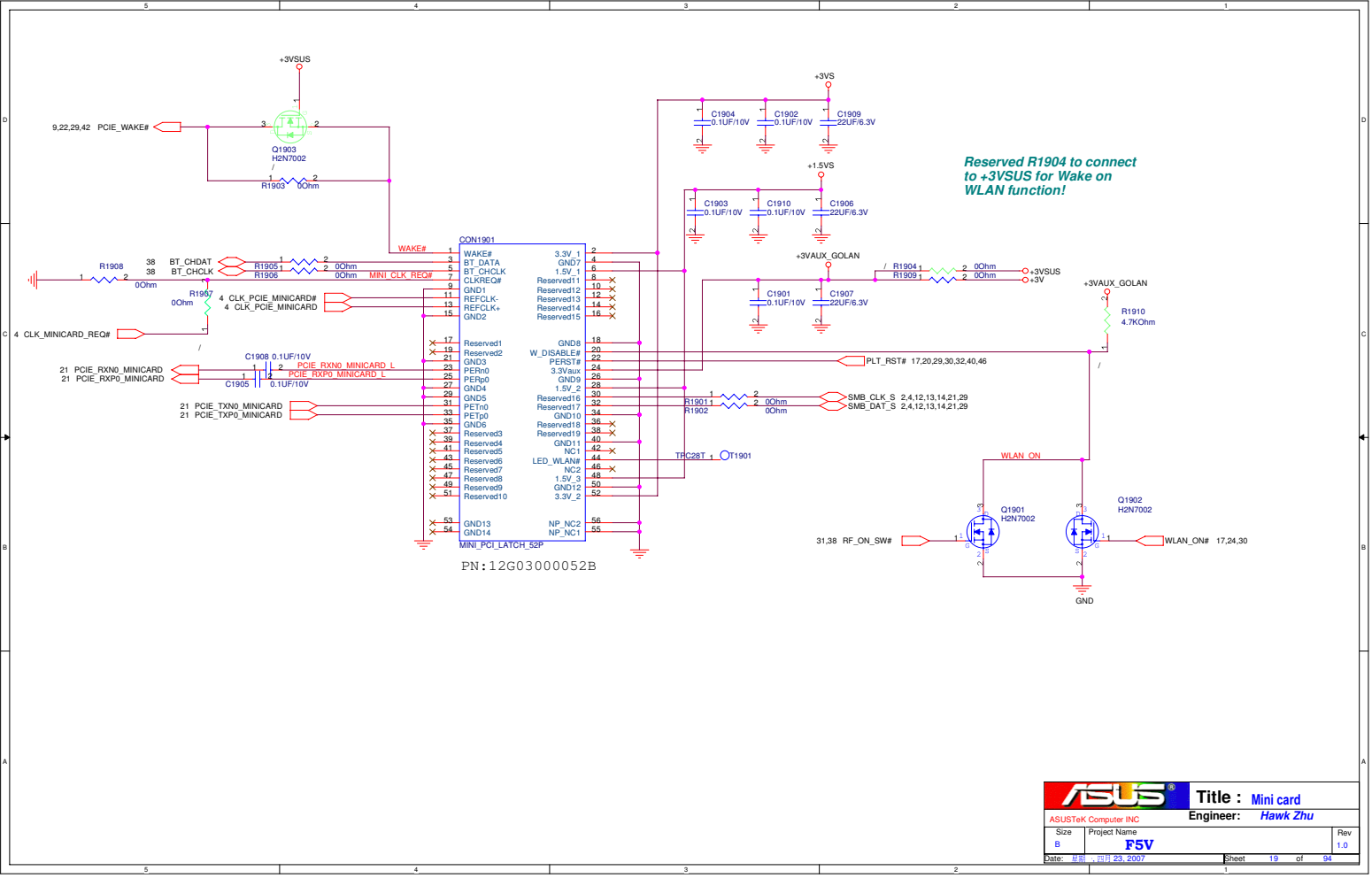
Title : CRT&DVI

Engineer: Hawk Zhu

Size	Project Name	Rev
C	F5V	1.0

Date: 星期二, 四月 23, 2007 Sheet 18 of 94

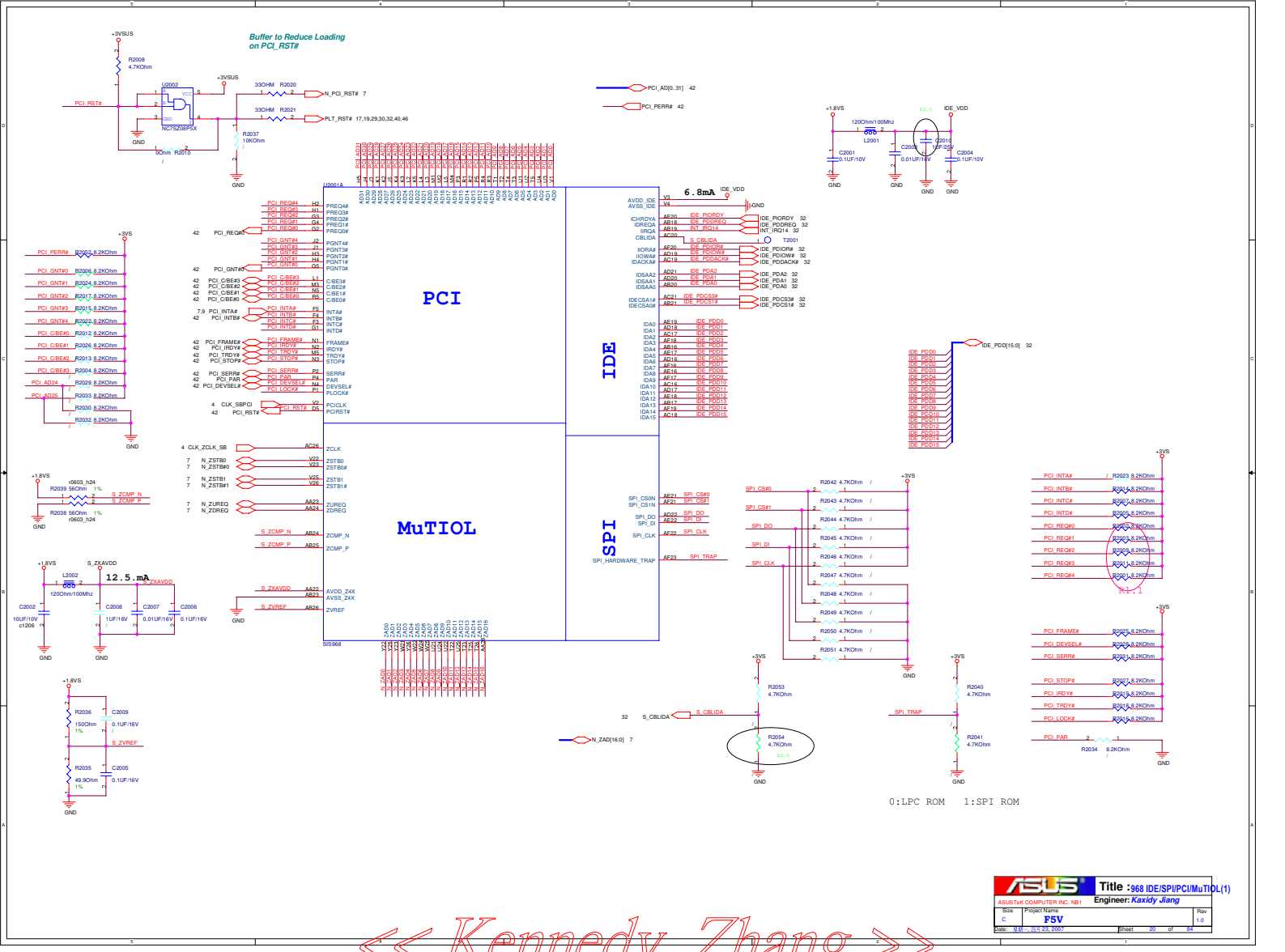
<< Kennedy_Zhang >>



PN:12G03000052B

ASUSTeK Computer INC	Title : Mini card	
	Engineer: Hawk Zhu	
Size: B	Project Name: F5V	Rev: 1.0
Date: 星期 一, 四月 23, 2007	Sheet 19 of 94	

<< Kennedy_Zhang >>



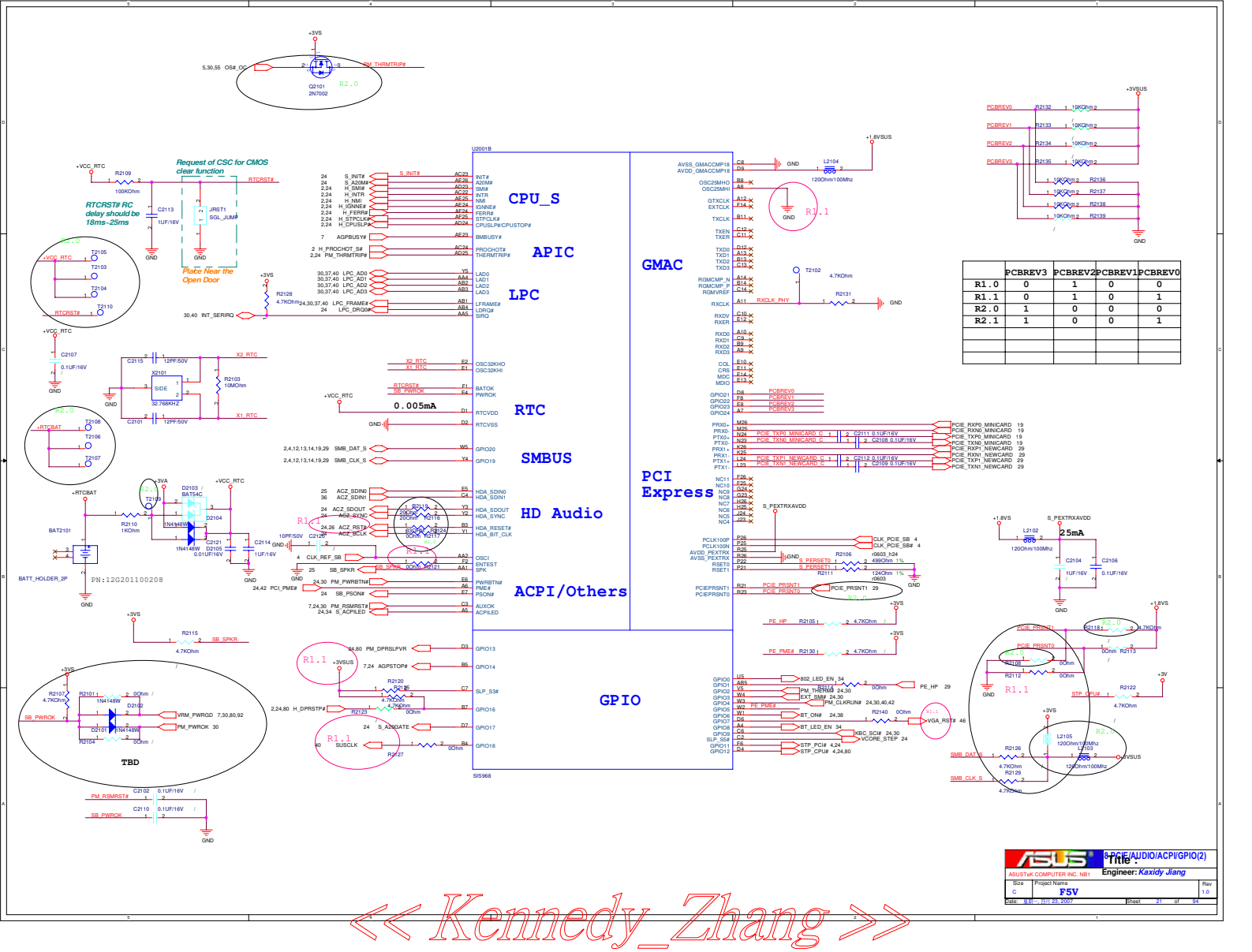
Title : 968 IDE/SPI/PCI/MuTIOL(1)

ASUSTeK COMPUTER INC. NB1 Engineer: Kaxidy Jiang

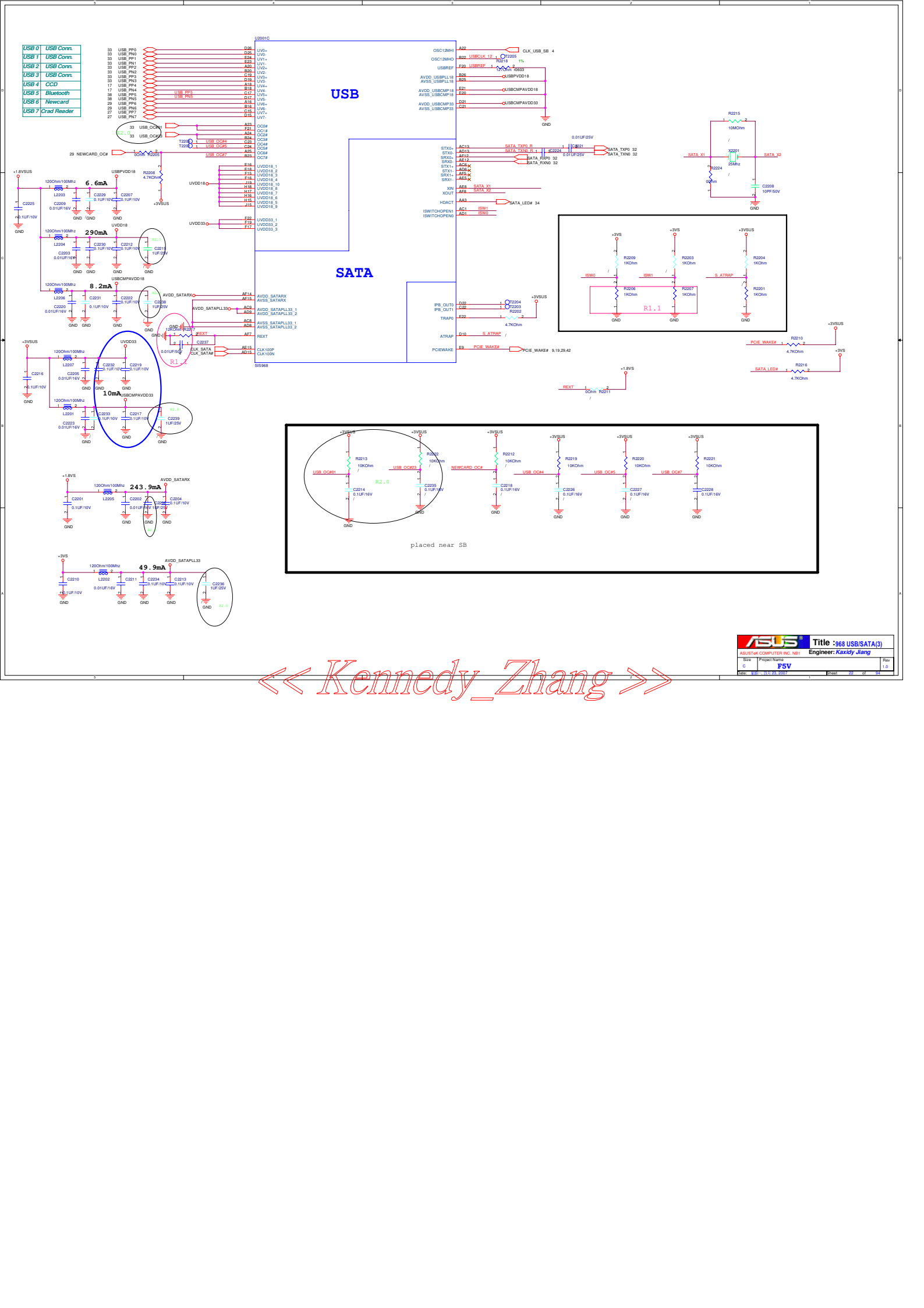
Size	Project Name	Rev
C	F5V	1.0

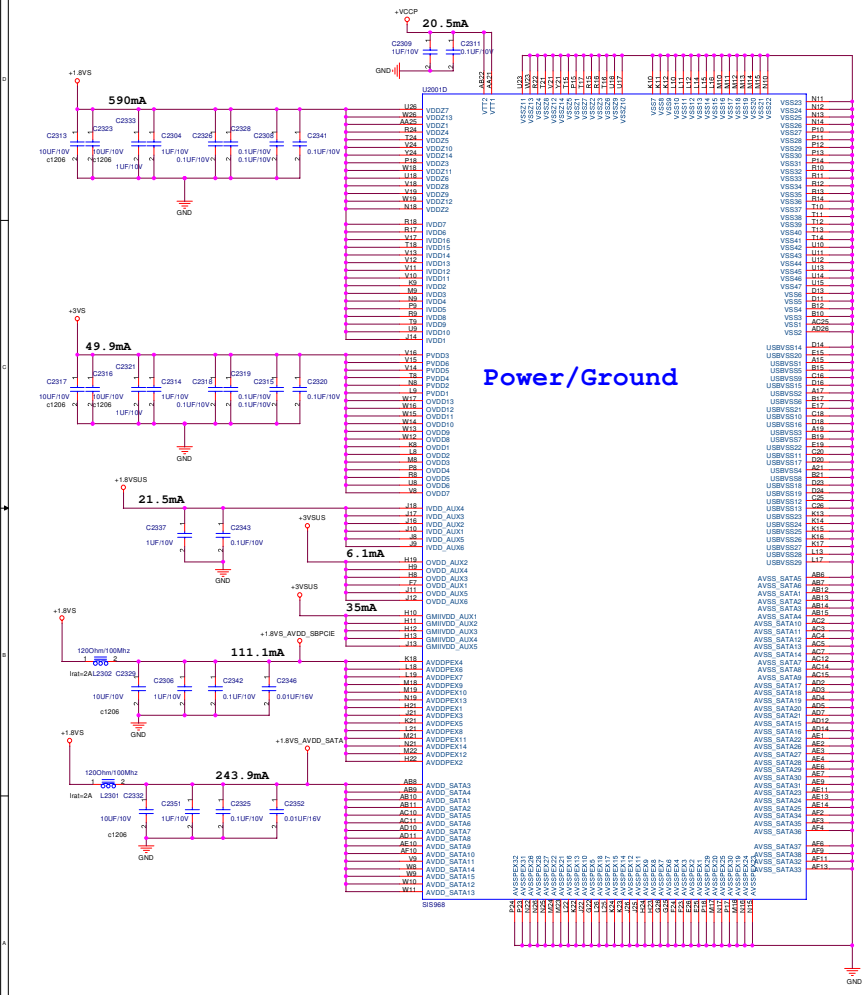
Date: 星期一, 四月 23, 2007 Sheet 20 of 54

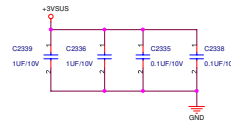
<< Kennedy_Zhang >>

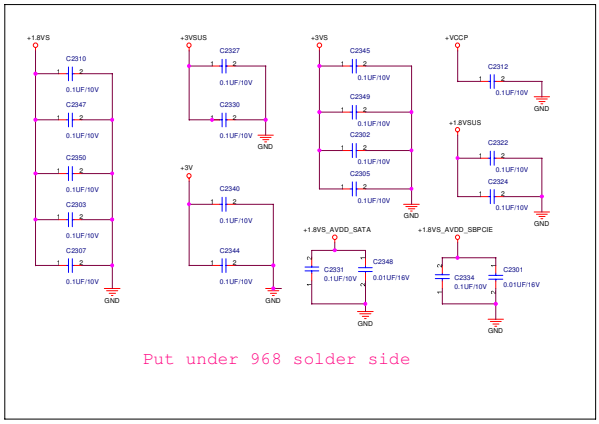


	PCBREV3	PCBREV2	PCBREV1	PCBREV0
R1.0	0	1	0	0
R1.1	0	1	0	1
R2.0	1	0	0	0
R2.1	1	0	0	1


USB 0 USB Conn.
USB 1 USB Conn.
USB 2 USB Conn.
USB 3 USB Conn.
USB 4 CCD
USB 5 Bluetooth
USB 6 Newcard
USB 7 Crad Reader
USB
SATA
SIS968
6.6mA
290mA
8.2mA
10mA
243.9mA
49.9mA
placed near SB
Title :968 USB/SATA(3)
ASUSTeK COMPUTER INC. NB1
Engineer: Kaxidy Jiang
F5V
Date: 三月 25, 2007
Sheet 22 of 64
<< Kennedy_Zhang >>

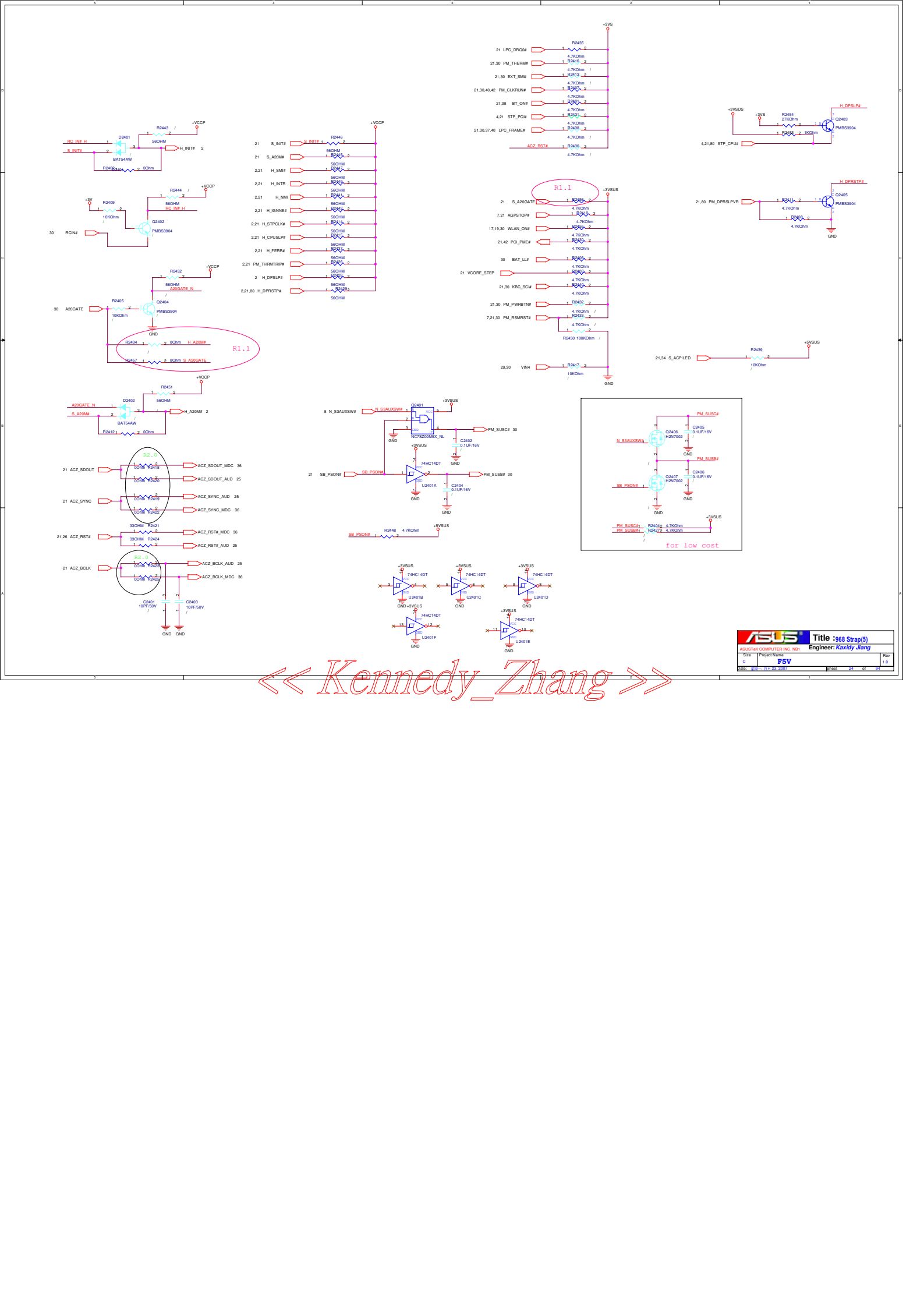


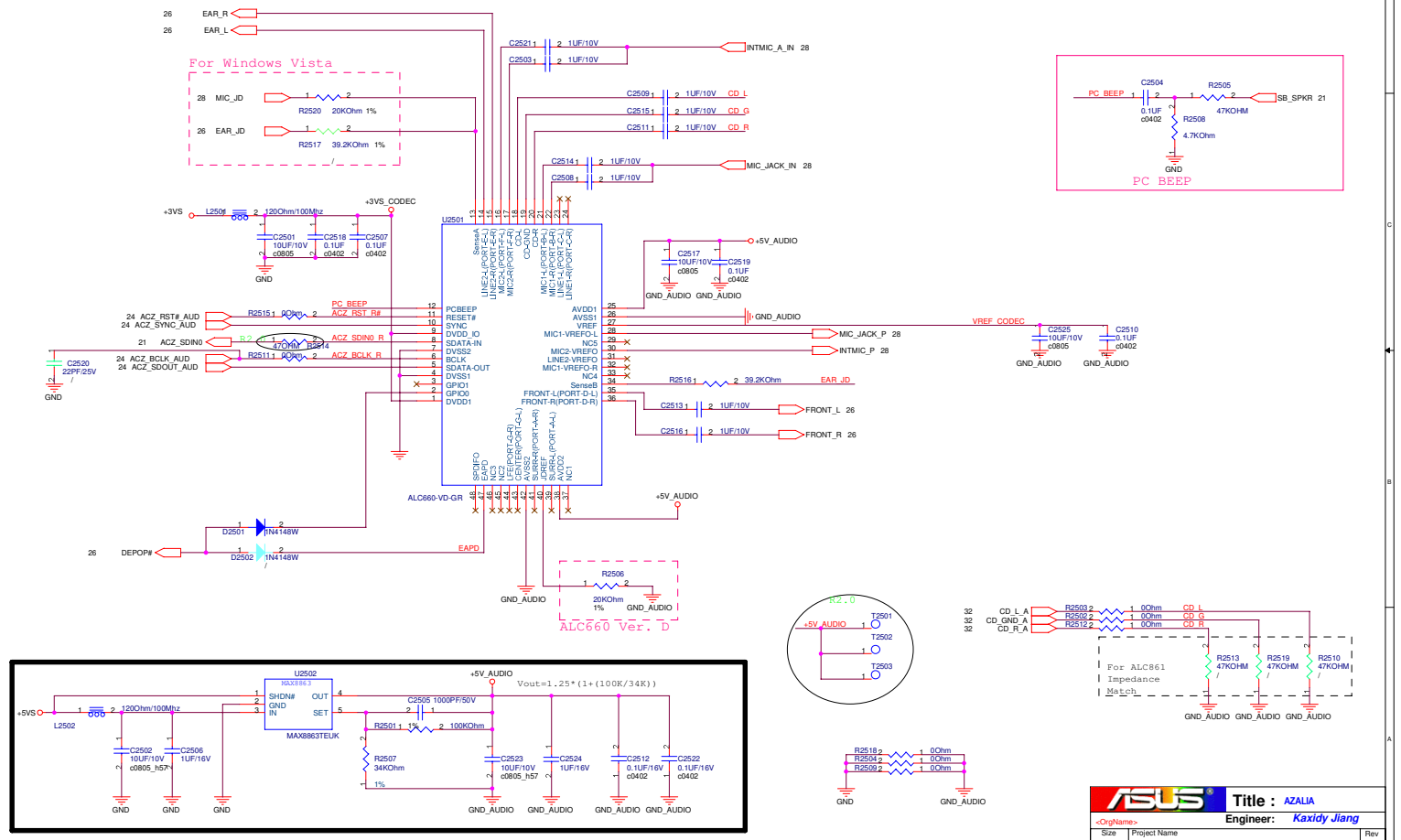


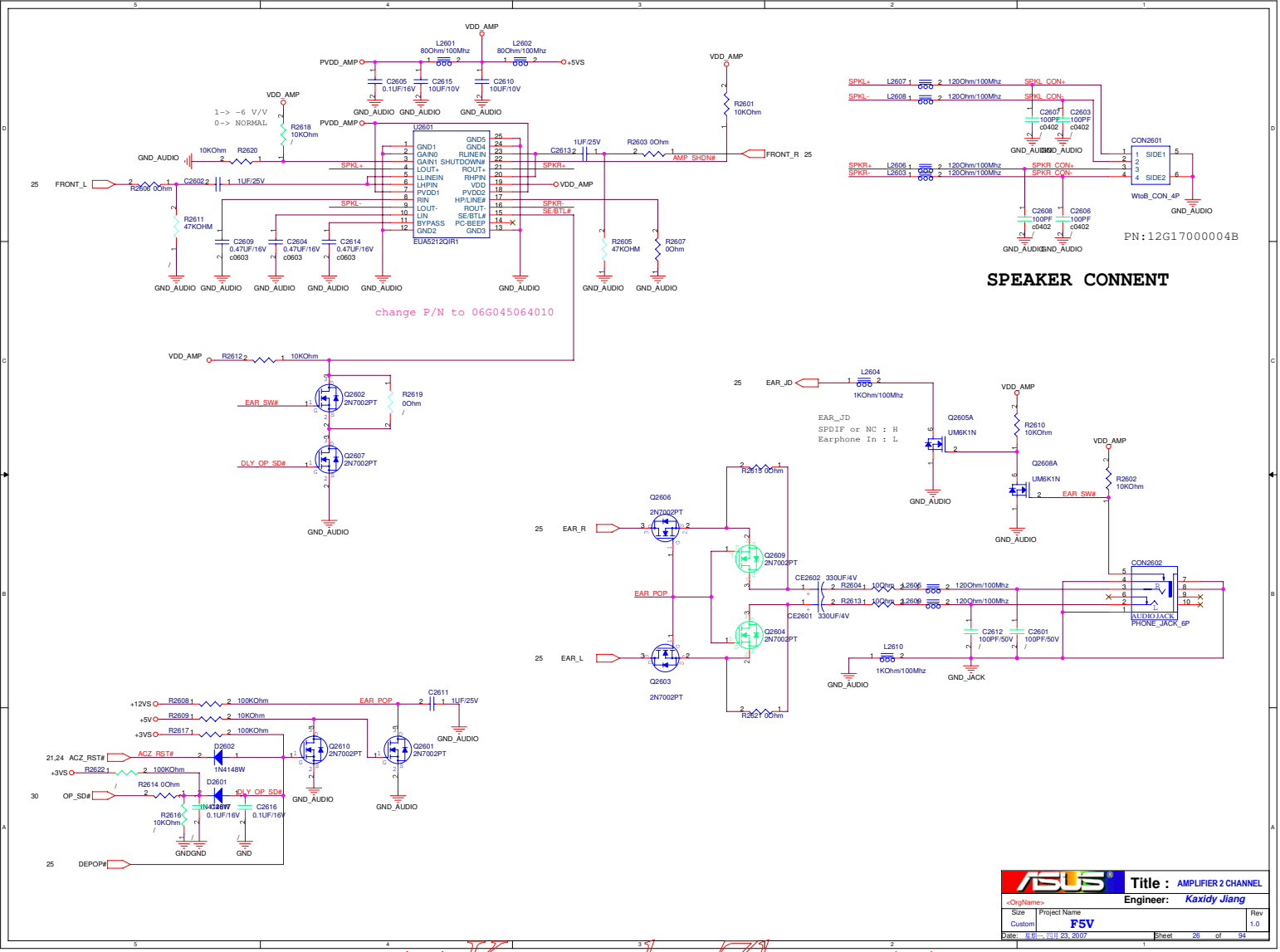


ASUSTeK COMPUTER INC. NB1		Title : 968 Power(4)	
		Engineer: Kaxidy Jiang	
Size: C	Project Name: F5V		Rev: 1.0
Date: 8月 - 13日 25, 2007		Sheet 23 of 64	

<< Kennedy_Zhang >>


21 LPC_DRQ0#
21,30 PM_THERM#
21,30 EXT_SMI#
21,30,40,42 PM_CLKRUN#
21,38 BT_ON#
4,21 STP_PCI#
21,30,37,40 LPC_FRAME#
ACZ_RST#
4.7KOhm
4,21,80 STP_CPU#
H_DPSLP#
Q2403
PMBS3904
21,80 PM_DPRSLPVR
H_DPRSTP#
Q2405
21 S_A20GATE
7,21 AGPSTOP#
17,19,30 WLAN_ON#
21,42 PCI_PME#
30 BAT_LL#
21 VCORE_STEP
21,30 KBC_SCI#
21,30 PM_PWRBTN#
7,21,30 PM_RSMRST#
R2450 100KOhm
29,30 VIN4
10KOhm
21,34 S_ACPILED
+5VSUS
R1.1
+3VSUS
+3VS
+VCCP
GND
21 S_INIT#
21 S_A20M#
2,21 H_SMI#
2,21 H_INTR
2,21 H_NMI
2,21 H_IGNNE#
2,21 H_STPCLK#
2,21 H_CPUSLP#
2,21 H_FERR#
2,21 PM_THRMTRIP#
2 H_DPSLP#
2,21,80 H_DPRSTP#
56OHM
D2401
BAT54AW
RC_IN#_H
S_INIT#
H_INIT#
R2402 0Ohm
+3V
10KOhm
Q2402
30 RCIN#
30 A20GATE
Q2404
A20GATE_N
S_A20M#
H_A20M#
R2434 0Ohm H_A20M#
R2457 0Ohm S_A20GATE
D2402
R2412 0Ohm
21 ACZ_SDOUT
21 ACZ_SYNC
21,26 ACZ_RST#
21 ACZ_BCLK
ACZ_SDOUT_MDC 36
ACZ_SDOUT_AUD 25
ACZ_SYNC_AUD 25
ACZ_SYNC_MDC 36
ACZ_RST#_MDC 36
ACZ_RST#_AUD 25
ACZ_BCLK_AUD 25
ACZ_BCLK_MDC 36
33OHM
C2401 10PF/50V
C2403 10PF/50V
8 N_S3AUXSW#
Q2401
NC7SZ00M5X_NL
PM_SUSC# 30
C2402 0.1UF/16V
21 SB_PSON#
74HC14DT
U2401A
PM_SUSB# 30
C2404 0.1UF/16V
SB_PSON#
R2446 4.7KOhm
U2401B
U2401C
U2401D
U2401F
U2401E
PM_SUSC#
PM_SUSB#
Q2406 H2N7002
Q2407 H2N7002
C2405 0.1UF/16V
C2406 0.1UF/16V
R2404 4.7KOhm
R2427 4.7KOhm
for low cost
ASUSTeK COMPUTER INC. NB1
Title : 968 Strap(5)
Engineer: Kaxidy Jiang
Size C
Project Name F5V
Rev 1.0
Date: 星期一, 11月 26, 2007
Sheet 24 of 94
<< Kennedy_Zhang >>

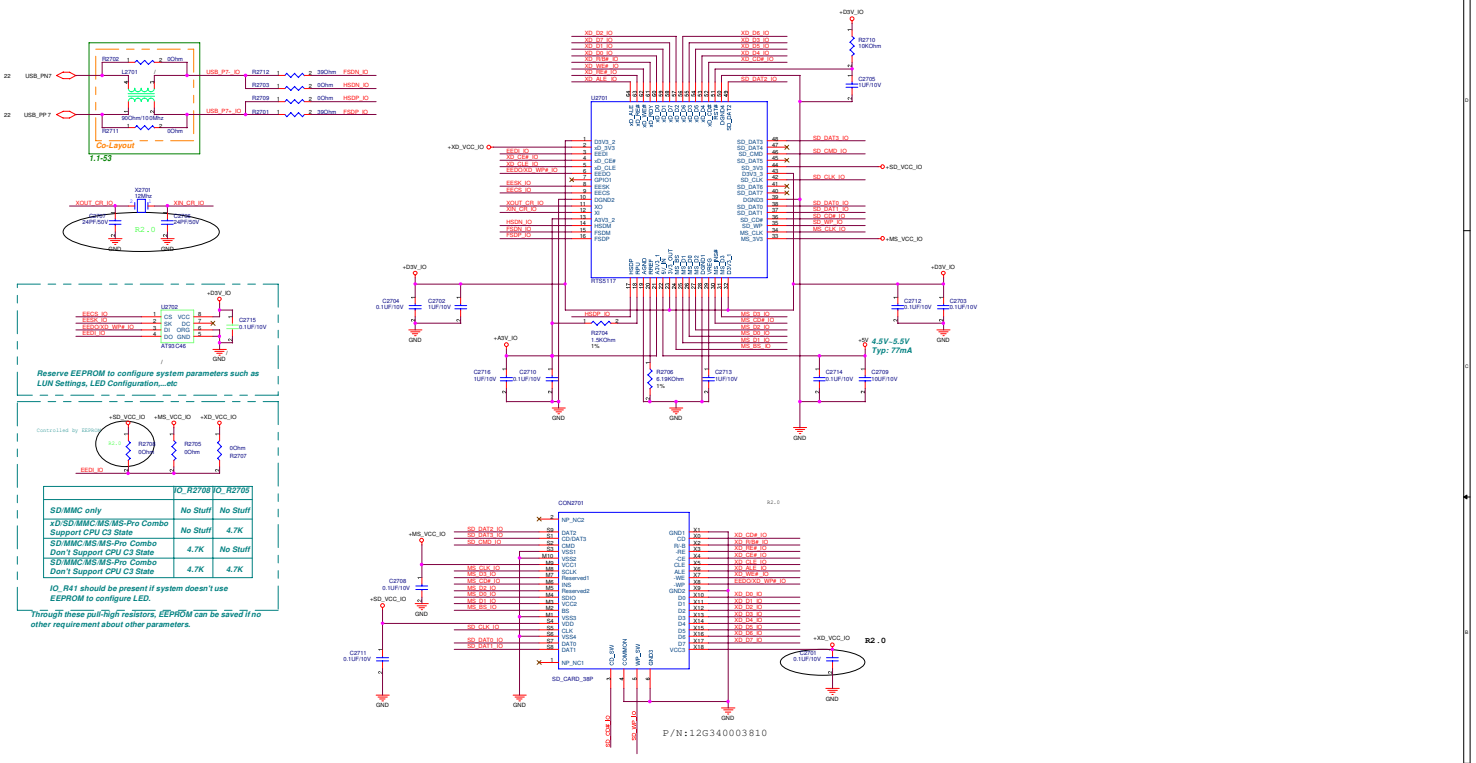




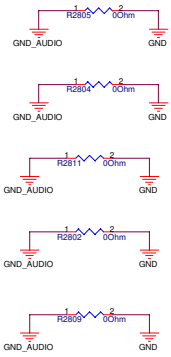
<OrgName>		Engineer: Kaxidy Jiang	
Size: Custom	Project Name: F5V		Rev: 1.0
Date: 星期一, 四月 23, 2007		Sheet 26 of 94	

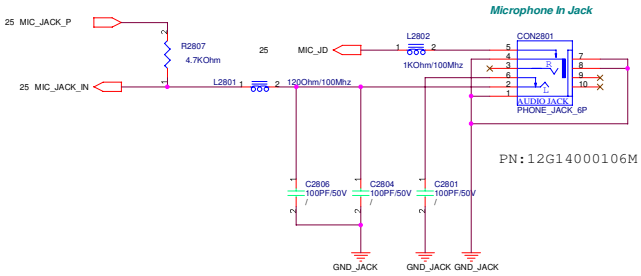
Title : AMPLIFIER 2 CHANNEL

<< Kennedy_Zhang >>



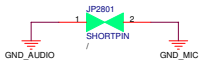
<< Kennedy_Zhang >>



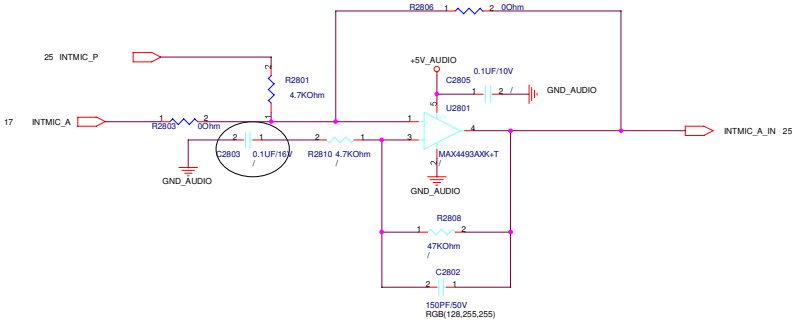


PN:12G14000106M

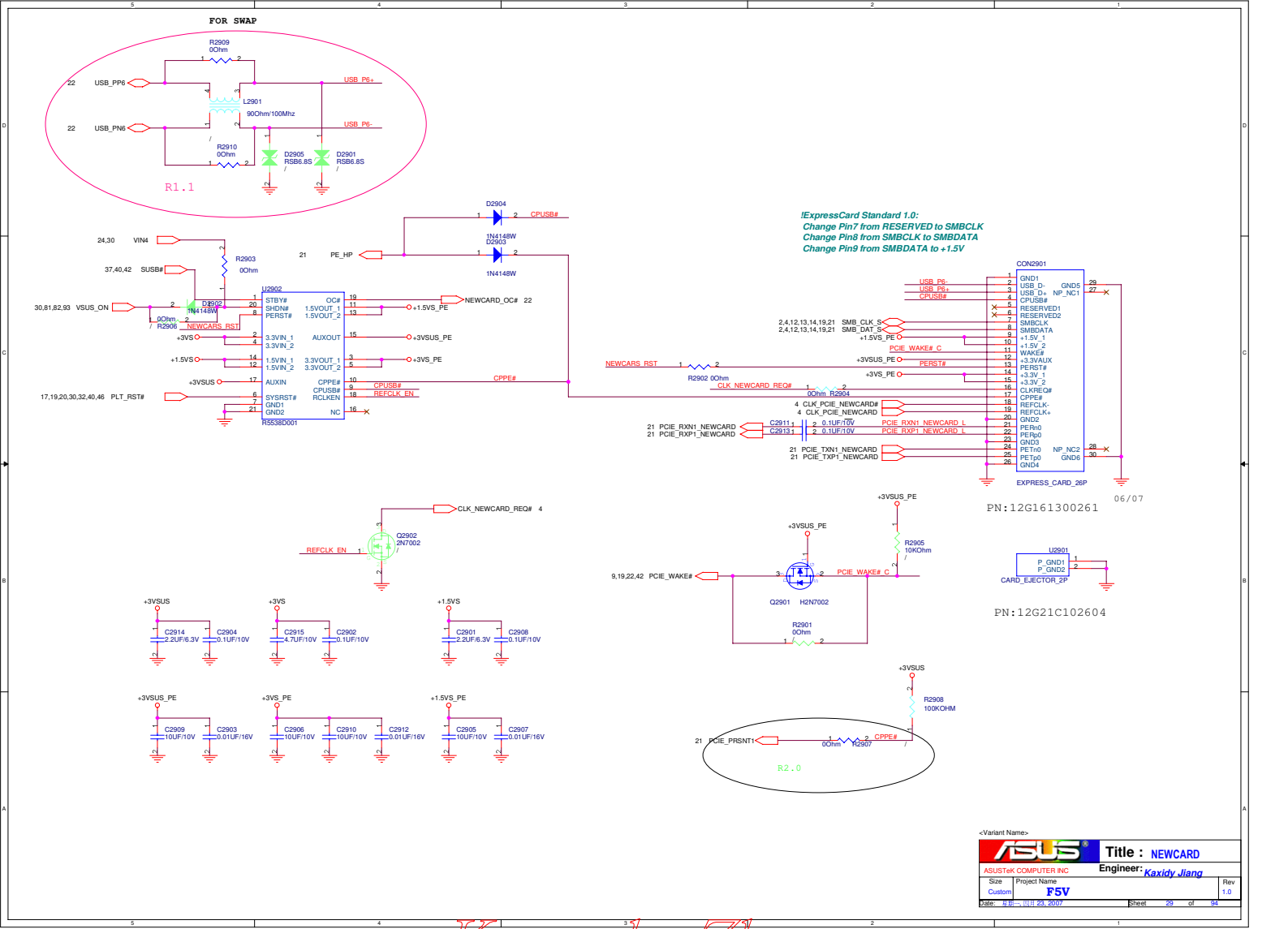
INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils



Pre-AMP **For Test Function**



Title : MIC,LINE-IN JACK			
<OrgName>	Engineer: Kaxidy Jiang		
Size: Custom	Project Name: F5V		Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 28 of 94		



<Variant Name>

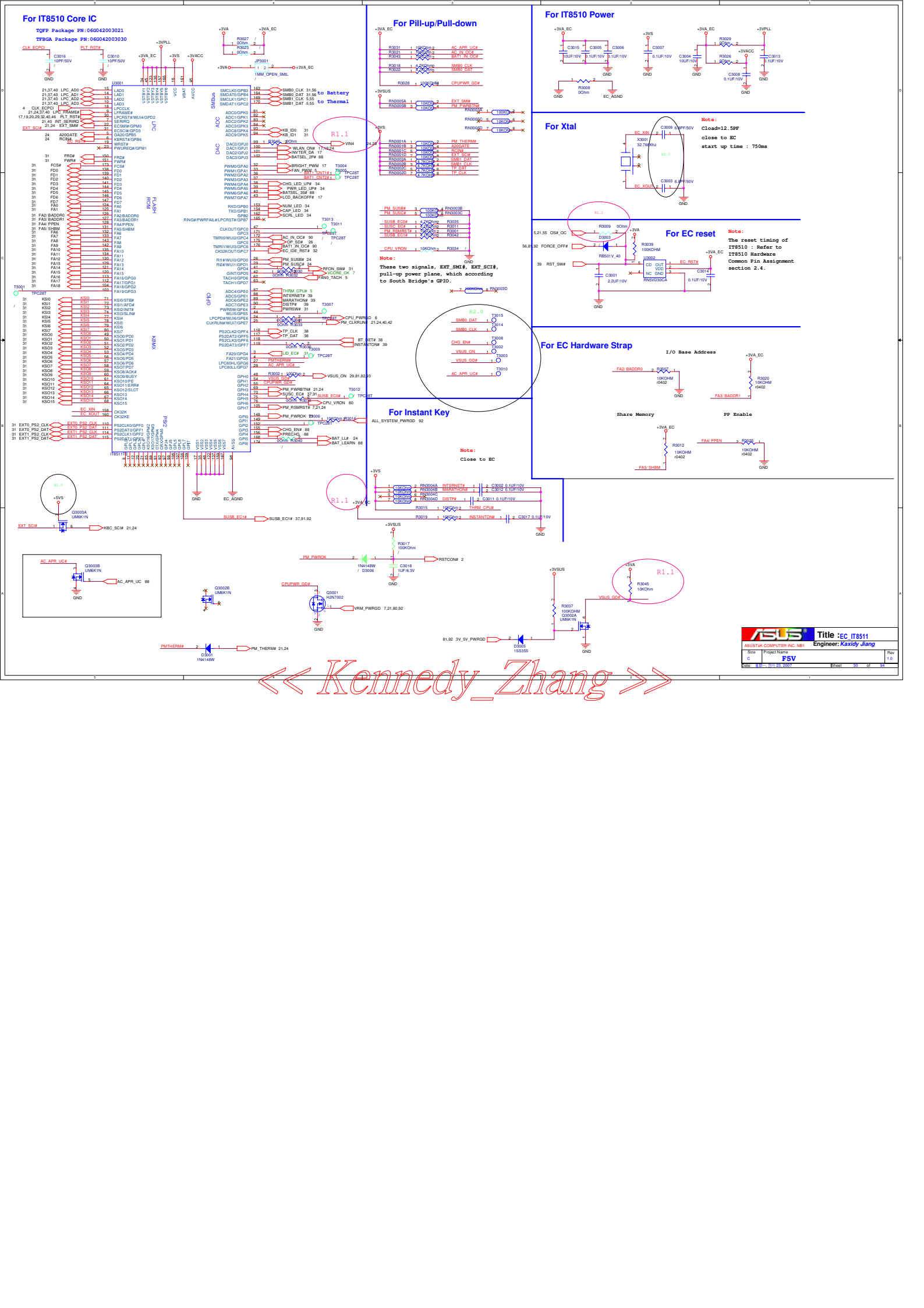
ASUSTeK COMPUTER INC

Title : NEWCARD

Engineer: Kaxidy Jiang

Size	Project Name	Rev
Custom	F5V	1.0

Date: 十月 一, 周日 23, 2007 Sheet 29 of 94


For IT8510 Core IC
TQFP Package PN:06G042003021
TFBGA Package PN:06G042003030
For Pill-up/Pull-down
For IT8510 Power
For Xtal
Note:
Cload=12.5PF
close to EC
start up time : 750ms
For EC reset
Note:
The reset timing of IT8510 : Refer to IT8510 Hardware Common Pin Assignment section 2.4.
For EC Hardware Strap
I/O Base Address
Share Memory
PP Enable
Note:
These two signals, EXT_SMI#, EXT_SCI#, pull-up power plane, which according to South Bridge's GPIO.
For Instant Key
Note:
Close to EC
to Battery
to Thermal
Title : EC_IT8511
Engineer: Kaxidy Jiang
ASUSTeK COMPUTER INC. NB1
Size: C
Project Name: FSV
Rev: 1.0
Date: 星期一, 四月 23, 2007
Sheet 30 of 94
<< Kennedy_Zhang >>

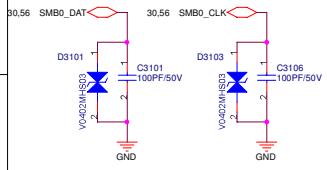
For Battery

Single Battery

BAT1_CNT1#, BAT1_CNT2#, BAT2_CNT1#, BAT2_CNT2# don't connect to Battery Connector.

Dual Battery

BAT1_CNT1#, BAT1_CNT2#, BAT2_CNT2# must connect to Battery Connector.

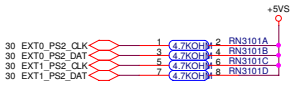


Note:

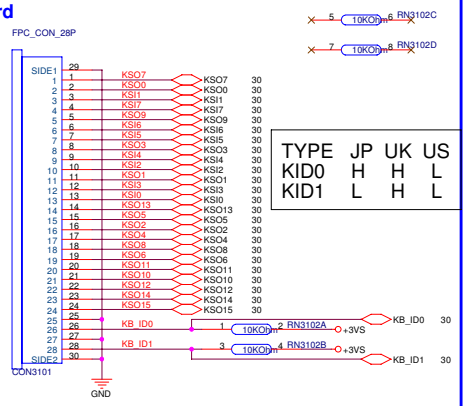
When we plug in or plug out the battery, it may cause a spike to damage the EC and gas gauge. It needed to add these varistors to protect those pins.

close to connector

For External PS/2 I/F

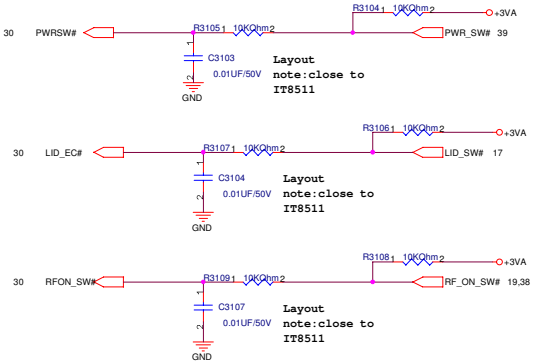


For Keyboard



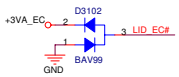
TYPE	JP	UK	US
KID0	H	H	L
KID1	L	H	L

For Switch



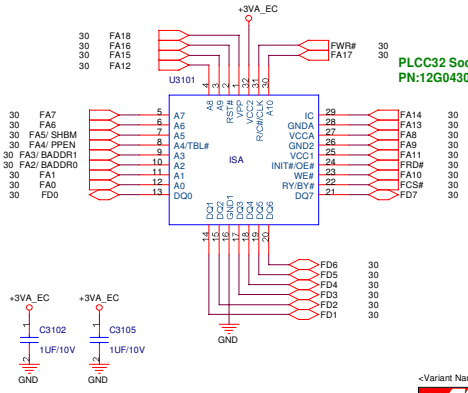
Note:

This LID_EC# is a signal from inverter board, it is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. It needed to add bidirectional diode to protect this pin.



Layout note:close to connector

For 4M bits ISA ROM



Note:

If you use 8M bits ROM, you need to connect FA19 to EC side.

PLCC32 Socket
PN:12G04300032F

SST-PLCC32 4Mbits Flash ROM
PN:05G001027221

<Variant Name>

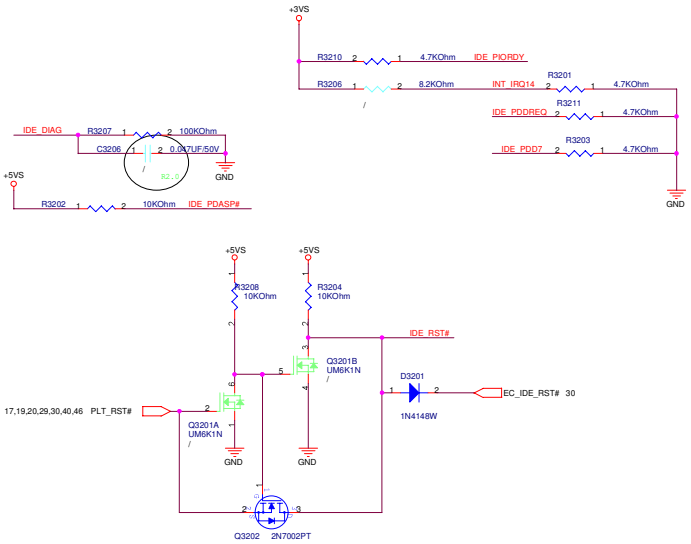
Title : KB&ISA ROM

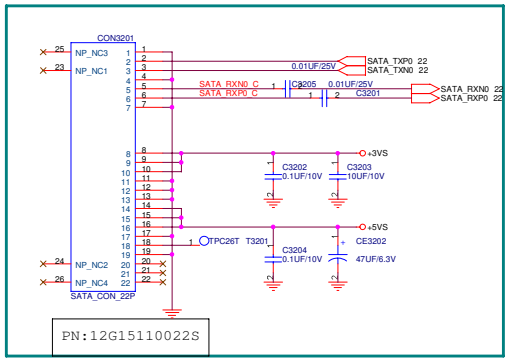
ASUSTeK COMPUTER INC. NB1

Engineer: Kaxidy Jiang

Size	Project Name	Rev
Custom	F5V	1.0

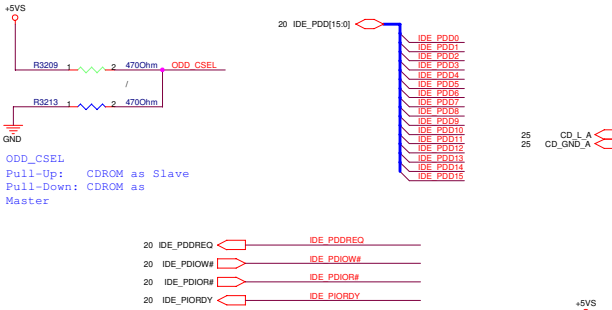
Date: 星期一, 四月 23, 2007 Sheet 31 of 94



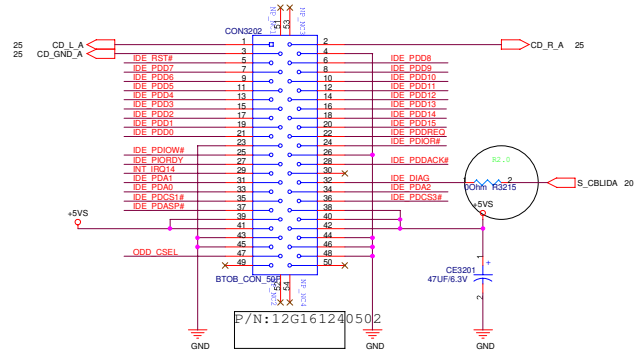


Dafult

SATA

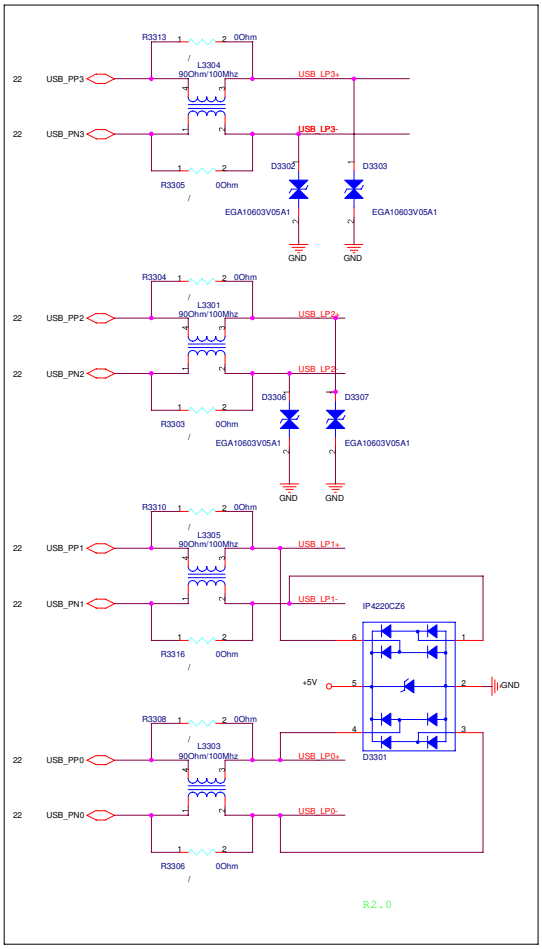


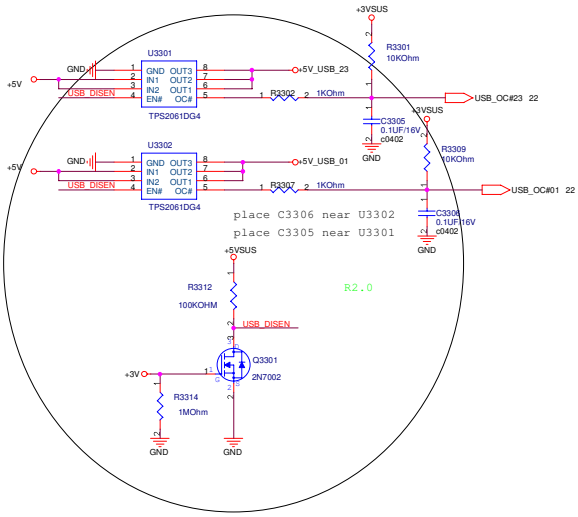
CD-ROM

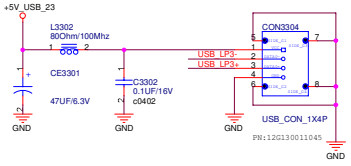


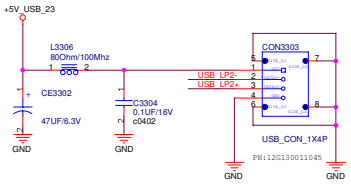
<Variant Name>

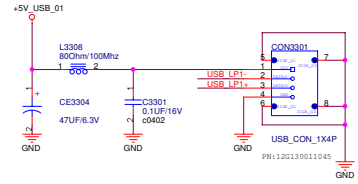
ASUSTeK COMPUTER INC	Title : HDD & CD-ROM	
	Engineer: Kaxidy Jiang	
Size: Custom	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 32 of 94	

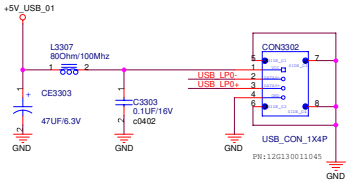








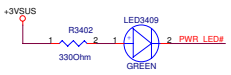


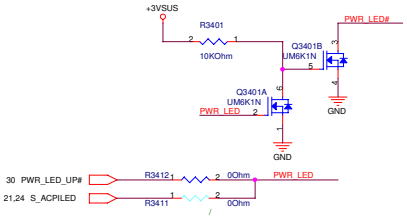


<Variant Name>

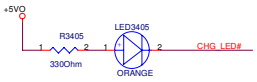
ASUSTeK COMPUTER INC. NB1	Title : USB CONN	
	Engineer: Kaxidy Jiang	
Size: Custom	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 33 of 94	

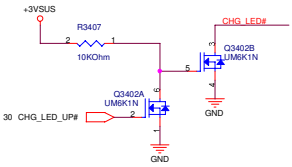
For POWER LED



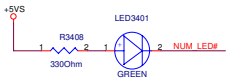


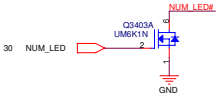
BATTERY LED



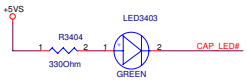


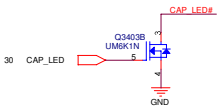
Num Lock



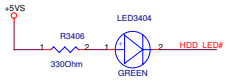


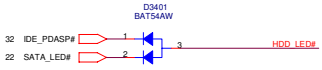
Cap Lock



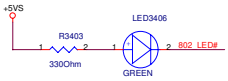


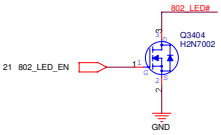
SATA/IDE LED



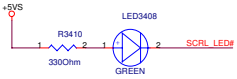


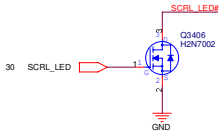
WireLess LED



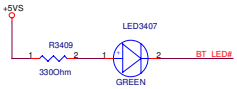


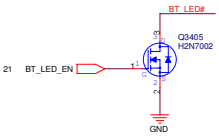
Scroll Lock

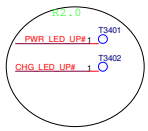




BT LED







<Variant Name>

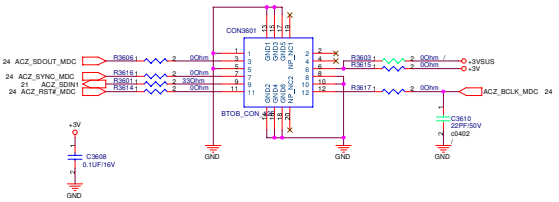
ASUSTeK COMPUTER INC	Title : LED	
	Engineer: Kaxidy Jiang	
Size: Custom	Project Name: F5V	Rev: 1.0
Date: 十月 一, 四月 23, 2007	Sheet 34 of 94	

ASUSTeK Computer INC	Title : BLANK	
	Engineer: Hawk Zhu	
Size: B	Project Name: F5V	Rev: 1.0
Date: 星期 一, 四月 23, 2007	Sheet 35 of 94	

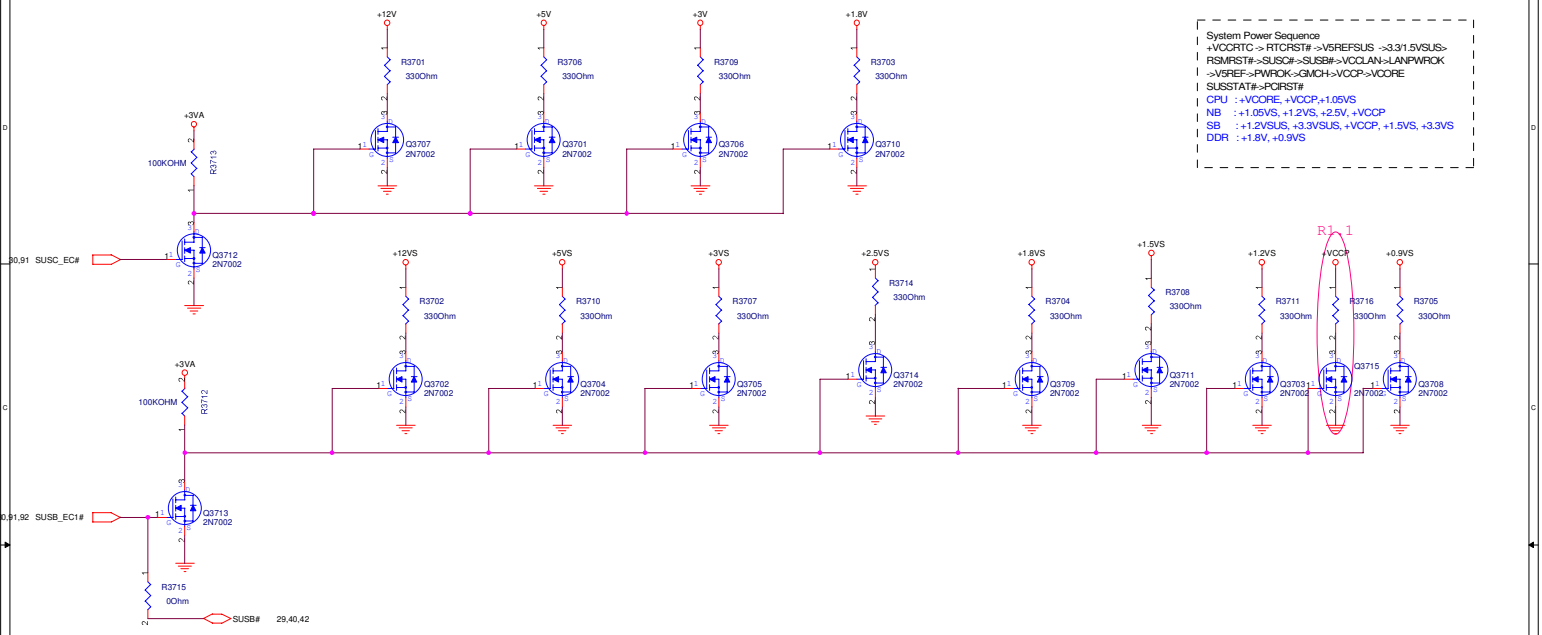
<< Kennedy_Zhang >>

LAN PORT

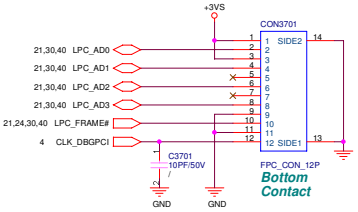
MDC



ASUSTeK COMPUTER INC	Title : RJ11+45 & MDC	
	Engineer: Kaxidy Jiang	
Size: C	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 38 of 94	



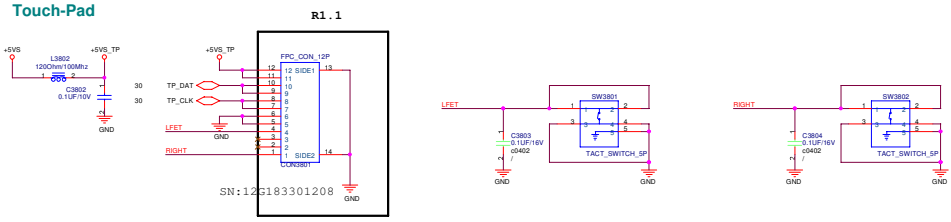
Debug Port



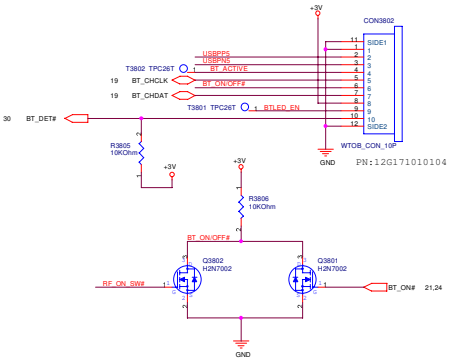
<Variant Name>

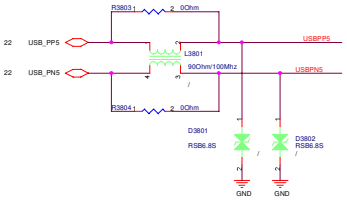
ASUSTeK COMPUTER INC	Title : DISCHARGE CKT	
	Engineer: Kaxidy Jiang	
Size: Custom	Project Name: F5V	Rev: 1.0
Date: 十月 23, 2007	Sheet 37 of 94	

Touch-Pad

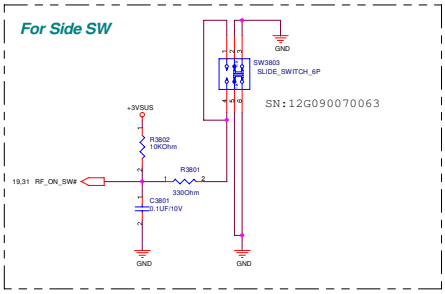


For Bluetooth





For Side SW



<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : BT&TP

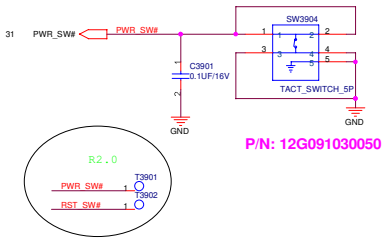
Engineer: Kaxidy Jiang

Size	Project Name	Rev
C	FSV	1.0

Date: 日 5, 月 23, 2007 Sheet 38 of 94

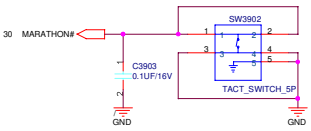
<< Kennedy_Zhang >>

Power SW.

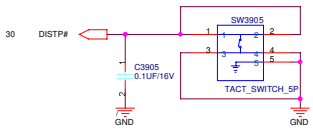


P/N: 12G091030050

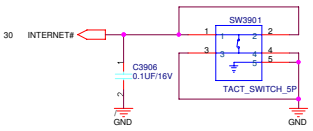
Marathon SW.



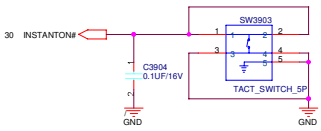
Disable Touch Pad SW.



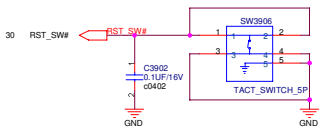
Internet SW.



IstantON SW.



RESET SW.

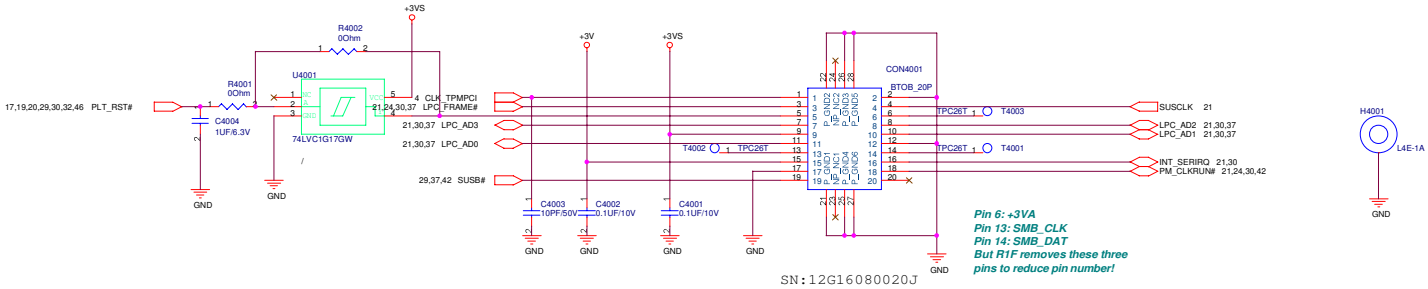


P/N: 12G091030050

<Variant Name>

ASUSTeK COMPUTER INC	Title : SWITCH	
	Engineer: Kaxidy jiang	
Size: Custom	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 39 of 94	

For TPM Module

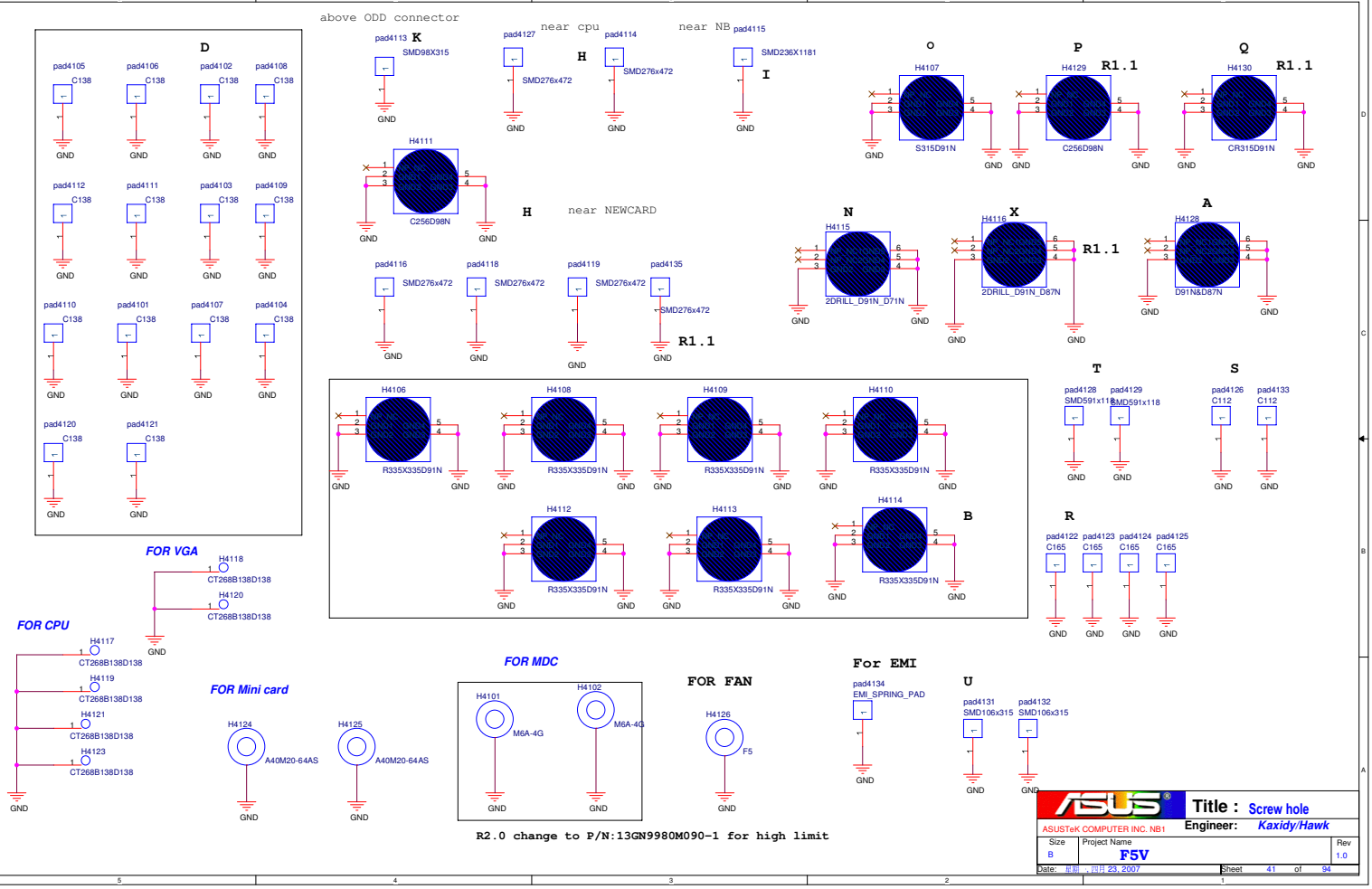


Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

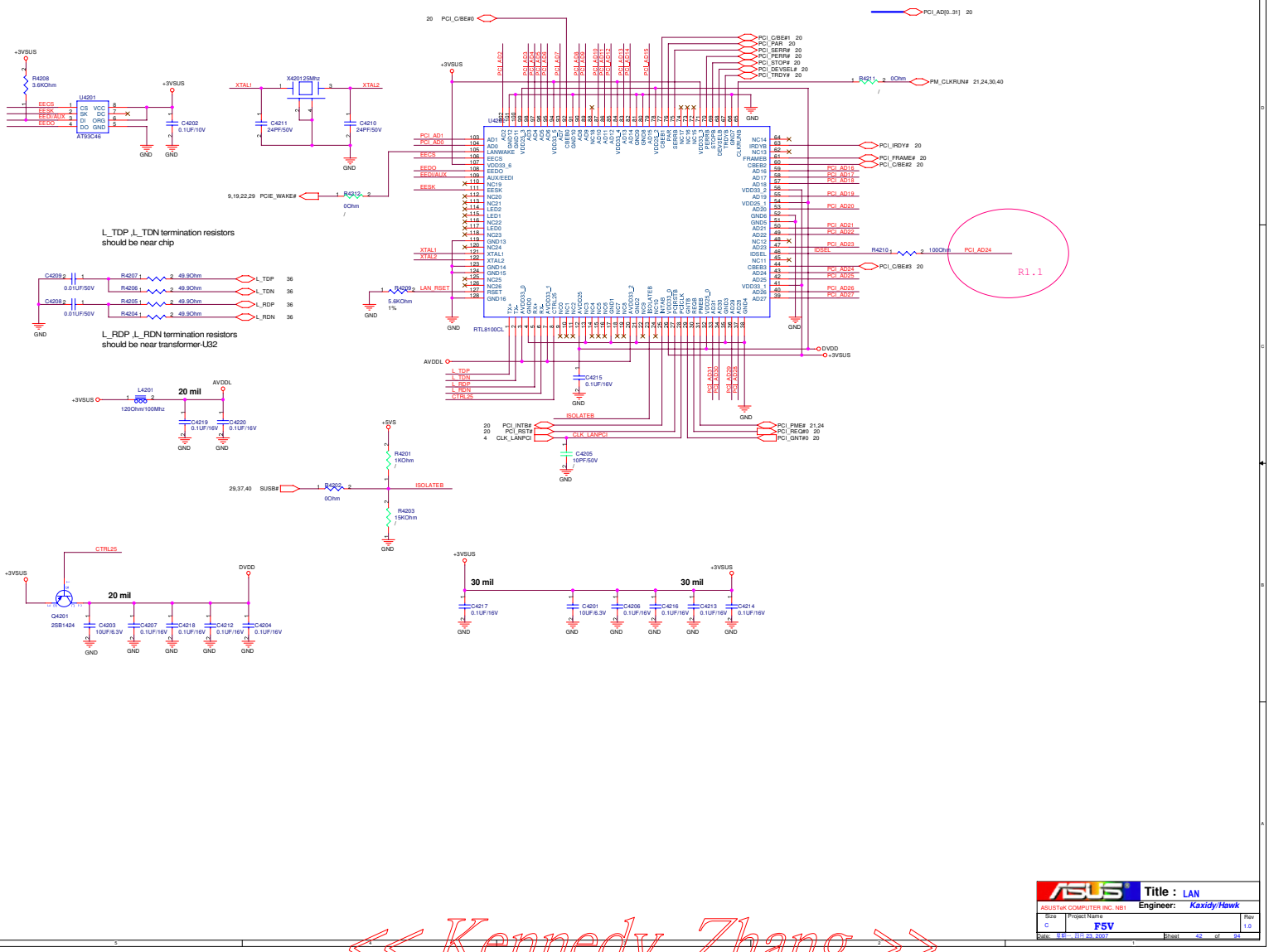
SN:12G16080020J

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : TPM	
	Engineer: Kaxidy Jiang	
Size: Custom	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 40 of 94	



<< Kennedy_Zhang >>



ASUSTeK COMPUTER INC. NB1

Title : LAN

Engineer: Kaxidy/Hawk

Size	Project Name	Rev
C	F5V	1.0

Date: 星期二, 四月 23, 2007 Sheet 42 of 94

<< Kennedy_Zhang >>

Title : BLANK

ASUSTeK COMPUTER INC. NB1

Engineer: Kaxidy/Hawk

Size	Project Name	Rev
A	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 43 of 94

Title : BLANK

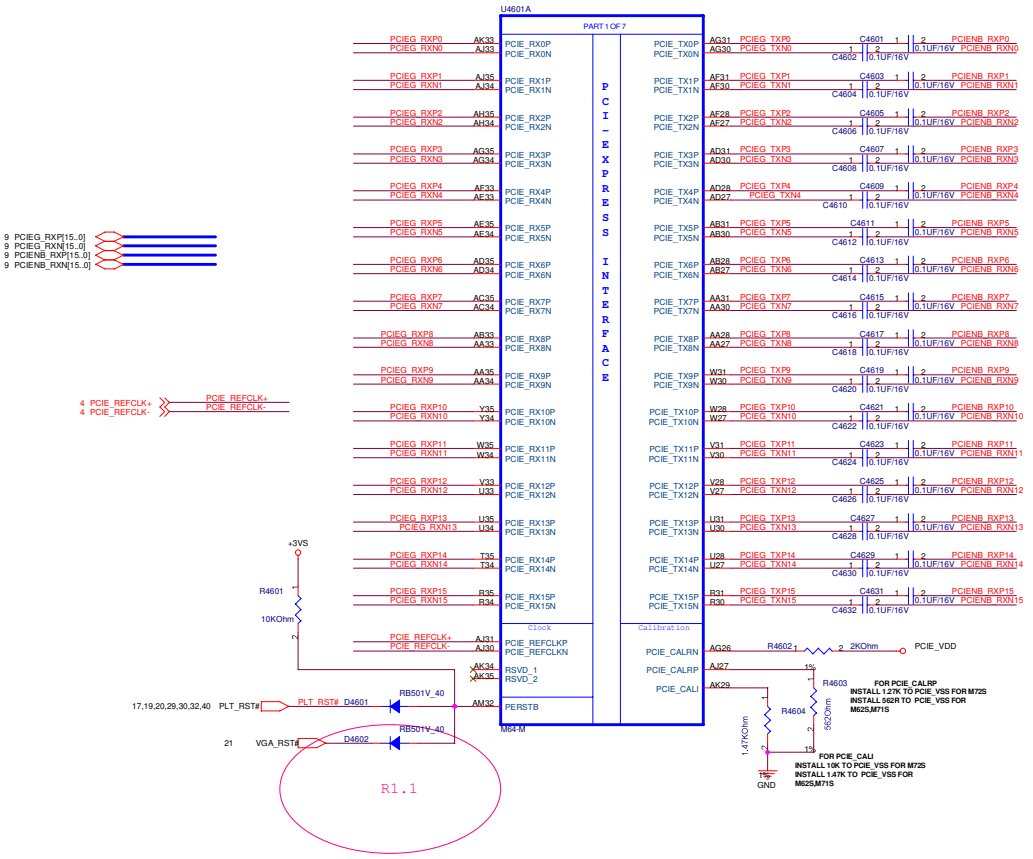
ASUSTeK COMPUTER INC. NB1

Engineer: Kaxidy/Hawk

Size	Project Name	Rev
A	F5V	1.0

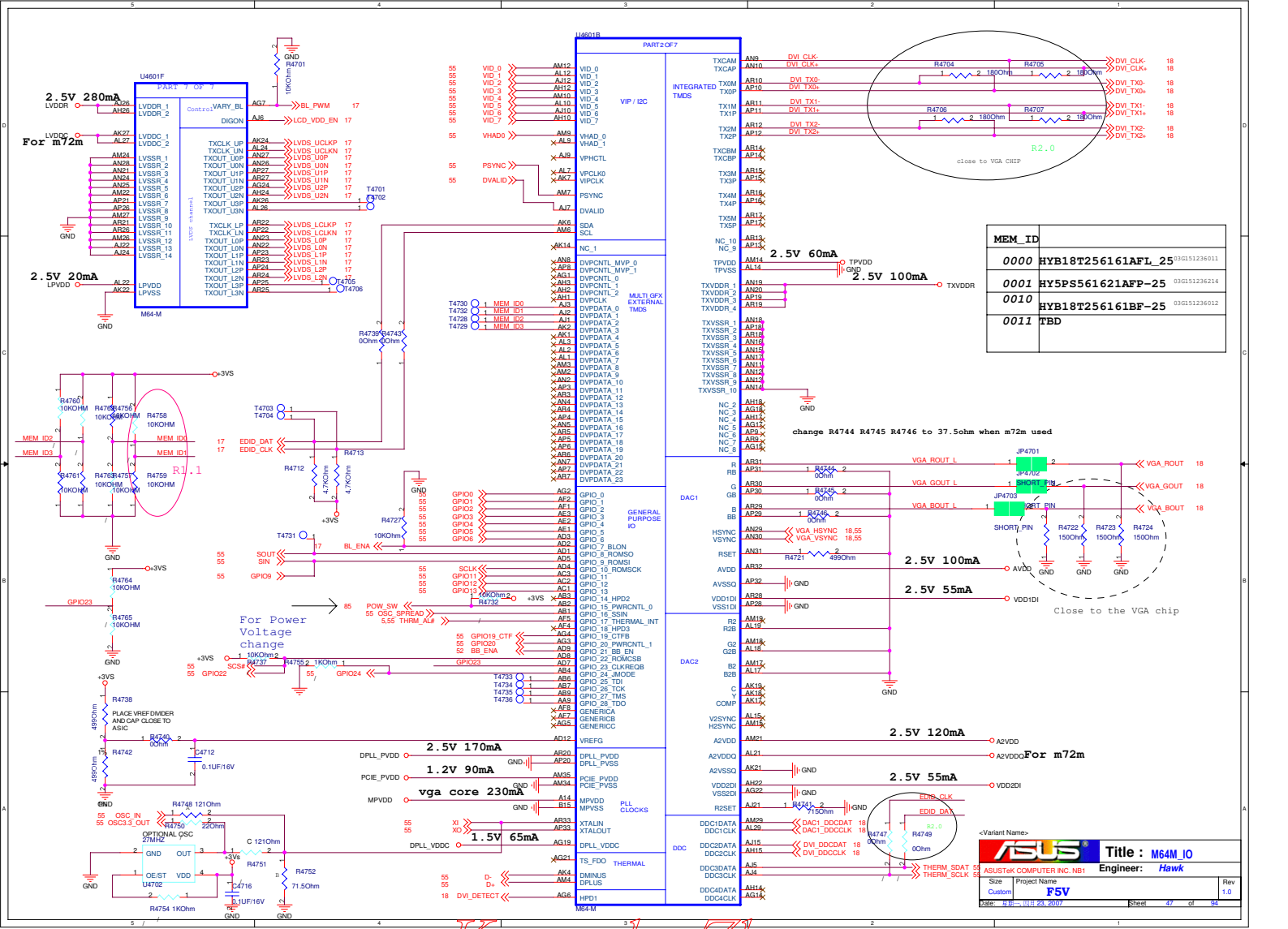
Date: 星期一, 四月 23, 2007 Sheet 44 of 94

Title : BLANK		
ASUSTeK COMPUTER INC. NB1	Engineer: Kaxidy/Hawk	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 45 of 94	

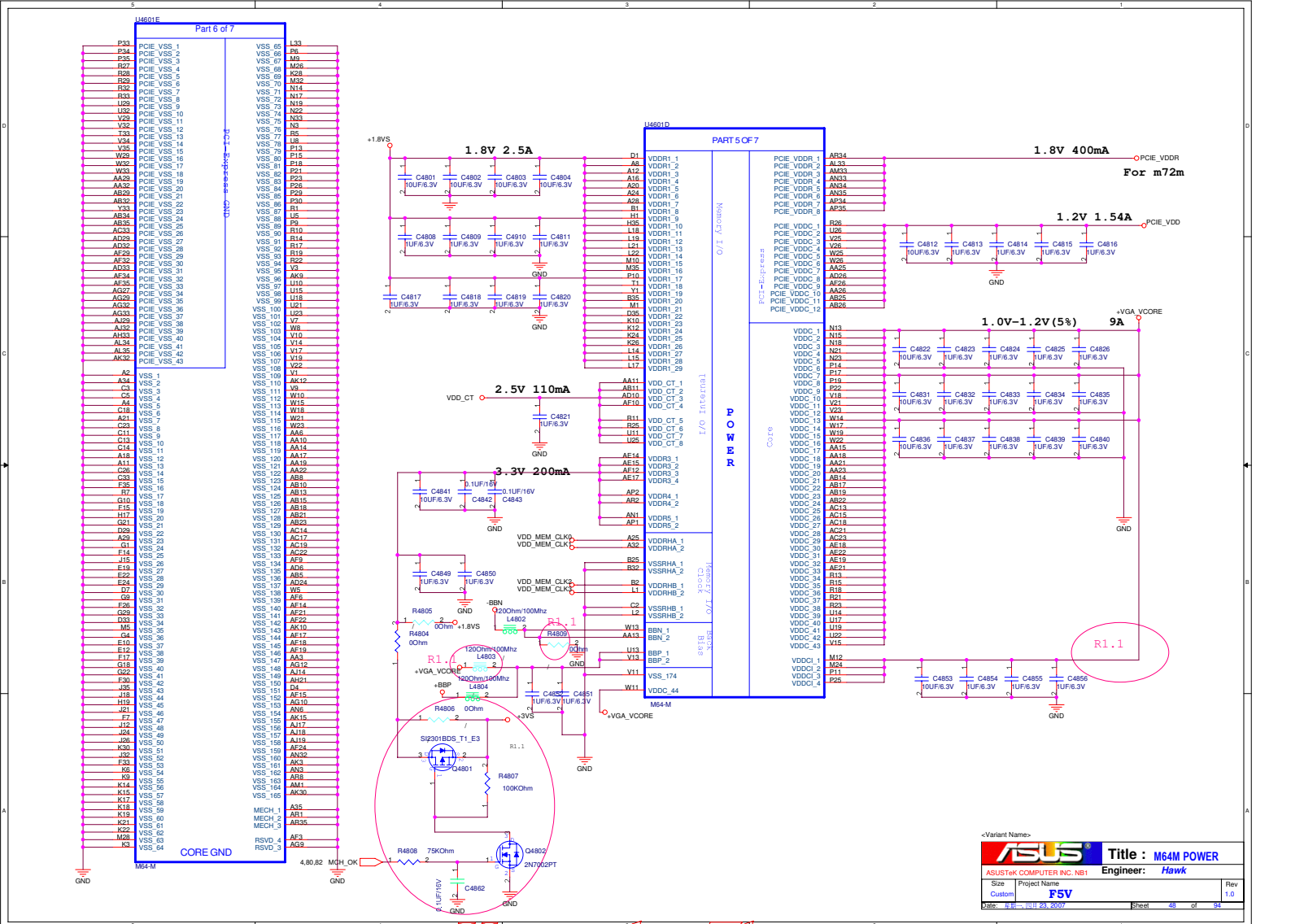


<Variant Name>

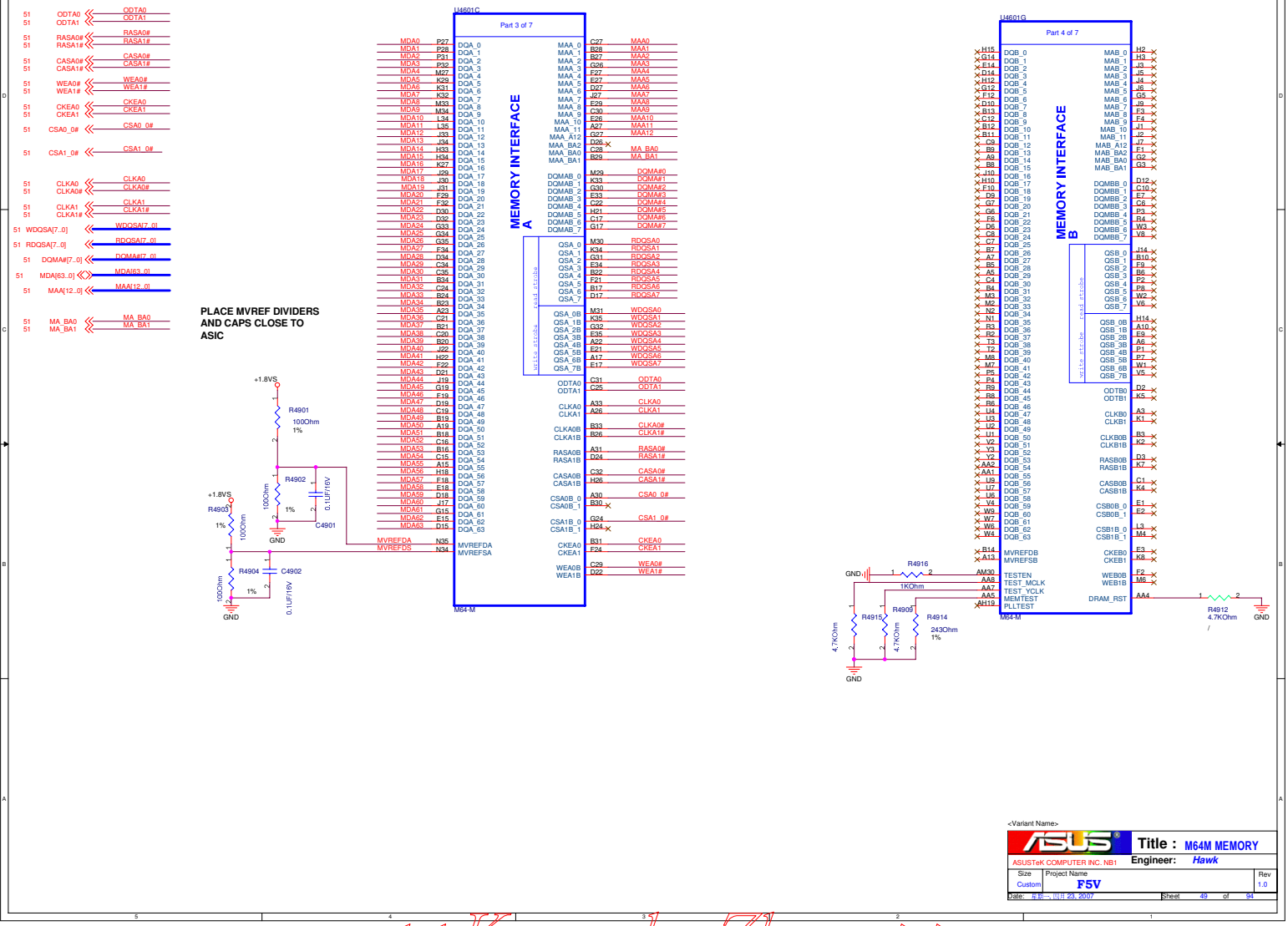
ASUSTeK COMPUTER INC. NB1	Title : M64M PCIE	
	Engineer: Hawk	
Size: Custom	Project Name: F5V	Rev: 1.0
Date: 十月 一, 向日 23, 2007	Sheet 46 of 94	



<< Kennedy_Zhang >>



<< Kennedy_Zhang >>



<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : M64M MEMORY

Engineer: Hawk

Size	Project Name	Rev
Custom	F5V	1.0

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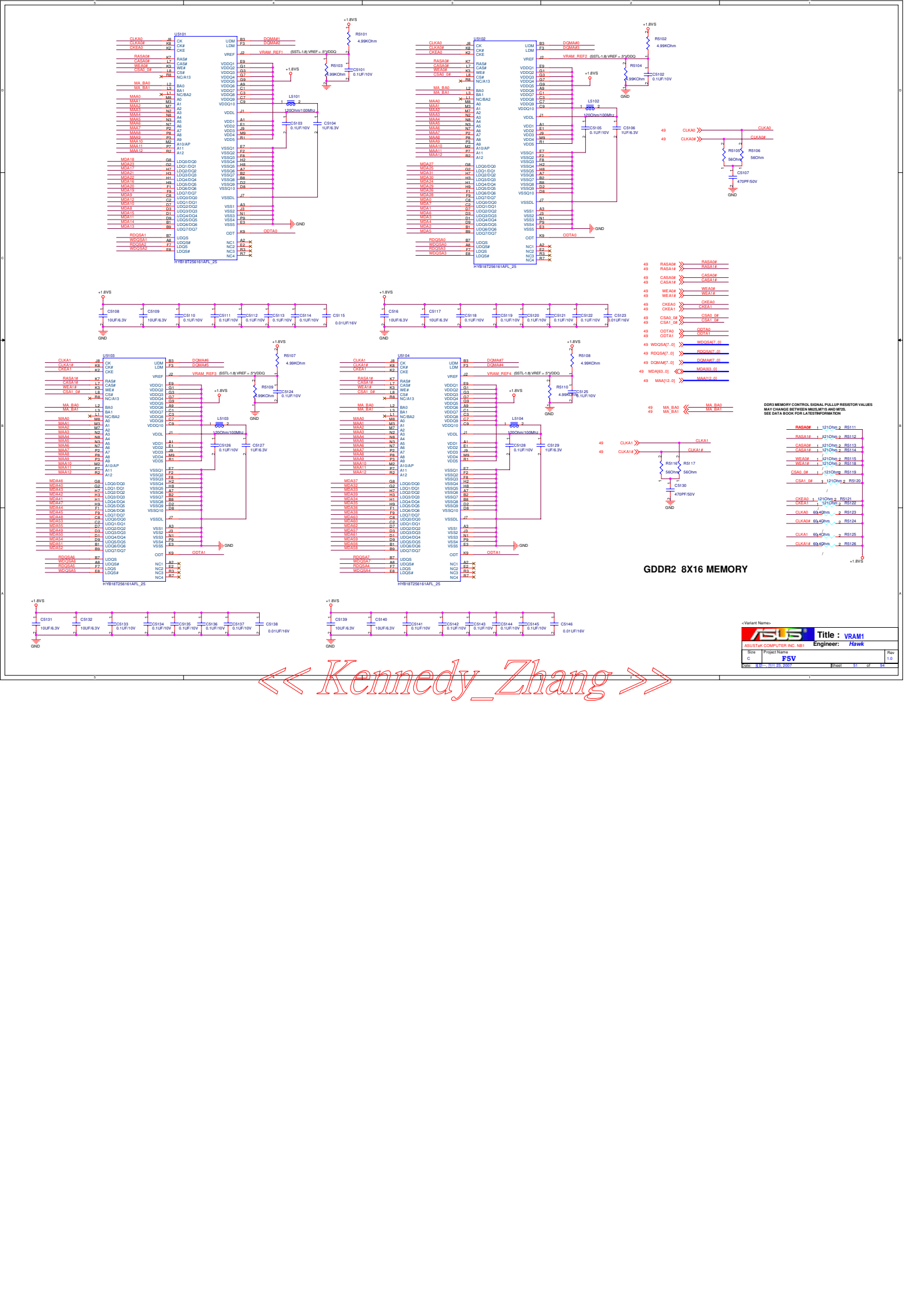
Title : BLANK		
ASUSTeK COMPUTER INC. NB1	Engineer: Kaxidy/Hawk	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 50 of 94	


GDDR2 8X16 MEMORY
DDR3 MEMORY CONTROL SIGNAL PULLUP RESISTOR VALUES
MAY CHANGE BETWEEN M625,M71S AND M725.
SEE DATA BOOK FOR LATEST INFORMATION
HYB18T256161AFL_25
Title : VRAM1
Engineer: Hawk
ASUSTeK COMPUTER INC. NB1
Size: C
Project Name: FSV
Rev: 1.0
Date: 二月 23, 2007
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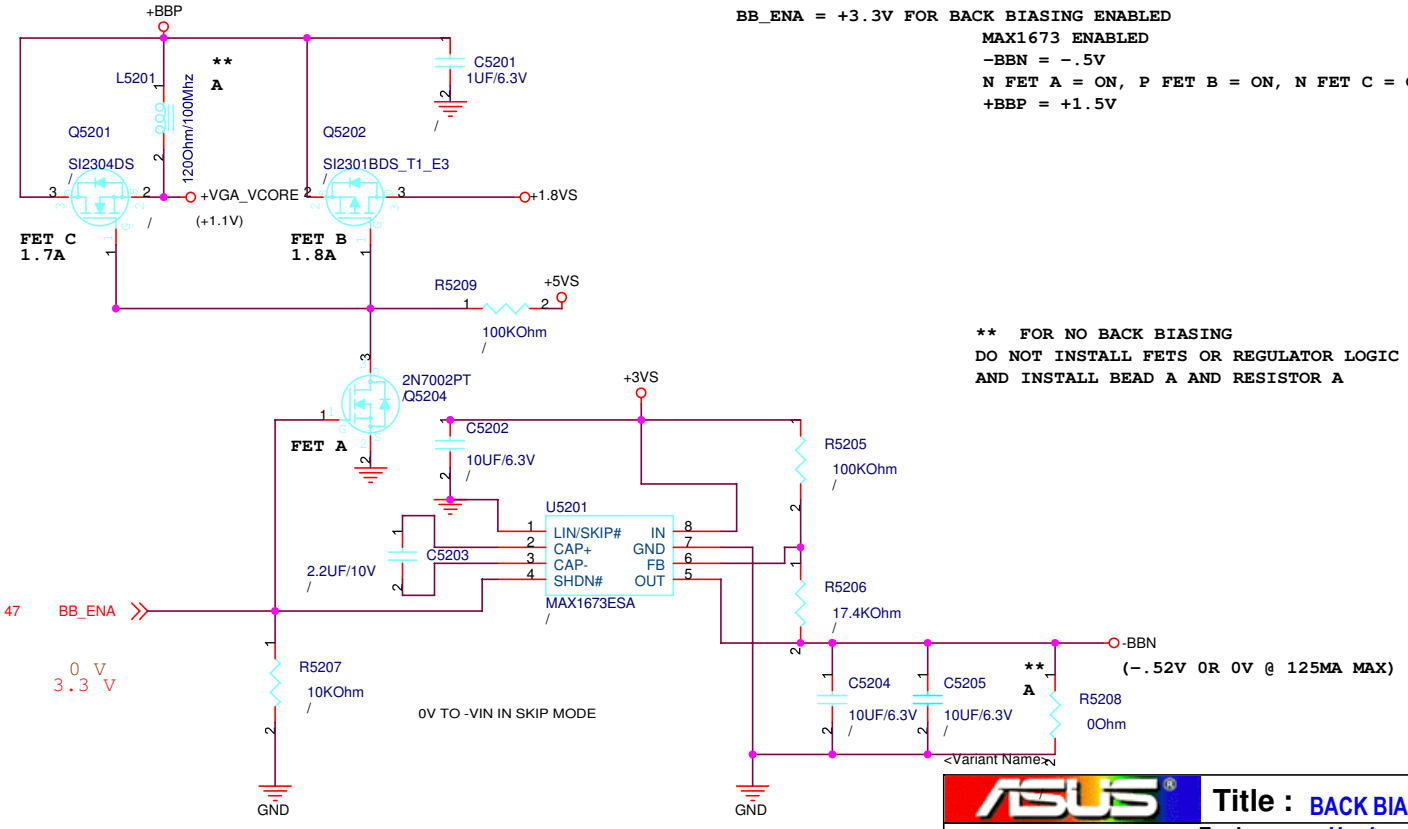
<< Kennedy_Zhang >>

COMPONENTS SHOWN ARE EXAMPLES ONLY AND NOT NECESSARILY QUALIFIED

BB_ENA = 0V FOR BACK BIASING DISABLED
MAX1673 SHUTDOWN
-BBN = 0V VIA MAX1673 INTERNAL 1 OHM TO GROUND
N FET A = OFF, P FET B = OFF, N FET C = ON
+BBP = VDD_CORE

BB_ENA = +3.3V FOR BACK BIASING ENABLED
MAX1673 ENABLED
-BBN = -.5V
N FET A = ON, P FET B = ON, N FET C = OFF
+BBP = +1.5V



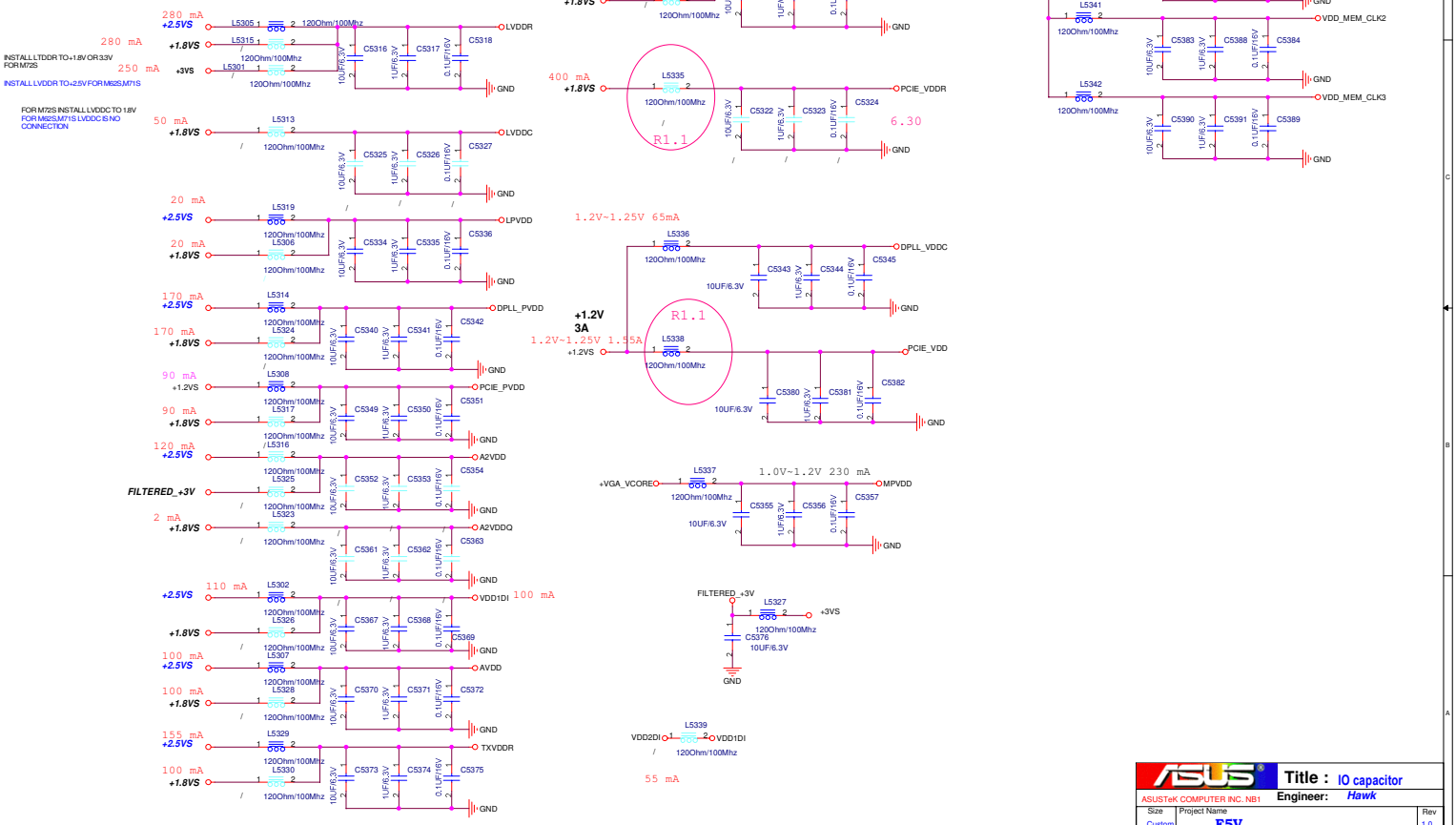
** FOR NO BACK BIASING
DO NOT INSTALL FETS OR REGULATOR LOGIC
AND INSTALL BEAD A AND RESISTOR A

ASUSTeK COMPUTER INC. NB1	Title : BACK BIAS	
	Engineer: Hawk	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 52 of 94	

COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED

LTPVSS18 DVSSDI TPVSS MPVSS
PCIE_PVSS PVSS A2VSSQ AVSSQ
*

PLACE CAPS FOR THESE GROUNDS CLOSE TO ASIC AND RUN DEDICATED TRACES FROM PINS TO JOIN THE GROUND PLANE WITH ONE VIA AT CAP



ASUSTeK COMPUTER INC. NB1

Title : IO capacitor
Engineer: Hawk
Size: Custom | Project Name: F5V | Rev: 1.0
Date: 星期一, 四月 23, 2007 | Sheet 53 of 94

<< Kennedy_Zhang >>

<Variant Name>

Title : VRAM2

ASUSTeK COMPUTER INC. NB1

Engineer: Hawk

Size	Project Name	Rev
C	FSV	1.0

Date: 日 8 , 月 29, 2007 Sheet 54 of 94

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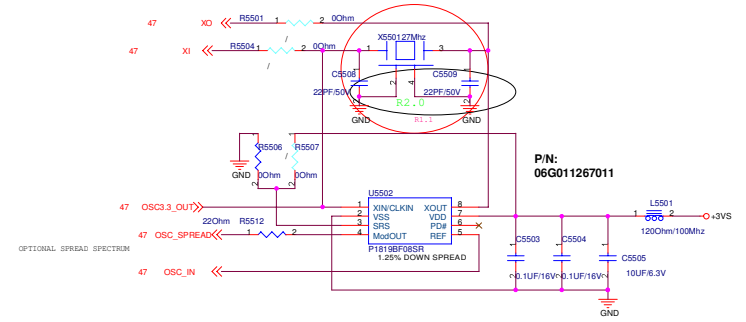
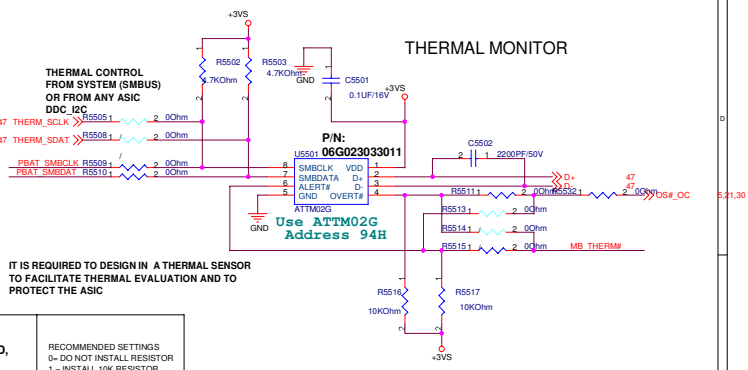
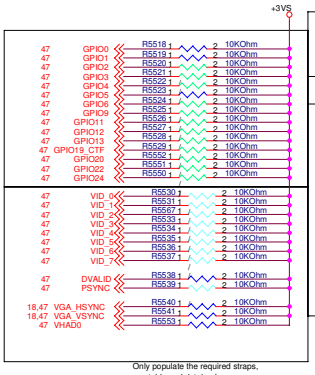






CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M62S,M71S	M72S
BIF_MSI_DIS	VID1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_64BAR_EN_A	VID5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1	1
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS NOT MUXED OUT	0	0
PLL_IBIAS_RD_1:0	GPIO[6:5]	BIAS CURRENT FOR PCIE PHY PLL	0 1	X X
BIOS_ROM_EN	GPIO19_CTF	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERATURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	O	O
BIF_VGA DIS	PSYNC	VGA ENABLED	NA	O
MEM_TYPE	UNUSED GPIO	MEMORY TYPE,MAKE AND SIZE INFO	X X X	X X X

ATI RESERVED CONFIGURATION STRAPS

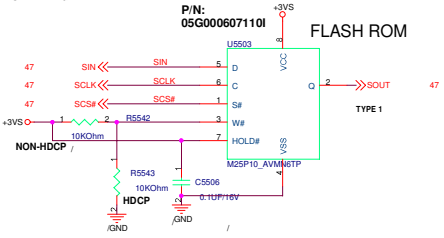
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

VID0 VID2 VID3 VID4 VID6 VID7 HSYNC GPIO8 DVALID GPIO2 GPIO3

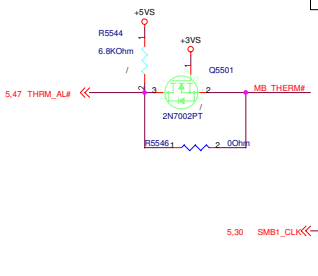
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

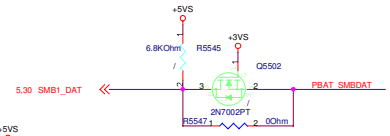
GENERICC GPIO18_HPD3 GPIO23_CLKREQB

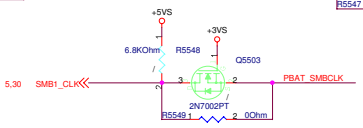
A 256MB MEMORY APERTURE SIZE CAN BE DEFINED USING A SEPARATE ROM OR STRAPPING



FOR M62S,M71S
A SPECIAL EXTERNAL EEPROM WITH THE WP PIN PULLED DOWN IS MANDATORY FOR HDCP SUPPORT
CONSULT HDCP APPLICATION NOTES FOR ADDITIONAL INFORMATION
M72S DOES NOT REQUIRE AN EXTERNAL ROM FOR HDCP SUPPORT

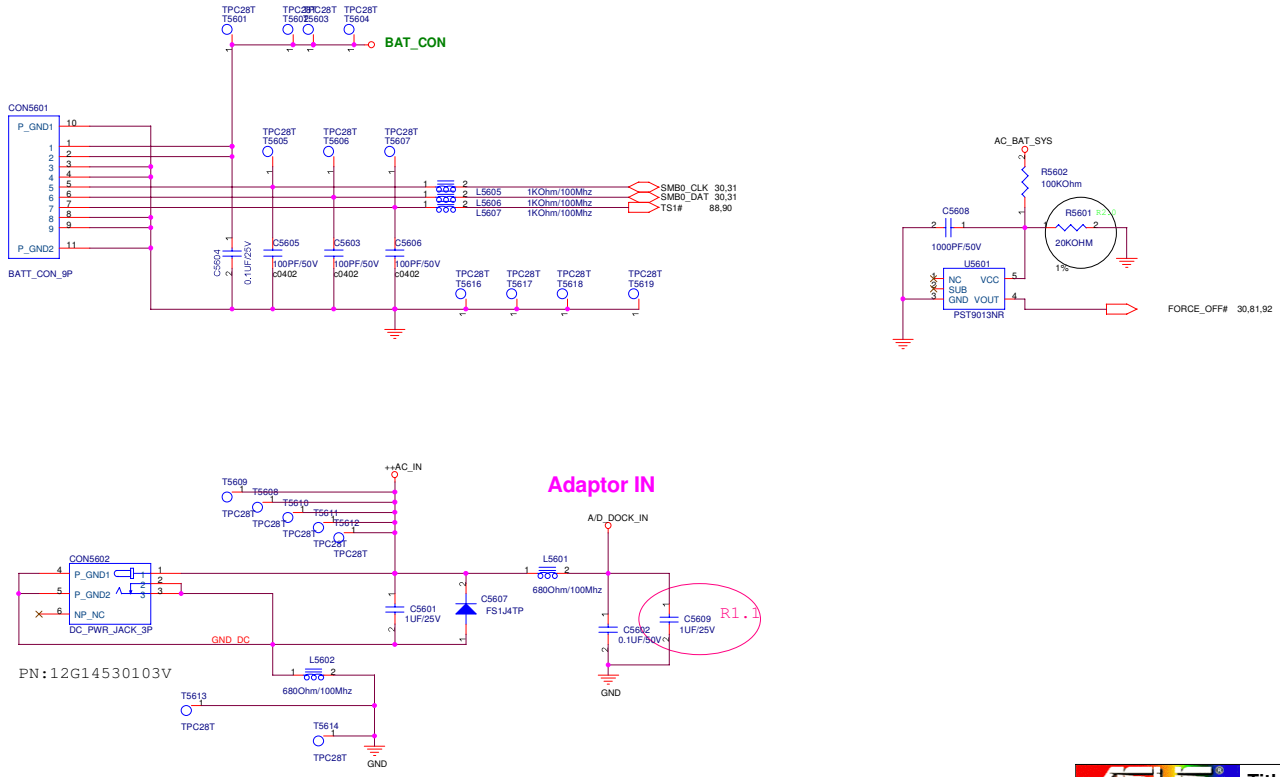






COMPONENTS SHOWN ARE EXAMPLES ONLY AND NOT NECESSARILY QUALIFIED

ASUSTeK COMPUTER INC. NB1	Title : SS STRAPS	
	Engineer: Hawk Kaxidy	
Size: Custom	Project Name: F5V	Rev: 1.0
Date: 十月 一, 向月 23, 2007	Sheet 55 of 94	



ASUSTeK COMPUTER INC. NB1	Title : AC/BAT JACK	
	Engineer: Hawk	
Size: B	Project Name: F5V	Rev: 1.0
Date: 星期 一, 四月 23, 2007	Sheet 56 of 94	

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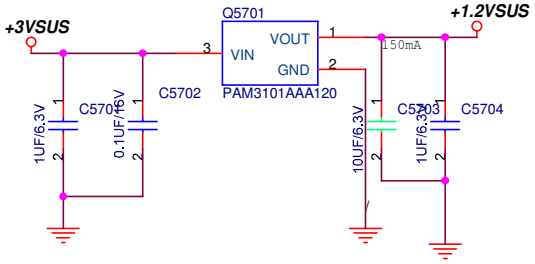
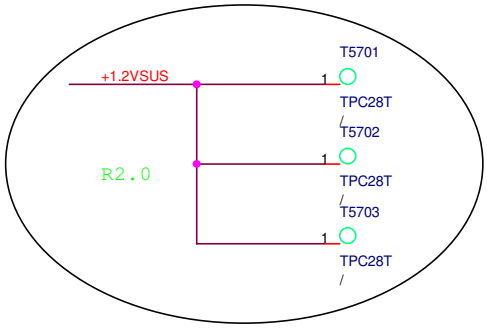
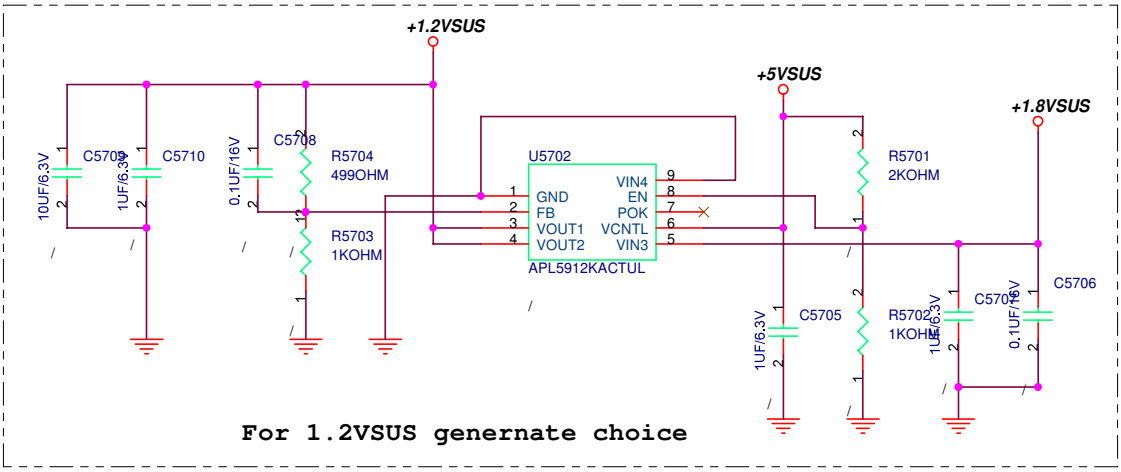






ASUSTeK COMPUTER INC. NB1

Title : +1.2VSUS

Engineer: Kaxidy/Hawk

Size	Project Name	Rev
A	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 57 of 94

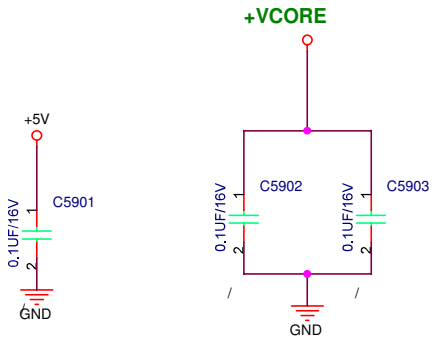
Title : BLANK

ASUSTeK COMPUTER INC. NB1

Engineer: Kaxidy/Hawk

Size	Project Name	Rev
A	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 58 of 94



ASUSTeK COMPUTER INC. NB1	Title : EMI	
	Engineer: Kaxidy/Hawk	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 59 of 94	

1. P2 unmount R201 for H_CPURST#, add T205/T206 for CLK_CPU_BCLK#/CLK_CPU_BCLK test.

2. P6 mount R605 for H_PWRGD timing, add T603/T604/T605/T606 to HA[32:35]#.

3. P7 unmount R706

4. P20 mount R2001/R2002/R2003/R2009/R2011 for PCI_REQ#[0:4]

5. P21 change R2121 to 0Ohm
   add R2124(33Ohm) for ACZ_RST# according to 968 ACT.
   add R2108/R2112(0Ohm) for PCIEPRSNT0/1 according to sis ACT
   ADD GMAC OSC25MHI to GND according to sis ACT.
   unmount L2103,mount L2105 according to spec.
   unmount R2122 for repeat with R2453, change R2120/R2125 PU to +3VSUS according to spec.
   change GPIO17 from VIN4 to S_A20GATE, add R2127(0Ohm) for reserve SUSCLK
6.P17 add R1708 and R1709 to change BL_PWM to BL_ENA to fix garbage

7. P22 change R2217 to 12KOhm, add C2237(22pF) for SATA REXT according to 968 ACT.

8. P24 add R2434 for A20GATE to H_A20M#,add R2457 for A20GATE to S_A20GATE,add R2456 to PU S_A20GATE

9. P29 add R2909/R2910(0Ohm), unmount L2901 for EMI.

10. P30 change D3002 to R3009 for OS#_OC to avoid no EC reset, .

    delete D3004 for DDR power are not SUS power,

    add R3045 for VSUS_GD# PU, change GPJ0 to VIN4 to control NEW card shutdown, add R3046 for VIN4,

    Add R3019 for INSTANTON#

11. P33/P5/P32 change the P/N of CE3202/CE501/CE3301/CE3302/CE3303/CE3304 for low cost

12. P37 mount R3716/Q3715 for +VCCP discharge

13. P42 change IDSEL to PCI_AD24

14.P46 add D4602 for VGA_RST#

15. P48 unmount L4803/R4809, delete L4801
    unmount R4806,mountQ4801/R4807/Q4802/R4808

16. P53 change L5335/L5338 to match the current.

17.P55 change X5501 to +-10ppm to follow spec,add C5508/C5509 to match X5501

18. P56 add C5609 for over current damaging charge IC.

19. P4 Change C440 from 0.1UF to 0.22UF

20. P10 change L1001 to 2A to match the current,, Add +1.2VS delay circuit.

21.P21 Add VGA_RST# to GPIO7, add R2140 for VGA_RST#.

22.P47 Unmount R4759,mount R4758 for Vram changed from 03G151236011 to 03G151236012.

R2.0

1.P29 mount R2907, connect PCIE_PRSNT1 to CPPE#
  P21 unmount R2108, mount R2118, change R2118 from 0Ohm to 4.7KOhm but unmount R2118

2.P27 change R2708 to 0Ohm and mount it to not support C3 mode

3.P33&22 add two TPS2061 (U3301/U3302) to avoid not start up caused by USB device with external power supply

4.P21 add R2141 to connect OS#_OC to PM_THRMTRIP#, change R2141 to Q2101

5.P30 change C3009/C3003 to 6.8pF

6.P27 change C2706/C2707 to 24pF

7.P55 change C5508/C5509 to 22pF

8.P33 unmount R3313/R3305/R3304/R3303/R3310/R3316/R3308/R3306, mount L3304/L3301/L3305/L3303, mount D3302/D3303/D3306/D3307/D3301

9.P47 add R4747/R4749 to reserve EDID_DAT/EDID_CLK to DDC3

10.P30 change Q3003 PU from +5V to +5VS

11.P5 unmount R506

12.P56 change R5601 to 20KOhm

13.P20 unmount R2054,add and mount C2010
  P32 add R3215 to connect S_CBLIDA to IDE_DIAG, unmount C3206
  P22 add and unmount C2215/C2238/C2239/C2236, add and mount C2206

14.P27 change 4in1 cardreader

15.P47 mount R4704/R4705/R4706/R4707
  P18 change DVI bead to R1832/R1833/R1834/R1835/R1836/R1837/R1838/R1839,change R1832/R1833/R1834/R1835/R1836/R1837/R1838/R1839 reference to L1806/L1807/L1808/L1809/L1810/L1811/L1812/L1813

16.P21 Unmount L2105, mount L2103

17.P21 change R2116 from 33Ohm to 20Ohm, change R2117 from 33Ohm to 0Ohm, change R2119 from 33Ohm to 20Ohm
   P24 change R2418 from 33Ohm to 0Ohm, change R2420 from 33Ohm to 0Ohm, change R2419 from 33Ohm to 0Ohm, change R2422 from 33Ohm to 0Ohm, change R2423 from 33Ohm to 0Ohm, change R2425 from 33Ohm to 0Ohm
   P25 change R2514 from 33Ohm to 47Ohm

F5VL

1. P2/3 change CPU socket to P
2. P32 delete R3205/R3212
3. P59 add C5902/C5903 for EMI

ASUSTeK COMPUTER INC. NB1

Title : BLANK

Engineer: Kaxidy/Hawk

Size	Project Name	Rev
C	F5V	1.0

Date: 星期二, 四月 23, 2007 Sheet 60 of 94

<< Kennedy_Zhang >>

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: Kaxidy/Hawk	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 61 of 94	

Title :	BLANK
ASUSTeK COMPUTER INC. NB1	Engineer: Kaxidy/Hawk
Size: A	Project Name: F5V
Rev: 1.0	
Date: 星期一, 四月 23, 2007	Sheet 62 of 94

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: Kaxidy/Hawk	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 63 of 94	

Title : BLANK

ASUSTeK COMPUTER INC. NB1

Engineer: Kaxidy/Hawk

Size	Project Name	Rev
A	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 64 of 94

Title :	BLANK	
ASUSTeK COMPUTER INC. NB1	Engineer:	Kaxidy/Hawk
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 65 of 94	

Title : BLANK

ASUSTeK COMPUTER INC. NB1

Engineer: Kaxidy/Hawk

Size	Project Name	Rev
A	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 66 of 94

Title : BLANK

ASUSTeK COMPUTER INC. NB1

Engineer: Kaxidy/Hawk

Size	Project Name	Rev
A	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 67 of 94

Title : BLANK		
ASUSTeK COMPUTER INC. NB1	Engineer: Kaxidy/Hawk	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 68 of 94	

Title :	BLANK
ASUSTeK COMPUTER INC. NB1	Engineer: Kaxidy/Hawk

Size	Project Name	Rev
A	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 69 of 94

Title : BLANK

ASUSTeK COMPUTER INC. NB1

Engineer: Kaxidy/Hawk

Size	Project Name	Rev
A	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 70 of 94

Title : BLANK

ASUSTeK COMPUTER INC. NB1

Engineer: Kaxidy/Hawk

Size	Project Name	Rev
A	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 71 of 94

Title : BLANK

ASUSTeK COMPUTER INC. NB1

Engineer: Kaxidy/Hawk

Size	Project Name	Rev
A	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 72 of 94

Title : BLANK

ASUSTeK COMPUTER INC. NB1

Engineer: Kaxidy/Hawk

Size	Project Name	Rev
A	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 73 of 94

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: Kaxidy/Hawk	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 74 of 94	

Title : BLANK

ASUSTeK COMPUTER INC. NB1

Engineer: Kaxidy/Hawk

Size	Project Name	Rev
A	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 75 of 94

Title : BLANK

ASUSTeK COMPUTER INC. NB1

Engineer: Kaxidy/Hawk

Size	Project Name	Rev
A	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 76 of 94

Title : BLANK

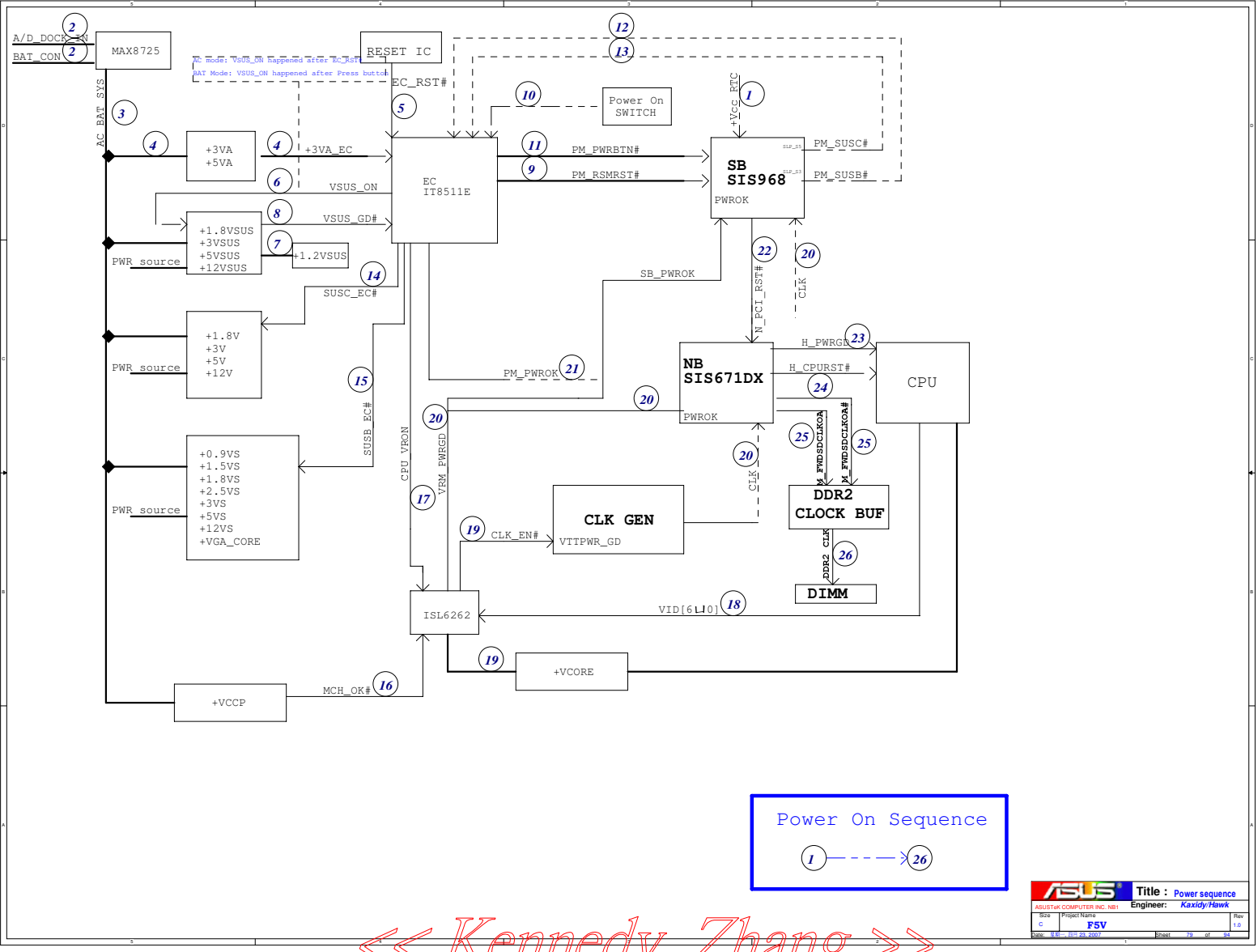
ASUSTeK COMPUTER INC. NB1

Engineer: Kaxidy/Hawk

Size	Project Name	Rev
A	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 77 of 94

Title : BLANK		
ASUSTeK COMPUTER INC. NB1	Engineer: Kaxidy/Hawk	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 78 of 94	



Power On Sequence

1 ---- 26

<< Kennedy_Zhang >>

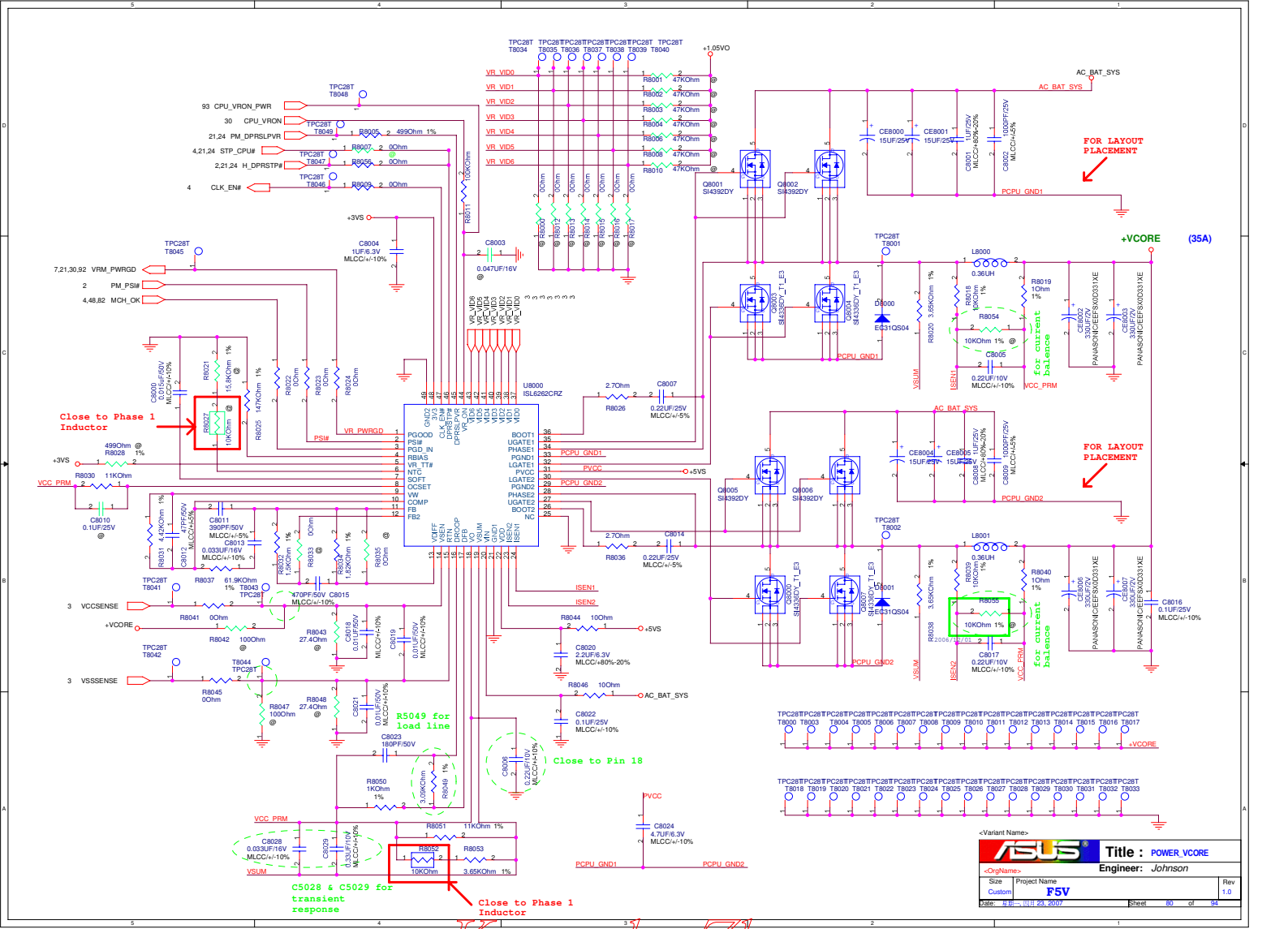
ASUSTeK COMPUTER INC. NB1

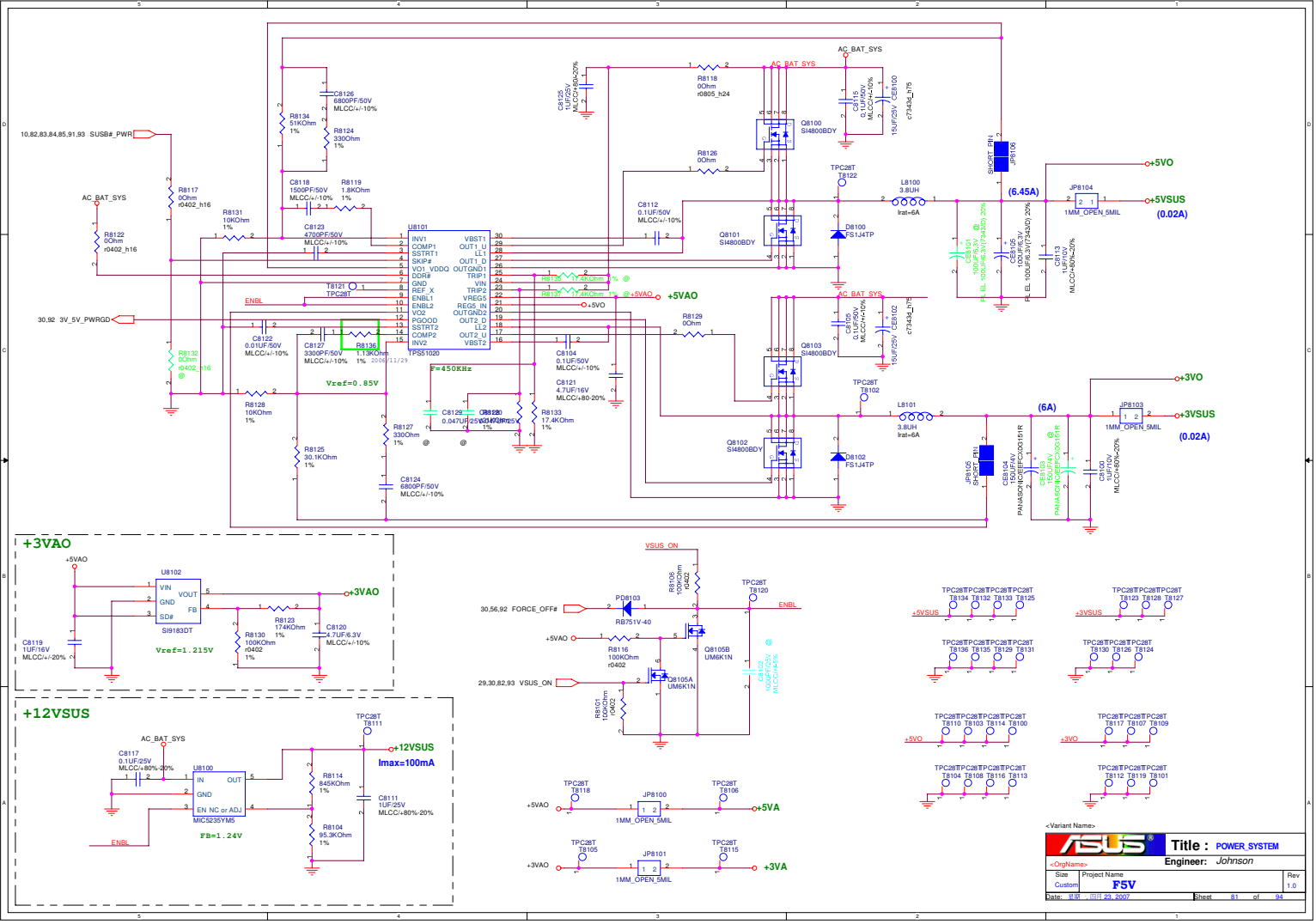
Title : Power sequence

Engineer: Kaxidy/Hawk

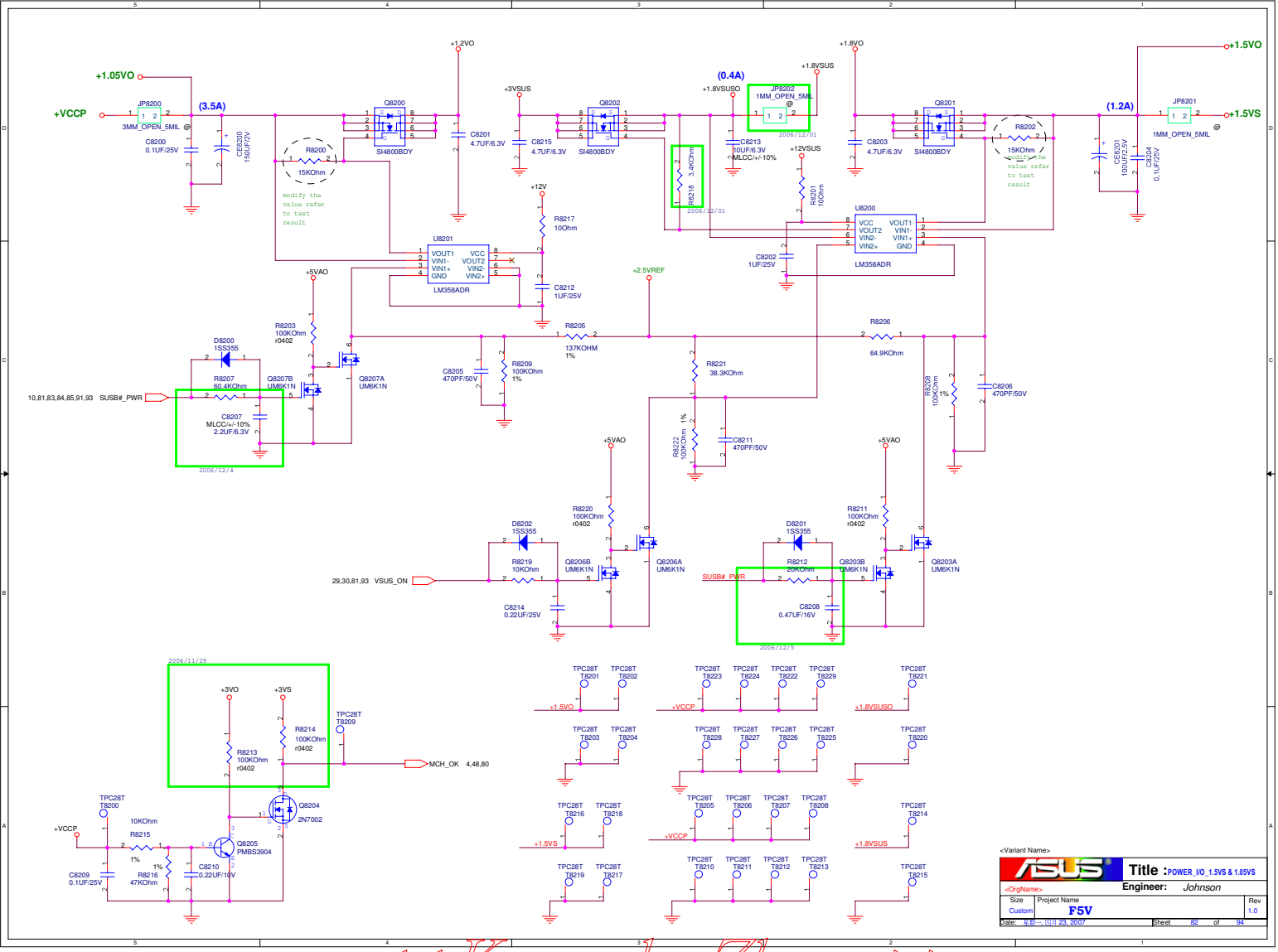
Size: C | Project Name: F5V | Rev: 1.0

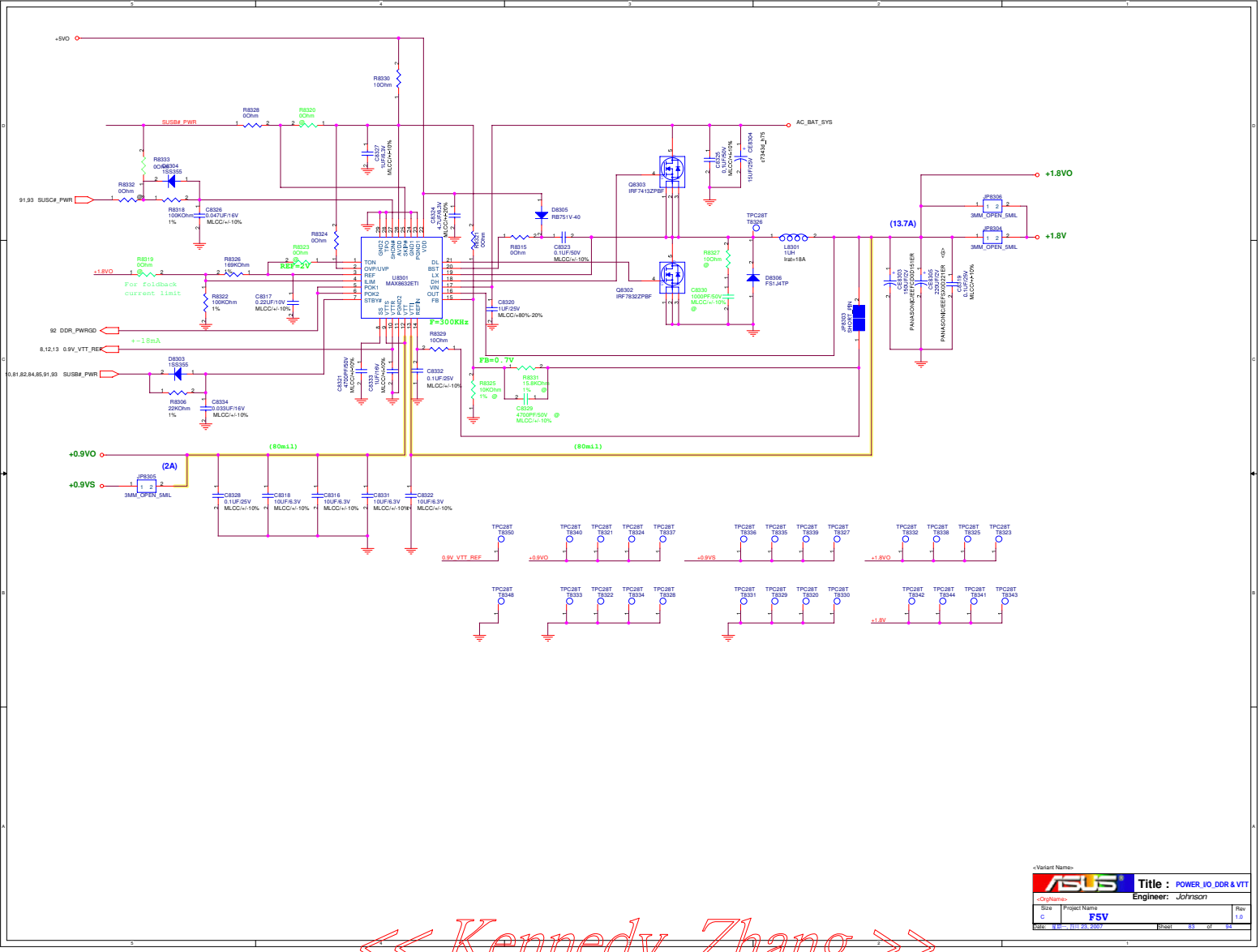
Date: 星期二, 四月 23, 2007 | Sheet 79 of 94





<< Kennedy_Zhang >>





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ASUS

Title : POWER_I/O_DDR & VTT

<OrgName>

Engineer: Johnson

Size	Project Name	Rev
C	P5V	1.0

Date: 日 8月 29, 2007 Sheet 83 of 94

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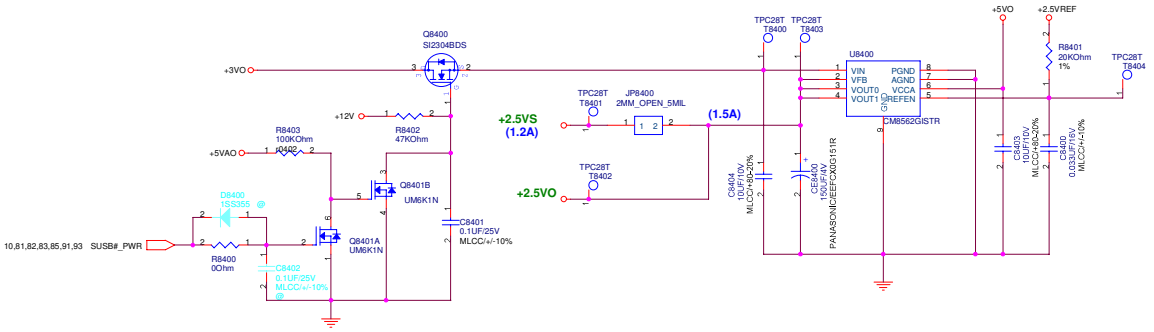
+2.5VS



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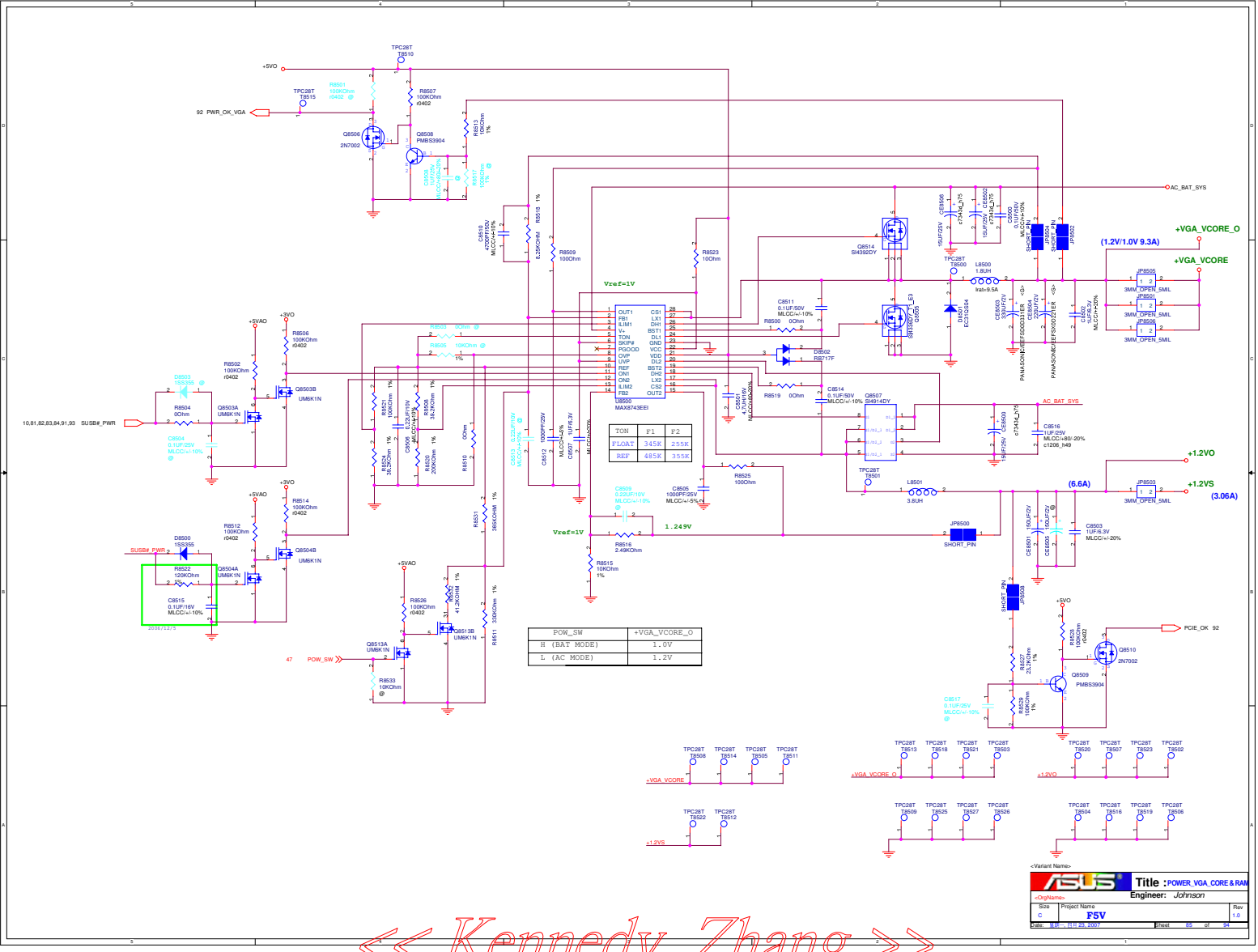
ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer: Johnson	
Size: Custom	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 84 of 94	



<< Kennedy_Zhang >>

<Variant Name>

Title : N/A

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Engineer: Johnson

Size	Project Name	Rev
B	F5V	1.0

Date: 星期 一, 四月 23, 2007 Sheet 86 of 94

<< Kennedy_Zhang >>

<Variant Name>

Title : N/A

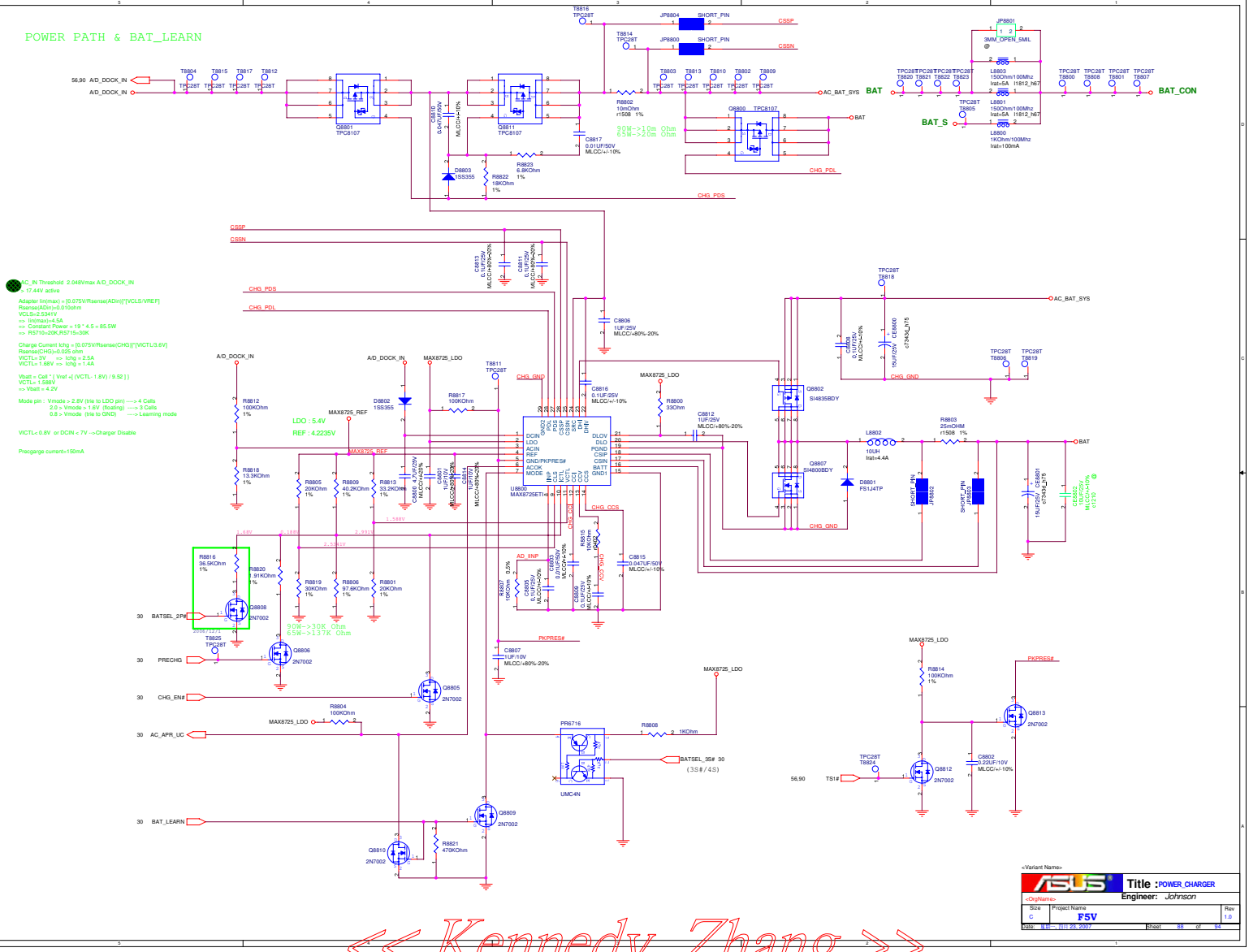
<OrgName>

Engineer: Johnson

Size	Project Name	Rev
Custom	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 87 of 94

<< Kennedy_Zhang >>



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Title : N/A

<OrgName>

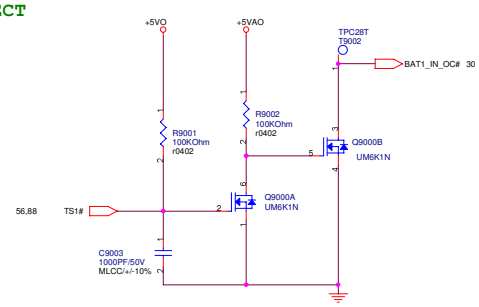
Engineer: Johnson

Size	Project Name	Rev
Custom	F5V	1.0

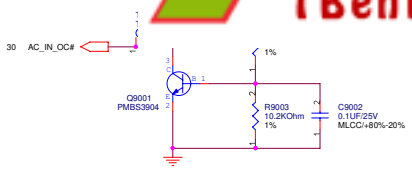
Date: 星期一, 四月 23, 2007 Sheet 89 of 94

<< Kennedy_Zhang >>

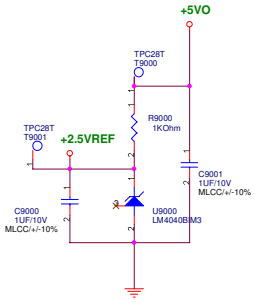
BATTERY IN DETECT



ADAPTER IN DETECT



+2.5VREF



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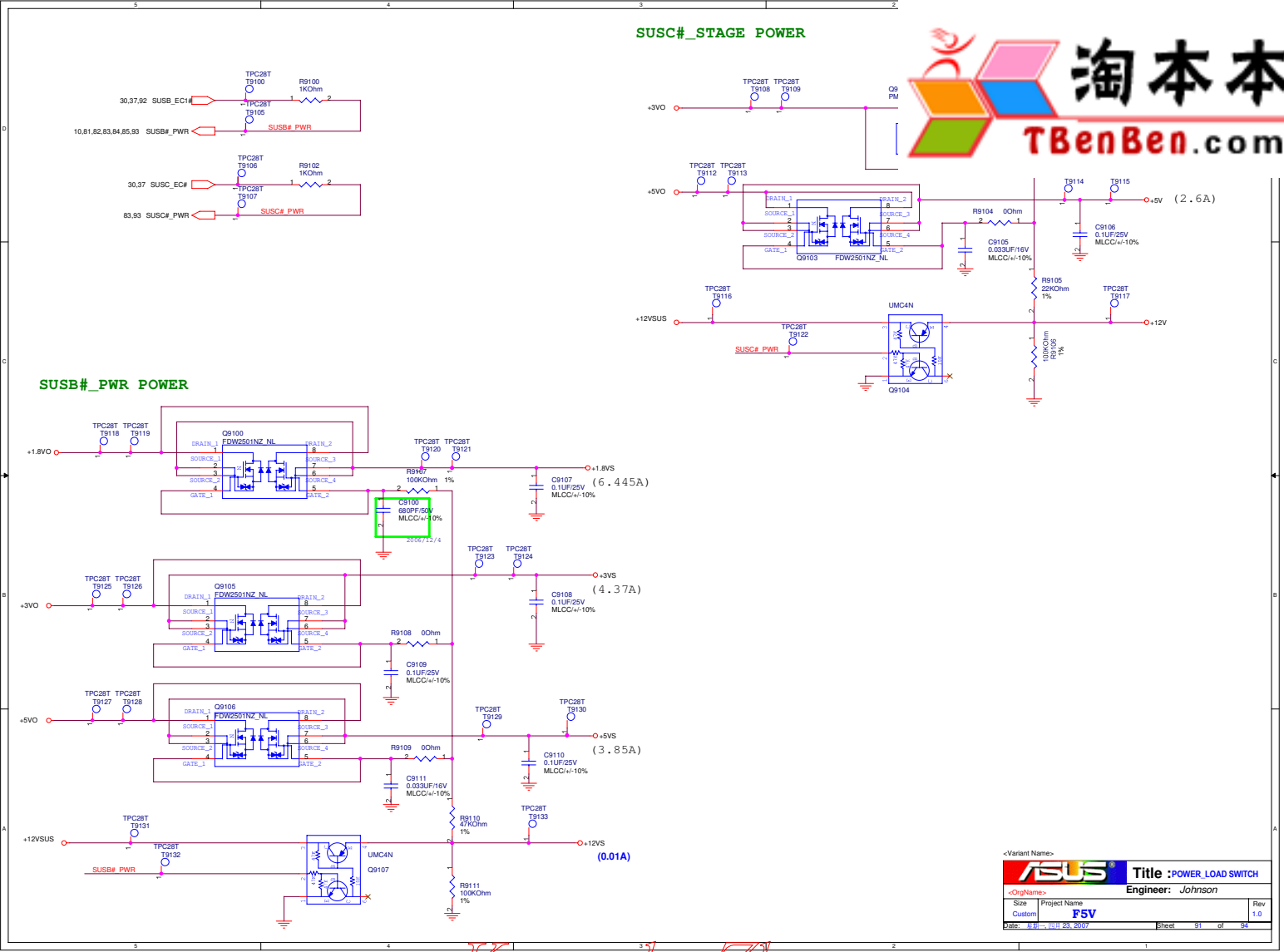
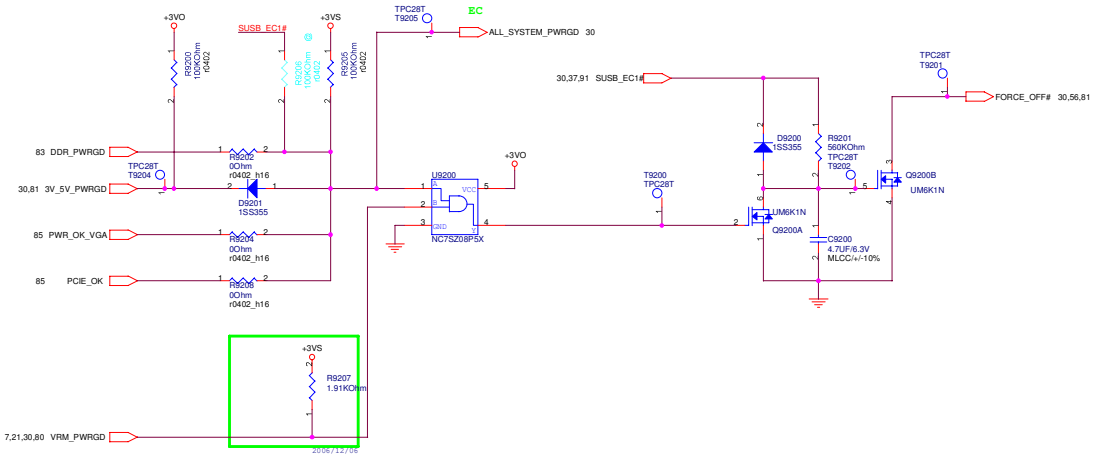
<OrgName>	Title : POWER_DETECT	
	Engineer: Johnson	
Size: Custom	Project Name: F5V	Rev: 1.0
Date: 五月 一, 向月 23, 2007	Sheet 90 of 94	



POWER GOOD DETECTER



<Variant Name>

<OrgName>	Title : POWER_PROTECT	
	Engineer: Johnson	
Size: Custom	Project Name: F5V	Rev: 1.0
Date: 五月 一, 向日 23, 2007	Sheet 92 of 94	

AC_BAT_SYS — AC_BAT_SYS 17,56,80,81,83,85,88
+3VA — +3VA 5,17,21,30,31,37,81
+5VA — +5VA 10,81

+5VO — +5VO 34,81,83,84,85,90,91
+3VO — +3VO 81,82,84,85,91,92
+3VSUS — +3VSUS 8,9,19,20,21,22,23,24,29,30,33,34,36,38,42,57,81,82
+5VSUS — +5VSUS 24,33,57,81
+3V — +3V 2,7,17,19,21,23,24,33,36,37,38,40,91
+3VS — +3VS 2,4,5,7,12,13,17,18,19,20,21,22,23,24,25,26,29,30,31,32,37,40,46,47,48,52,53,55,80,82,91,92

+12VSUS — +12VSUS 10,81,82,91
+12V — +12V 37,82,84,91
+12VS — +12VS 17,26,37,91

+5V — +5V 17,26,27,33,37,59,91
+5VS — +5VS 5,18,25,26,30,31,32,34,37,38,42,52,55,80,91

+2.5VO — +2.5VO 84
+2.5VS — +2.5VS 37,53,84
+1.8VO — +1.8VO 82,83,91
+1.8VSUS — +1.8VSUS 10,21,22,23,57,82
+1.8V — +1.8V 8,10,12,13,15,37,83
+1.8VS — +1.8VS 6,7,8,10,14,20,21,22,23,37,48,49,51,52,53,91
+1.5VS — +1.5VS 3,19,29,37,82
+VCCP — +VCCP 2,4,6,7,10,23,24,37,82

+0.9VS — +0.9VS 15,37,83
BAT — BAT 88

+2.5VREF — +2.5VREF 82,84,90
+VCORE — +VCORE 3,80

+VGA_VCORE — +VGA_VCORE 48,52,53,85

+1.2VO — +1.2VO 82,85
+1.2VS — +1.2VS 10,37,53,85

BAT_CON — BAT_CON 56,88

FOR POWER TEST

+3VA — JP9300 (SGL_JUMP) — CPU_VRON_PWR 80
JP9301 (SGL_JUMP) — SUSB#_PWR — SUSB#_PWR 10,81,82,83,84,85,91
JP9302 (SGL_JUMP) — SUSC#_PWR — SUSC#_PWR 83,91
JP9303 (SGL_JUMP) — VSUS_ON — VSUS_ON 29,30,81,82

CHANGE LIST

2006/11/29	1. Pull high R8213 to +3VO , 2. change C8334 to 0.1uF, 3.change R8136 to 1.13KOhm
2006/12/01	1. change R8218 to 3.4KOhm, 2. add JP8202, 3. delete R8055, 4.add Q8808 & R8816
2006/12/04	1. change C8207 to 2.2uF & R8207 to 60.4KOhm , 2. delete R8055, 3.change C9910 to 680pF
2006/12/05	1. change C8208 to 0.47uF & R8212 to 20KOhm. 2. change C8515 to 0.1uF & R8522 to 120KOhm.
2006/12/05	1.change R9207 to 1.91KOhm
2007/01/12	1. change input cap footprint. 2. add necessary TP.
2007/01/30	1. C8207 to 2.2uF/6.3V

<Variant Name>

ASUS — Title : POWER_SIGNAL
<OrgName> — Engineer: Johnson
Size: Custom | Project Name: F5V | Rev: 1.0
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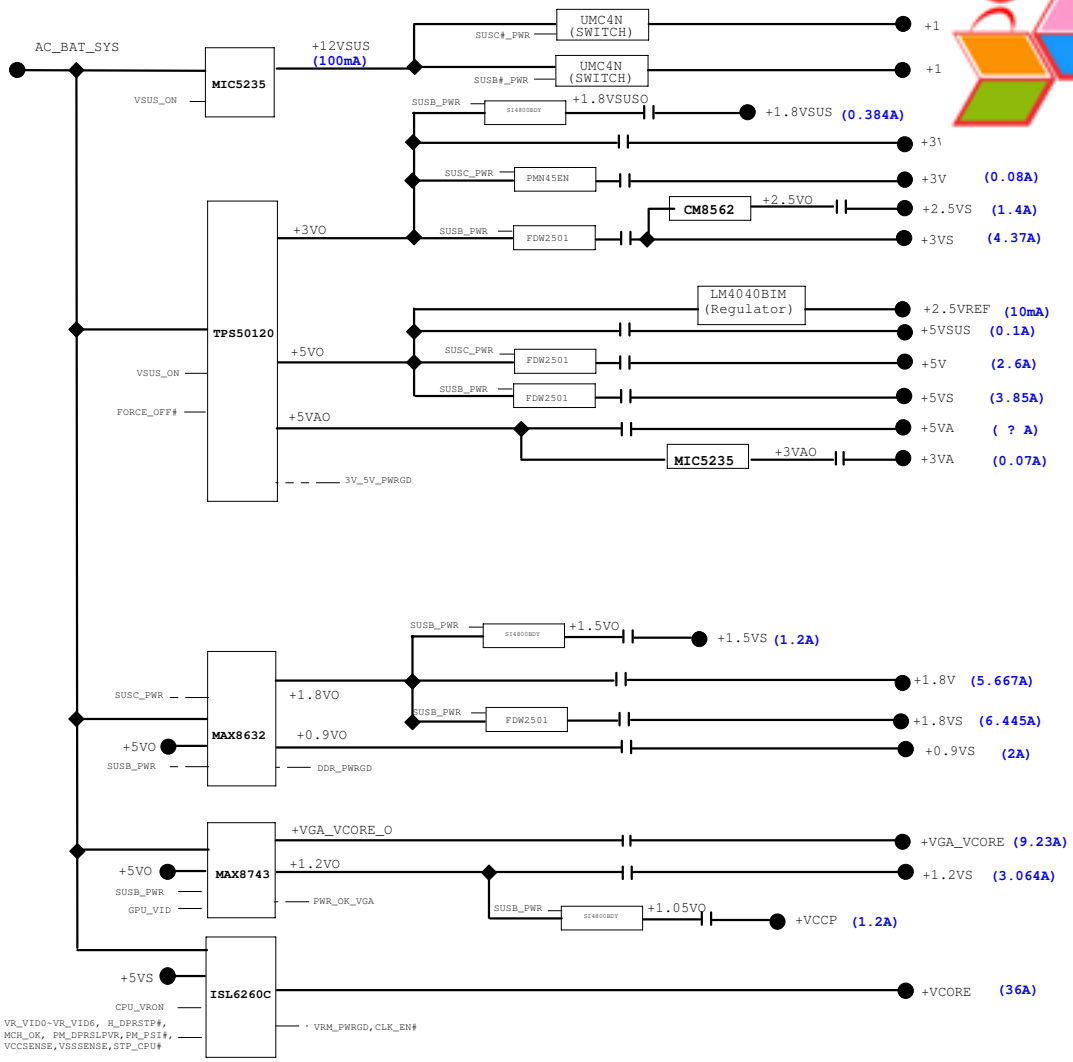

<Variant Name>

Title : POWER_FLOWCHART

<OrgName>

Engineer: Johnson

Size	Project Name	Rev
Custom	F5V	1.0

Date: 日期 , 四月 25, 2007 Sheet 94 of 94