


E540

NM-A161 Rev1.0 Schematic

***Intel Haswell Processor with DDRIII + Lynx point PCH
nVIDIA N14P-GV2/ N14M-GL***

2013-07-11 Rev 1.0

Security Classification	LC Future Center Secret Data			Title Cover Page			
Issued Date	2012/12/05	Deciphered Date	2014/12/05	Size Custom	Document Number E540 NM-A161	Rev 1.0	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Date:	Thursday, July 11, 2013	Sheet	1 of 57

N14P-GV2 2G
N14M-GL 1G
 VRAM 128M*16 *4
 VRAM 256M*16 *4
 Page 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33

PCI-Express 16X Gen3
 PEG 0~7

Intel CPU
Haswell
rPGA-989
 37.5mm*37.5mm
 Page 5, 6, 7, 8, 9, 10, 11

Memory BUS (DDRIII)
Dual Channel
 1.35V DDRIII 1066/1333/1600 MT/s

DDR3-SO-DIMM X2
 BANK 0, 1, 2, 3
 UP TO 16G

HDMI Conn.
 HDMI 1.4b Page 36

HDMI
 1.65GT/s

eDP Conn.
 Page 35

eDP
 3.3V 5.4GT/s

DP
Docking Conn
 USB 3.0 Port 1
 Page 51

DMI *4
 5GT/s

FDI *2
 5GT/s

CRT Conn.
 Page 35

CRT

Small Board

Realtek RTL8111G
 LAN Board

Realtek RTS5227
 USB Charge Port
 Card Reader Board

ODD Board For 15"
 Card Reader Board

JRJ45 Conn.
 PCIe port 4 Page 42

PCIe Gen1
 1.5V 2.5GT/s

JUCR Conn.
 PCIe port 3 Page 43

PCIe Gen1
 1.5V 2.5GT/s

SATA ODD For 15"
 SATA Port 2 Page 44

SATA Gen1 Port2
 5V 3GHz(150MB/s)

SATA ODD For 14"
 SATA Port 2 Page 45

SATA HDD
 SATA Port 1 Page 44

SATA Gen3 Port 0
 5V 6GHz(600MB/s)

SPI ROM
 (4MB+8MB)
 Page 17

SPI BUS
 3.3V 33MHz

Intel PCH
Lynx point
 695 ball FCBGA
 20mm*20mm
 Page 14, 15, 16, 17, 18, 19, 20, 21, 22

USB 3.0
 5V 500MB/S

USB Left
 USB 3.0 Port 2
 USB 3.0 Port 5
 Page 50

USB 2.0
 5V 60MB/S

Touch panel
 USB 2.0 Port 4
 Page 51

USB Right
 USB 2.0 Port 5
 Sub Board Page 50

Int. Camera
 USB 2.0 Port 13
 Page 34

USB 2.0
 5V 60MB/S

PCleMini Card
 WLAN
 PCIe Port 5
 USB 2.0 Port 10
 Page 37

mSATA SSD
 SATA Port 0
 Page 37

PCleMini Card
 WWAN
 USB 2.0 Port 11
 Page 38

PCIe Gen1
 5V 2.5GT/s

SATA Gen3
 5V 6GHz(600MB/s)

HD Audio
 3.3V 24MHz

Codec
COX 20751
 Page 45

SPK Conn.
 Page 46

Int. Comb Conn.
 (Ext MIC & HP)
 Page 34

SMBus

LPC BUS
 3.3V 33MHz

Debug Port
 Page 45

EC
ITE IT8586E-CX
 Page 47

PS2

Click Pad
 SMBus Port3
 Page 47

Track Point
 SMBus
 Page 48

ADC

G-Sensor
LIS34ALTR
 Page 47

Int. K/B

Int.KBD
 Page 46

SMBus

Thermal Sensor
EMC 1403
 SMBus Port3
 Page 40

Security EEPROM
 SMBus Port3
 Page 41

Power Circuit DC/DC
 Page 52, 53, 54, 55, 56, 57,
 58, 59, 60, 61, 62

DC/DC Interface CKT.
 Page 51

Finger Print Conn
 Page 56

POWER/B Conn.
 Page 40

ODD/B Conn.
 page 41

Touch Pad Conn
 Page 56

Click Pad Conn
 Page 55

SIM Conn
 Page 54

Track Point Conn
 Page 53

Security Classification		LC Future Center Secret Data					
Issued Date		2012/12/05		Deciphered Date		2014/12/05	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.							

E540 NM-A161
 Rev 1.0

<div>Power Plane</div> <div>State</div>	B+	+3VALW +5VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

USB Port Table

BOM Structure Table

SMBUS Control Table

PCIE PORT LIST

EC SM Bus2 address

PCH SM Bus address

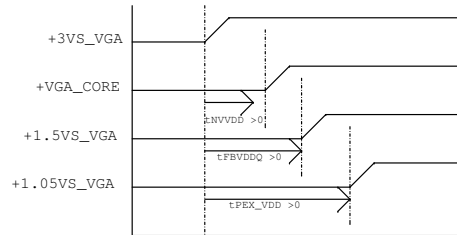
Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

Title			
Notes List			
Size	Document Number	Rev	
Custom	E540 NM-A161	1.0	
Date	Thursday, July 11, 2013	Sheet	2 of 57

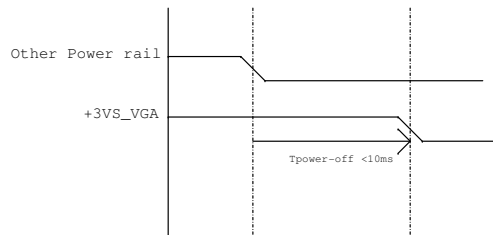
Hot plug detect for IFP link E

VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	-	VGA_BL_PWM
GPIO3	OUT	-	VGA_ENVDD
GPIO4	OUT	-	VGA_ENBKL
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	-	DPRSLPVR_VGA
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	GPIO9
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	-	FB_CLAMP_TOGGLE_REQ#
GPIO15	IN	N/A	(100K pull low)
GPIO16	OUT	-	FRMLCK#
GPIO17	IN	N/A	
GPIO18	IN	-	dGPU_HDMI_HPD
GPIO19	IN	-	HPD_IRQ



1. all power rail ramp up time should be larger than 40us



1. all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

Products	GPU (4)	Mem (1,5)	NVCLK /MCLK (MHz)	NVVDD (V)			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
(W)	(W)	(W)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

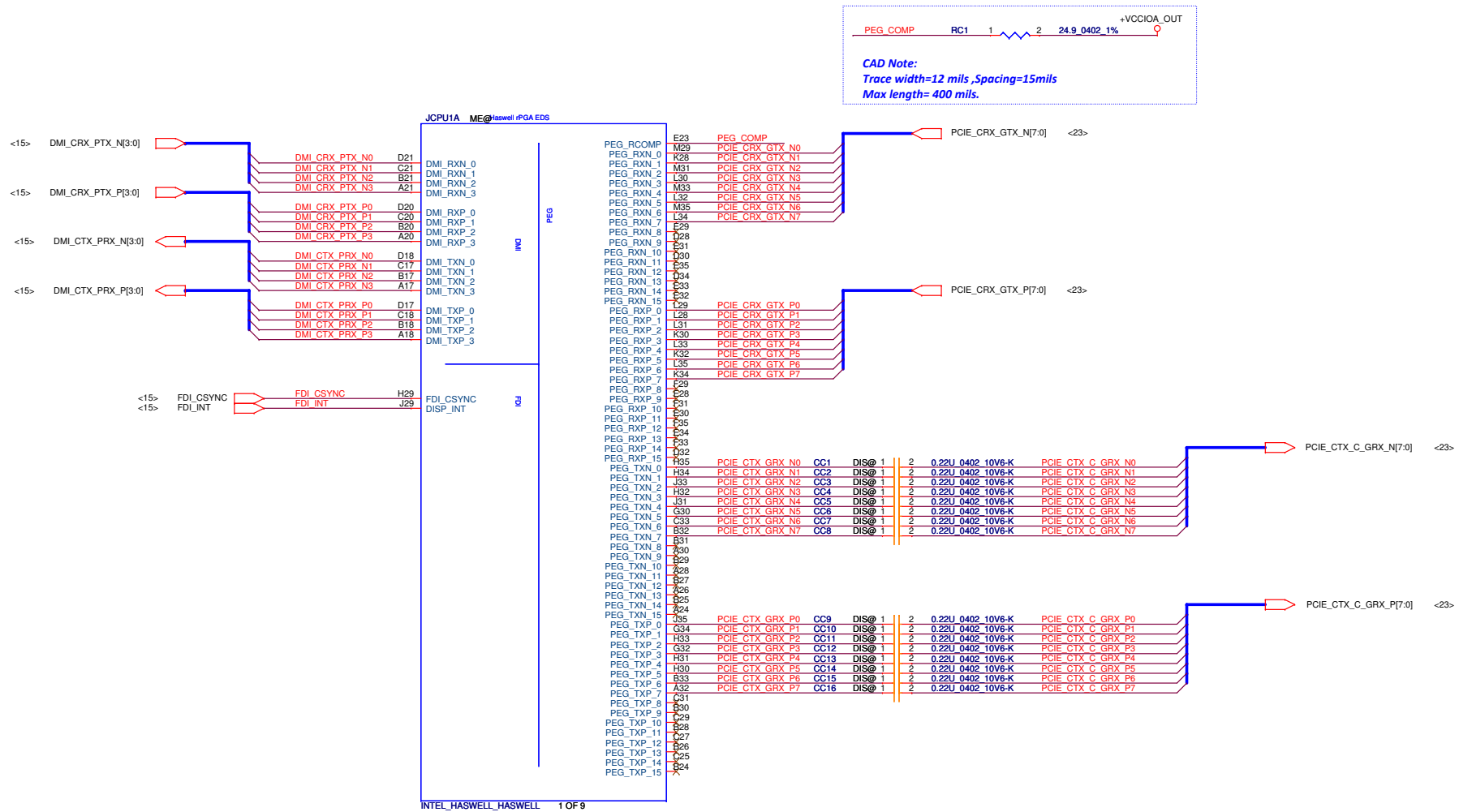
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

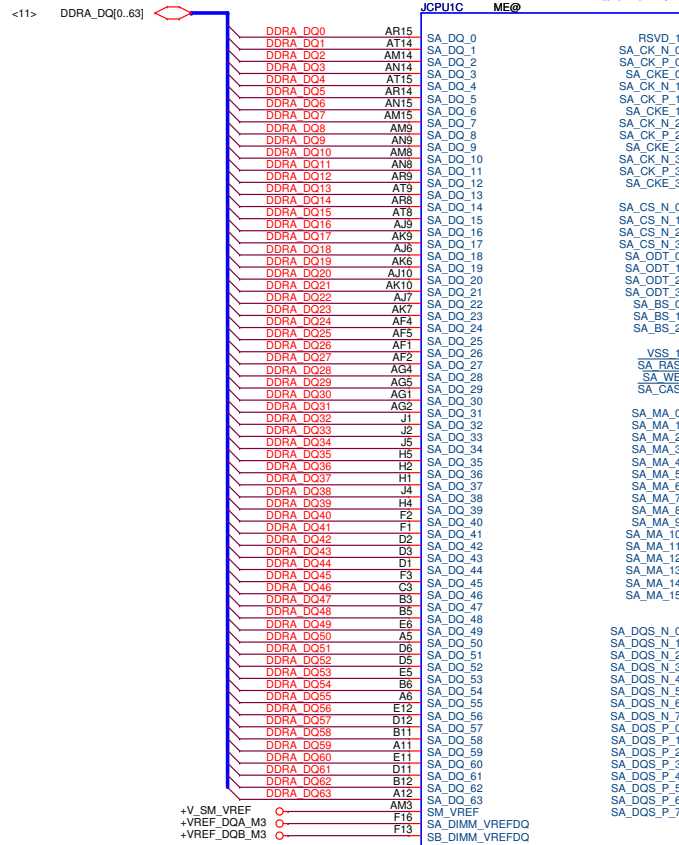
	Device ID		setting	I2C Slave addresses ID
N13P-GT (28nm)	0x0FDB	SMB_ALT_ADDR (ROM_SO Bit 1)	0	0x9E
			1	0x9C

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	PU 10K	PU 25K	PU 45K	PD 35K	PD 10K	PU 5K	PD 10K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

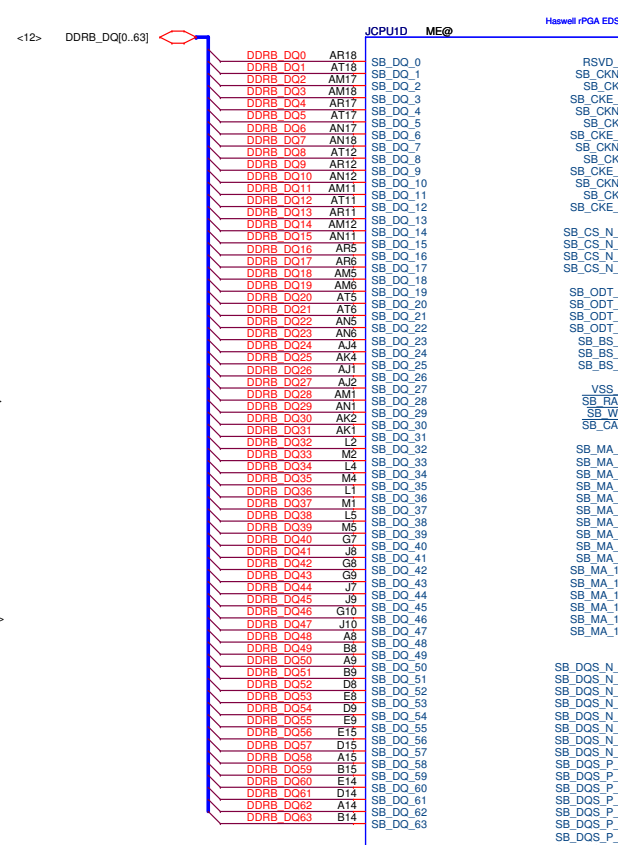
GPU		N13P-GT		
FB Memory (GDDR5)		ROM_SI		
Samsung 2500MHz	K4G10325FG-HC04			
	32Mx32	PD 45K		
Hynix 2500MHz	H5GQ1H24BFR-T2C			
	32Mx32	PD 35K		
Samsung 2500MHz	K4G20325FD-FC04			
	64Mx32	PD 30K		
Hynix 2500MHz	H5GQ2H24MFR-T2C			
	64Mx32	PD 25K		

Security Classification	LC Future Center Secret Data				Title	
Issued Date	2012/12/05	Deciphered Date	2014/12/05		VGA Notes List	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					Size Custom	Document Number E540 NM-A161
					Date: Thursday, July 11, 2013	Rev 1.0
					Sheet 4 of 57	

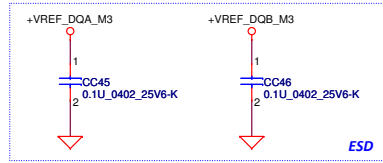




INTEL_HASWELL_HASWELL 3 OF 9

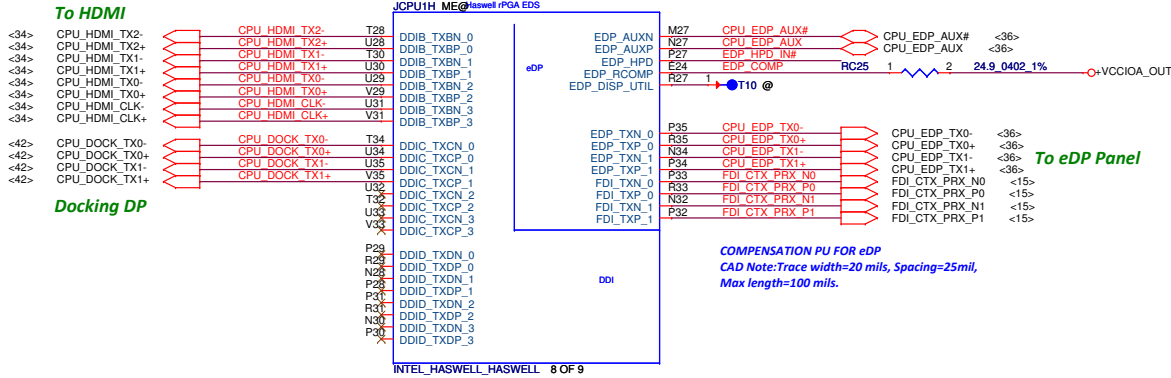


INTEL_HASWELL_HASWELL 4 OF 9

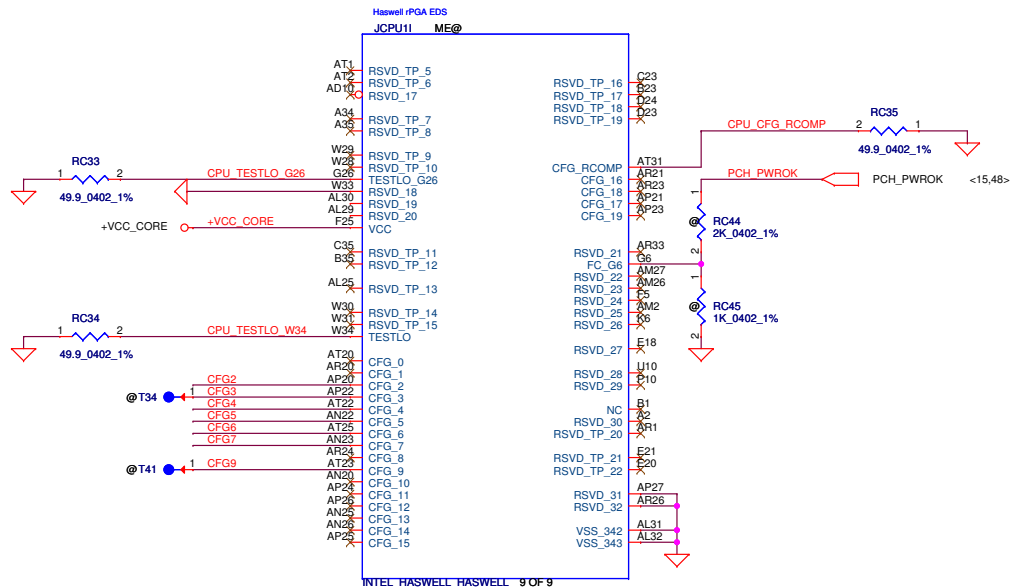


ESD

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/12/05	Deciphered Date	2014/12/05	CPU_DDR3 INTERFACE	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size Custom	Document Number E440 NM-A151
				Date: Thursday, July 11, 2013	Rev 1.0



CFG STRAPS For CPU (CFG[17:0] internal pull high 5 ~15K to VCCIO)



PEG Static Lane Reversal - CFG2 is for the 16x

CFG2

- * 1: (Default) Normal Operation; Lane# definition matches socket pin map definition
- 0: Lane Reversed

Display Port Presence Strap

CFG4

- 1: Disabled
- No Physical Display Port attached to Embedded Display Port
- * 0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps

CFG[6:5]

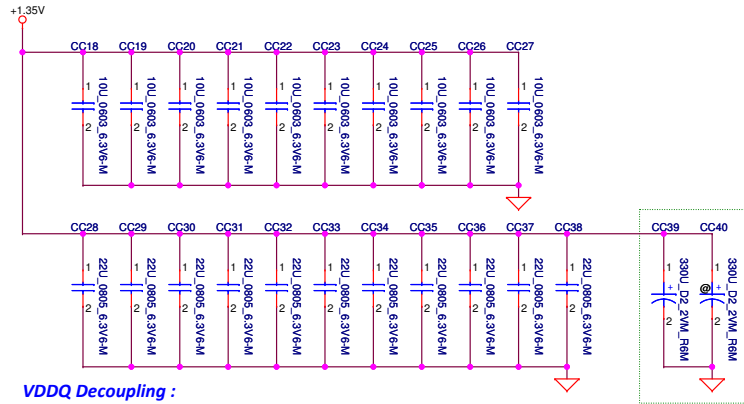
- 11: Func 1 Disabled, Func 2 Disabled (x16,---,---)
- * 10: Func 1 Enabled, Func 2 Disabled (x8,x8,---)
- 01: Func 1 Disabled, Func 2 Enabled
- 00: Func 1 Enabled, Func 2 Enabled (x8,x4,x4)

PEG DEFER TRAINING

CFG7

- * 1: (Default) PEG Train Immediately Following XXRESETB Deassertion
- 0: PEG Wait for BIOS for Training

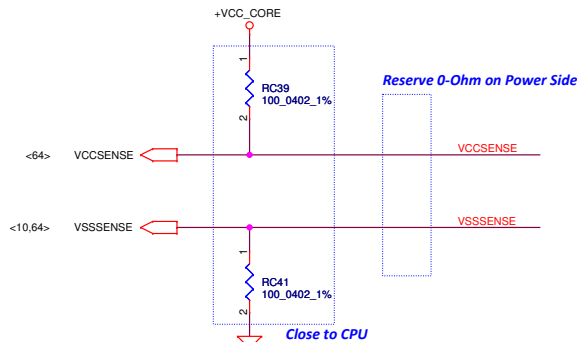
CPU VDDQ DECOUPLING



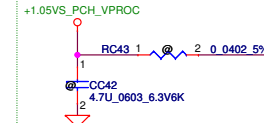
VDDQ Decoupling :

1. MB Bottom Socket Edge --> 2* 330uf, 6mΩ
2. 6x MB Bottom Socket Cavity --> 11* 22 μF (0805), 3mΩ
5x MB Top Socket Cavity
3. 5x MB Bottom Socket Cavity --> 10 x 10 μF (0805), 3mΩ
5x MB Top Socket Cavity

VCC/VSS SENSE

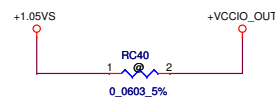


Reserve for VCCST.

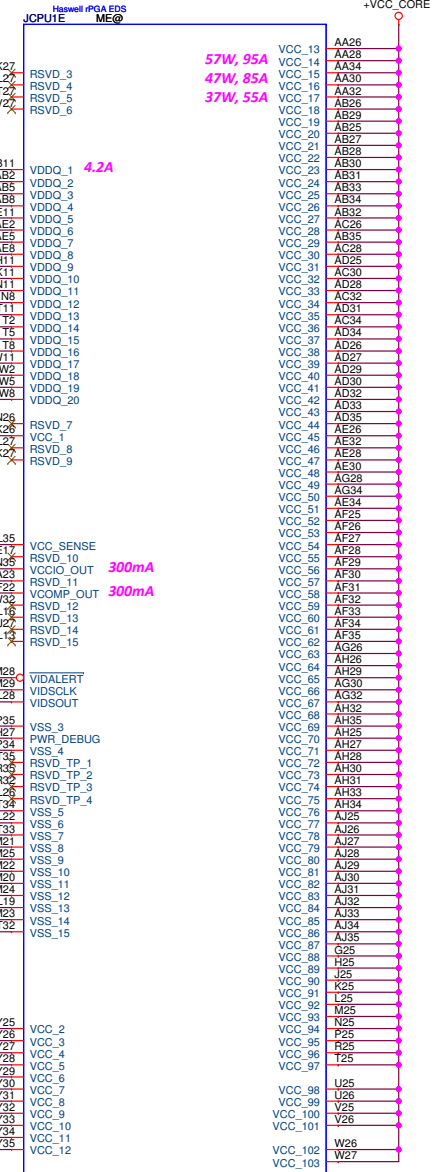


<64>	VR_SVID_ALRT#	RC36	1	2	43 0402 1%	H CPU_SVIDALRT#	AM28
<64>	VR_SVID_CLK	RC37	1	2	0 0402 5%	H CPU_SVIDCLK	AM29
<64>	VR_SVID_DAT	RC38	1	2	0 0402 5%	H CPU_SVIDDAT	AL28

Pull high resistor on VR side
+VCCIO_OUT

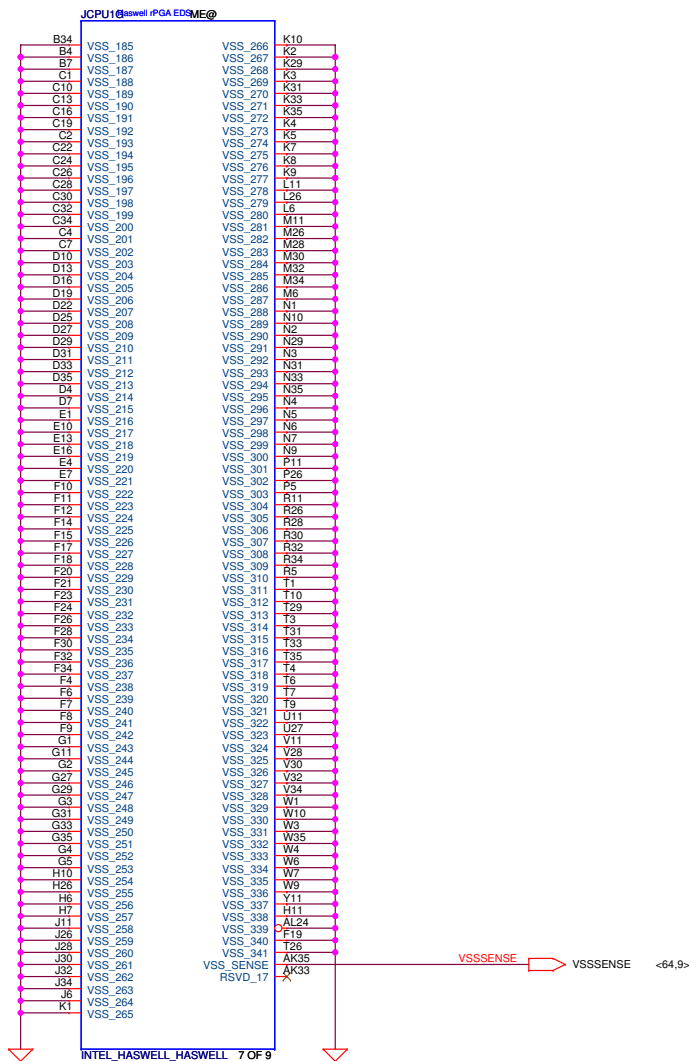
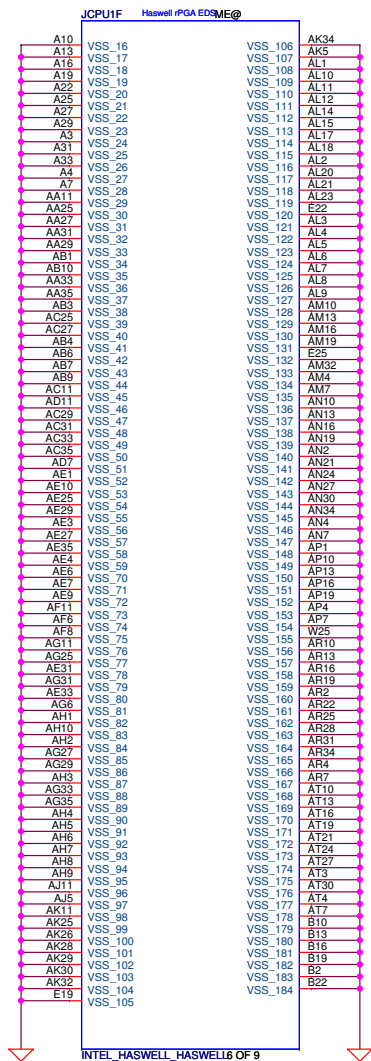


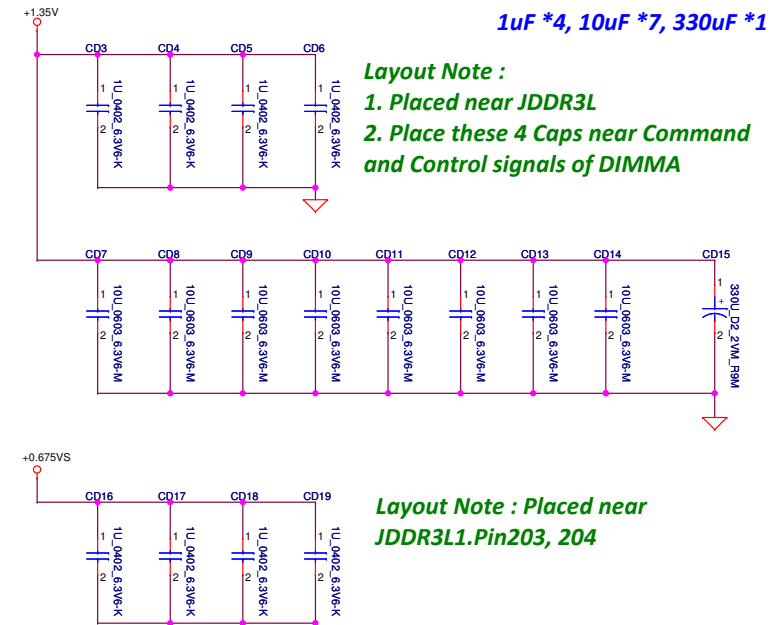
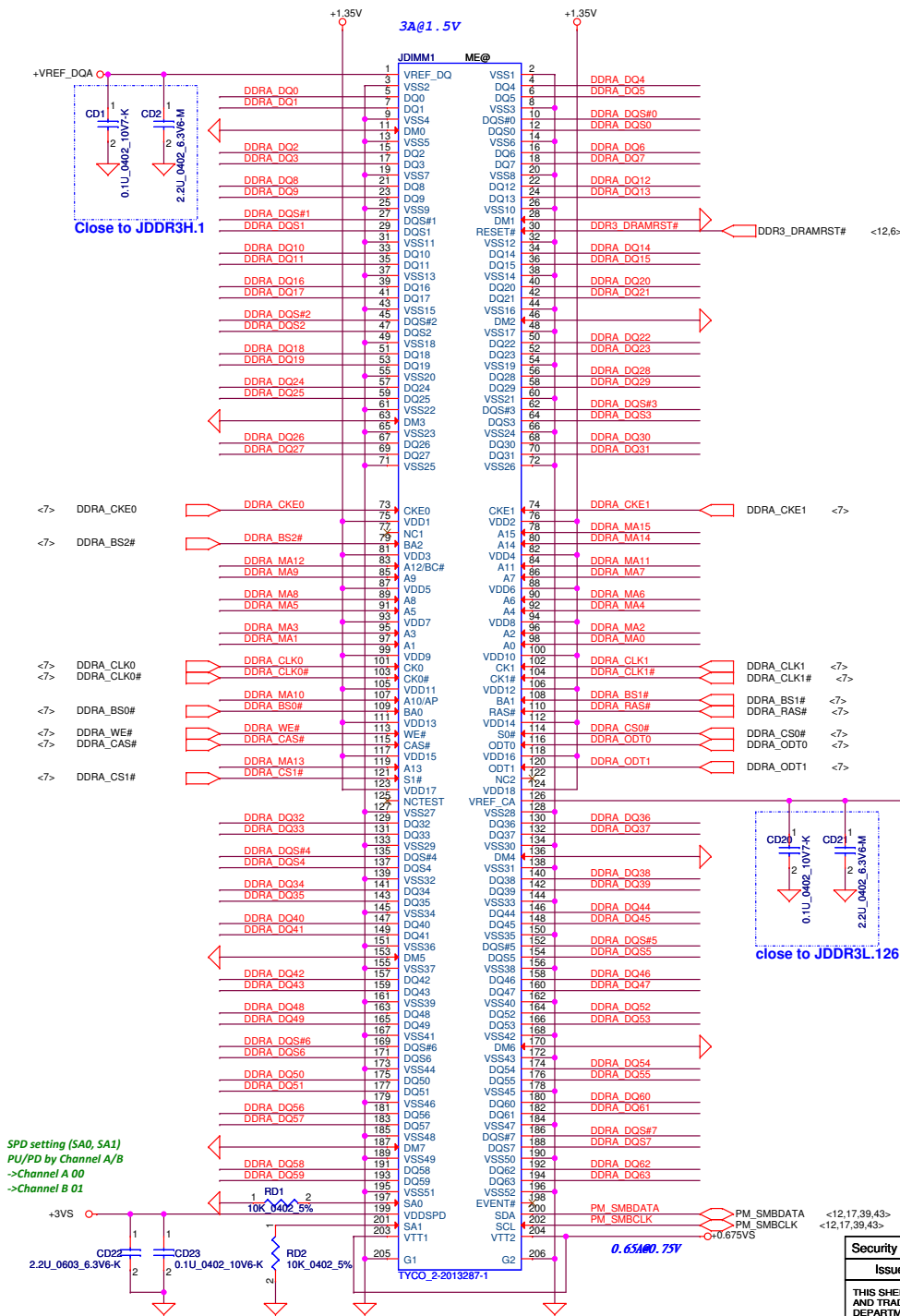
RESISTOR STUFFING OPTIONS ARE
PROVIDED FOR TESTING PURPOSES




Security Classification	LC Future Center Secret Data			Title
Issued Date	2012/12/05	Deciphered Date	2014/12/05	CPU_POWER
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				
Date:	Thursday, July 11, 2013	Sheet	9	of 57

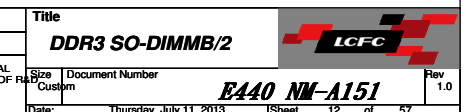
Size	Document Number	Rev
Custom	E440 NM-A151	1.0



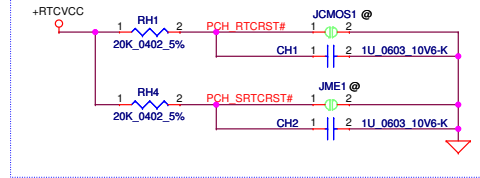
DDR3 SO-DIMM A

Security Classification		LC Future Center Secret Data		Title			
Issued Date	2012/12/05	Deciphered Date	2014/12/05	DDR3 SO-DIMMA/1			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RPL DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size	Document Number	E440 NW-A151	Rev 1.0
				Custom			
Date:				Thursday, July 11, 2013	Sheet	11	of 57

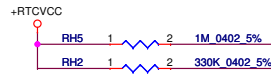
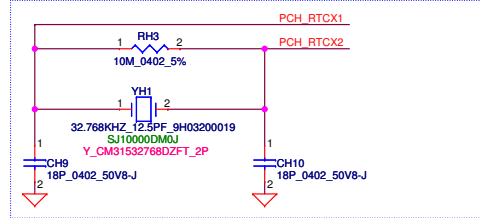
3A@1.5V



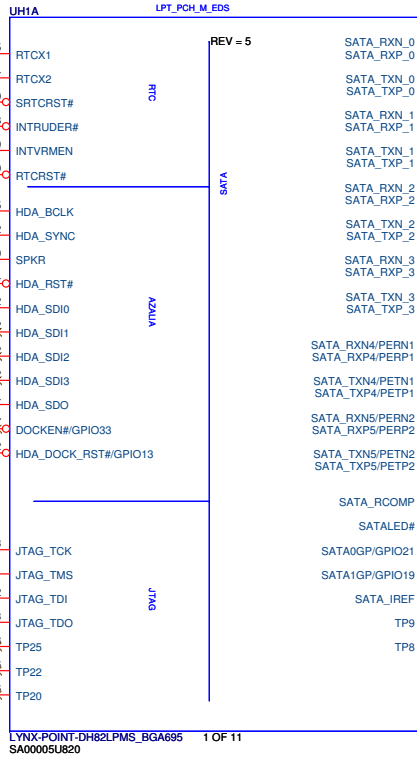
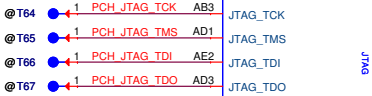
JCMOS, JME Setting, Need Under DDR Door



1. INTVRMEN, should always be pull high
H : Integrated VRM enable (Default)
L : Integrated VRM disable
2. Internal Voltage Regulator Enable:
This signal enables the internal 1.05 V regulators.

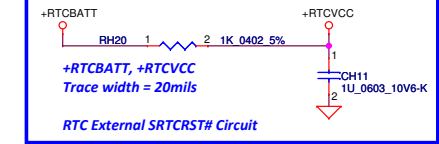


During Reset", Immediately after Reset and S3/S4/S5
1. JTAG_TDI, JTAG_TMS --> Int. PU 20K
2. JTAG_TCK --> Int. PD 20K
3. JTAG_TDO --> High-Z



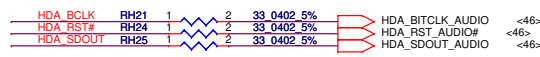
SATA Impedance Compensation :
--> Place the resistor within 500 mils of the PCH.
Avoid routing next to clock pins.

RTCVCV Circuit

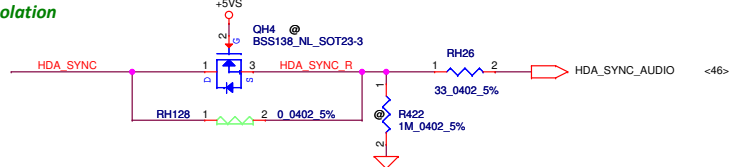


HDA AUDIO SIGNAL

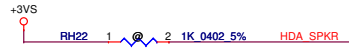
HDA AUDIO For Codec



Isolation



HDA STRAP

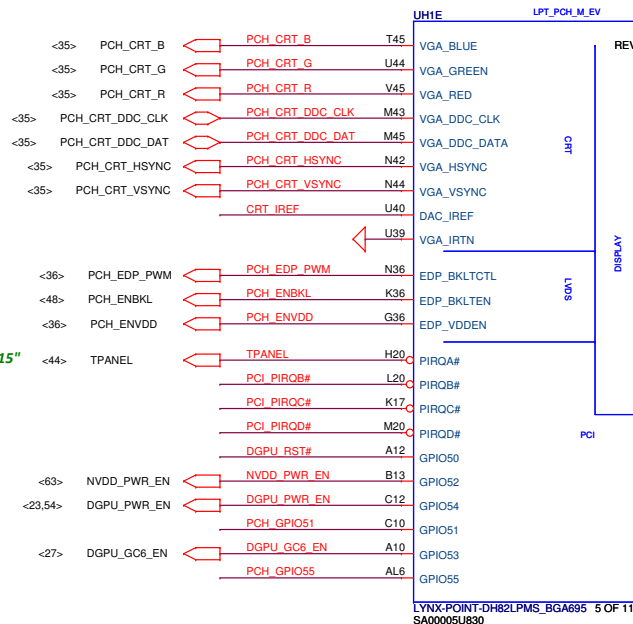
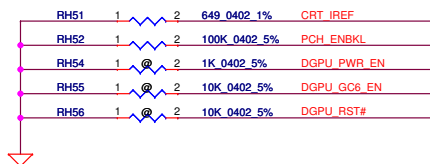
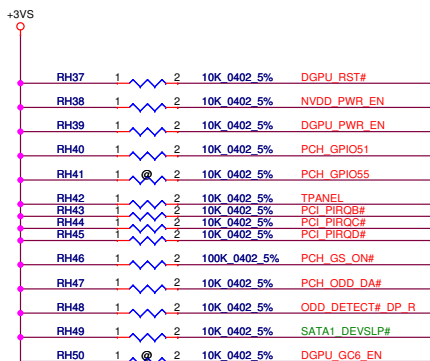
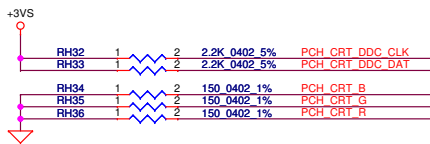


- HIGH= Enable (No Reboot)
- LOW= Disable (Default)
- 1. The internal pull-down is disabled after PLTRST# deasserts.
- 2. When Sampled : Rising edge of PWROK

1. This signal has a weak internal pull-down 15K
2. The internal pull-down on AZA_SYNC and AZA_SDO are enabled during reset.

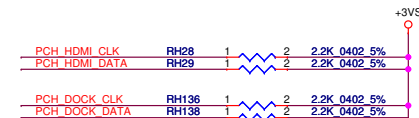
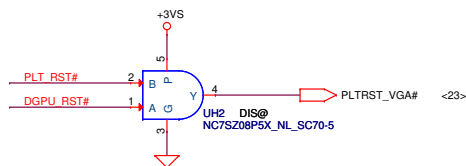
Security Classification	LC Future Center Secret Data	
Issued Date	2012/12/05	Deciphered Date
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.		

Title	Size	Document Number	Date	Thursday, July 11, 2013	Sheet	13	of	57
PCH_RTC/HDA/SATA	Custom	E440 NM-A151	Rev	1.0				



Only for 15"

+VGA_CORE
+3VS_VGA



To JIMIN1.Pin38
Integrated Pull-Up 20K

A16 swap override Strap/Top-Block
Swap Override jumper

PCI_GNT3#
Low = A16 swap
override/Top-Block
Swap Override enabled
★ **High=Default

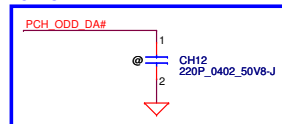
- The signal has a weak internal pull-up, which is disabled after PLTRST# deasserts.
- When sampled : Rising edge of PWROK

Boot BIOS Straps (BBS)

BBS_BIT1 (GPIO51)	BBS_BIT0 (GPIO19)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI ★

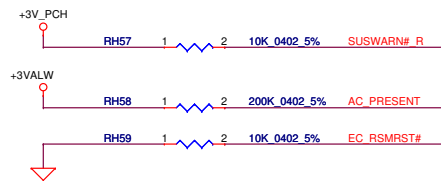
- GPIO51/19 has weak internal pull-up via 20kohm
- The internal pull-up is disabled after PLTRST# deasserts.
- GPIO51 (bit 11) at the rising edge of PWROK
SATA1GP/GPIO19 (bit 10) at the rising edge of PWROK.

For ESD

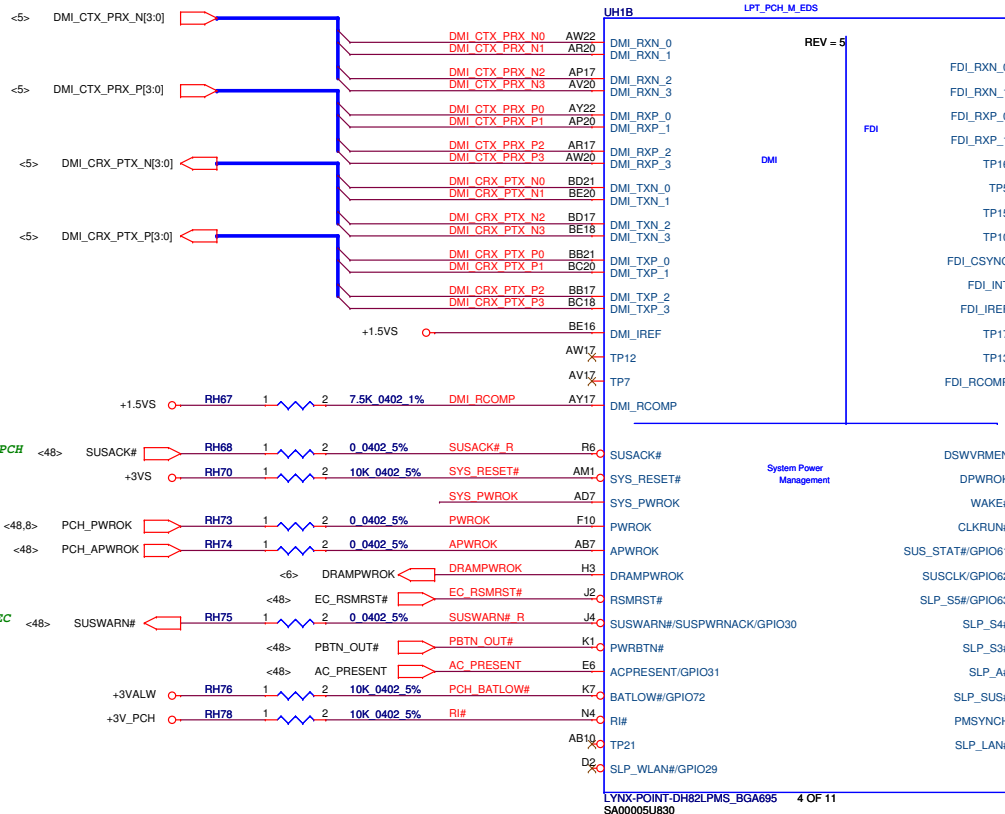
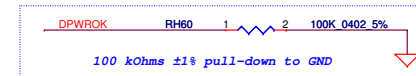
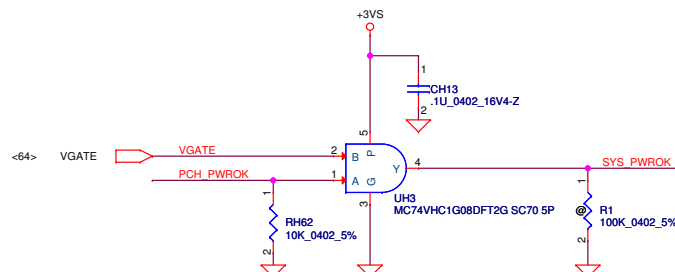


Security Classification			
LC Future Center Secret Data			
Issued Date	2012/12/05	Deciphered Date	2014/12/05
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.			

Title		Size	
PCH_CRT/EDP/DDP		Document Number	Custom
E540 NM-A161		Date:	Thursday, July 11, 2013
Rev 1.0		Sheet 14	of 57



SUSACK# R RH61 1 @ 2 0.0402 5% SUSWARN# R
 Stuff RH289 if EC does not want to involve in the handshake mechanism for the DeepSX state entry and exit

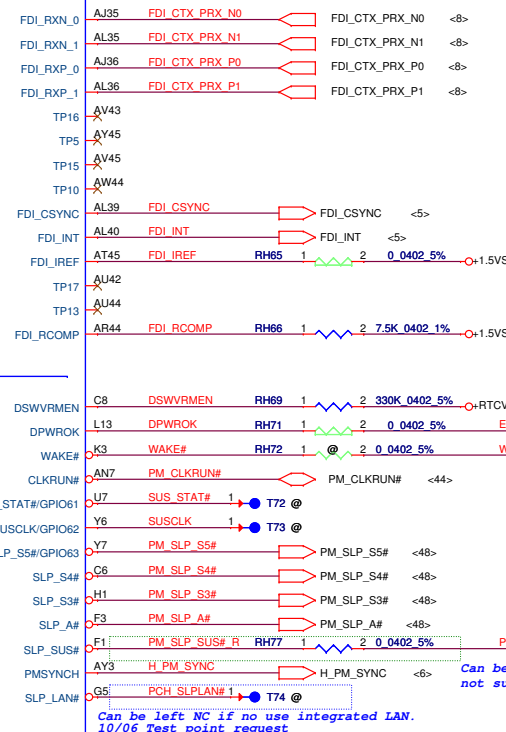


APWROK may come up earlier than PWROK but no later

PCH to EC

APWROK only for A phase

PWROK RH13 1 @ 2 0.0402 5% APWROK



DSXVRMEN must be always pulled high to +RTCVCC
 DSXVRMEN - Internal Deep Sleep 1.05V regulator
 ***H: Enable
 L: Disable

For Deep S3
 For WLAN WAKE# (Disable)

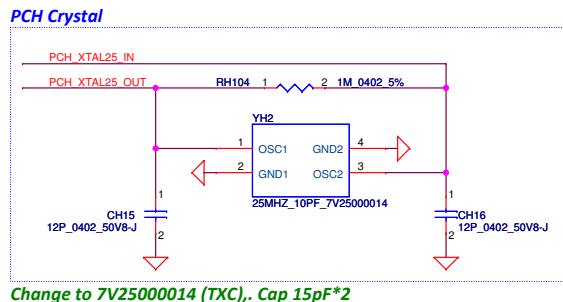
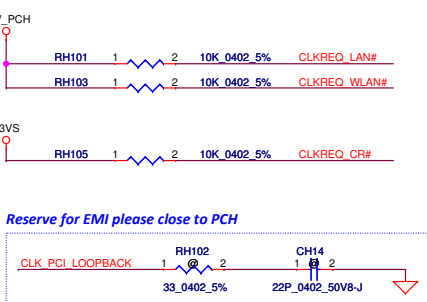
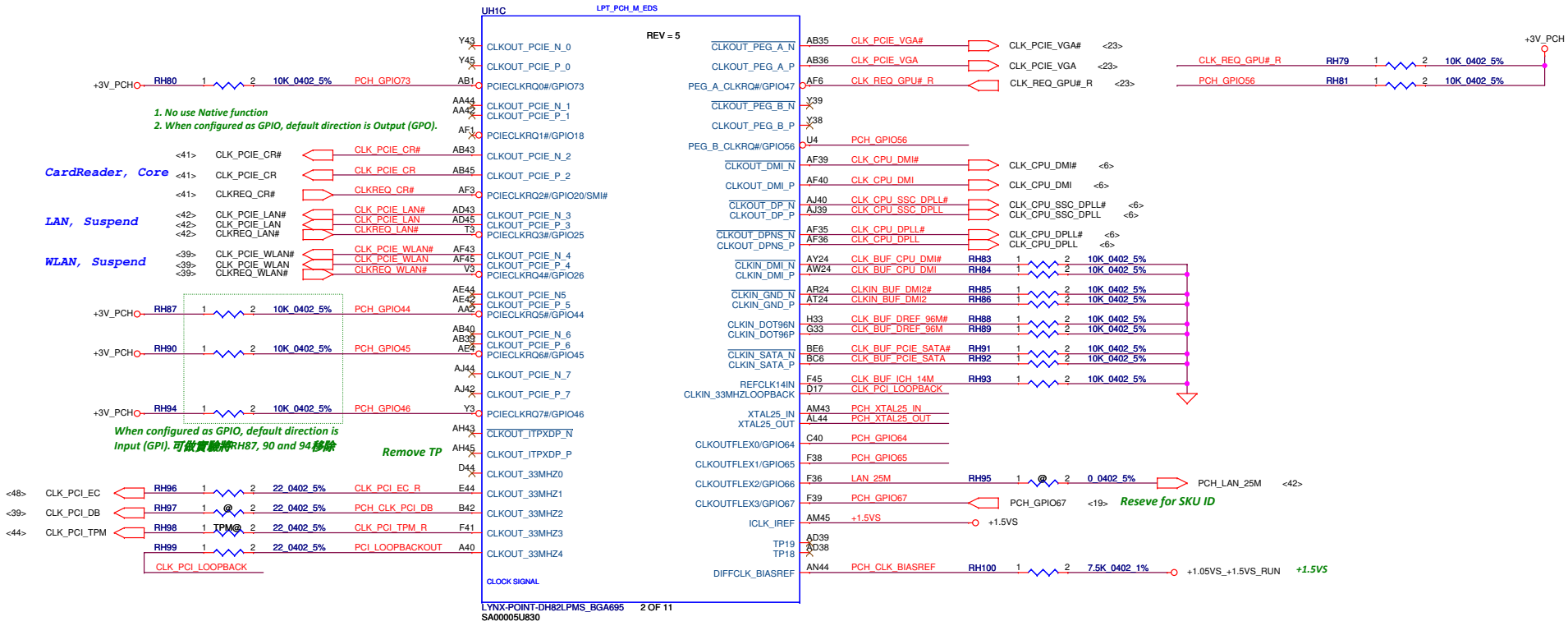
For Deep S3
 Can be left NC when IAMT is not support on the platform

SUSCLK#/GPIO62

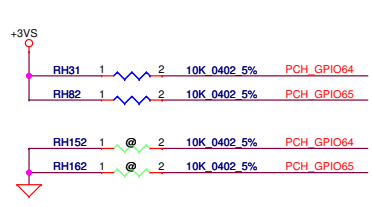
This signal has a weak internal pull-up.
 0 = Disable PLL On-Die voltage regulator.
 * 1 = Enable PLL On-Die voltage regulator.
 NOTES:
 1. The internal pull-up is disabled after RSMRST# deasserts.
 2. This signal is in the Suspend well.

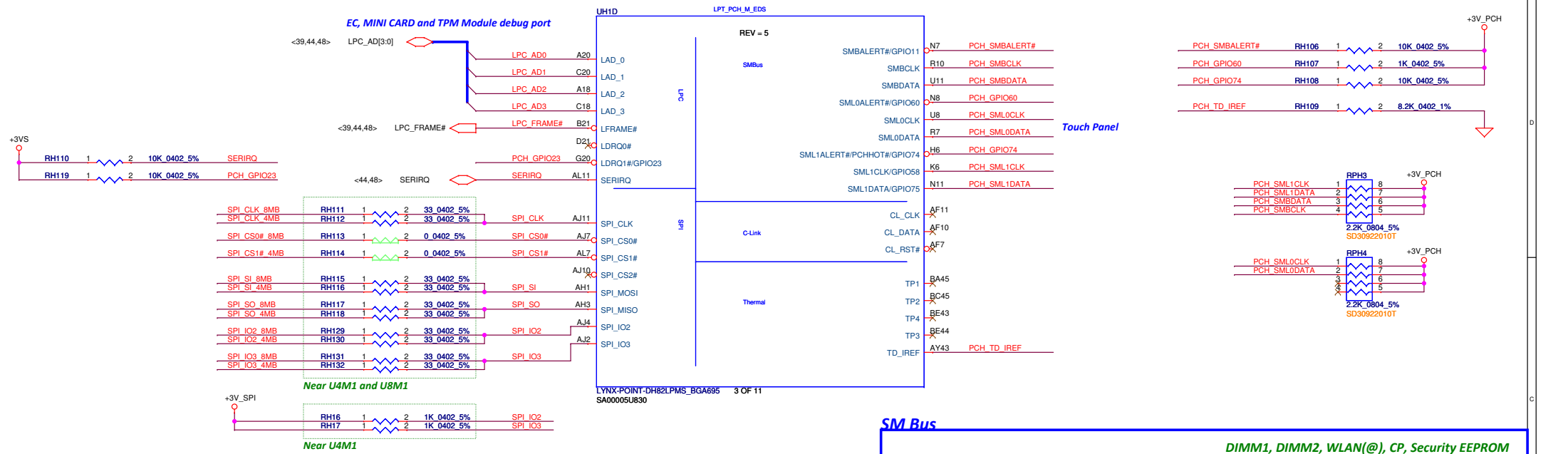
Security Classification			
LC Future Center Secret Data			
Issued Date	2012/12/05	Deciphered Date	2014/12/05
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.			

Title	
PCH_DMI/FDI/PM	
Size	Document Number
Custom	E440 NM-A151
Date	Thursday, July 11, 2013
Sheet	15 of 57
Rev	1.0

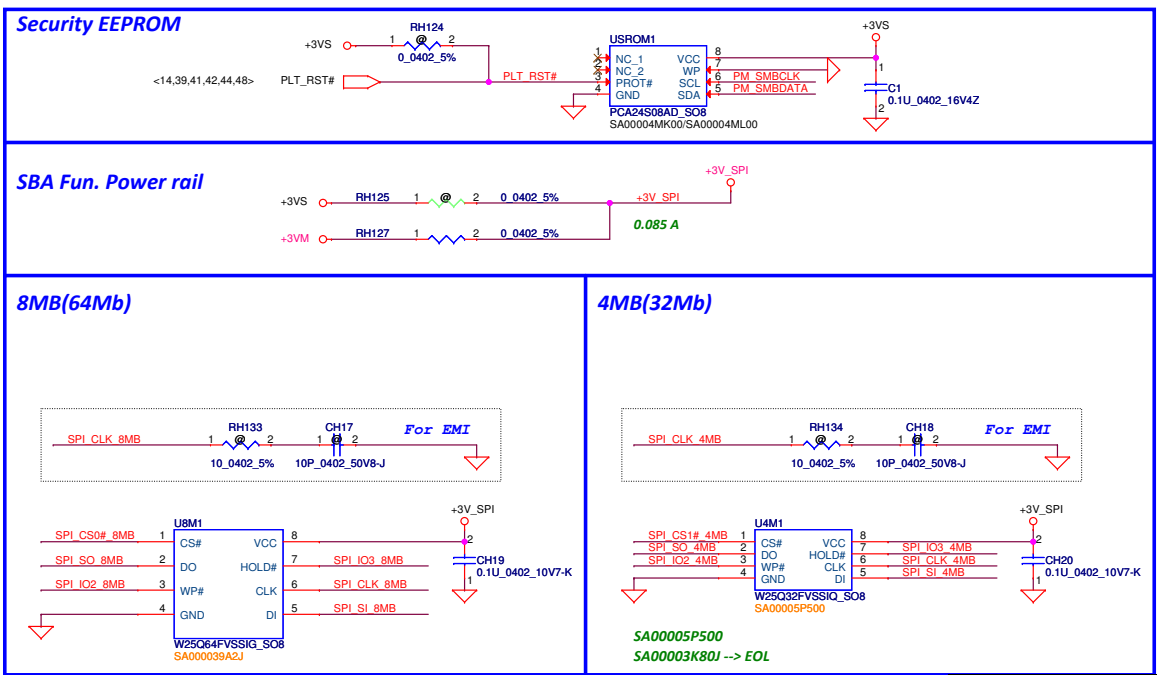


Project Phase ID		
Project Phase	PCH_GPIO64	PCH_GPIO65
SDV, FVT	0	0
SIT2 (R 0.5)	0	1
SIT (R 0.4)	1	0
* SVT	1	1

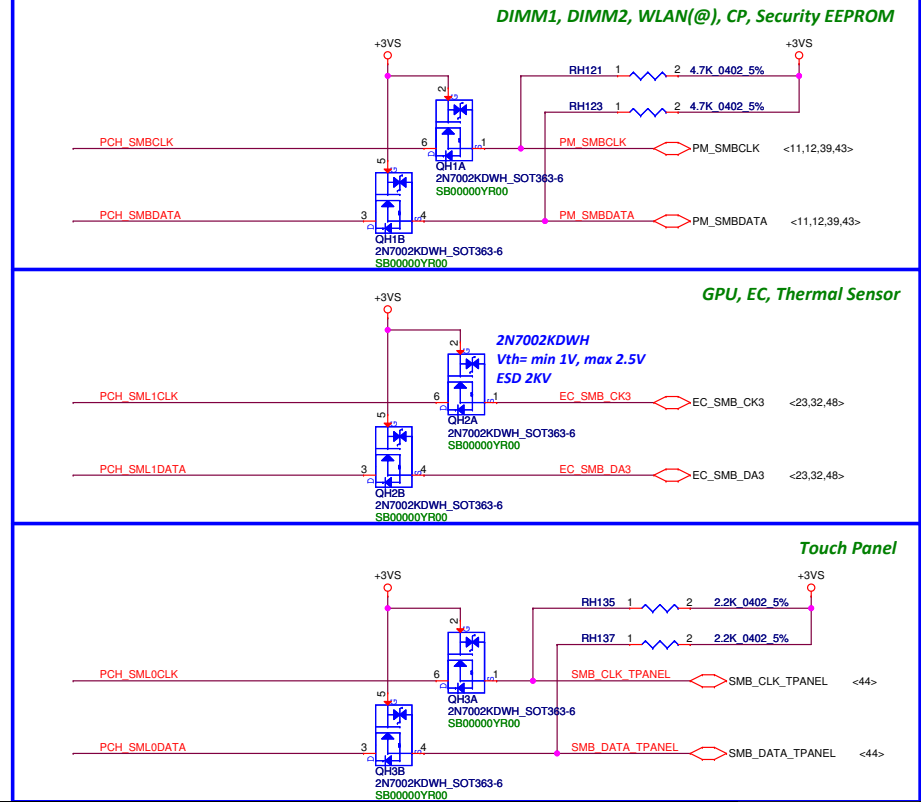




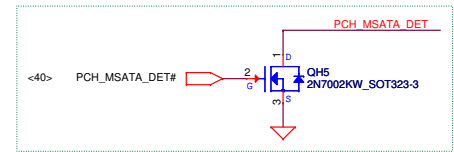
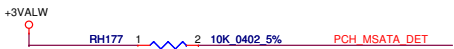
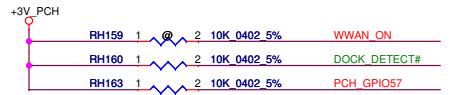
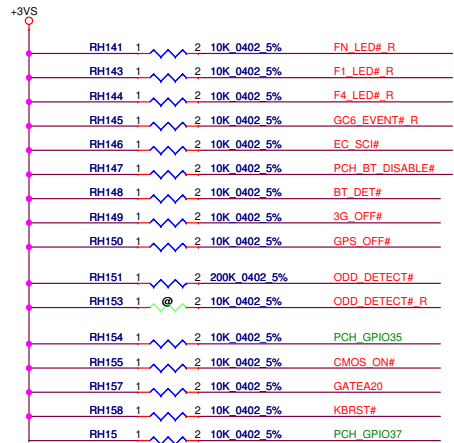
8MB + 4MB SPI ROM, 5MB ME(SBA), Security EEPROM



SM Bus

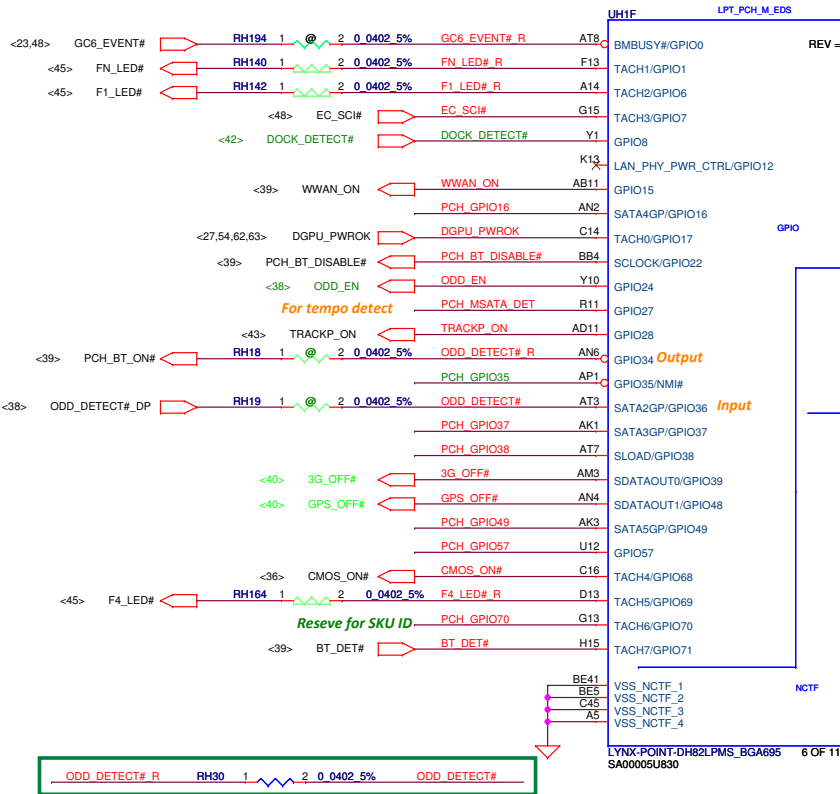
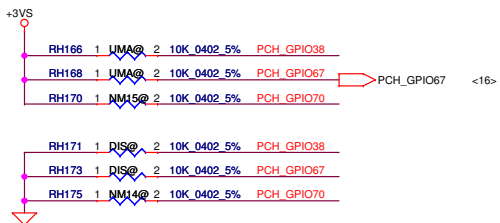


LC Future Center Secret Data				Title	
Security Classification	Issued Date	Deciphered Date	2012/12/05	PCH_LPC/SPI/SM BUS	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR COUNSELLED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size	Document Number
				Custom	E440 NM-A151
				Date:	Thursday, July 11, 2013
				Sheet	17 of 57
				Rev	1.0

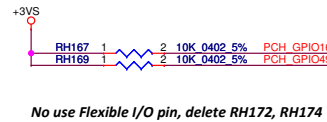


SKU ID

Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70
* Optimus	0	0	
Reserve	0	1	
DIS	1	0	
* UMA	1	1	
* 14"			0
* 15"			1



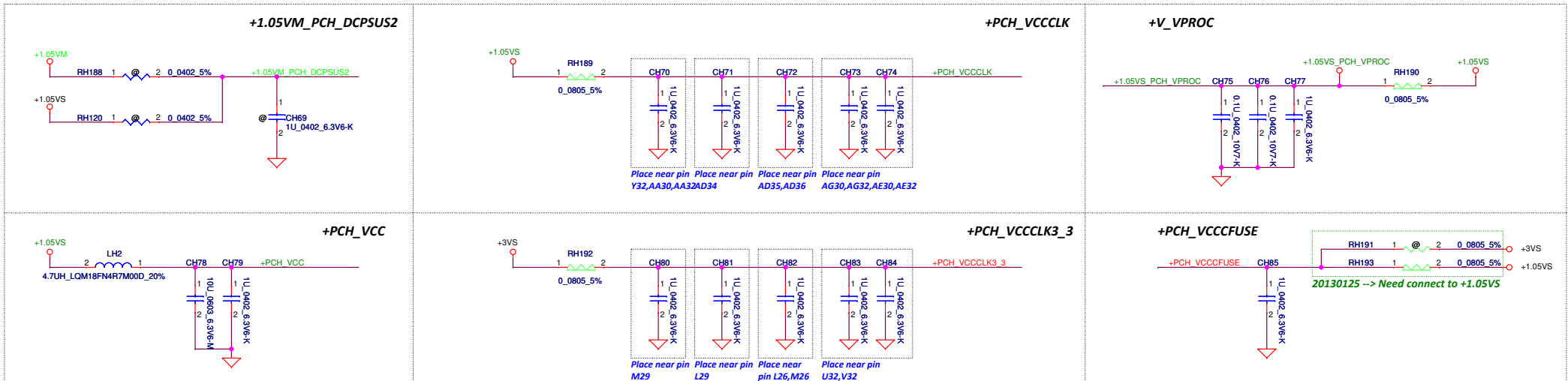
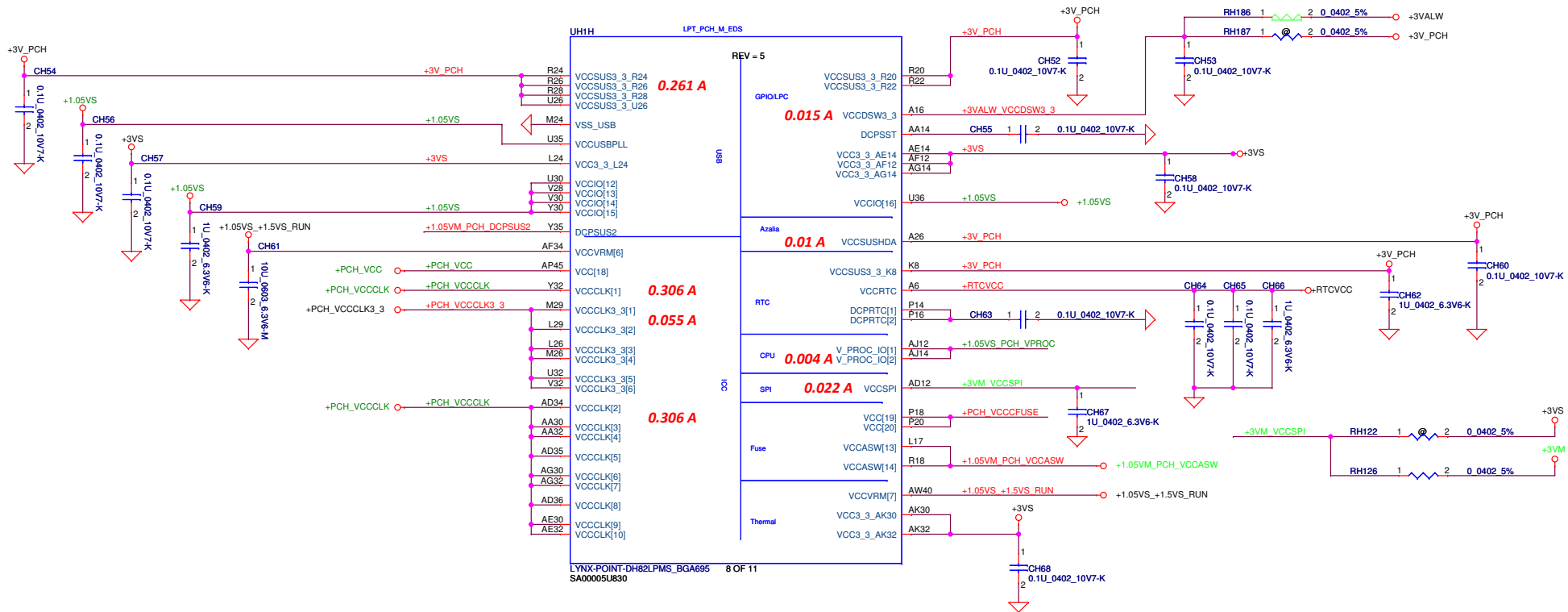
CONFIG	GPIO16, 49
* USB X4,PCIEX8,SATAx6	11
USB X6,PCIEX8,SATAx4	01

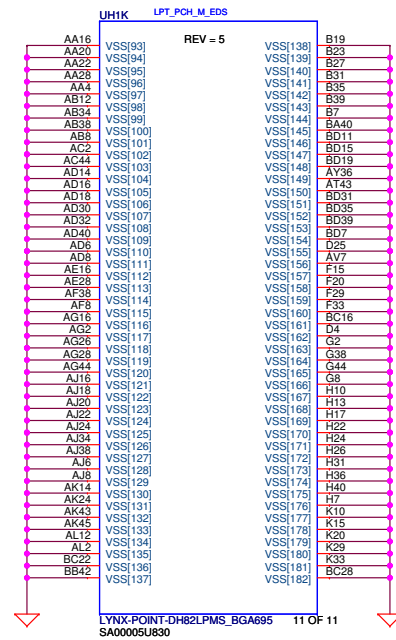
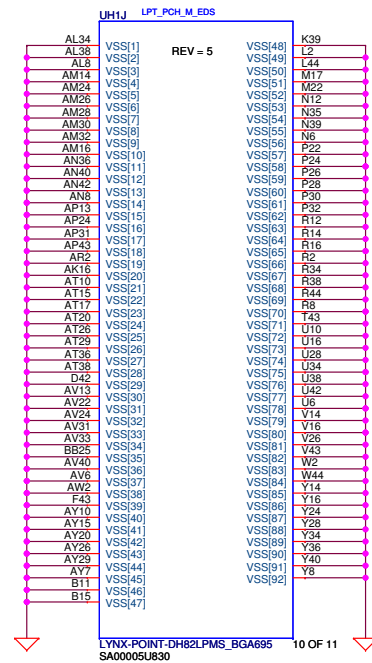



No use Flexible I/O pin, delete RH172, RH174

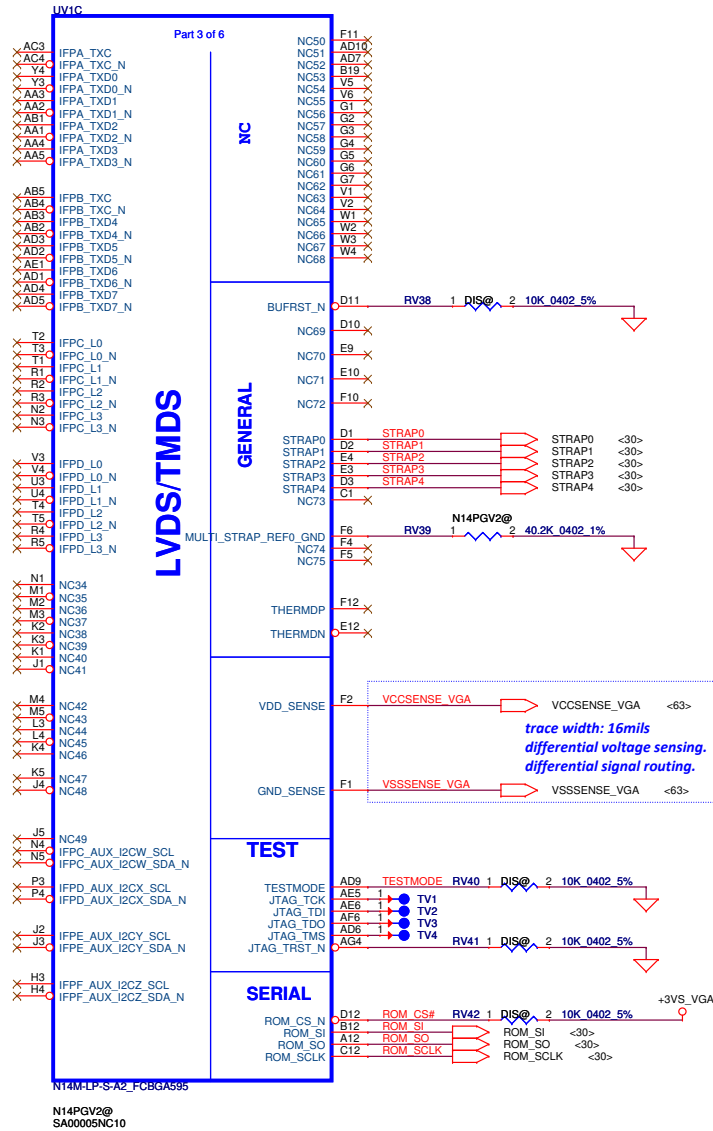
Fixed Signals				Muxed Signals		Fixed Signals								Muxed Signals		Fixed Signals			
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1	PCIE 2	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	PCIE 9	PCIE 10	SATA 4	SATA 5	SATA 0	SATA 1	SATA 2	SATA 3
				(00)	(00)									(00)	(00)				
				USB3 3	USB3 4									PCIE 1	PCIE 2				
				(01)	(01)									(01)	(01)				

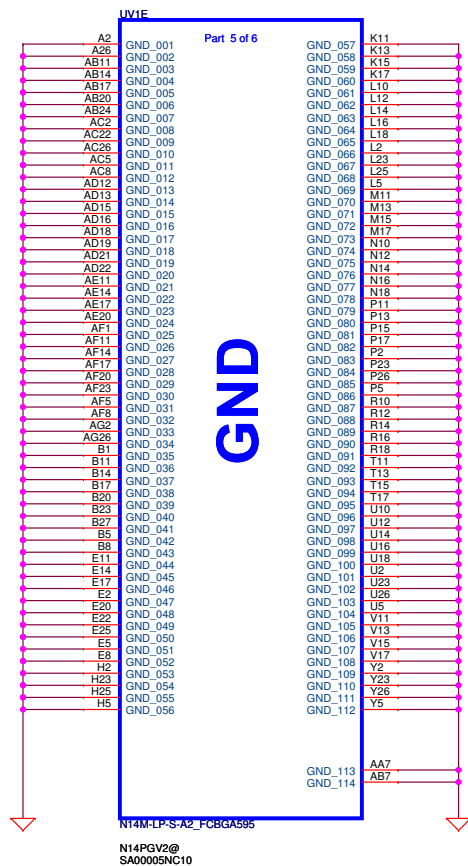
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/12/05	Deciphered Date	2014/12/05	PCH_GPIO/CPU-MISC	
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</p>					
Size	Custom	Document Number	E440 NW-A151		Rev 1.0
Date:	Thursday, July 11, 2013	Sheet	19	of	57





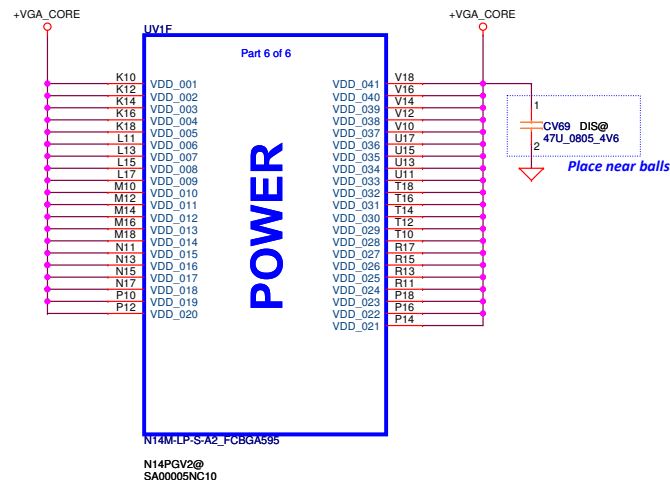
Title			
N14P_PClE/GPIO/I2C			
Size	Document Number	Rev	
Custom	E440 NM-A151	1.0	
Date:	Thursday, July 11, 2013	Sheet	23 of 57





N14M-LP-S-A2_FCBGA595

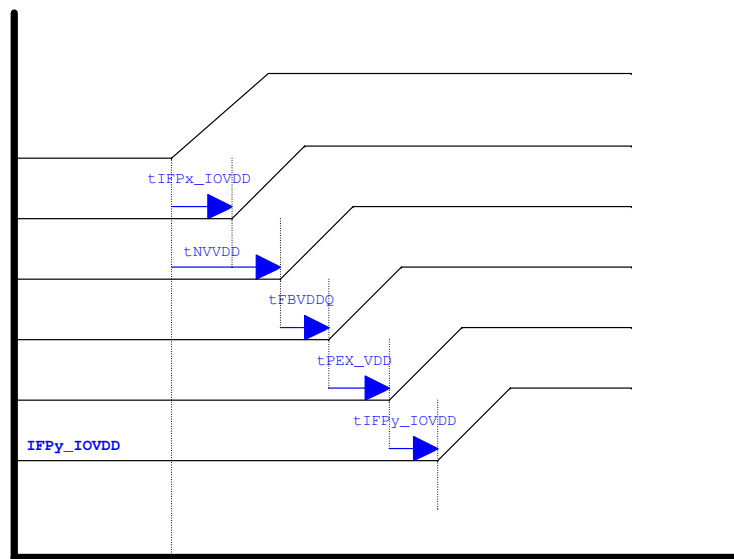
N14PGV2@
SA00005NC10



N14M-LP-S-A2_FCBGA595


N14PGV2@
SA00005NC10

VDD33 (+3VS_VGA)
IFPx_IOVDD
NVVDD (+VGA_CORE)
FBVDDQ (+1.5VS_VGA)
PEX_VDD (+1.05VS_VGA)



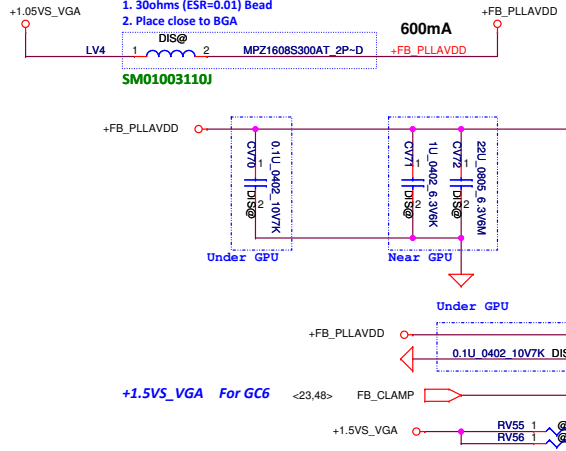
NV Recommended Power On Sequencing Order

X=A and B
Y=C,D,E and F

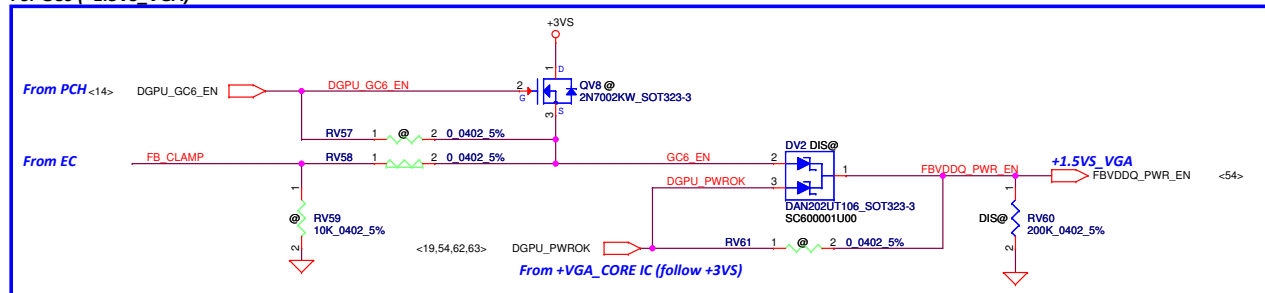
Security Classification	LC Future Center Secret Data		Title		
Issued Date	2012/12/05	Deciphered Date	2014/12/05	N14P_VDD/GND	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					Size Custom Document Number E540 NM-A161 Date: Thursday, July 11, 2013 Sheet 26 of 57 Rev 1.0

<28,29> FBA_D[0..63] FBA_D[0..63]
<28,29> FBA_DQM[7..0] FBA_DQM[7..0]
<28,29> FBA_DQS[7..0] FBA_DQS[7..0]
<28,29> FBA_DQS#[7..0] FBA_DQS#[7..0]

FBA_MA[15..0] FBA_MA[15..0] <28,29>
FBA_BA[2..0] FBA_BA[2..0] <28,29>



For GC6 (+1.5V_VGA)



UV18
Part 2 of 6

FBA_D0 E18 FBA_D00
FBA_D1 F18 FBA_D01
FBA_D2 E16 FBA_D02
FBA_D3 F17 FBA_D03
FBA_D4 D20 FBA_D04
FBA_D5 D21 FBA_D05
FBA_D6 F20 FBA_D06
FBA_D7 E21 FBA_D07
FBA_D8 E16 FBA_D08
FBA_D9 D15 FBA_D09
FBA_D10 F15 FBA_D10
FBA_D11 F13 FBA_D11
FBA_D12 C13 FBA_D12
FBA_D13 B13 FBA_D13
FBA_D14 E13 FBA_D14
FBA_D15 D13 FBA_D15
FBA_D16 B15 FBA_D16
FBA_D17 C16 FBA_D17
FBA_D18 A13 FBA_D18
FBA_D19 A15 FBA_D19
FBA_D20 B18 FBA_D20
FBA_D21 A18 FBA_D21
FBA_D22 A19 FBA_D22
FBA_D23 C19 FBA_D23
FBA_D24 B24 FBA_D24
FBA_D25 A25 FBA_D25
FBA_D26 A24 FBA_D26
FBA_D27 A21 FBA_D27
FBA_D28 B21 FBA_D28
FBA_D29 C20 FBA_D29
FBA_D30 C21 FBA_D30
FBA_D31 R22 FBA_D31
FBA_D32 R24 FBA_D32
FBA_D33 T22 FBA_D33
FBA_D34 R23 FBA_D34
FBA_D35 N25 FBA_D35
FBA_D36 N26 FBA_D36
FBA_D37 N23 FBA_D37
FBA_D38 N24 FBA_D38
FBA_D39 V23 FBA_D39
FBA_D40 V22 FBA_D40
FBA_D41 T23 FBA_D41
FBA_D42 U22 FBA_D42
FBA_D43 Y24 FBA_D43
FBA_D44 AA24 FBA_D44
FBA_D45 V22 FBA_D45
FBA_D46 AA23 FBA_D46
FBA_D47 AB27 FBA_D47
FBA_D48 AB25 FBA_D48
FBA_D49 AD26 FBA_D49
FBA_D50 AD25 FBA_D50
FBA_D51 AC25 FBA_D51
FBA_D52 AA27 FBA_D52
FBA_D53 AA26 FBA_D53
FBA_D54 V26 FBA_D54
FBA_D55 Y25 FBA_D55
FBA_D56 R26 FBA_D56
FBA_D57 T25 FBA_D57
FBA_D58 N27 FBA_D58
FBA_D59 R27 FBA_D59
FBA_D60 V26 FBA_D60
FBA_D61 V27 FBA_D61
FBA_D62 W27 FBA_D62
FBA_D63 W25 FBA_D63

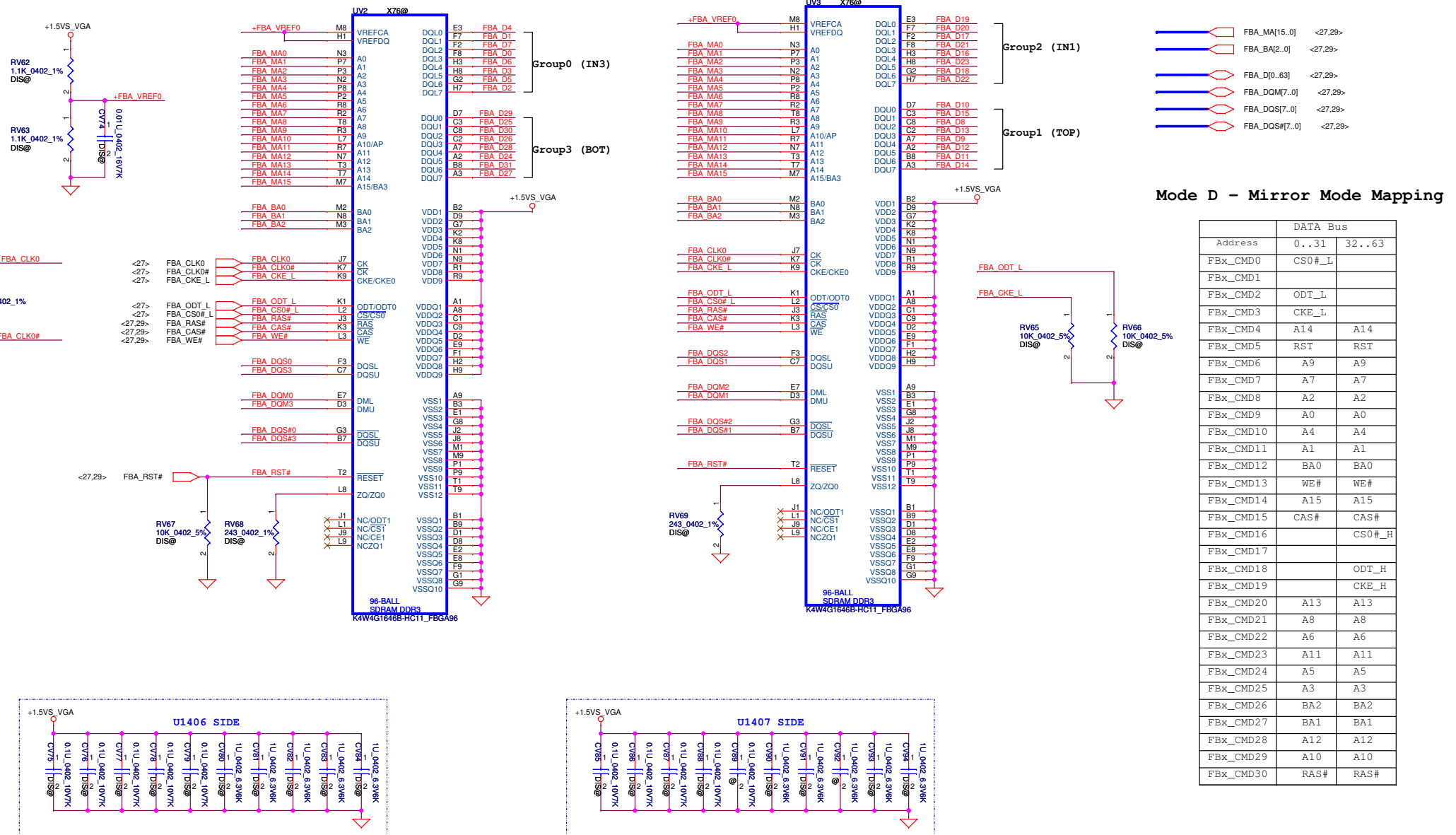
MEMORY
INTERFACE A

FBA_CMD0 C27 FBA_CS0#_L <28>
FBA_CMD1 C26 FBA_ODT_L <28>
FBA_CMD2 E24 FBA_CKE_L <28>
FBA_CMD3 F24 FBA_RST# <28,29>
FBA_CMD4 D27 FBA_MA14
FBA_CMD5 D26 FBA_MA9
FBA_CMD6 F25 FBA_MA7
FBA_CMD7 F26 FBA_MA5
FBA_CMD8 F23 FBA_MA2
FBA_CMD9 G22 FBA_MA0
FBA_CMD10 G23 FBA_MA4
FBA_CMD11 G24 FBA_MA1
FBA_CMD12 F27 FBA_BA0
FBA_CMD13 G25 FBA_WE# <28,29>
FBA_CMD14 G27 FBA_MA15
FBA_CMD15 G26 FBA_CAS# <28,29>
FBA_CMD16 M24 FBA_CS0#_H <29>
FBA_CMD17 M23 FBA_ODT_H <29>
FBA_CMD18 K23 FBA_CKE_H <29>
FBA_CMD19 M27 FBA_MA13
FBA_CMD20 M26 FBA_MA8
FBA_CMD21 M25 FBA_MA6
FBA_CMD22 K26 FBA_MA11
FBA_CMD23 K22 FBA_MA5
FBA_CMD24 J23 FBA_MA3
FBA_CMD25 J25 FBA_BA2
FBA_CMD26 J24 FBA_BA1
FBA_CMD27 K27 FBA_MA12
FBA_CMD28 K25 FBA_MA10
FBA_CMD29 J27 FBA_RAS# <28,29>
FBA_CMD30 J26
FBA_CMD31
FBA_DOM0 D19 FBA_DOM0
FBA_DOM1 D14 FBA_DOM1
FBA_DOM2 C17 FBA_DOM2
FBA_DOM3 C22 FBA_DOM3
FBA_DOM4 P24 FBA_DOM4
FBA_DOM5 W24 FBA_DOM5
FBA_DOM6 AA25 FBA_DOM6
FBA_DOM7 U25 FBA_DOM7
FBA_DQS_RN0 F19 FBA_DQS#0
FBA_DQS_RN1 C14 FBA_DQS#1
FBA_DQS_RN2 A16 FBA_DQS#2
FBA_DQS_RN3 A22 FBA_DQS#3
FBA_DQS_RN4 P25 FBA_DQS#4
FBA_DQS_RN5 W22 FBA_DQS#5
FBA_DQS_RN6 AB27 FBA_DQS#6
FBA_DQS_RN7 C127 FBA_DQS#7
FBA_CLK0 D24 FBA_CLK0 <28>
FBA_CLK1 N22 FBA_CLK1 <28>
FBA_CLK2 M22 FBA_CLK1# <29>
FBA_CLK3
FBA_WCK0 D18
FBA_WCK1 C18
FBA_WCK2 D17
FBA_WCK3 D16
FBA_WCK4 T24
FBA_WCK5 U24
FBA_WCK6 V24
FBA_WCK7 V25

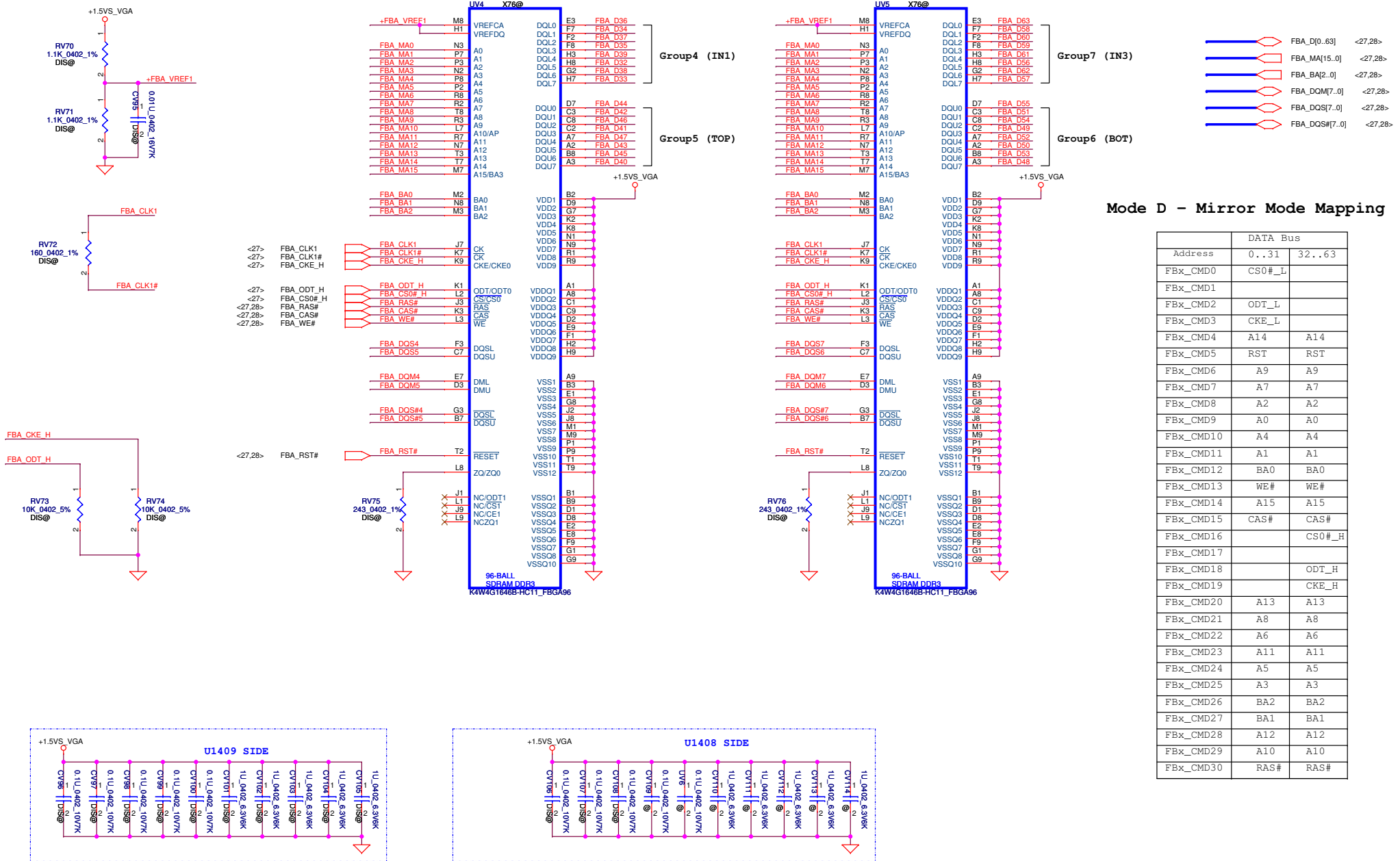
Mode D - Mirror Mode Mapping

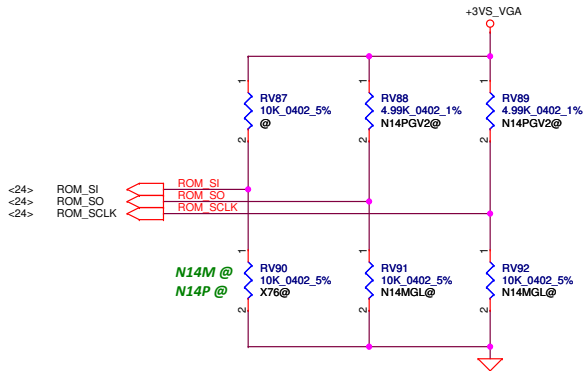
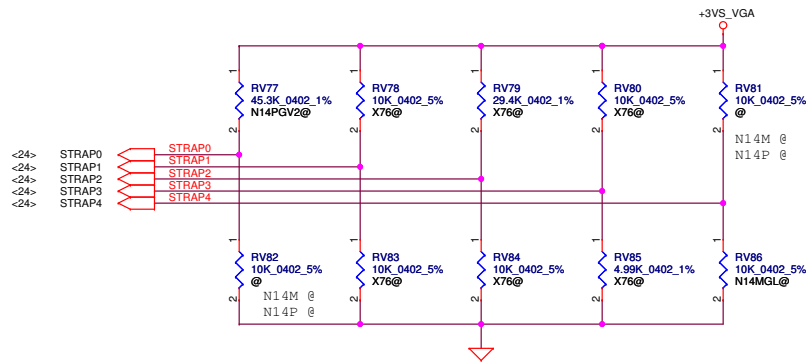
Address	DATA Bus
FBx_CMD0	0..31 CS0#_L
FBx_CMD1	ODT_L
FBx_CMD3	CKE_L
FBx_CMD4	A14 A14
FBx_CMD5	RST RST
FBx_CMD6	A9 A9
FBx_CMD7	A7 A7
FBx_CMD8	A2 A2
FBx_CMD9	A0 A0
FBx_CMD10	A4 A4
FBx_CMD11	A1 A1
FBx_CMD12	BA0 BA0
FBx_CMD13	WE# WE#
FBx_CMD14	A15 A15
FBx_CMD15	CAS# CAS#
FBx_CMD16	CS0#_H
FBx_CMD17	ODT_H
FBx_CMD18	CKE_H
FBx_CMD20	A13 A13
FBx_CMD21	A8 A8
FBx_CMD22	A6 A6
FBx_CMD23	A11 A11
FBx_CMD24	A5 A5
FBx_CMD25	A3 A3
FBx_CMD26	BA2 BA2
FBx_CMD27	BA1 BA1
FBx_CMD28	A12 A12
FBx_CMD29	A10 A10
FBx_CMD30	RAS# RAS#

Memory Partition A - Lower 32 bits

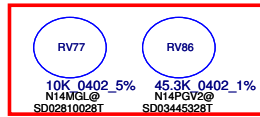


Memory Partition A - Upper 32 bits

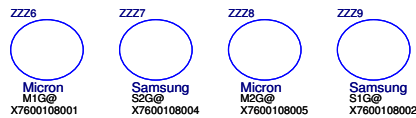




For N14P-GV2 QS Sample
ROM_SO change from PU 10K to PU 5K
ROM_SCLK change from PD 15K to PU 5K
STRAP1 change from PD 5K to PD 45K
STRAP2 change from PU 30K to PD 15K
STRAP4 change from PD 5K to PD 45K



Load BOM時，要改成RV86，RV77



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG[3:0]	
0110	Gen1/Gen2 support only
0000	Gen3 support

FB[1:0]	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

PCIE_MAX_SPEED	
0	Limit booting to PCIe Gen1
1	Allow booting to PCIe Gen 2/3

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

USER Straps	
User [3:0]	
1000-1100	Customer defined

PCIE_SPEED_CHANGE_GEN3	
0	Disable PCIe Gen3 operation
1	Enable PCIe Gen3 operation

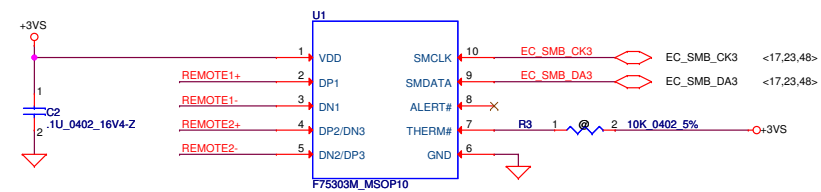
DP_PLL_VDD33V	
0	Reserved
1	Default

					X76 RV90	RV77	PU, RV78 PD, RV83	PU, RV79 PD, RV84	PU, RV80 PD, RV85	PD, RV86	
	GPU	FB Memory GDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
S2G, X76~04 SA00005OM00	N14P-GV2	Samsung 1000MHz	K4W2G1646E-BC1A	PU 5K	PD 45K	PU 45.3K	PD 45.3K	PD 15K	PD 5K	PD 45.3K	
			128Mx16								
		Micron 1000MHz	MT41J128M16JT-093G		PD 30K						
			128Mx16								
		*Samsung 900MHz	K4W4G1646B-HC11		PD 20K						
			256Mx16								
		*Micron 900MHz	MT41K256M16HA-107G		PD 10K						
			256Mx16								
M2G, X76~05 SA00005ON00											

						RV77	PU, RV78 PD, RV83	PU, RV79 PD, RV84	PU, RV80 PD, RV85	PD, RV86
GPU	FB Memory GDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
S1G, X76~02 SA00005SH20	N14M-GL	*Samsung 1000MHz	K4W2G1646E-BC1A	PD 10K		PU 10K	PD 10K	PU 10K	PD 10K	PD 10K
		128Mx16								
Hynix 1000MHz		H5TQ2G63DFR-N0C	PD 10K			PU 10K	PU 10K	PD 10K		
128Mx16										
*Micron 1000MHz		MT41J128M16JT-093G	PU 10K			PD 10K	PD 10K	PD 10K		
128Mx16										
Samsung 900MHz		K4W4G1646B-HC11	PU 10K			PU 10K	PU 10K	PU 10K		
256Mx16										
Hynix 900MHz		H5TQ4G63MFR-11C	PU 10K			PU 10K	PD 10K	PD 10K		
256Mx16										
M1G, X76~01 SA00005M110		Micron 900MHz	MT41K256M16HA-107G			PD 10K	PD 10K	PU 10K	PU 10K	
256Mx16										

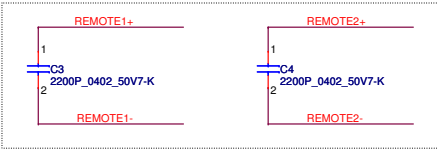
Thermal Sensor

Thermal Sensor
placed near by VRAM

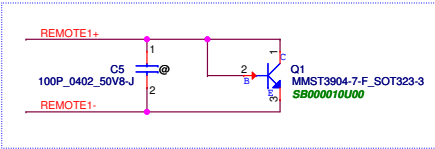


Address 1001_101xb
Internal pull up 1.2K to 1.5V
R for initial thermal shutdown temp

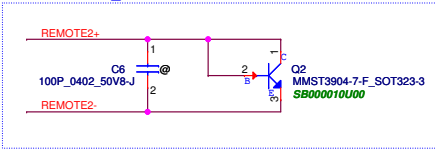
Close to U2



Close to BOTTOM DDR3

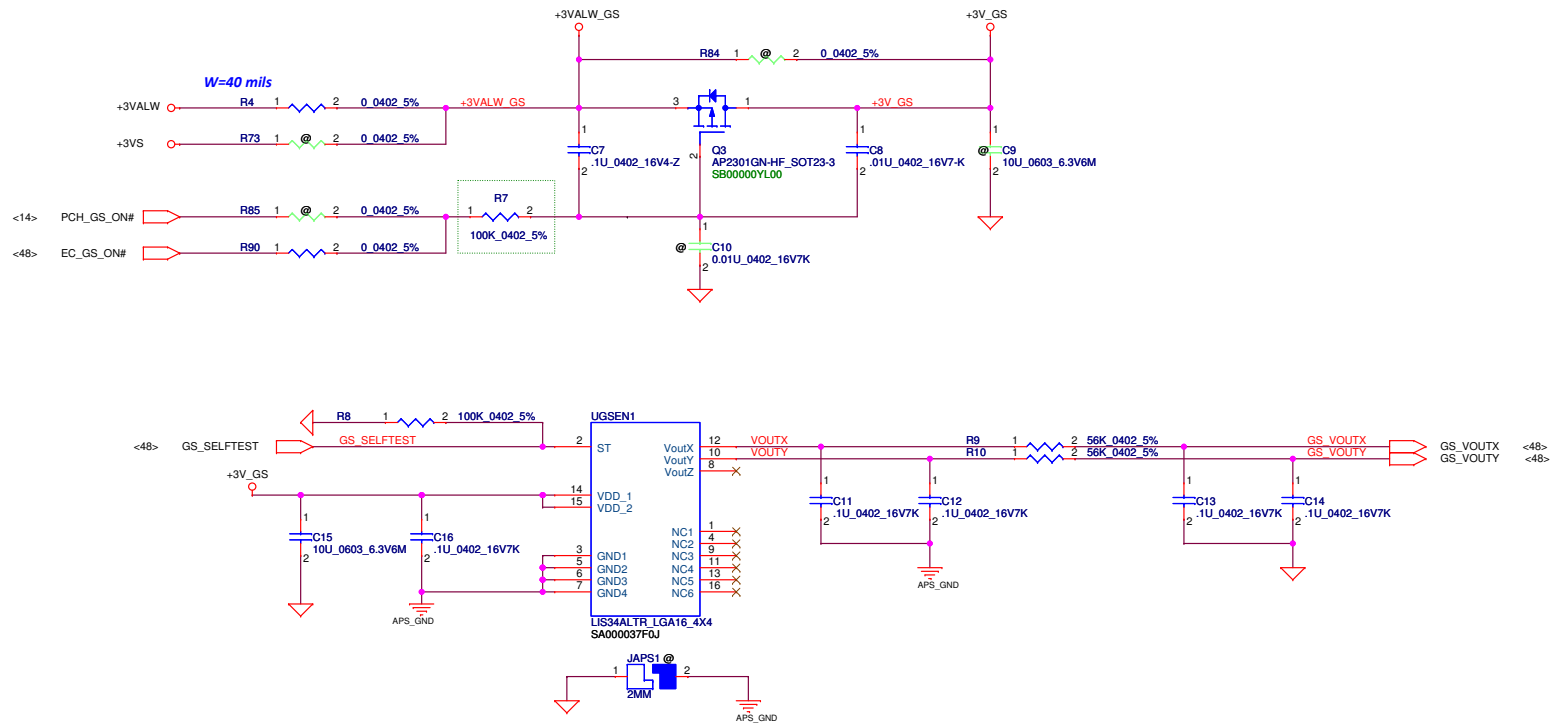


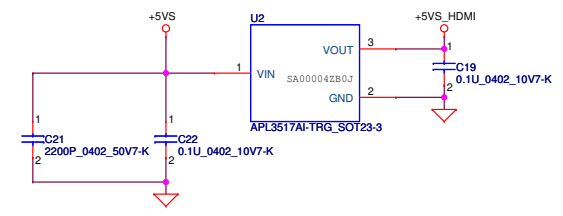
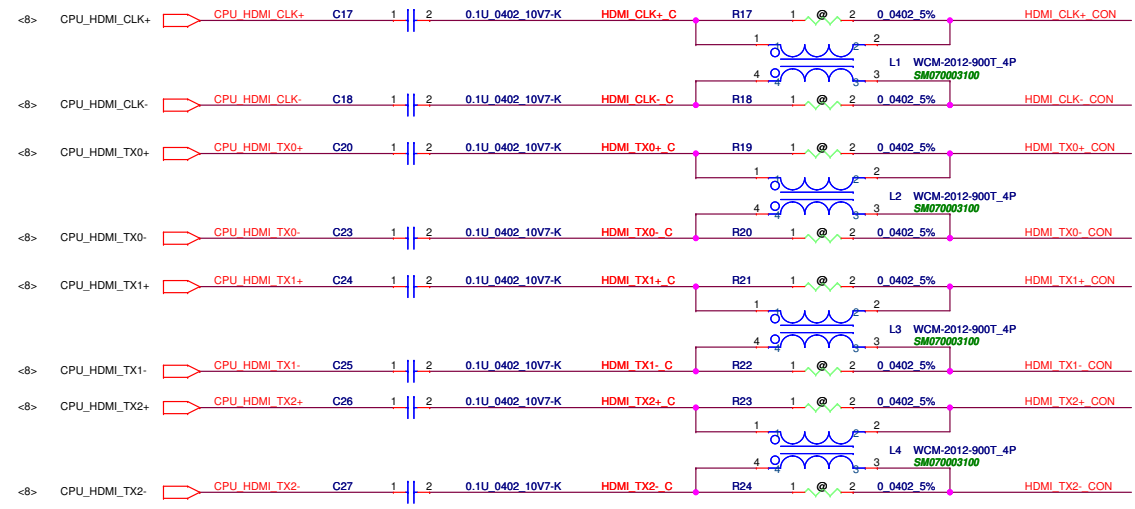
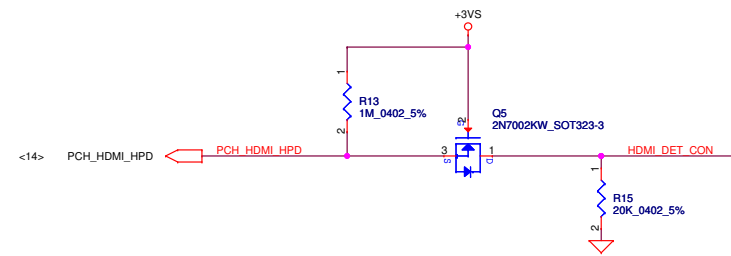
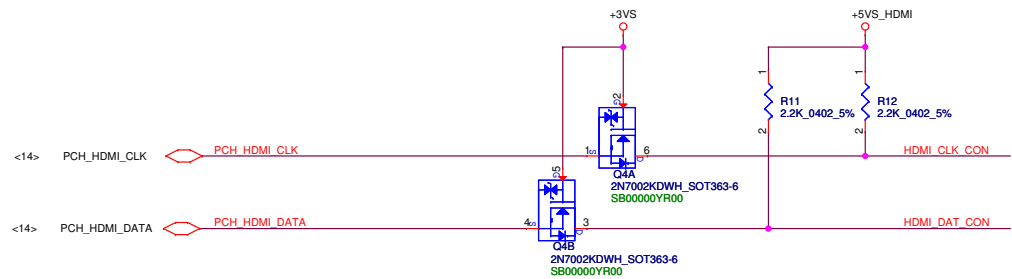
Close to +CPU_CORE



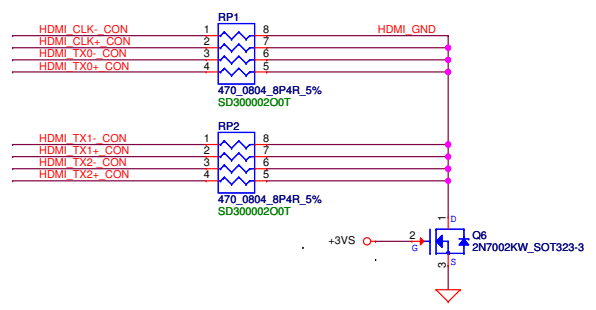
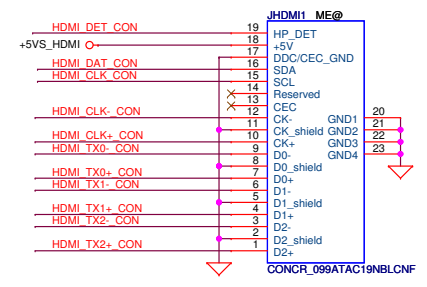
REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

APS G-Sensor

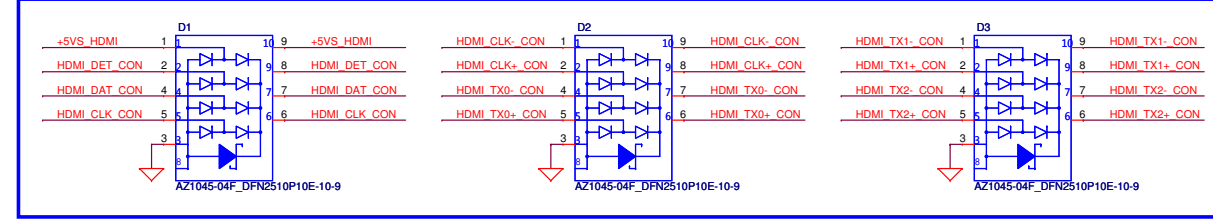


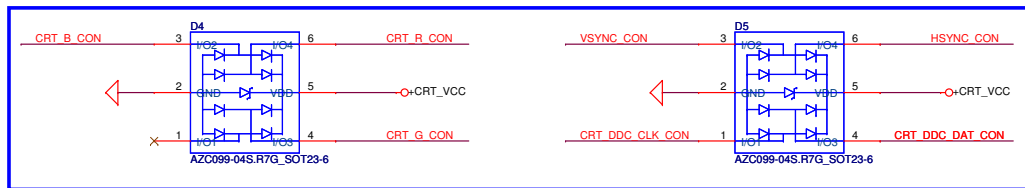


HDMI CONN.

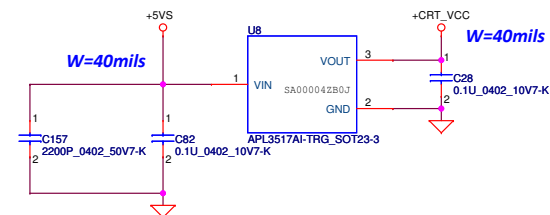


For ESD



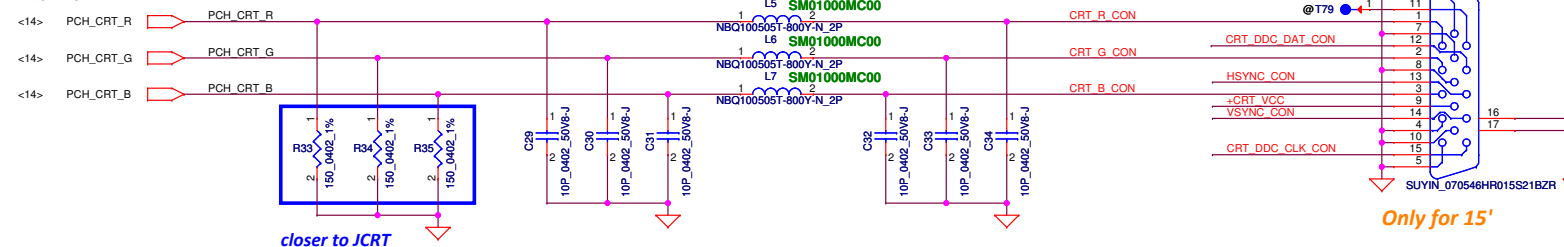


closer to JCRT

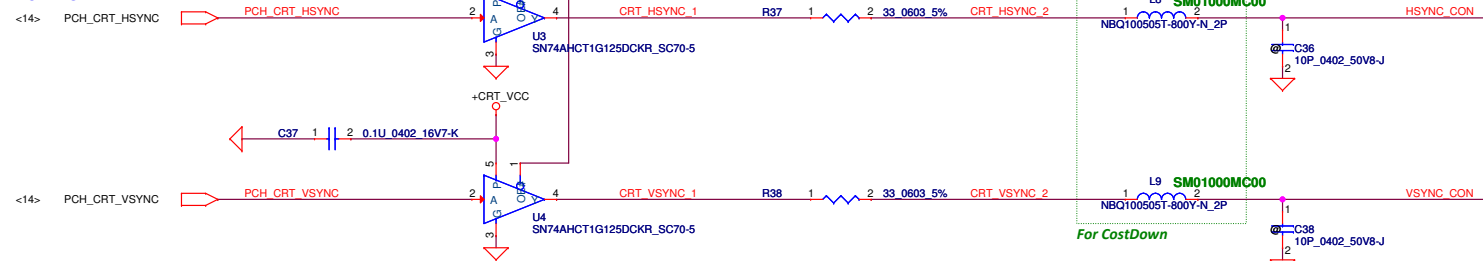


CRT Connector

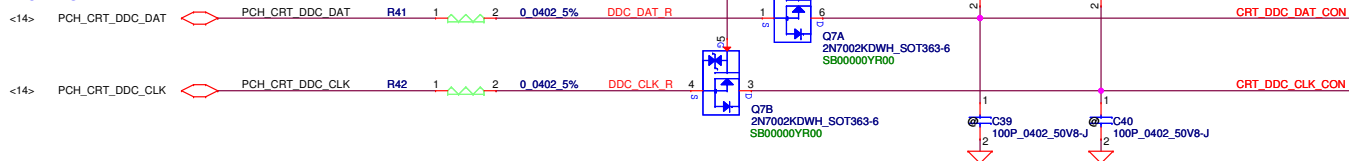
From PCH



From PCH



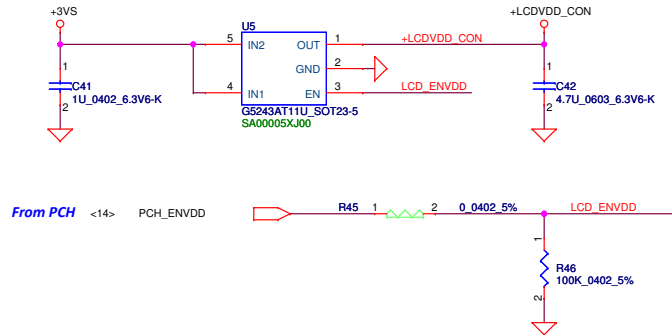
From PCH



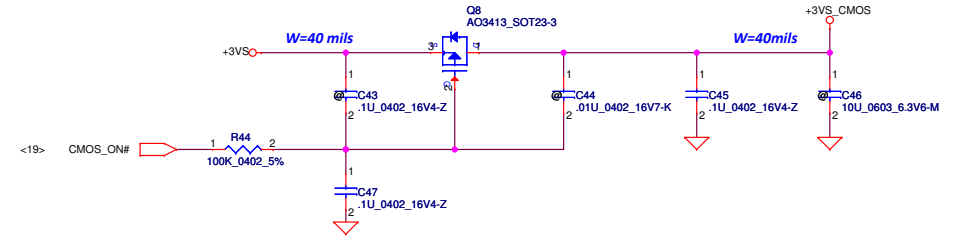
Security Classification	LC Future Center Secret Data	
Issued Date	2012/12/05	Deciphered Date
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.		

Title	Size	Document Number	Rev
CRT CONN.	Custom	E540 NM-A161	1.0
Date:	Thursday, July 11, 2013	Sheet	35 of 57

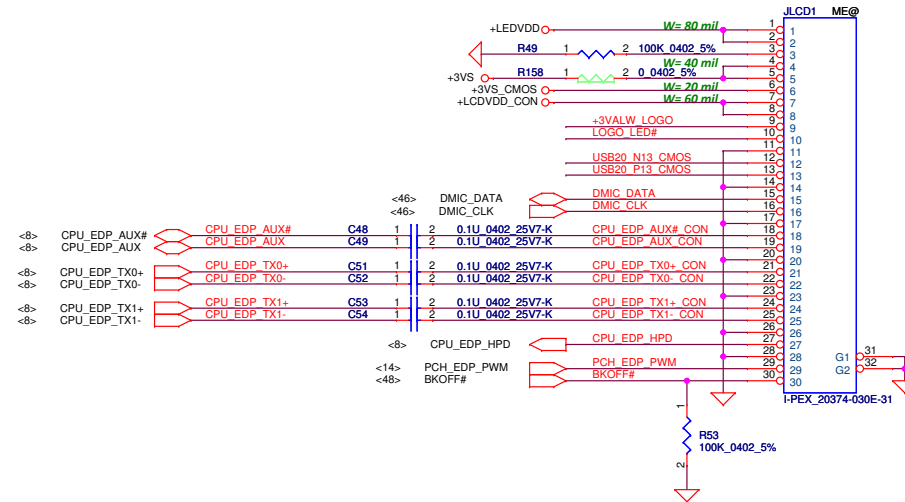
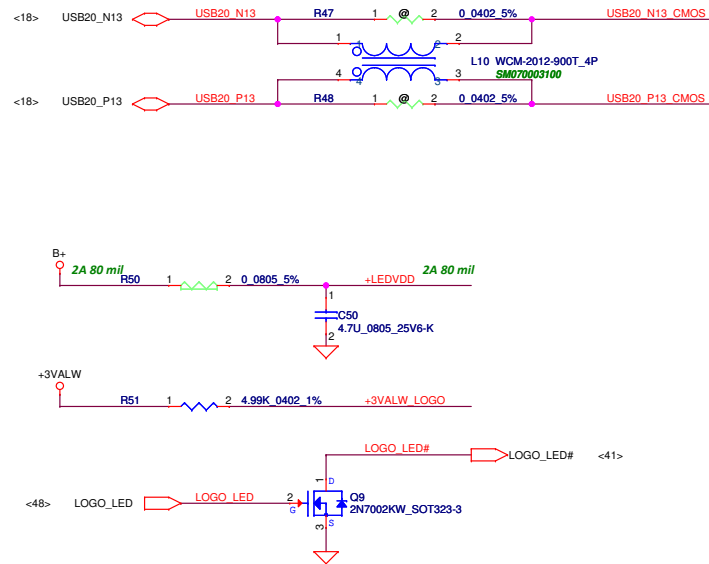
LCDVDD Circuit



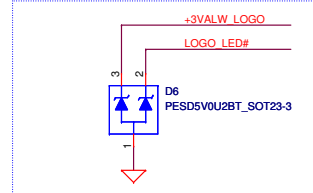
CMOS Camera



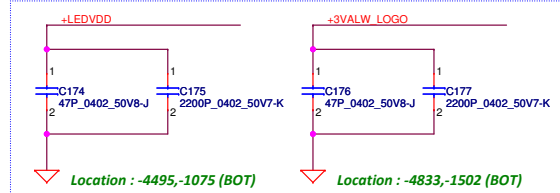
CMOS USB Port10



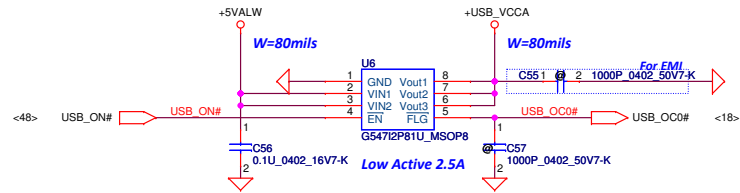
ESD request



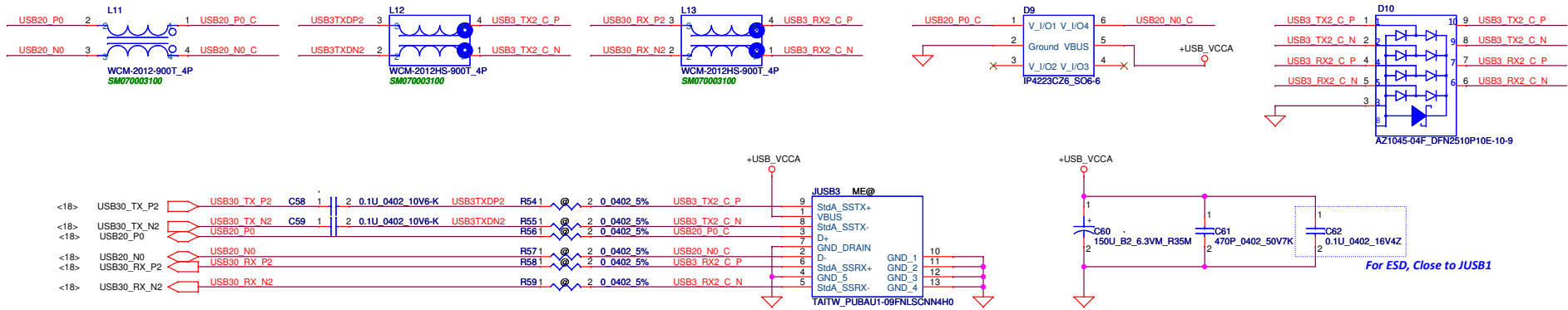
EMI



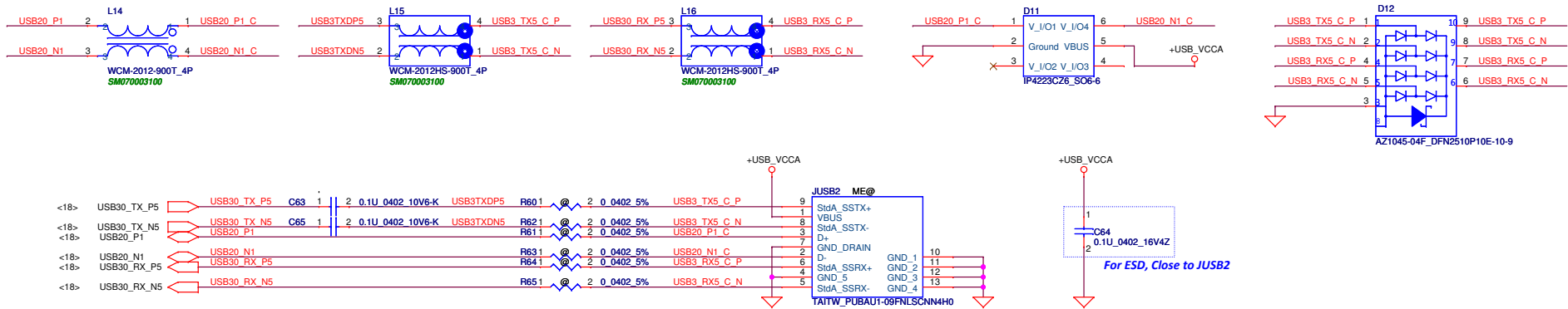
Security Classification	LC Future Center Secret Data		Title	
Issued Date	2012/12/05	Deciphered Date	2014/12/05	LCD/CMOS CONN.
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Rev 1.0
Date: Thursday, July 11, 2013		Sheet 36 of 57		E440 NM-A151




USB30 Front

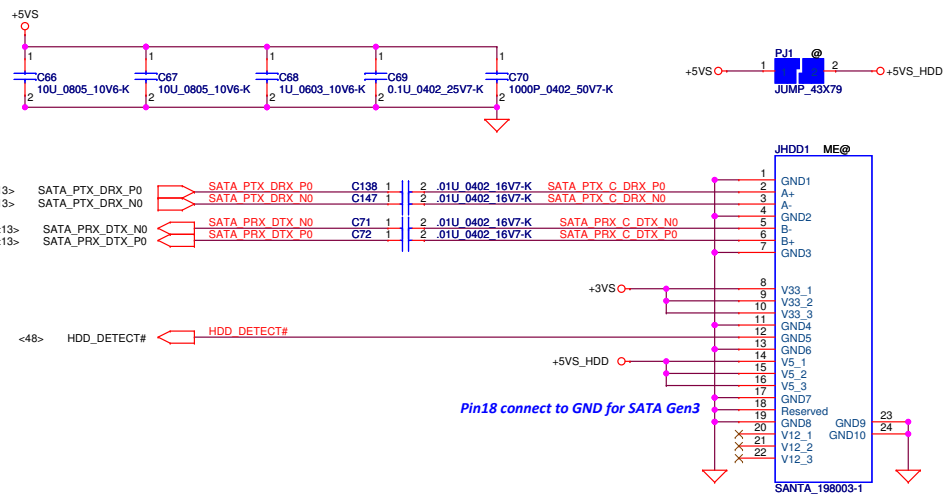


USB30 Back



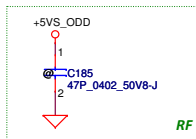
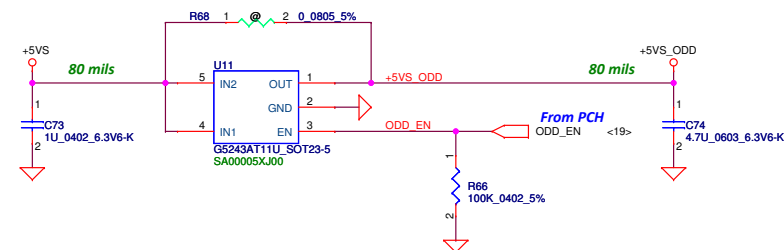
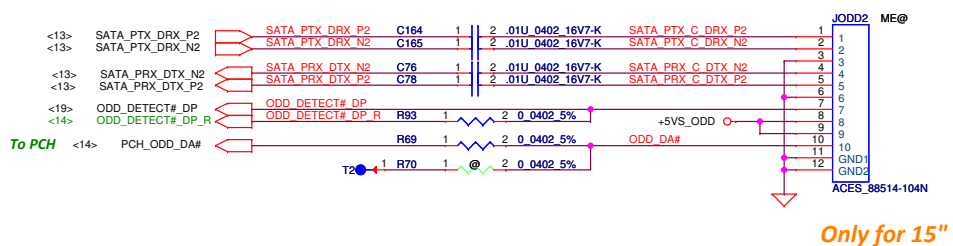
Security Classification		LC Future Center Secret Data				Title			
Issued Date		2012/12/05		Deciphered Date		2014/12/05			
						USB30 PORT CONN.			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.									
Size		Document Number		E440 NM-A151				Rev 1.0	
Date:		Thursday, July 11, 2013		Sheet		37		of 57	

SATA HDD CONN.



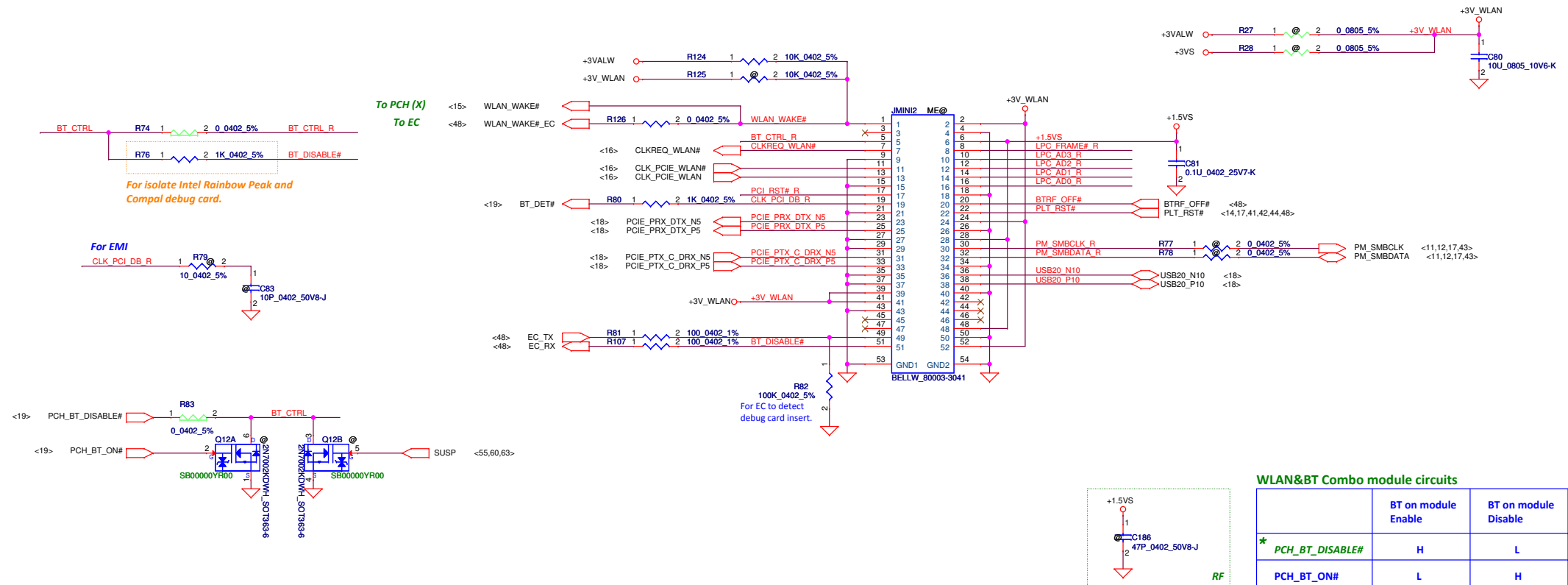
SATA ODD CONN & ODD Power Control

+5VS TO +5VS_ODD



Security Classification				LC Future Center Secret Data		Title		Document Number		Rev	
Issued Date				2012/12/05		Deciphered Date		2014/12/05		1.0	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.						SATA HDD/ODD CONN.		E540 NM-A161		Rev 1.0	
Date:				Thursday, July 11, 2013		Sheet		38 of 57			

Mini-Express Card(WLAN/WiMAX)



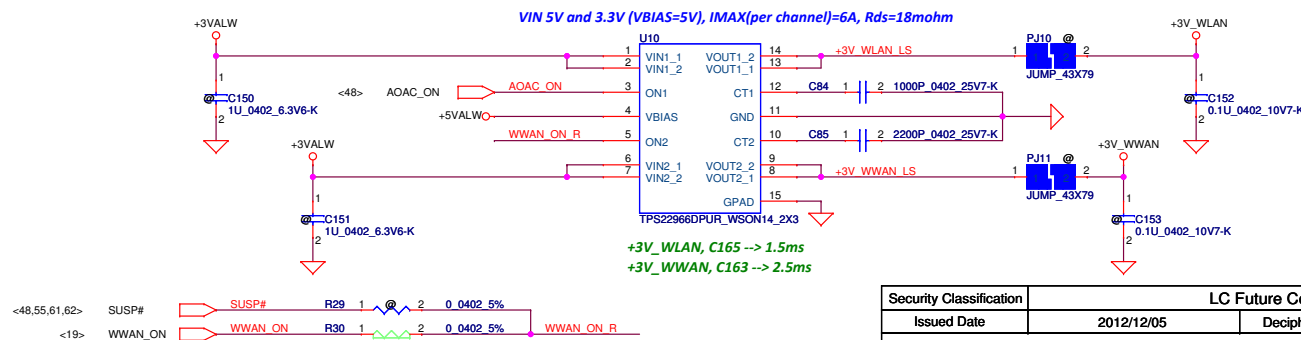
Load Switch

+3VALW To +3V WLAN

1. softstart (RC) will check on EVT PCB
2. if AOAC enable +3V_WLAN always ON
if AOAC disable +3V_WLAN is same as +3VS


+3VALW To +3V_WWAN

if AOAC disable +3V_WLAN is same as +3VS

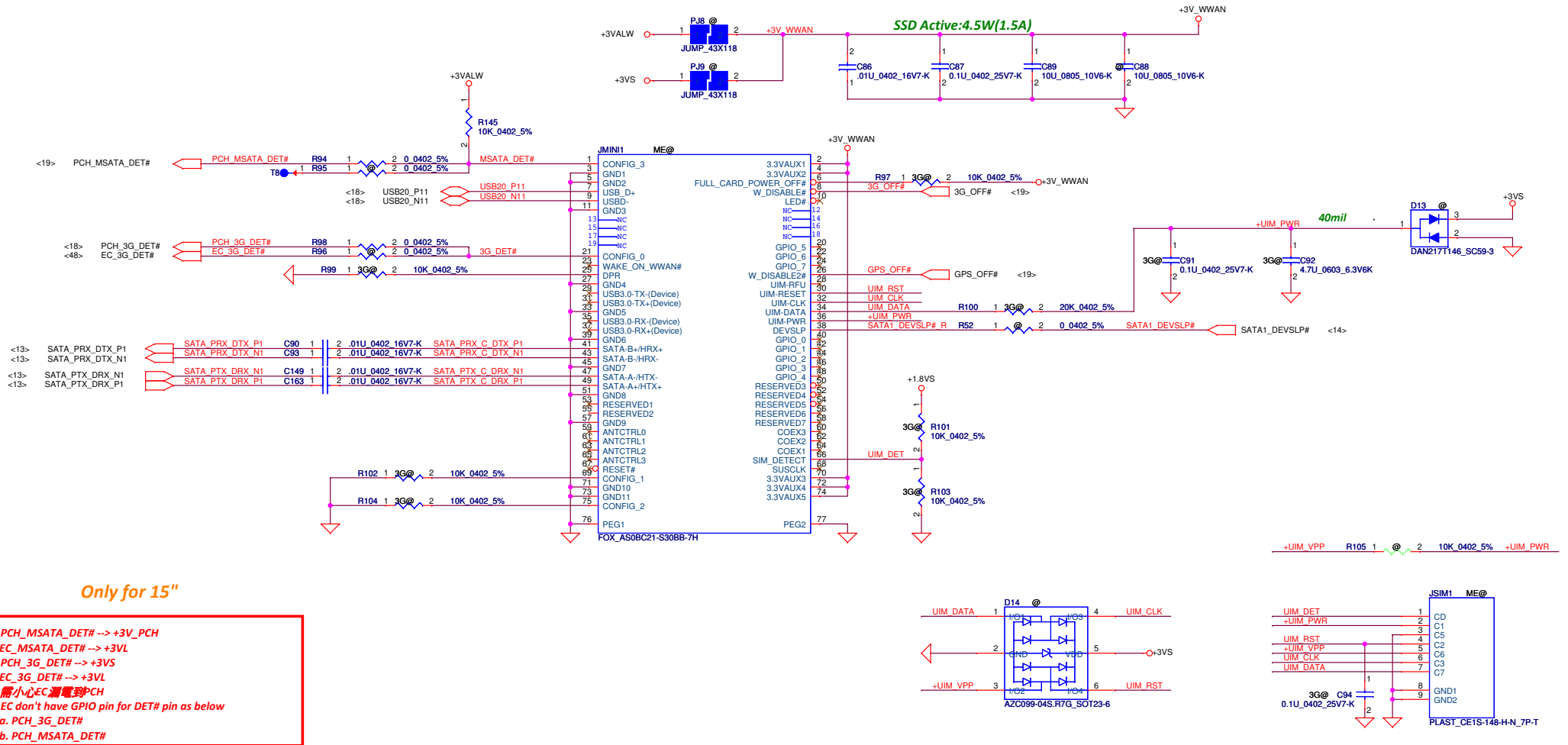


*Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.*

LPC FRAME# R	R86	1	2	0 0402 5%	LPC_FRAME#	LPC_FRAME#	<17,44,48>
LPC AD3 R	R87	1	2	0 0402 5%	LPC AD3	LPC AD3	<17,44,48>
LPC AD2 R	R88	1	2	0 0402 5%	LPC AD2	LPC AD2	<17,44,48>
LPC AD1 R	R89	1	2	0 0402 5%	LPC AD1	LPC AD1	<17,44,48>
PLC RST# R	R91	1	2	0 0402 5%	LPC AD0	LPC AD0	<17,44,48>
PLC RST# R	R92	1	2	0 0402 5%	PLT_RST#	PLC AD0	<17,44,48>
CLK PCI DB R	R106	1	2	0 0402 5%	CLK PCI DB	CLK PCI DB	<16>

Security Classification		LC Future Center Secret Data		Title		
Issued Date	2012/12/05	Deciphered Date	2014/12/05	PCIe-WLAN SLOT		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size Custom	Document Number E440 NM-A151	
				Date:	Thursday, July 11, 2013	Sheet 39 of 57 Rev 1.0

NGFF(SSD) & SIM CARD CONN.

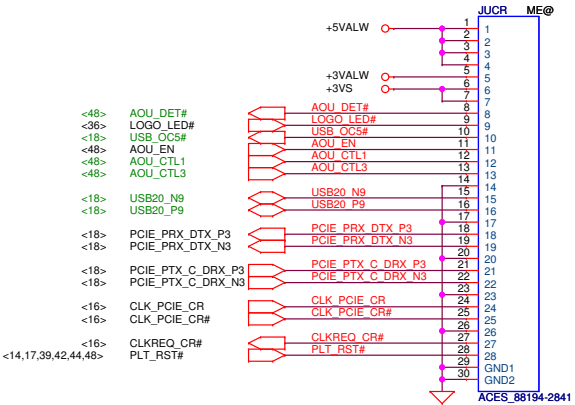


1. PCH_MSATA_DET# --> +3V_PCH
EC_MSATA_DET# --> +3VL
2. PCH_3G_DET# --> +3VS
EC_3G_DET# --> +3VL
需小心EC漏電到PCH
3. EC don't have GPIO pin for DET# pin as below
a. PCH_3G_DET#
b. PCH_MSATA_DET#

NGFF Detect Desc.

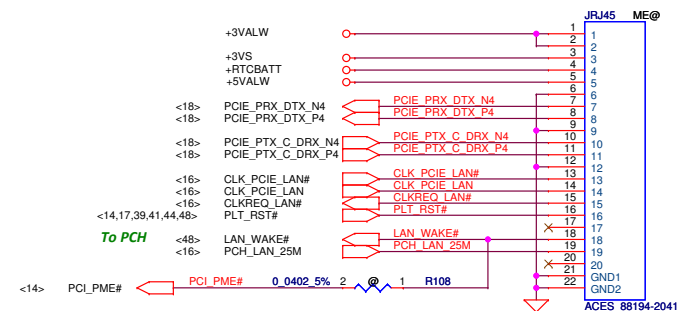
	MSATA_DET#	3G_DET#
No Card	1	1
WWAN CARD	1	0
SSD CARD	0	0

USB2.0, CR & LOGO Board

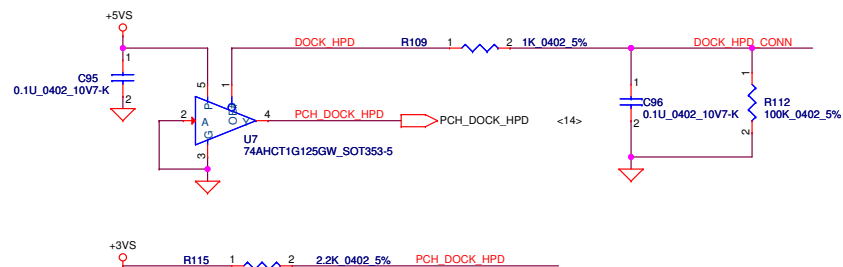
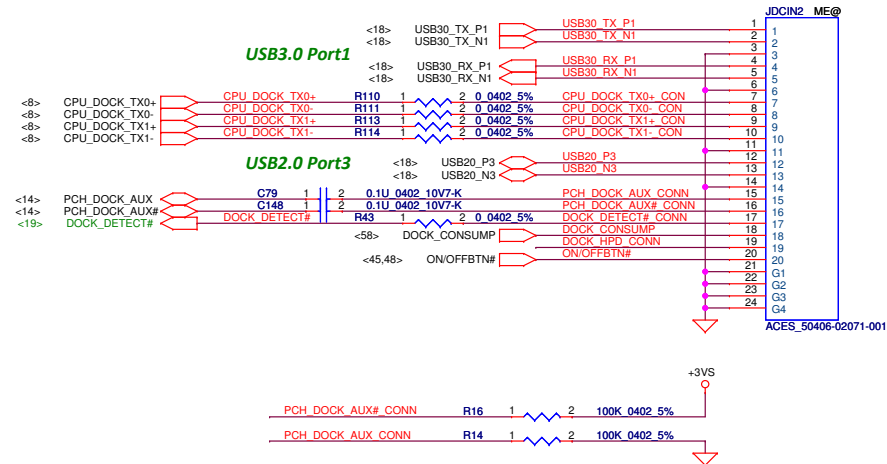


LAN (Port4)
USB3.0/2.0 (Port1/3)
DP(DDIC)

LAN CONN. (FFC)

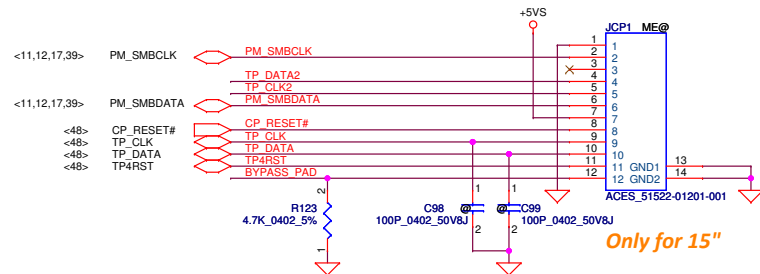


DCIN CONN. (Coaxial)

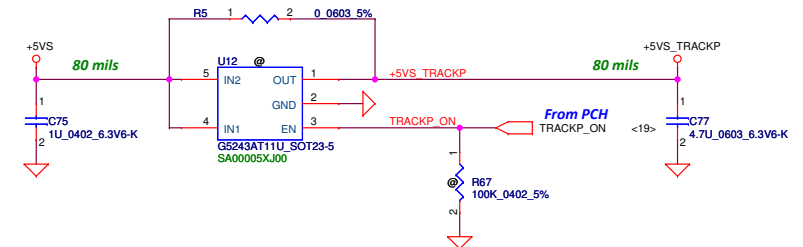
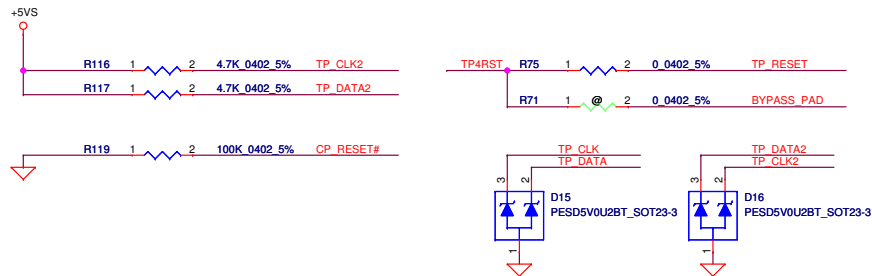
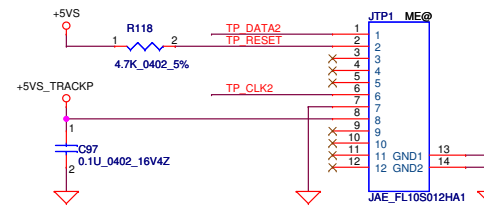


Security Classification	LC Future Center Secret Data		Title	PCle-RJ45/RTC/Docking CON	
Issued Date	2012/12/05	Deciphered Date	2014/12/05	Size	Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FUTURE CENTER DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.			Custom	E440 NM-A151	
Date:	Thursday, July 11, 2013	Sheet	42	of	57

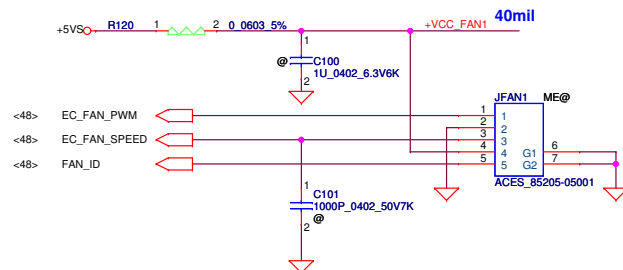
Click Pad



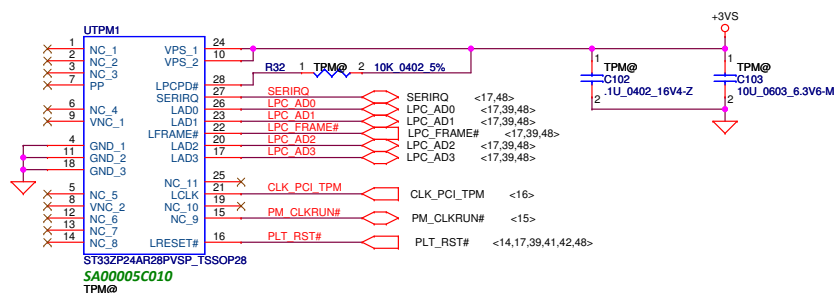
Track point



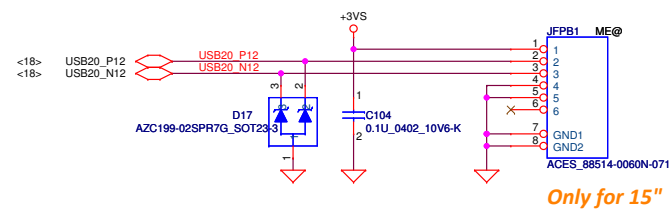
FAN CONN.



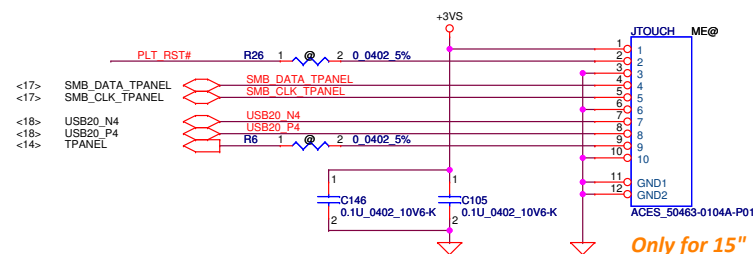
TPM IC




FingerPrint CONN.



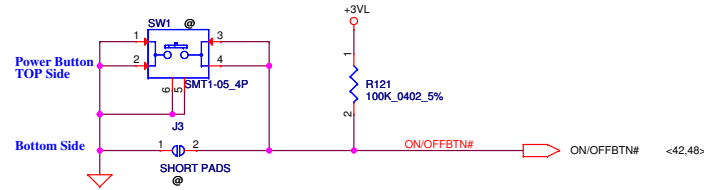
Touch Panel CONN.



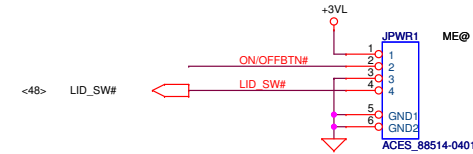
Security Classification		LC Future Center Secret Data		Title		
Issued Date	2012/12/05	Deciphered Date	2014/12/05	TPM/TPanel/FP CONN.		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL, AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size Custom	Document Number E540 NM-A161	
				Date:	Thursday, July 11, 2013	Sheet 44 of 57 Rev 1.0

PWR BTN/LID SW CONN.

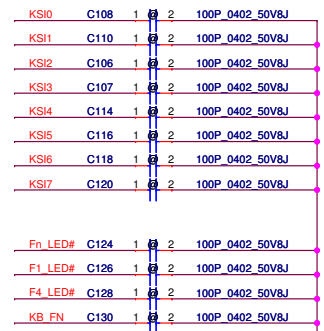
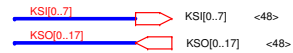
ON/OFF switch



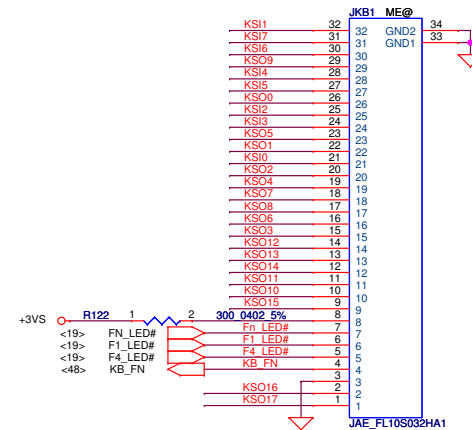
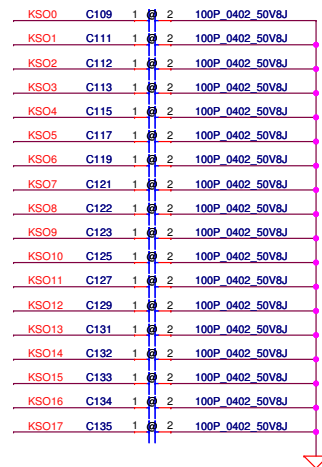
1. Power Button/B link to Function/B Conn. 10pin
2. Lid Switch

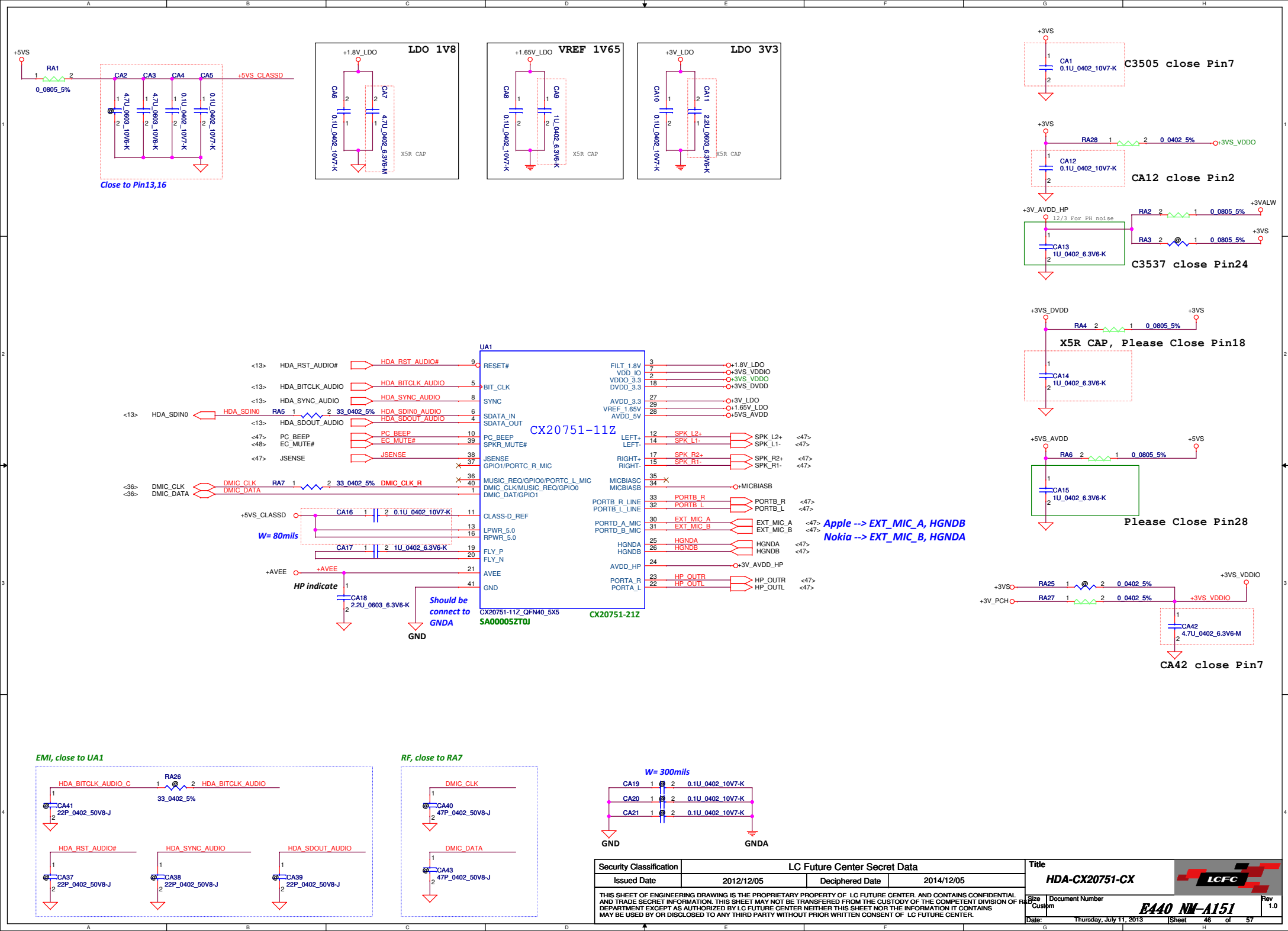


KeyBoard CONN.(14")

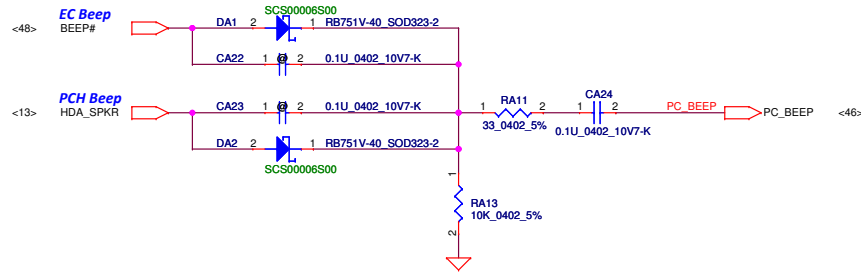


CONN PIN define need double check

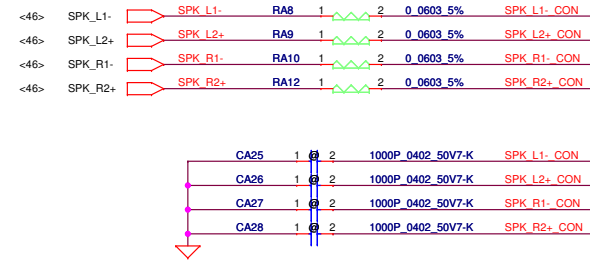




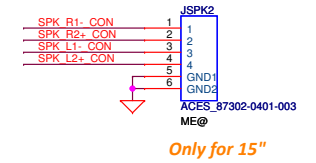
PC BEEP



Speaker OUT

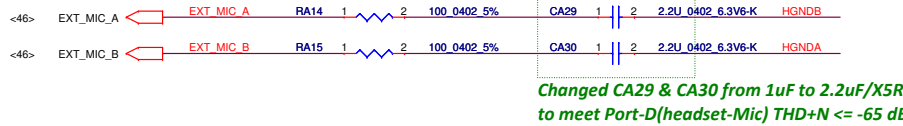


SPK CONN.

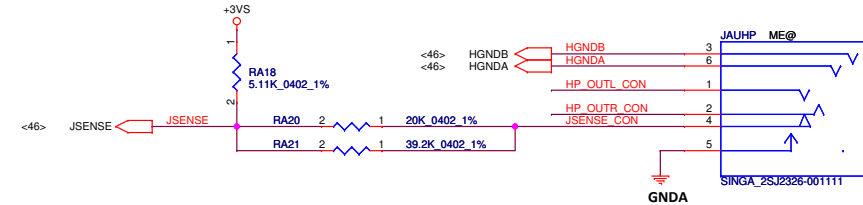


EXT. MIC/LINE IN

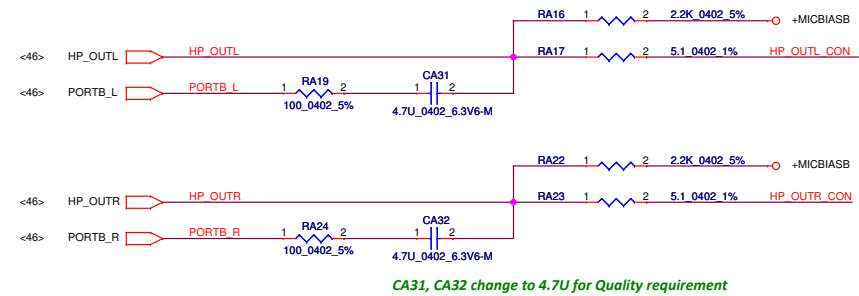
Apple --> EXT_MIC_A, HGNCB
Nokia --> EXT_MIC_B, HGNCB



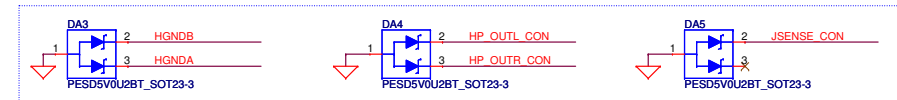
Audio Jack



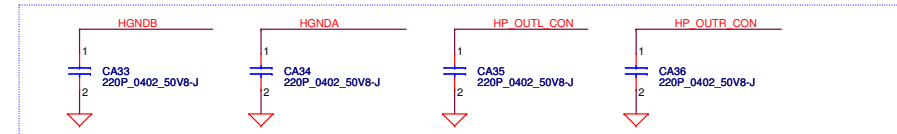
HeadPhone/LINE OUT




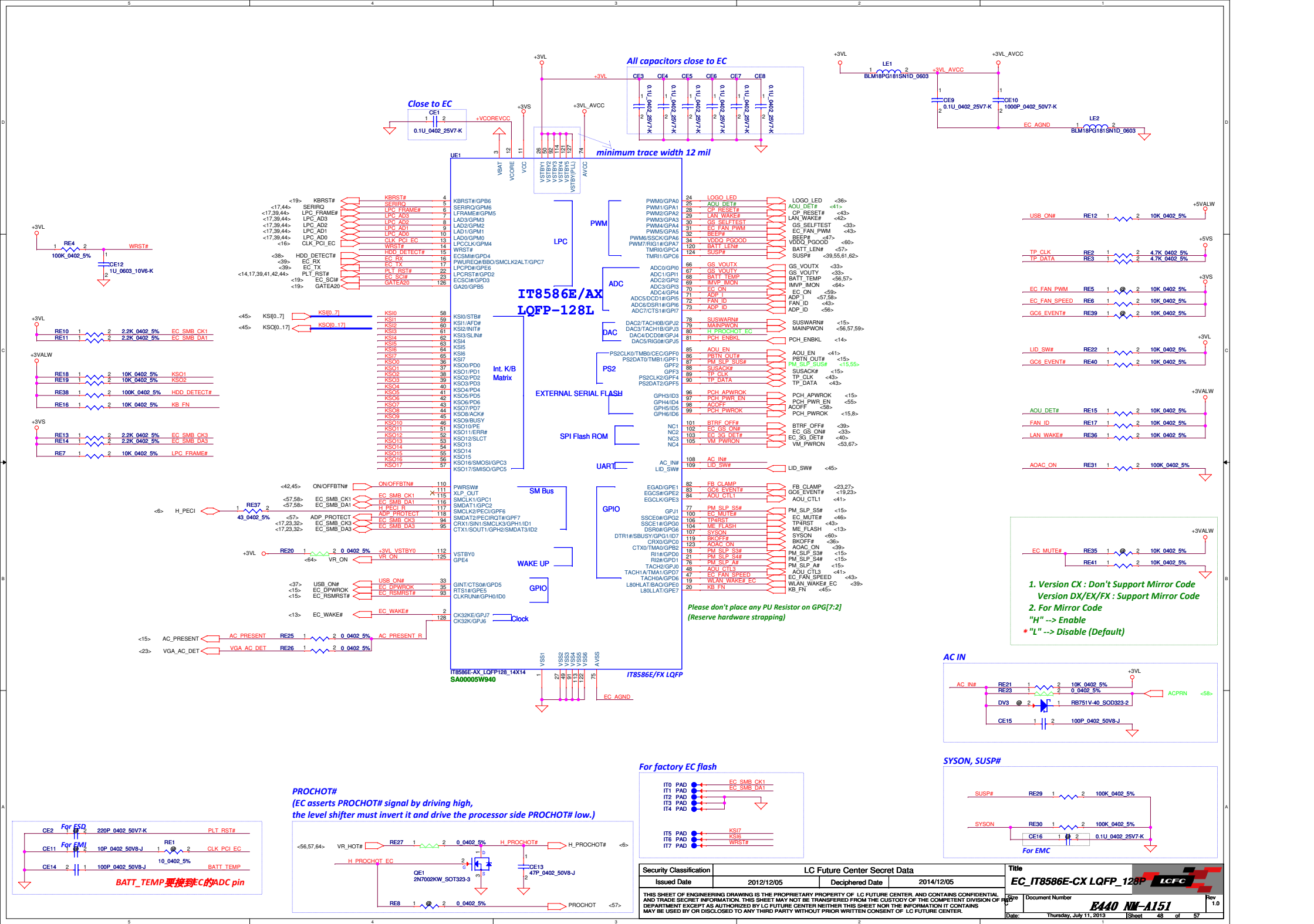
ESD Diode, close to JAUHP

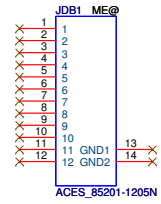



EMI, close to JAUHP

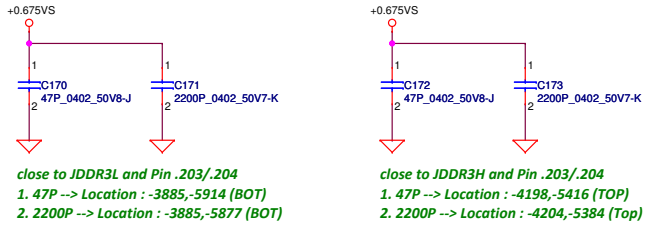
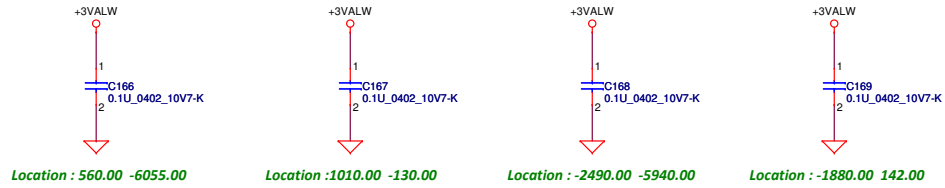


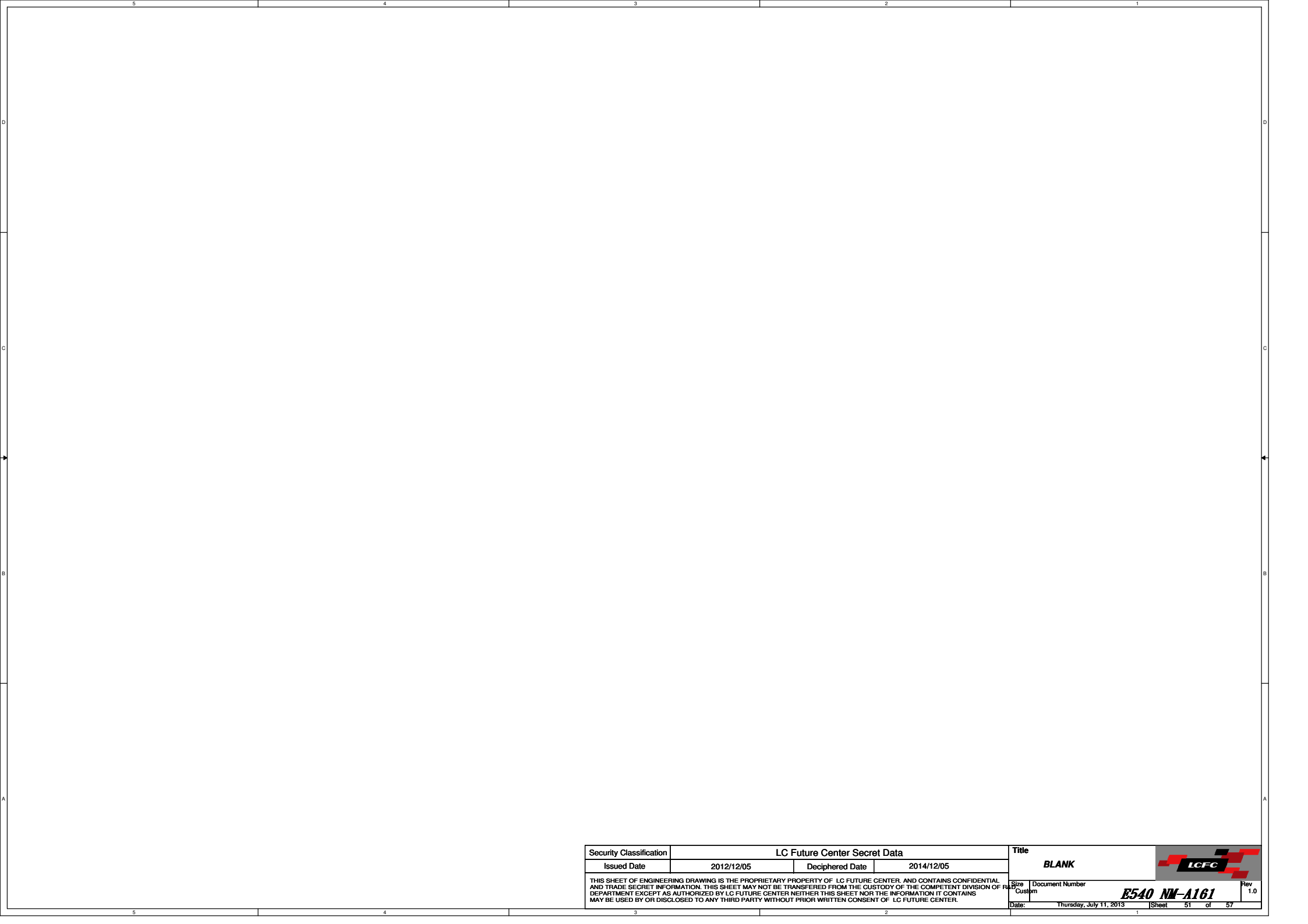
Security Classification		LC Future Center Secret Data				Title			
Issued Date		2012/12/05		Deciphered Date		2014/12/05			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.									
Size Custom		Document Number		E540 NM-A161				Rev 1.0	
Date:		Thursday, July 11, 2013		Sheet		47 of 57			






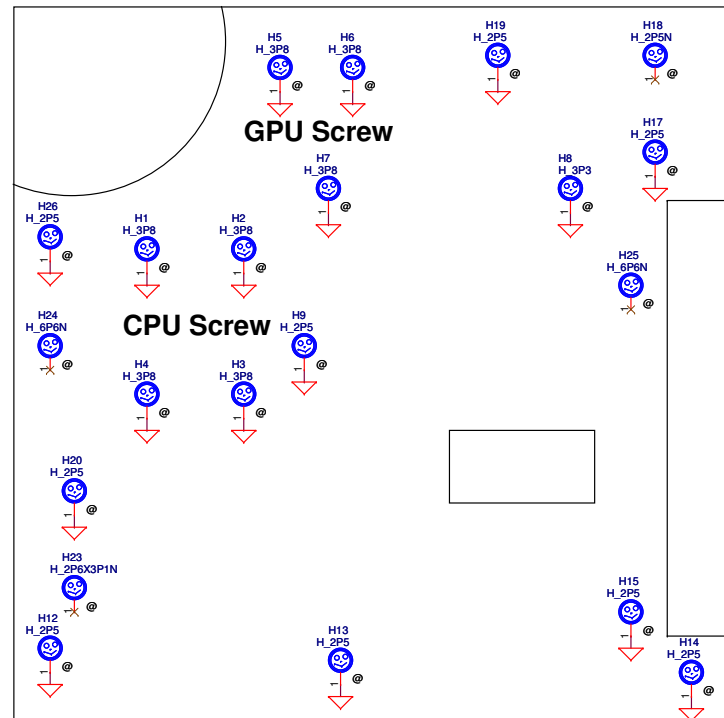
Security Classification	LC Future Center Secret Data			Title		
Issued Date	2012/12/05	Deciphered Date	2014/12/05	BLANK		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size	Document Number	Rev
				Custom	E440 NM-A151	1.0
				Date:	Thursday, July 11, 2013	Sheet 49 of 57






Security Classification	LC Future Center Secret Data			Title			
Issued Date	2012/12/05	Deciphered Date	2014/12/05	BLANK			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size	Document Number	Rev	
				Custom	E540 NW-A161	1.0	
				Date:	Thursday, July 11, 2013	Sheet	51 of 57

Screw Hole



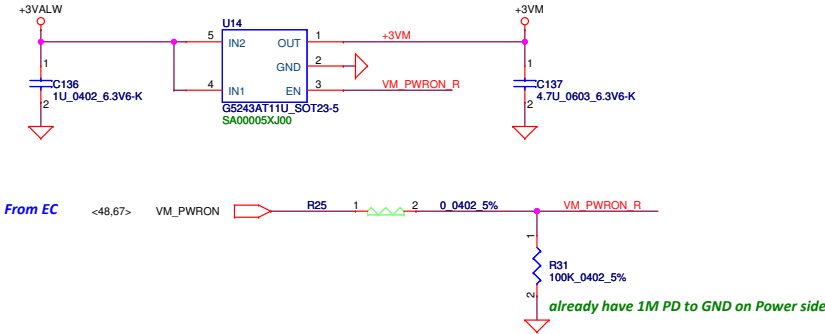
PCB Fedical Mark PAD



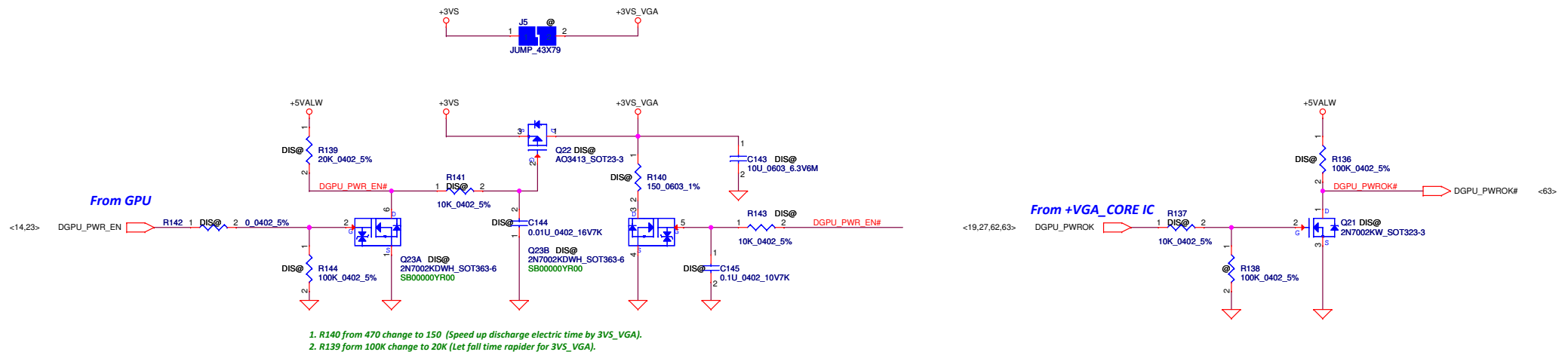
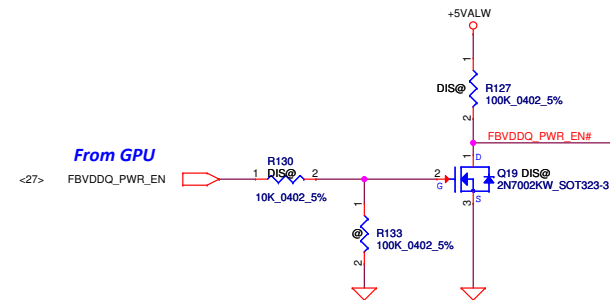
Security Classification	LC Future Center Secret Data			Title		
Issued Date	2012/12/05	Deciphered Date	2014/12/05	PLM/SCREW HOLE		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size Custom	Document Number E540 NM-A161	Rev 1.0
				Date:	Thursday, July 11, 2013	Sheet 52 of 57

+3VALW to +3VM


FOR SBA Function POWER(always mount)



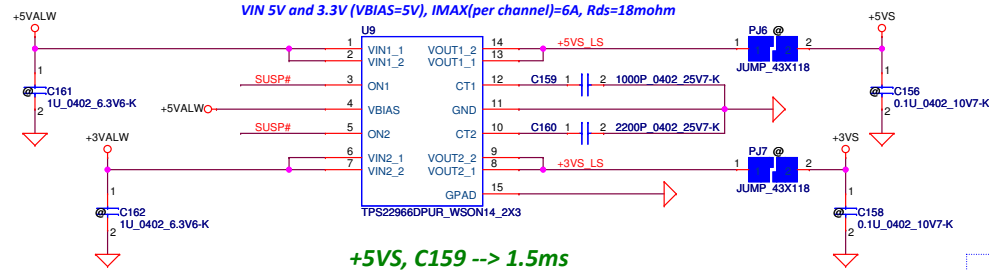
+3VS to +3VS_VGA



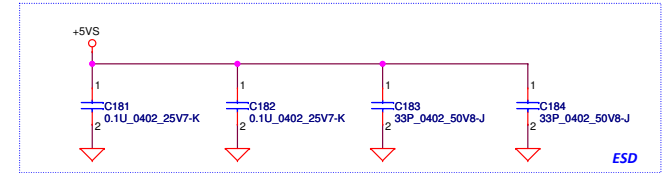
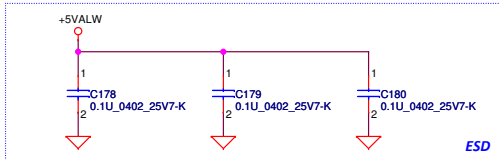
+3VS_VGA (En:DGPU_PWR_EN)
+VGA_CORE (En:NVDD_PWR_EN, POK:DGPU_PWROK)
+1.5VS_VGA (En:FBVDDQ_PWR_EN# = FB_CLAMP and DGPU_PWROK)
+1.05VS_VGA (En:DGPU_PWROK#)

Security Classification		LC Future Center Secret Data		Title								
Issued Date		2012/12/05	Deciphered Date	2014/12/05	DOCKING USB30/DP							
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.												
								Size	Document Number	E440 NW-A151		Rev 1.0
								Custom				
Date:		Thursday, July 11, 2013		Sheet	54	of	57					

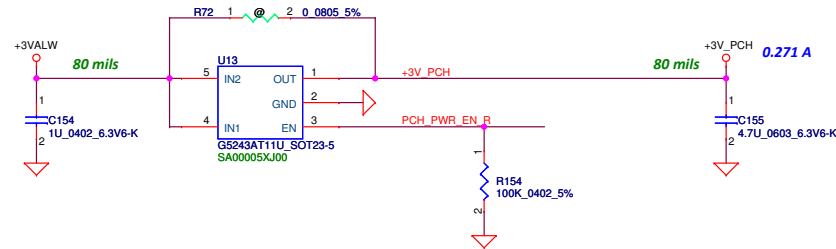
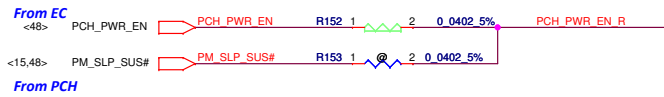
Load Switch
+5VALW To +5VS
+3VALW To +3VS



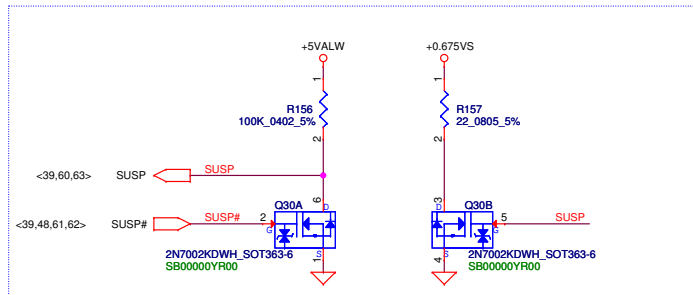
+5VS, C159 --> 1.5ms
+3VS, C160 --> 2.5ms

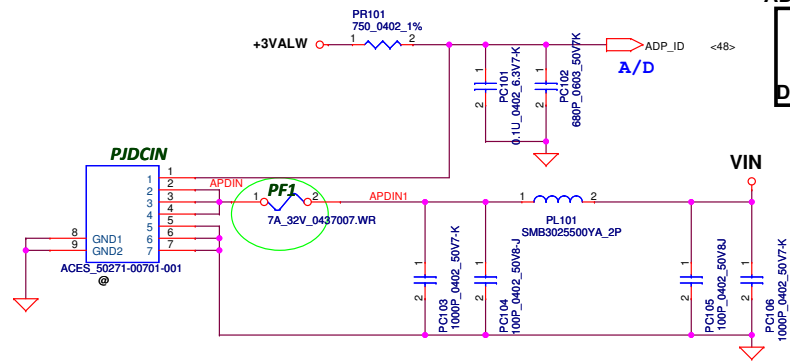


+3VALW To +3V_PCH

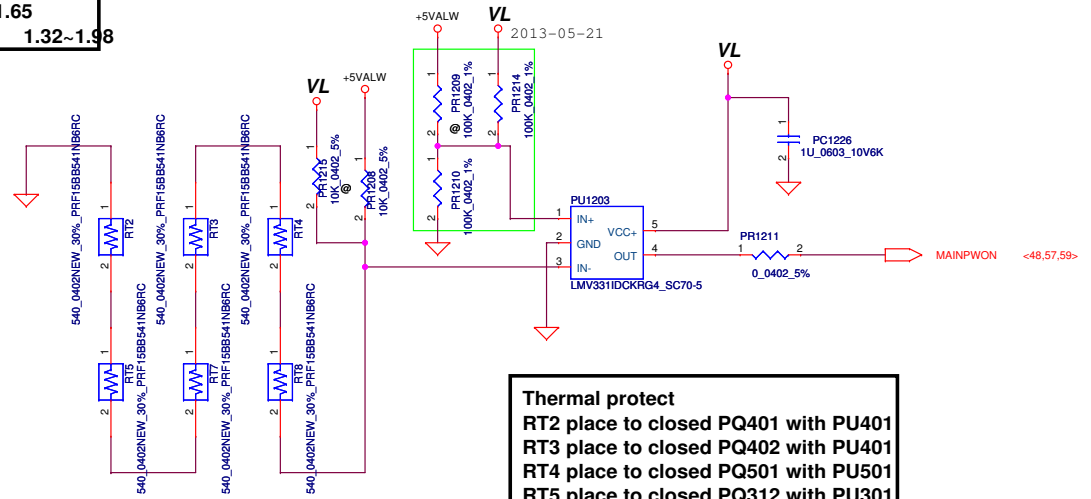


For DisCharge

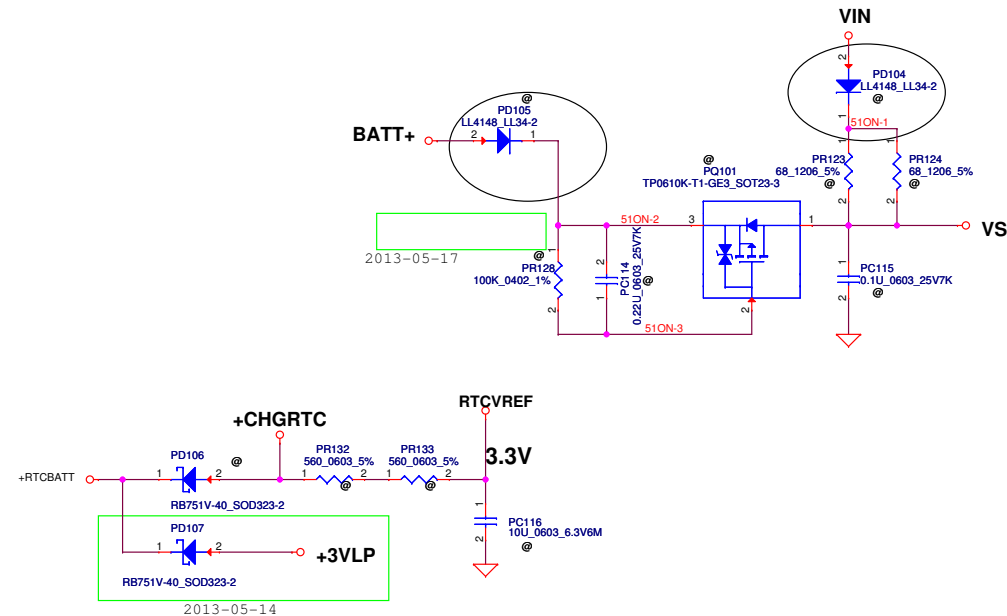




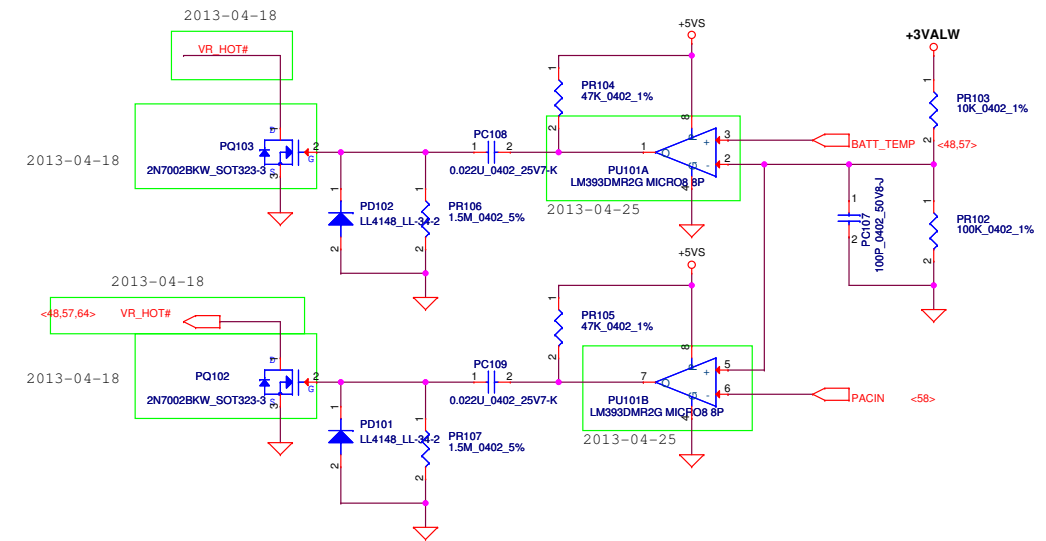
ADP_ID	AC Adapter	90W	65W
R(K ohm)	open	10	
ADP_ID(V)	3.3	1.65	
Detection voltage	>2.64	1.32~1.98	



Thermal protect
 RT2 place to closed PQ401 with PU401
 RT3 place to closed PQ402 with PU401
 RT4 place to closed PQ501 with PU501
 RT5 place to closed PQ312 with PU301
 RT7 place to closed PQ804 with PU801
 RT8 place to closed PQ1001 with PU901

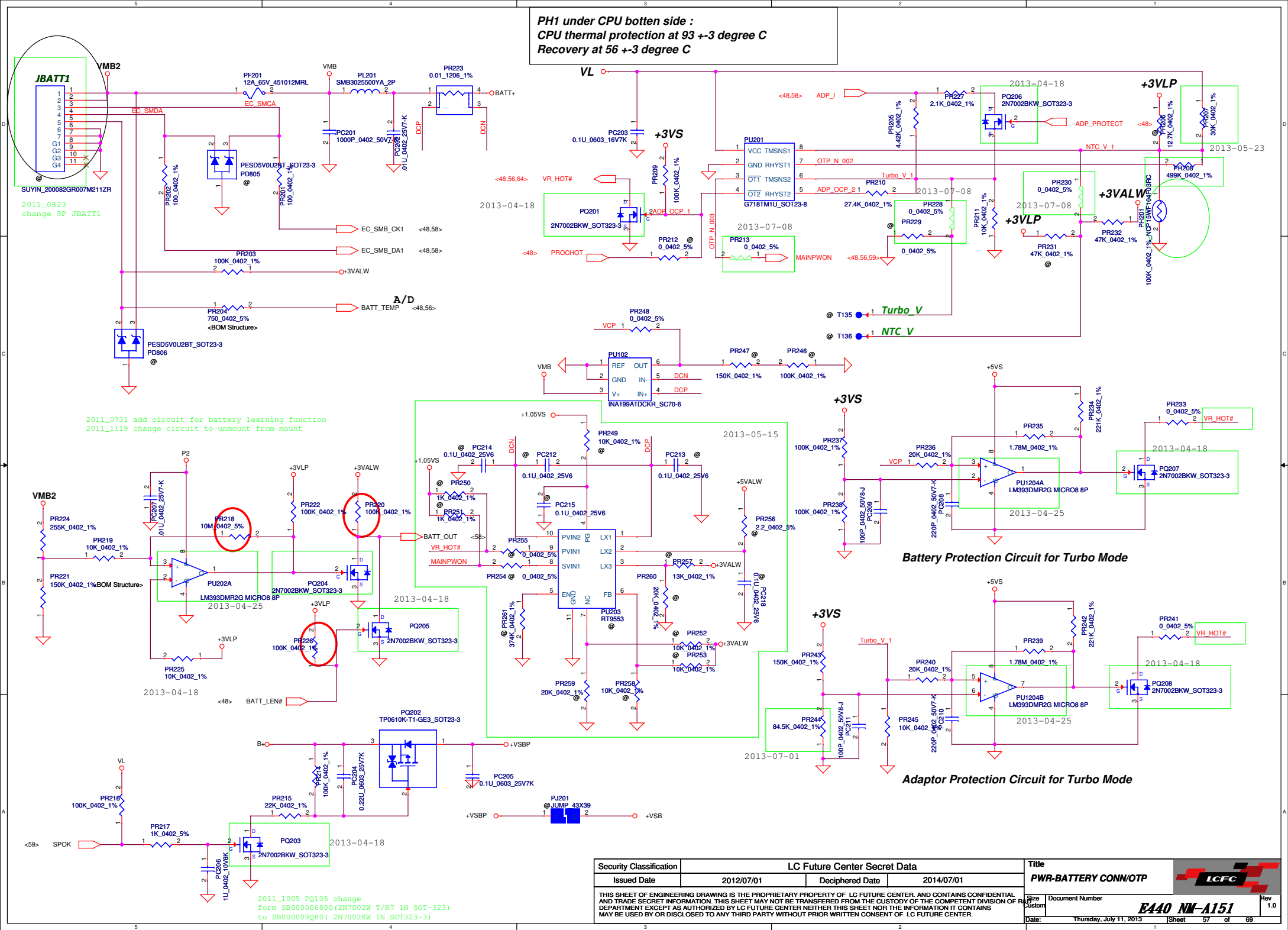


RTC Battery




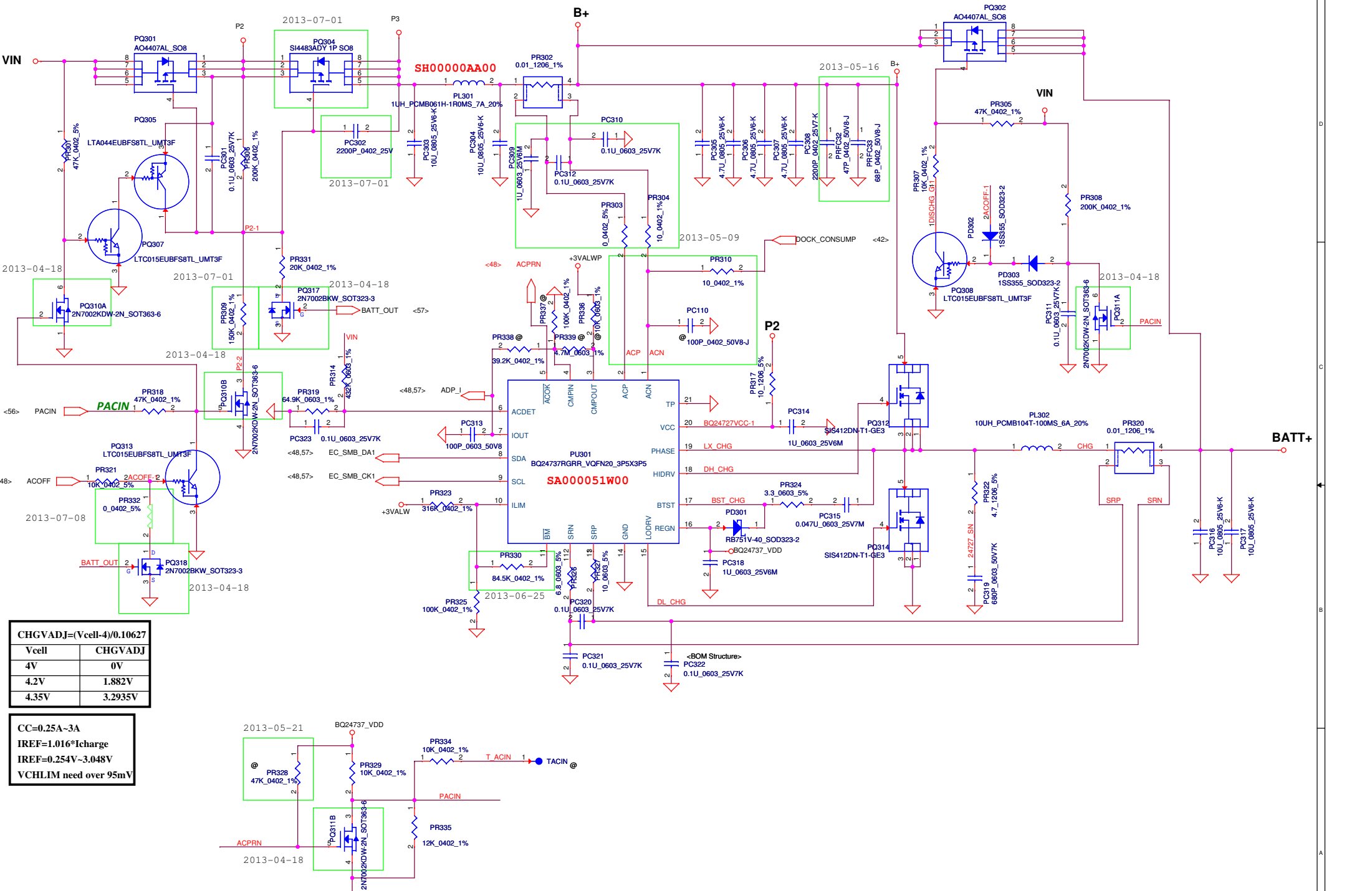
Security Classification	LC Future Center Secret Data			Title	E440 NM-A151	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	PWR-DCIN / Vin Detector	Size	Rev
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF P&E DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Document Number	36	1.0
Date:	Thursday, July 11, 2013	Sheet	36	of	69	

PH1 under CPU bottom side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.			

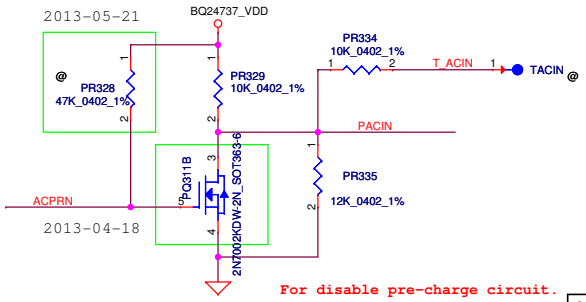
Title			
PWR-BATTERY CONN/OTP			
Size Custom	Document Number	<i>E440 NM-A151</i>	
Date:	Thursday, July 11, 2013	Sheet	57 of 69



CHGVADJ=(Vcell-4)/0.10627

Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

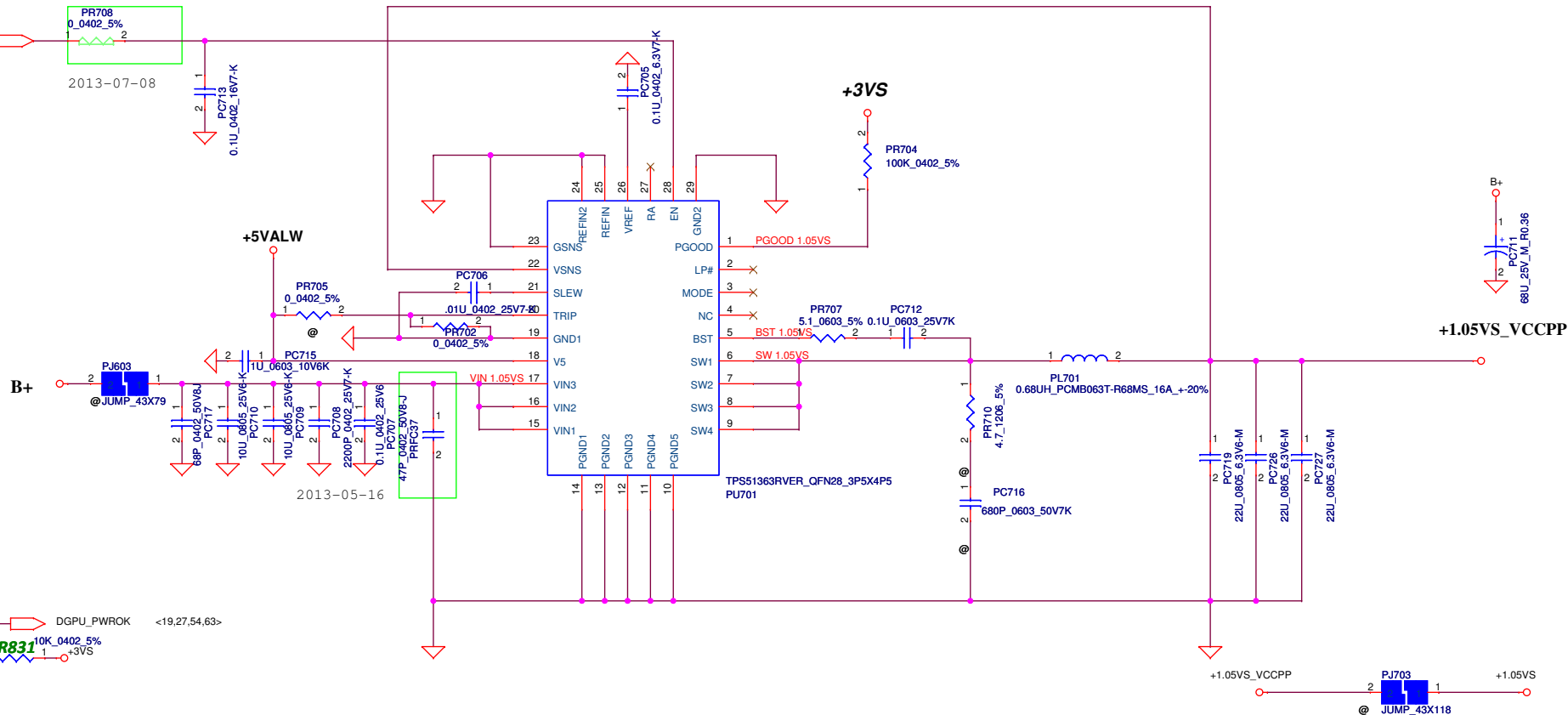
CC=0.25A-3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV



For disable pre-charge circuit.

<39,48,55,61> SUSP#

PR708
0.0402_5%
2013-07-08



+5VALW

PR703
0.0402_5%
2013-07-08

PR716
1M_0402_5%
PC721
0.1U_0402_6.3V7-K

PU702
SY8032ABC_SOT23-6


IN LX
PG GND
FB EN

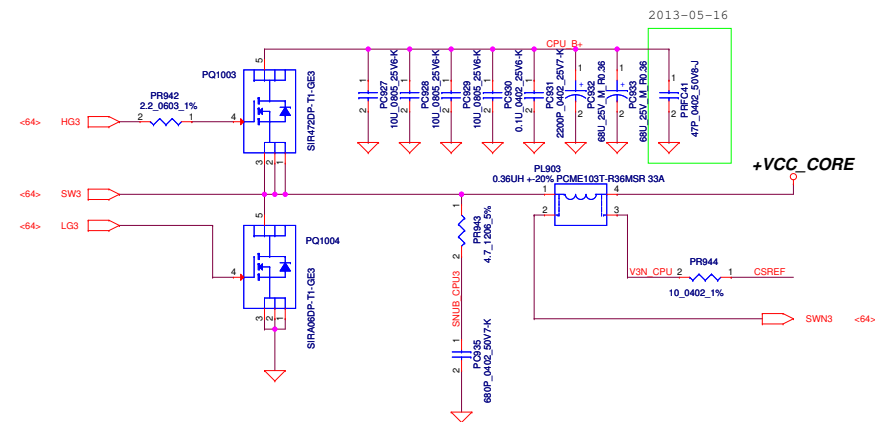
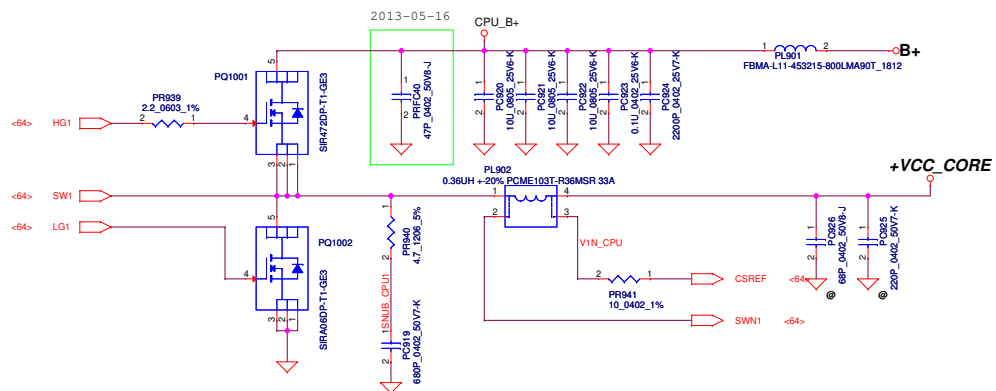
PL702
1UH_PH041H-1R0MS_3.8A_20%
PR717
4.7_1206_5%
PR718
20K_0402_1%
PC722
680P_0603_50V7K
PR719
10K_0402_1%

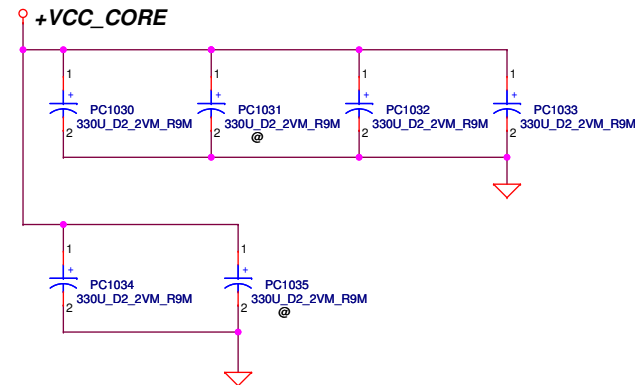
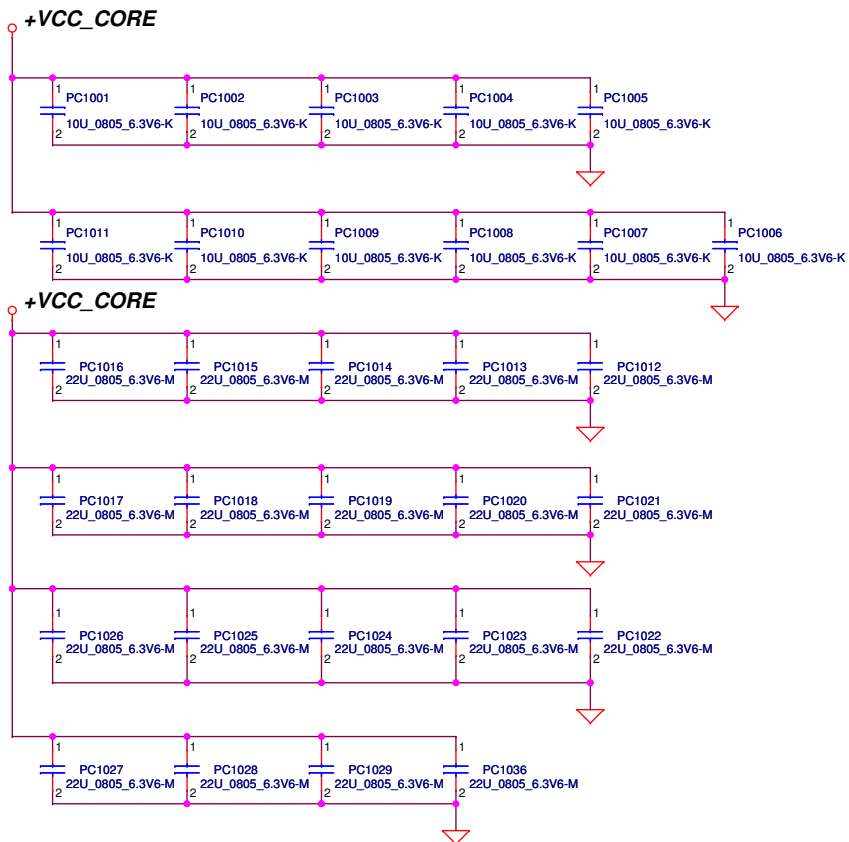
PC723
68P_0402_50V8
PC724
22U_0805_6.3V6-M
PC725
22U_0805_6.3V6-M

+1.8VSP

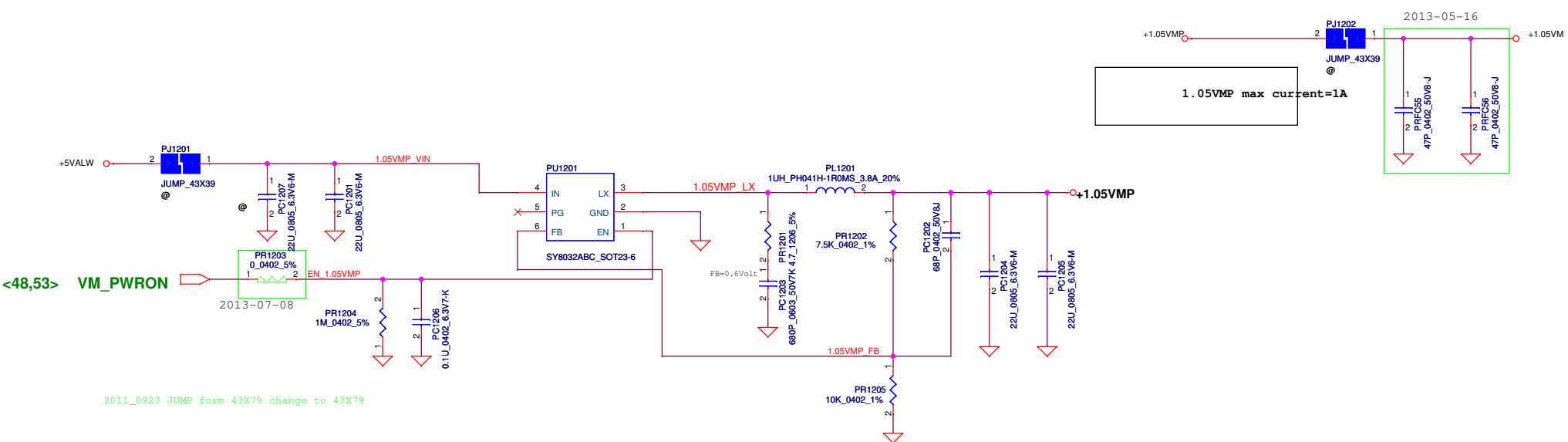
+1.8VSP
PJ704
JUMP_43X39

Security Classification	LC Future Center Secret Data			Title		
Issued Date	2012/07/01	Deciphered Date	2014/07/01	PWR--1.05VS_VCCPP/+1.8VSP		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FUTURE CENTER DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Document Number	E440 NM-A151	Rev 1.0
Date:	Thursday, July 11, 2013	Sheet	62	of	69	





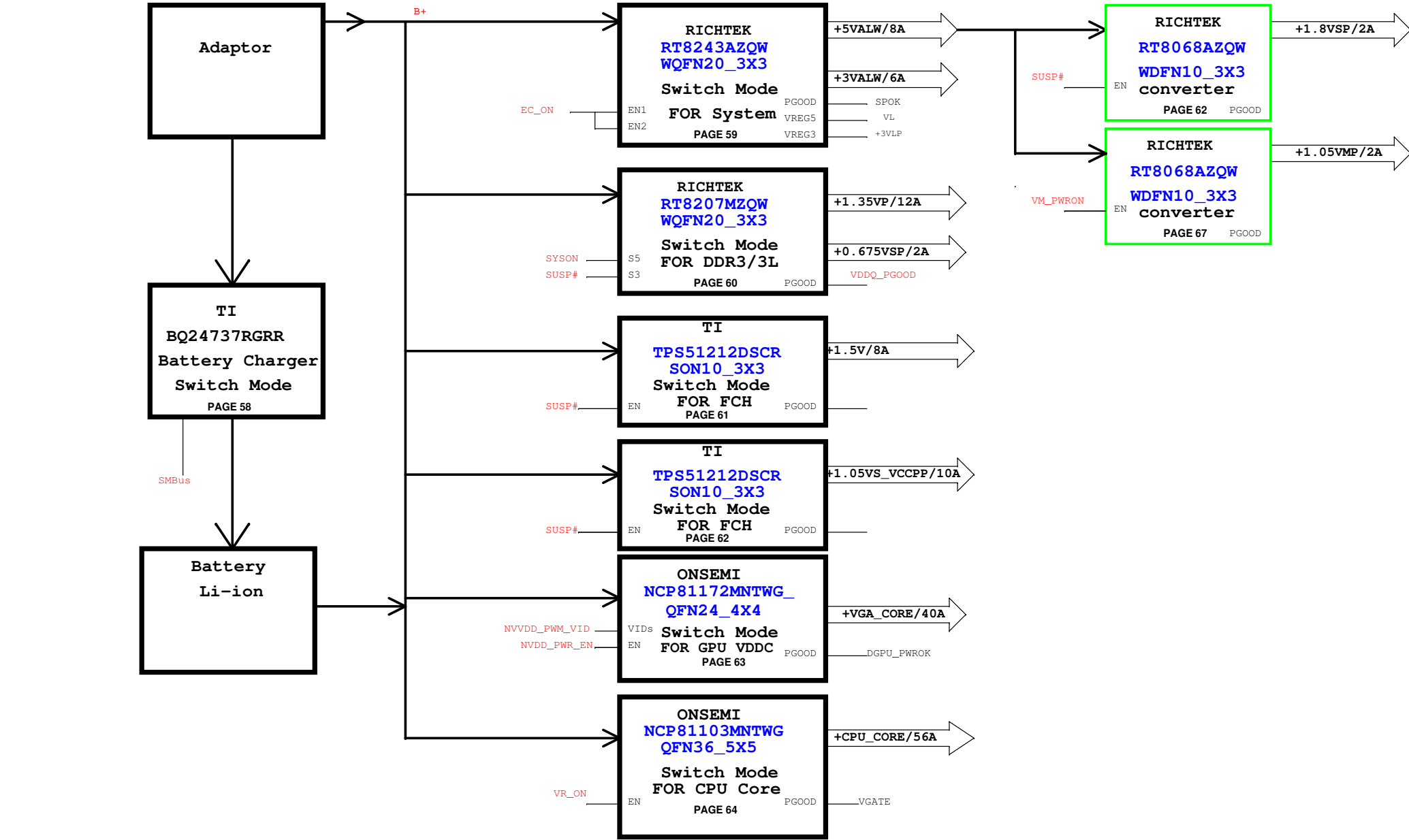
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	PWR-PROCESSOR DECOUPLING	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Document Number	Rev
				E440 NM-A151	1.0
Date: Thursday, July 11, 2013				Sheet 66	of 69



POWER PIR (Product Improve Record)

AILE1 NM-A151 SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1
GERBER-OUT DATE: 2013/01/16

NO DATE PAGE MODIFICATION LIST PURPOSE



HW PIR (Product Improve Record)

AILE1 NM-A151 SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1
GERBER-OUT DATE: 2013/01/16

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01)	03/14	10	R64	Change R64 BOM structure from "@" to "DS3@"
				For Deep S3 Function

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2012/12/05		Deciphered Date	
		2014/12/05		Title	
				PIR (PWR)	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Document Number		Rev	
		Y490-LA8691P		1.0	
Date:		Thursday, July 11, 2013		Sheet 69 of 69	