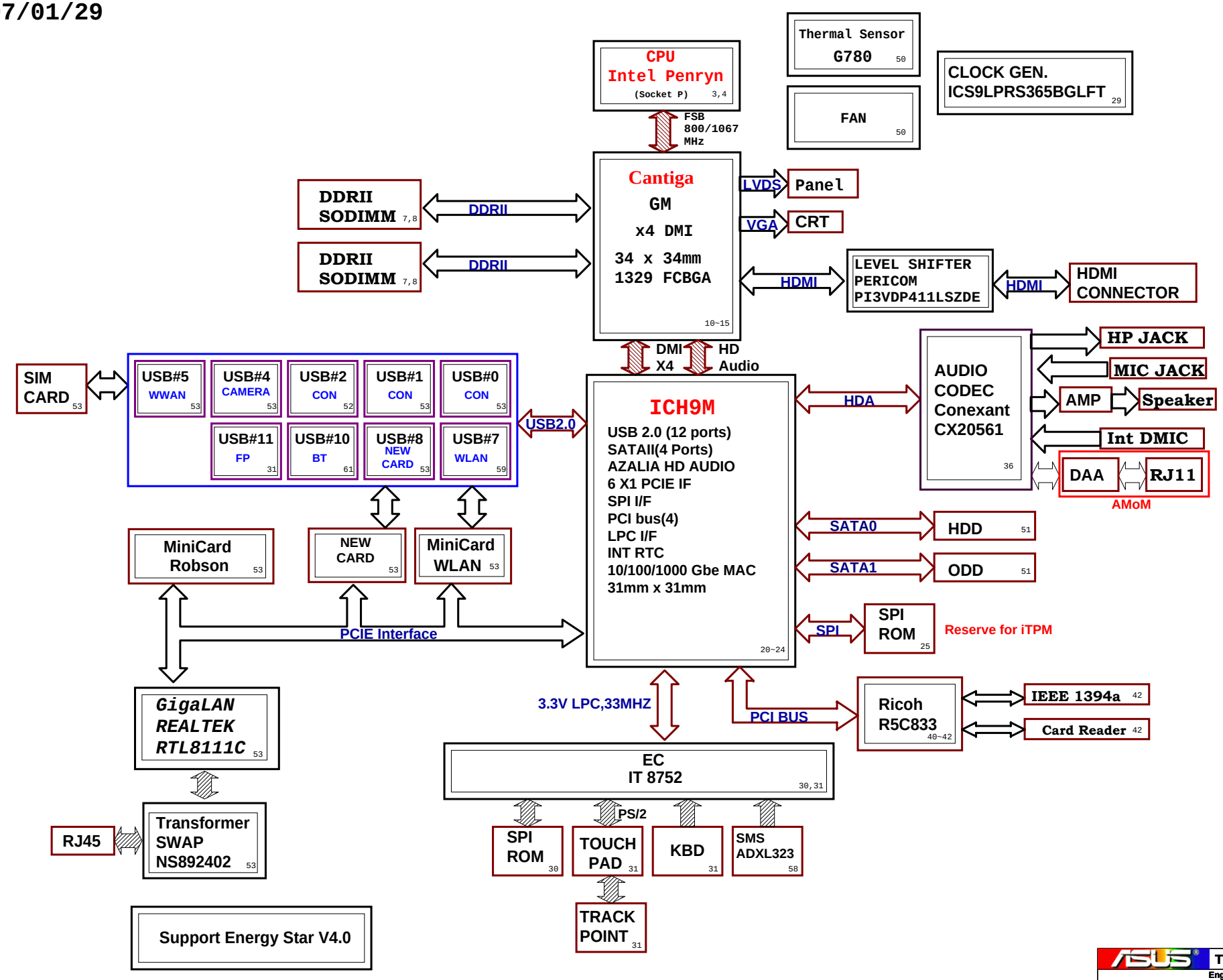
B3 NOTE 13" UMA Block Diagram
2007/01/29



Title : Block Diagram			
Engineer: Peter Lo			
Size: C	Project Name: Rocky30		Rev: 1.0
Date: Tuesday, January 29, 2008	Sheet 1 of 94		

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90	PWR_DETECT
91	PWR_LOAD SWITCH
92	PWR_PROTECT
93	PWR_SIGNAL
94	PWR_FLOWCHART

ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	GPI	PM_SYNC#	+3VS
GPIO 01	GPI	-	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#	+3VS
GPIO 06	GPI		+3VS
GPIO 07	GPI		+3VS
GPIO 08	GPI	EXT_SMI#	+3VSUS
GPIO 09	Native	UWB_ON	+3VSUS
GPIO 10	GPI	-	+3VSUS
GPIO 11	Native	EXT_SCI#	+3VSUS
GPIO 12	GPO	-	+3VSUS
GPIO 13	GPI	CB_SD#	+3VSUS
GPIO 14	GPI	RTLAN_DSM#	+3VSUS
GPIO 15	Native	-	+3VSUS
GPIO 16	Native	PM_DPRSLPVR	+3VS
GPIO 17	GPI	WLAN_LED	+3VS
GPIO 18	GPO		+3VS
GPIO 19	GPI	-	+3VS
GPIO 20	GPO	-	+3VS
GPIO 21	GPI	-	+3VS
GPIO 22	GPI	BT_DET#	+3VS
GPIO 23	Native	-	+3VS
GPIO 24	GPO	WLAN_ON	+3VSUS
GPIO 25	Native	-	+3VSUS
GPIO 26	Native	-	+3VSUS
GPIO 27	GPO	BT_ON	+3VSUS
GPIO 28	GPO	-	+3VSUS
GPIO 29	Native	USB_OC5#	+3VSUS
GPIO 30	Native	USB_OC6#	+3VSUS
GPIO 31	Native	USB_OC7#	+3VSUS
GPIO 32	GPO	-	+3VS
GPIO 33	GPO	-	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	CLK_SATA_REQ#	+3VS
GPIO 36	GPI	GPIO36	+3VS
GPIO 37	GPI	PCB_ID0	+3VS
GPIO 38	GPI	PCB_ID1	+3VS
GPIO 39	GPI	PCB_ID2	+3VS
GPIO 40	Native	USB_OC1#	+3VSUS
GPIO 41	Native	USB_OC2#	+3VSUS
GPIO 42	Native	USB_OC3#	+3VSUS
GPIO 43	Native	USB_OC4#	+3VSUS
GPIO 44	Native	USB_OC8#	N/A
GPIO 45	Native	USB_OC9#	N/A
GPIO 46	Native	USB_OC10#	N/A
GPIO 47	Native	USB_OC11#	N/A
GPIO 48	GPI	-	+3VS
GPIO 49	GPO	HDCP_EEPROM_PROTECT#	**+3VS**
GPIO 50	Native	PCI_REQ#1	+3VS
GPIO 51	Native	-	+3VS
GPIO 52	Native	PCI_REQ#2	+3VS
GPIO 53	Native	-	+3VS
GPIO 54	Native	PCI_REQ#3	+3VS
GPIO 55	Native	-	+3VS
GPIO 56	GPI	-	+3VSUS
GPIO 57	GPI	-	+3VSUS
GPIO 58	GPI	-	+3VSUS
GPIO 59	Native	USB_OC0#	+3VSUS
GPIO 60	Native	RTLAN_DSM_EN	+3VSUS

EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED#	
GPA1	GPO	CHG_LED#	
GPA2	GPO	BATSEL_3S#	
GPA3	-	NOVO_CARE_LED#	
GPA4	GPO	LCD_BL_PWM	
GPA5	GPO	FAN_PWM	
GPA6	GPO	-	
GPA7	GPO	-	
GPB0	GPO	CHG_EN#	
GPB1	GPO	PRECHG	
GPB2	GPI	-	
GPB3	ALT	SMB0_CLK	
GPB4	ALT	SMB0_DAT	
GPB5	OD	A20GATE	
GPB6	OD	RCIN#	
GPB7	GPO	PM_RSMRST#	
GPC0	GPI	-	
GPC1	ALT	SMB1_CLK	
GPC2	ALT	SMB1_DAT	
GPC3	GPO	PM_PWRBTN#	
GPC4	ALT	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	ALT	BAT1_IN_OC#	
GPC7	GPO	RFON_SW#	
GPD0	GPI	PWRLIMIT#	
GPD1	ALT	PM_SUSC#	
GPD2	ALT	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	ALT	FAN0_TACH	
GPD7	GPI	-	
GPE0	GPO	VSUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC#	
GPE3	GPO	CPU_VRON	
GPE4	ALT	PWR_SW#	
GPE5	ALT	-	
GPE6	GPI	LID_SW#	
GPE7	GPO	MEDIA_KEY#	
GPF0	GPI	-	
GPF1	GPI	NOVO_CARE#	
GPF2	ALT	TP1_CLK	
GPF3	ALT	TP1_DAT	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	GPO	SUSPEND_LED#	
GPG0	GPI	PM_THERM#_EC	
GPG1	ALT	PM_SUSB#	
GPG2	GPO	BAT1_CNT2#	
-	-	-	
-	-	-	

EC GPIO	Use As	Signal Name	Power
-	-	-	
GPG6	GPO	-	
-	-	-	
GPH0	OD	PM_CLKRUN#	
GPH1	ALT	3G_ON#	
GPH2	ALT	LOGO_LED#	
GPH3	GPO	BAT_LEARN	
GPH4	GPO	-	
GPH5	GPO	NUM_LED#	
GPH6	GPO	CAP_LED#	
-	-	-	
GPI0	GPI	NV_OVERT#	
GPI1	GPI	SUS_PWRGD	
GPI2	GPI	ALL_SYSTEM_PWRGD	
GPI3	GPI	VRM_PWRGD	
GPI4	GPI	XOUT	
GPI5	GPI	YOUT	
GPI6	GPI	-	
GPI7	GPI	-	
GPJ0	GPO	EC_CLK_EN	
GPJ1	GPO	PM_PWROK	
GPJ2	GPI	-	
GPJ3	-	-	
GPJ4	GPO	BL_DA	
GPJ5	GPO	-	
GPK0	GPI	-	
GPK1	GPI	-	
GPK2	GPI	-	
GPK3	GPI	-	
GPK4	GPI	-	
GPK5	GPI	-	
GPL0	GPI	APS_PWR_CNT#	
GPL1	GPI	APS_ST#	
GPL2	GPO	USB_PWR_EN#	
GPL3	GPO	-	
GPL4	GPO	-	
GPL5	GPO	AC_ID	
GPL6	GPO	AC_65W	
GPL7	GPO	CHG_LOW_LED#	
GPK6	GPO	-	
GPK7	GPI	-	

ASUS Title : Schematic Information

Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.0

Date: Tuesday, January 15, 2008 Sheet 2 of 94

10 H_D#[63:0] — H_D#[63:0]

10 H_A#[35:3] — H_A#[35:3]

10 H_REQ#[4:0] — H_REQ#[4:0]

Reserved for the S3 reboot issue

U0301A

ADDR GROUP 0: H_A#3 J4, H_A#4 L5, H_A#5 L4, H_A#6 K5, H_A#7 M3, H_A#8 N2, H_A#9 J1, H_A#10 N3, H_A#11 P5, H_A#12 P2, H_A#13 L2, H_A#14 P4, H_A#15 P1, H_A#16 R1, 10 H_ADSTB#0 M1; H_REQ#0 K3, H_REQ#1 H2, H_REQ#2 K2, H_REQ#3 J3, H_REQ#4 L1

ADDR GROUP 1: H_A#17 Y2, H_A#18 U5, H_A#19 R3, H_A#20 W6, H_A#21 U4, H_A#22 Y5, H_A#23 U1, H_A#24 R4, H_A#25 T5, H_A#26 T3, H_A#27 W2, H_A#28 W5, H_A#29 Y4, H_A#30 U2, H_A#31 V4, H_A#32 W3, H_A#33 AA4, H_A#34 AB2, H_A#35 AA3, 10 H_ADSTB#1 V1

H CLK: 20 H_A20M# A6, 20 H_FERR# A5, 20 H_IGNNE# C4; 20 H_STPCLK# D5, 20 H_INTR C6, 20 H_NMI B4, 20 H_SMI# A3

RESERVED: T0308 M4, T0309 N5, T0310 T2, T0311 V3, T0312 B2, T0313 C3, T0314 D2, T0315 D22, T0316 D3, T0317 E6

CONTROL: ADS# H1 — H_ADS# 10; BNR# E2 — H_BNR# 10; BPRI# G5 — H_BPRI# 10; DEFER# H5 — H_DEFER# 10; DRDY# F21 — H_DRDY# 10; DBSY# E1 — H_DBSY# 10; BR0# F1 — H_BR0# 10; IERR# D20 — H_IERR# — R0309 1 2 56Ohm — +VCCP_CPU; INIT# B3 — H_INIT# 20; LOCK# H4 — H_LOCK# 10 — T0352; RESET# C1 — H_CPURST# 10; RS[0]# F3 — H_RS#0 10; RS[1]# F4 — H_RS#1 10; RS[2]# G3 — H_RS#2 10; TRDY# G2 — H_TRDY# 10; HIT# G6 — H_HIT# 10; HITM# E4 — H_HITM# 10

Place Series Resistor on H_CPURST# Without Stub

XDP/ITP SIGNALS: BPM[0]# AD4 — T0330; BPM[1]# AD3 — XDP_BPM#1; BPM[2]# AD1 — T0331; BPM[3]# AC4 — T0332; PRDY# AC2 — T0333; PREQ# AC1 — H_PREQ#; TCK AC5 — H_TCK; TDI AA6 — H_TDI; TDO AB3 — H_TDO; TMS AB5 — H_TMS; TRST# AB6 — H_TRST#; DBR# C20 — H_DBR#

THERMAL: PROCHOT# D21 — H_PROCHOT_S#; THRMDA A24 — CPU_THRM_DA 50; THRMDC B25 — CPU_THRM_DC 50; THERMTRIP# C7 — H_THRMTRIP# 5,11,20,31

To Thermal sensor page

T0302 — A22 — CLK_CPU_BCLK 29; A21 — CLK_CPU_BCLK# 29 — T0303

SOCKET478BR

H_CPURST# — @ C0302 10PF/50V

U0301B

DATA GRP 0: H_D#0 E22, H_D#1 F24, H_D#2 E26, H_D#3 G22, H_D#4 E23, H_D#5 G25, H_D#6 E25, H_D#7 E23, H_D#8 K24, H_D#9 G24, H_D#10 J24, H_D#11 J23, H_D#12 H22, H_D#13 F26, H_D#14 K22, H_D#15 H23; 10 H_DSTBN#0 J26, 10 H_DSTBP#0 H26, 10 H_DINV#0 H25

DATA GRP 2: D[32]# Y22 H_D#32, D[33]# AB24 H_D#33, D[34]# V24 H_D#34, D[35]# V26 H_D#35, D[36]# V23 H_D#36, D[37]# T22 H_D#37, D[38]# U25 H_D#38, D[39]# U23 H_D#39, D[40]# Y25 H_D#40, D[41]# W22 H_D#41, D[42]# Y23 H_D#42, D[43]# W24 H_D#43, D[44]# W25 H_D#44, D[45]# AA23 H_D#45, D[46]# AA24 H_D#46, D[47]# AB25 H_D#47; DSTBN[2]# Y26 — H_DSTBN#2 10; DSTBP[2]# AA26 — H_DSTBP#2 10; DINV[2]# U22 — H_DINV#2 10

DATA GRP 1: H_D#16 N22, H_D#17 K25, H_D#18 P26, H_D#19 R23, H_D#20 L23, H_D#21 M24, H_D#22 L22, H_D#23 M23, H_D#24 P25, H_D#25 P23, H_D#26 P22, H_D#27 T24, H_D#28 R24, H_D#29 L25, H_D#30 T25, H_D#31 N25; 10 H_DSTBN#1 L26, 10 H_DSTBP#1 M26, 10 H_DINV#1 N24

DATA GRP 3: D[48]# AE24 H_D#48, D[49]# AD24 H_D#49, D[50]# AA21 H_D#50, D[51]# AB22 H_D#51, D[52]# AB21 H_D#52, D[53]# AC26 H_D#53, D[54]# AD20 H_D#54, D[55]# AE22 H_D#55, D[56]# AF23 H_D#56, D[57]# AC25 H_D#57, D[58]# AE21 H_D#58, D[59]# AD21 H_D#59, D[60]# AC22 H_D#60, D[61]# AD23 H_D#61, D[62]# AF22 H_D#62, D[63]# AC23 H_D#63; DSTBN[3]# AE25 — H_DSTBN#3 10; DSTBP[3]# AF24 — H_DSTBP#3 10; DINV[3]# AC20 — H_DINV#3 10

MISC: GTLREF, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6; BSEL[0] B22 — 29 CPU_BSEL0; BSEL[1] B23 — 29 CPU_BSEL1; BSEL[2] C21 — 29 CPU_BSEL2

COMP[0] R26 — H_COMP0 — R0311 1 2 27.4Ohm 1%; COMP[1] U26 — H_COMP1 — R0312 1 2 54.9Ohm 1%; COMP[2] AA1 — H_COMP2 — R0313 1 2 27.4Ohm 1%; COMP[3] Y1 — H_COMP3 — R0314 1 2 54.9Ohm 1%

DPRSTP# E5 — H_DPRSTP# 11,20,80; DPSLP# B5 — H_DPSLP# 20; DPWR# D24 — H_DPWR# 10; PWRGOOD D6 — H_PWRGD 20; SLP# D7 — H_CPUSLP# 10; PSI# AE6 — PM_PSI# 80

SOCKET478BR

Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5". Comp 1,3 connect with Z0=55 ohm, make trace length shorter than 0.5".

Place Series Resistor on H_PWRGD Without Stub

+VCCP_CPU — R0319 2 1 200Ohm @

+VCCP_CPU — R0315 1KOhm 1% — GTL_REF — R0316 2KOhm 1% — C0301 0.1UF/10V @

R0317 2 @ 1% 1 1KOhm — R0318 2 @ 1% 1 1KOhm

T0304 1 C24; T0305 1 AF26; T0306 1 AF1; T0307 1 A26

Zo=55 ohm, 0.5" max for GTLREF

BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L

Default Strapping When Not Used

+VCCP_CPU

XDP_BPM#1 R0301 1 2 54.9Ohm 1% @

H_PREQ# R0302 1 2 54.9Ohm 1%

H_TDI R0303 1 2 54.9Ohm 1%

H_TDO R0304 1 2 54.9Ohm 1% @

H_TMS R0305 1 2 54.9Ohm 1%

H_DBR# R0306 1 2 1KOhm 1% @ — +3VS

H_TCK R0307 1 2 54.9Ohm 1%

H_TRST# R0308 1 2 54.9Ohm 1%

Place R0304 & R0306 for XDP function

+VCCP_CPU — R0310 68Ohm — H_PROCHOT_S# — D0301 RB751V-40 — 30,88 PWRLIMIT#

Q0301 2N7002E-T1-E3 — G — THRO_CPU 30

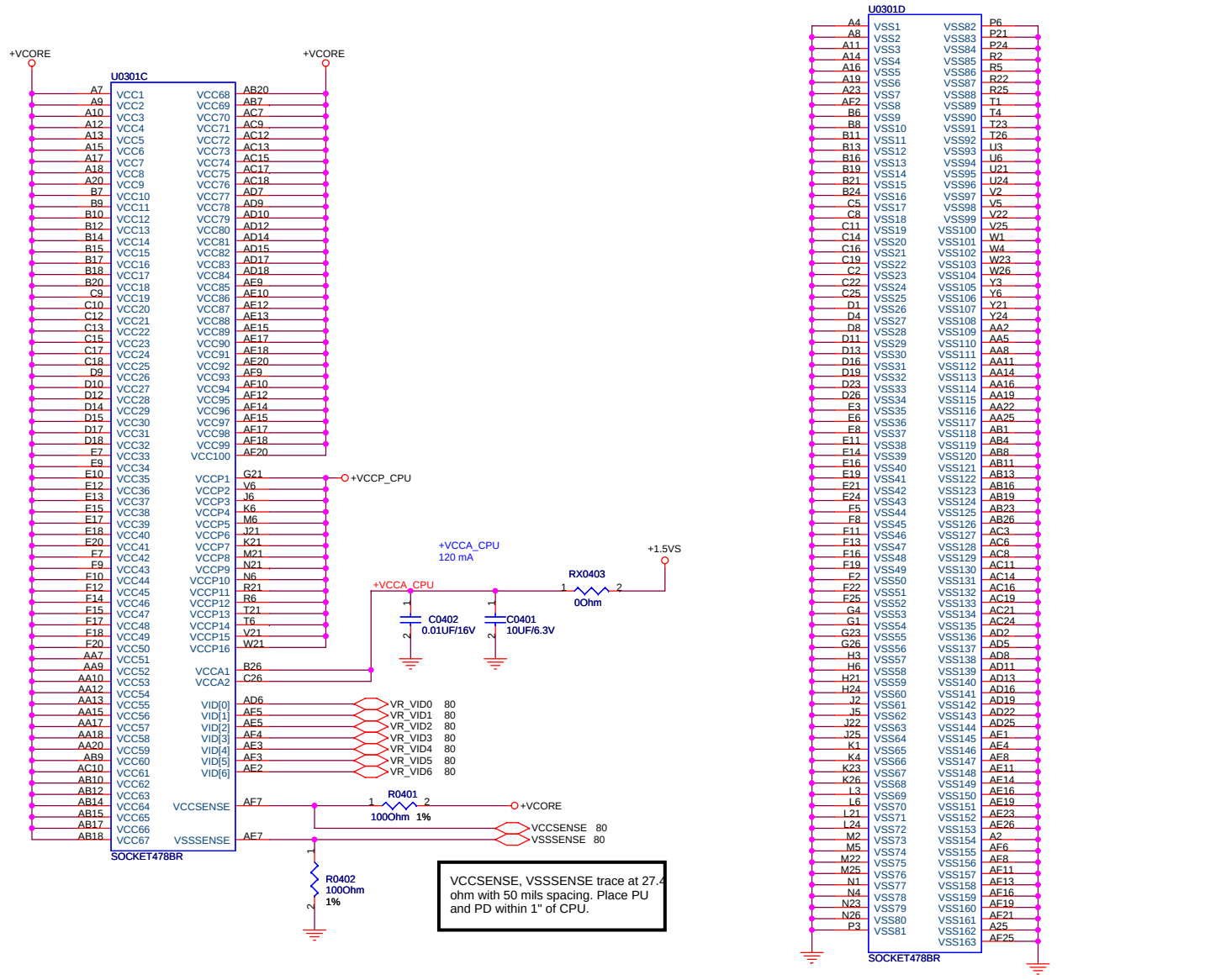
ASUS

Title : Penryn CPU (1)

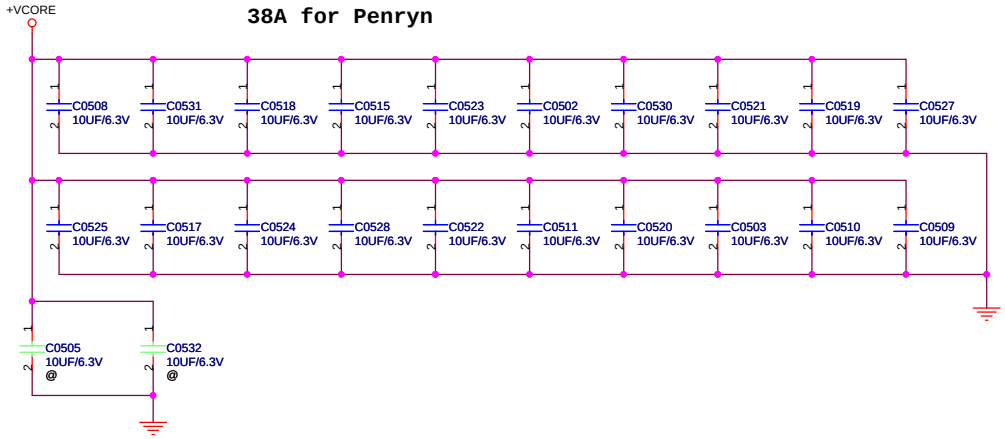
Engineer: Peter Lo

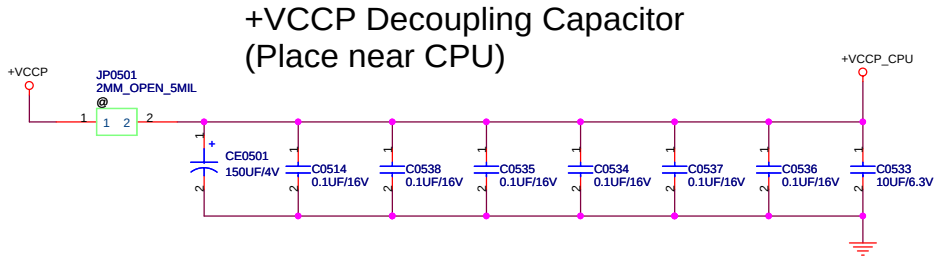
Size	Project Name	Rev
Custom	Rocky30	1.0

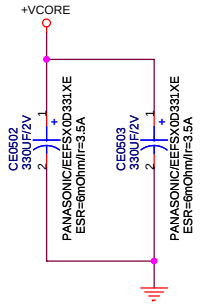
Date: Monday, February 04, 2008 Sheet 3 of 94

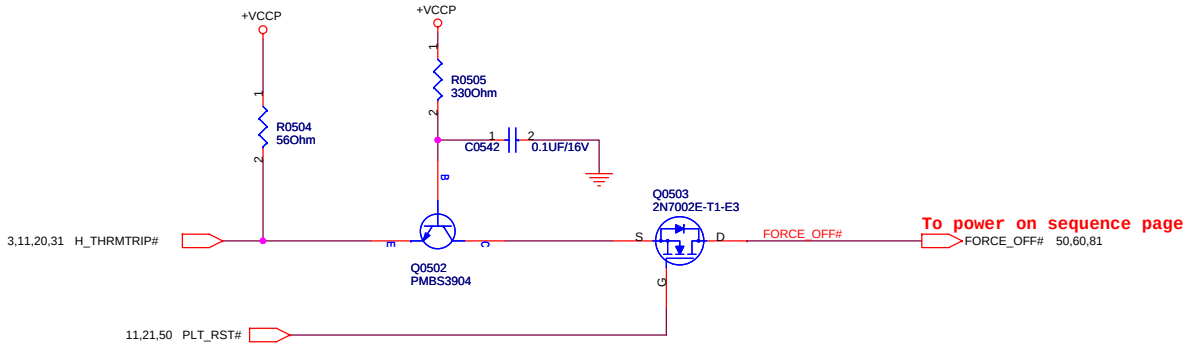


Title : Penryn CPU (2)		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 4 of 94	









Thermal Trip signal(From CPU to ICH-9M and sequence)

Title : CPU CAPS		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 5 of 94	

Title :	
Engineer:	Peter Lo
Size: A	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
Sheet	6 of 94

+3VS +3VS 3,8,11,14,15,20,22,23,24,25,29,30,31,37,40,41,45,46,48,50,51,53,54,57,58,59,61,91,92

+1.8V +1.8V 8,9,11,13,83,91

M_VREF_MCH M_VREF_MCH 8,9,11

SMBus Slave Address:A0H

temp_5886_tl01
(12G025M22000LV with 12G025C2200WLV
co-lay symbol)

SMBus Slave Address: A0H

9,12 M_A_A[0..14]

M_A_DQ[0..63] 12

J0701A

M_A_A0 102 A0
M_A_A1 101 A1
M_A_A2 100 A2
M_A_A3 99 A3
M_A_A4 98 A4
M_A_A5 97 A5
M_A_A6 94 A6
M_A_A7 92 A7
M_A_A8 93 A8
M_A_A9 91 A9
M_A_A10 105 A10/AP
M_A_A11 90 A11
M_A_A12 89 A12
M_A_A13 116 A13
M_A_A14 86 A14
84 A15
9,12 M_A_BS2 85 A16_BA2
9,12 M_A_BS0 107 BA0
9,12 M_A_BS1 106 BA1
9,11 M_CS#0 110 S0#
9,11 M_CS#1 115 S1#
11 M_CLK_DDR0 30 CK0
11 M_CLK_DDR#0 32 CK0#
11 M_CLK_DDR1 164 CK1
11 M_CLK_DDR#1 166 CK1#
9,11 M_CKE0 79 CKE0
9,11 M_CKE1 80 CKE1
9,12 M_A_CAS# 113 CAS#
9,12 M_A_RAS# 108 RAS#
9,12 M_A_WE# 109 WE#
M_A_SA0 198 SA0
M_A_SA1 200 SA1
8,24,25,29 SMB_CLK_M 197 SCL
8,24,25,29 SMB_DAT_M 195 SDA
9,11 M_ODT0 114 ODT0
9,11 M_ODT1 119 ODT1
12 M_A_DM[0..7]
M_A_DM1 10 DM0
M_A_DM2 26 DM1
M_A_DM0 52 DM2
M_A_DM3 67 DM3
M_A_DM4 130 DM4
M_A_DM5 147 DM5
M_A_DM6 170 DM6
M_A_DM7 185 DM7
12 M_A_DQS[0..7]
M_A_DQS1 13 DQS0
M_A_DQS2 31 DQS1
M_A_DQS0 51 DQS2
M_A_DQS3 70 DQS3
M_A_DQS4 131 DQS4
M_A_DQS5 148 DQS5
M_A_DQS6 169 DQS6
M_A_DQS7 188 DQS7
12 M_A_DQS#[0..7]
M_A_DQS#1 11 DQS#0
M_A_DQS#2 29 DQS#1
M_A_DQS#0 49 DQS#2
M_A_DQS#3 68 DQS#3
M_A_DQS#4 129 DQS#4
M_A_DQS#5 146 DQS#5
M_A_DQS#6 167 DQS#6
M_A_DQS#7 186 DQS#7

DQ0 5 M_A_DQ8
DQ1 7 M_A_DQ9
DQ2 17 M_A_DQ15
DQ3 19 M_A_DQ10
DQ4 4 M_A_DQ12
DQ5 6 M_A_DQ13
DQ6 14 M_A_DQ11
DQ7 16 M_A_DQ14
DQ8 23 M_A_DQ20
DQ9 25 M_A_DQ17
DQ10 35 M_A_DQ22
DQ11 37 M_A_DQ18
DQ12 20 M_A_DQ21
DQ13 22 M_A_DQ19
DQ14 36 M_A_DQ23
DQ15 38 M_A_DQ16
DQ16 43 M_A_DQ6
DQ17 45 M_A_DQ2
DQ18 55 M_A_DQ1
DQ19 57 M_A_DQ5
DQ20 44 M_A_DQ3
DQ21 46 M_A_DQ7
DQ22 56 M_A_DQ0
DQ23 58 M_A_DQ4
DQ24 61 M_A_DQ29
DQ25 63 M_A_DQ25
DQ26 73 M_A_DQ26
DQ27 75 M_A_DQ31
DQ28 62 M_A_DQ24
DQ29 64 M_A_DQ28
DQ30 74 M_A_DQ30
DQ31 76 M_A_DQ27
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DQ47 154 M_A_DQ47
DQ48 157 M_A_DQ48
DQ49 159 M_A_DQ53
DQ50 173 M_A_DQ51
DQ51 175 M_A_DQ55
DQ52 158 M_A_DQ49
DQ53 160 M_A_DQ52
DQ54 174 M_A_DQ50
DQ55 176 M_A_DQ54
DQ56 179 M_A_DQ63
DQ57 181 M_A_DQ56
DQ58 189 M_A_DQ57
DQ59 191 M_A_DQ59
DQ60 180 M_A_DQ61
DQ61 182 M_A_DQ60
DQ62 192 M_A_DQ58
DQ63 194 M_A_DQ62

DDR2_DIMM_200P

M_CLK_DDR0
C0701 10PF/50V @
M_CLK_DDR#0
Place near SO-DIMM_0
M_CLK_DDR1
C0702 10PF/50V @
M_CLK_DDR#1

R0703 10KOhm
R0704 10KOhm

Layout Note: Place these caps near SO DIMM 0

Layout Note: Place these caps near SO DIMM 0

+1.8V
C0703 0.1UF/10V
C0704 0.1UF/10V
C0705 0.1UF/10V
C0706 0.1UF/10V
+3VS
C0707 2.2UF/6.3V
C0708 0.1UF/10V

J0701B

VDD1 112
VDD2 111
VDD3 117
VDD4 96
VDD5 95
VDD6 118
VDD7 81
VDD8 82
VDD9 87
VDD10 103
VDD11 88
VDD12 104
VDDSPD 199
NC1 83
NC2 120
NC3 50
NC4 69
NCTEST 163
VREF 1
GND0 201
GND1 202
NP_NC1 203
NP_NC2 204
VSS1 47
VSS2 133
VSS3 183
VSS4 77
VSS5 12
VSS6 48
VSS7 184
VSS8 78
VSS9 71
VSS10 72
VSS11 121
VSS12 122
VSS13 196
VSS14 193
VSS15 8
VSS16 18
VSS17 24
VSS18 41
VSS19 53
VSS20 42
VSS21 54
VSS22 59
VSS23 65
VSS24 60
VSS25 66
VSS26 127
VSS27 139
VSS28 128
VSS29 145
VSS30 165
VSS31 171
VSS32 172
VSS33 177
VSS34 187
VSS35 178
VSS36 190
VSS37 9
VSS38 21
VSS39 33
VSS40 155
VSS41 34
VSS42 132
VSS43 144
VSS44 156
VSS45 168
VSS46 2
VSS47 3
VSS48 15
VSS49 27
VSS50 39
VSS51 149
VSS52 161
VSS53 28
VSS54 40
VSS55 138
VSS56 150
VSS57 162

DDR2_DIMM_200P

11 PM_EXTTS#0
RX0702 0Ohm @
PM_EXTTS#0_R
M_VREF_MCH
C0709 2.2UF/6.3V
C0710 0.1UF/10V

VREF -> 10/10 mils

SO-DIMM 0 is placed nearer the GMCH than SO-DIMM 1

+1.8V
C0716 2.2UF/6.3V
C0717 2.2UF/6.3V
C0718 2.2UF/6.3V
C0719 2.2UF/6.3V

Layout Note: Place these Caps near SO DIMM 0

+1.8V
CE0701 220UF/4V @ +/-ESR=40mOhm/Ir=1900mA

PLACE NEAR SO-DIMM_0 / SO-DIMM_1

ASUS

Title DDR3 SO-DIMM_0

Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.0

Date: Monday, February 04, 2008 Sheet 7 of 94

+3VS → +3VS 3,7,11,14,15,20,22,23,24,25,29,30,31,37,40,41,45,46,48,50,51,53,54,57,58,59,61,91,92

+1.8V → +1.8V 7,9,11,13,83,91

M_VREF_MCH → M_VREF_MCH 7,9,11

temp_5886_tl02
(12G025032005LV with 12G025022004LV
CO-LAY symbol)

9,12 M_B_A[0..14]

M_B_DQ[0..63] 12

SMBus Slave Address:A4H

J0801A

M_B_A0 102 A0
M_B_A1 101 A1
M_B_A2 100 A2
M_B_A3 99 A3
M_B_A4 98 A4
M_B_A5 97 A5
M_B_A6 94 A6
M_B_A7 92 A7
M_B_A8 93 A8
M_B_A9 91 A9
M_B_A10 105 A10/AP
M_B_A11 90 A11
M_B_A12 89 A12
M_B_A13 116 A13
M_B_A14 86 A14
84 A15
85 A16_BA2

9,12 M_B_BS2

9,12 M_B_BS0 107 BA0
9,12 M_B_BS1 106 BA1
9,11 M_CS#2 110 S0#
9,11 M_CS#3 115 S1#
11 M_CLK_DDR2 30 CK0
11 M_CLK_DDR#2 32 CK0#
11 M_CLK_DDR3 164 CK1
11 M_CLK_DDR#3 166 CK1#
9,11 M_CKE2 79 CKE0
9,11 M_CKE3 80 CKE1
9,12 M_B_CAS# 113 CAS#
9,12 M_B_RAS# 108 RAS#
9,12 M_B_WE# 109 WE#
198 SA0
M_B_SA0 200 SA1
7,24,25,29 SMB_CLK_M 197 SCL
7,24,25,29 SMB_DAT_M 195 SDA

9,11 M_ODT2 114 ODT0
9,11 M_ODT3 119 ODT1

12 M_B_DM[0..7]

M_B_DM0 10 DM0
M_B_DM1 26 DM1
M_B_DM3 52 DM2
M_B_DM2 67 DM3
M_B_DM5 130 DM4
M_B_DM4 147 DM5
M_B_DM6 170 DM6
M_B_DM7 185 DM7

12 M_B_DQS[0..7]

M_B_DQS0 13 DQS0
M_B_DQS1 31 DQS1
M_B_DQS3 51 DQS2
M_B_DQS2 70 DQS3
M_B_DQS5 131 DQS4
M_B_DQS4 148 DQS5
M_B_DQS6 169 DQS6
M_B_DQS7 188 DQS7

12 M_B_DQS#[0..7]

M_B_DQS#0 11 DQS#0
M_B_DQS#1 29 DQS#1
M_B_DQS#3 49 DQS#2
M_B_DQS#2 68 DQS#3
M_B_DQS#5 129 DQS#4
M_B_DQS#4 146 DQS#5
M_B_DQS#6 167 DQS#6
M_B_DQS#7 186 DQS#7

DQ0 5 M_B_DQ5
DQ1 7 M_B_DQ4
DQ2 17 M_B_DQ1
DQ3 19 M_B_DQ7
DQ4 4 M_B_DQ0
DQ5 6 M_B_DQ6
DQ6 14 M_B_DQ3
DQ7 16 M_B_DQ2
DQ8 23 M_B_DQ9
DQ9 25 M_B_DQ8
DQ10 35 M_B_DQ15
DQ11 37 M_B_DQ14
DQ12 20 M_B_DQ13
DQ13 22 M_B_DQ12
DQ14 36 M_B_DQ10
DQ15 38 M_B_DQ11
DQ16 43 M_B_DQ24
DQ17 45 M_B_DQ25
DQ18 55 M_B_DQ26
DQ19 57 M_B_DQ27
DQ20 44 M_B_DQ28
DQ21 46 M_B_DQ29
DQ22 56 M_B_DQ30
DQ23 58 M_B_DQ31
DQ24 61 M_B_DQ22
DQ25 63 M_B_DQ23
DQ26 73 M_B_DQ21
DQ27 75 M_B_DQ19
DQ28 62 M_B_DQ16
DQ29 64 M_B_DQ18
DQ30 74 M_B_DQ17
DQ31 76 M_B_DQ20
DQ32 123 M_B_DQ44
DQ33 125 M_B_DQ41
DQ34 135 M_B_DQ43
DQ35 137 M_B_DQ46
DQ36 124 M_B_DQ40
DQ37 126 M_B_DQ45
DQ38 134 M_B_DQ42
DQ39 136 M_B_DQ47
DQ40 141 M_B_DQ36
DQ41 143 M_B_DQ33
DQ42 151 M_B_DQ38
DQ43 153 M_B_DQ35
DQ44 140 M_B_DQ32
DQ45 142 M_B_DQ34
DQ46 152 M_B_DQ39
DQ47 154 M_B_DQ37
DQ48 157 M_B_DQ48
DQ49 159 M_B_DQ53
DQ50 173 M_B_DQ55
DQ51 175 M_B_DQ49
DQ52 158 M_B_DQ52
DQ53 160 M_B_DQ54
DQ54 174 M_B_DQ50
DQ55 176 M_B_DQ51
DQ56 179 M_B_DQ61
DQ57 181 M_B_DQ60
DQ58 189 M_B_DQ63
DQ59 191 M_B_DQ57
DQ60 180 M_B_DQ56
DQ61 182 M_B_DQ59
DQ62 192 M_B_DQ58
DQ63 194 M_B_DQ62

DDR2_DIMM_200P

+3VS
R0803 10KOhm
R0804 1 2 10KOhm M_B_SA1

M_CLK_DDR3
C0801 10PF/50V @
M_CLK_DDR#3

M_CLK_DDR2
C0802 10PF/50V @
M_CLK_DDR#2

Place near SO-DIMM_1

+1.8V

Layout Note: Place these Caps near the SO-DIMM_1

C0816 2.2UF/6.3V
C0817 2.2UF/6.3V
C0818 2.2UF/6.3V
C0819 2.2UF/6.3V

+1.8V

Layout Note: Place these Caps near SO DIMM 1

C0807 0.1UF/10V
C0808 0.1UF/10V
C0809 0.1UF/10V
C0810 0.1UF/10V

+3VS
C0811 2.2UF/6.3V
C0812 0.1UF/10V

11 PM_EXTTS#1
RX0802 @ 0Ohm
PM_EXTTS#1_R

M_VREF_MCH
C0821 2.2UF/6.3V
C0820 0.1UF/10V

Layout Note: Place these Caps near SO DIMM 1

VREF -> 10/10 mils

J0801B

VDD1 112
VDD2 111
VDD3 117
VDD4 96
VDD5 95
VDD6 118
VDD7 81
VDD8 82
VDD9 87
VDD10 103
VDD11 88
VDD12 104
VDDSPD 199
NC1 83
NC2 120
NC3 50
NC4 69
NCTEST 163
VREF 1
GND0 201
GND1 202
NP_NC1 203
NP_NC2 204
VSS1 47
VSS2 133
VSS3 183
VSS4 77
VSS5 12
VSS6 48
VSS7 184
VSS8 78
VSS9 71
VSS10 72
VSS11 121
VSS12 122
VSS13 196
VSS14 193
VSS15 8
VSS16 18
VSS17 24
VSS18 41
VSS19 53
VSS20 42
VSS21 54
VSS22 59
VSS23 65
VSS24 60
VSS25 66
VSS26 127
VSS27 139
VSS28 128
VSS29 145
VSS30 165
VSS31 171
VSS32 172
VSS33 177
VSS34 187
VSS35 178
VSS36 190
VSS37 9
VSS38 21
VSS39 33
VSS40 155
VSS41 34
VSS42 132
VSS43 144
VSS44 156
VSS45 168
VSS46 2
VSS47 3
VSS48 15
VSS49 27
VSS50 39
VSS51 149
VSS52 161
VSS53 28
VSS54 40
VSS55 138
VSS56 150
VSS57 162

DDR2_DIMM_200P

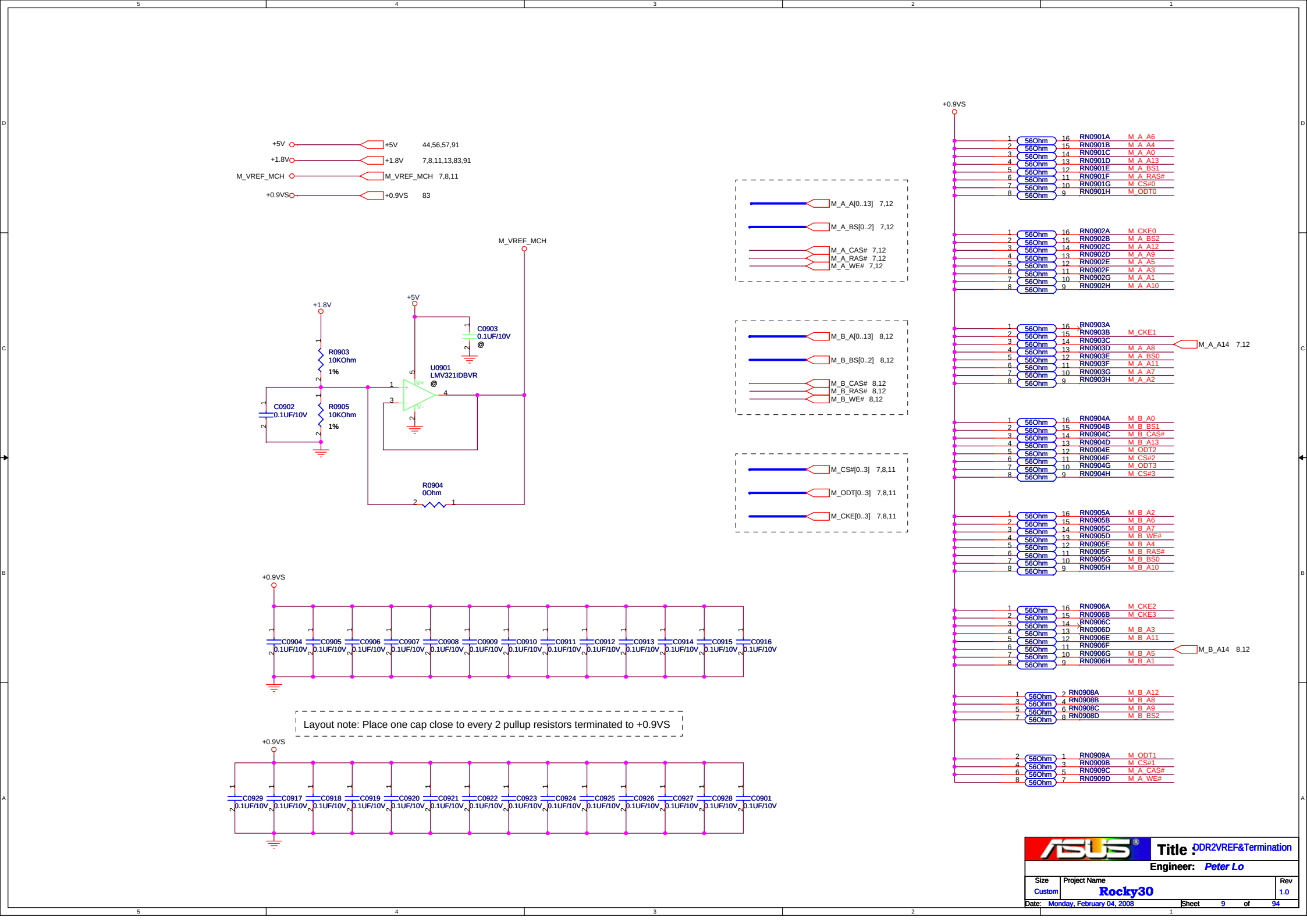
ASUS

Title :DDR3 SO-DIMM_1

Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.0

Date: Monday, February 04, 2008 Sheet 8 of 94


+5V +5V 44,56,57,91
+1.8V +1.8V 7,8,11,13,83,91
M_VREF_MCH M_VREF_MCH 7,8,11
+0.9VS +0.9VS 83
M_VREF_MCH
+1.8V
+5V
R0903 10KOhm 1%
C0903 0.1UF/10V @
U0901 LMV321IDBVR @
C0902 0.1UF/10V
R0905 10KOhm 1%
R0904 0Ohm
M_A_A[0..13] 7,12
M_A_BS[0..2] 7,12
M_A_CAS# 7,12
M_A_RAS# 7,12
M_A_WE# 7,12
M_B_A[0..13] 8,12
M_B_BS[0..2] 8,12
M_B_CAS# 8,12
M_B_RAS# 8,12
M_B_WE# 8,12
M_CS#[0..3] 7,8,11
M_ODT[0..3] 7,8,11
M_CKE[0..3] 7,8,11
+0.9VS
C0904 0.1UF/10V
C0905 0.1UF/10V
C0906 0.1UF/10V
C0907 0.1UF/10V
C0908 0.1UF/10V
C0909 0.1UF/10V
C0910 0.1UF/10V
C0911 0.1UF/10V
C0912 0.1UF/10V
C0913 0.1UF/10V
C0914 0.1UF/10V
C0915 0.1UF/10V
C0916 0.1UF/10V
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS
+0.9VS
C0929 0.1UF/10V
C0917 0.1UF/10V
C0918 0.1UF/10V
C0919 0.1UF/10V
C0920 0.1UF/10V
C0921 0.1UF/10V
C0922 0.1UF/10V
C0923 0.1UF/10V
C0924 0.1UF/10V
C0925 0.1UF/10V
C0926 0.1UF/10V
C0927 0.1UF/10V
C0928 0.1UF/10V
C0901 0.1UF/10V
+0.9VS
RN0901A M_A_A6
RN0901B M_A_A4
RN0901C M_A_A0
RN0901D M_A_A13
RN0901E M_A_BS1
RN0901F M_A_RAS#
RN0901G M_CS#0
RN0901H M_ODT0
RN0902A M_CKE0
RN0902B M_A_BS2
RN0902C M_A_A12
RN0902D M_A_A9
RN0902E M_A_A5
RN0902F M_A_A3
RN0902G M_A_A1
RN0902H M_A_A10
RN0903A
RN0903B M_CKE1
RN0903C M_A_A14 7,12
RN0903D M_A_A8
RN0903E M_A_BS0
RN0903F M_A_A11
RN0903G M_A_A7
RN0903H M_A_A2
RN0904A M_B_A0
RN0904B M_B_BS1
RN0904C M_B_CAS#
RN0904D M_B_A13
RN0904E M_ODT2
RN0904F M_CS#2
RN0904G M_ODT3
RN0904H M_CS#3
RN0905A M_B_A2
RN0905B M_B_A6
RN0905C M_B_A7
RN0905D M_B_WE#
RN0905E M_B_A4
RN0905F M_B_RAS#
RN0905G M_B_BS0
RN0905H M_B_A10
RN0906A M_CKE2
RN0906B M_CKE3
RN0906C
RN0906D M_B_A3
RN0906E M_B_A11
RN0906F M_B_A14 8,12
RN0906G M_B_A5
RN0906H M_B_A1
RN0908A M_B_A12
RN0908B M_B_A8
RN0908C M_B_A9
RN0908D M_B_BS2
RN0909A M_ODT1
RN0909B M_CS#1
RN0909C M_A_CAS#
RN0909D M_A_WE#
Title : DDR2VREF&Termination
Engineer: Peter Lo
Size Custom
Project Name Rocky30
Rev 1.0
Date: Monday, February 04, 2008
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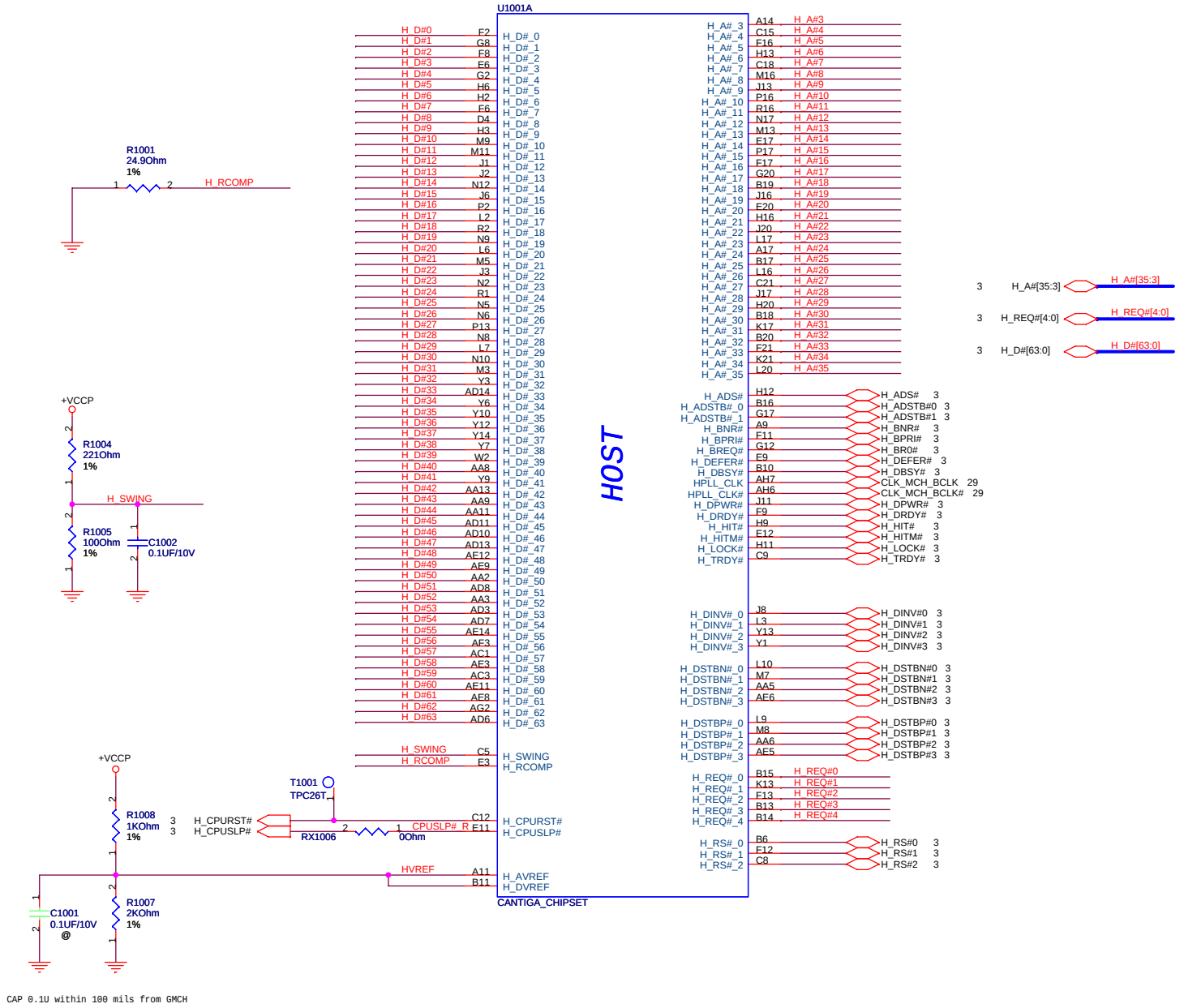


CAP 0.1U within 100 mils from GMCH

Title : Cantiga -- CPU (1)		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 10 of 94	

U1001B

RSVD
M36 RSVD1
N36 RSVD2
R33 RSVD3
T33 RSVD4
AH9 RSVD5
AH10 RSVD6
AH12 RSVD7
AH13 RSVD8
K12 RSVD9
AL34 RSVD10
AK34 RSVD11
AN35 RSVD12
AM35 RSVD13
T24 RSVD14
B31 RSVD15
AJ6 RSVD16
M1 RSVD17
AY21 RSVD20
A47 RSVD21
BG23 RSVD22
BF23 RSVD23
BH18 RSVD24
BF18 RSVD25

DDR CONTROL/COMPENSATION
SA_CK_0 AP24 M_CLK_DDR0 7
SA_CK_1 AT21 M_CLK_DDR1 7
SB_CK_0 AV24 M_CLK_DDR2 8
SB_CK_1 AU20 M_CLK_DDR3 8
SA_CK#_0 AR24 M_CLK_DDR#0 7
SA_CK#_1 AR21 M_CLK_DDR#1 7
SB_CK#_0 AU24 M_CLK_DDR#2 8
SB_CK#_1 AV20 M_CLK_DDR#3 8
SA_CKE_0 BC28 M_CKE0 7,9
SA_CKE_1 AY28 M_CKE1 7,9
SB_CKE_0 AY36 M_CKE2 8,9
SB_CKE_1 BB36 M_CKE3 8,9
SA_CS#_0 BA17 M_CS#0 7,9
SA_CS#_1 AY16 M_CS#1 7,9
SB_CS#_0 AV16 M_CS#2 8,9
SB_CS#_1 AR13 M_CS#3 8,9
SA_ODT_0 BD17 M_ODT0 7,9
SA_ODT_1 AY17 M_ODT1 7,9
SB_ODT_0 BF15 M_ODT2 8,9
SB_ODT_1 AY13 M_ODT3 8,9
SM_RCOMP BG22 M_RCOMP
SM_RCOMP# BH21 M_RCOMP# R1112 1% 80.6Ohm
SM_RCOMP_VOH BF28 SM_RCOMP_VOH
SM_RCOMP_VOL BH28 SM_RCOMP_VOL R1117 1% 80.6Ohm
SM_VREF AV42 M_VREF_MCH
SM_PWROK AR36
SM_REXT BF17 SM_REXT R1121 499Ohm 1% C1105 0.01UF/16V
SM_DRAMRST# BC36

CLK
DPLL_REF_CLK B38 CLK_DREF 29
DPLL_REF_CLK# A38 CLK_DREF# 29
DPLL_REF_SSCLK F41 CLK_DREFSS 29
DPLL_REF_SSCLK# F41 CLK_DREFSS# 29
PEG_CLK F43 CLK_MCH_3GPLL 29
PEG_CLK# E43 CLK_MCH_3GPLL# 29

DMI
DMI_RXN_0 AE41 DMI_TXN0 21
DMI_RXN_1 AE37 DMI_TXN1 21
DMI_RXN_2 AE47 DMI_TXN2 21
DMI_RXN_3 AH39 DMI_TXN3 21
DMI_RXP_0 AE40 DMI_TXP0 21
DMI_RXP_1 AE38 DMI_TXP1 21
DMI_RXP_2 AE48 DMI_TXP2 21
DMI_RXP_3 AH40 DMI_TXP3 21
DMI_TXN_0 AE35 DMI_RXN0 21
DMI_TXN_1 AE43 DMI_RXN1 21
DMI_TXN_2 AE46 DMI_RXN2 21
DMI_TXN_3 AH42 DMI_RXN3 21
DMI_TXP_0 AD35 DMI_RXP0 21
DMI_TXP_1 AE44 DMI_RXP1 21
DMI_TXP_2 AE46 DMI_RXP2 21
DMI_TXP_3 AH43 DMI_RXP3 21

CFG
29 MCH_BSEL0 T25 CFG_0
29 MCH_BSEL1 R25 CFG_1
29 MCH_BSEL2 P25 CFG_2
T1102 P20 CFG_3
T1101 P24 CFG_4
15 MCH_CFG_5 C25 CFG_5
15 MCH_CFG_6 N24 CFG_6
15 MCH_CFG_7 M24 CFG_7
T1115 F21 CFG_8
15 MCH_CFG_9 C23 CFG_9
15 MCH_CFG_10 C24 CFG_10
T1107 N21 CFG_11
P21 CFG_12
15 MCH_CFG_12 T21 CFG_13
15 MCH_CFG_13 T1103 R20 CFG_14
T1108 M20 CFG_15
15 MCH_CFG_16 L21 CFG_16
T1104 H21 CFG_17
T1109 P29 CFG_18
15 MCH_CFG_19 R28 CFG_19
15 MCH_CFG_20 T28 CFG_20

GRAPHICS VID
GFX_VID_0 B33 TP_GFX_VID0 T1110
GFX_VID_1 B32 TP_GFX_VID1 T1111
GFX_VID_2 G33 TP_GFX_VID2 T1112
GFX_VID_3 F33 TP_GFX_VID3 T1113
GFX_VID_4 E33 TP_GFX_VID4 T1114
GFX_VR_EN C34 TP_GFX_VREN T1106

PWR
22 PM_SYNC# RX1103 0Ohm R29 PM_SYNC#
3,20,80 H_DPRSTP# B7 PM_DPRSTP#
PM_EXTTS#0 N33 PM_EXT_TS#_0
PM_EXTTS#1 P32 PM_EXT_TS#_1
22,30 PM_PWROK RX1102 0Ohm AT40 PWROK
5,21,50 PLT_RST# AT11 RSTIN#
3,5,20,31 H_THRMTRIP# RX1101 100Ohm T20 THERMTRIP#
22,80 PM_DPRSLPVR RX1104 0Ohm R32 DPRSLPVR

ME
CL_CLK AH37 CL_CLK0 22
CL_DATA AH36 CL_DATA0 22
CL_PWROK AN36 RX1105 0Ohm PM_PWROK 22,30
CL_RST# AJ35 CL_RST#0 22
CL_VREF AH34 CL_VREF
C1106 0.1UF/10V
+VCCP
R1108 1KOhm 1%
R1102 499Ohm 1%

MISC
DDPC_CTRLCLK N28 T1121
DDPC_CTRLDATA M28 T1122
SDVO_CTRLCLK G36 SDVO_CTRLCLK 48
SDVO_CTRLDATA E36 SDVO_CTRLDATA 48
CLKREQ# K36 CLK_PEG_REQ# 29
ICH_SYNC# H36 MCH_ICH_SYNC# 22
TSATN# B12 T1117 R1126 56Ohm

HDA
HDA_BCLK B28 ACZ_BCLK_HDMI 20
HDA_RST# B30 ACZ_RST#_HDMI 20
HDA_SDI B29 ACZ_SDIN2_HDMI_R RX1107 33Ohm 1% ACZ_SDIN2_HDMI 20
HDA_SDO C29 ACZ_SDOUT_HDMI 20
HDA_SYNC A28 ACZ_SYNC_HDMI 20

NC
BG48 NC_1
BF48 NC_2
BD48 NC_3
BC48 NC_4
BH47 NC_5
BG47 NC_6
BE47 NC_7
BH46 NC_8
BF46 NC_9
BG45 NC_10
BH44 NC_11
BH43 NC_12
BH6 NC_13
BH5 NC_14
BC4 NC_15
BH3 NC_16
BF3 NC_17
BH2 NC_18
BG2 NC_19
BE2 NC_20
BG1 NC_21
BF1 NC_22
BD1 NC_23
BC1 NC_24
F1 NC_25

CANTIGA_CHIPSET

+1.8V
R1105 1KOhm 1%
SM_RCOMP_VOH
C1101 2.2UF/6.3V
C1102 0.01UF/16V
R1106 3.01KOhm 1%
SM_RCOMP_VOL
C1103 2.2UF/6.3V
C1104 0.01UF/16V
R1107 1KOhm 1%

T1123 ME_JTAG_TCK AL34
T1124 ME_JTAG_TDI AK34
T1125 ME_JTAG_TDO AN35
T1126 ME_JTAG_TMS AM35

+3VS
R1103 10KOhm PM_EXTTS#0 7
R1104 10KOhm PM_EXTTS#1 8

U1001C

L_BKLT_CTRL L32
L_BKLT_EN G32
L_CTRL_CLK M32
L_CTRL_DATA M33
L_DDC_CLK K33
L_DDC_DATA J33
L_VDD_EN M29
LVDS_IBG C44
LVDS_VBG B43
LVDS_VREFH E37
LVDS_VREFL E38
LVDSA_CLK# C41
LVDSA_CLK C40
LVDSB_CLK# B37
LVDSB_CLK A37
LVDSA_DATA#_0 H47
LVDSA_DATA#_1 E46
LVDSA_DATA#_2 G40
LVDSA_DATA#_3 A40
LVDSA_DATA_0 H48
LVDSA_DATA_1 D45
LVDSA_DATA_2 F40
LVDSA_DATA_3 B40
LVDSB_DATA#_0 A41
LVDSB_DATA#_1 H38
LVDSB_DATA#_2 G37
LVDSB_DATA#_3 J37
LVDSB_DATA_0 B42
LVDSB_DATA_1 G38
LVDSB_DATA_2 F37
LVDSB_DATA_3 K37

LVDS

T1127 L_BKLT_CTRL
46 LCD_BACKEN T1119 L_CTRL_CLK
T1120 L_CTRL_DATA
46 EDID_CLK
46 EDID_DAT
+3VS 2.2KOhm RN1125A 2.2KOhm RN1125B
46 LCD_VDD_EN R1110 2.37KOhm 1% 0Ohm R1123 @
46 LVDS_CLKN
46 LVDS_CLKP
46 LVDS_BCLKN
46 LVDS_BCLKP
46 LVDS_0N
46 LVDS_1N
46 LVDS_2N
46 LVDS_0P
46 LVDS_1P
46 LVDS_2P
46 LVDS_B0N
46 LVDS_B1N
46 LVDS_B2N
46 LVDS_B0P
46 LVDS_B1P
46 LVDS_B2P

TV
R1126 75Ohm 1%
R1111 75Ohm 1%
R1114 75Ohm 1%
TV_CVBS_J F25
TV_Y_J H25
TV_C_J K25
TVA_DAC
TVB_DAC
TVC_DAC
TV_RTN H24
TV_DCONSEL_0 C31
TV_DCONSEL_1 E32

VGA
CRT_BLUE_J E28
CRT_GREEN_J G28
CRT_RED_J J28
G29
CRT_IRTN H32
CRT_DDC_CLK J32
CRT_DDC_DATA J29
CRT_HSYNC E29
CRT_TVO_IREF L29
CRT_VSYNC
45 CRT_DDC_CLK
45 CRT_DDC_DAT
45 DAC_HSYNC RX1106 1% 33Ohm DAC_HSYNC_J
R1119 1% 1.02KOhm CRT_TVO_IREF_J
45 DAC_VSYNC RX1108 1% 33Ohm DAC_VSYNC_J

PCI-EXPRESS GRAPHICS

+VCCP
PEG_COMPI
PEG_COMPO
T37 PEGCOMP R1156 49.9Ohm 1%
T36

PEG_RX#_0 H44
PEG_RX#_1 J46
PEG_RX#_2 L44
PEG_RX#_3 L40
PEG_RX#_4 N41
PEG_RX#_5 P48
PEG_RX#_6 N44
PEG_RX#_7 T43
PEG_RX#_8 U43
PEG_RX#_9 Y43
PEG_RX#_10 Y48
PEG_RX#_11 Y36
PEG_RX#_12 AA43
PEG_RX#_13 AD37
PEG_RX#_14 AC47
PEG_RX#_15 AD39
PEG_RX_0 H43
PEG_RX_1 J44
PEG_RX_2 L43
PEG_RX_3 L41 HDMI_DETECT# 48
PEG_RX_4 N40
PEG_RX_5 P47
PEG_RX_6 N43
PEG_RX_7 T42 T1116
PEG_RX_8 U42
PEG_RX_9 Y42
PEG_RX_10 W47
PEG_RX_11 Y37
PEG_RX_12 AA42
PEG_RX_13 AD36
PEG_RX_14 AC48
PEG_RX_15 AD40

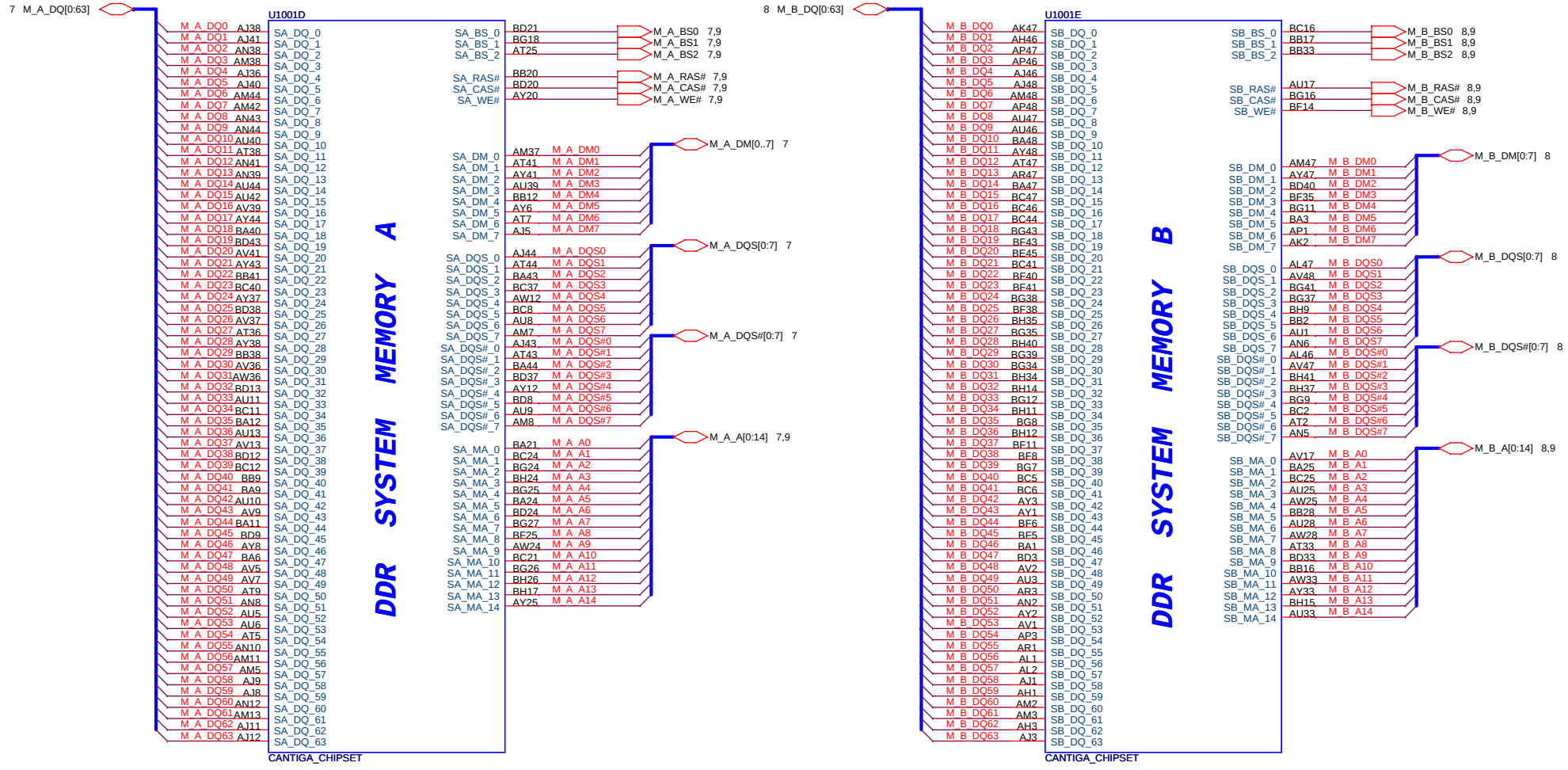
PEG_TX#_0 J41 TMDS_B_D2# CX1116 0.1UF/10V DVI_TX5-_C 48
PEG_TX#_1 M46 TMDS_B_D1# CX1114 0.1UF/10V DVI_TX4-_C 48
PEG_TX#_2 M47 TMDS_B_D0# CX1113 0.1UF/10V DVI_TX3-_C 48
PEG_TX#_3 M40 TMDS_B_CLK# CX1112 0.1UF/10V DVI_CLKB-_C 48
PEG_TX#_4 M42
PEG_TX#_5 R48
PEG_TX#_6 N38
PEG_TX#_7 T40
PEG_TX#_8 U37
PEG_TX#_9 U40
PEG_TX#_10 Y40
PEG_TX#_11 AA46
PEG_TX#_12 AA37
PEG_TX#_13 AA40
PEG_TX#_14 AD43
PEG_TX#_15 AC46
PEG_TX_0 J42 TMDS_B_D2 CX1107 0.1UF/10V DVI_TX5+_C 48
PEG_TX_1 L46 TMDS_B_D1 CX1106 0.1UF/10V DVI_TX4+_C 48
PEG_TX_2 M48 TMDS_B_D0 CX1115 0.1UF/10V DVI_TX3+_C 48
PEG_TX_3 M39 TMDS_B_CLK CX1104 0.1UF/10V DVI_CLKB+_C 48
PEG_TX_4 M43
PEG_TX_5 R47
PEG_TX_6 N37
PEG_TX_7 T39
PEG_TX_8 U36
PEG_TX_9 U39
PEG_TX_10 Y39
PEG_TX_11 Y46
PEG_TX_12 AA36
PEG_TX_13 AA39
PEG_TX_14 AD42
PEG_TX_15 AD46

CANTIGA_CHIPSET

45 DAC_B JP1101 SHORT_PIN CRT_BLUE_J
45 DAC_G JP1102 SHORT_PIN CRT_GREEN_J
45 DAC_R JP1103 SHORT_PIN CRT_RED_J
R1118 150Ohm 1%
R1120 150Ohm 1%
R1115 150Ohm 1%

ASUS

Title : Cantiga-DDR2/PEG(2)
Engineer: Peter Lo
Size: Custom
Project Name: Rocky30
Rev: 1.0
Date: Monday, February 04, 2008
Sheet 11 of 94



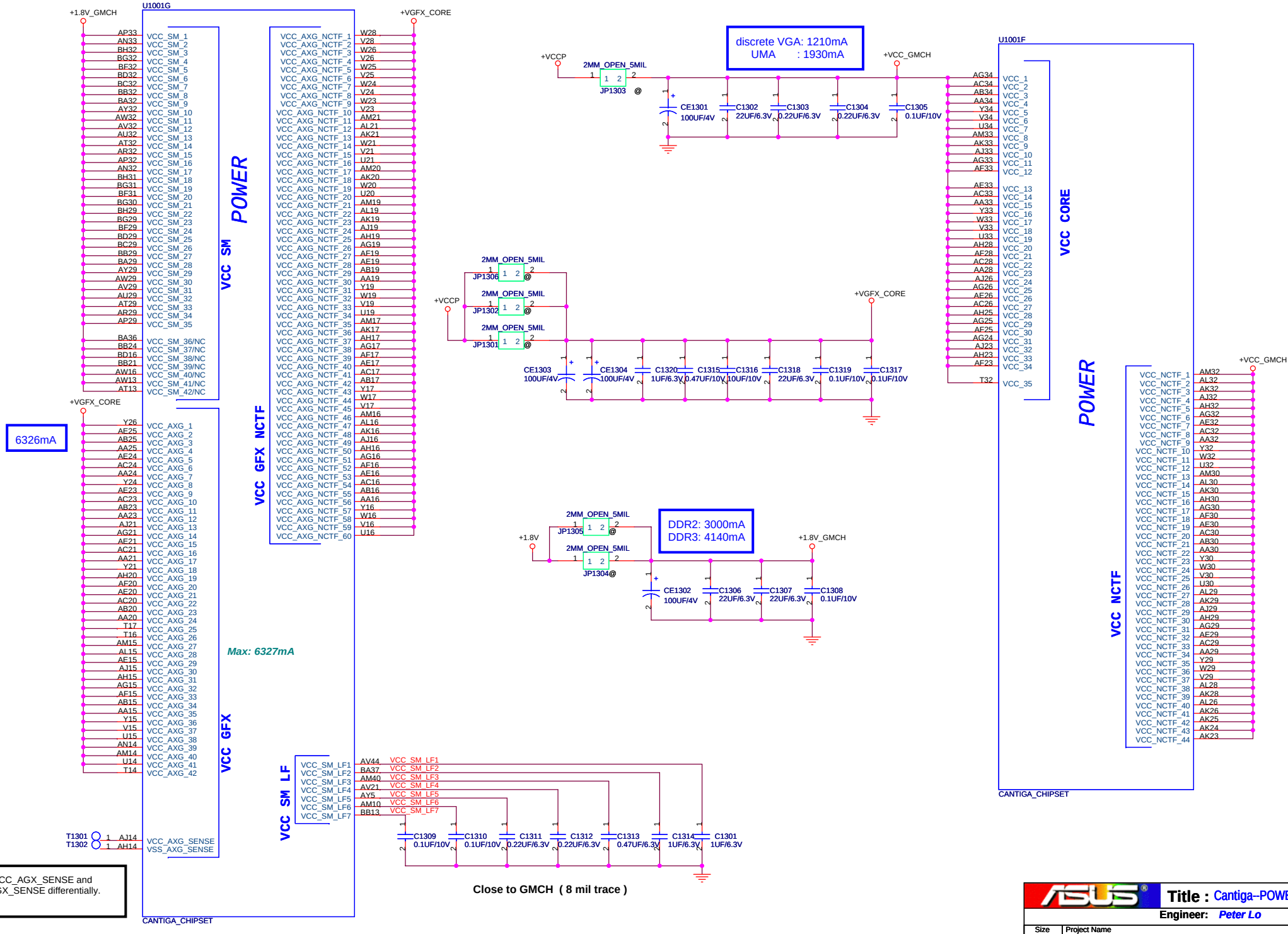
ASUS

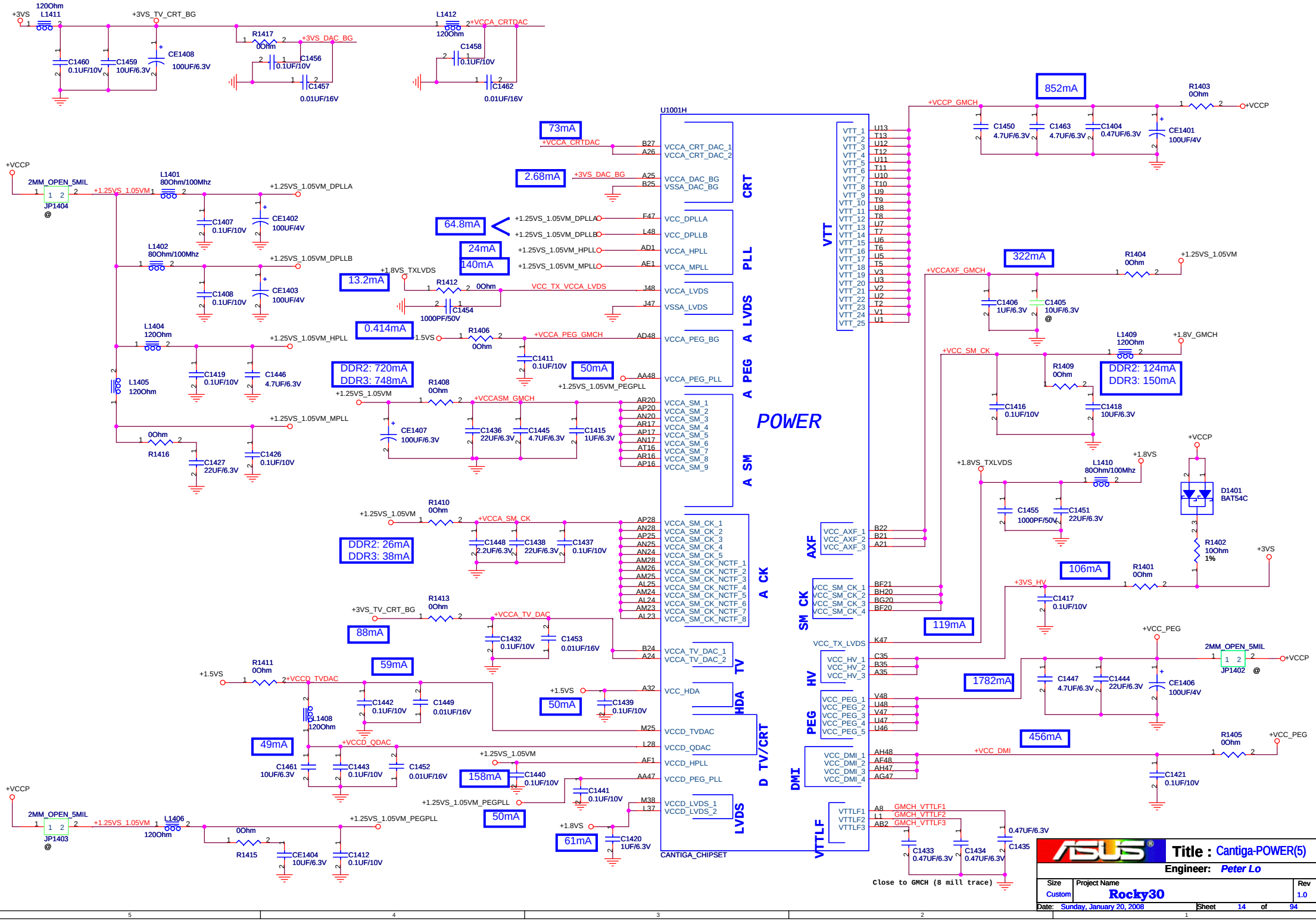
Title : Cantiga--DDR2 (3)

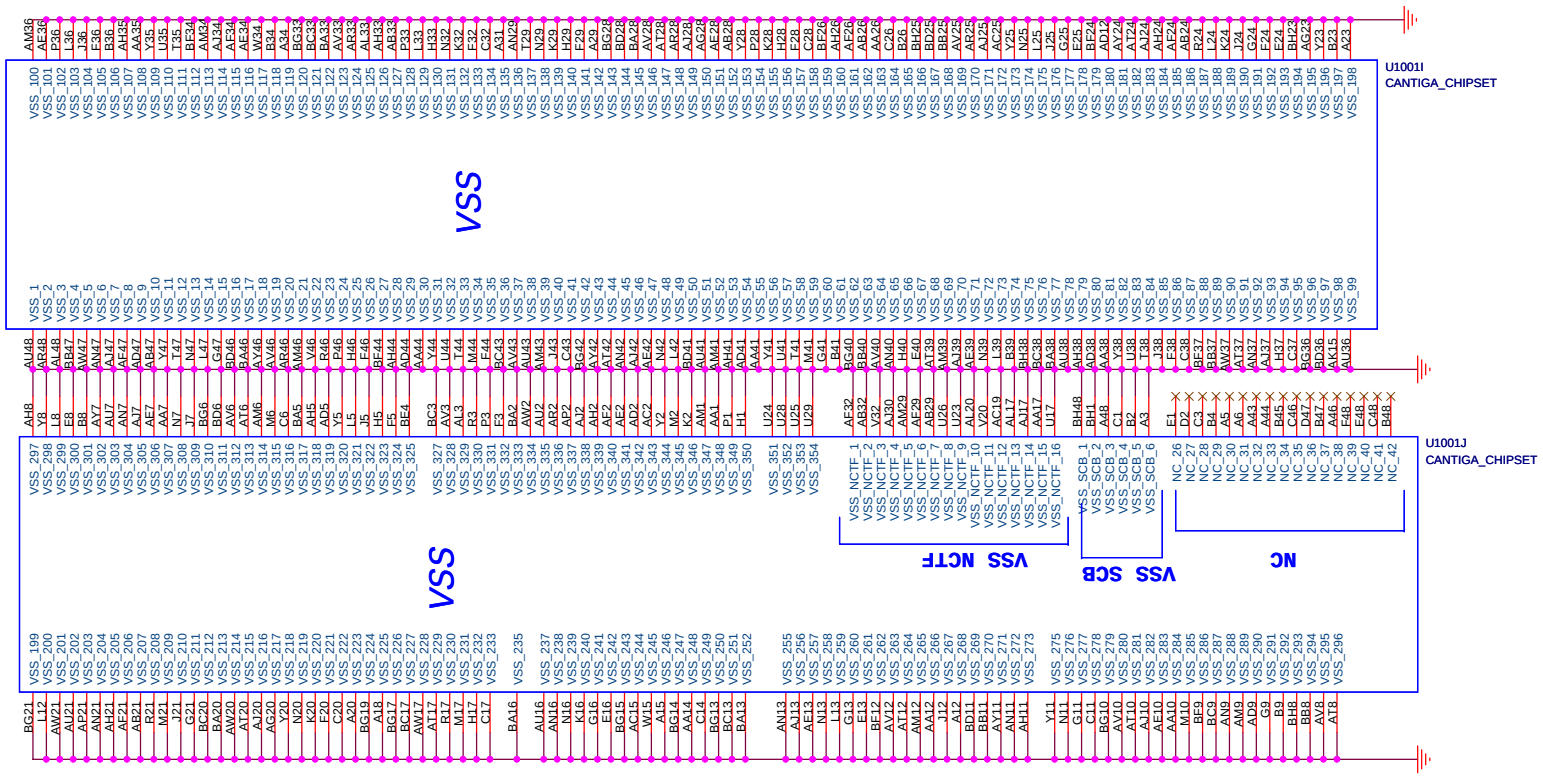
Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.0

Date: Monday, February 04, 2008 Sheet 12 of 94


U1001G
+1.8V_GMCH
+VGFX_CORE
VCC_SM_1
VCC_SM_2
VCC_SM_3
VCC_SM_4
VCC_SM_5
VCC_SM_6
VCC_SM_7
VCC_SM_8
VCC_SM_9
VCC_SM_10
VCC_SM_11
VCC_SM_12
VCC_SM_13
VCC_SM_14
VCC_SM_15
VCC_SM_16
VCC_SM_17
VCC_SM_18
VCC_SM_19
VCC_SM_20
VCC_SM_21
VCC_SM_22
VCC_SM_23
VCC_SM_24
VCC_SM_25
VCC_SM_26
VCC_SM_27
VCC_SM_28
VCC_SM_29
VCC_SM_30
VCC_SM_31
VCC_SM_32
VCC_SM_33
VCC_SM_34
VCC_SM_35
VCC_SM_36/NC
VCC_SM_37/NC
VCC_SM_38/NC
VCC_SM_39/NC
VCC_SM_40/NC
VCC_SM_41/NC
VCC_SM_42/NC
VCC SM
POWER
VCC_AXG_NCTF_1
VCC_AXG_NCTF_2
VCC_AXG_NCTF_3
VCC_AXG_NCTF_4
VCC_AXG_NCTF_5
VCC_AXG_NCTF_6
VCC_AXG_NCTF_7
VCC_AXG_NCTF_8
VCC_AXG_NCTF_9
VCC_AXG_NCTF_10
VCC_AXG_NCTF_11
VCC_AXG_NCTF_12
VCC_AXG_NCTF_13
VCC_AXG_NCTF_14
VCC_AXG_NCTF_15
VCC_AXG_NCTF_16
VCC_AXG_NCTF_17
VCC_AXG_NCTF_18
VCC_AXG_NCTF_19
VCC_AXG_NCTF_20
VCC_AXG_NCTF_21
VCC_AXG_NCTF_22
VCC_AXG_NCTF_23
VCC_AXG_NCTF_24
VCC_AXG_NCTF_25
VCC_AXG_NCTF_26
VCC_AXG_NCTF_27
VCC_AXG_NCTF_28
VCC_AXG_NCTF_29
VCC_AXG_NCTF_30
VCC_AXG_NCTF_31
VCC_AXG_NCTF_32
VCC_AXG_NCTF_33
VCC_AXG_NCTF_34
VCC_AXG_NCTF_35
VCC_AXG_NCTF_36
VCC_AXG_NCTF_37
VCC_AXG_NCTF_38
VCC_AXG_NCTF_39
VCC_AXG_NCTF_40
VCC_AXG_NCTF_41
VCC_AXG_NCTF_42
VCC_AXG_NCTF_43
VCC_AXG_NCTF_44
VCC_AXG_NCTF_45
VCC_AXG_NCTF_46
VCC_AXG_NCTF_47
VCC_AXG_NCTF_48
VCC_AXG_NCTF_49
VCC_AXG_NCTF_50
VCC_AXG_NCTF_51
VCC_AXG_NCTF_52
VCC_AXG_NCTF_53
VCC_AXG_NCTF_54
VCC_AXG_NCTF_55
VCC_AXG_NCTF_56
VCC_AXG_NCTF_57
VCC_AXG_NCTF_58
VCC_AXG_NCTF_59
VCC_AXG_NCTF_60
VCC GFX NCTF
6326mA
VCC_AXG_1
VCC_AXG_2
VCC_AXG_3
VCC_AXG_4
VCC_AXG_5
VCC_AXG_6
VCC_AXG_7
VCC_AXG_8
VCC_AXG_9
VCC_AXG_10
VCC_AXG_11
VCC_AXG_12
VCC_AXG_13
VCC_AXG_14
VCC_AXG_15
VCC_AXG_16
VCC_AXG_17
VCC_AXG_18
VCC_AXG_19
VCC_AXG_20
VCC_AXG_21
VCC_AXG_22
VCC_AXG_23
VCC_AXG_24
VCC_AXG_25
VCC_AXG_26
VCC_AXG_27
VCC_AXG_28
VCC_AXG_29
VCC_AXG_30
VCC_AXG_31
VCC_AXG_32
VCC_AXG_33
VCC_AXG_34
VCC_AXG_35
VCC_AXG_36
VCC_AXG_37
VCC_AXG_38
VCC_AXG_39
VCC_AXG_40
VCC_AXG_41
VCC_AXG_42
VCC GFX
Max: 6327mA
T1301
T1302
VCC_AXG_SENSE
VSS_AXG_SENSE
Route VCC_AGX_SENSE and VSS_AGX_SENSE differentially.
CANTIGA_CHIPSET
VCC_SM_LF1
VCC_SM_LF2
VCC_SM_LF3
VCC_SM_LF4
VCC_SM_LF5
VCC_SM_LF6
VCC_SM_LF7
VCC SM LF
C1309 0.1UF/10V
C1310 0.1UF/10V
C1311 0.22UF/6.3V
C1312 0.22UF/6.3V
C1313 0.47UF/6.3V
C1314 1UF/6.3V
C1301 1UF/6.3V
Close to GMCH (8 mil trace)
discrete VGA: 1210mA
UMA : 1930mA
+VCCP
2MM_OPEN_5MIL
JP1303 @
CE1301 100UF/4V
C1302 22UF/6.3V
C1303 0.22UF/6.3V
C1304 0.22UF/6.3V
C1305 0.1UF/10V
+VCC_GMCH
JP1306 @
JP1302 @
JP1301 @
CE1303 100UF/4V
CE1304 100UF/4V
C1320 1UF/6.3V
C1315 0.47UF/10V
C1316 10UF/10V
C1318 22UF/6.3V
C1319 0.1UF/10V
C1317 0.1UF/10V
+VGFX_CORE
JP1305 @
JP1304@
+1.8V
DDR2: 3000mA
DDR3: 4140mA
+1.8V_GMCH
CE1302 100UF/4V
C1306 22UF/6.3V
C1307 22UF/6.3V
C1308 0.1UF/10V
U1001F
VCC_1
VCC_2
VCC_3
VCC_4
VCC_5
VCC_6
VCC_7
VCC_8
VCC_9
VCC_10
VCC_11
VCC_12
VCC_13
VCC_14
VCC_15
VCC_16
VCC_17
VCC_18
VCC_19
VCC_20
VCC_21
VCC_22
VCC_23
VCC_24
VCC_25
VCC_26
VCC_27
VCC_28
VCC_29
VCC_30
VCC_31
VCC_32
VCC_33
VCC_34
VCC_35
VCC CORE
POWER
VCC_NCTF_1
VCC_NCTF_2
VCC_NCTF_3
VCC_NCTF_4
VCC_NCTF_5
VCC_NCTF_6
VCC_NCTF_7
VCC_NCTF_8
VCC_NCTF_9
VCC_NCTF_10
VCC_NCTF_11
VCC_NCTF_12
VCC_NCTF_13
VCC_NCTF_14
VCC_NCTF_15
VCC_NCTF_16
VCC_NCTF_17
VCC_NCTF_18
VCC_NCTF_19
VCC_NCTF_20
VCC_NCTF_21
VCC_NCTF_22
VCC_NCTF_23
VCC_NCTF_24
VCC_NCTF_25
VCC_NCTF_26
VCC_NCTF_27
VCC_NCTF_28
VCC_NCTF_29
VCC_NCTF_30
VCC_NCTF_31
VCC_NCTF_32
VCC_NCTF_33
VCC_NCTF_34
VCC_NCTF_35
VCC_NCTF_36
VCC_NCTF_37
VCC_NCTF_38
VCC_NCTF_39
VCC_NCTF_40
VCC_NCTF_41
VCC_NCTF_42
VCC_NCTF_43
VCC_NCTF_44
VCC NCTF
CANTIGA_CHIPSET
Title : Cantiga--POWER (4)
Engineer: Peter Lo
Size Custom
Project Name Rocky30
Rev 1.0
Date: Sunday, January 20, 2008
Sheet 13 of 94


+3VS
L1411 120Ohm
+3VS_TV_CRT_BG
C1460 0.1UF/10V
C1459 10UF/6.3V
CE1408 100UF/6.3V
R1417 0Ohm
+3VS_DAC_BG
C1456 0.1UF/10V
C1457 0.01UF/16V
L1412 120Ohm
+VCCA_CRTDAC
C1458 0.1UF/10V
C1462 0.01UF/16V
U1001H
73mA
+VCCA_CRTDAC
B27
A26
VCCA_CRT_DAC_1
VCCA_CRT_DAC_2
2.68mA
+3VS_DAC_BG
A25
B25
VCCA_DAC_BG
VSSA_DAC_BG
CRT
64.8mA
24mA
140mA
+1.25VS_1.05VM_DPLLA
+1.25VS_1.05VM_DPLLB
+1.25VS_1.05VM_HPLL
+1.25VS_1.05VM_MPLL
F47
L48
AD1
AE1
VCC_DPLLA
VCC_DPLLB
VCCA_HPLL
VCCA_MPLL
PLL
13.2mA
+1.8VS_TXLVDS
R1412 0Ohm
VCC_TX_VCCA_LVDS
C1454 1000PF/50V
J48
J47
VCCA_LVDS
VSSA_LVDS
A LVDS
0.414mA
1.5VS
R1406 0Ohm
+VCCA_PEG_GMCH
C1411 0.1UF/10V
AD48
VCCA_PEG_BG
A PEG
DDR2: 720mA
DDR3: 748mA
50mA
+1.25VS_1.05VM_PEGPLL
AA48
VCCA_PEG_PLL
R1408 0Ohm
+1.25VS_1.05VM
+VCCASM_GMCH
CE1407 100UF/6.3V
C1436 22UF/6.3V
C1445 4.7UF/6.3V
C1415 1UF/6.3V
AR20
AP20
AN20
AR17
AP17
AN17
AT16
AR16
AP16
VCCA_SM_1
VCCA_SM_2
VCCA_SM_3
VCCA_SM_4
VCCA_SM_5
VCCA_SM_6
VCCA_SM_7
VCCA_SM_8
VCCA_SM_9
A SM
POWER
R1410 0Ohm
+1.25VS_1.05VM
+VCCA_SM_CK
DDR2: 26mA
DDR3: 38mA
C1448 2.2UF/6.3V
C1438 22UF/6.3V
C1437 0.1UF/10V
AP28
AN28
AP25
AN25
AN24
AM28
AM26
AM25
AL25
AM24
AL24
AM23
AL23
VCCA_SM_CK_1
VCCA_SM_CK_2
VCCA_SM_CK_3
VCCA_SM_CK_4
VCCA_SM_CK_5
VCCA_SM_CK_NCTF_1
VCCA_SM_CK_NCTF_2
VCCA_SM_CK_NCTF_3
VCCA_SM_CK_NCTF_4
VCCA_SM_CK_NCTF_5
VCCA_SM_CK_NCTF_6
VCCA_SM_CK_NCTF_7
VCCA_SM_CK_NCTF_8
A CK
R1413 0Ohm
+3VS_TV_CRT_BG
+VCCA_TV_DAC
88mA
C1432 0.1UF/10V
C1453 0.01UF/16V
B24
A24
VCCA_TV_DAC_1
VCCA_TV_DAC_2
TV
R1411 0Ohm
+1.5VS
+VCCD_TVDAC
59mA
C1442 0.1UF/10V
C1449 0.01UF/16V
L1408 120Ohm
50mA
+1.5VS
C1439 0.1UF/10V
A32
VCC_HDA
HDA
M25
VCCD_TVDAC
49mA
+VCCD_QDAC
C1461 10UF/6.3V
C1443 0.1UF/10V
C1452 0.01UF/16V
L28
VCCD_QDAC
+1.25VS_1.05VM
158mA
C1440 0.1UF/10V
AF1
VCCD_HPLL
AA47
VCCD_PEG_PLL
C1441 0.1UF/10V
+1.25VS_1.05VM_PEGPLL
50mA
M38
L37
VCCD_LVDS_1
VCCD_LVDS_2
D TV/CRT
LVDS
+1.8VS
61mA
C1420 1UF/6.3V
CANTIGA_CHIPSET
VTT
VTT_1
VTT_2
VTT_3
VTT_4
VTT_5
VTT_6
VTT_7
VTT_8
VTT_9
VTT_10
VTT_11
VTT_12
VTT_13
VTT_14
VTT_15
VTT_16
VTT_17
VTT_18
VTT_19
VTT_20
VTT_21
VTT_22
VTT_23
VTT_24
VTT_25
U13
T13
U12
T12
U11
T11
U10
T10
U9
T9
U8
T8
U7
T7
U6
T6
U5
T5
V3
U3
V2
U2
T2
V1
U1
AXF
VCC_AXF_1
VCC_AXF_2
VCC_AXF_3
B22
B21
A21
SM CK
VCC_SM_CK_1
VCC_SM_CK_2
VCC_SM_CK_3
VCC_SM_CK_4
BF21
BH20
BG20
BF20
VCC_TX_LVDS
K47
HV
VCC_HV_1
VCC_HV_2
VCC_HV_3
C35
B35
A35
PEG
VCC_PEG_1
VCC_PEG_2
VCC_PEG_3
VCC_PEG_4
VCC_PEG_5
V48
U48
V47
U47
U46
DMI
VCC_DMI_1
VCC_DMI_2
VCC_DMI_3
VCC_DMI_4
AH48
AF48
AH47
AG47
VTTLF
VTTLF1
VTTLF2
VTTLF3
A8
L1
AB2
GMCH_VTTLF1
GMCH_VTTLF2
GMCH_VTTLF3
0.47UF/6.3V
C1433 0.47UF/6.3V
C1434 0.47UF/6.3V
C1435
Close to GMCH (8 mill trace)
852mA
+VCCP_GMCH
R1403 0Ohm
+VCCP
C1450 4.7UF/6.3V
C1463 4.7UF/6.3V
C1404 0.47UF/6.3V
CE1401 100UF/4V
322mA
+VCCAXF_GMCH
R1404 0Ohm
+1.25VS_1.05VM
C1406 1UF/6.3V
C1405 10UF/6.3V
@
L1409 120Ohm
+1.8V_GMCH
+VCC_SM_CK
R1409 0Ohm
DDR2: 124mA
DDR3: 150mA
C1416 0.1UF/10V
C1418 10UF/6.3V
+VCCP
+1.8VS_TXLVDS
L1410 80Ohm/100Mhz
+1.8VS
D1401 BAT54C
C1455 1000PF/50V
C1451 22UF/6.3V
R1402 10Ohm 1%
+3VS
106mA
R1401 0Ohm
+3VS_HV
C1417 0.1UF/10V
119mA
+VCC_PEG
2MM_OPEN_5MIL
JP1402
@
+VCCP
1782mA
C1447 4.7UF/6.3V
C1444 22UF/6.3V
CE1406 100UF/4V
456mA
R1405 0Ohm
+VCC_PEG
+VCC_DMI
C1421 0.1UF/10V
+VCCP
2MM_OPEN_5MIL
JP1404
@
+1.25VS_1.05VM
L1401 80Ohm/100Mhz
+1.25VS_1.05VM_DPLLA
C1407 0.1UF/10V
CE1402 100UF/4V
L1402 80Ohm/100Mhz
+1.25VS_1.05VM_DPLLB
C1408 0.1UF/10V
CE1403 100UF/4V
L1404 120Ohm
+1.25VS_1.05VM_HPLL
L1405 120Ohm
C1419 0.1UF/10V
C1446 4.7UF/6.3V
+1.25VS_1.05VM_MPLL
0Ohm
R1416
C1427 22UF/6.3V
C1426 0.1UF/10V
+VCCP
2MM_OPEN_5MIL
JP1403
@
+1.25VS_1.05VM
L1406 120Ohm
0Ohm
R1415
CE1404 10UF/6.3V
C1412 0.1UF/10V
+1.25VS_1.05VM_PEGPLL
Title : Cantiga-POWER(5)
Engineer: Peter Lo
Size Custom
Project Name Rocky30
Rev 1.0
Date: Sunday, January 20, 2008
Sheet 14 of 94



11 MCH_CFG_5 — R1509 2.21KOhm @ 1%

CFG5 : DMI STRAP
HIGH = DMI X 4 (Default)
LOW = DMI X 2

11 MCH_CFG_6 — R1514 2.21KOhm @ 1%

CFG6 : Integrated TPM Host Interface
HIGH = iTPM disable (Default)
LOW = iTPM enable

11 MCH_CFG_7 — R1511 2.21KOhm @ 1%

CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite
HIGH = With confidentiality (Default)
LOW = Without confidentiality

11 MCH_CFG_9 — R1512 2.21KOhm @ 1%

CFG9 : PCIE GRAPHIC LANE
LOW = Reverse Lanes
HIGH = Normal Operation (Default)

11 MCH_CFG_16 — R1507 2.21KOhm @ 1%

CFG16 : FSB Dynamic ODT
HIGH = Ensable (Default)
LOW = Disable

11 MCH_CFG_10 — R1508 2.21KOhm @ 1%

CFG10 : PCIe Loopback
HIGH = Disable (Default)
LOW = Enable

11 MCH_CFG_12 — R1513 2.21KOhm @ 1%

11 MCH_CFG_13 — R1510 2.21KOhm @ 1%

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)

+3VS — R1503 4.02KOhm @ 1% — 11 MCH_CFG_19

CFG19 : DMI Lane Reversal
LOW = NORMAL (default)
HIGH = Reverse Lanes

+3VS — R1506 4.02KOhm @ 1% — 11 MCH_CFG_20

CFG20 : SDVO/PCIE CONCURRENT MODE
LOW = ONLY SDVO or PCIE is Operational (Default)
HIGH = SDVO and PCIE are operating simultaneously via the PEG port

Title : Cantiga-GND		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 15 of 94	

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 16 of 94

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 17 of 94

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

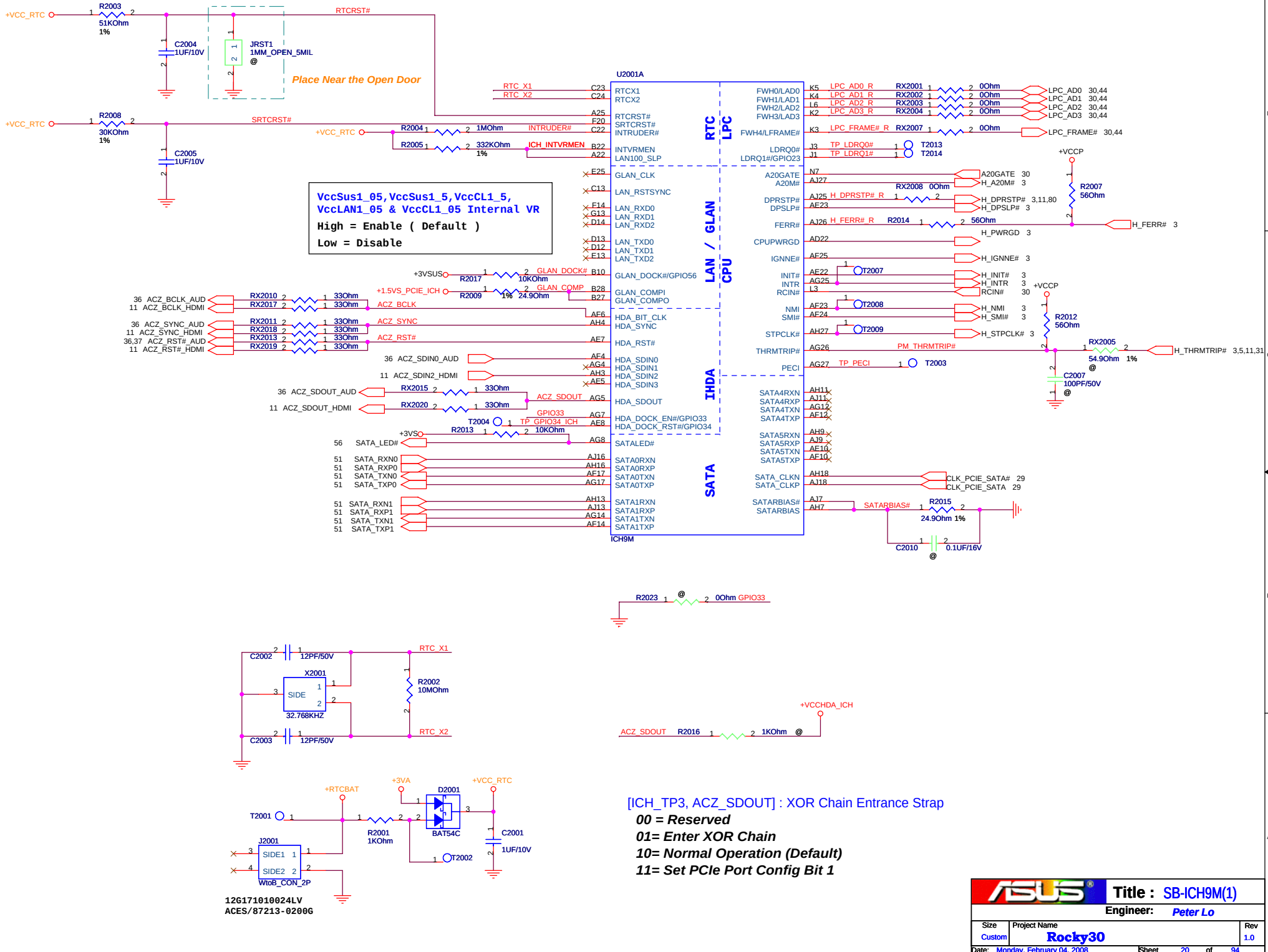
Date: Thursday, October 18, 2007 Sheet 18 of 94

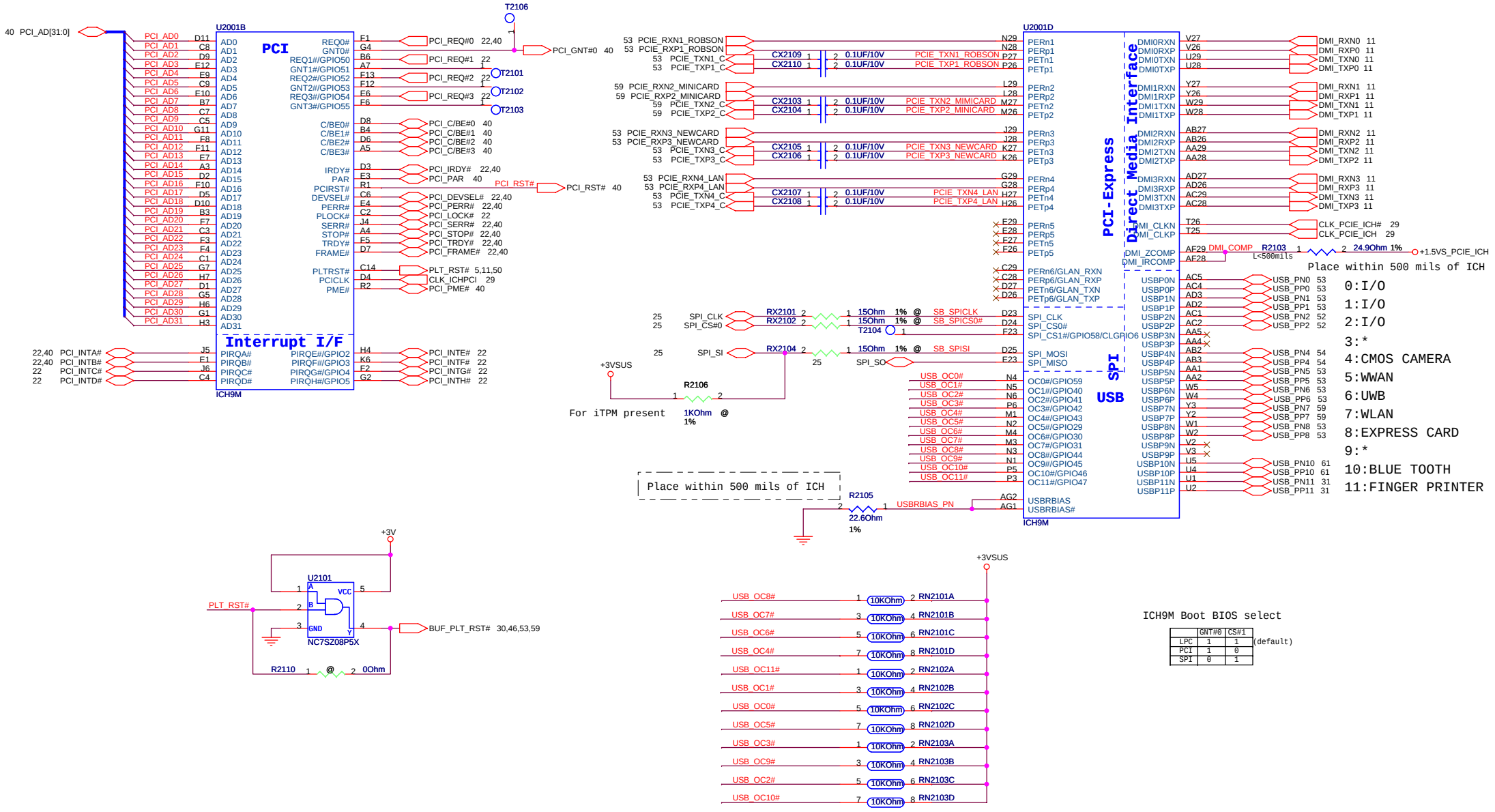
Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

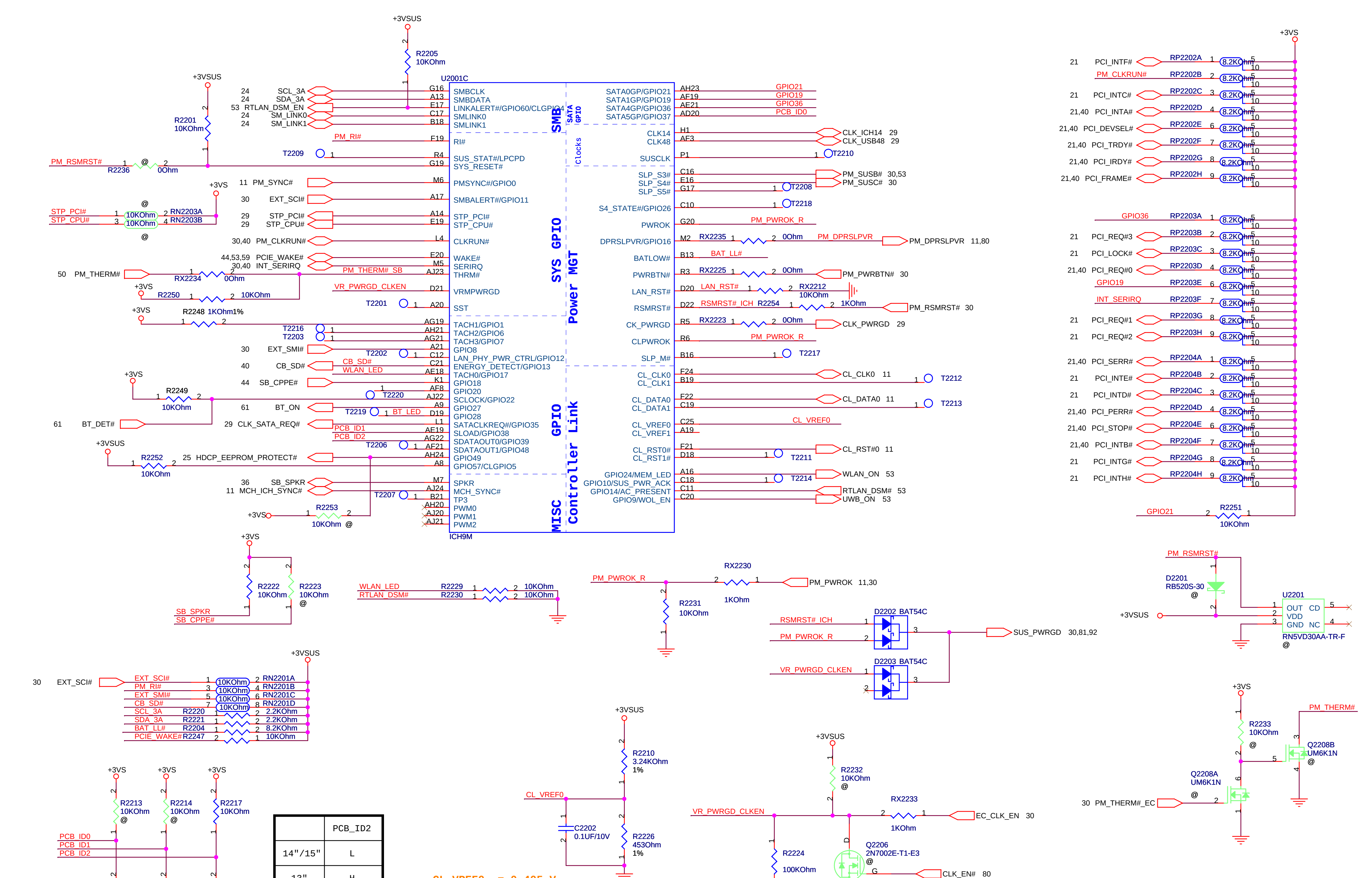
Date: Thursday, October 18, 2007 Sheet 19 of 94


R2003 51KOhm 1%
C2004 1UF/10V
JRST1 1MM_OPEN_5MIL @
Place Near the Open Door
RTCRST#
R2008 30KOhm 1%
C2005 1UF/10V
SRTCRST#
R2004 1MOhm
R2005 332KOhm 1%
INTRUDER#
ICH_INTVRMEN
VccSus1_05,VccSus1_5,VccCL1_5,
VccLAN1_05 & VccCL1_05 Internal VR
High = Enable (Default)
Low = Disable
U2001A
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
ICH9M
R2017 10KOhm
R2009 24.9Ohm 1%
GLAN_DOCK#
GLAN_COMP
ACZ_BCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDOUT
GPIO33
R2013 10KOhm
SATALED#
R2023 @ 0Ohm GPIO33
C2002 12PF/50V
X2001 32.768KHZ
C2003 12PF/50V
R2002 10MOhm
RTC_X1
RTC_X2
R2016 1KOhm @
+VCCHDA_ICH
+RTCBAT
+3VA
D2001 BAT54C
T2001
T2002
R2001 1KOhm
C2001 1UF/10V
J2001 WtoB_CON_2P
12G171010024LV
ACES/87213-0200G
[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap
00 = Reserved
01= Enter XOR Chain
10= Normal Operation (Default)
11= Set PCIe Port Config Bit 1
Title : SB-ICH9M(1)
Engineer: Peter Lo
Size Custom
Project Name Rocky30
Rev 1.0
Date: Monday, February 04, 2008
Sheet 20 of 94



	GNT#0	CS#1	
LPC	1	1	(default)
PCI	1	0	
SPI	0	1	

Title :	SB-ICH9M(2)		
Engineer:	Peter Lo		
Size: Custom	Project Name: Rocky30		Rev: 1.0
Date: Monday, February 04, 2008	Sheet 21 of 94		



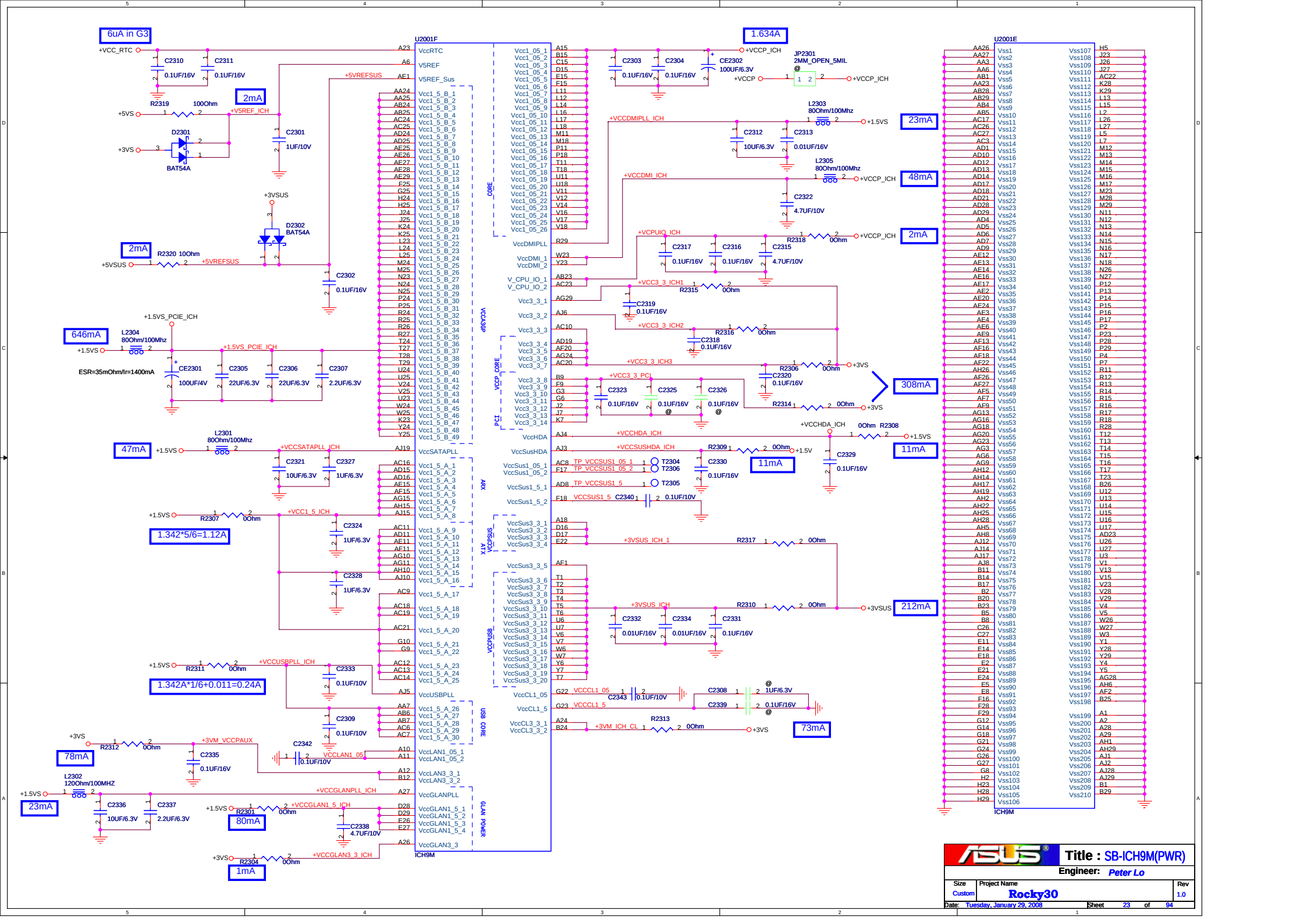
	PCB_ID2
14"/15"	L
13"	H

CL_VREF0 ~= 0.405 V

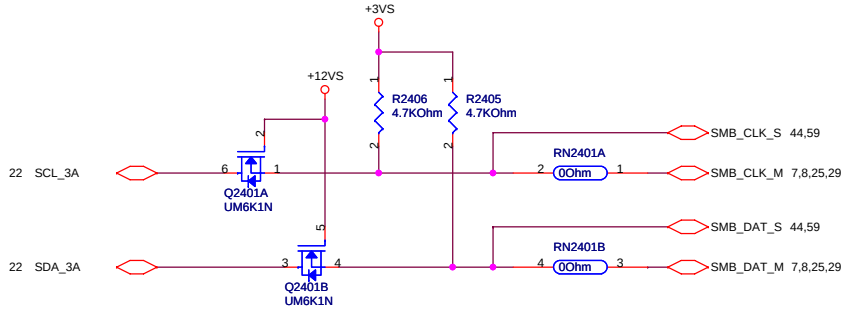
CL_VREF0 routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out: 5 mils on 5 mils for 300 mils max

ASUS

Title : SB-ICH9M(3)
Engineer: Peter Lo
Size: Custom
Project Name: Rocky30
Rev: 1.0
Date: Monday, February 04, 2008
Sheet 22 of 94


6uA in G3
2mA
2mA
646mA
47mA
1.342*5/6=1.12A
1.342A*1/6+0.011=0.24A
78mA
23mA
80mA
1mA
1.634A
23mA
48mA
2mA
308mA
11mA
212mA
73mA
U2001F
U2001E
ICH9M
Title : SB-ICH9M(PWR)
Engineer: Peter Lo
Size Custom
Project Name Rocky30
Rev 1.0
Date: Tuesday, January 29, 2008
Sheet 23 of 94

ICH9-M



ICH9M

NEWCARD,WLAN

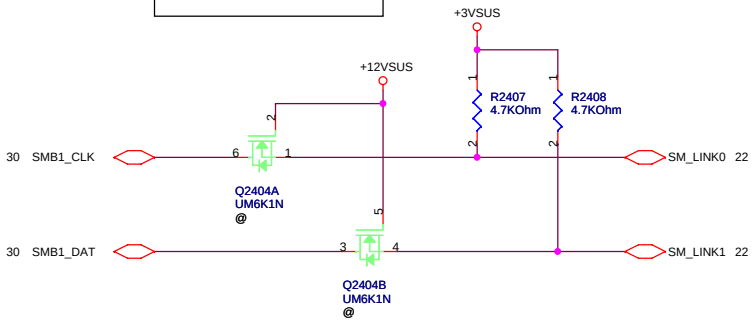
CLOCK GEN
SO-DIMM0 , SO-DIMM1

NEWCARD,WLAN

CLOCK GEN
SO-DIMM0 , SO-DIMM1

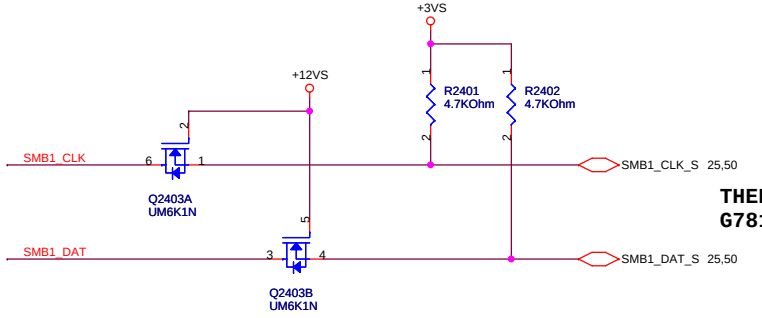
EC

Don't support iAMT
Remove ME-EC SMBus.



EC

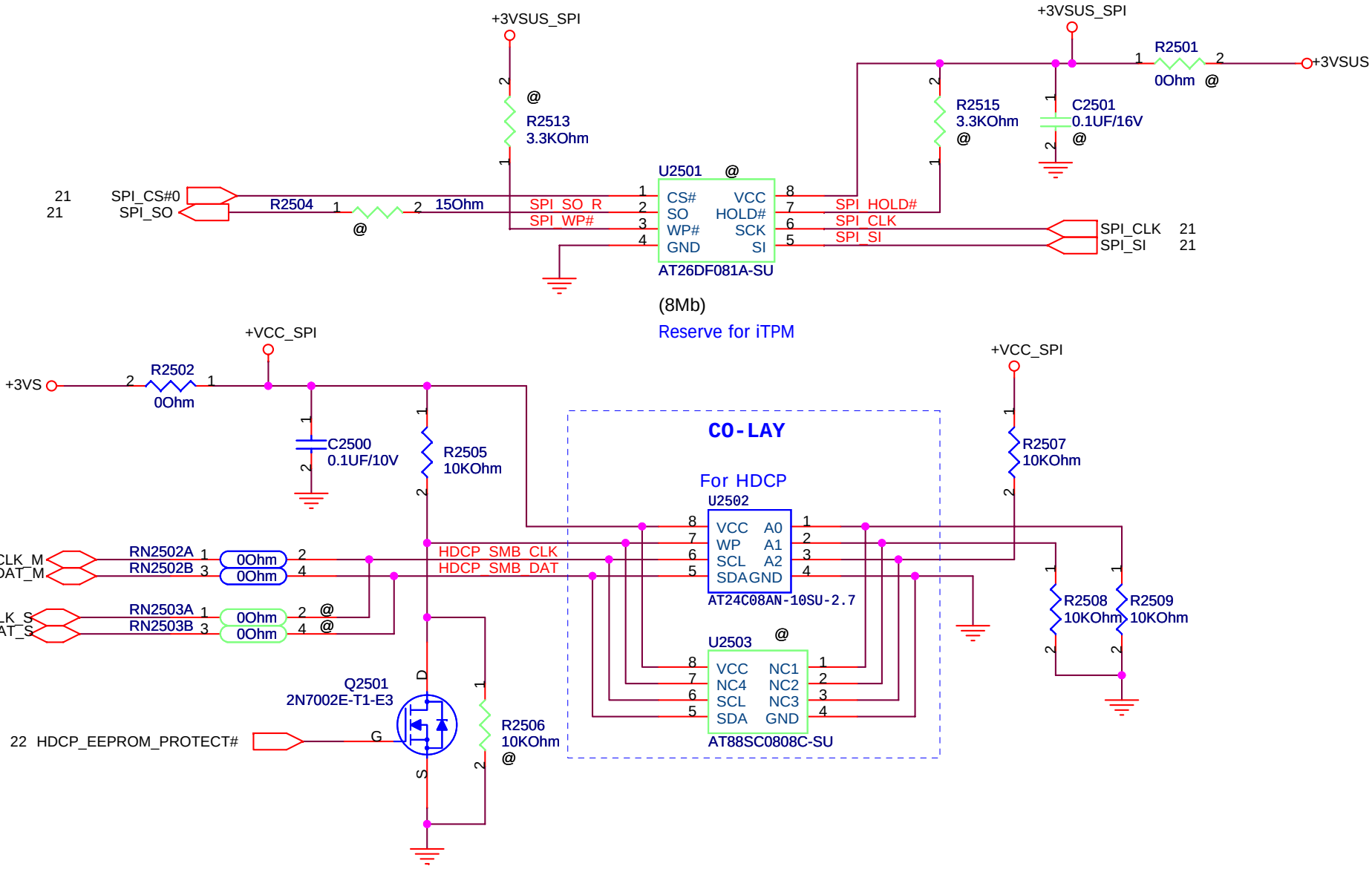
SB



EC

THERMAL IC
G781,G781-1

Title : ICH9M-Other		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 24 of 94	



U2502-AT24C08A :
Stuff : R2506 ; U2502 ; R2507 ; R2508 ; R2509
Nostuff : R2505

U2503-AT88SC0808C :
Stuff : U2503
Nostuff : R2505 ; R2506 ; R2507 ; R2508 ; R2509

ASUS	Title : SPI ROM	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 25 of 94	

Title :	
Engineer:	Peter Lo
Size: A	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
Sheet	26 of 94

Title :	
Engineer:	Peter Lo
Size: A	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
Sheet	27 of 94

Title :	
Engineer:	Peter Lo
Size: A	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
Sheet	28 of 94

+VCCP → +VCCP 5,10,11,13,14,20,23,80,82

+3VS → +3VS 3,7,8,11,14,15,20,22,23,24,25,30,31,37,40,41,45,46,48,50,51,53,54,57,58,59,61,91,92

U2901

ICS9LPRS365BGLFT

C2917,C2918,C2919 near CLK Gen.

CR#_A	0 = SRC 0 1 = SRC 2 SATA
CR#_B	0 = SRC 1 1 = SRC 4 MCH
CR#_C	0 = SRC 0 1 = SRC 2
CR#_D	0 = SRC 1 1 = SRC 4
CR#_E	SRC 6 WLAN
CR#_F	SRC 8 LAN
CR#_G	SRC 9 New Card
CR#_H	SRC 10 Robson

Latched Input Select

0 = SRC 8
1 = CPU_ITP CLK

Decide pin 46,47

ITP_EN — R2909 10KOhm

27_Select =0, pin#13/14=DOT96; pin#17/18=LCD_SST;

27_Select =1, pin#13/14=SRC0; pin#17/18=27MHz non-spread SE clock;

Decide pin 13/14,17/18

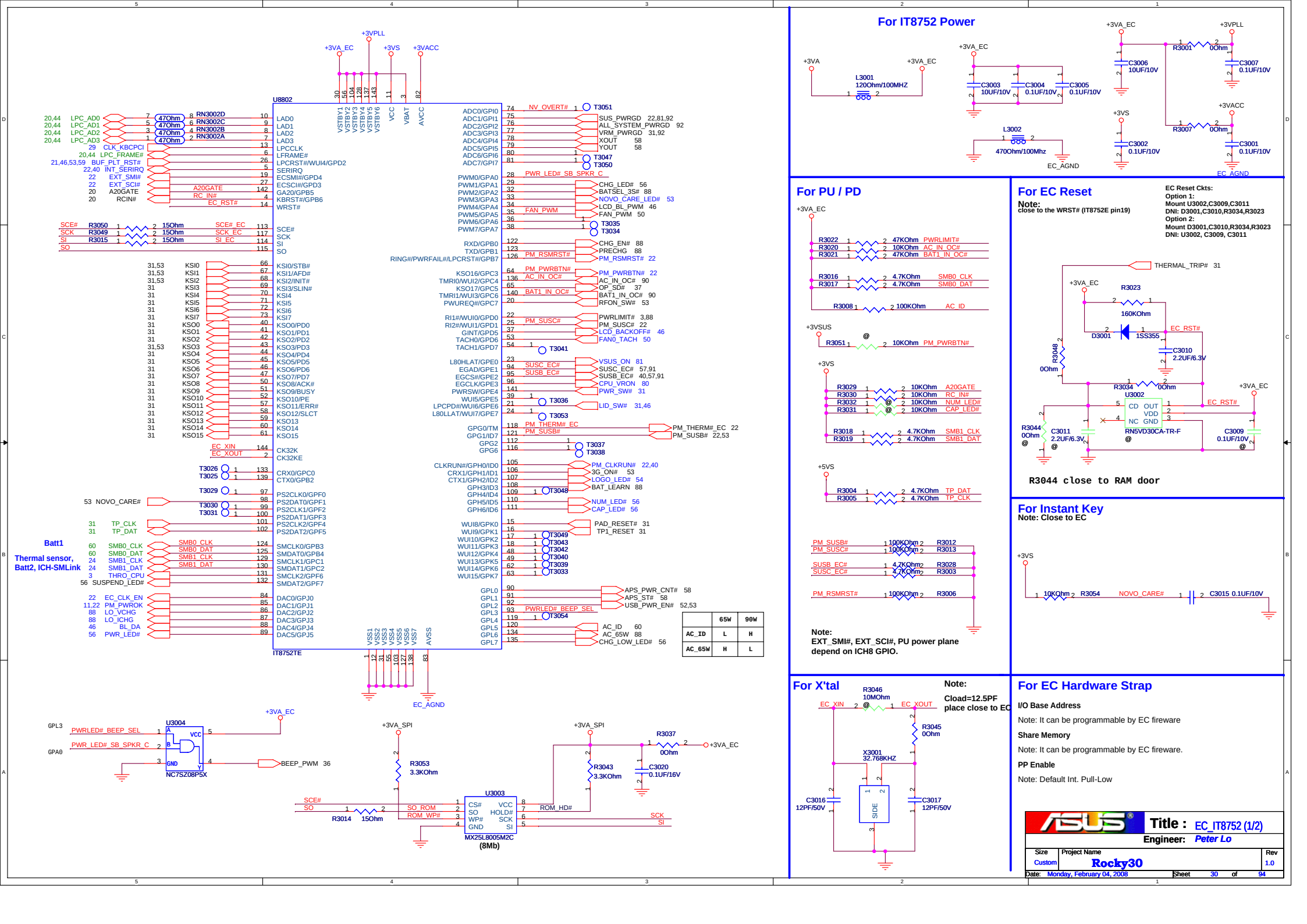
27_SEL — R2915 10KOhm @ / R2913 10KOhm

For GM/GL, need to PD for 96MHz output.
For PM, need to PU for 27MHz output.

C2921, C2922, C2923, C2924, C2925, C2926, C2927, C2928, C2929, C2930 near CLK Gen.

	FSLC	FSLB	FSLA
BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0

Title : ICS9LPR365
Engineer: Peter Lo
Size: Custom | Project Name: Rocky30 | Rev: 1.0
Date: Monday, February 04, 2008 | Sheet 29 of 94



For IT8752 Power

For PU / PD

Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH8 GPIO.

For EC Reset

Note:
close to the WRST# (IT8752E pin19)

EC Reset Ckts:
Option 1:
Mount U3002,C3009,C3011
DNI: D3001,C3010,R3034,R3023
Option 2:
Mount D3001,C3010,R3034,R3023
DNI: U3002, C3009, C3011

R3044 close to RAM door

For Instant Key

Note: Close to EC

For X'tal

Note:
Cload=12.5PF
place close to EC

For EC Hardware Strap

I/O Base Address

Note: It can be programmable by EC fireware

Share Memory

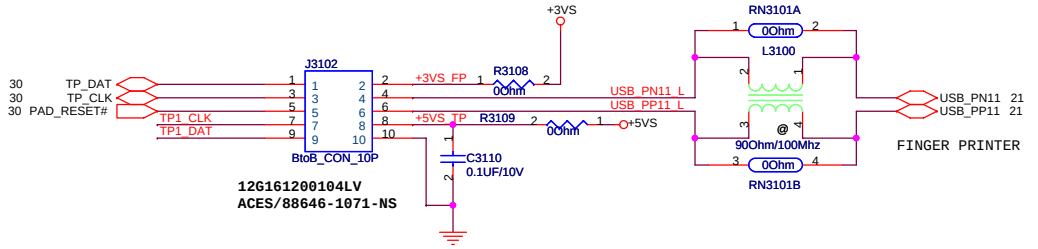
Note: It can be programmable by EC fireware.

PP Enable

Note: Default Int. Pull-Low

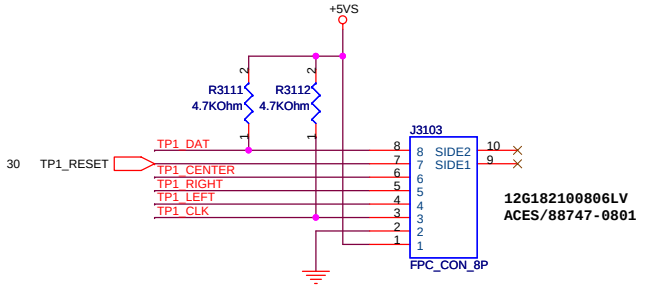
ASUS	Title :	EC_IT8752 (1/2)	
	Engineer:	Peter Lo	
Size: Custom	Project Name: Rocky30		Rev: 1.0
Date: Monday, February 04, 2008	Sheet 30 of 94		

TOUCH PAD CONN



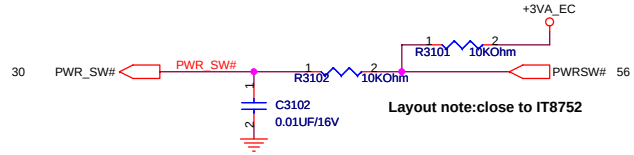
TP : Touch Pad
TP1: Track Point

TRACK POINT CONN

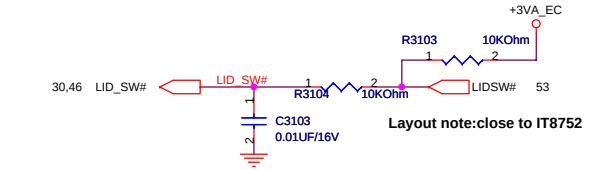


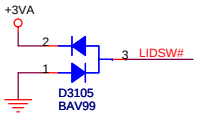
For Switch

PWR SWITCH



LID SWITCH

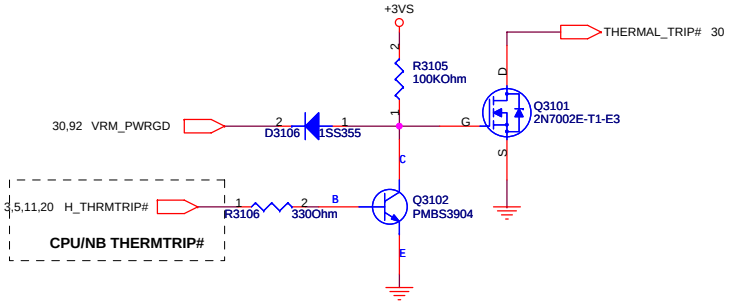




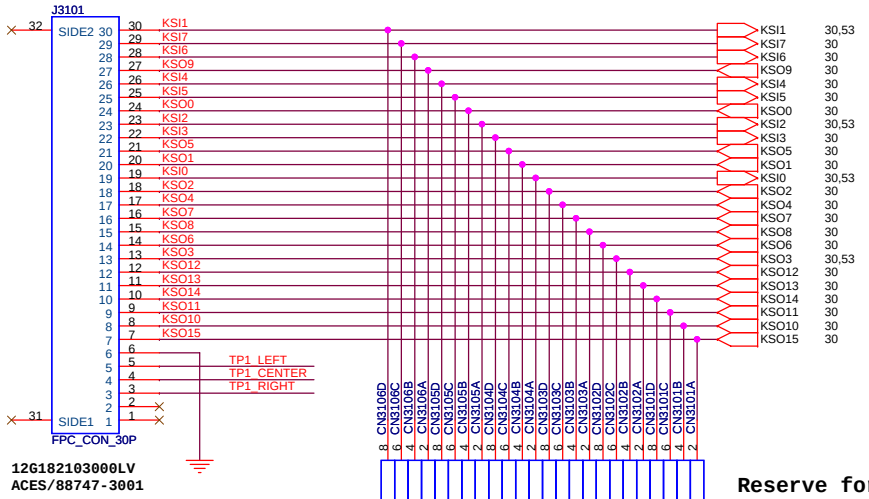
close to connector

Note:
LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.

For Thermal Control Method



Keyboard Connector

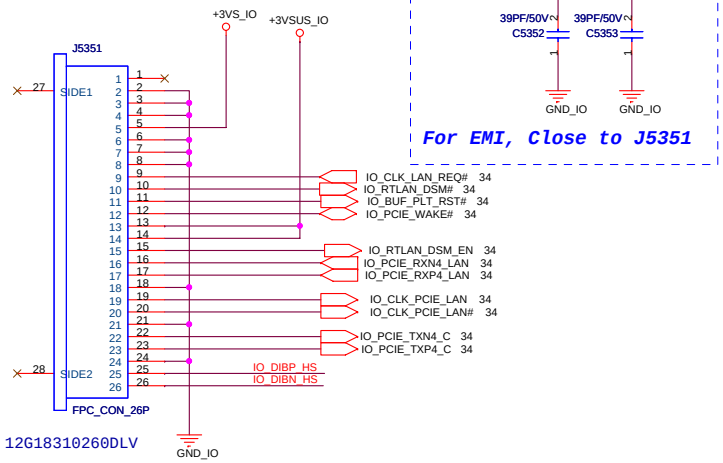


Reserve for WWAN

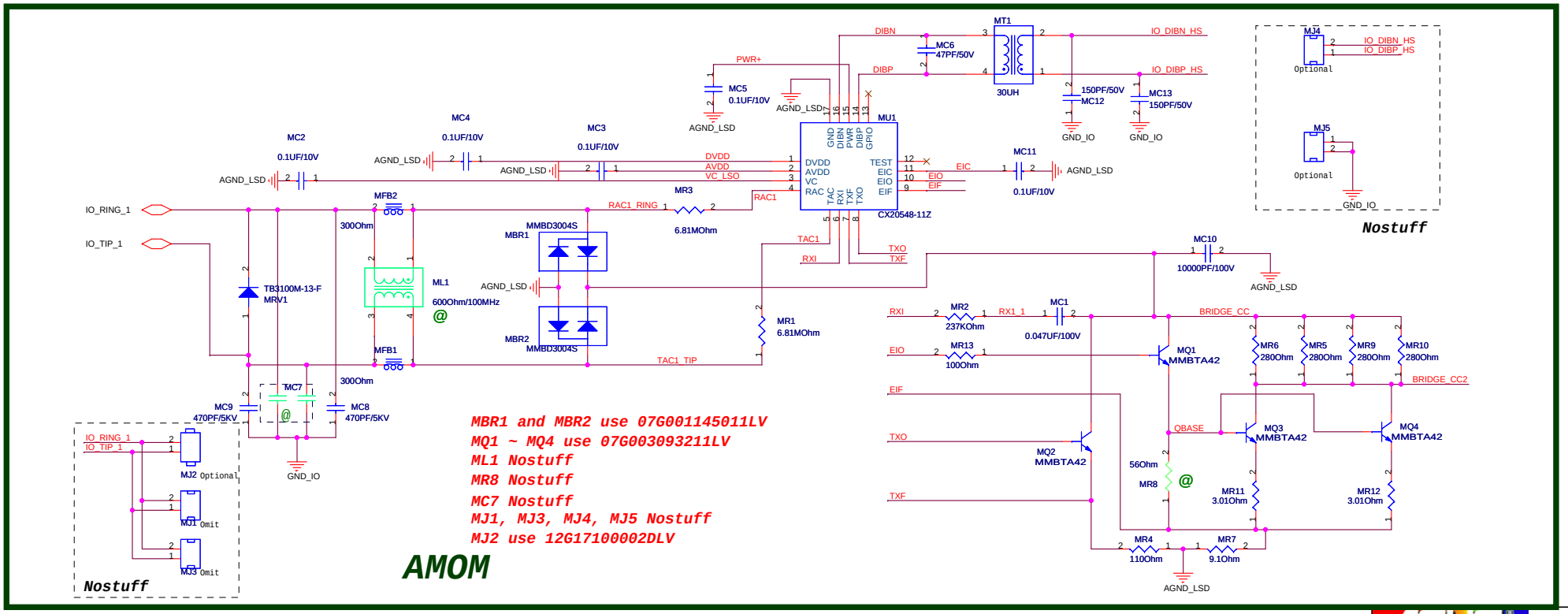
Title : EC_IT8752 (2/2)		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 31 of 94	

Title : *			
Engineer: Peter Lo			
Size: Custom	Project Name: Rocky30		Rev: 1.0
Date: Sunday, January 20, 2008	Sheet 32 of 94		

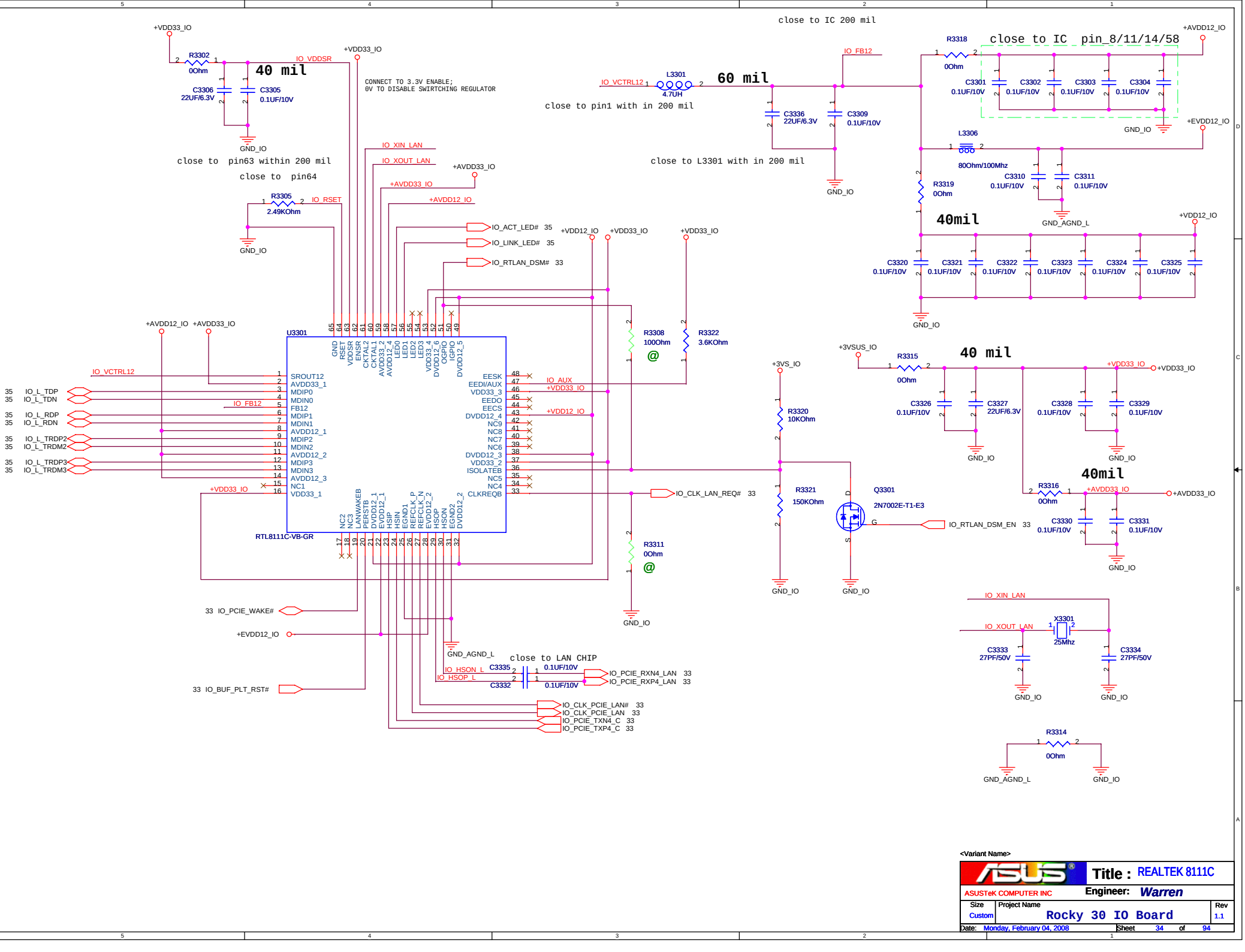
IO BOARD

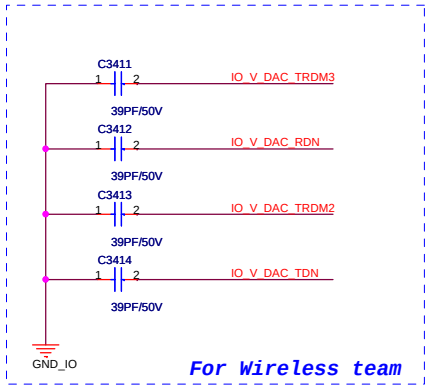


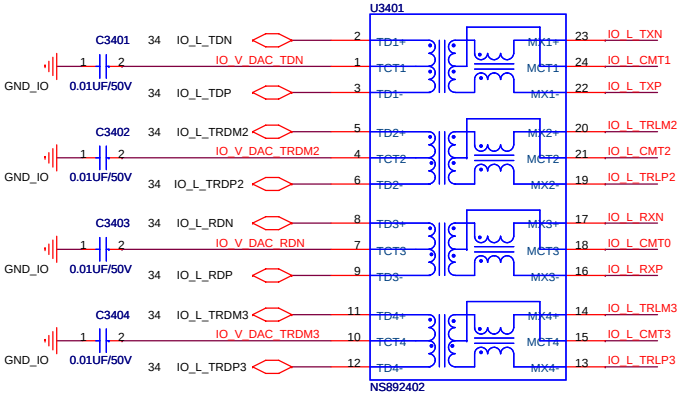
12G18310260DLV



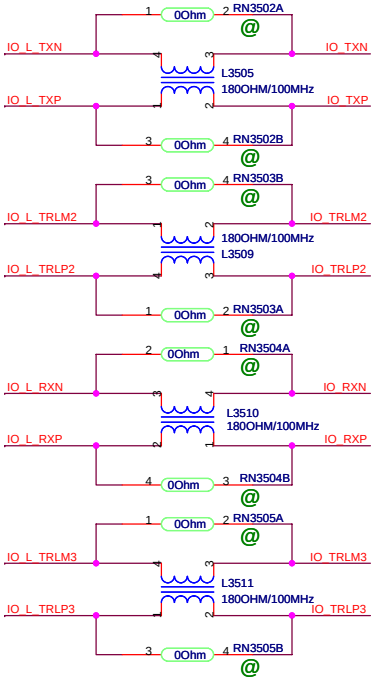
ASUSALPHA ODM NB1	Title : IO BRD CONN&DAA	
	Engineer: Warren	
Size: Custom	Project Name: Rocky 30 IO Board	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 33 of 94	

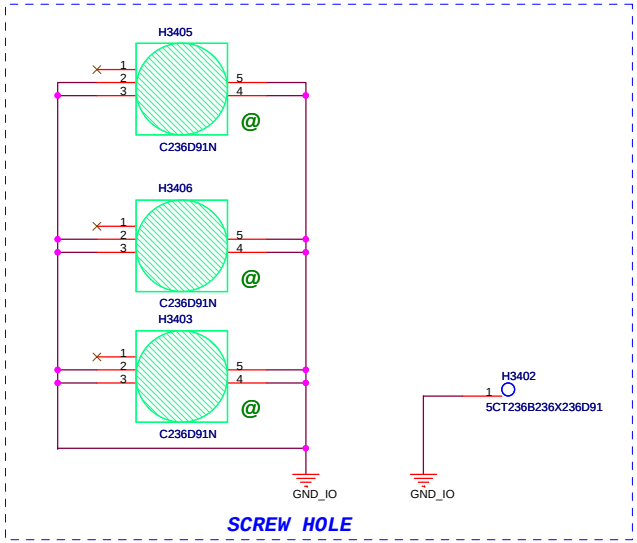

close to IC 200 mil
close to IC pin_8/11/14/58
close to pin1 with in 200 mil
close to L3301 with in 200 mil
close to pin63 within 200 mil
close to pin64
close to LAN CHIP
CONNECT TO 3.3V ENABLE;
0V TO DISABLE SWIRTCHING REGULATOR
40 mil
60 mil
40mil
RTL8111C-VB-GR
U3301
+VDD33_IO
+AVDD12_IO
+EVDD12_IO
+VDD12_IO
+3VS_IO
+3VSUS_IO
GND_IO
GND_AGND_L
IO_XIN_LAN
IO_XOUT_LAN
IO_FB12
IO_RSET
IO_VCTRL12
IO_AUX
IO_ACT_LED# 35
IO_LINK_LED# 35
IO_RTLAN_DSM# 33
IO_CLK_LAN_REQ# 33
IO_RTLAN_DSM_EN 33
33 IO_PCIE_WAKE#
33 IO_BUF_PLT_RST#
IO_HSON_L
IO_HSOP_L
IO_PCIE_RXN4_LAN 33
IO_PCIE_RXP4_LAN 33
IO_CLK_PCIE_LAN# 33
IO_CLK_PCIE_LAN 33
IO_PCIE_TXN4_C 33
IO_PCIE_TXP4_C 33
35 IO_L_TDP
35 IO_L_TDN
35 IO_L_RDP
35 IO_L_RDN
35 IO_L_TRDP2
35 IO_L_TRDM2
35 IO_L_TRDP3
35 IO_L_TRDM3
R3302 0Ohm
R3305 2.49KOhm
R3308 100Ohm @
R3322 3.6KOhm
R3320 10KOhm
R3321 150KOhm
R3311 0Ohm @
R3315 0Ohm
R3316 0Ohm
R3318 0Ohm
R3319 0Ohm
R3314 0Ohm
L3301 4.7UH
L3306 80Ohm/100Mhz
Q3301 2N7002E-T1-E3
X3301 25Mhz
C3306 22UF/6.3V
C3305 0.1UF/10V
C3335 0.1UF/10V
C3332 0.1UF/10V
C3336 22UF/6.3V
C3309 0.1UF/10V
C3301 0.1UF/10V
C3302 0.1UF/10V
C3303 0.1UF/10V
C3304 0.1UF/10V
C3310 0.1UF/10V
C3311 0.1UF/10V
C3320 0.1UF/10V
C3321 0.1UF/10V
C3322 0.1UF/10V
C3323 0.1UF/10V
C3324 0.1UF/10V
C3325 0.1UF/10V
C3326 0.1UF/10V
C3327 22UF/6.3V
C3328 0.1UF/10V
C3329 0.1UF/10V
C3330 0.1UF/10V
C3331 0.1UF/10V
C3333 27PF/50V
C3334 27PF/50V
<Variant Name>
Title : REALTEK 8111C
ASUSTeK COMPUTER INC
Engineer: Warren
Size Custom
Project Name Rocky 30 IO Board
Rev 1.1
Date: Monday, February 04, 2008
Sheet 34 of 94

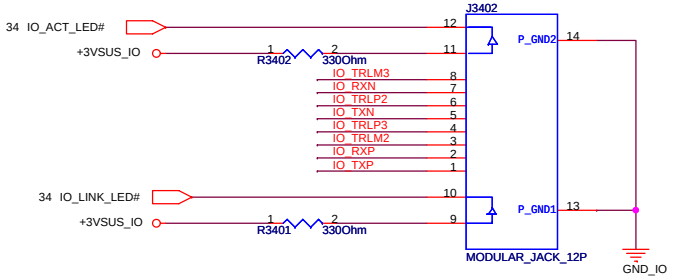




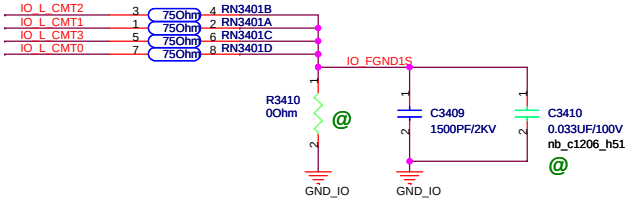
Transformer close CN3402

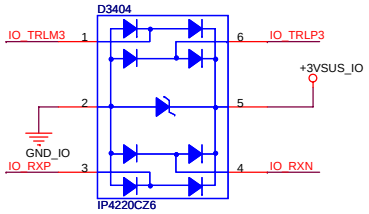


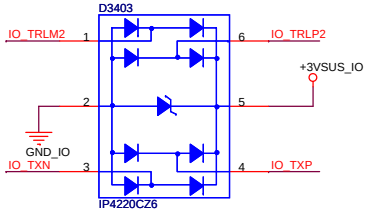




12G148301089LV
ALLTOP/C100Q2-10806-L

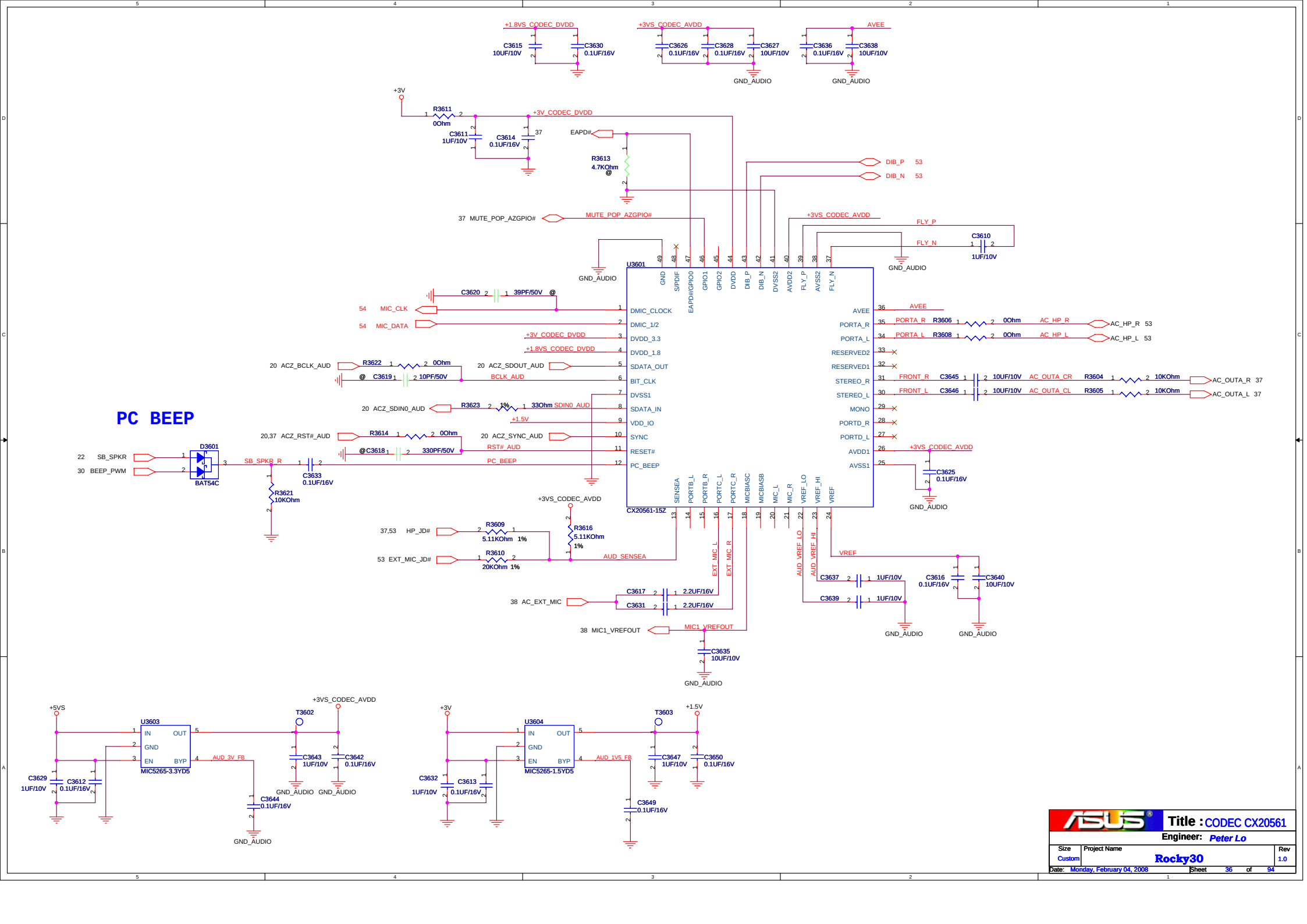


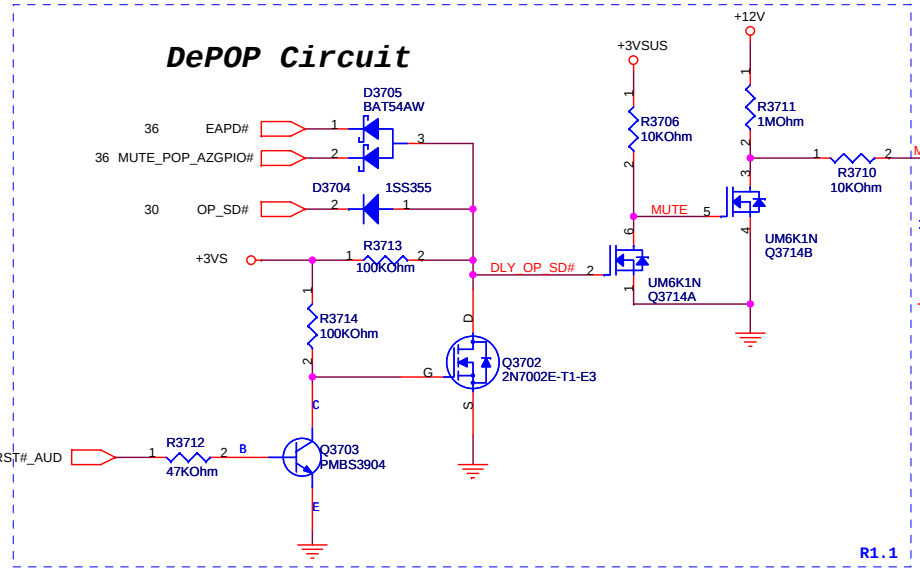


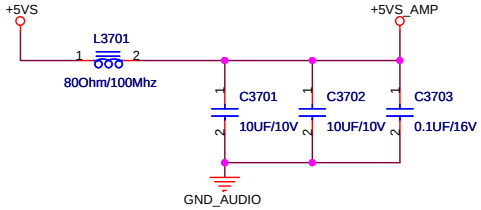


<Variant Name>

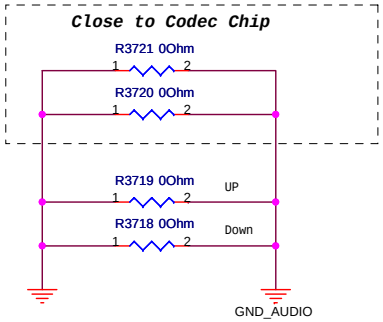
ASUSTeK COMPUTER INC	Title : LAN-RJ45	
	Engineer: Warren	
Size: Custom	Project Name: Rocky 30 IO Board	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 35 of 94	


PC BEEP
U3601
CX20561-15Z
U3603
MIC5265-3.3YD5
U3604
MIC5265-1.5YD5
D3601
BAT54C
Title : CODEC CX20561
Engineer: Peter Lo
Project Name
Rocky30
Size
Custom
Rev
1.0
Date: Monday, February 04, 2008
Sheet 36 of 94

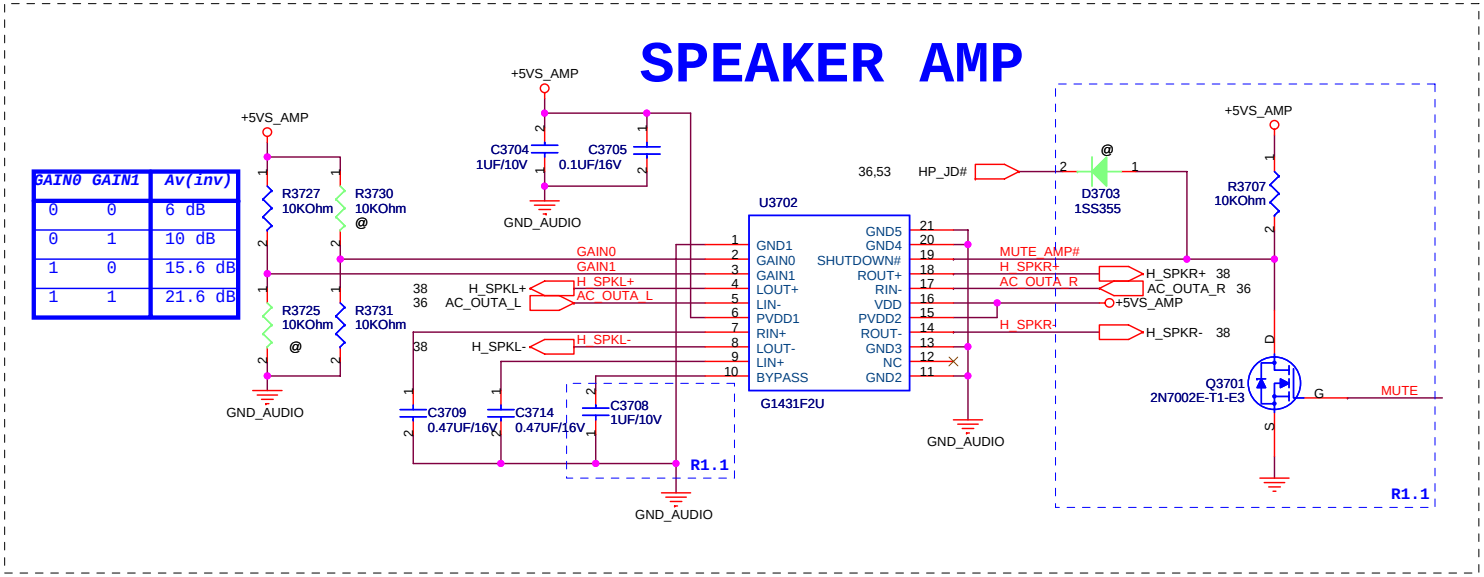




JACK GND

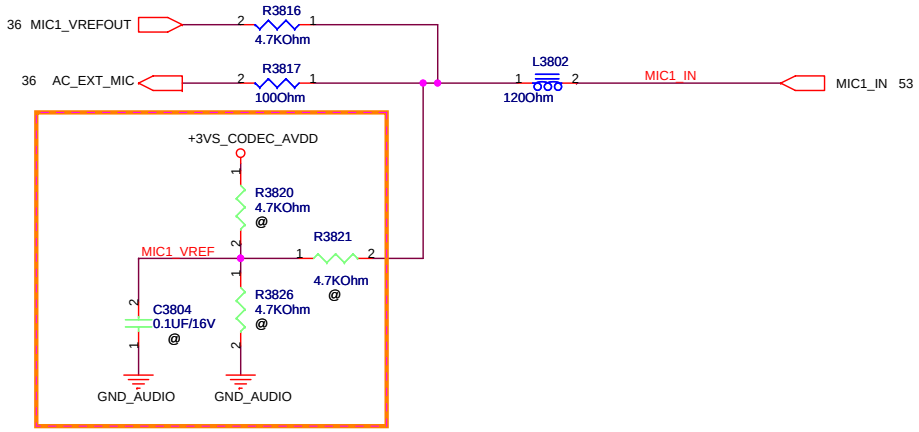


SPEAKER AMP



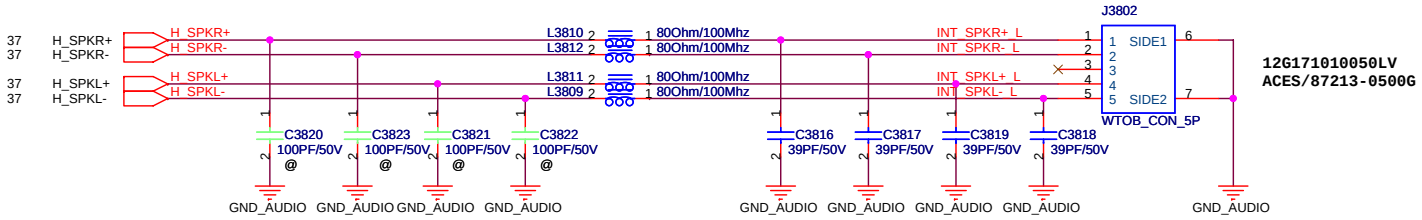
Title : AUDIO AMP		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 37 of 94	

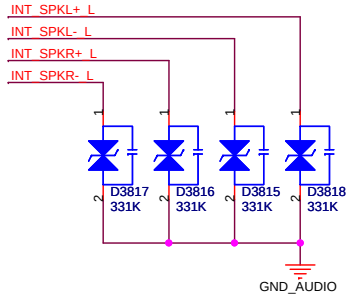
EXT MICROPHONE



Reserved the external MIC bias(T filter).

SPEAKER CONNECTOR





Title : MIC&LINEIN		
Engineer: Peter Lo		
Size: B	Project Name: Rocky30	Rev: 1.0
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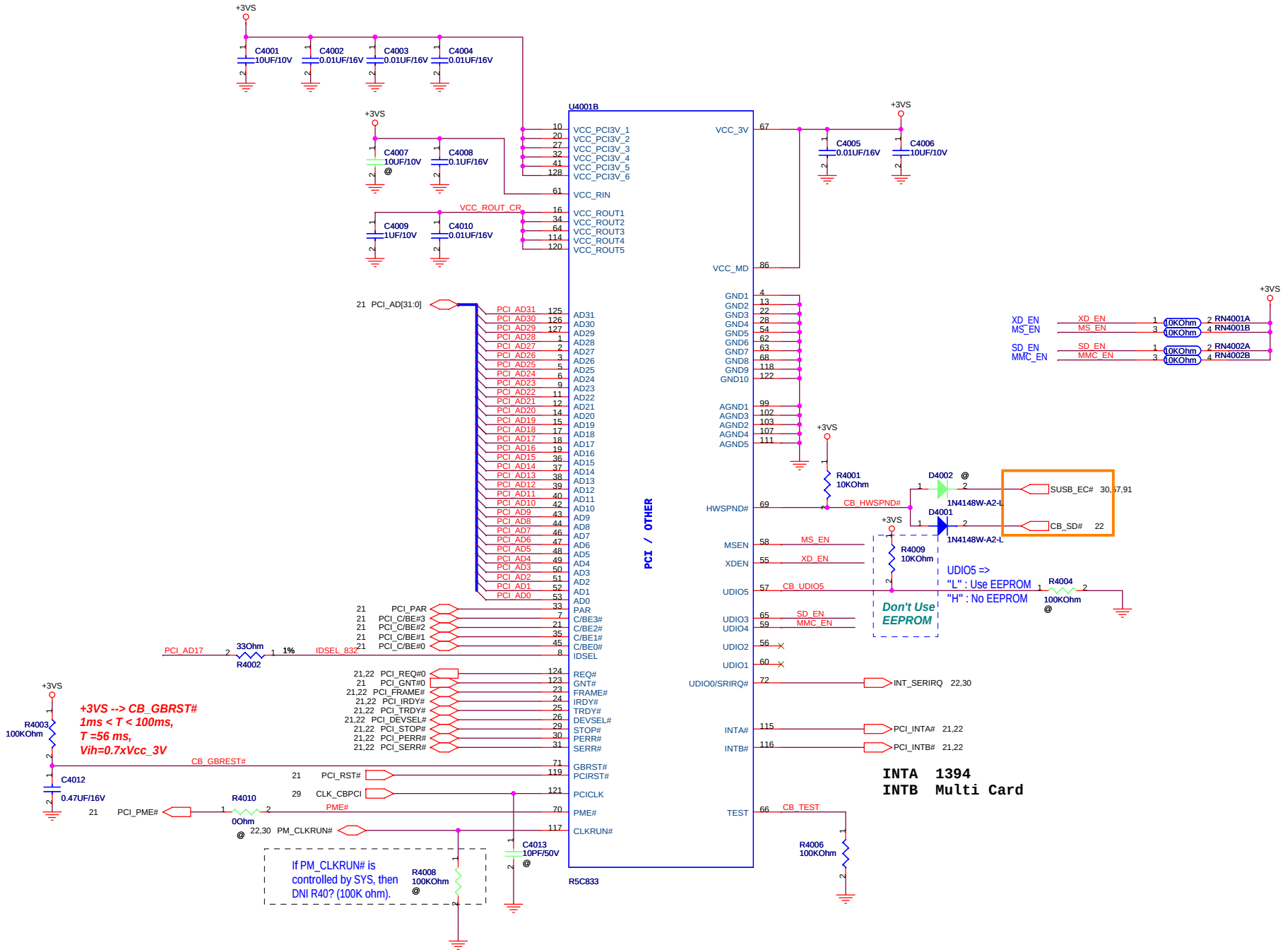
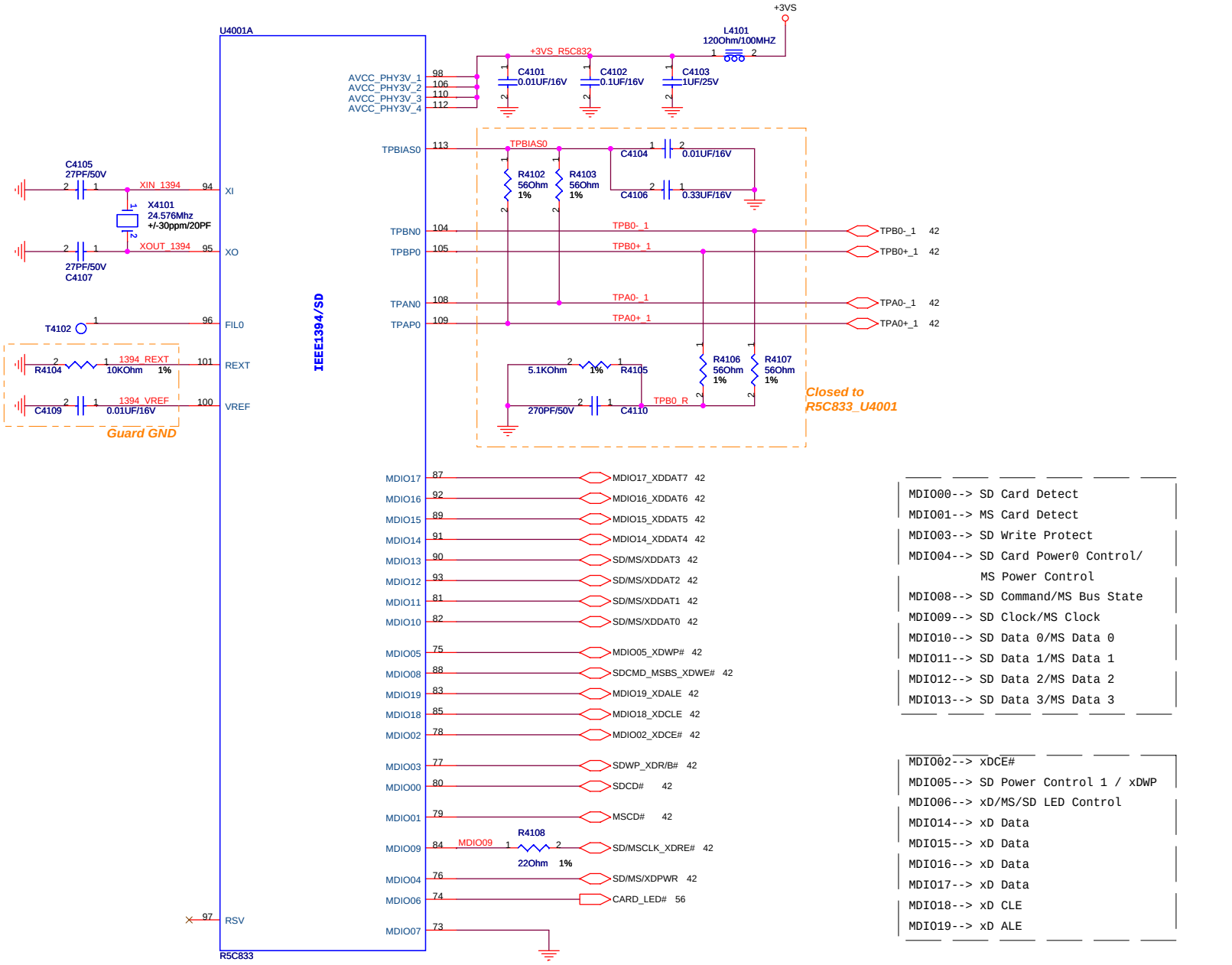
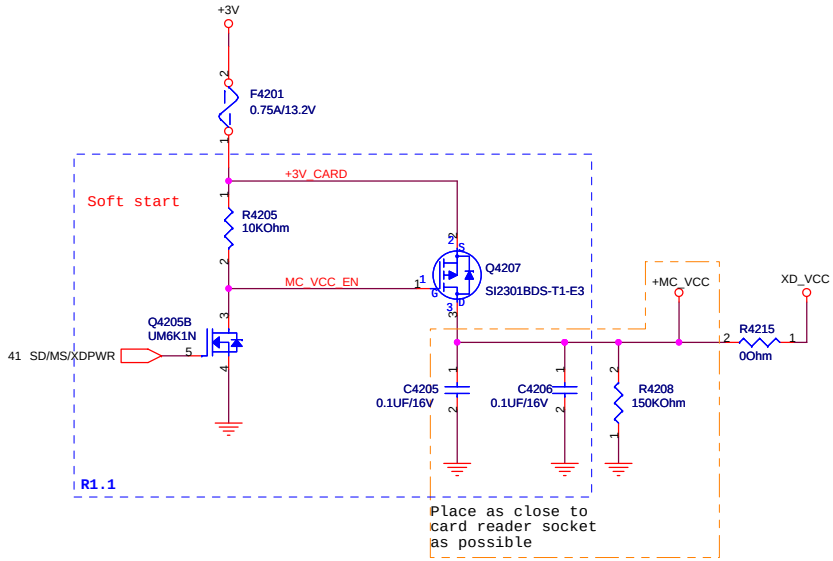
Title :	***
Engineer:	Peter Lo
Size: Custom	Project Name: Rocky30
Rev:	1.0
Date: Thursday, October 18, 2007	Sheet 39 of 94

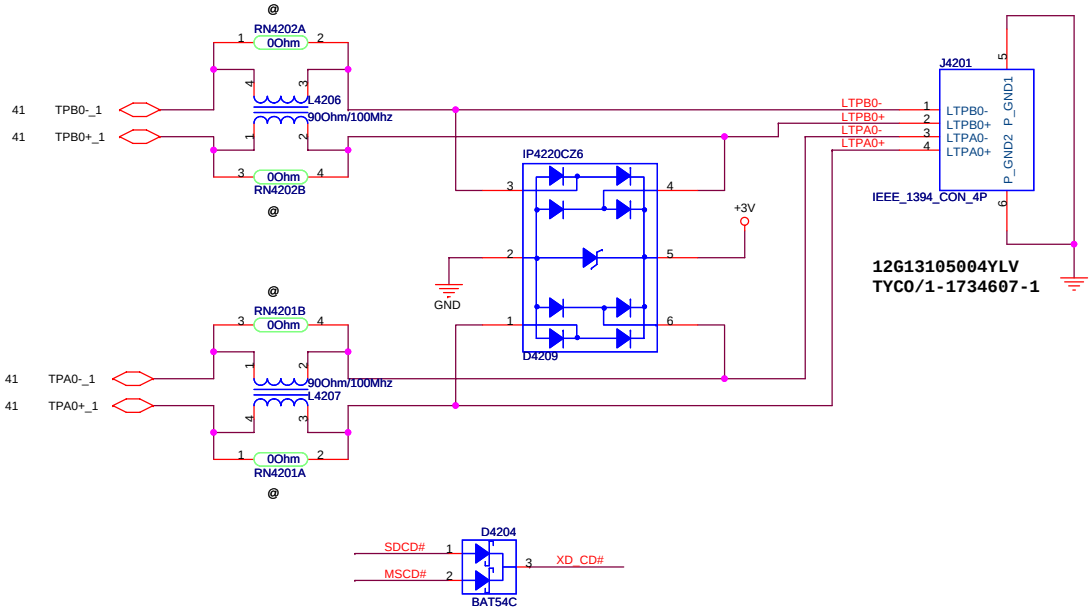


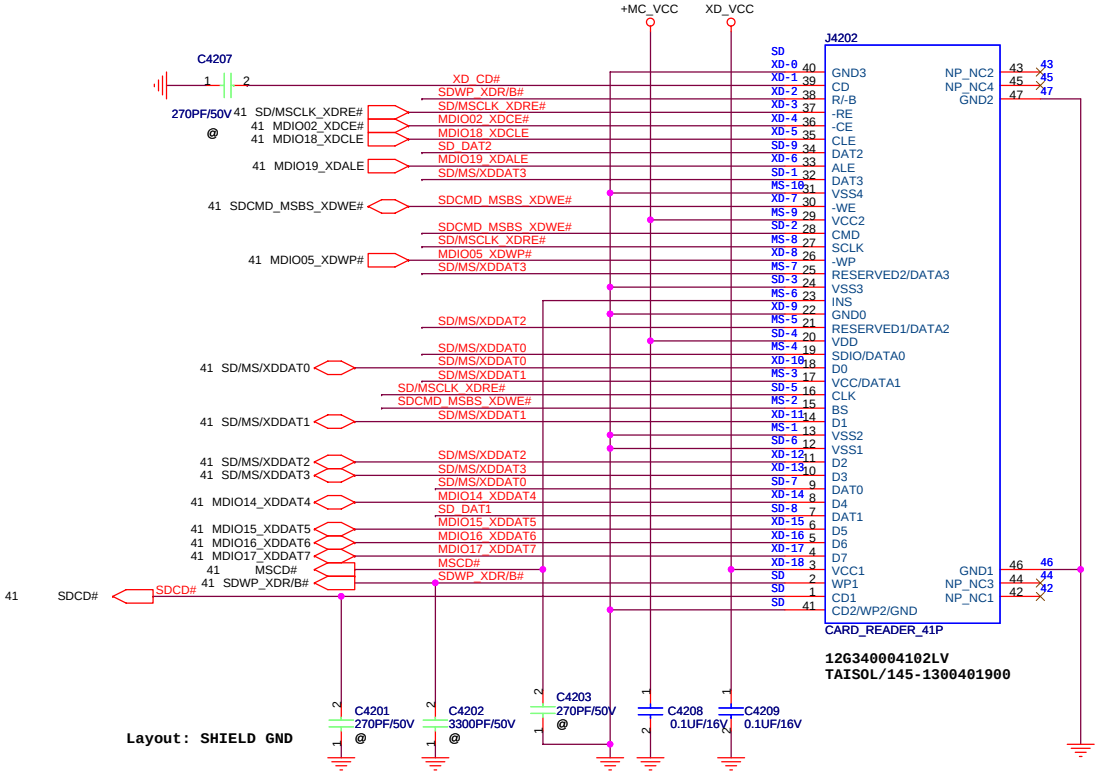
Title : CARDBUS R5C833 (1)		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 40 of 94	

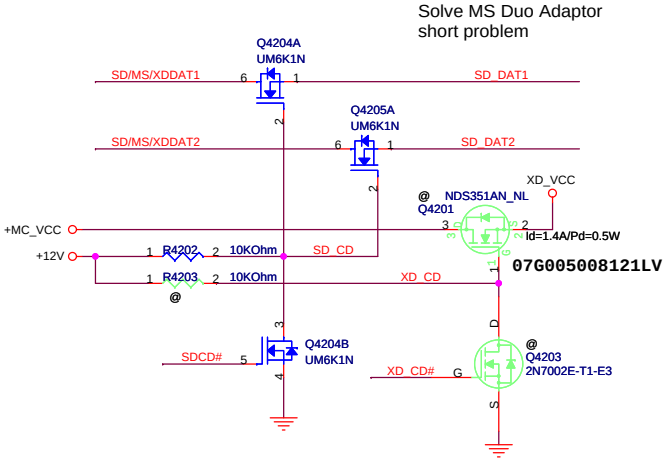


Title : CARDBUS R5C833 (2)			
Engineer: Peter Lo			
Size: Custom	Project Name: Rocky30		Rev: 1.0
Date: Monday, February 04, 2008	Sheet 41 of 94		









ASUS	Title : 1394 & CardReader	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.0
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Title : ****

Engineer: *Peter Lo*

Size	Project Name	Rev
Custom	Rocky30	1.0

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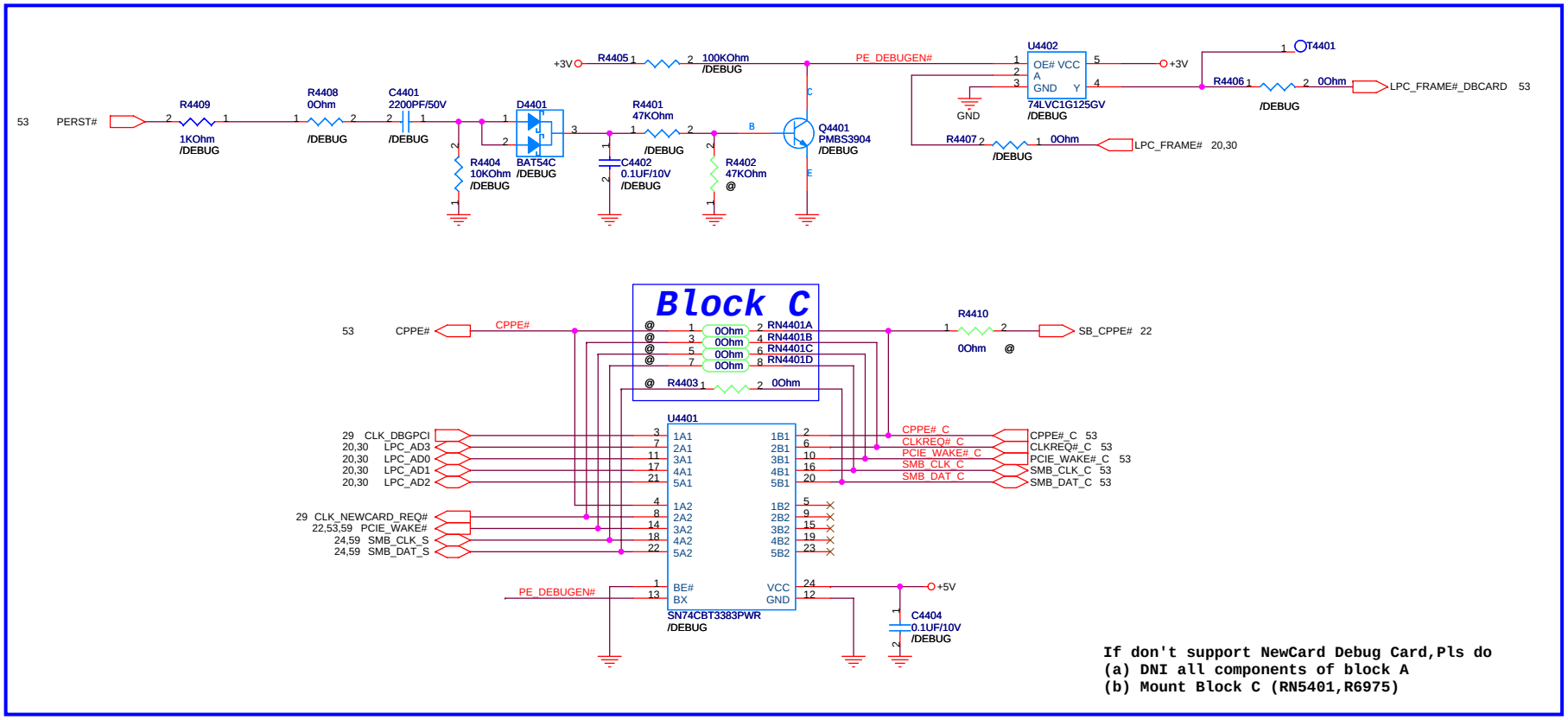
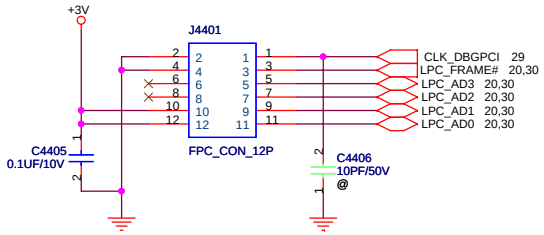
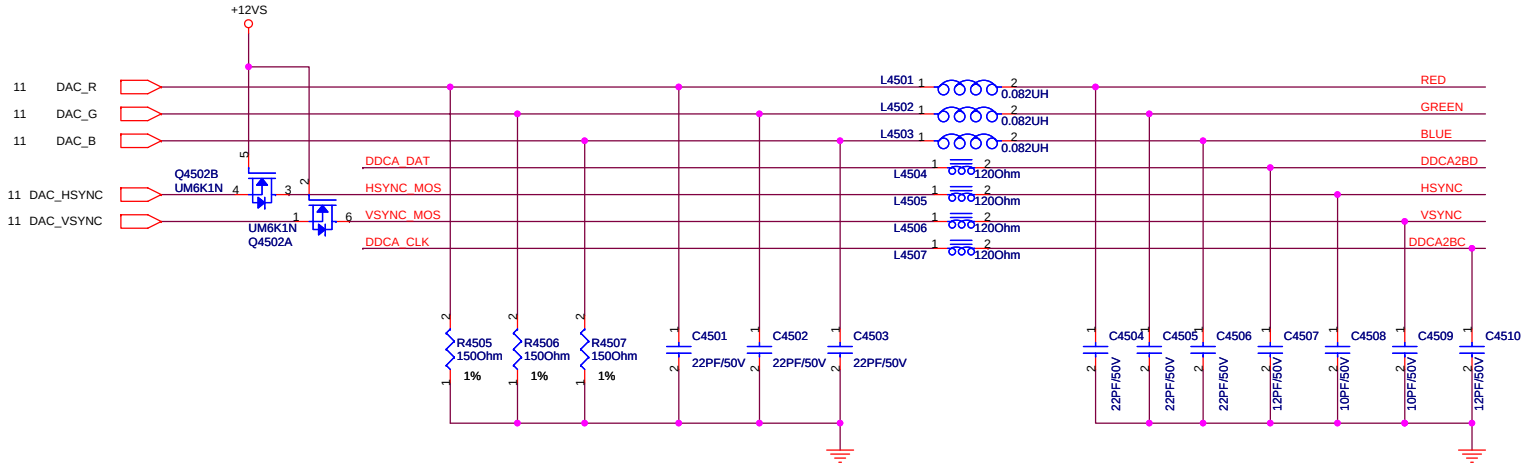
Block A

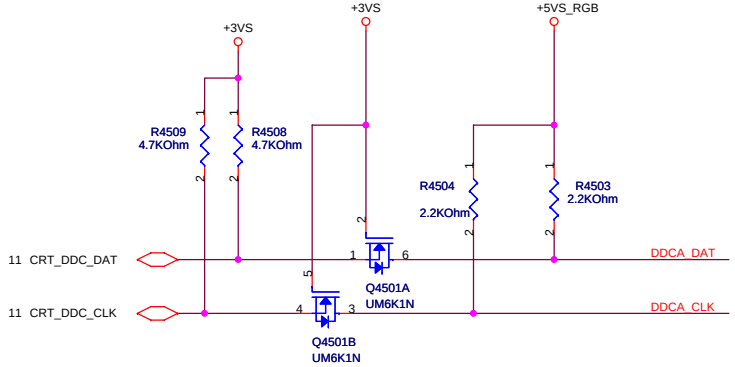


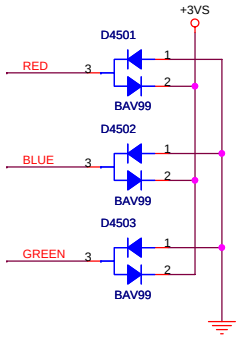


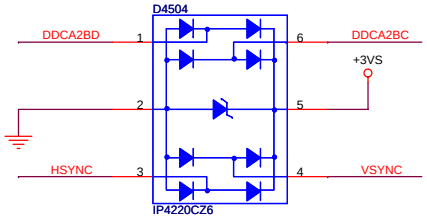
ASUS	Title : DEBUG	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 44 of 94	

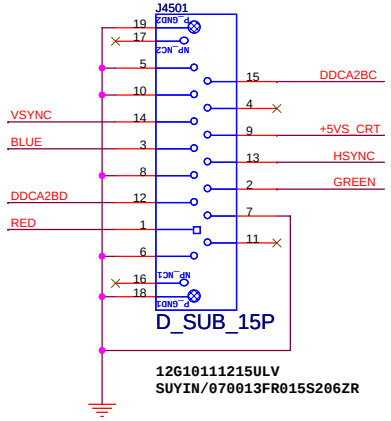


PLACE ESD Diodes near VGA port





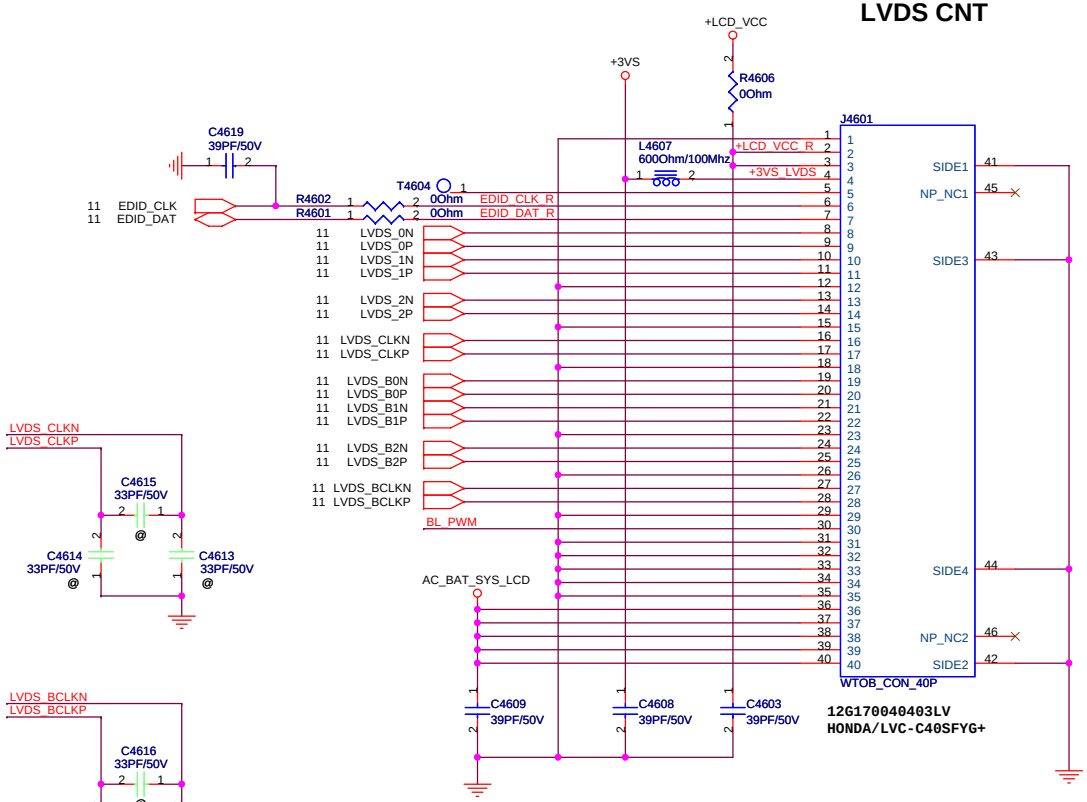




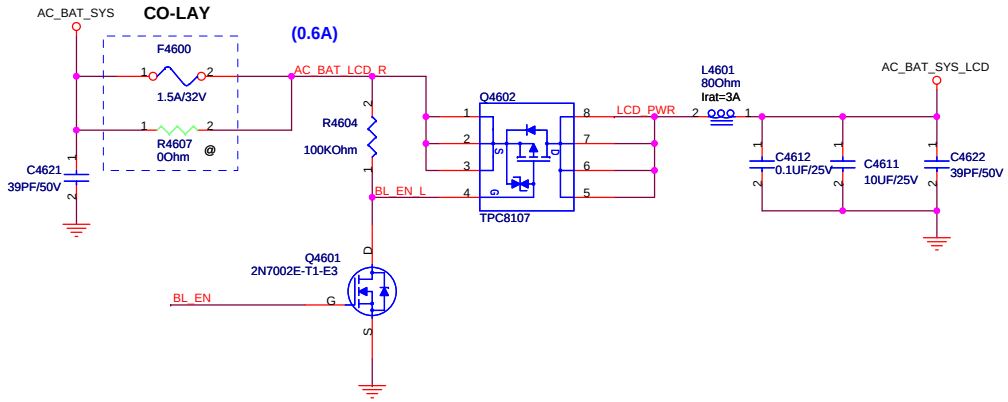
12G10111215ULV
SUYIN/070013FR015S206ZR

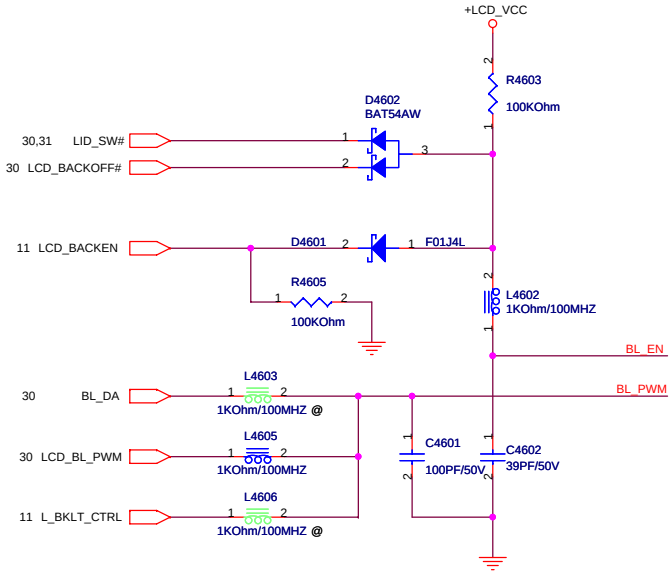
Title : CRT		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 45 of 94	

LVDS CNT

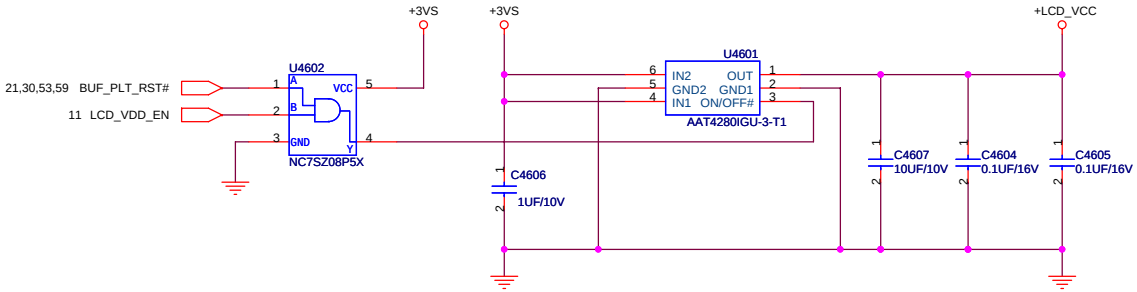


12G170040403LV
HONDA/LVC-C40SFYG+





Power Switch for LCD Power



Title : LVDS & Inverter CON		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
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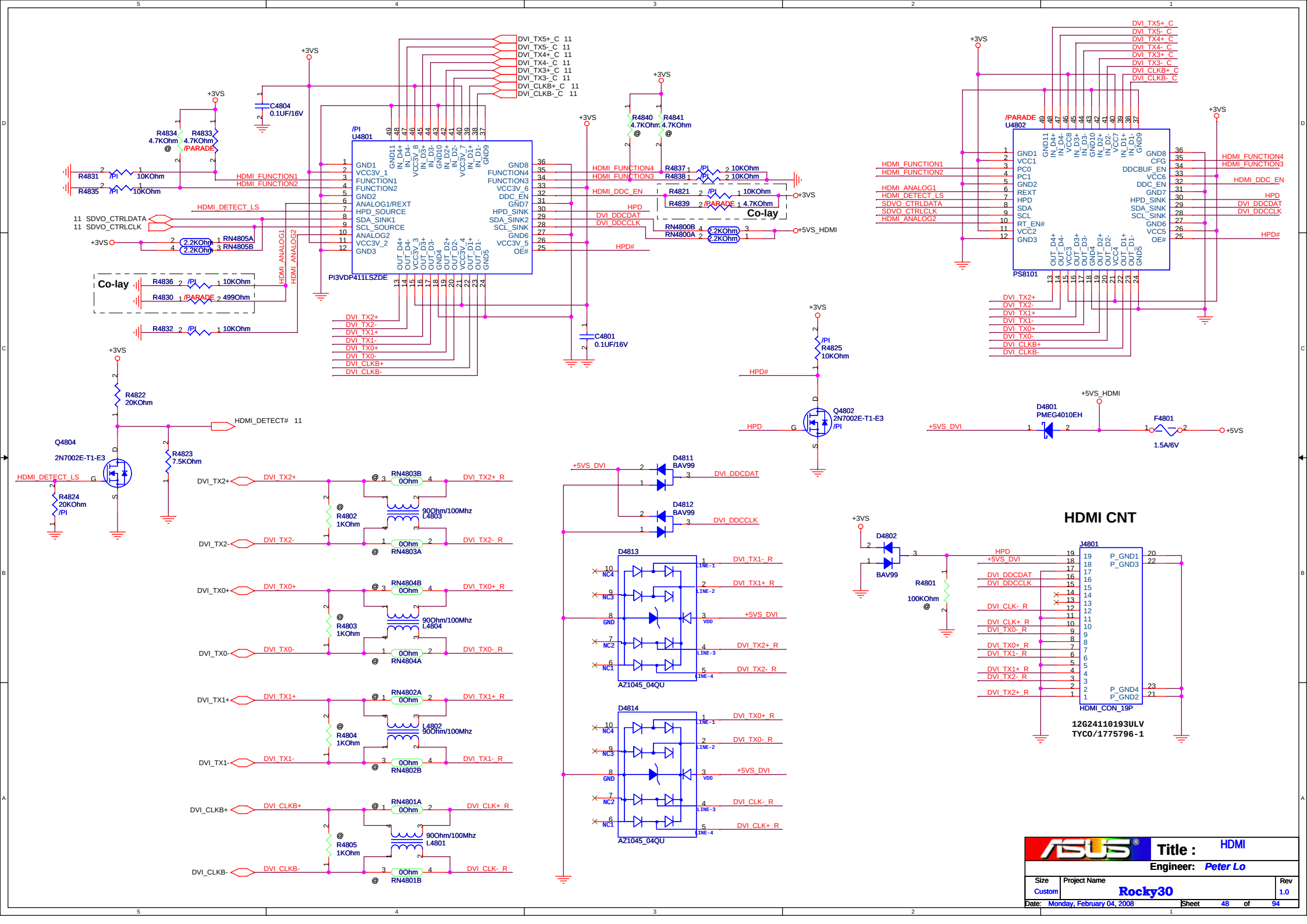
Title :	***
Engineer:	Peter Lo
Size: C	Project Name: Rocky30
Rev: 1.0	
Date: Thursday, October 18, 2007	Sheet 47 of 94


DVI_TX5+_C 11
DVI_TX5-_C 11
DVI_TX4+_C 11
DVI_TX4-_C 11
DVI_TX3+_C 11
DVI_TX3-_C 11
DVI_CLKB+_C 11
DVI_CLKB-_C 11
+3VS
C4804
0.1UF/16V
R4834
4.7KOhm
@
R4833
4.7KOhm
/PARADE
R4831
/PI
10KOhm
R4835
/PI
10KOhm
HDMI_FUNCTION1
HDMI_FUNCTION2
HDMI_DETECT_LS
11 SDVO_CTRLDATA
11 SDVO_CTRLCLK
2.2KOhm
2.2KOhm
RN4805A
RN4805B
HDMI_ANALOG1
HDMI_ANALOG2
Co-lay
R4836
/PI
10KOhm
R4830
/PARADE
499Ohm
R4832
/PI
10KOhm
/PI
U4801
GND1
VCC3V_1
FUNCTION1
FUNCTION2
GND2
ANALOG1/REXT
HPD_SOURCE
SDA_SINK1
SCL_SOURCE
ANALOG2
VCC3V_2
GND3
GND8
FUNCTION4
FUNCTION3
VCC3V_6
DDC_EN
GND7
HPD_SINK
SDA_SINK2
SCL_SINK
GND6
VCC3V_5
OE#
PI3VDP411LSZDE
R4840
4.7KOhm
@
R4841
4.7KOhm
@
HDMI_FUNCTION4
HDMI_FUNCTION3
R4837
/PI
10KOhm
R4838
/PI
10KOhm
HDMI_DDC_EN
R4821
/PI
10KOhm
R4839
/PARADE
4.7KOhm
Co-lay
+5VS
HPD
DVI_DDCDAT
DVI_DDCCLK
RN4800B
2.2KOhm
RN4800A
2.2KOhm
+5VS_HDMI
HPD#
C4801
0.1UF/16V
DVI_TX2+
DVI_TX2-
DVI_TX1+
DVI_TX1-
DVI_TX0+
DVI_TX0-
DVI_CLKB+
DVI_CLKB-
DVI_TX5+_C
DVI_TX5-_C
DVI_TX4+_C
DVI_TX4-_C
DVI_TX3+_C
DVI_TX3-_C
DVI_CLKB+_C
DVI_CLKB-_C
/PARADE
U4802
HDMI_FUNCTION1
HDMI_FUNCTION2
HDMI_ANALOG1
HDMI_DETECT_LS
SDVO_CTRLDATA
SDVO_CTRLCLK
HDMI_ANALOG2
HDMI_FUNCTION4
HDMI_FUNCTION3
HDMI_DDC_EN
HPD
DVI_DDCDAT
DVI_DDCCLK
HPD#
PS8101
R4822
20KOhm
HDMI_DETECT# 11
Q4804
2N7002E-T1-E3
R4823
7.5KOhm
R4824
20KOhm
/PI
R4825
10KOhm
Q4802
2N7002E-T1-E3
/PI
+5VS_DVI
D4801
PMEG4010EH
F4801
1.5A/6V
D4811
BAV99
D4812
BAV99
D4813
AZ1045_04QU
D4814
AZ1045_04QU
RN4803B
0Ohm
RN4803A
0Ohm
RN4804B
0Ohm
RN4804A
0Ohm
RN4802A
0Ohm
RN4802B
0Ohm
RN4801A
0Ohm
RN4801B
0Ohm
R4802
1KOhm
R4803
1KOhm
R4804
1KOhm
R4805
1KOhm
90Ohm/100Mhz
L4803
L4804
L4802
L4801
DVI_TX2+_R
DVI_TX2-_R
DVI_TX0+_R
DVI_TX0-_R
DVI_TX1+_R
DVI_TX1-_R
DVI_CLK+_R
DVI_CLK-_R
D4802
BAV99
R4801
100KOhm
@
HDMI CNT
J4801
HDMI_CON_19P
12G24110193ULV
TYCO/1775796-1
Title : HDMI
Engineer: Peter Lo
Size Custom
Project Name Rocky30
Rev 1.0
Date: Monday, February 04, 2008
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Title :	
Engineer:	Peter Lo
Size: A	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
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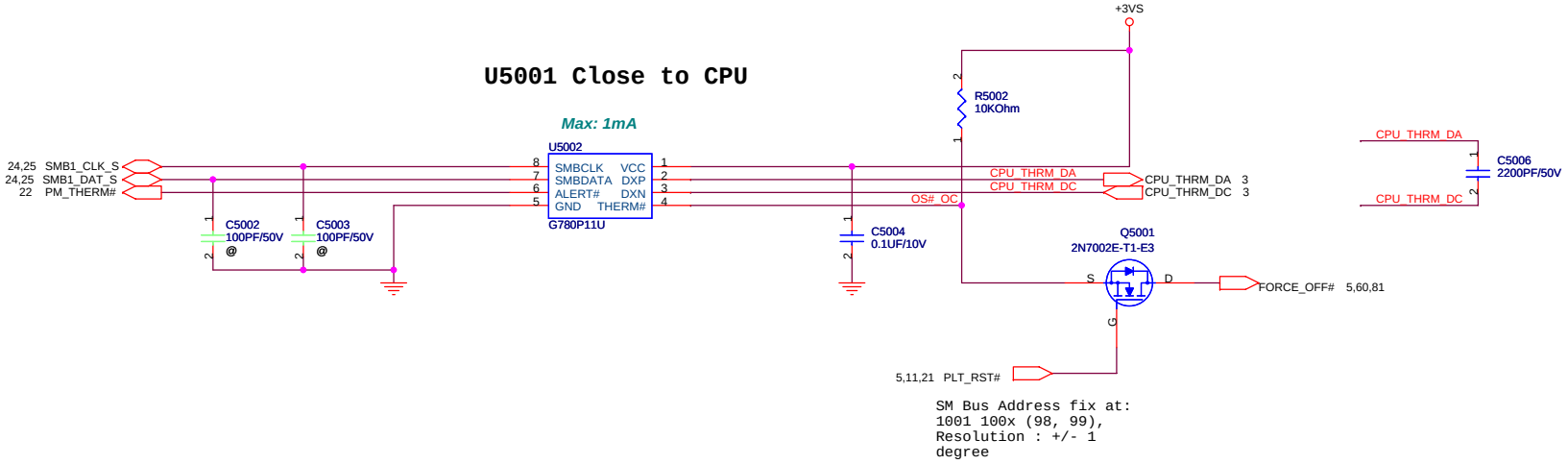
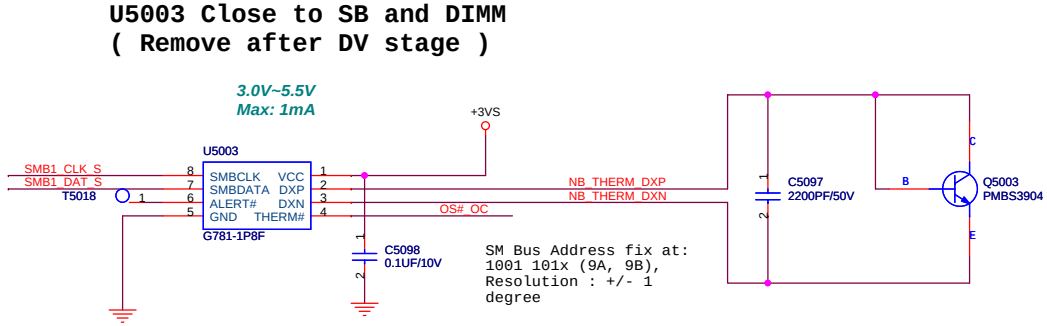
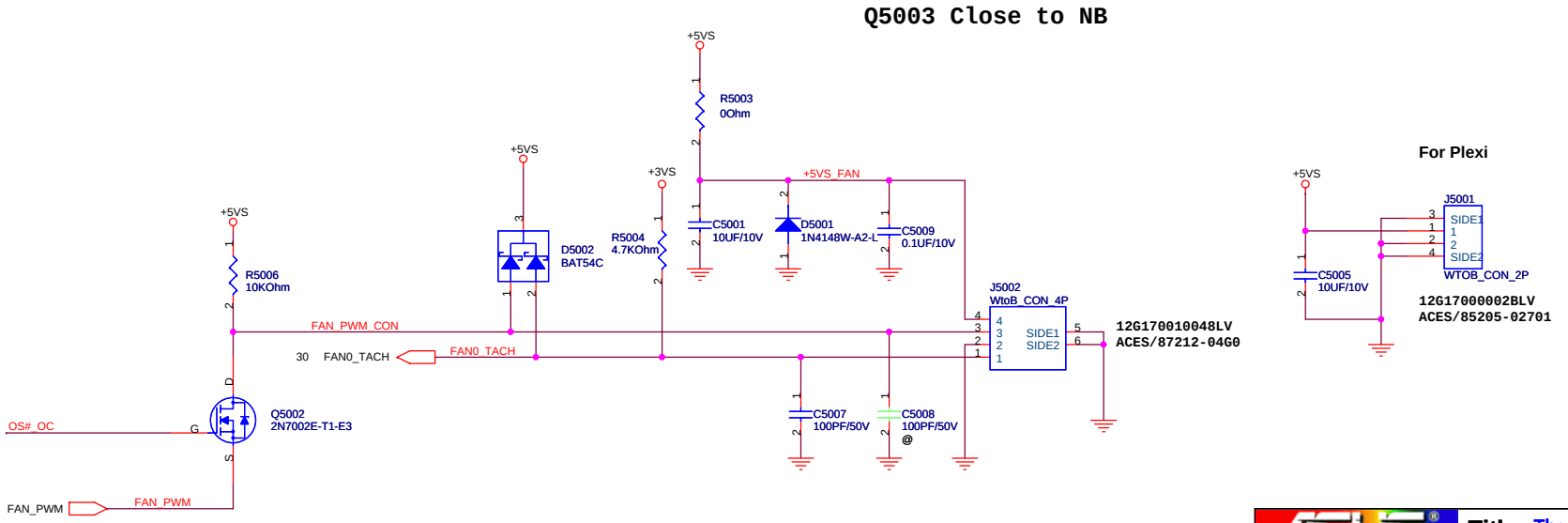
Thermal Sensor

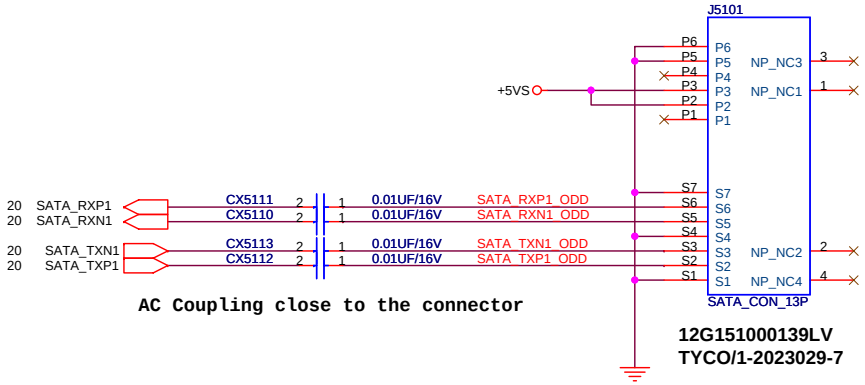






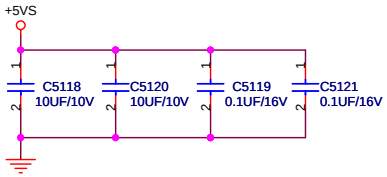
Title : Thermal & Fan		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 50 of 94	

ODD CON

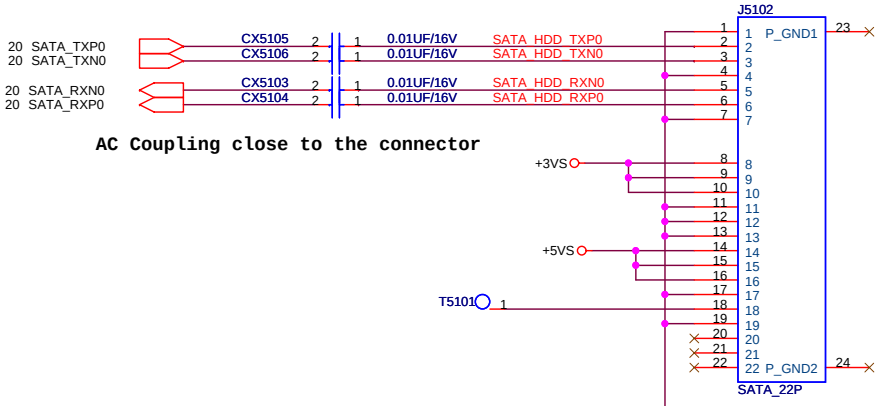


AC Coupling close to the connector

12G151000139LV
TYCO/1-2023029-7

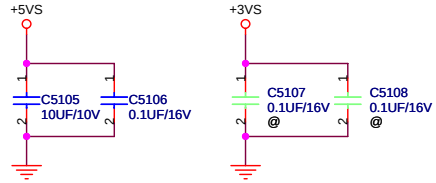


SATA HDD CON



AC Coupling close to the connector

12G15111022PLV
TYCO/1735544-1



Title : Sata HDD & Swap Bay		
Engineer: Peter Lo		
Size: B	Project Name: Rocky30	Rev: 1.0
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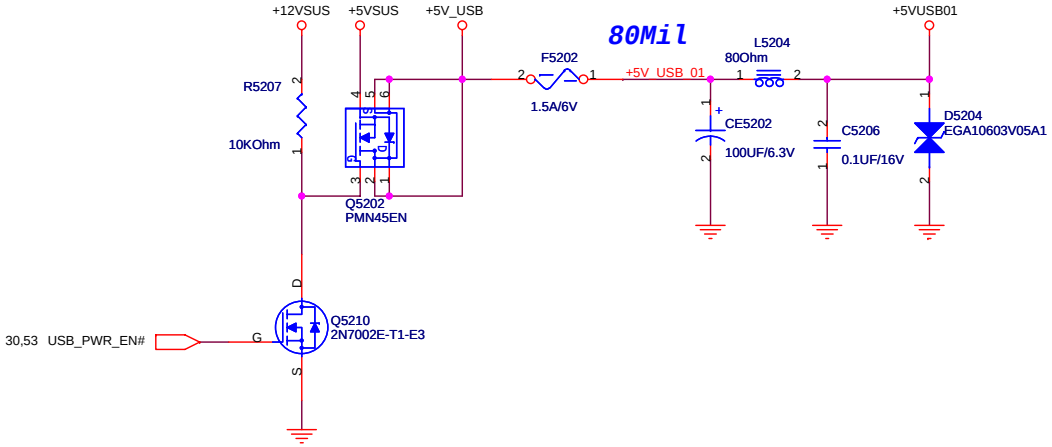
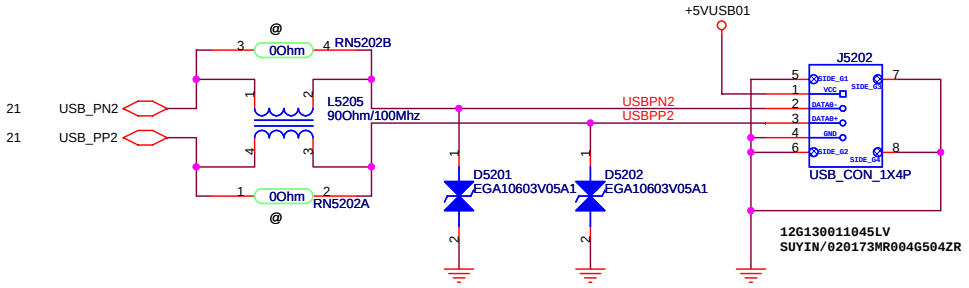
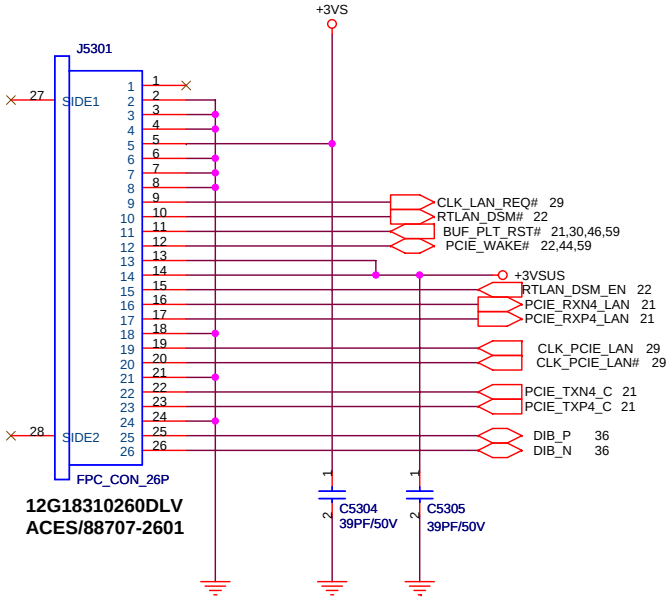




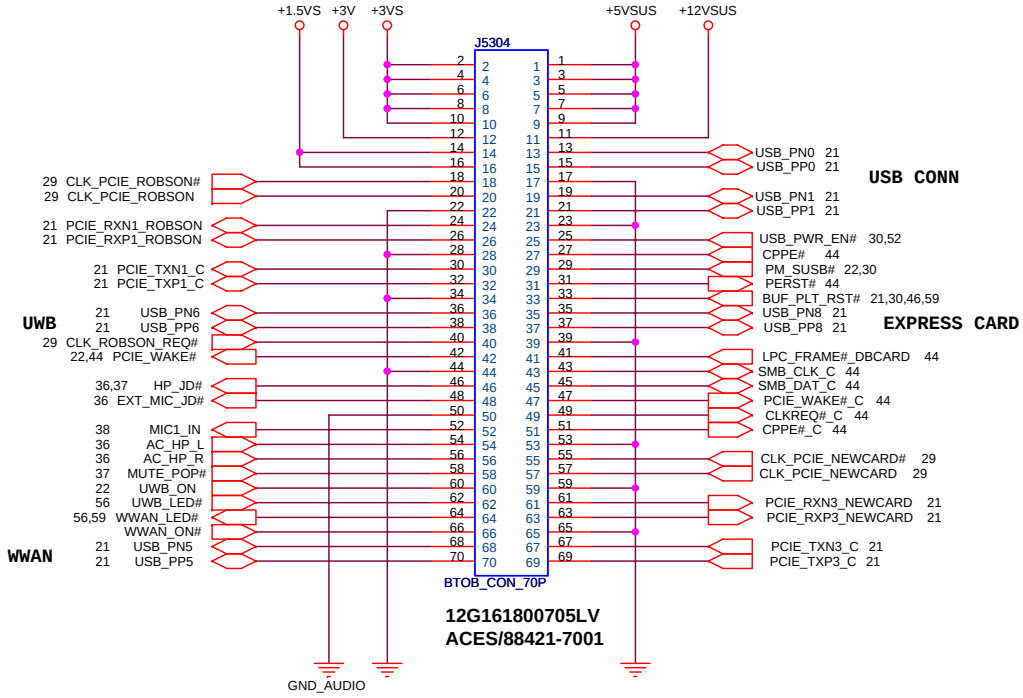
Title : USB CONN		
Engineer: Peter Lo		
Size: B	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 52 of 94	

IO BOARD



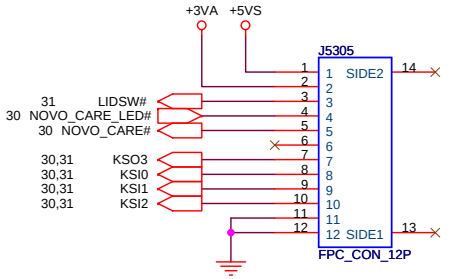
12G18310260DLV
ACES/88707-2601

SMALL BOARD

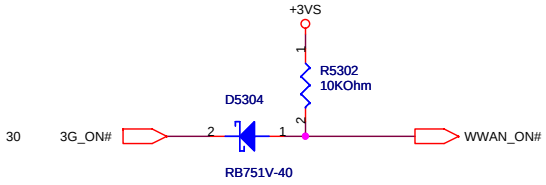


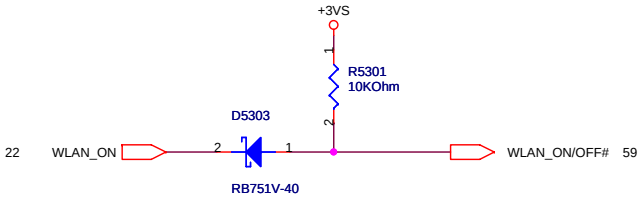
12G161800705LV
ACES/88421-7001

For Media Control Board

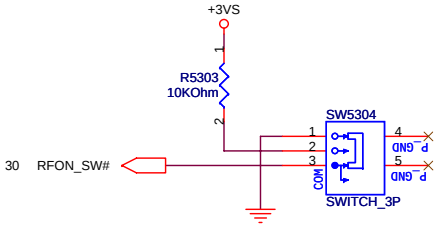


12G18310120BLV
ACES/88278-1200L



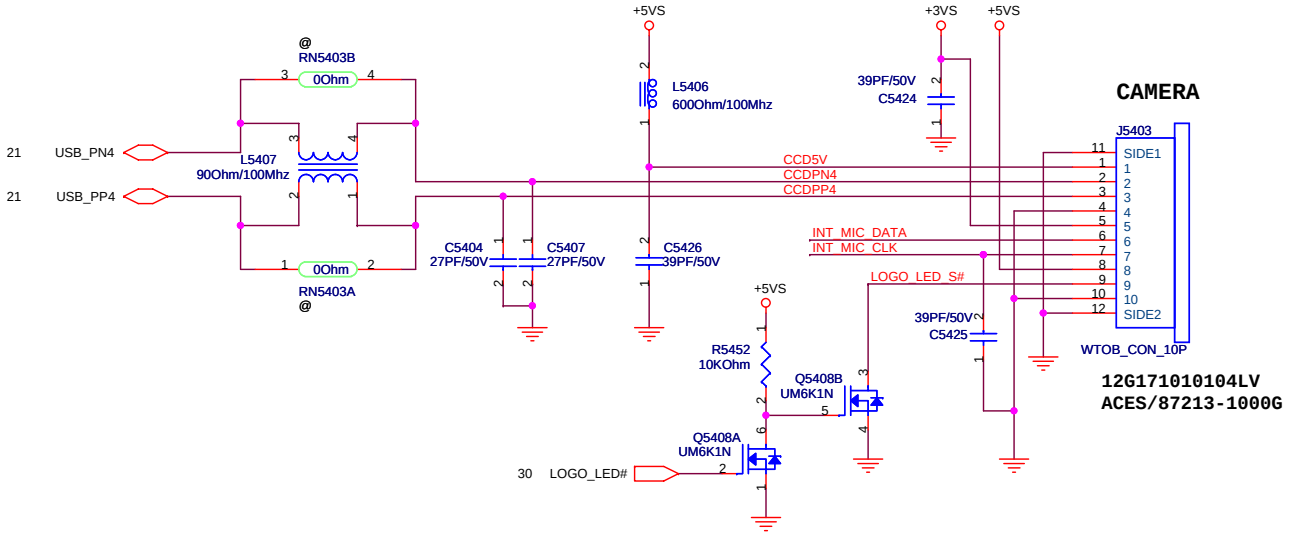


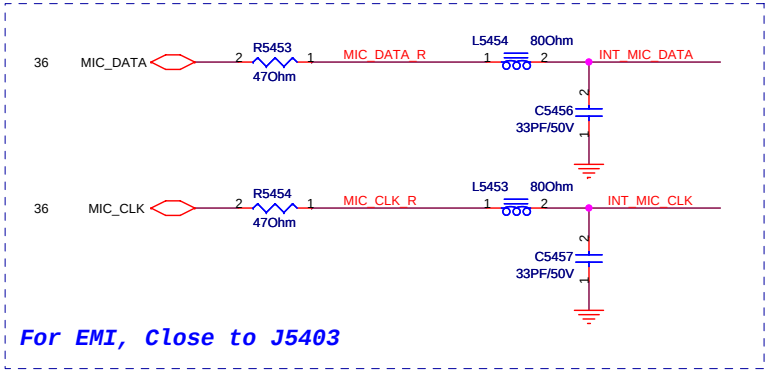
Wireless Switch



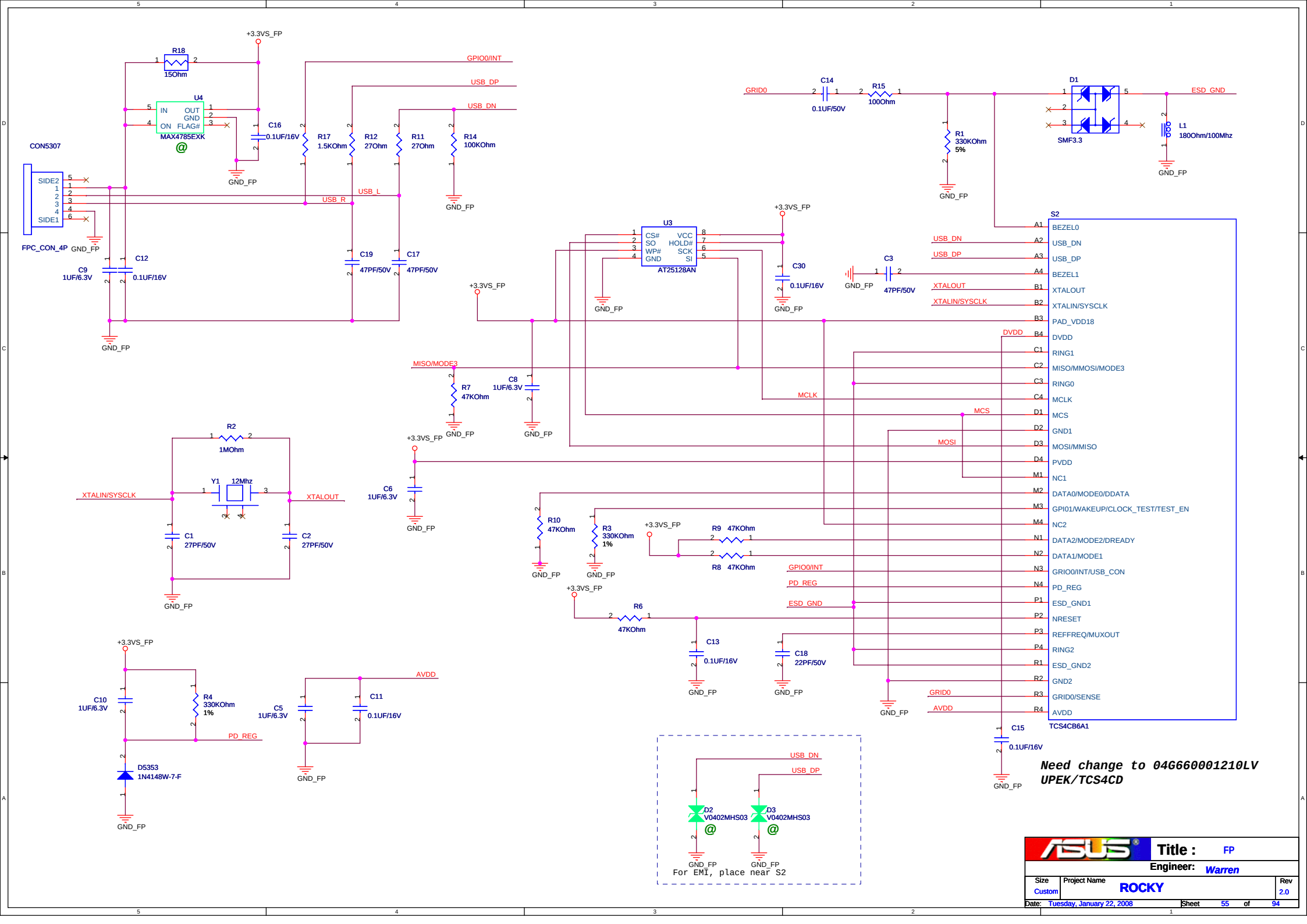
12G091070031LV
ALPS/SSSS710603

Title : IO BOARD		
Engineer: Peter Lo		
Size: B	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 53 of 94	

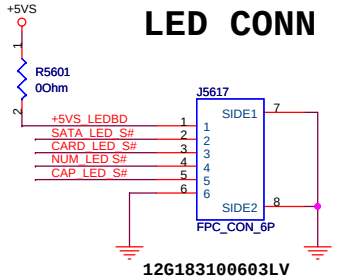




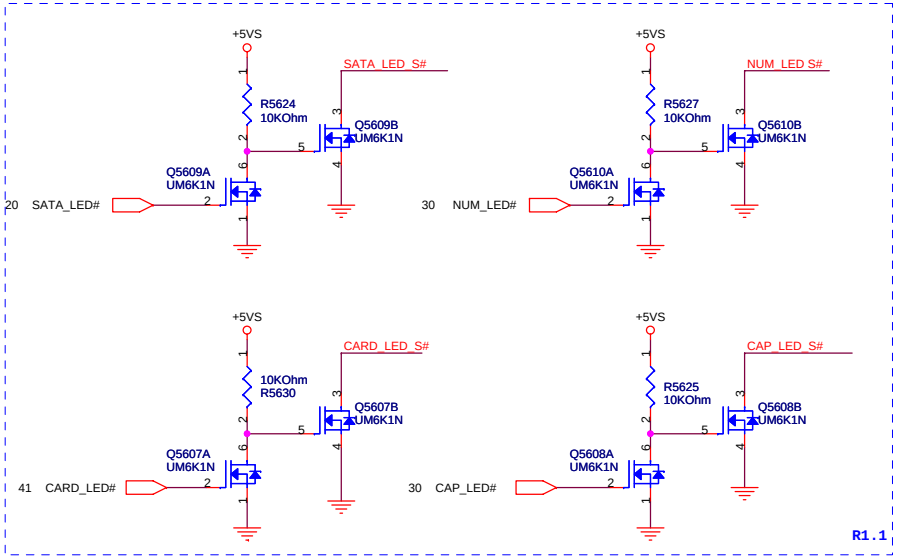
Title : CAMERA		
Engineer: Peter Lo		
Size: B	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 54 of 94	

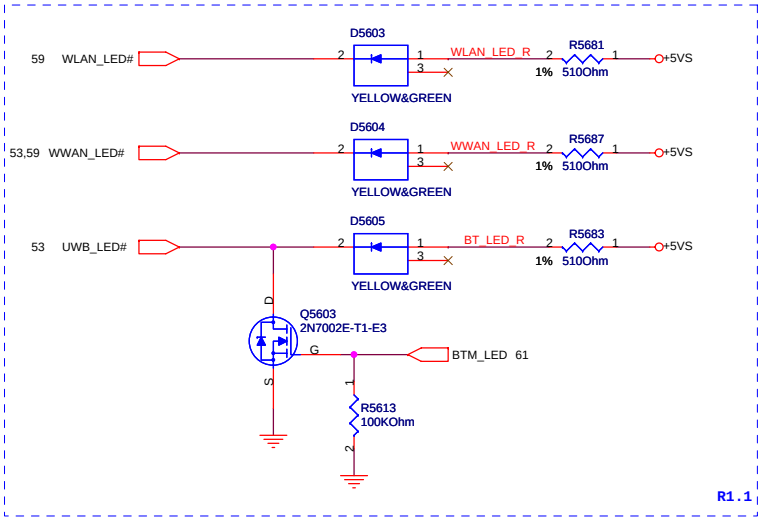

+3.3VS_FP
R18
15Ohm
U4
IN
OUT
GND
ON
FLAG#
MAX4785EXK
@
C16
0.1UF/16V
GND_FP
GPIO0/INT
USB_DP
USB_DN
R17
1.5KOhm
R12
27Ohm
R11
27Ohm
R14
100KOhm
CON5307
SIDE2
SIDE1
FPC_CON_4P
USB_L
USB_R
C9
1UF/6.3V
C12
0.1UF/16V
C19
47PF/50V
C17
47PF/50V
GRID0
C14
0.1UF/50V
R15
100Ohm
D1
SMF3.3
ESD_GND
L1
180Ohm/100Mhz
R1
330KOhm
5%
U3
CS#
SO
WP#
GND
VCC
HOLD#
SCK
SI
AT25128AN
C30
0.1UF/16V
C3
47PF/50V
S2
BEZEL0
USB_DN
USB_DP
BEZEL1
XTALOUT
XTALIN/SYSCLK
PAD_VDD18
DVDD
RING1
MISO/MMOSI/MODE3
RING0
MCLK
MCS
GND1
MOSI/MMISO
PVDD
NC1
DATA0/MODE0/DDATA
GPI01/WAKEUP/CLOCK_TEST/TEST_EN
NC2
DATA2/MODE2/DREADY
DATA1/MODE1
GRIO0/INT/USB_CON
PD_REG
ESD_GND1
NRESET
REFFREQ/MUXOUT
RING2
ESD_GND2
GND2
GRID0/SENSE
AVDD
TCS4CB6A1
C15
0.1UF/16V
MISO/MODE3
R7
47KOhm
C8
1UF/6.3V
C6
1UF/6.3V
R2
1MOhm
Y1
12Mhz
XTALIN/SYSCLK
XTALOUT
C1
27PF/50V
C2
27PF/50V
R10
47KOhm
R3
330KOhm
1%
R9
47KOhm
R8
47KOhm
MCLK
MCS
MOSI
GPIO0/INT
PD_REG
ESD_GND
R6
47KOhm
C13
0.1UF/16V
C18
22PF/50V
C10
1UF/6.3V
R4
330KOhm
1%
C5
1UF/6.3V
C11
0.1UF/16V
AVDD
D5353
1N4148W-7-F
D2
V0402MHS03
D3
V0402MHS03
For EMI, place near S2
Need change to 04G660001210LV
UPEK/TCS4CD
Title : FP
Engineer: Warren
Size Custom
Project Name ROCKY
Rev 2.0
Date: Tuesday, January 22, 2008
Sheet 55 of 94

LED CONN

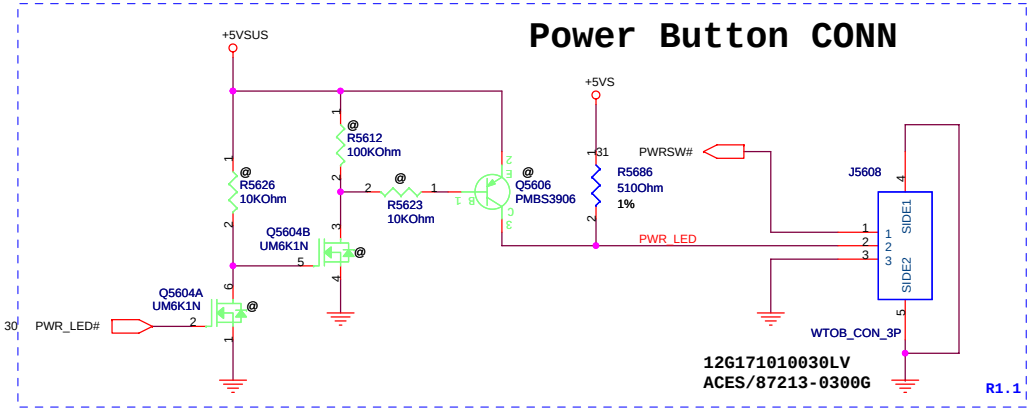


12G183100603LV
ACES/88278-06001

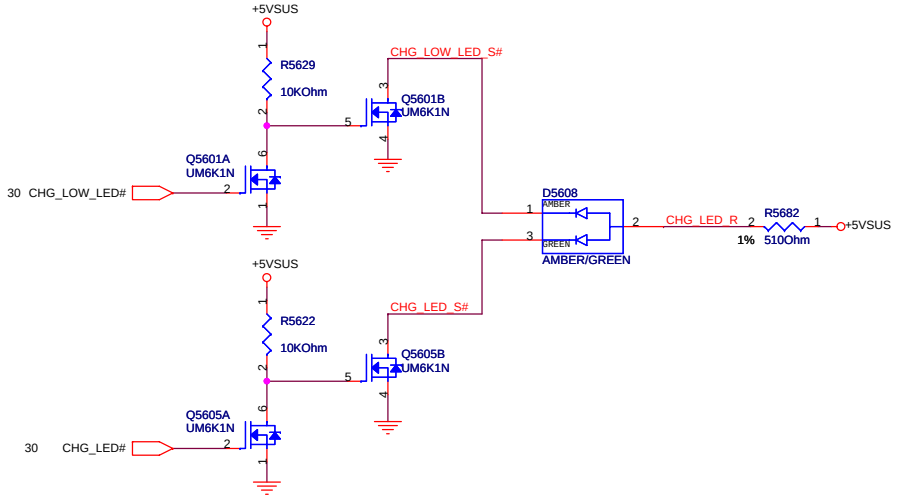


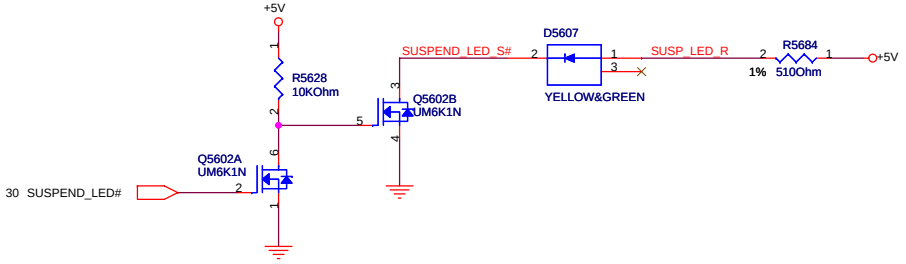


Power Button CONN

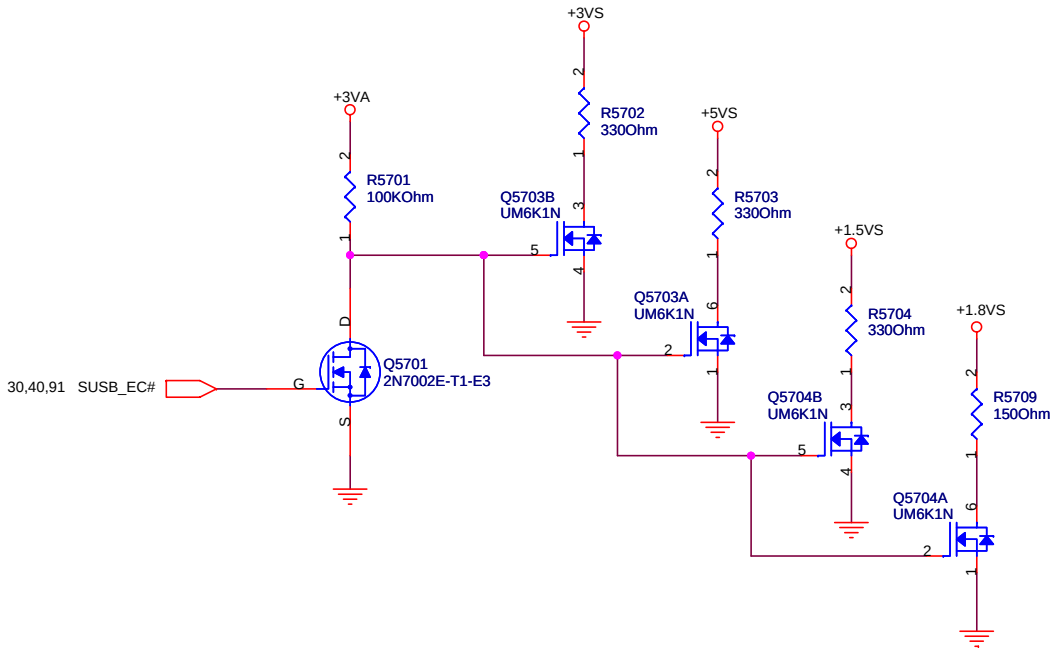


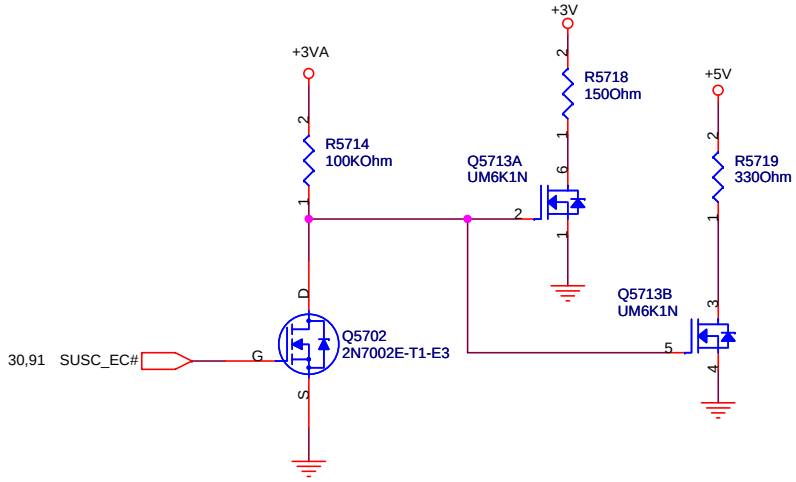
12G171010030LV
ACES/87213-0300G
R1.1



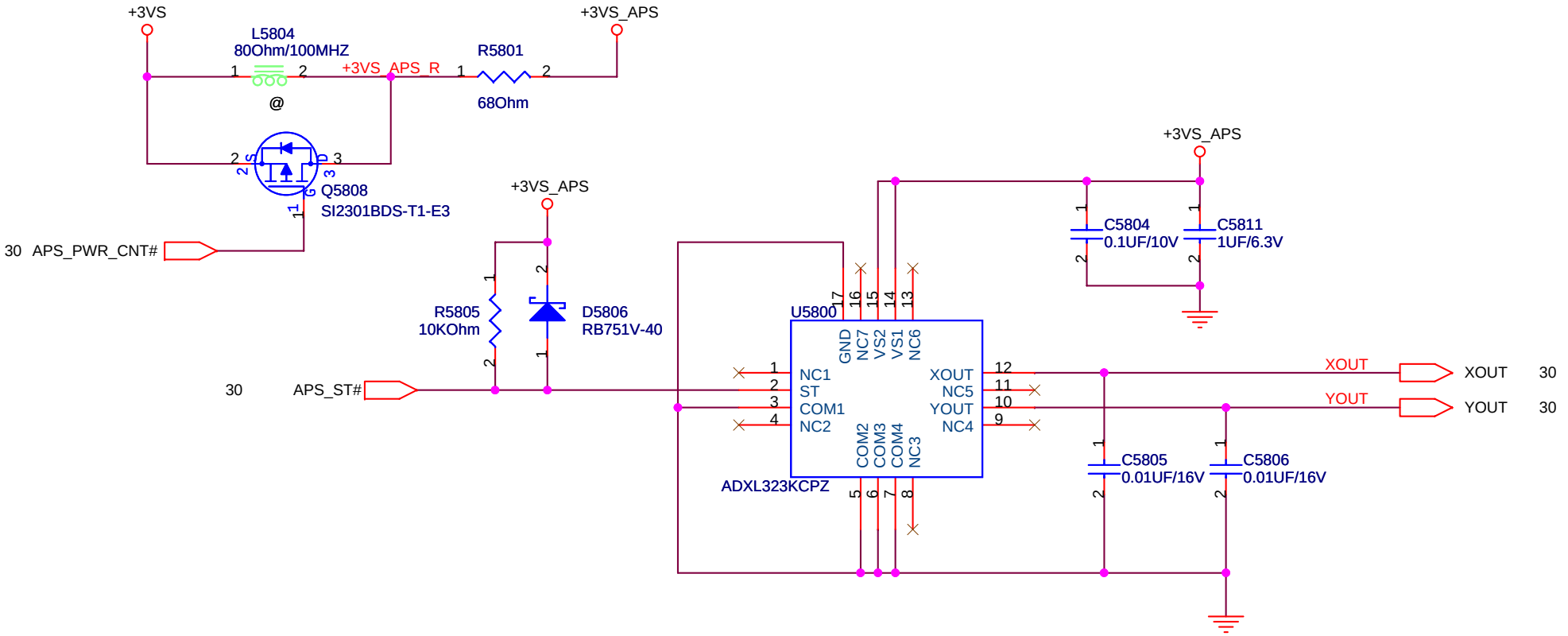


Title : LED/SW		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 56 of 94	

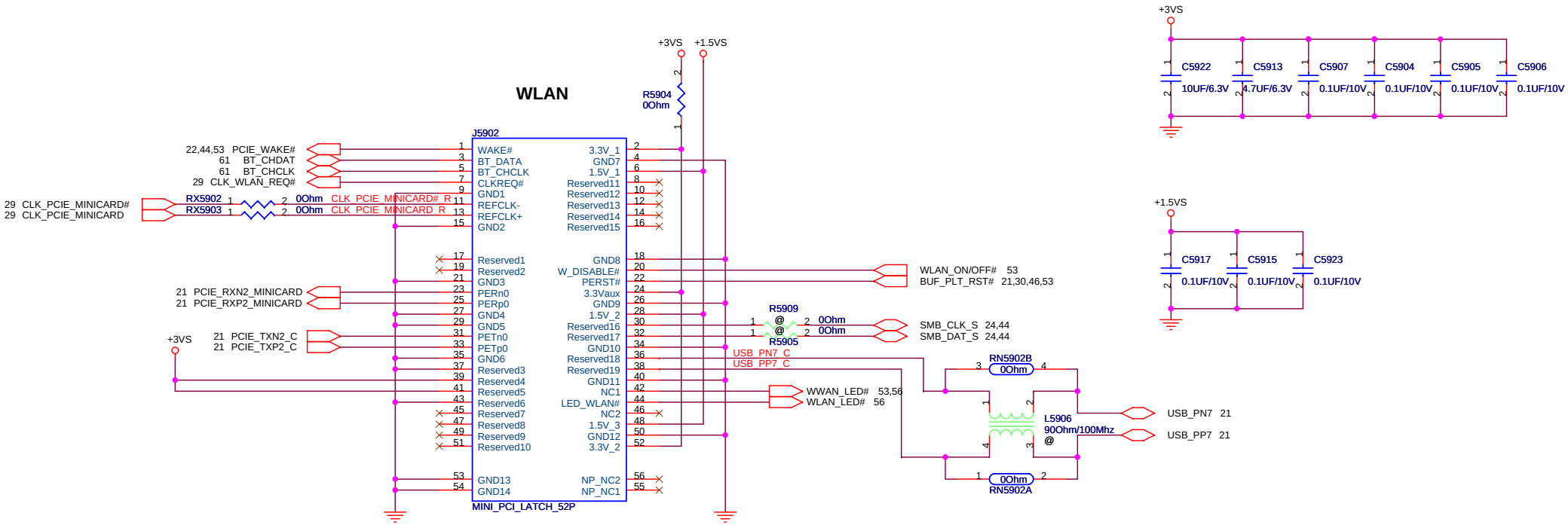




Title : DISCHARGE		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 57 of 94	

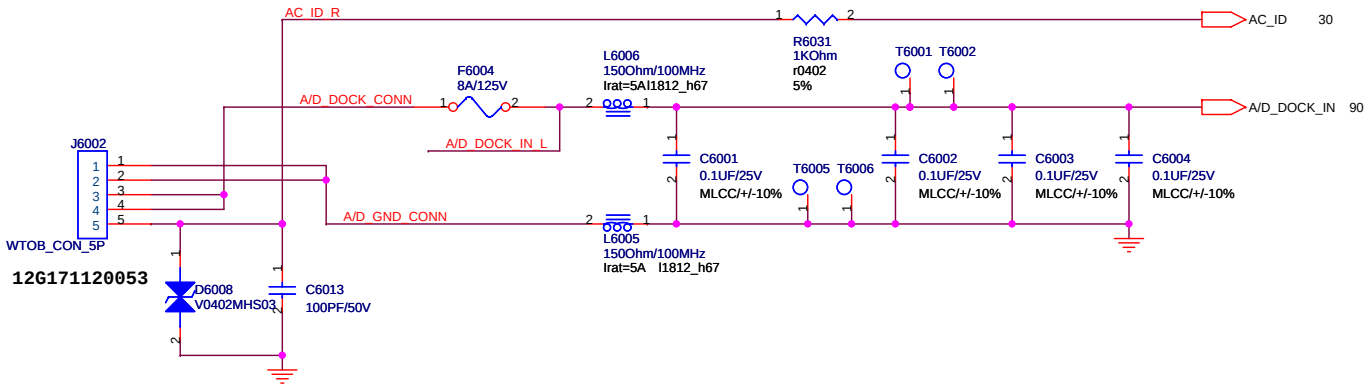


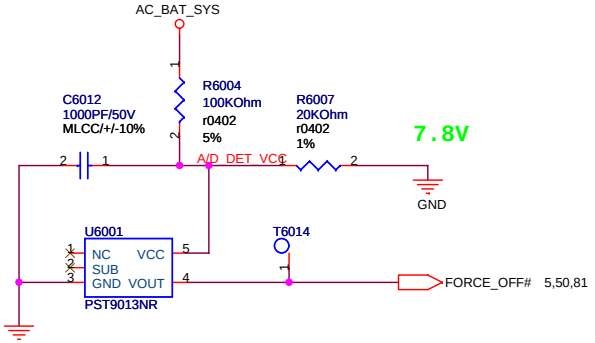
ASUS	Title : SMS	
	Engineer: Peter Lo	
Size: A	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 58 of 94	



ASUS	Title : Mini Card	
	Engineer: Peter Lo	
Size: B	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 59 of 94	

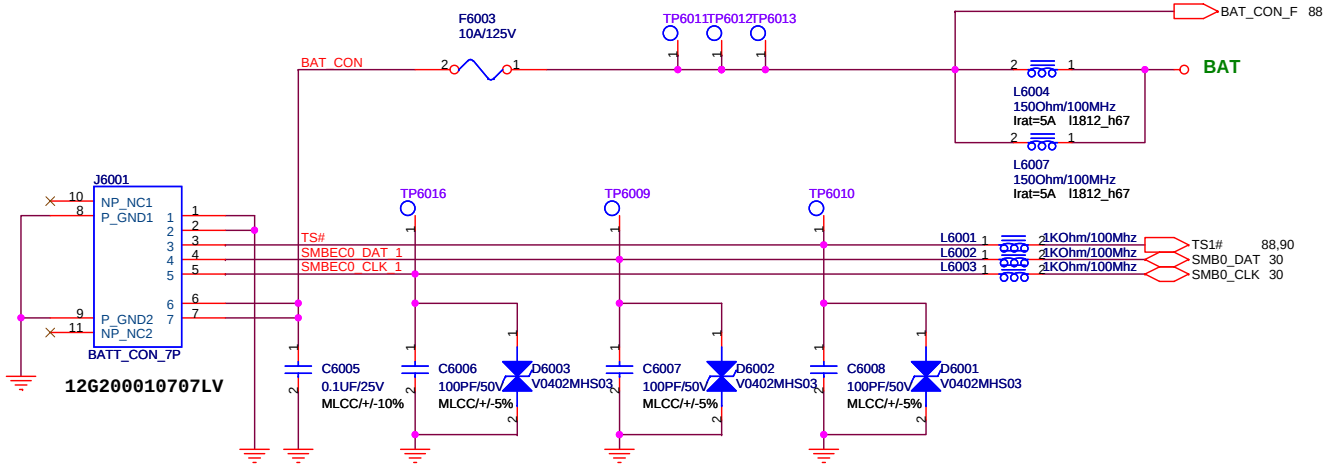
DC IN CONN





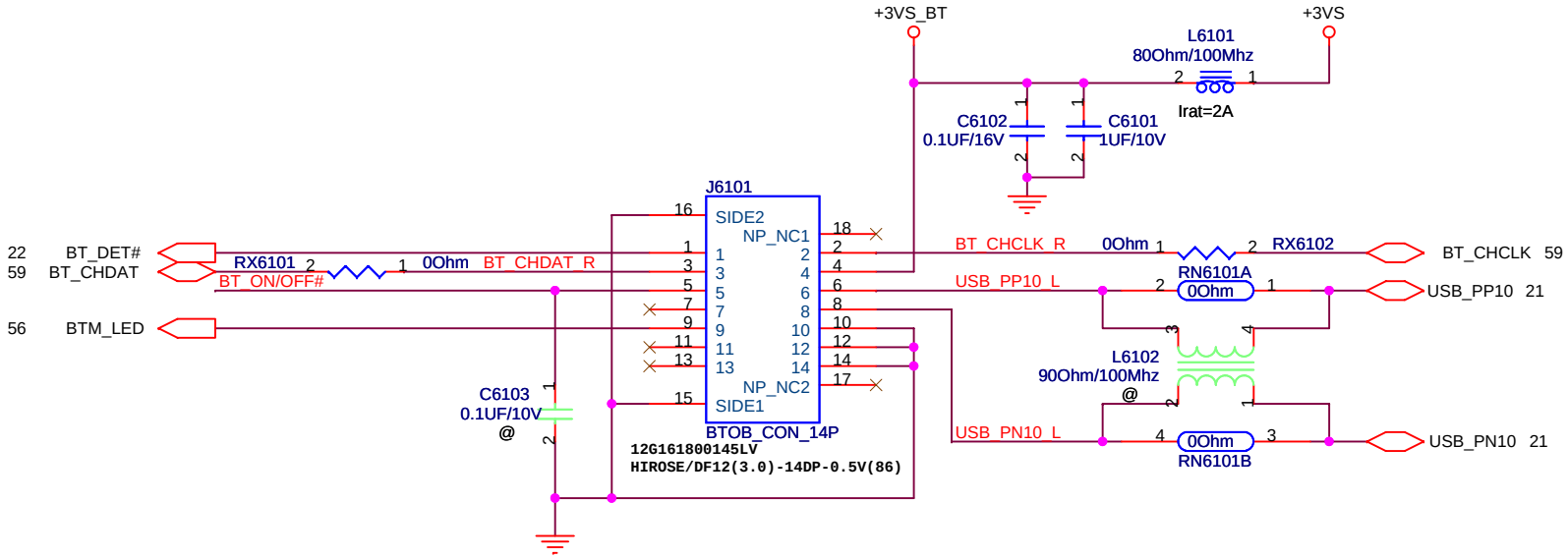
Without Battery & Pull out Adapter

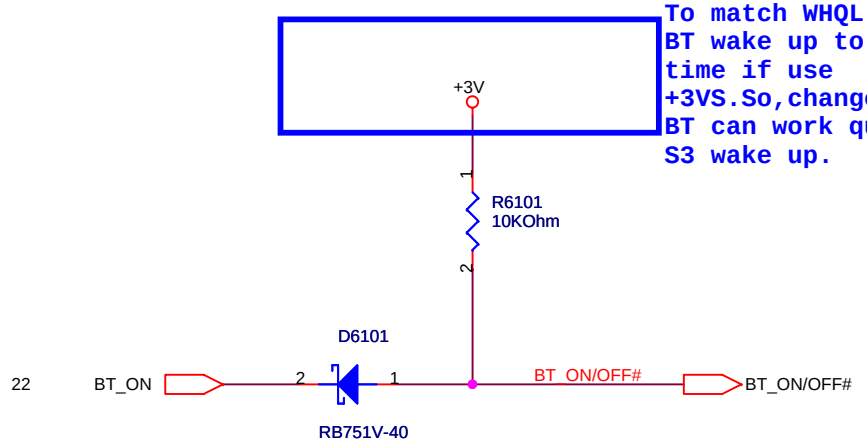
Battery CONN



Title : DC Jack & Battery CONN		
Engineer: Kevin Chang		
Size: Custom	Project Name: Rocky 30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 60 of 94	

Blue Tooth





To match WHQL test.Due to BT wake up to spend much time if use +3VS.So,change to +3V,let BT can work quickly when S3 wake up.

From GPIO27 ICH9

Title : BlueTooth		
Engineer: Peter Lo		
Size: A4	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 61 of 94	

Title :	***
Engineer:	*Peter Lo*
Size: A4	Project Name: **Rocky30**
Rev: 1.0	
Date: Thursday, October 18, 2007	Sheet 62 of 94

Title :	***
Engineer:	Peter Lo
Size: A4	Project Name: Rocky30
Rev: 1.0	
Date: Thursday, October 18, 2007	Sheet 63 of 94

Title :	
Engineer:	Peter Lo
Size: A	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
Sheet	64 of 94

CPU

@ H6513 CT276B197D138
@ H6514 CT276B197D138
@ H6515 CT276B197D138
@ H6516 CT276B197D138

CT276B197D138

TOP 5CT236B236X236D91 PTH

@ H6508 5CT236B236X236D91
@ H6517 5CT236B236X236D91
@ H6509 5CT236B236X236D91
@ H6510 5CT236B236X236D91
@ H6511 5CT236B236X236D91
@ H6512 5CT236B236X236D91
@ H6506 5CT236B236X236D91
@ H6518 5CT236B236X236D91

MCH NUT
(mirror)

H6520 U5F-M-EXPREE
H6519 U5F-M-EXPREE

CR236X236D91 PTH

@ H6507 CR236X236D91
@ H6529 CR236X236D91
@ H6504 CR236X236D91

BOT 5CT236B236X236D91 PTH

@ H6528 5CT236B236X236D91

H6530
H6531
H6526
H6527

U5F-M-EXPREE
U5F-M-EXPREE
U5F-M-EXPREE
U5F-M-EXPREE

GND_AUDIO

MINI CARD

C236D91 PTH

@ H6521 C236D91
@ H6536 C236D91
@ H6502 C236D91
@ H6503 C236D91

For Fan Stand Off
C236B189D150 PTH (mirror)

H6524 U5F-M-EXPREE
H6525 U5F-M-EXPREE

For KB Stand Off
C236B189D150 PTH

H6533 U5F-M-EXPREE

@ H6534 SMD169X169

For BT StandOff

H6546 ROCKY50-1A

TOOLING HOLE

For ICT

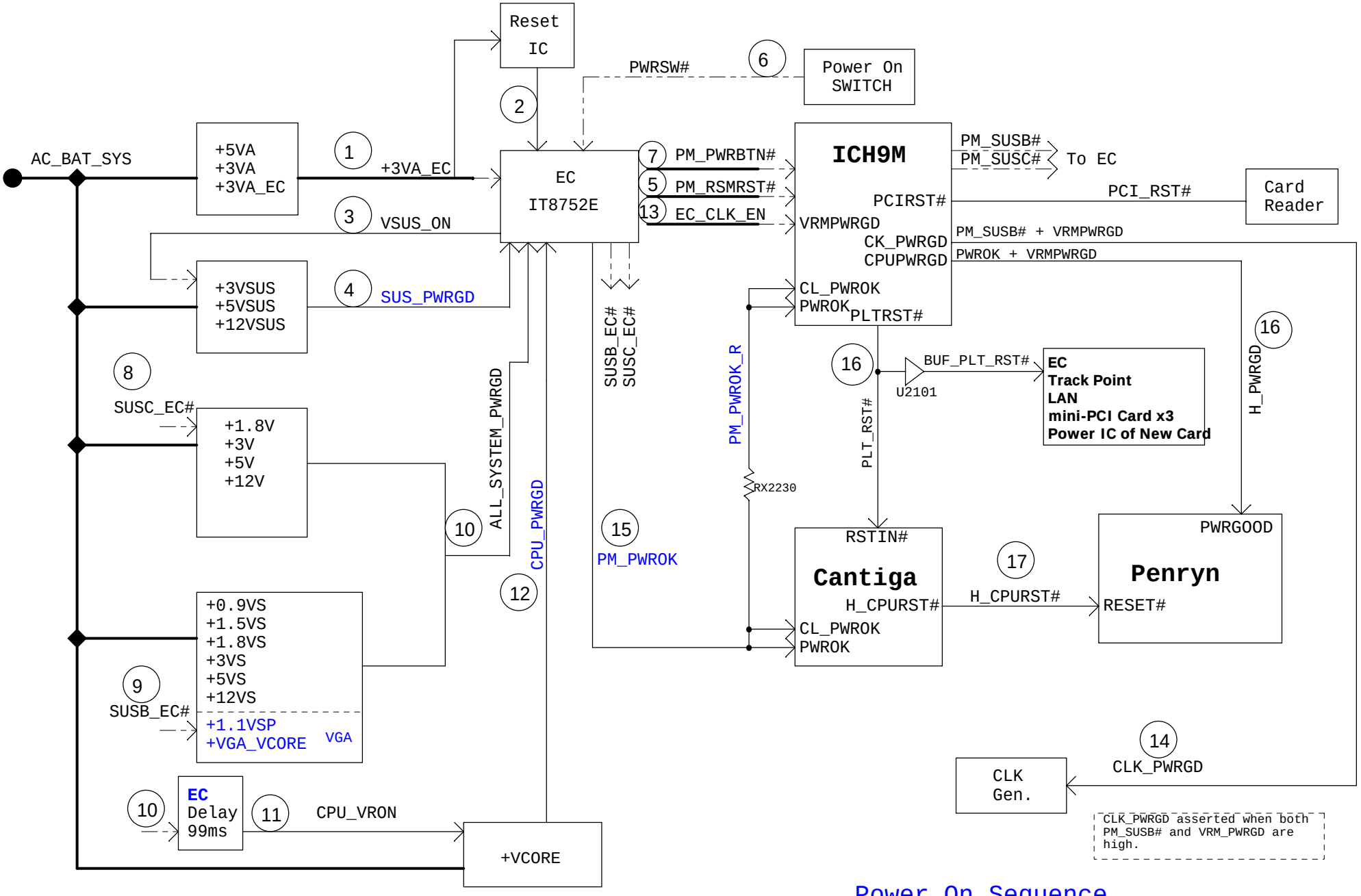
@ H6522 C103D103N
@ H6523 C103D103N
@ H6532 C103D103N

Title: MDC NUT & Hinksink NUT		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Tuesday, January 22, 2008	Sheet 65 of 94	

Title :	***
Engineer:	*Peter Lo*
Size: Custom	Project Name: **Rocky30**
Rev: 1.0	
Date: Thursday, October 18, 2007	Sheet 66 of 94

Title :	***
Engineer:	Peter Lo
Size: Custom	Project Name: Rocky30
Rev:	1.0
Date: Thursday, October 18, 2007	Sheet 67 of 94

Title :	***
Engineer:	*Peter Lo*
Size: Custom	Project Name: Rocky30
Rev: 1.0	
Date: Thursday, October 18, 2007	Sheet 68 of 94



Power On Sequence

1 → 17

ASUS	Title :	Power Sequence
	Engineer:	Peter Lo
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, November 05, 2007	Sheet 69 of 94	

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 70 of 94

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 71 of 94

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 72 of 94

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 73 of 94

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 74 of 94

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 75 of 94

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 76 of 94

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 77 of 94

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 78 of 94

Title :

Engineer: Peter Lo

Size	Project Name	Rev
A	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 79 of 94

IMVP6 CPU VCORE REGULATOR

3.3V level logic level: DPRSLPVR, SHDN#

1.05V level logic: VID, PSI#, DPRSTP#

POUT=(VCSN2-VGNDS)x(CSP1-CNS1+CSP2-CSN2)/16.67mV

FSW=297.8kHz

Slewrate=12.5mV/us

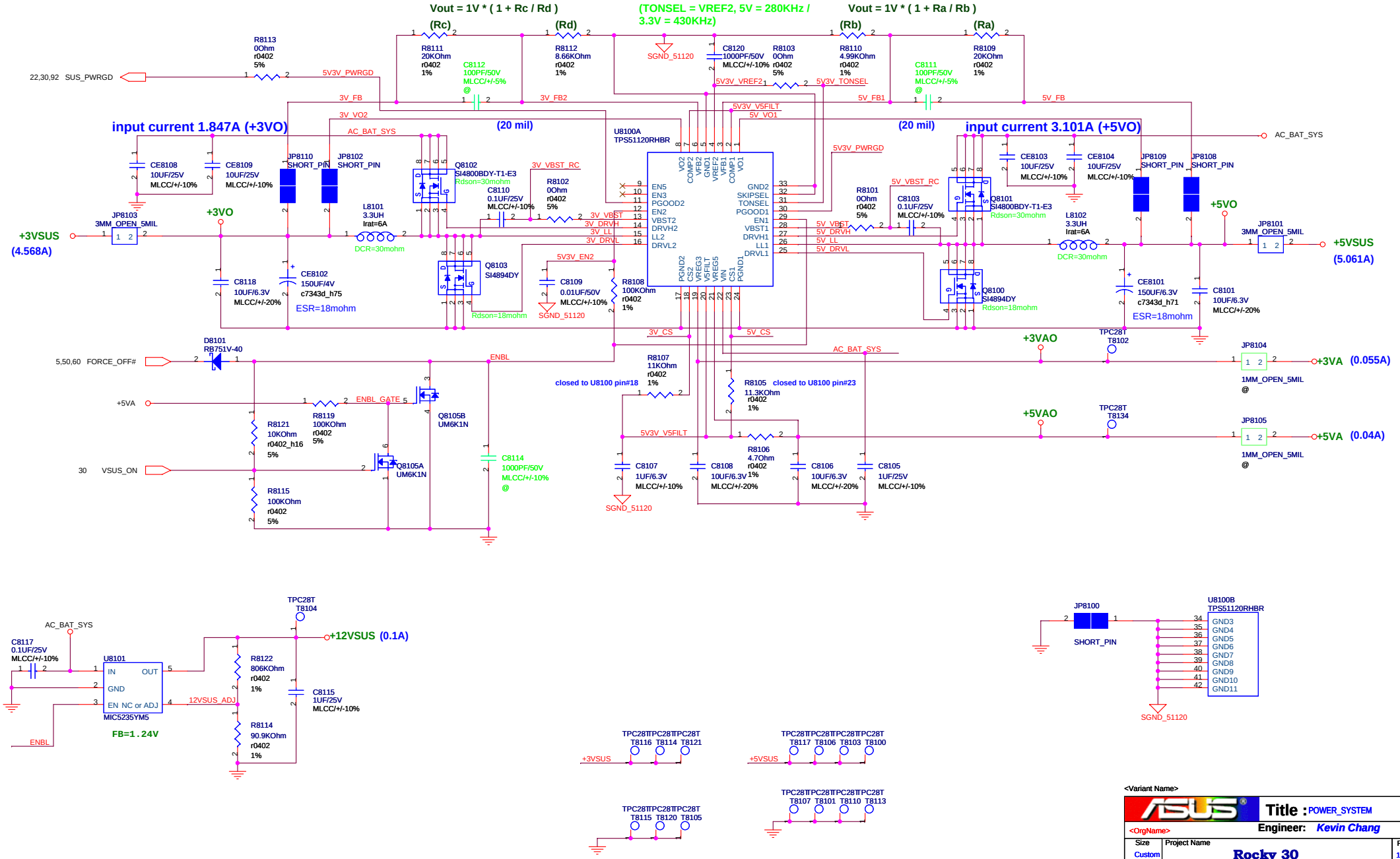
VPS=-2.1mV/A

Max input ripple: 5.59A

Max input ripple: 5.59A

Title :	POWER_VCORE	
<OrgName>	Engineer:	Kevin Chang
Size: Custom	Project Name: Rocky 30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 80 of 94	

+5V / +3.3V POWER SUPPLY



<Variant Name>

<OrgName>

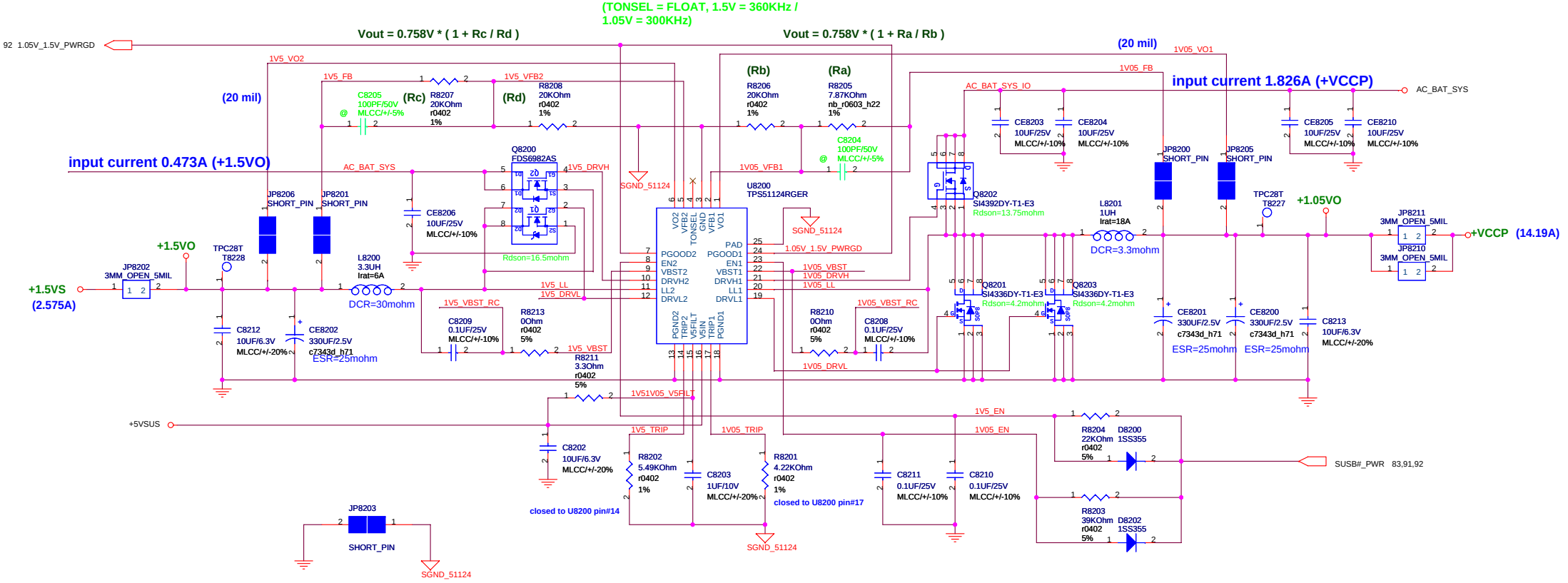
Title : POWER_SYSTEM

Engineer: Kevin Chang

Size	Project Name	Rev
Custom	Rocky 30	1.0

Date: Monday, February 04, 2008 Sheet 81 of 94

+1.5VS / +VCCP POWER SUPPLY



<Variant Name>

Title : POWER_I/O_1.5VS & 1.05VS

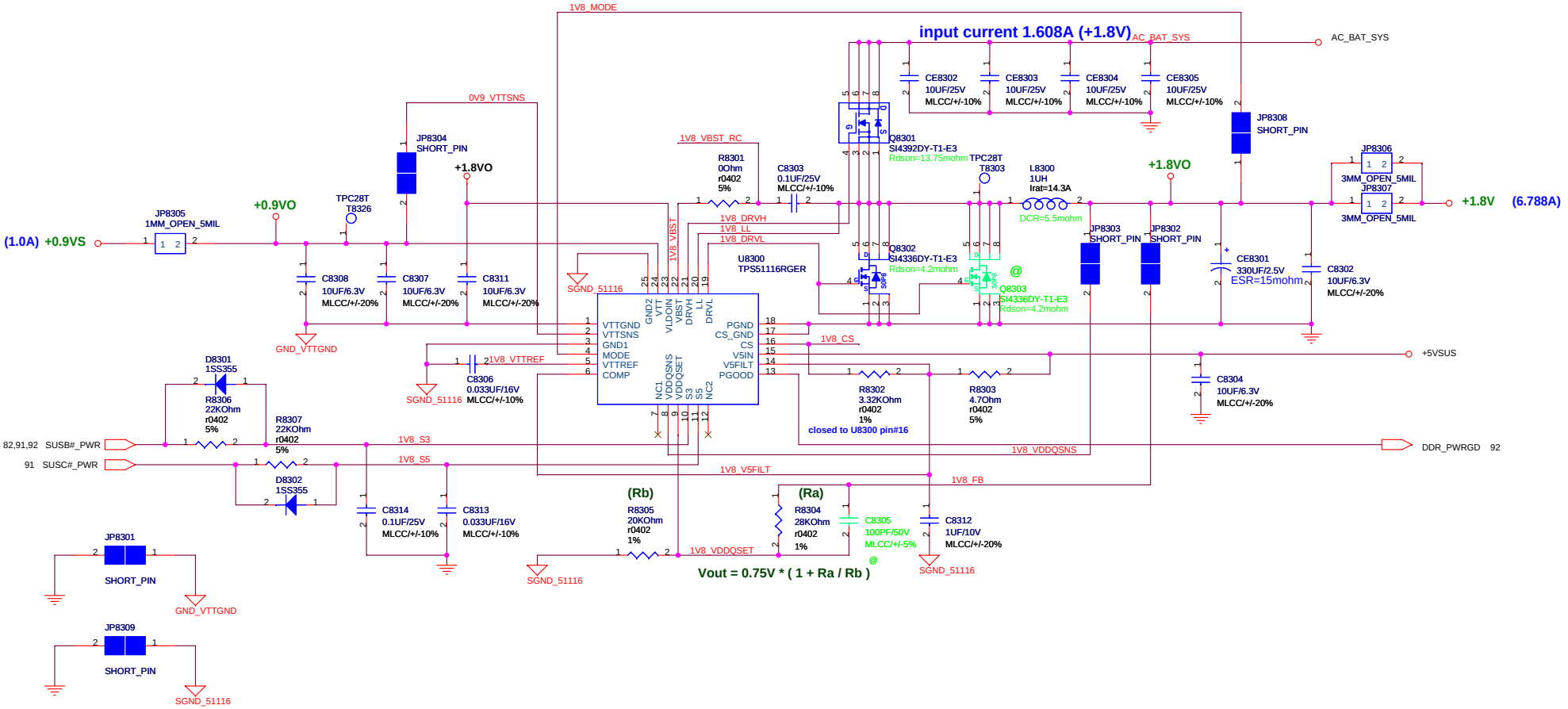
<OrgName>

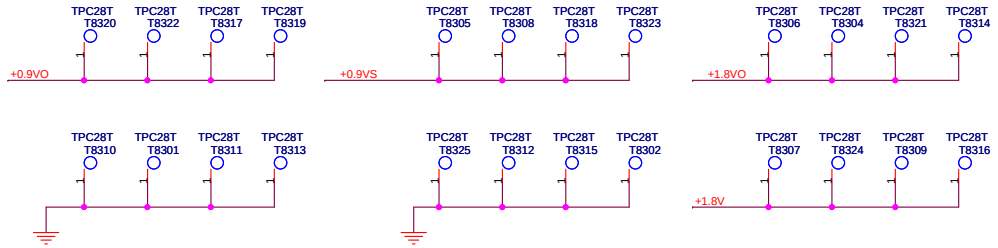
Engineer: Kevin Chang

Size	Project Name	Rev
Custom	Rocky 30	1.0

Date: Monday, February 04, 2008 Sheet 82 of 94

+1.8V / +0.9VS POWER SUPPLY





<Variant Name>

Title : POWER_I/O_DDR & VTT

<OrgName> Engineer: Kevin Chang

Size	Project Name	Rev
Custom	Rocky 30	1.0

Date: Monday, February 04, 2008 Sheet 83 of 94

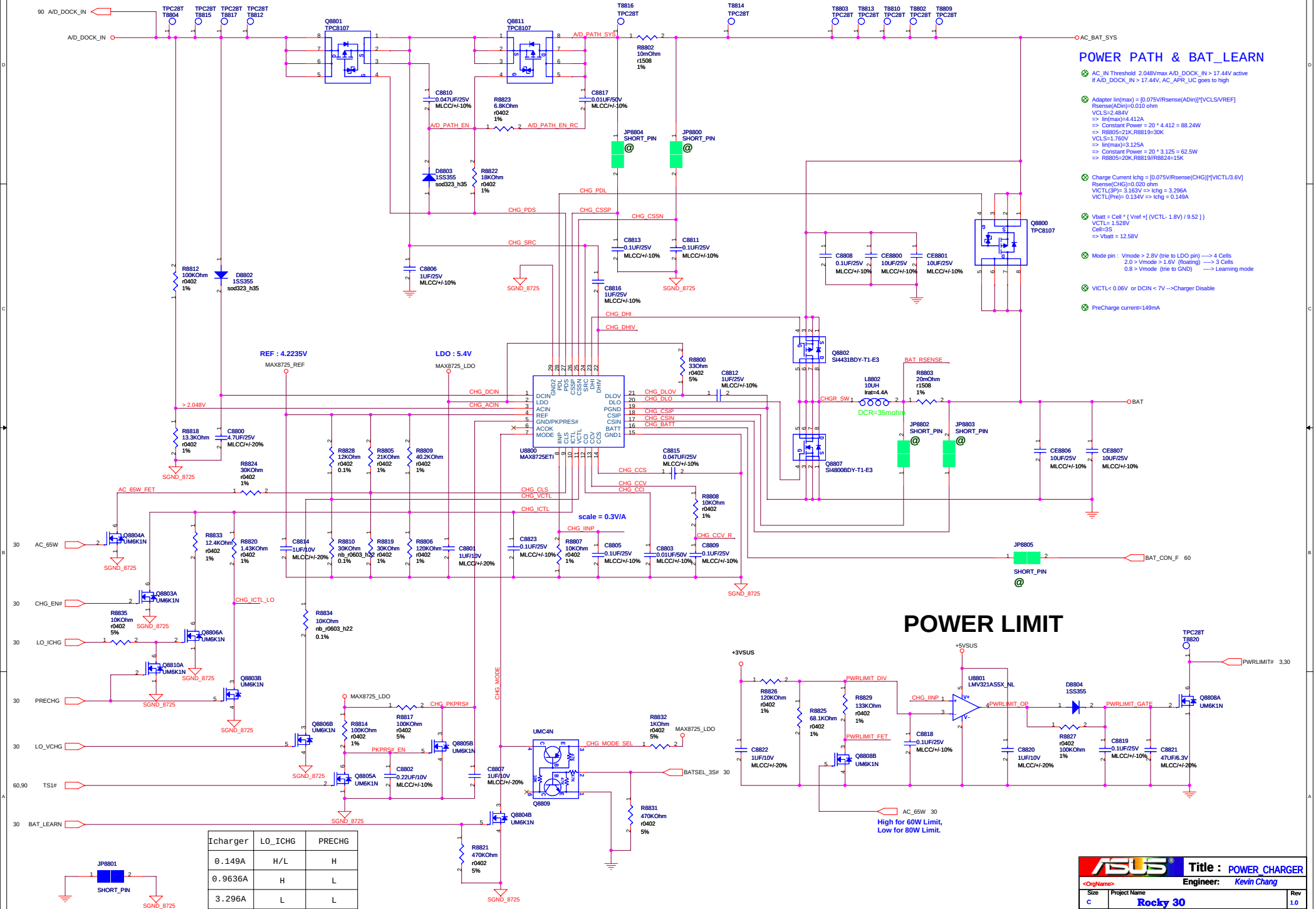
Title : PWR_-****		
Engineer: <OrgName>		
Size: A4	Project Name: Rocky30	Rev: 1.0
Date: Saturday, January 26, 2008	Sheet 84 of 94	

Title :	
Engineer:	Kevin Chang
<OrgName>	
Size: Custom	Project Name: Rocky30
Rev: 1.0	
Date: Friday, January 11, 2008	Sheet 85 of 94

Title : PWR_-****		
<OrgName>	Engineer: Kevin Chang	
Size: A4	Project Name: Rocky30	Rev: 1.0
Date: Friday, January 11, 2008	Sheet 86 of 94	

Title : POWER_SHUTDOWN#				
Engineer: <OrgName>				
Size: A4	Project Name: Rocky30			Rev: 1.0
Date: Saturday, January 26, 2008		Sheet 87 of 94		

BATTERY CHARGER



Icharger	LO_ICHG	PRECHG
0.149A	H/L	H
0.9636A	H	L
3.296A	L	L

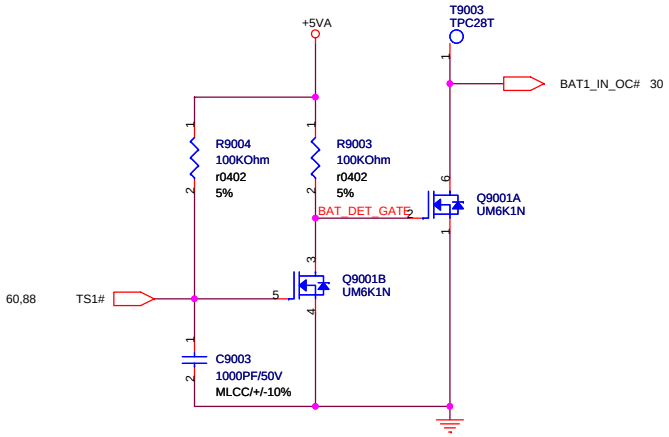
POWER PATH & BAT_LEARN

- AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active
  If A/D_DOCK_IN > 17.44V, AC_APR_UC goes to high
- Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
  Rsense(ADin)=0.010 ohm
  VCLS=2.484V
  => Iin(max)=4.412A
  => Constant Power = 20 * 4.412 = 88.24W
  => R8805=21K,R8819=30K
  VCLS=1.760V
  => Iin(max)=3.125A
  => Constant Power = 20 * 3.125 = 62.5W
  => R8805=20K,R8819//R8824=15K
- Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
  Rsense(CHG)=0.020 ohm
  VICTL(3P)= 3.163V => Ichg = 3.296A
  VICTL(Pre)= 0.134V => Ichg = 0.149A
- Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }
  VCTL= 1.528V
  Cell=3S
  => Vbatt = 12.58V
- Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
  2.0 > Vmode > 1.6V (floating) ----> 3 Cells
  0.8 > Vmode (trie to GND) ----> Learning mode
- VICTL< 0.06V or DCIN < 7V -->Charger Disable
- PreCharge current=149mA

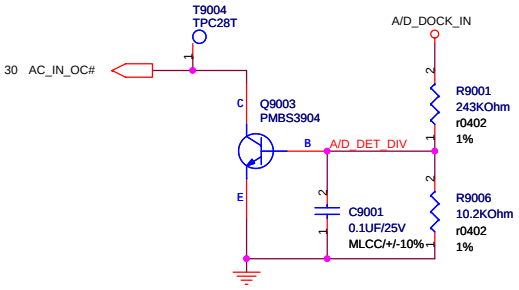
POWER LIMIT

Title :	TFT-LCD DRIVE
<OrgName>	Engineer:
Size: A4	Project Name: Rocky30
Rev: 1.0	
Date: Friday, January 11, 2008	Sheet 89 of 94

BATTERY IN DETECT

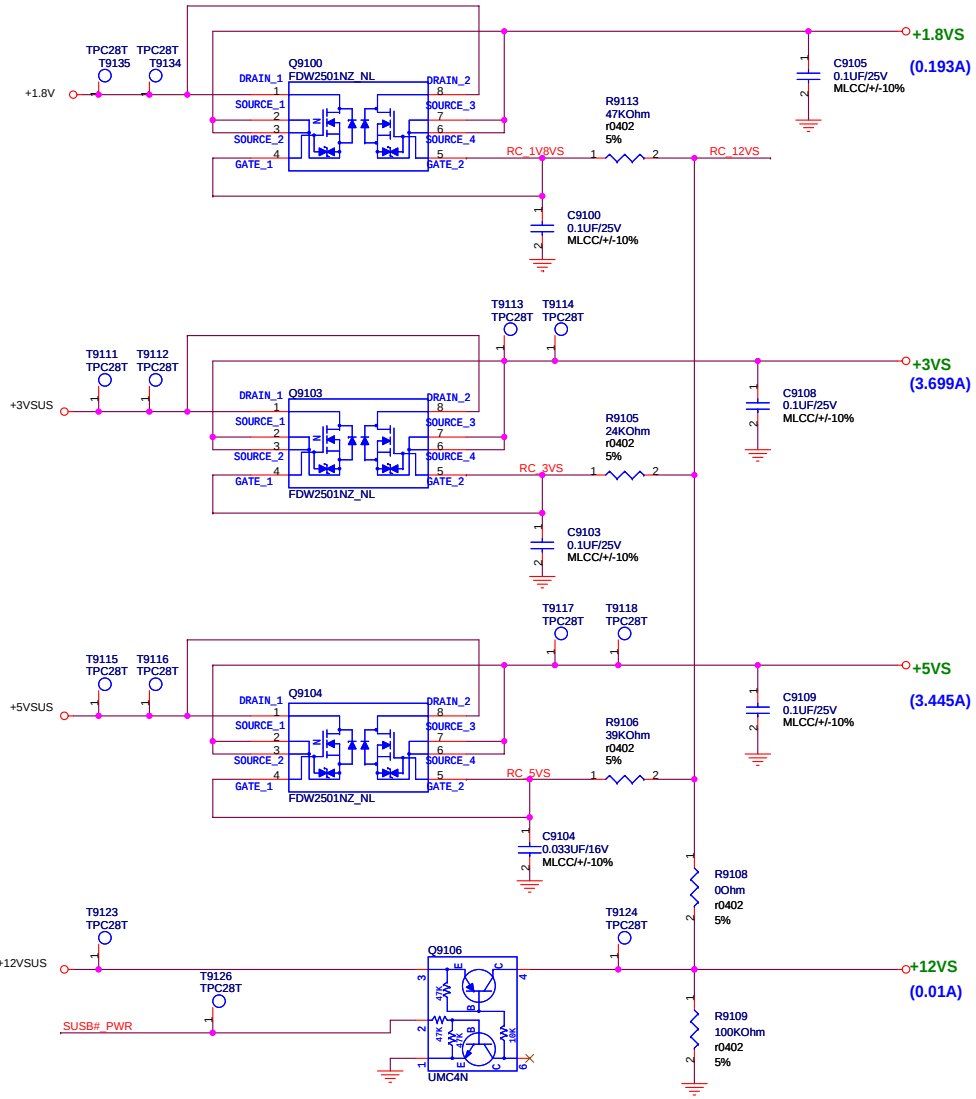


ADAPTER IN DETECT

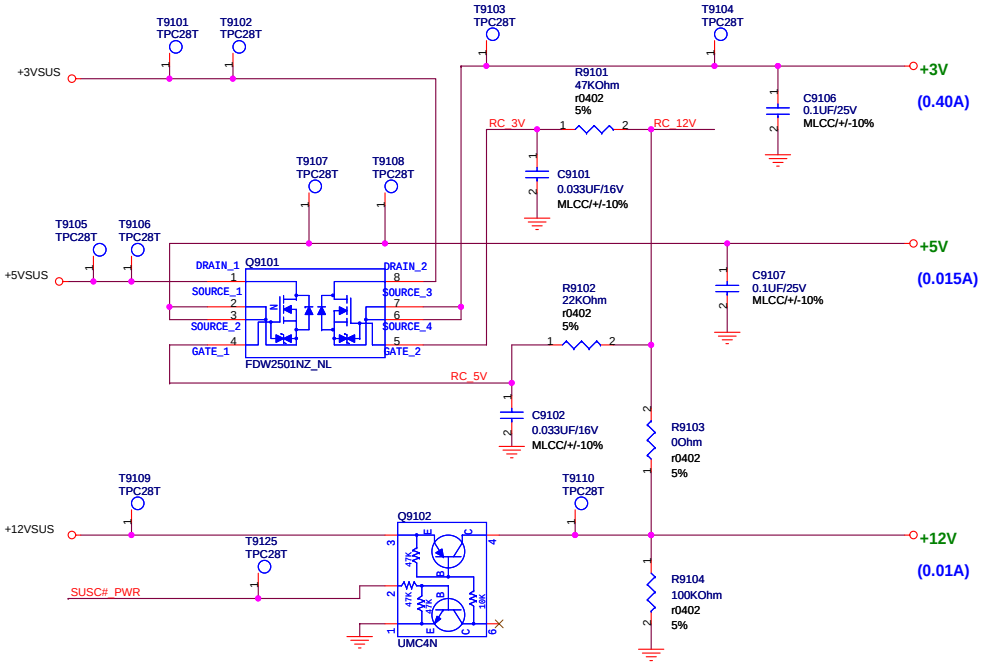


Title : POWER_DETECT		
<OrgName>	Engineer: Kevin Chang	
Size: A3	Project Name: Rocky 30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 90 of 94	

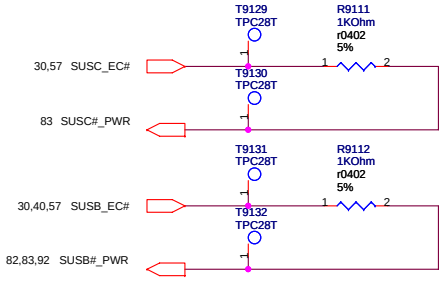
SUSB#_PWR Load SW



SUSC#_PWR Load SW

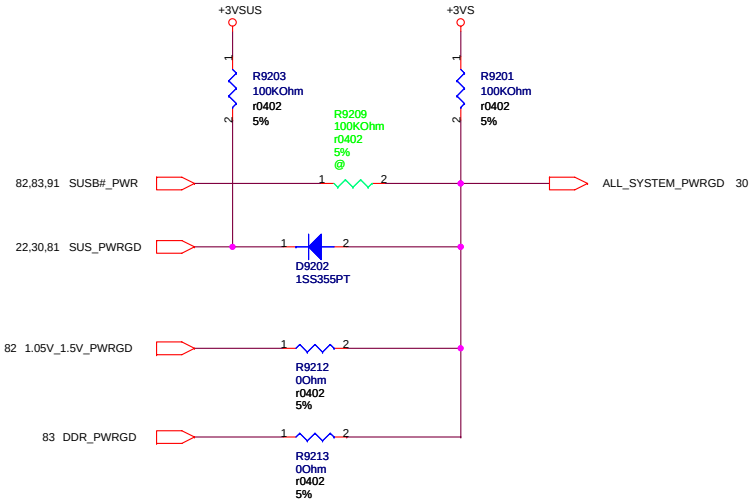


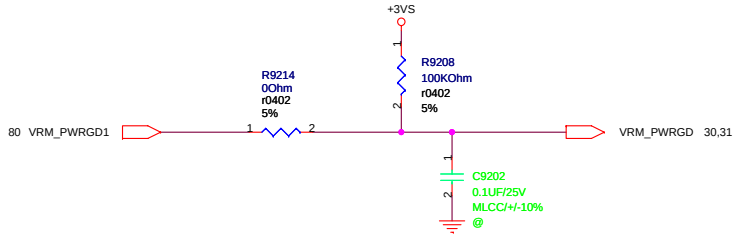
Enable Signal



<OrgName>	Title : POWER_LOAD SWITCH	
	Engineer: Kevin Chang	
Size: Custom	Project Name: Rocky 30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 91 of 94	

POWER GOOD DETECTER





Title : POWER_PROTECT		
Engineer: Kevin Chang		
<OrgName>		
Size: Custom	Project Name: Rocky 30	Rev: 1.0
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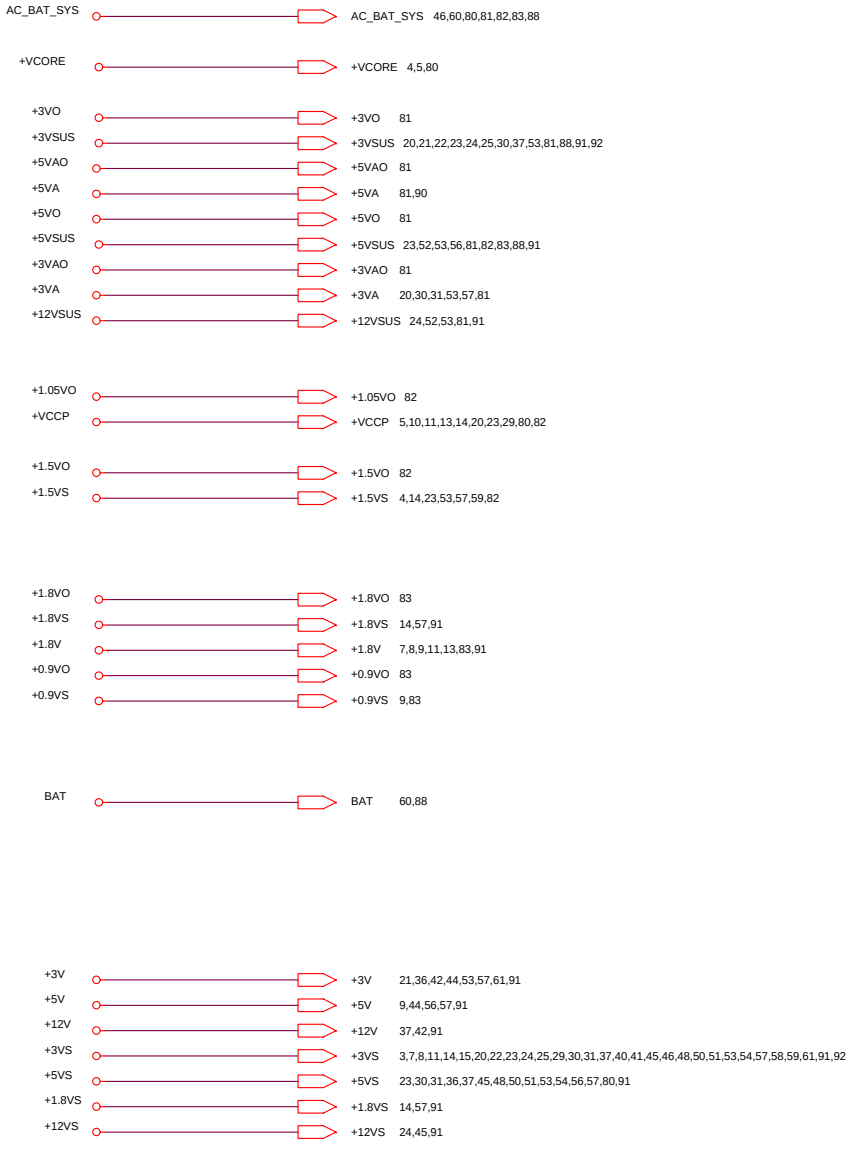

ASUS	Title : POWER_SIGNAL	
<OrgName>	Engineer: Kevin Chang	
Size: Custom	Project Name: Rocky 30	Rev: 1.0
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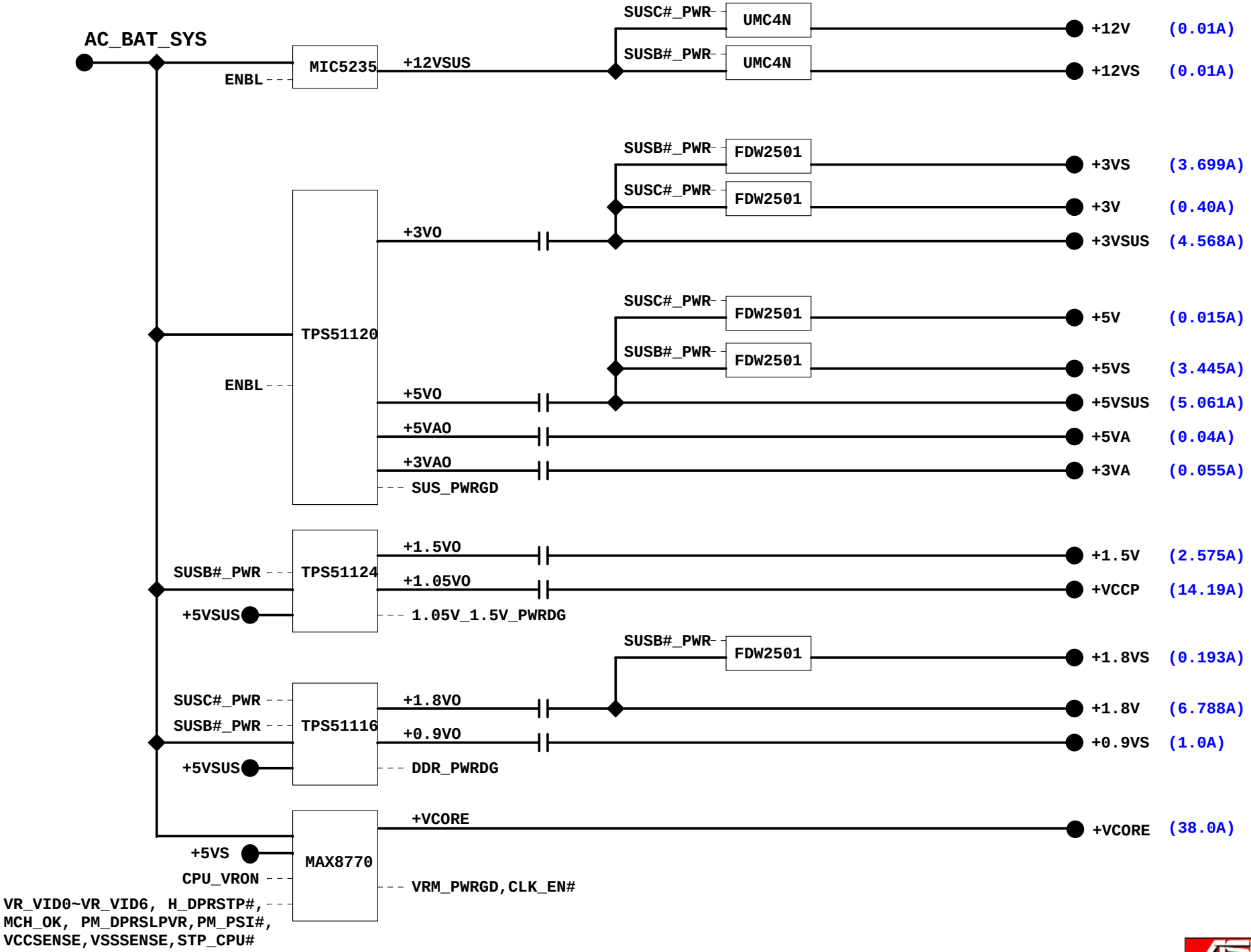

ASUS	Title : POWER_FLOWCHART		
<OrgName>	Engineer: Kevin Chang		
Size: Custom	Project Name: Rocky 30		Rev: 1.0
Date: Saturday, January 26, 2008	Sheet 94 of 94		