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Compal Confidential

EBQ10 LA-2741 Schematics Document

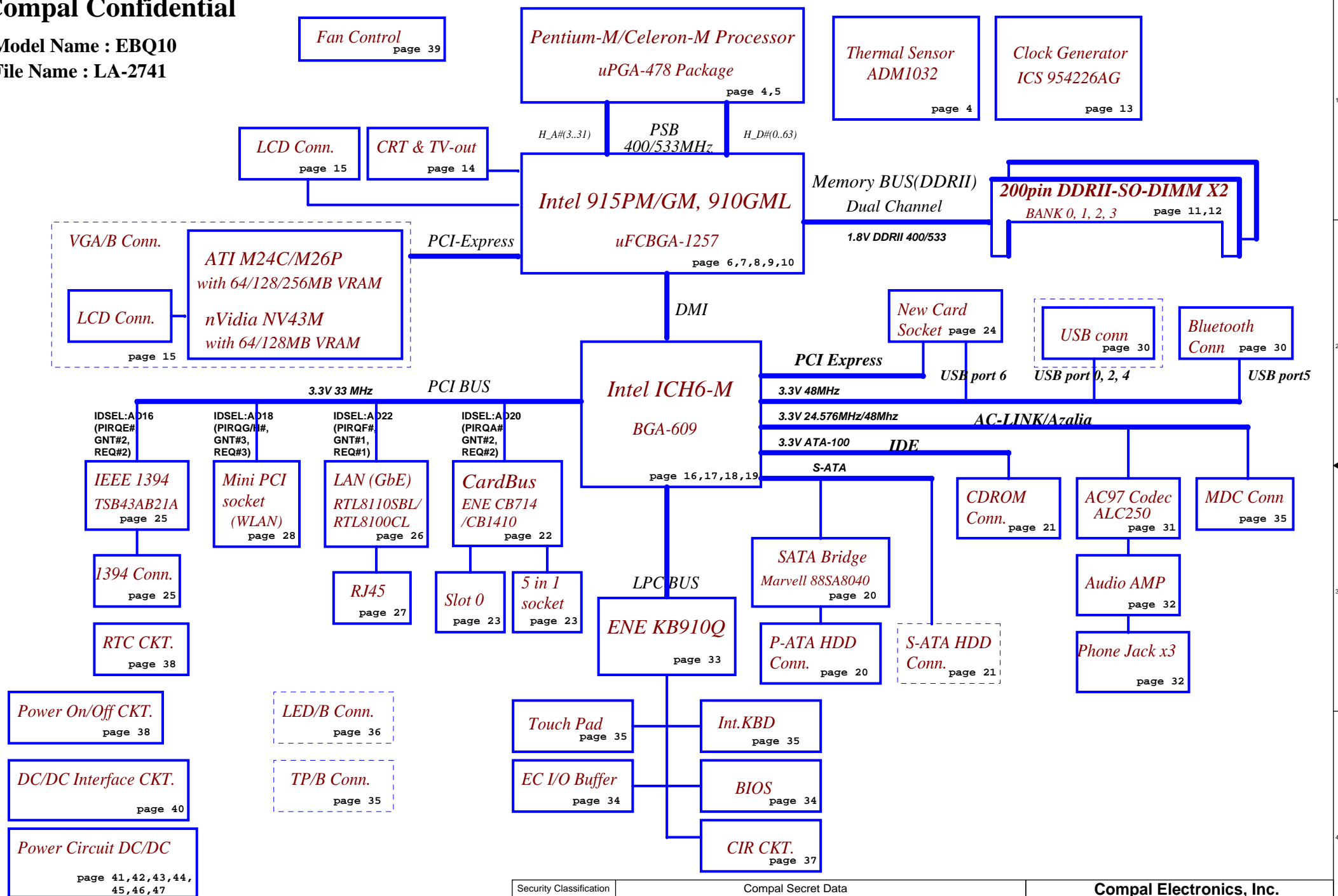
Intel Dothan with 915PM(GM)/910GML + DDRII + ICH6M
(nVidia NV43M or ATi M24/M26)

2005-03-25

REV: 0.3

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				Sheet 1 of 49	EBQ10 LA-2741

Model Name : EBQ10
File Name : LA-2741



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Issued Date	2005/03/25	Deciphered Date	2006/03/25	Title Block Diagram		
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN	AD17	1	PIRQF
Mini-PCI(WLAN)	AD18	3	PIRQG/PORQH
Mini-PCI(TV-Tuer)	AD19	4	PIRQH/PORQA

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b		

EC SM Bus2 address

ICH6M SM Bus address

Device	Address
Clock Generator (ICS 954226)	1101 001Xb
DDR DIM#0	1001 000Xb
DDR DIM#2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

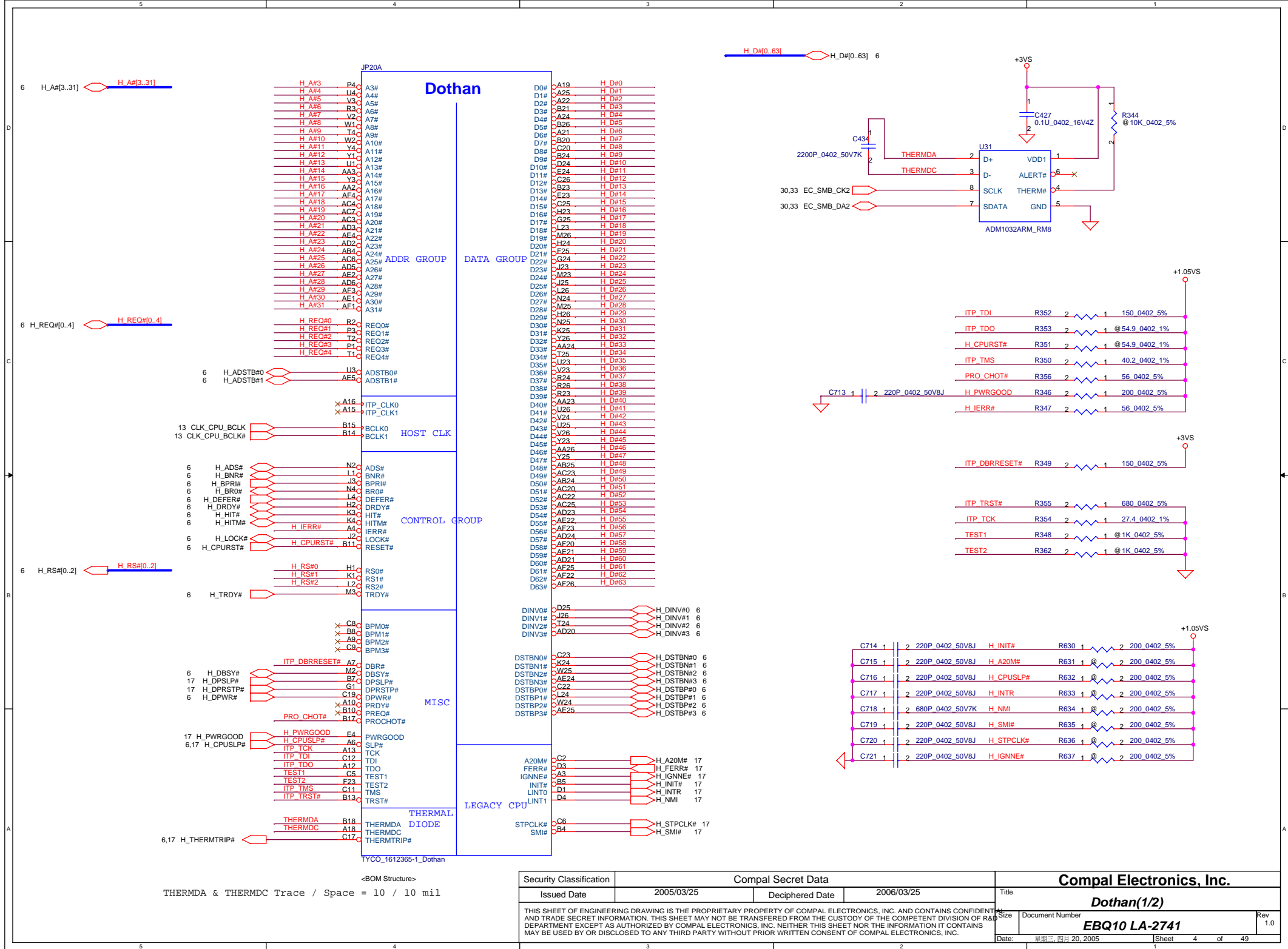
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
VGA	GM@ PM@
Card Reader	5IN1@
Giga LAN	8100C@ 8110S@
New Card	NEWCARD@
IEEE1394	1394@
TV Tuner	TUNER@
INT MIC.	MIC@
KILL SW	WLAN@
CIR	CIR@
HW EQ	EQ@ NOEQ@

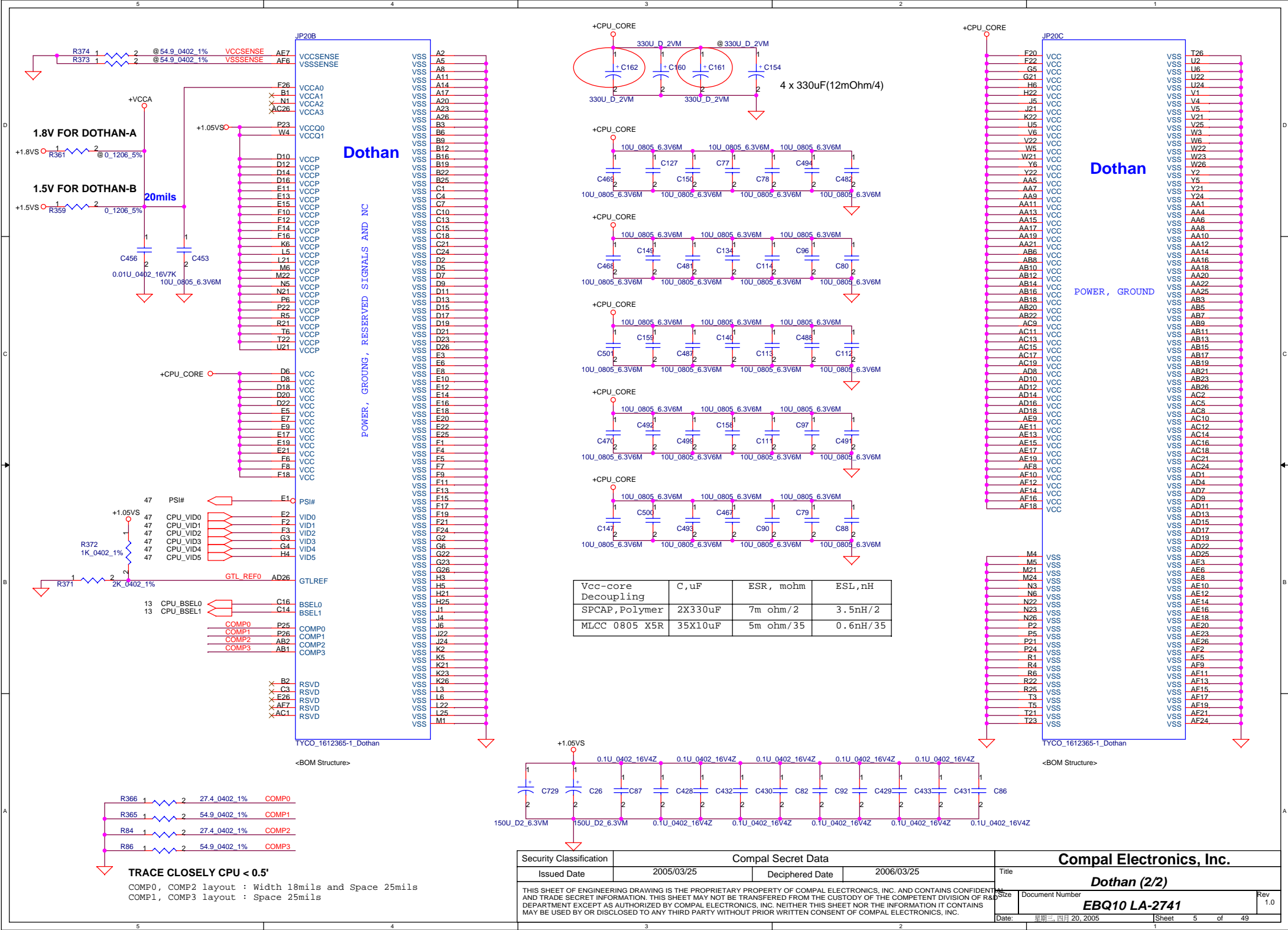
SKU ID Table

SKU ID	SKU
0	
1	
2	
3	
4	
5	
6	
7	



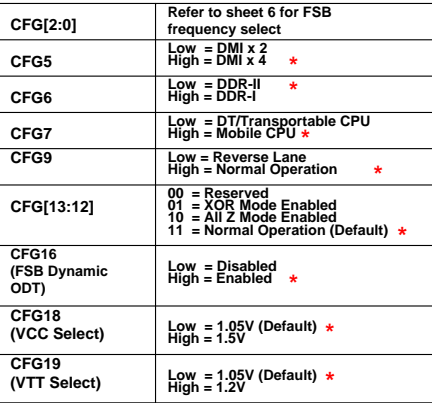
<BOM Structure>
THERMDA & THERMDC Trace / Space = 10 / 10 mil

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								Dothan(1/2)		
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Vcc-core Decoupling	C, uF	ESR, mohm	ESL, nH
SPCAP, Polymer	2X330uF	7m ohm/2	3.5nH/2
MLCC 0805 X5R	35X10uF	5m ohm/35	0.6nH/35

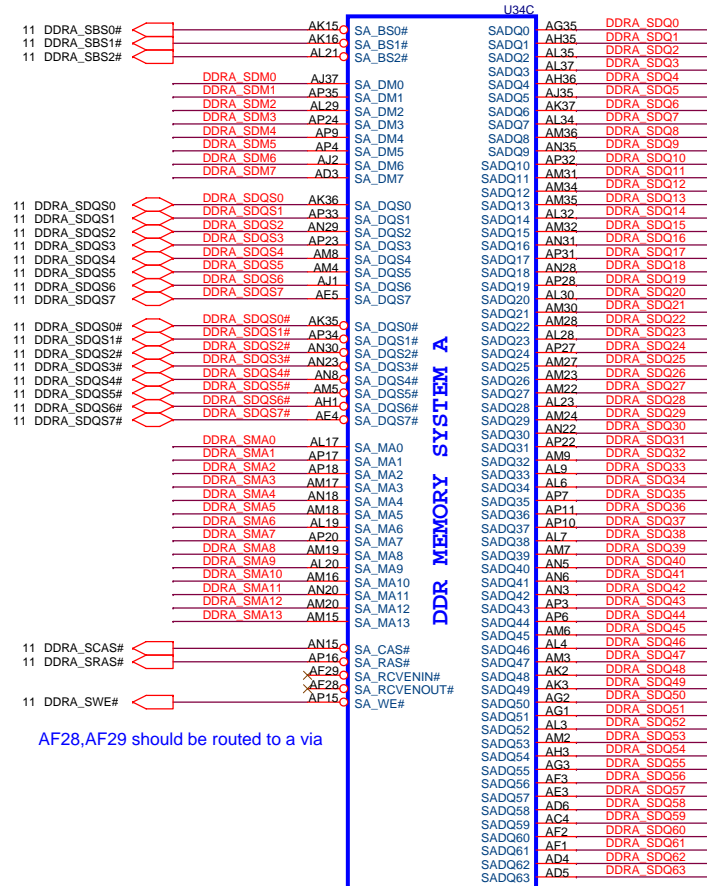
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11 DDRA_SDQ[0..63] <-- DDRA_SDQ[0..63]
11 DDRA_SDM[0..7] <-- DDRA_SDM[0..7]
11 DDRA_SMA[0..13] <-- DDRA_SMA[0..13]

12 DDRB_SDQ[0..63] <-- DDRB_SDQ[0..63]
12 DDRB_SDM[0..7] <-- DDRB_SDM[0..7]
12 DDRB_SMA[0..13] <-- DDRB_SMA[0..13]



DDR MEMORY SYSTEM A

915GM@ ALVISO_BGA1257

AF28,AF29 should be routed to a via

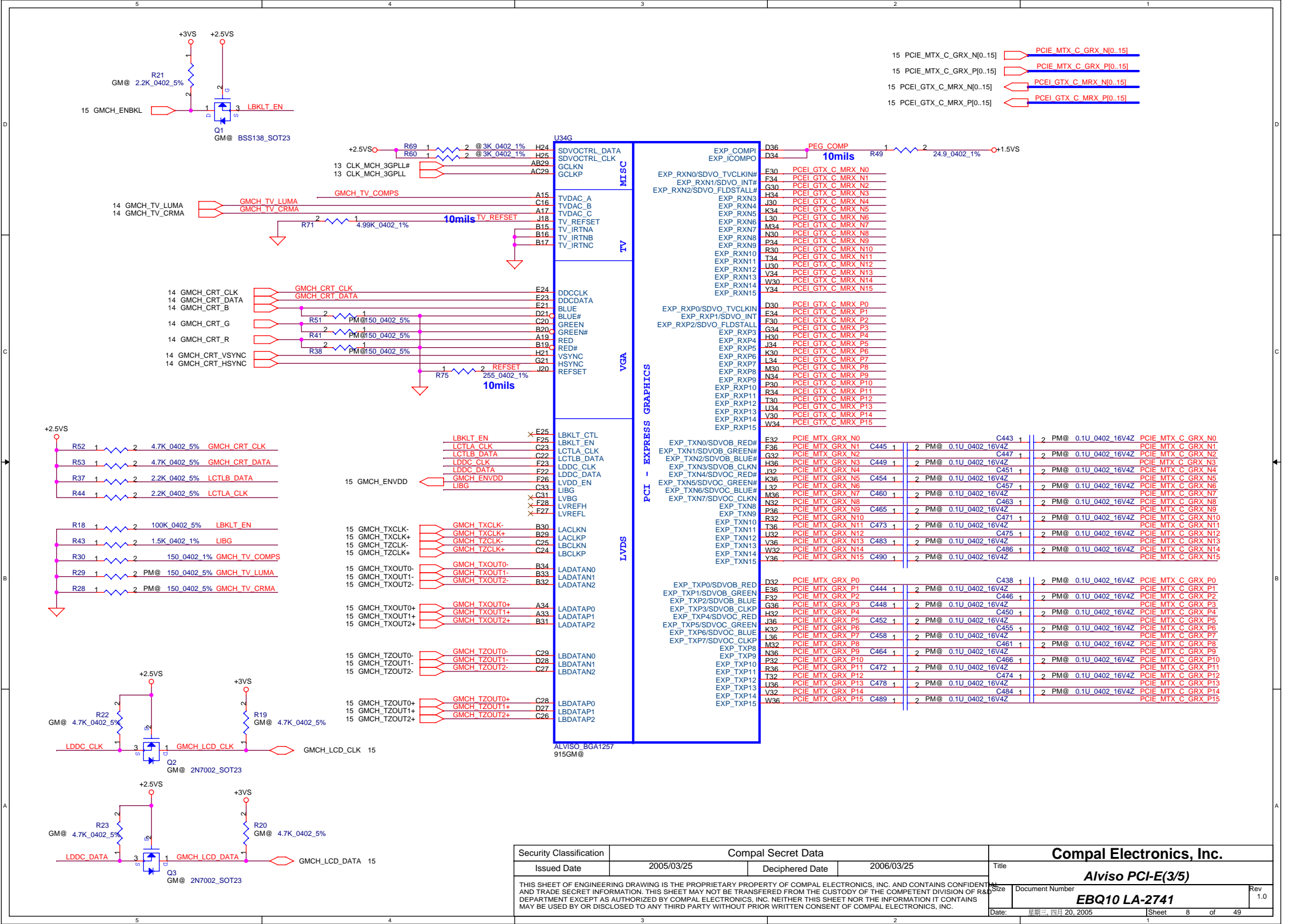


DDR SYSTEM MEMORY B

915GM@ ALVISO_BGA1257

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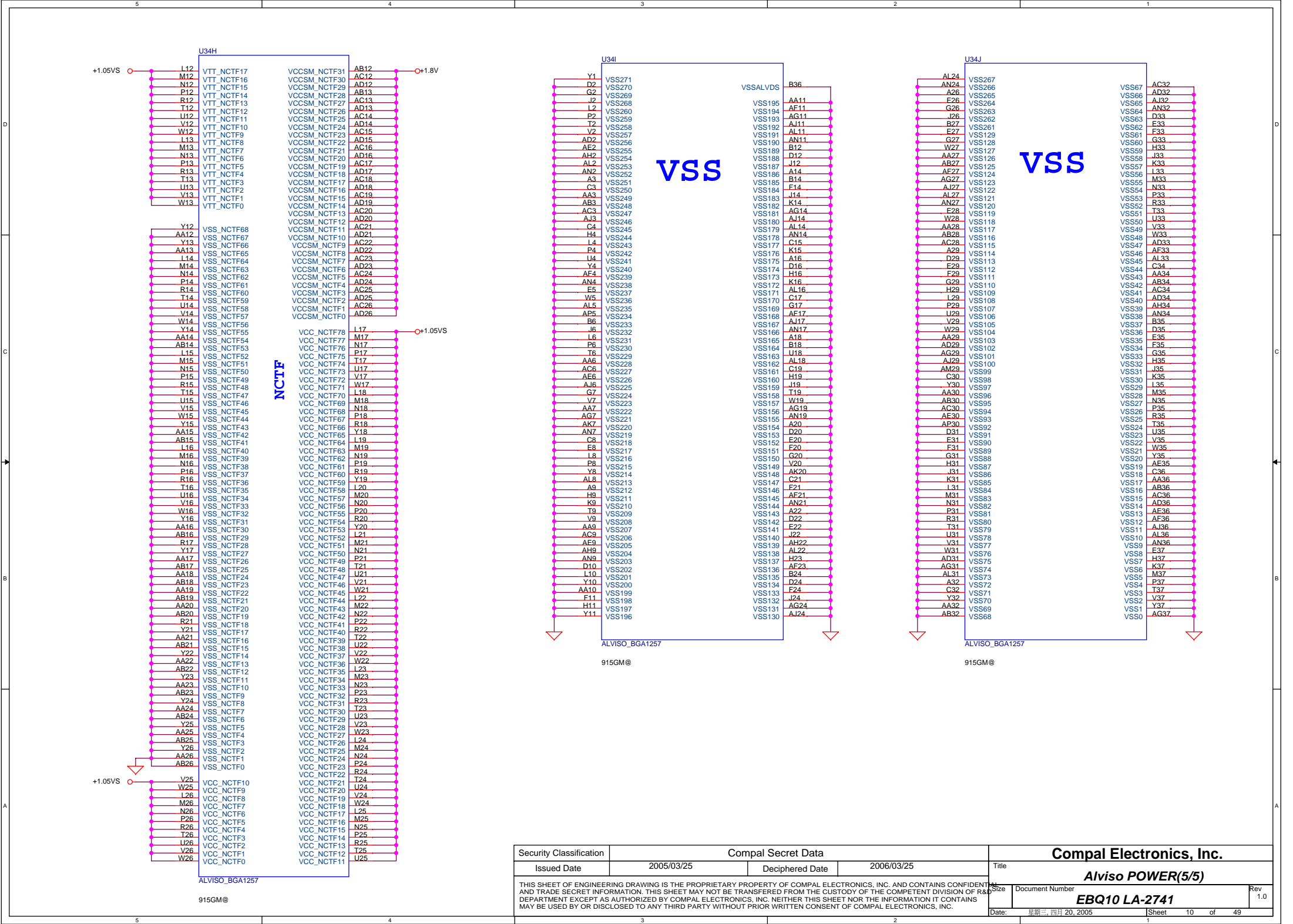
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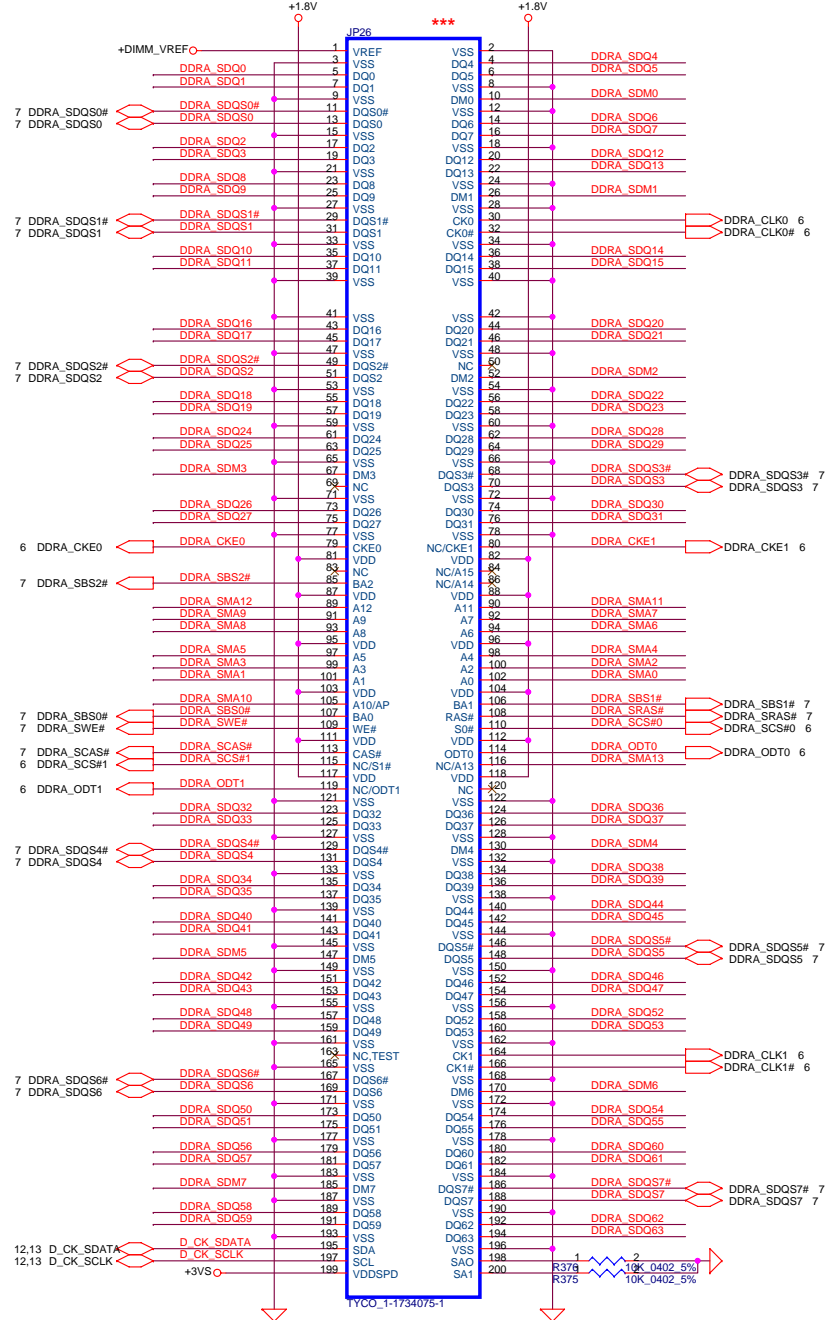




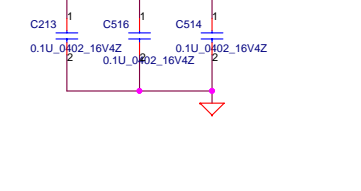
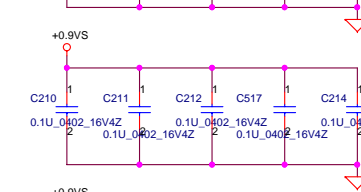
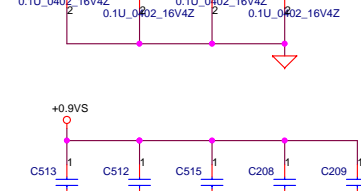
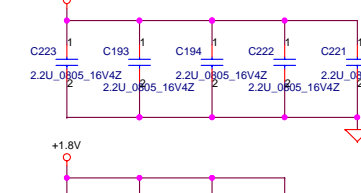
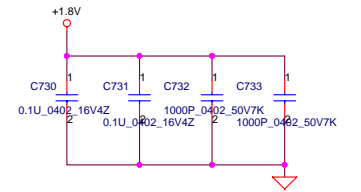
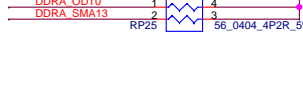
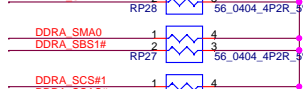
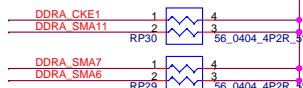
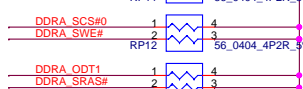
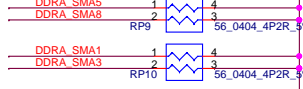
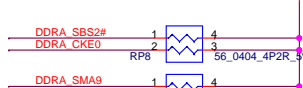
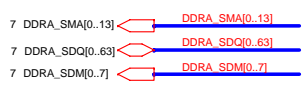
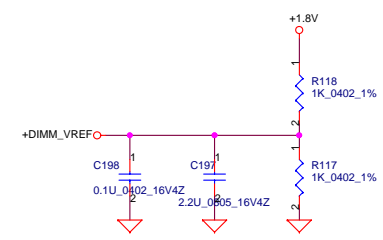
Compal Electronics, Inc.
Alviso POWER(4/5)

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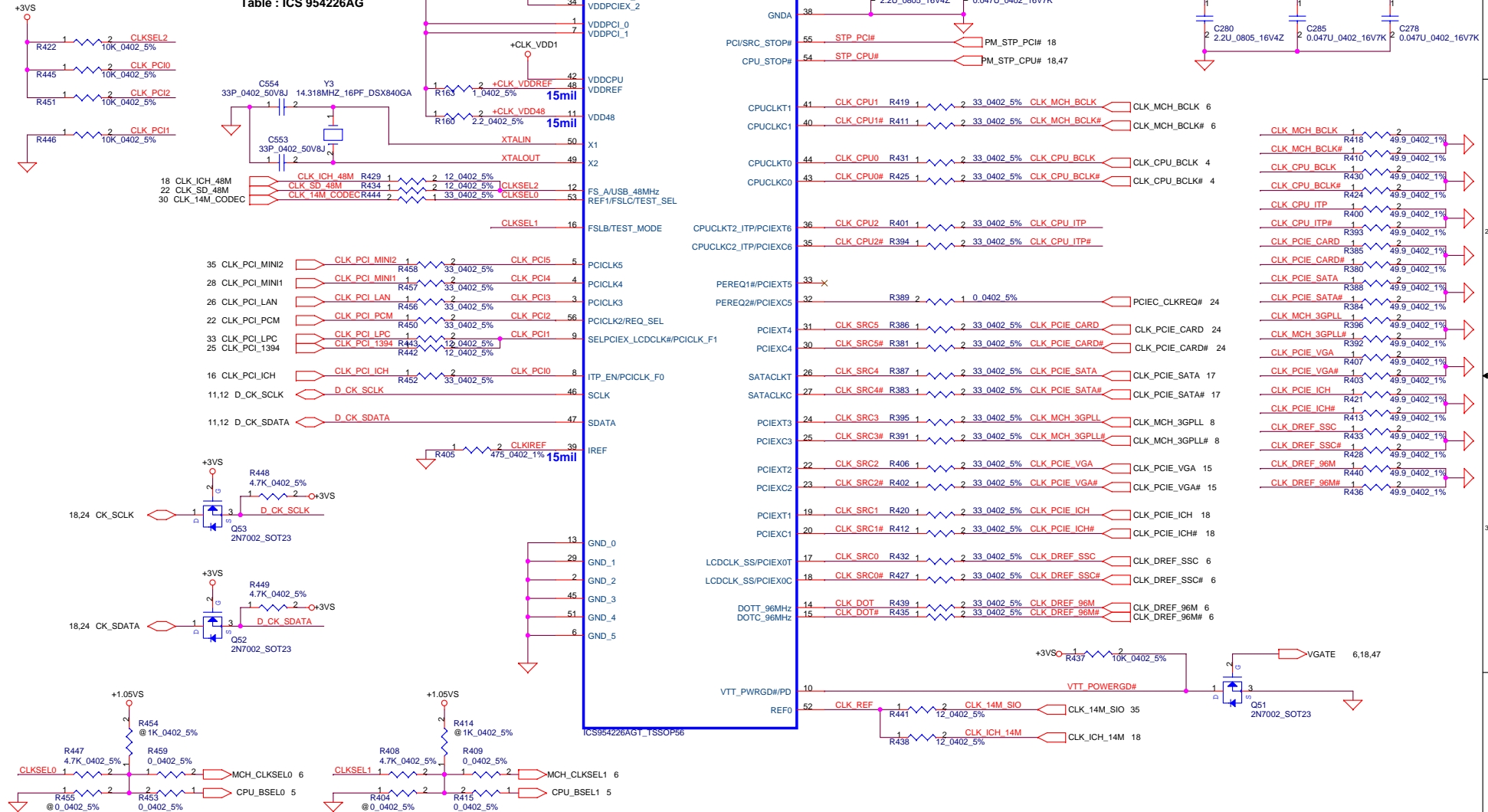
DIMM0 STD H:5.2mm (BOT)



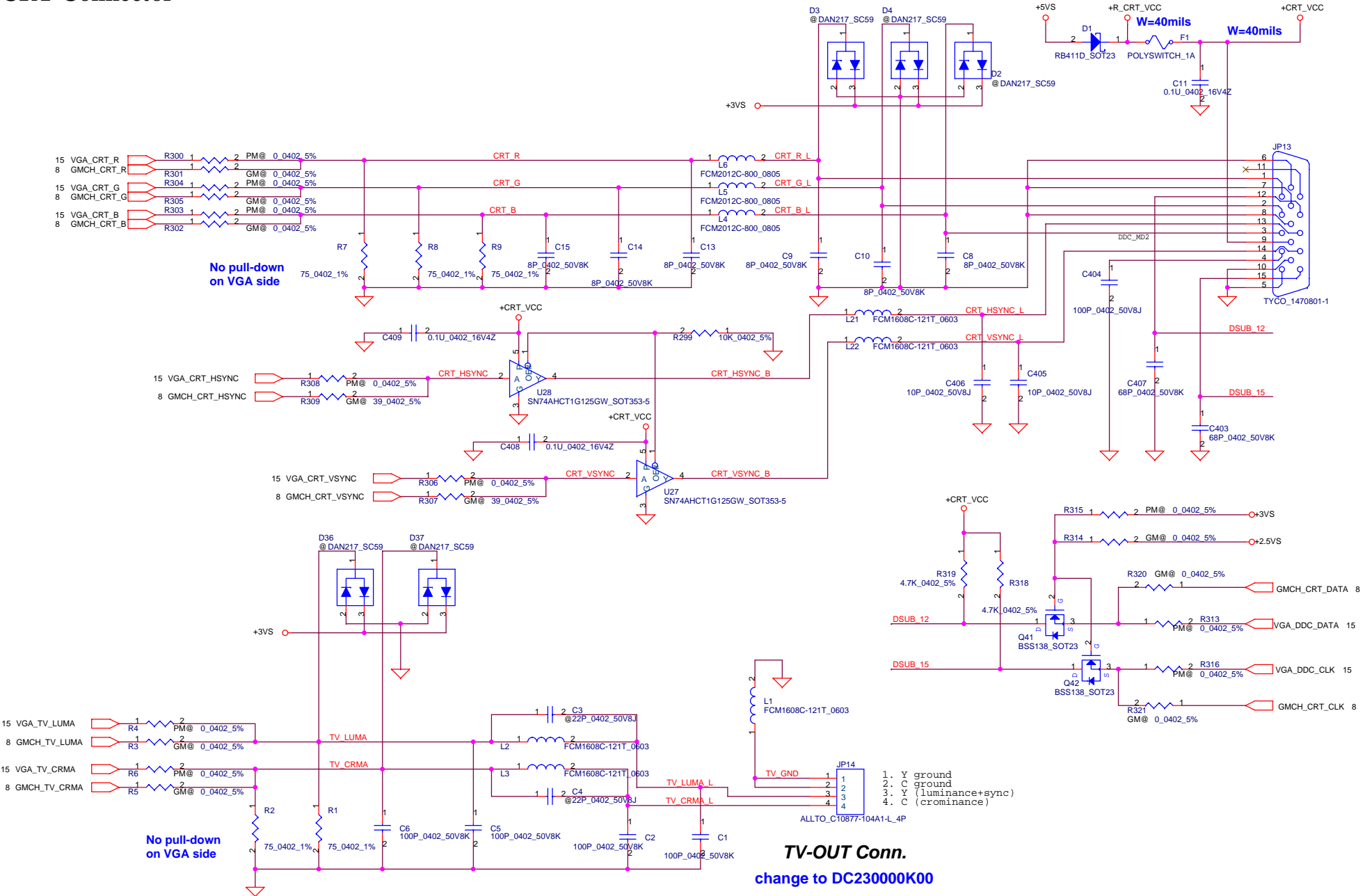
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FSC	FSB	FSA	CPU	SRC	PCI
CLKSEL0	CLKSEL1	CLKSEL2	MHz	MHz	MHz
1	0	1	100	100	33.3
0	0	1	133	100	33.3
0	1	1	166	100	33.3
0	1	0	200	100	33.3

Table : ICS 954226AG

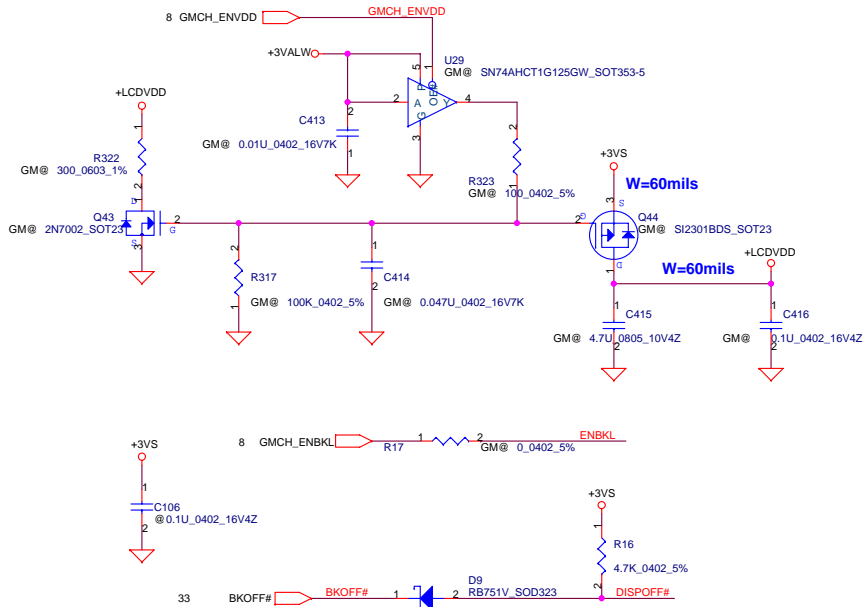


CRT Connector

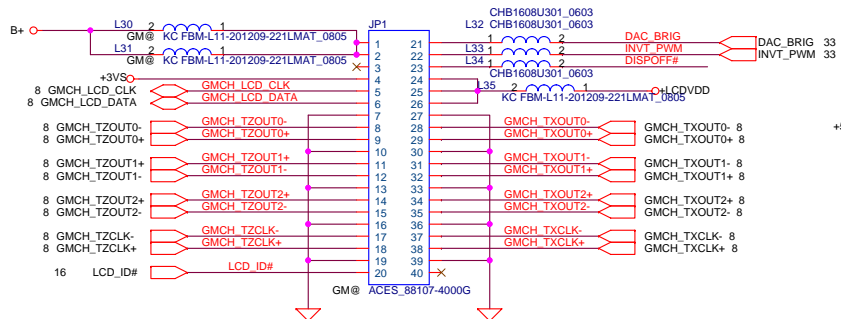


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				CRT&TV out Connector					
				Size		Document Number		Rev	
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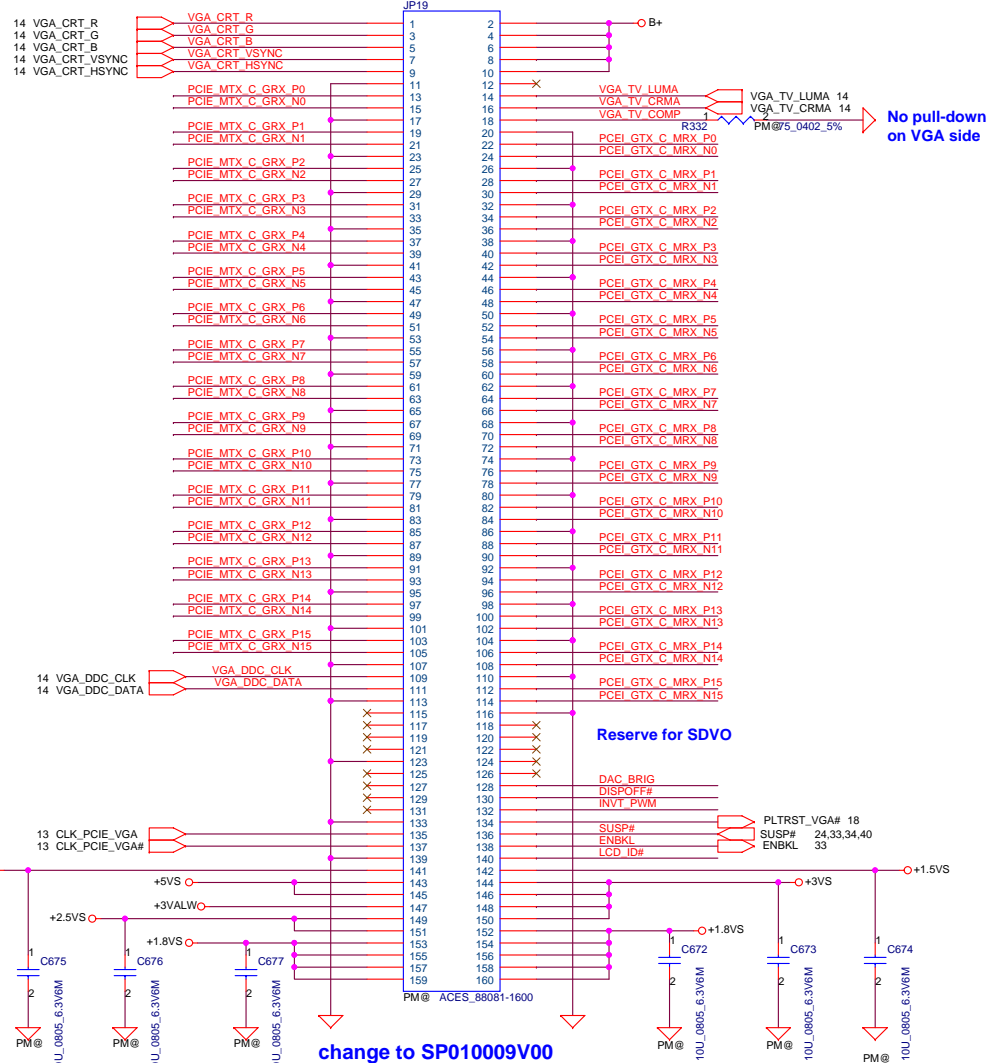
LCD POWER CIRCUIT



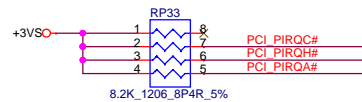
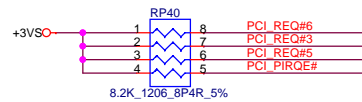
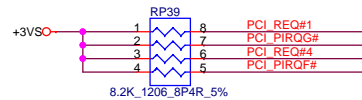
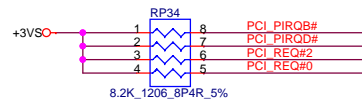
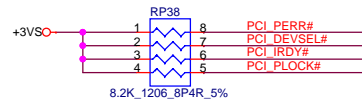
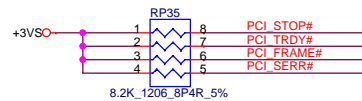
LCD/PANEL BD. Conn.



VGA BOARD Conn.



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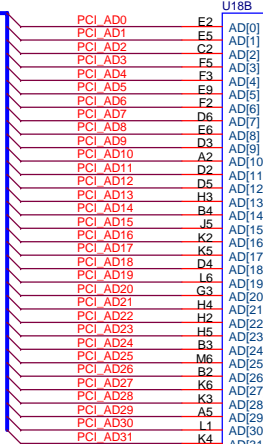


22,25,26,28 PCI_AD[0..31]

22,25,26,28 PCI_FRAME#

22 PCI_PIRQA#

22 PCI_PIRQB#



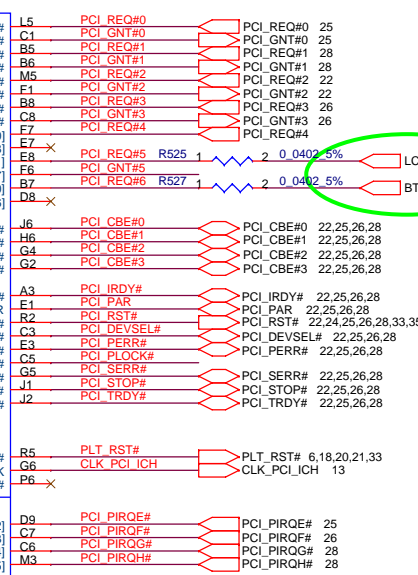
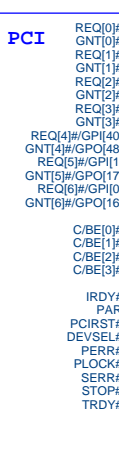
×AC5
×AD5
×AF4
×AG4
×AD9
×AF8
×AG8
×U3
ICH6_BGA609

Interrupt I/F
PIRQ[A]# PIRQ[E]/GPI[2]
PIRQ[B]# PIRQ[F]/GPI[3]
PIRQ[C]# PIRQ[G]/GPI[4]
PIRQ[D]# PIRQ[H]/GPI[5]

RESERVED

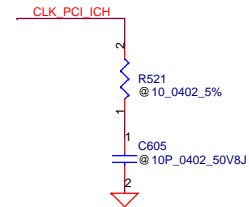
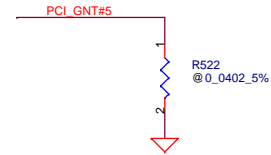
SATA[1]RXN/RSVD[1]
SATA[1]RXP/RSVD[2]
SATA[1]TXN/RSVD[3]
SATA[1]TXP/RSVD[4]
SATA[3]RXN/RSVD[5]
SATA[3]RXP/RSVD[6]
SATA[3]TXN/RSVD[7]
SATA[3]TXP/RSVD[8]
TP[3]/RSVD[9]

ICH6_BGA609



LCD_ID#
High when used EDID panel
Low when used non-EDID panel

Internal Pull-up.
Sample high destination is LPC.

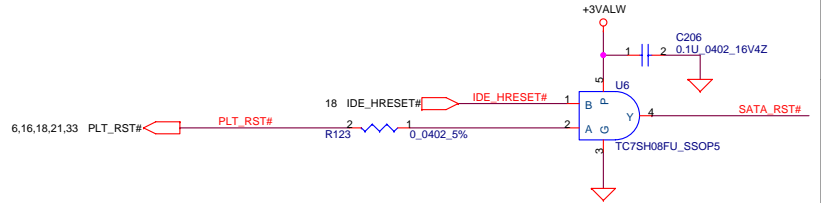
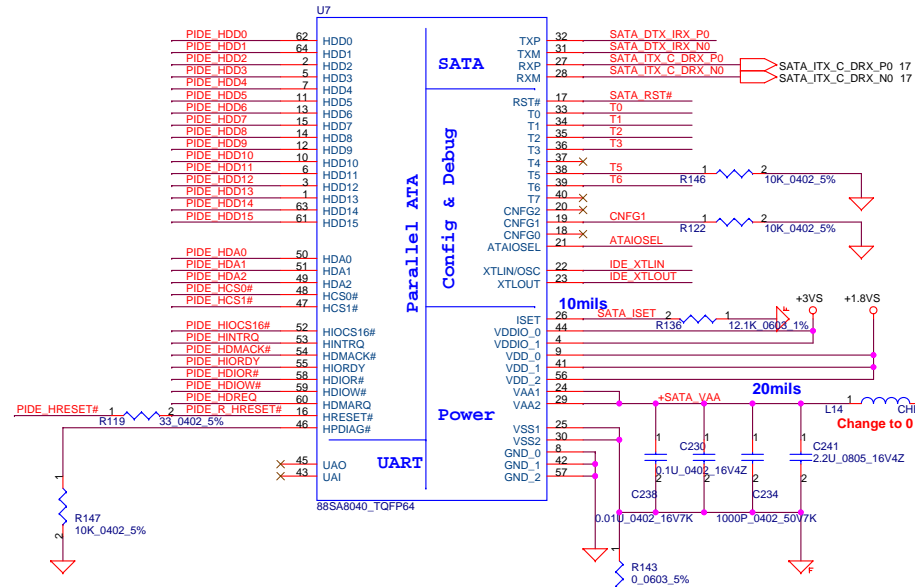
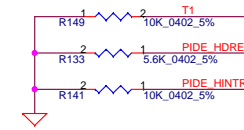
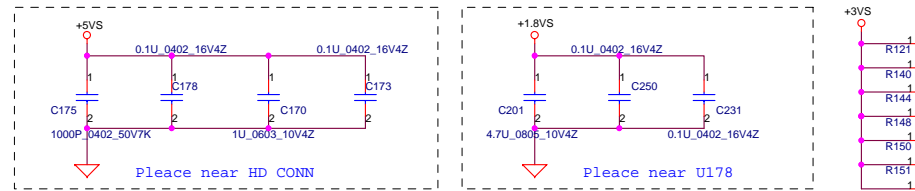


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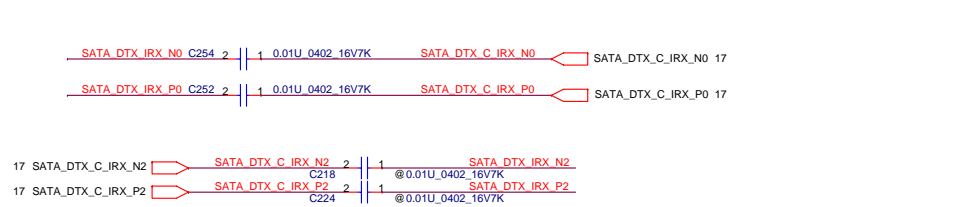
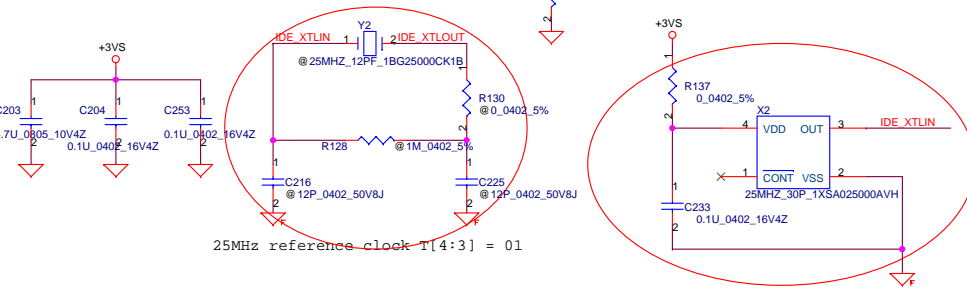
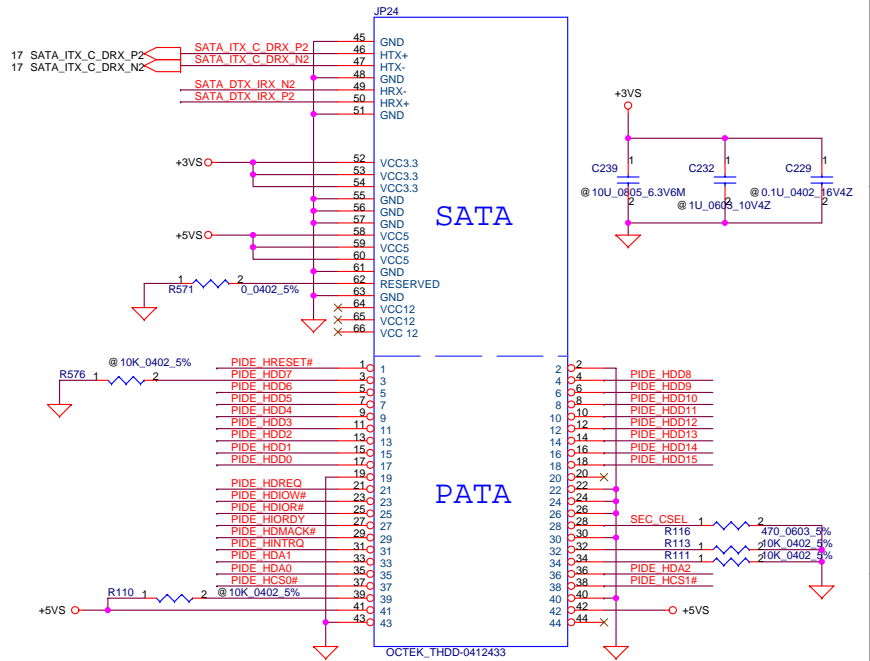
SATA Module

Sets maximum transfer rate and UDMA mode

CNFG2 INT PD	CNFG1	CNFG0 INT PD	NOTE
0	0	0	Device Mode 100MB/s
0	0	1	Device Mode 133MB/s
0	1	0	Device Mode 150MB/s
1	0	0	Host Mode 100MB/s
1	0	1	Host Mode 133MB/s
1	1	0	Host Mode 150MB/s
0	1	1	Reserved
1	1	1	Reserved



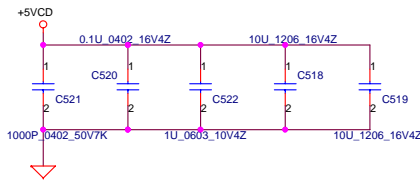
PATA/SATA HDD Conn.



reserved for SATA HDD

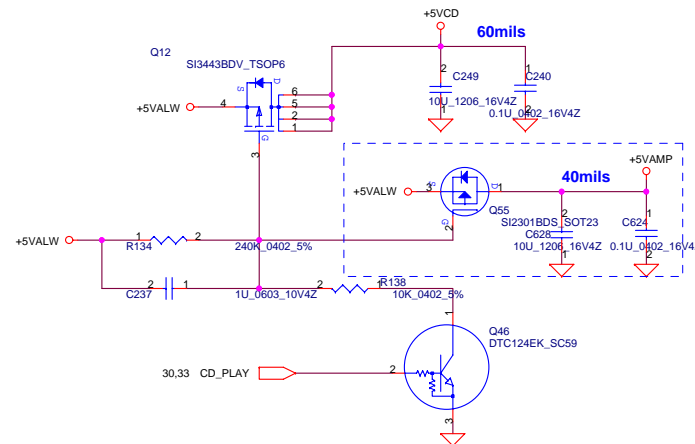
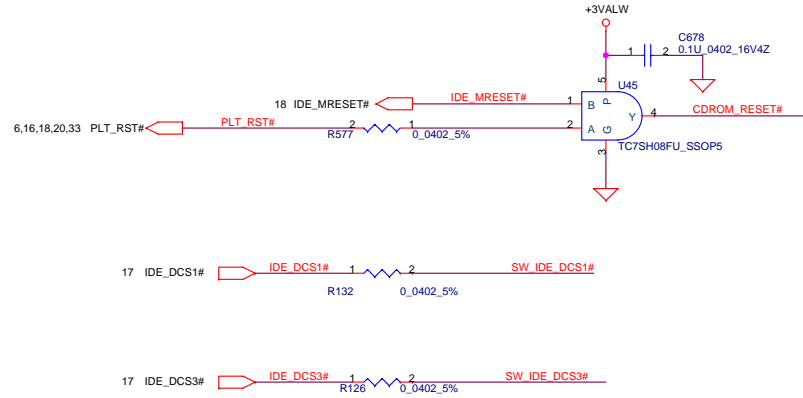
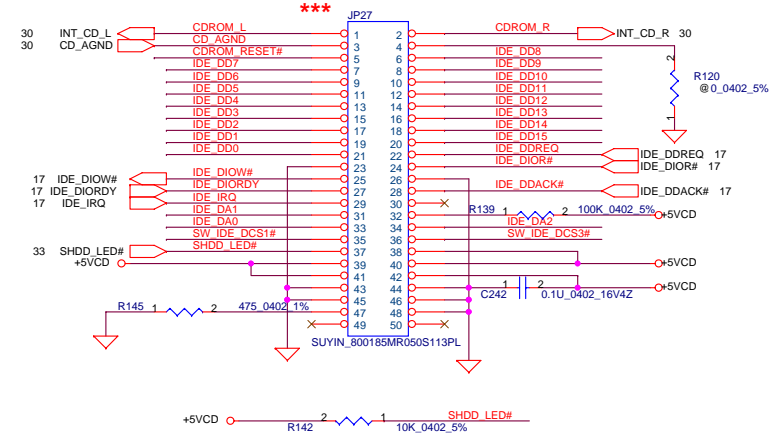
Security Classification	Compal Secret Data			Title	Compal Electronics, Inc.
Issued Date	2005/03/25	Deciphered Date	2006/03/25	Document Number	Marvell 88SA8040&HDD CONN
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				2005. 04. 20	1.0
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Placea caps. near ODD CONN.

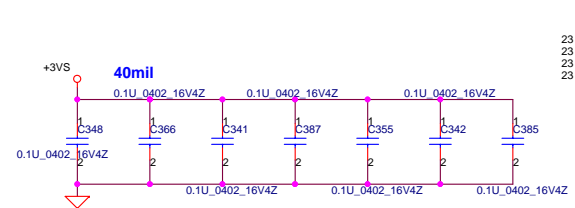


17 IDE_DD[0..15] IDE_DD[0..15]
17 IDE_DA[0..2] IDE_DA[0..2]

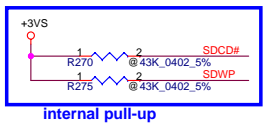
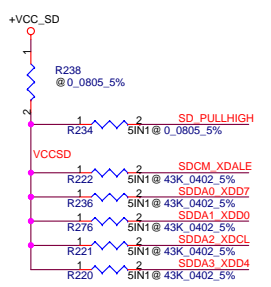
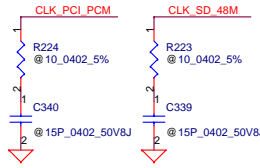
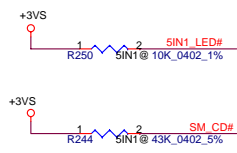
ODD Conn. (EAT10)



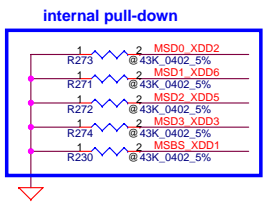
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Issued Date	2005/03/25	Deciphered Date	2006/03/25	Title	ODD CONN & SATA HDD CONN
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16,25,26,28 PCI_AD[0..31] \rightarrow PCI_AD[0..31]
 16,25,26,28 PCI_CBE#[0..3] \rightarrow PCI_CBE#[0..3]



internal pull-up



internal pull-down

MFUNC5[3:0] = (0 1 0 1)
 MFUNC5[4] = 1

MFUNC5[3:0] = (0 1 0 1)
 MFUNC5[4] = 1

MFUNC5[3:0] = (0 1 0 1)
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MFUNC5[3:0] = (0 1 0 1)
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MFUNC5[3:0] = (0 1 0 1)
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MFUNC5[3:0] = (0 1 0 1)
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MFUNC5[3:0] = (0 1 0 1)
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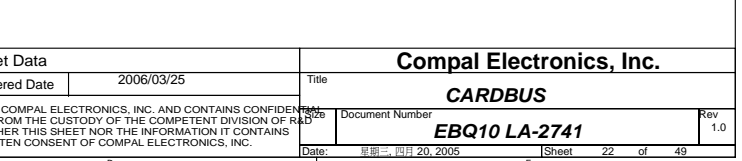
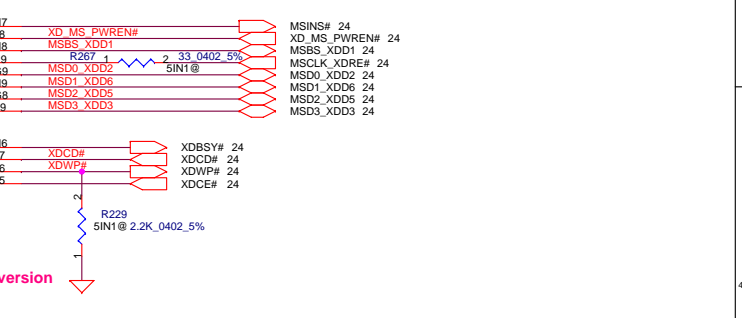
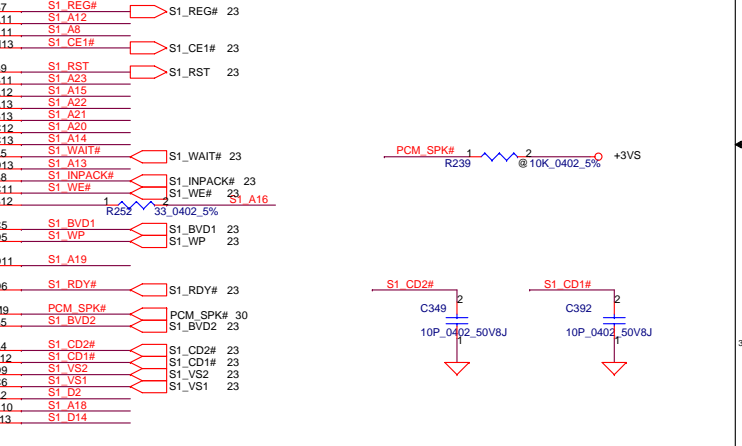
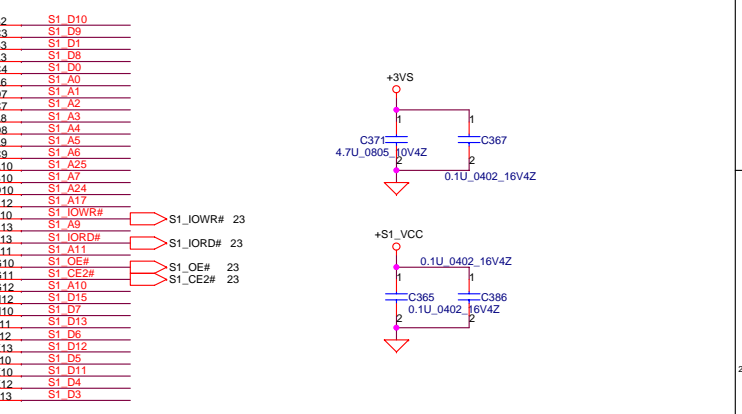
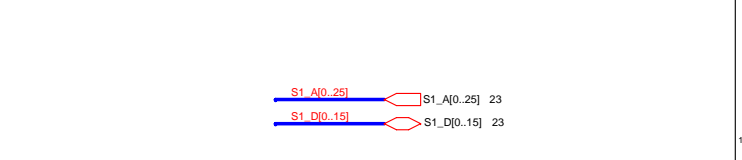
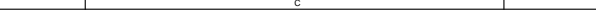
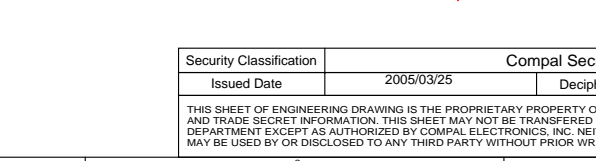
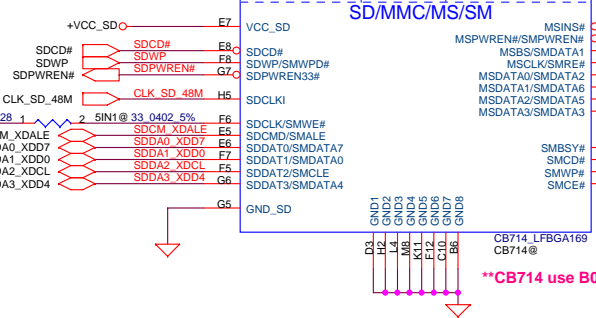
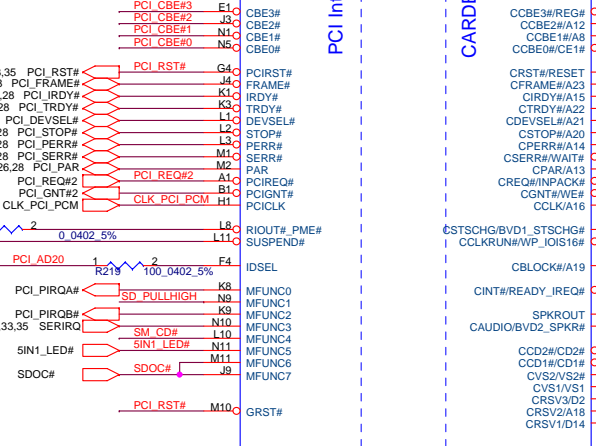
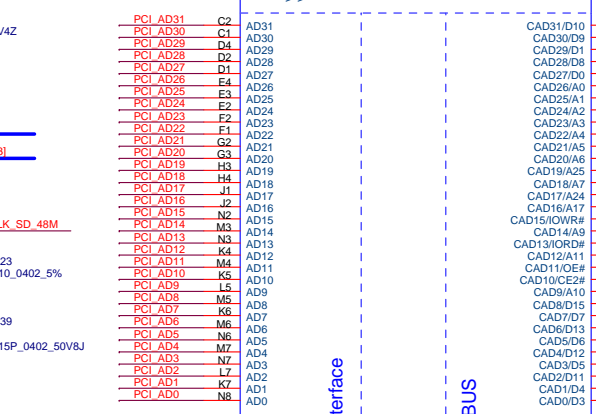
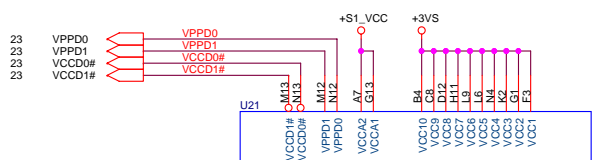
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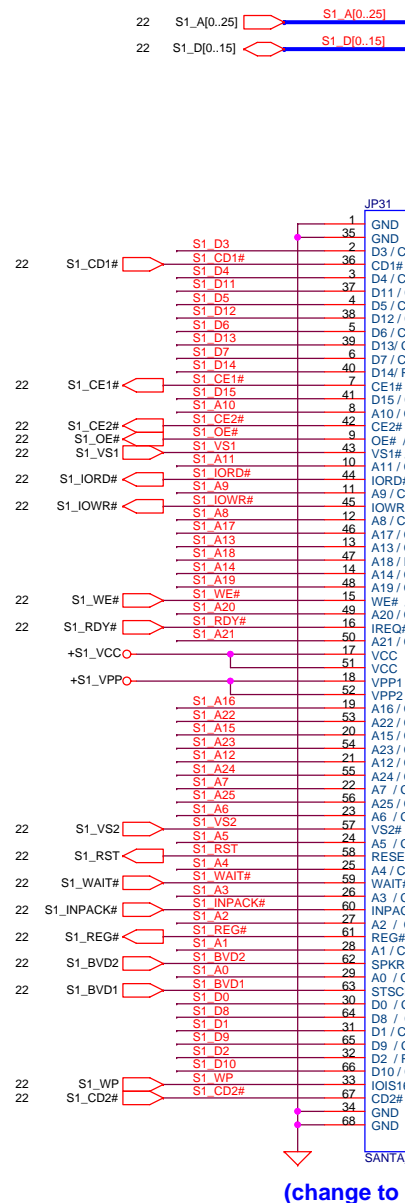
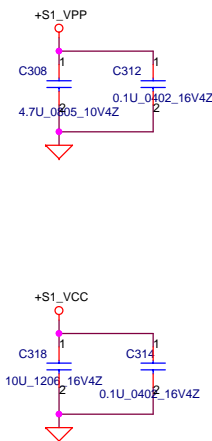
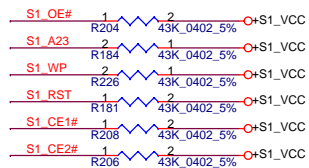
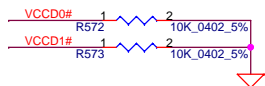
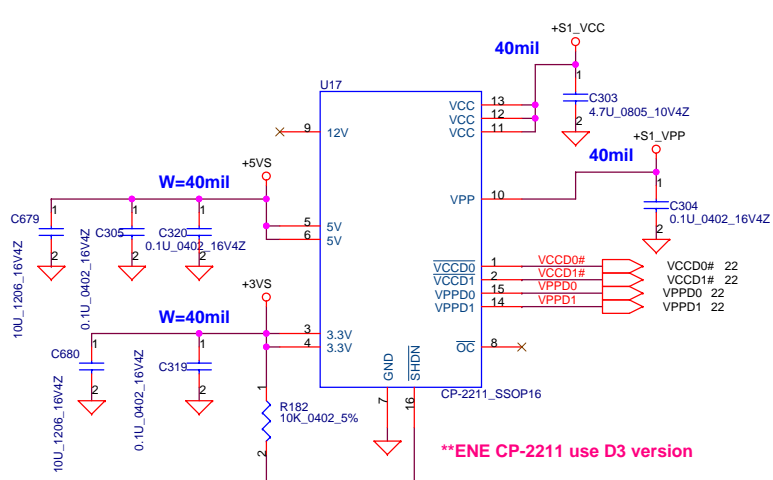
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				Sheet 22 of 49	

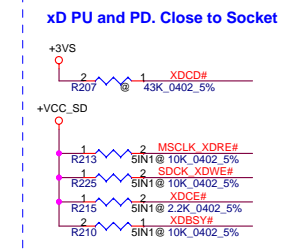
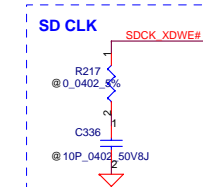
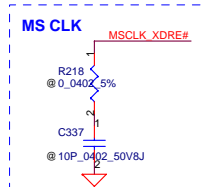
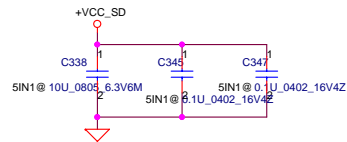
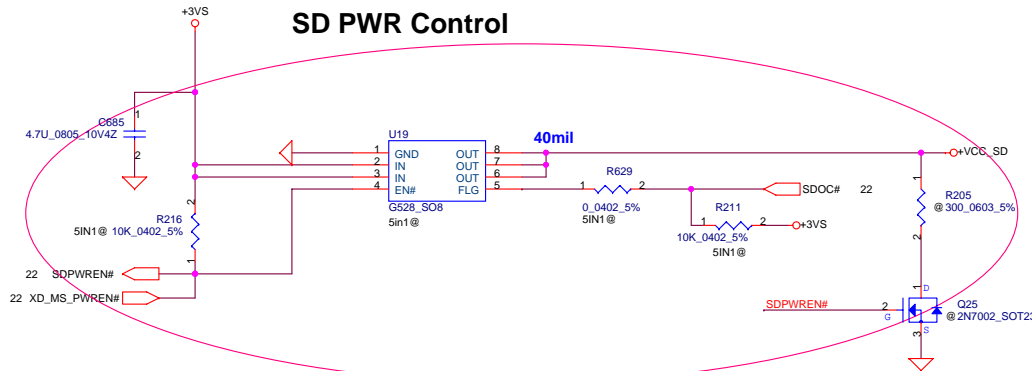


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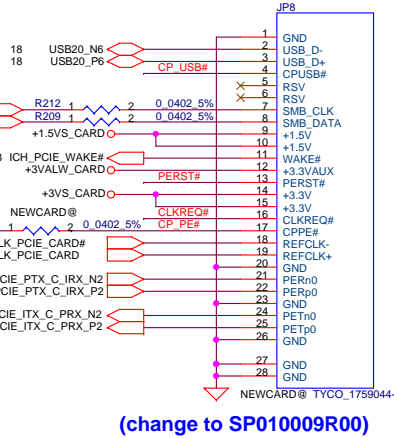
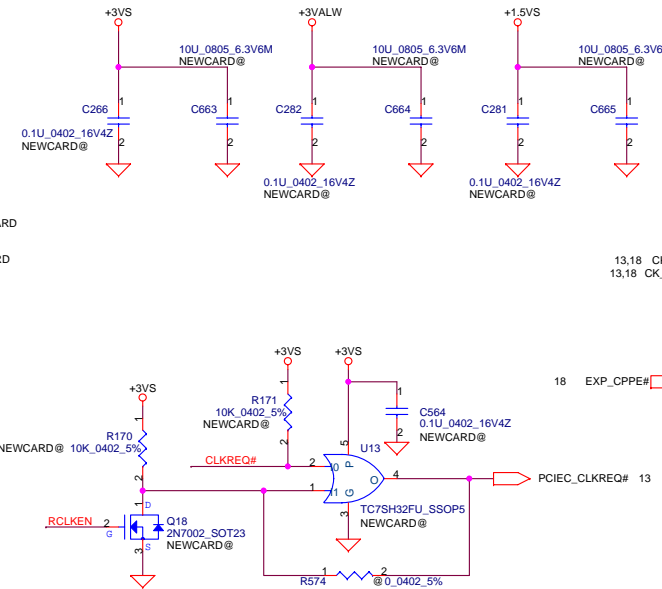
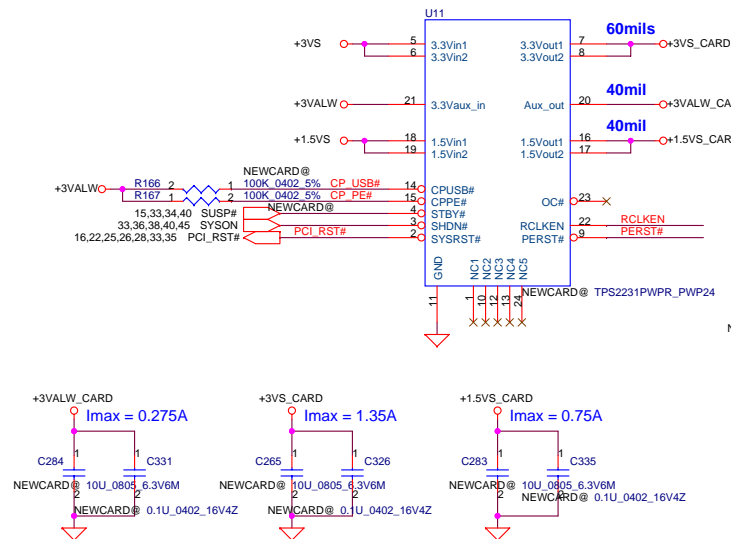
PCMCIA Conn.

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						EBQ10 LA-2741			
						Rev 1.0			
						Date: 星期三, 四月 20, 2005			
						Sheet 23 of 49			

SD PWR Control

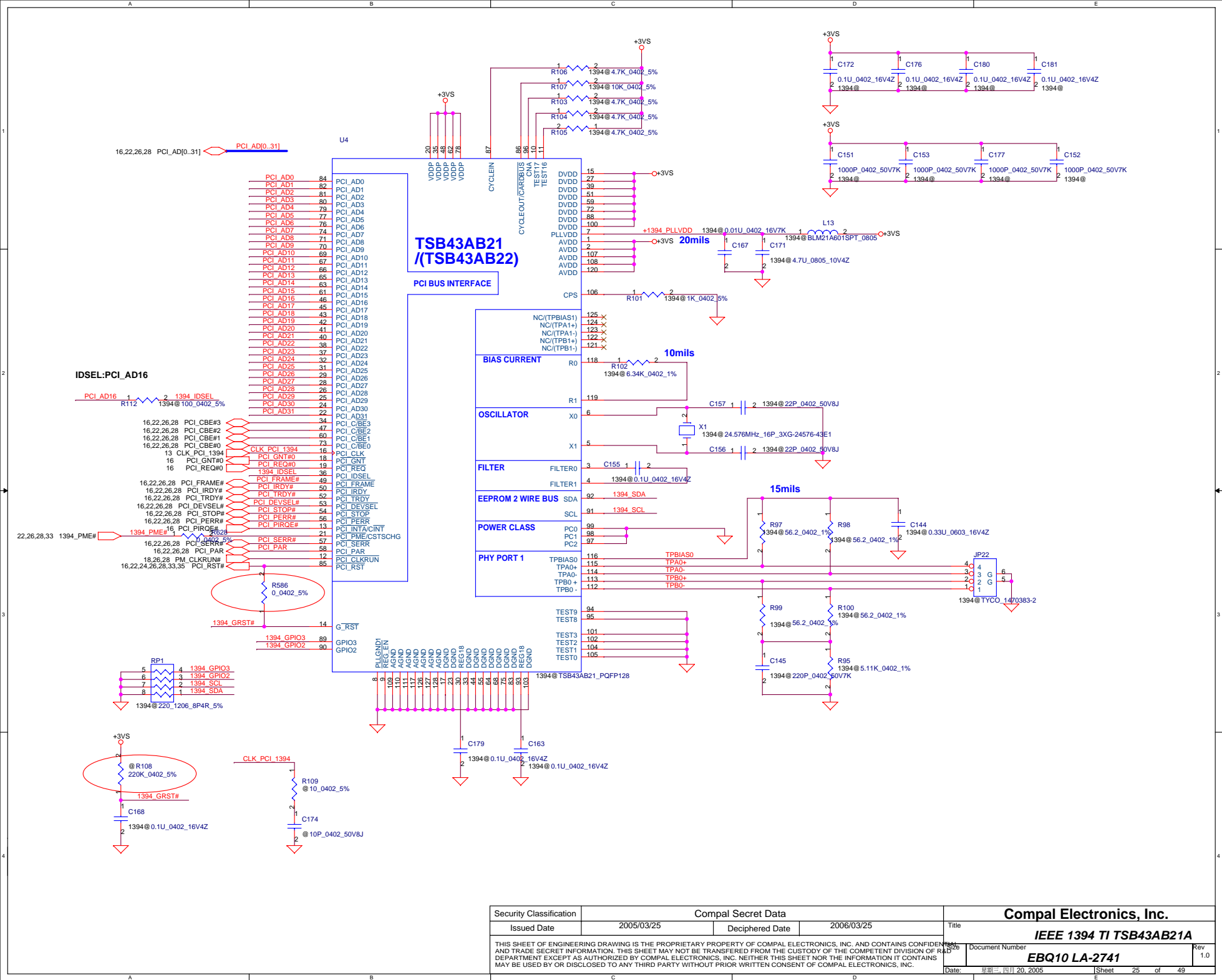


New Card Power Switch

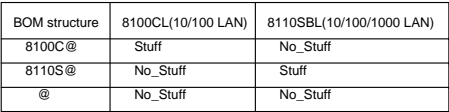


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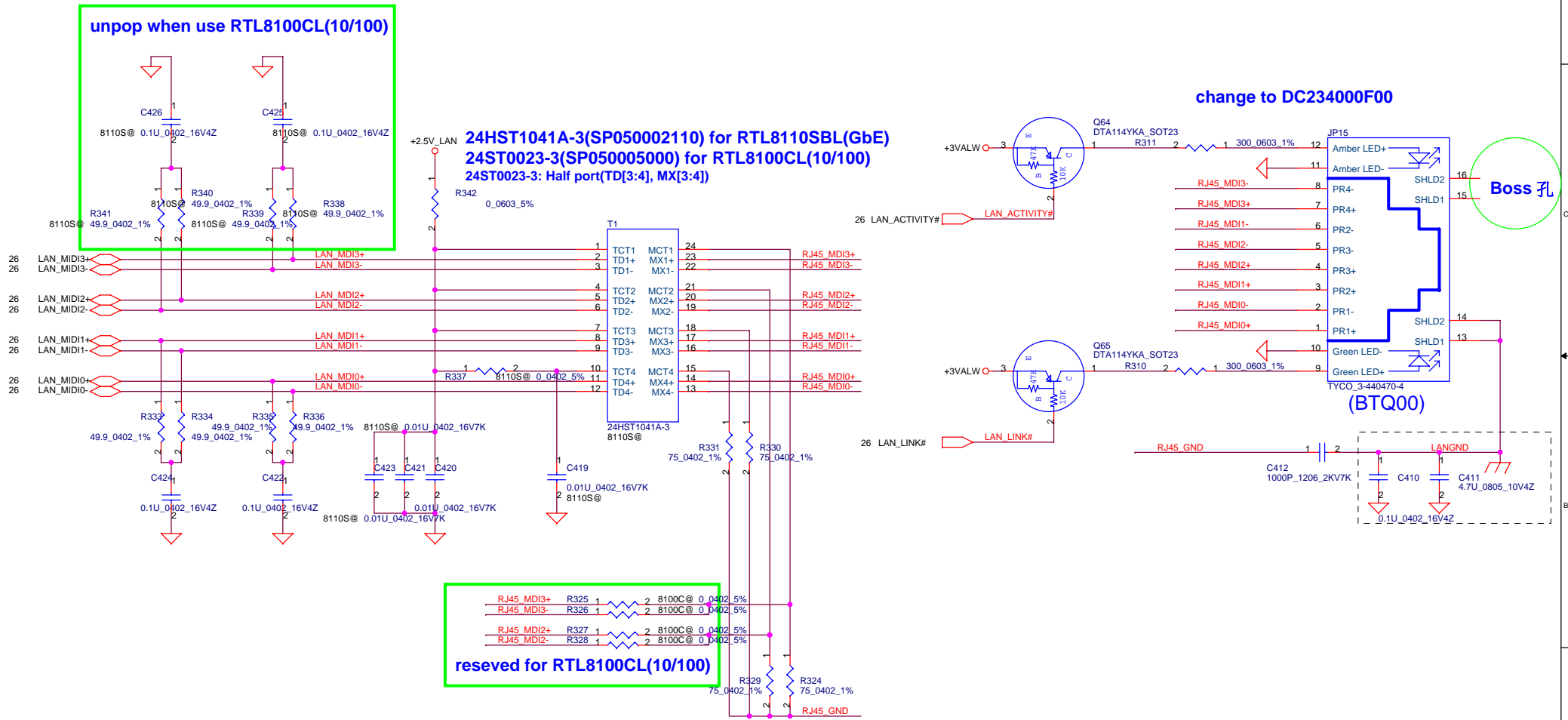
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Deciphered Date				2006/03/25				5IN1 & NEW Card Socket			
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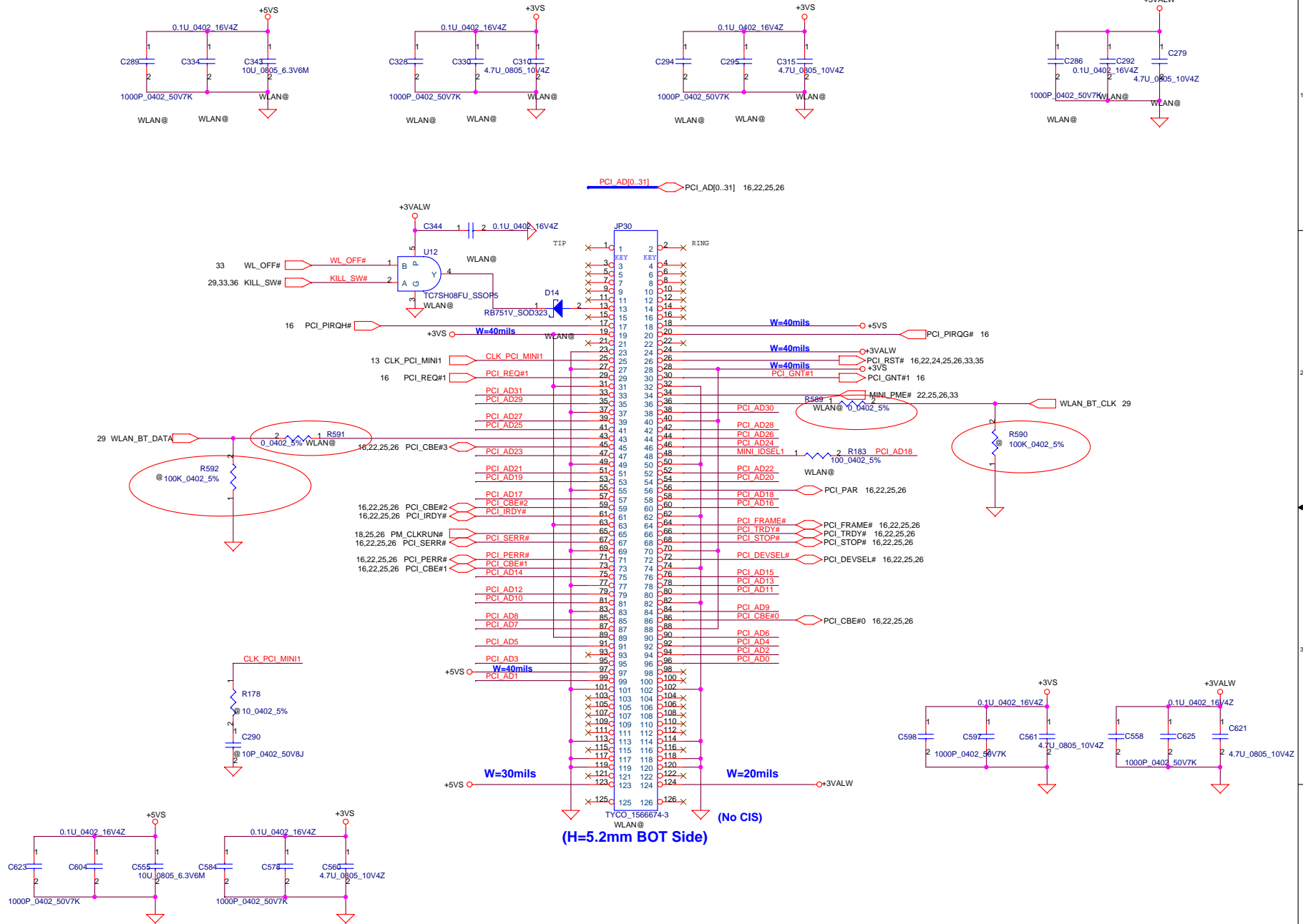
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				Document Number	Rev	
				EBQ10 LA-2741	1.0	
				Date:	Sheet	
C		D		2005.04.20		
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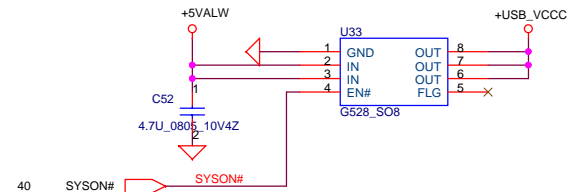
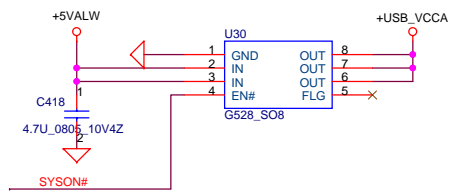
LAN RTL8110SBL/RTL8100CL



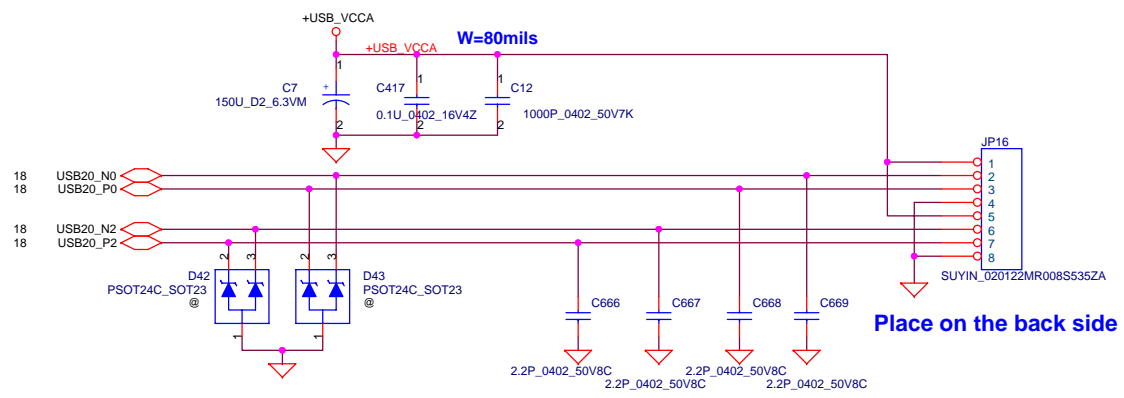
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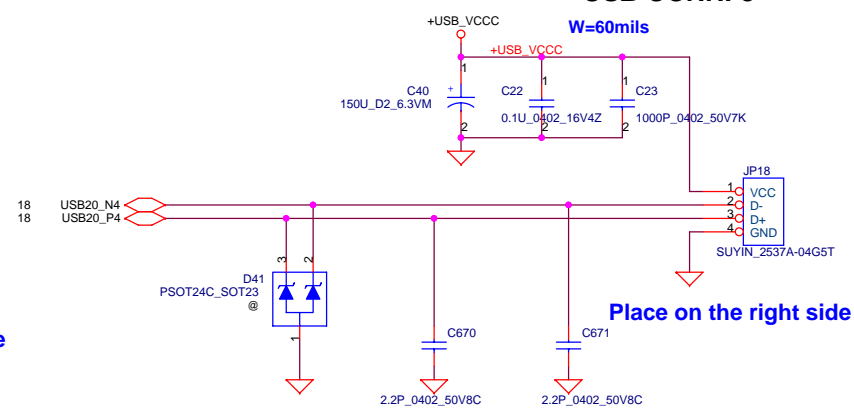
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				EBQ10 LA-2741	1.0
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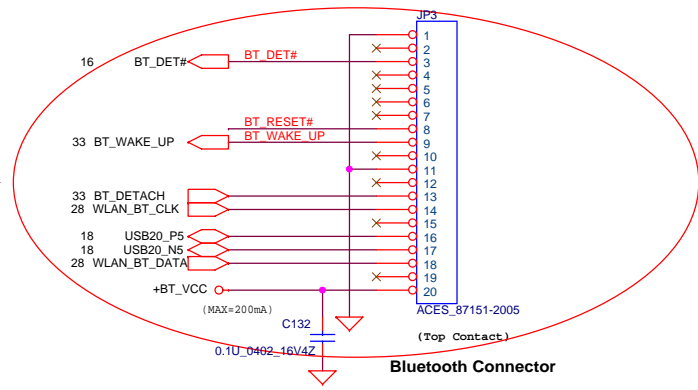
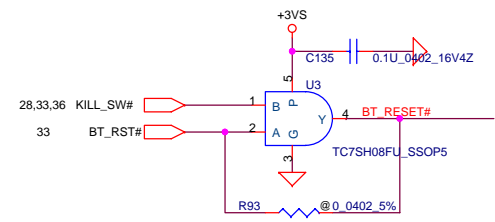
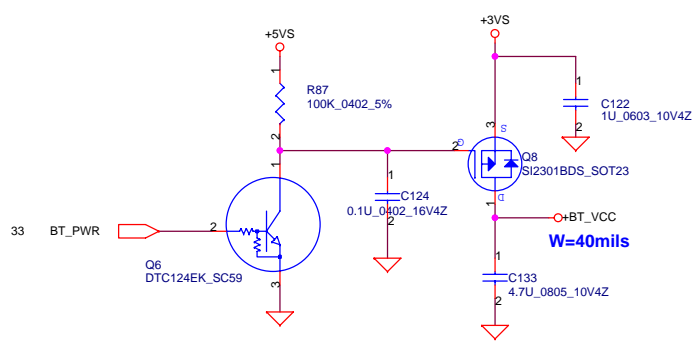
USB CONN. 1 & 2



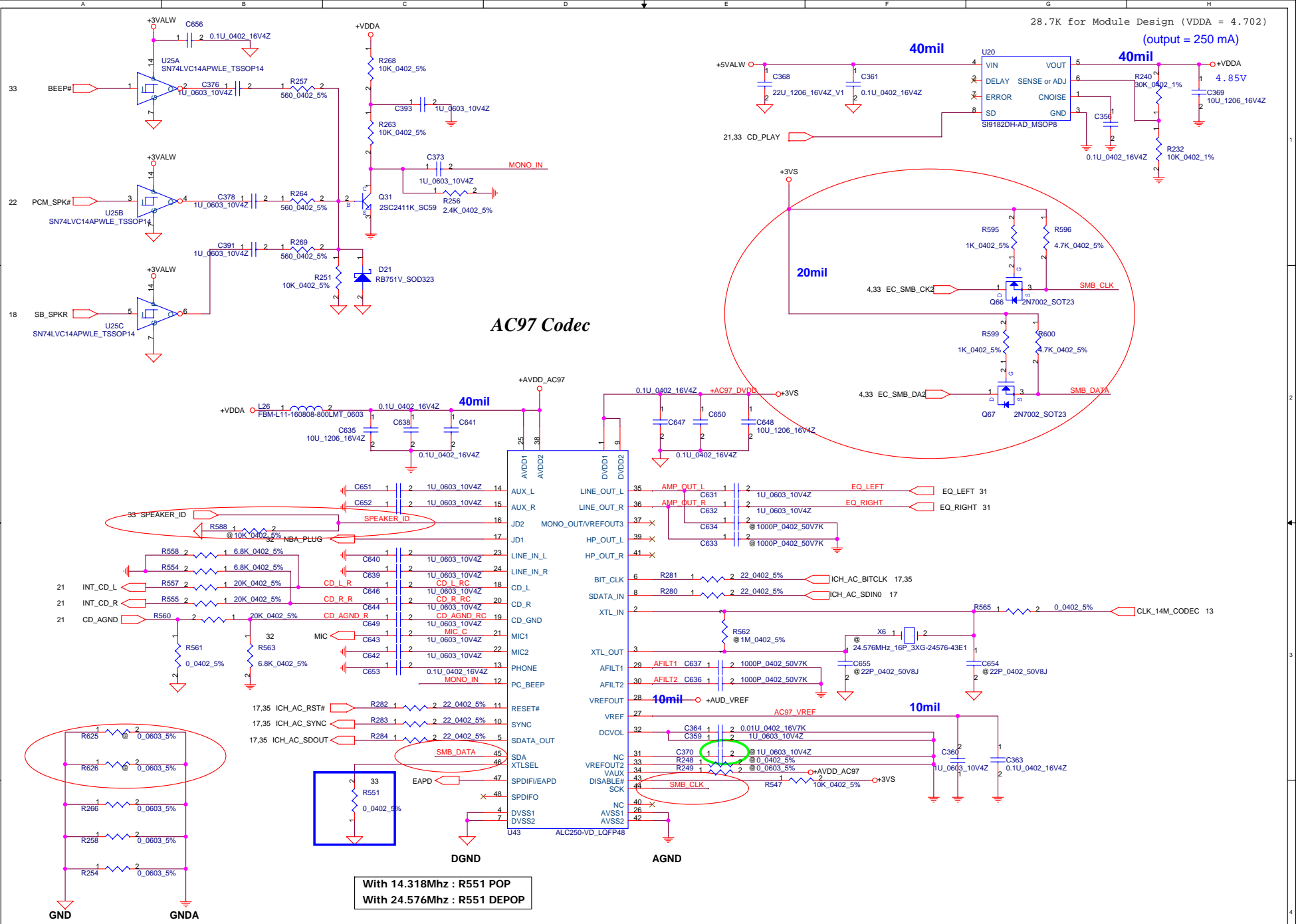
USB CONN. 3



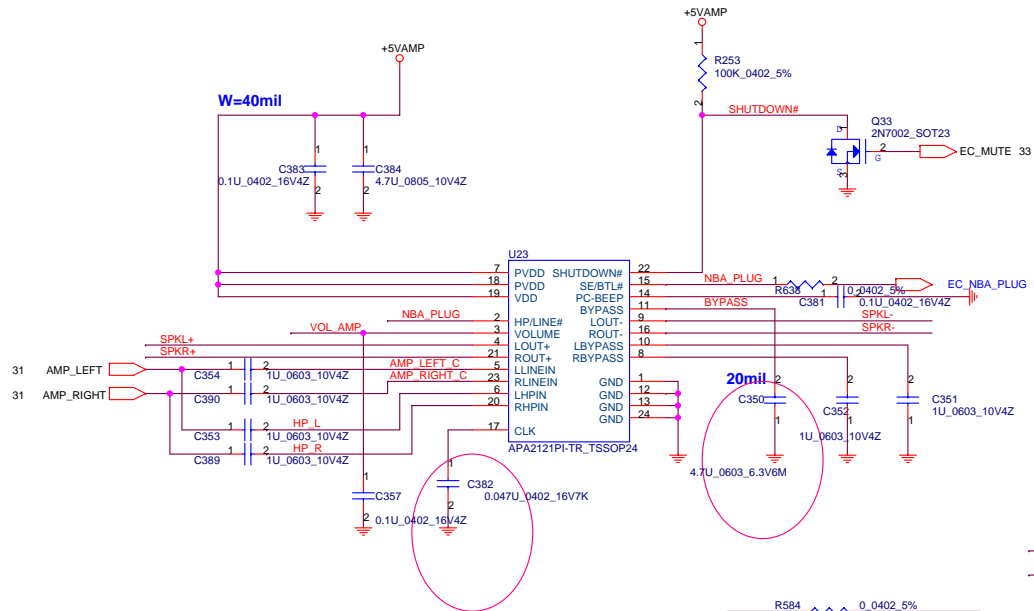
Bluetooth Conn.



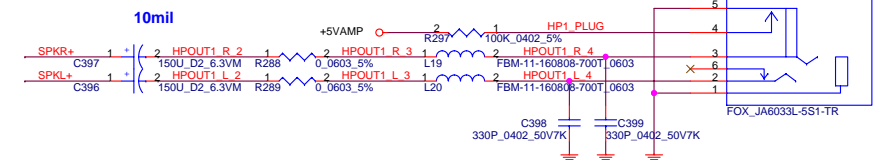
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				EBQ10 LA-2741	
Date: 星期三, 四月 20, 2005		Sheet 29 of 49			



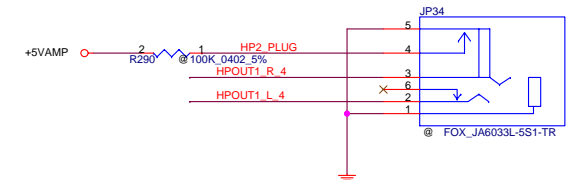
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				Date	Rev
				2005 年 04 月 20 日	1.0
				Sheet	30 of 49



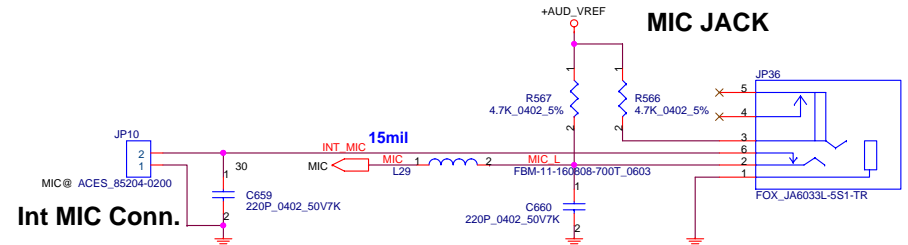
Headphone JACK 1



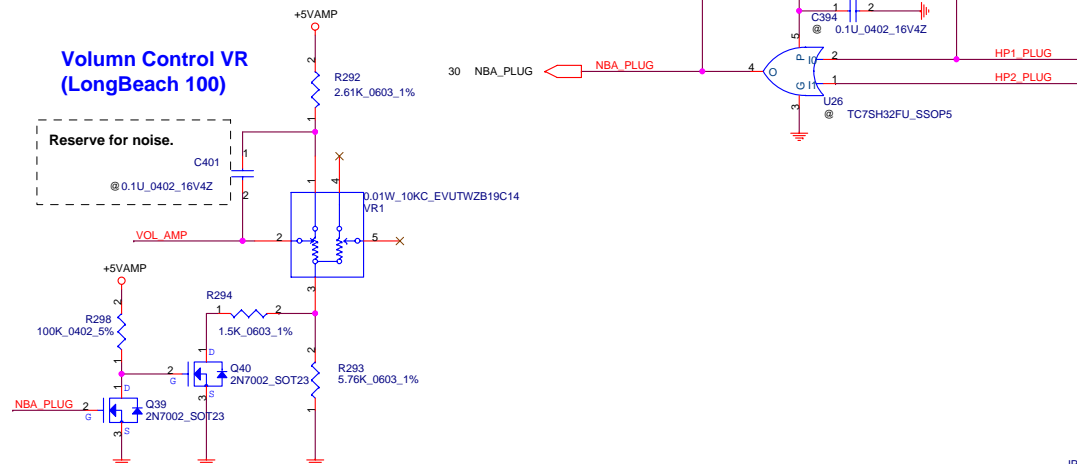
Headphone JACK 2



MIC JACK



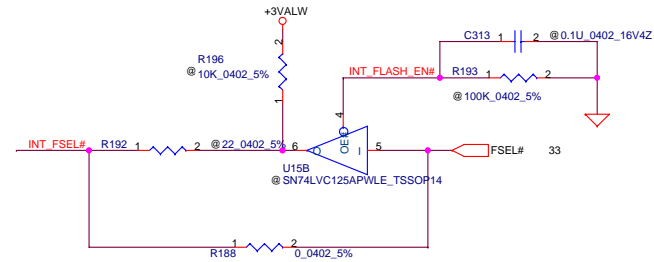
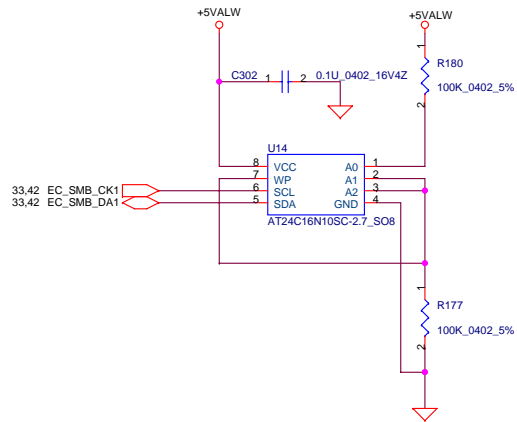
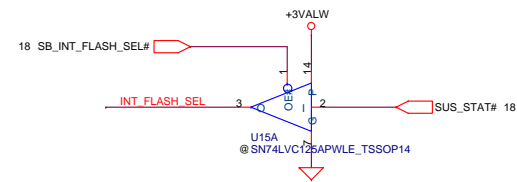
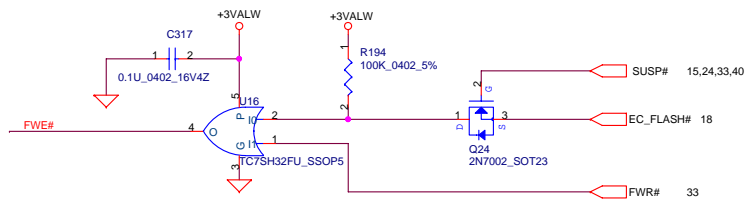
Volumn Control VR (LongBeach 100)



BTL MODE
R293/R294=1.19K
Vmax=0.431V , GAINmax=14dB
Vmin=4.05V, GAINmin=-80dB

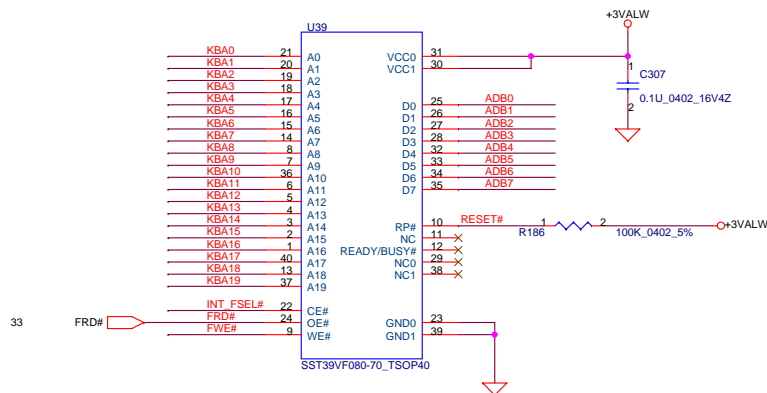
SE MODE
Vmax=1.53V , GAINmax=-6db
Vmin=4.28V, GAINmin=-80db

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				Date: 星期三, 四月 20, 2005	Sheet 32 of 49

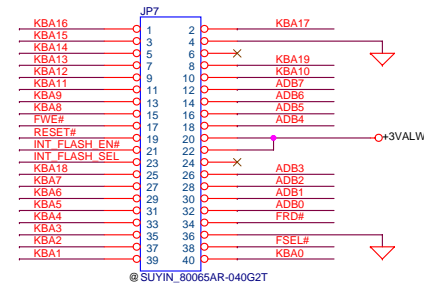


33 KBA[0..19] KBA[0..19]
33 ADB[0..7] ADB[0..7]

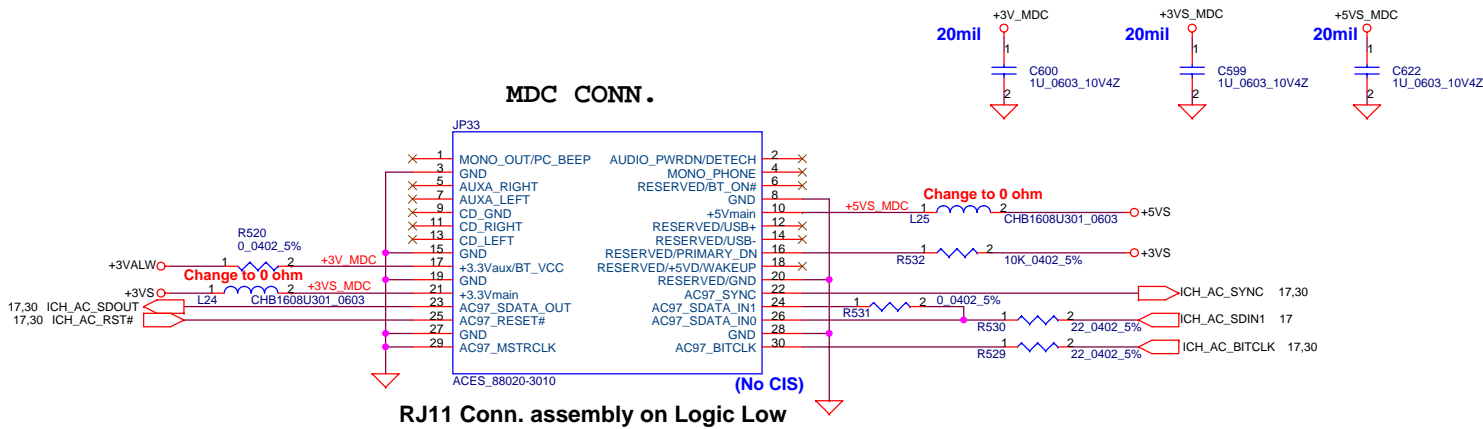
1MB Flash ROM



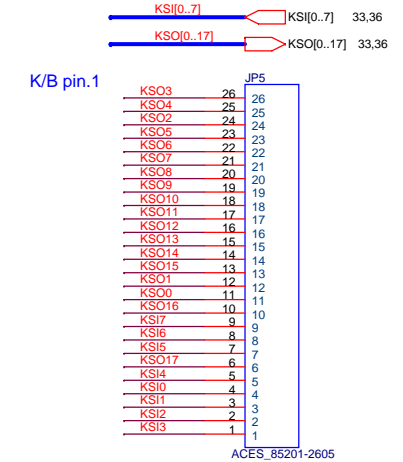
1MB ROM Socket



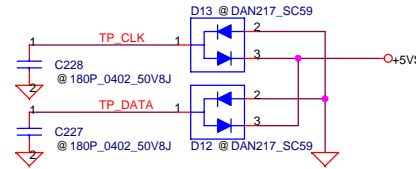
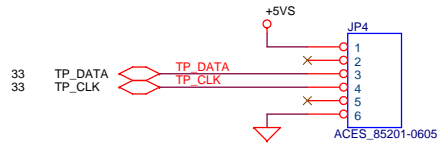
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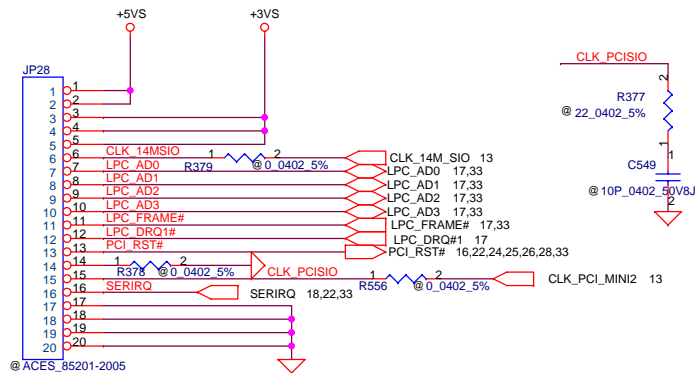
INT_KBD CONN.



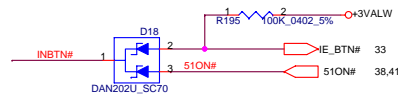
To TP/B Conn.



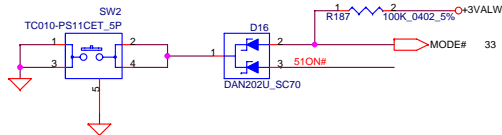
LPC Debug Port



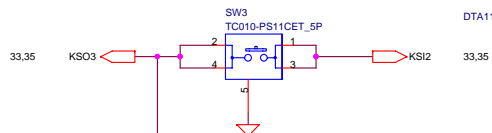
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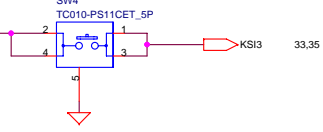
Vivace(SW-DJ) Button



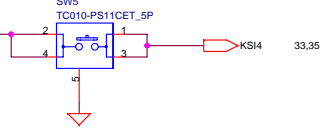
Play/Pause Button



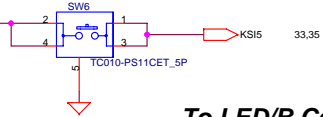
Stop/Eject Button



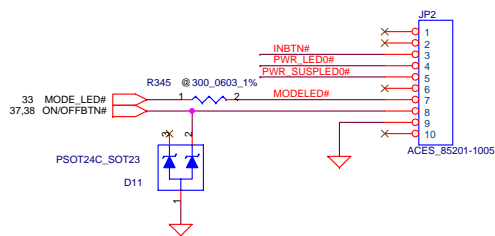
Next(FR) Button



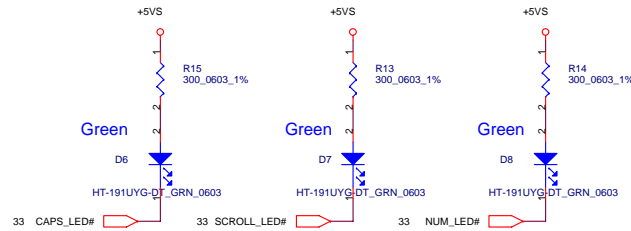
Previous(FF) Button



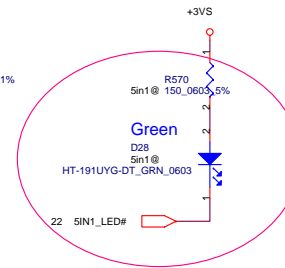
To LED/B Conn.



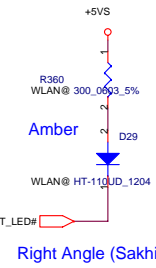
CAP Lock LED Scroll Lock LED Number Lock LED



5 In 1 Card LED (Close to Socket)

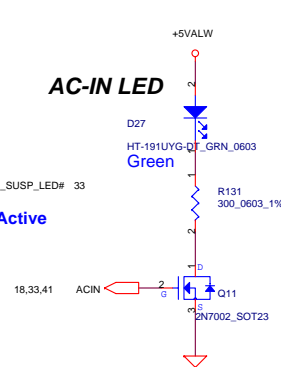


Wireless/BT LED (Close to Killer SW)

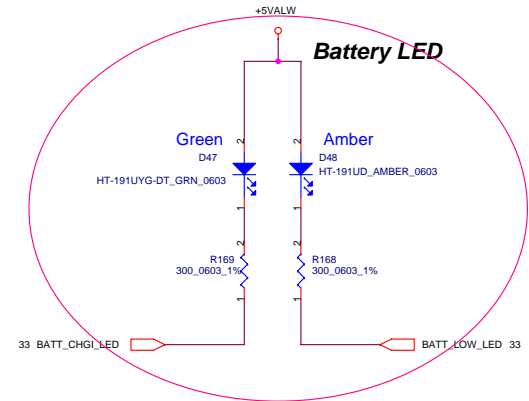


Right Angle (Sakhir)

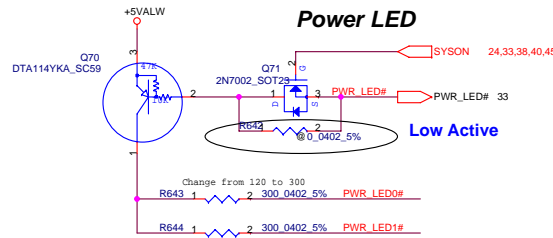
AC-IN LED



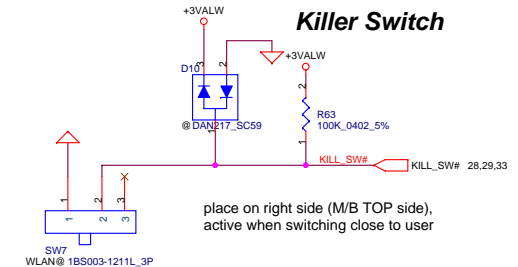
Battery LED



Power LED

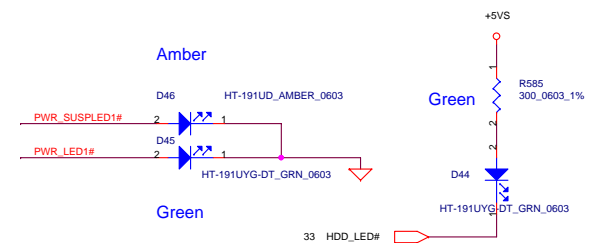


Killer Switch

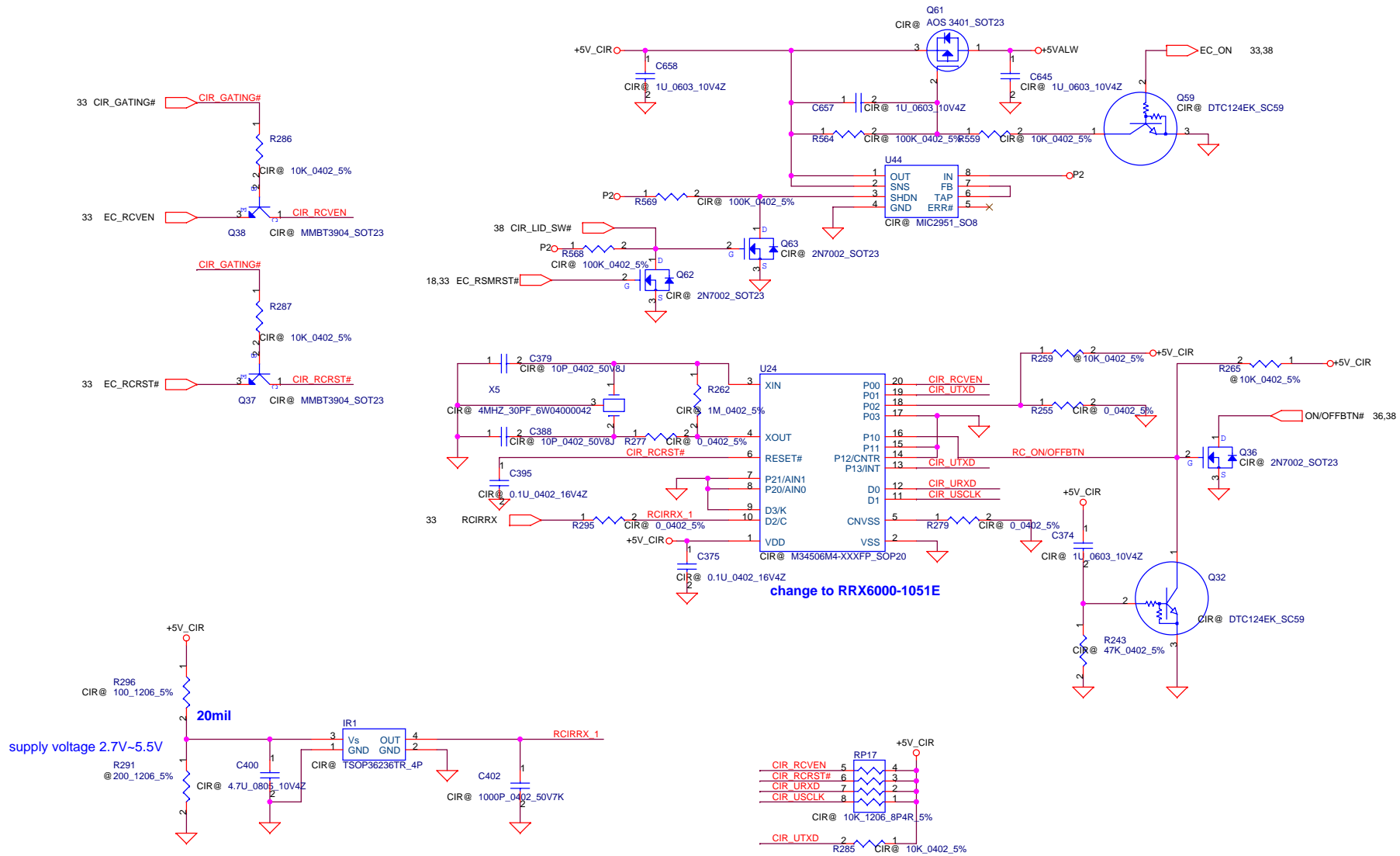


place on right side (M/B TOP side), active when switching close to user

HDD LED



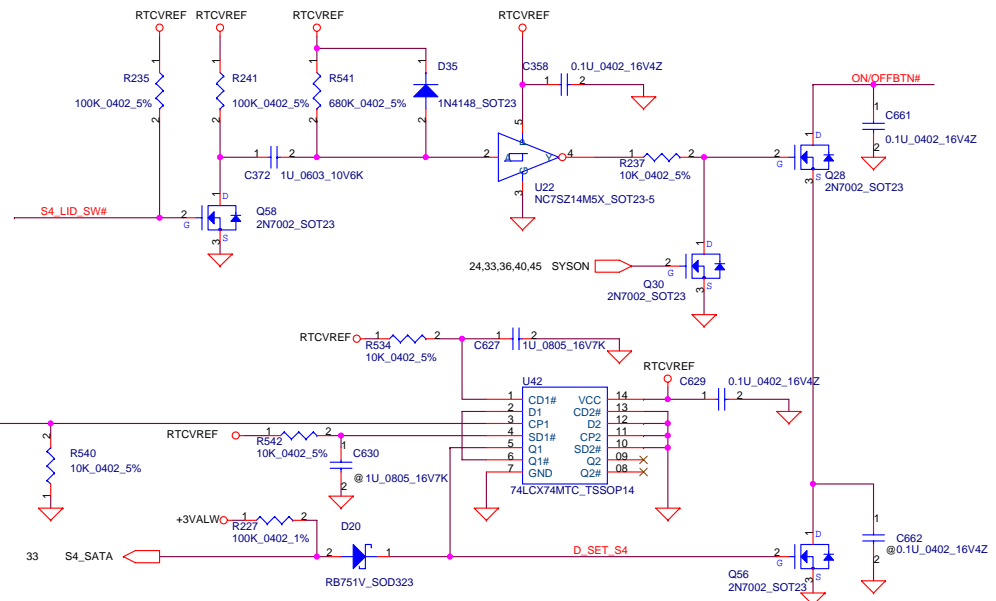
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				Date	Rev 1.0



[illegible]

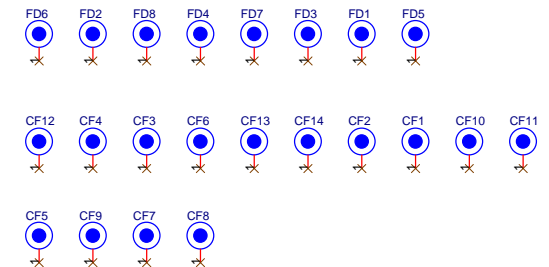
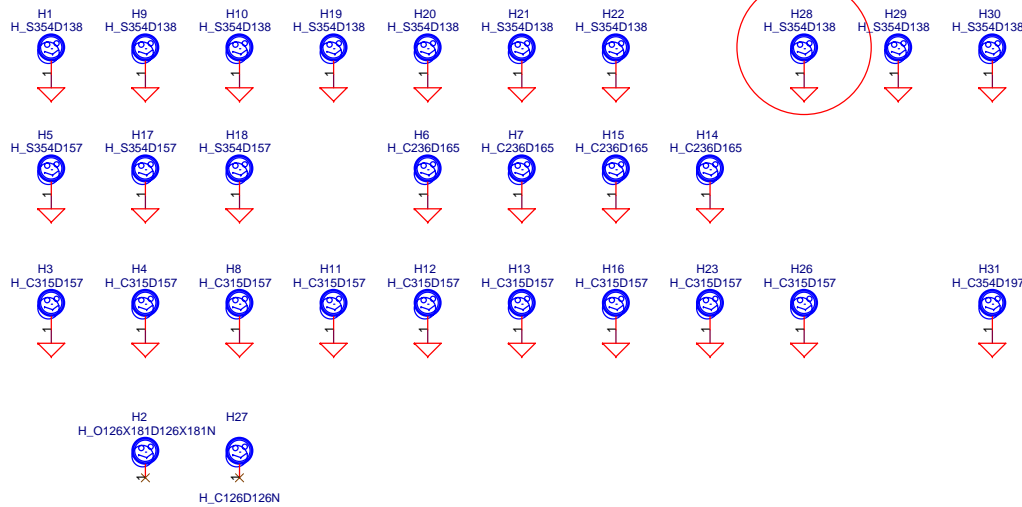
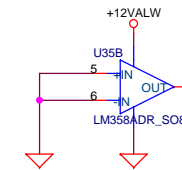
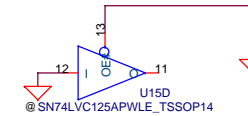
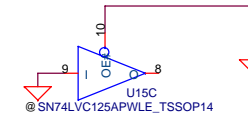
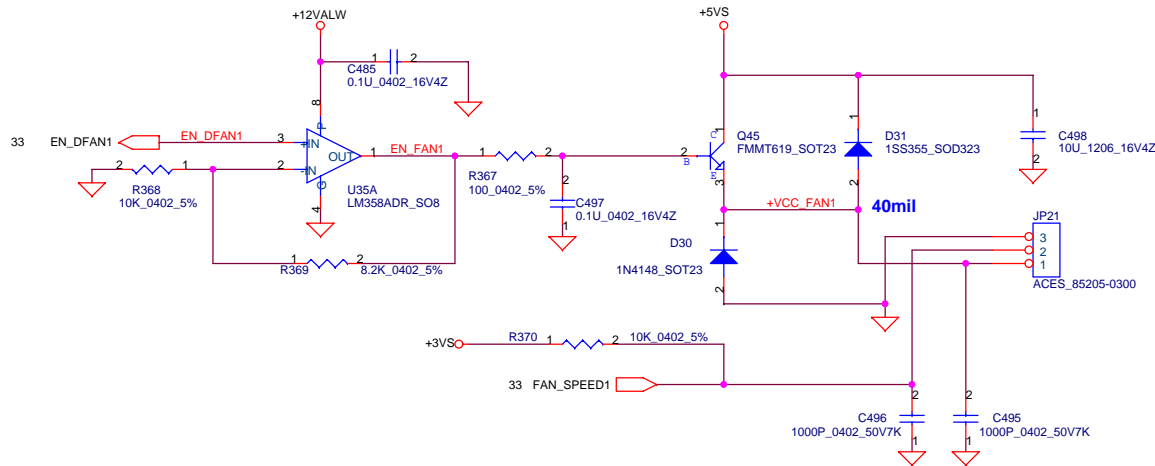
Lid Switch

The schematic shows a switch SW1 connected to the MPU-101-81_4P. The switch is controlled by the DAN202U_SC70 (D15) and the RB751V_SOD323 (D17) diodes. The switch is connected to the LID_SW# (33) and CiR_LID_SW# (37) pins. The circuit also includes a +3VALW supply, a 100K resistor R185, and a PSOT24C_SOT23 package.

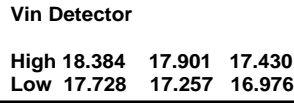


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FAN Conn

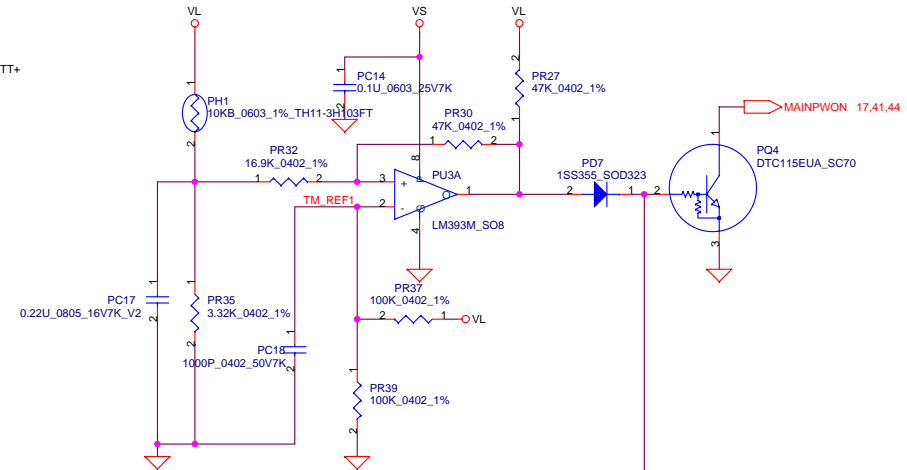
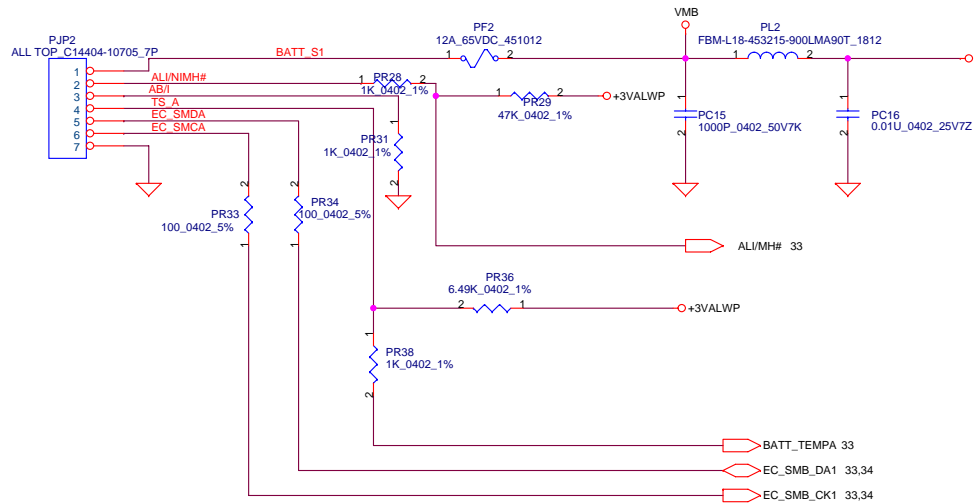


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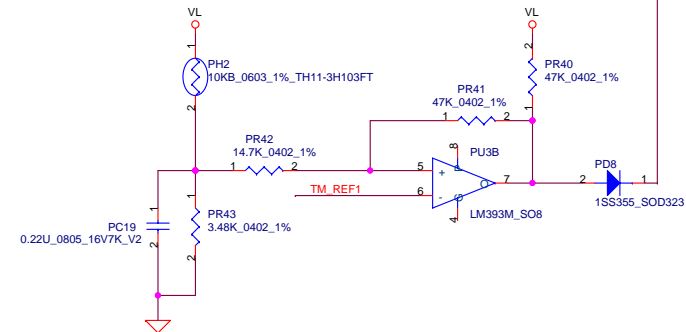


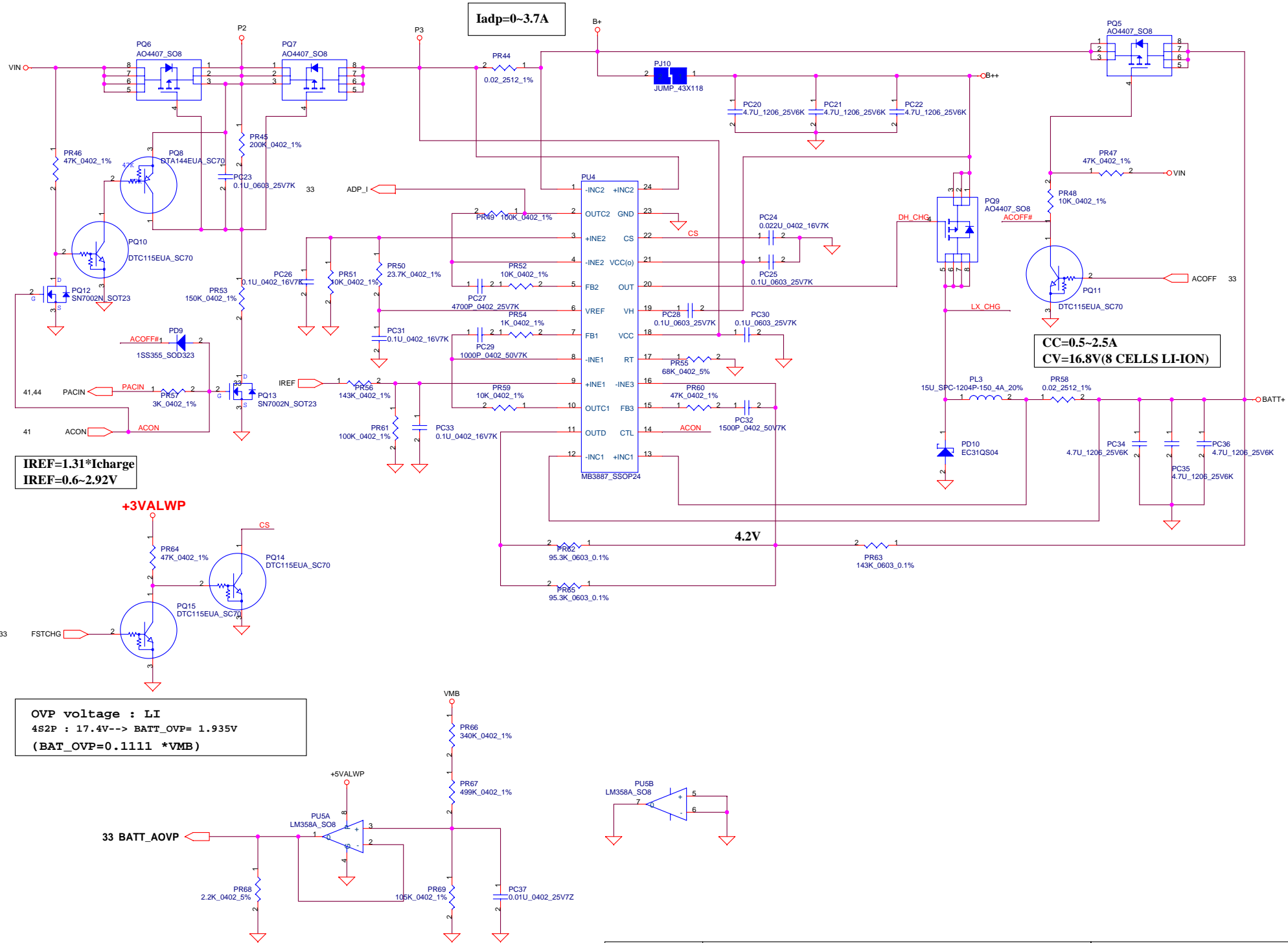
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PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C





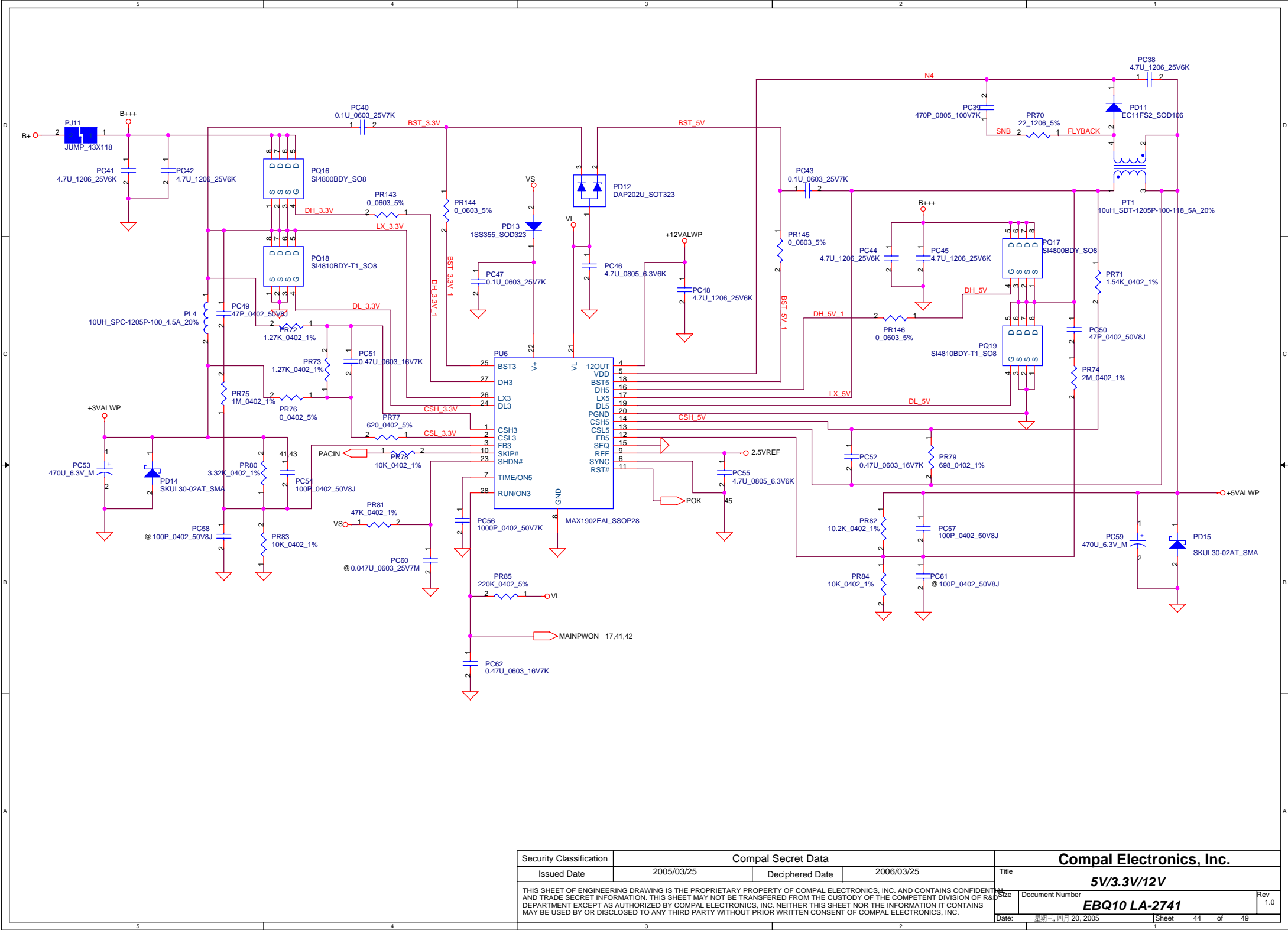
IREF=1.31*Icharge
IREF=0.6~2.92V

+3VALWP

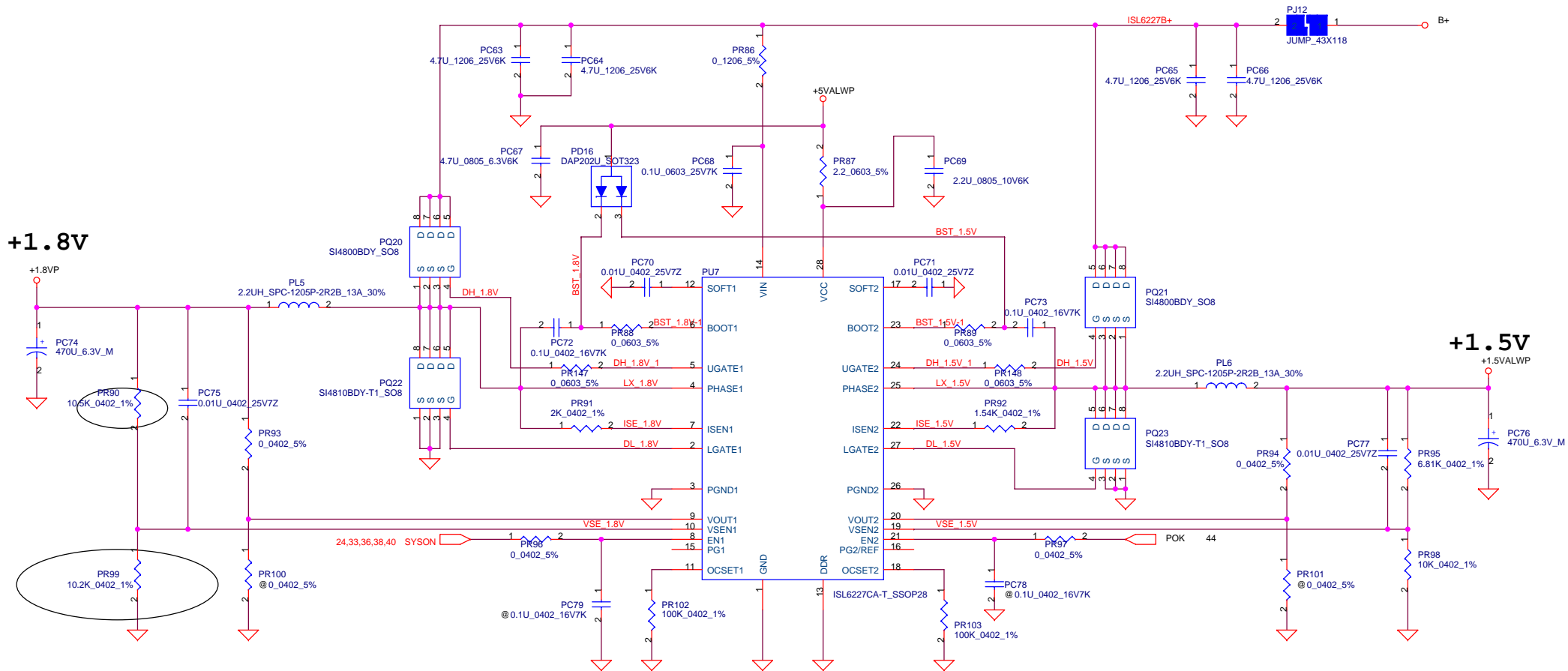
OVP voltage : LI
4S2P : 17.4V--> BATT_OVP= 1.935V
(BAT_OVP=0.1111 *VMB)

CC=0.5~2.5A
CV=16.8V(8 CELLS LI-ION)

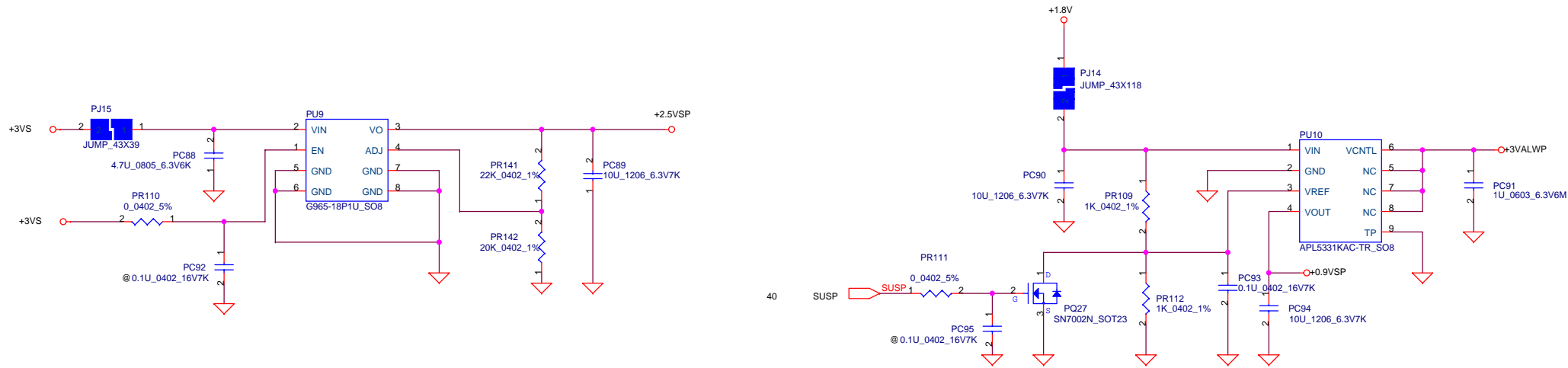
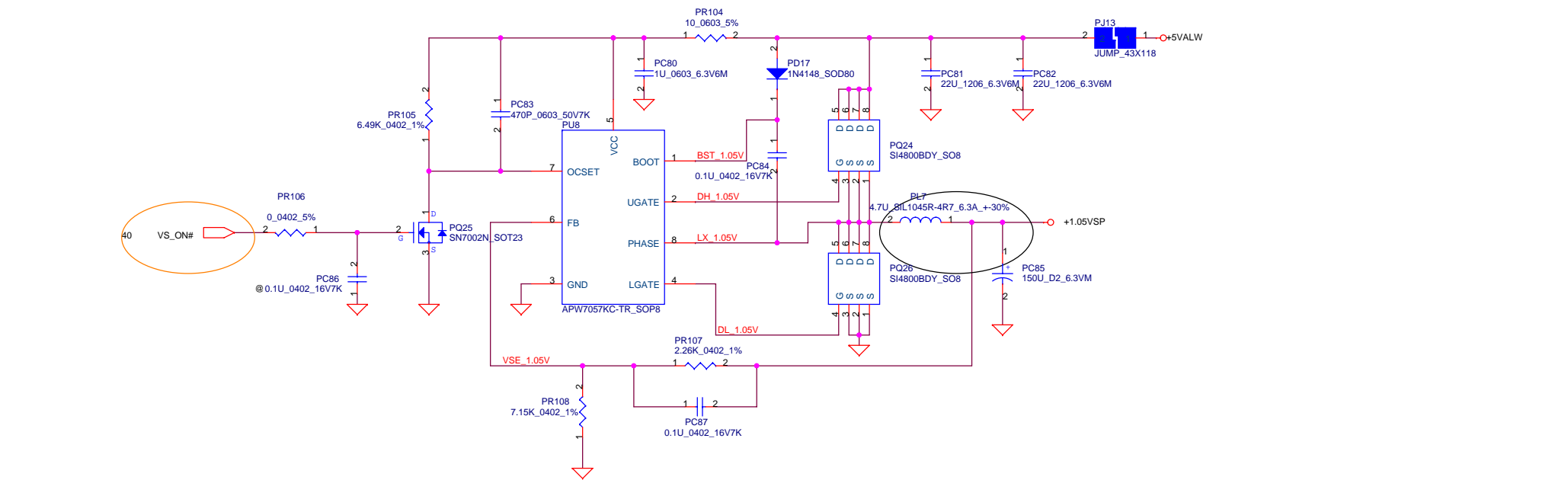
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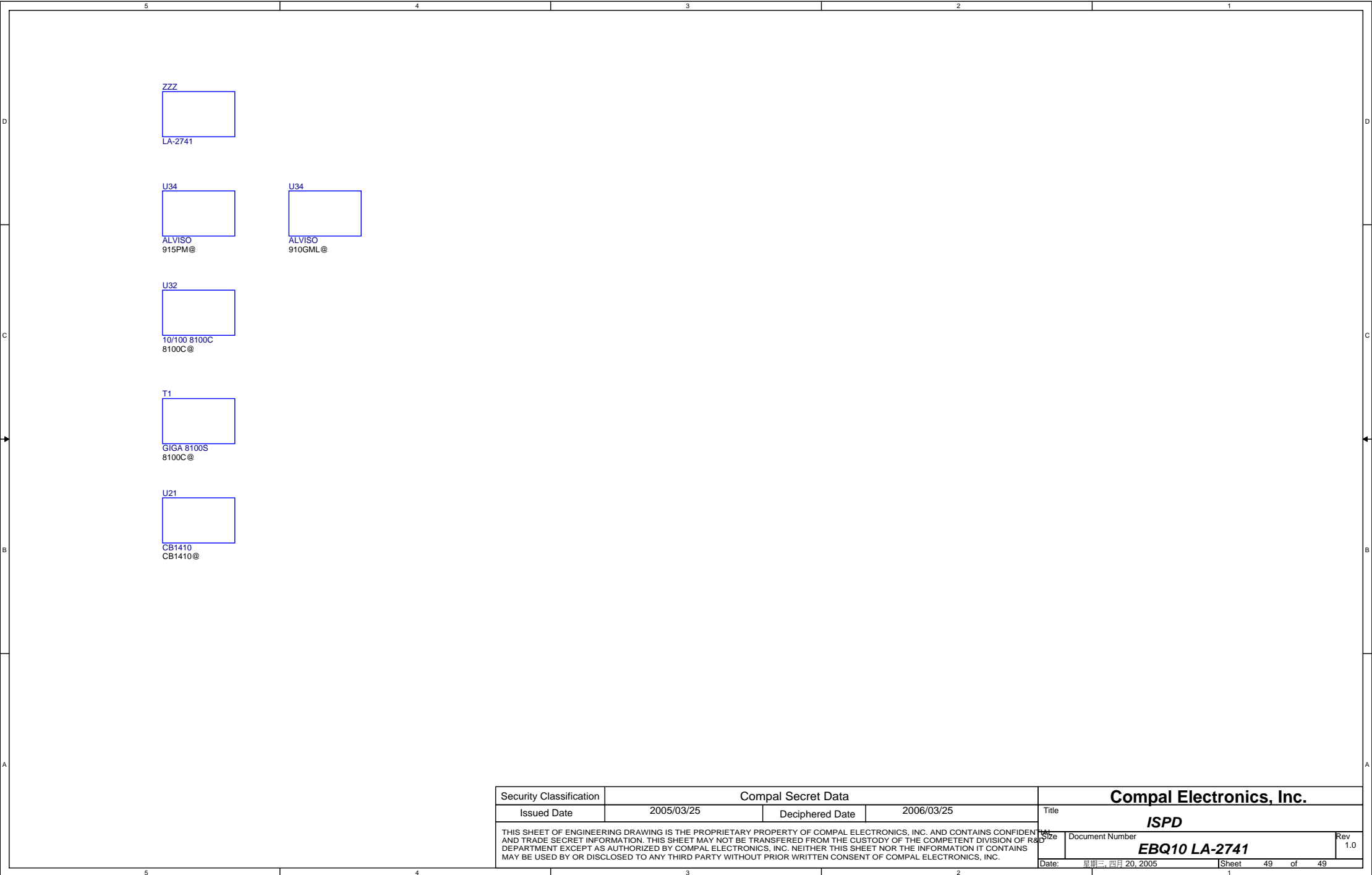


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5					4					3					2					1				
2005.1.31 Change JP17 P/N to SP070012100 Change JP19 P/N to SP010009V00 Change JP23 P/N to SP070005L00 Change JP26 P/N to SP070013200					NO DATE PAGE MODIFICATION LIST PURPOSE																			
					3/24 P.4 Reserve R,C circuit for reboot issue																			
					P.39 Change SW1 footprint																			
					P.37 Change SW7 pin define for LID swith light																			
					P.37 Add D11 for ESD concern																			
					P34 Add EC_NBA_PLUG pin for linux's EQ																			
					P34 Change R173 to 18K for Board ID																			
					P9 Reserve Cap 0.1uF																			
					P29 Delete AV-IN,RF-IN connector																			
					P33 change VR to SMD type																			
2005.2.02 Change 5in1 LED(D28) from Blue to Green Change Power LED(D45), Battery Charge LED(D47) Battery Low LED(D48) to single die LED Remove transistors(Q19,Q21,Q22) Change Q23 from transistor to 2N7002					3/25 P.5 Add R729 for 3Dmark2003 issue																			
					3/29 P.29 Delete Mini_PCI (TV tuner connector)																			
					4/2 P.40 Delete H24,H32																			
					4/4 P.14 Change R7,R8,R9 to 75ohm 1%																			
2005.2.04 Change U19 to G528					P.31 modify U46D circuit																			
					P.39 modify U35B circuit																			
					P.15 Add L32-L35 for EMI's request																			
					4/6 P.36 Modify Power LED and Suspend LED																			
2005.2.05 Add C161,C162 and @C154					4/15 P.38 Modify schematic for Lid switch																			
					4/25 P.11 ADD C730,C731,C732,C733 for EMI request																			
2005.2.15 ADD R586 (0 ohm) between 1394 GRST# and PCI_RST# R108 @ ADD SPEAKER_ID between EC and Codec Connect WLAN and BT with R589(0 ohm),R590(100k pull low),R591(0 ohm) and R592(100k pull low)					4/25 P.17 ADD C734 for HW request																			
2005.2.16 R73 on with 8100CL and 8110S Use SM bus into Codec Swap BT connector Add Page32 HW EQ																								
2005.2.18 Change H28 digital GND to analog GND Swap back the BT connector																								
2005.2.21 Add R611 and R612 to NOEQ@ C161,C162 change to 330uF R108 Change to 220K ohm R590,R592 change to @ Change D40 and R578 to @ Change 5in1 LED to +3VS and R570 to 150 ohm. Change R91 to 180K ohm and R155 to 220K ohm Add two 10uF on +5VS C711 and C712 Change SATA crystal to Oscillator Change C309 and C316 to 12PF																								
2005.2.23 Help power to updat PL7, PR90 and PR99 Change R164 and R165 to 470ohm Change C350 to 4.7UF; Change C382 to @																								
2005.2.24 Add R625 and R626 @: remove H25 Change H28 to digital GND Add R629 0 ohm on U19.5 FLG pin Help power to update PR20 and PR21 to 510 ohm																								
2005.3.2 Add KBC Cap. for EMI's request on p36																								



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