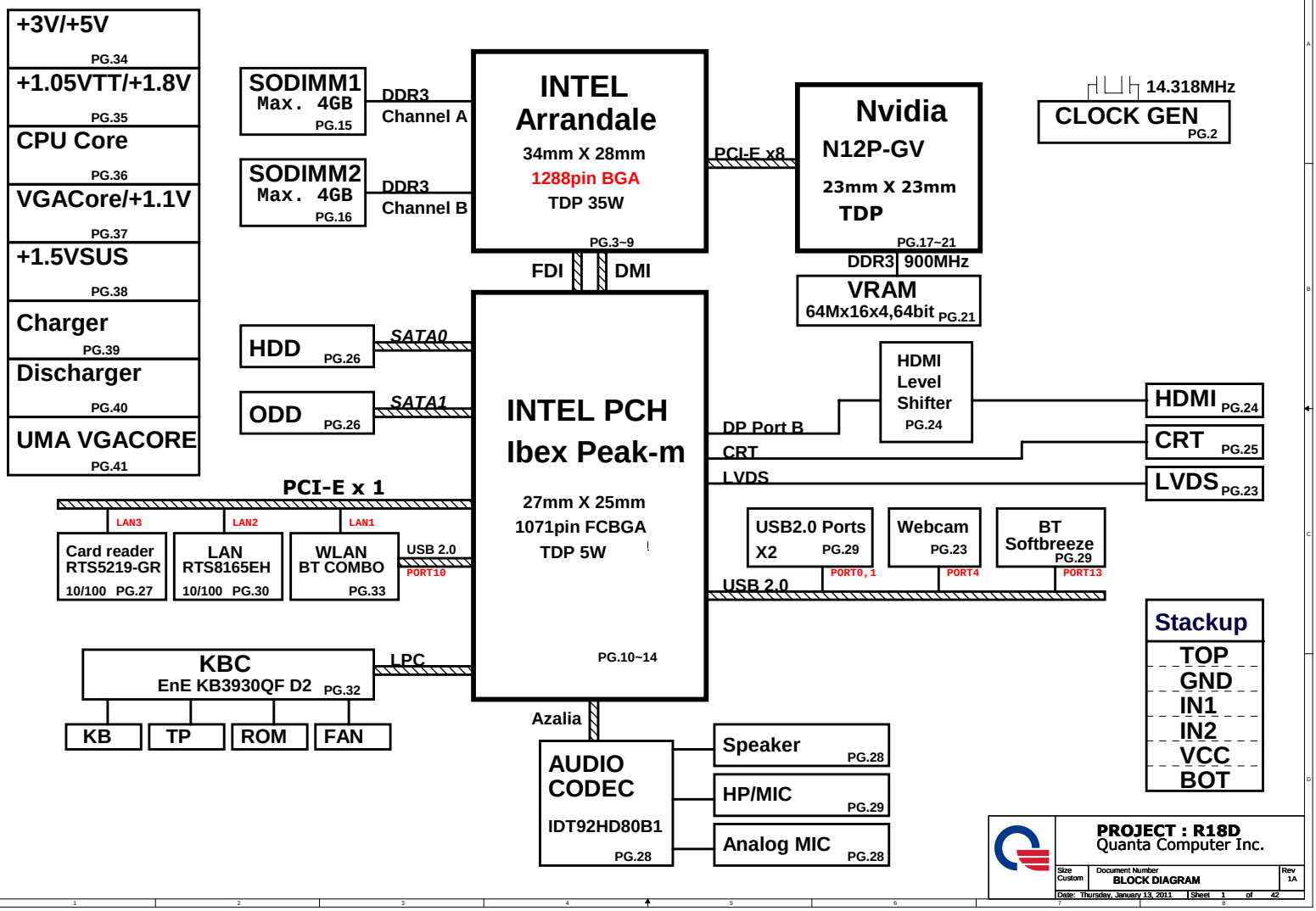
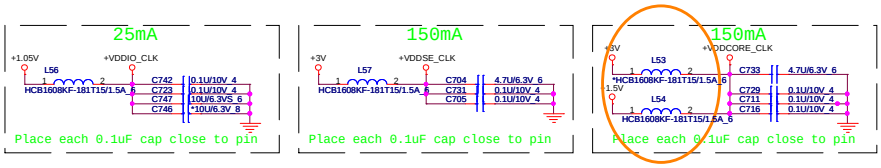
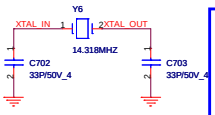
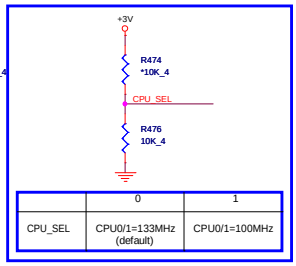
R18D INTEL UMA/DISCRETE SYSTEM DIAGRAM

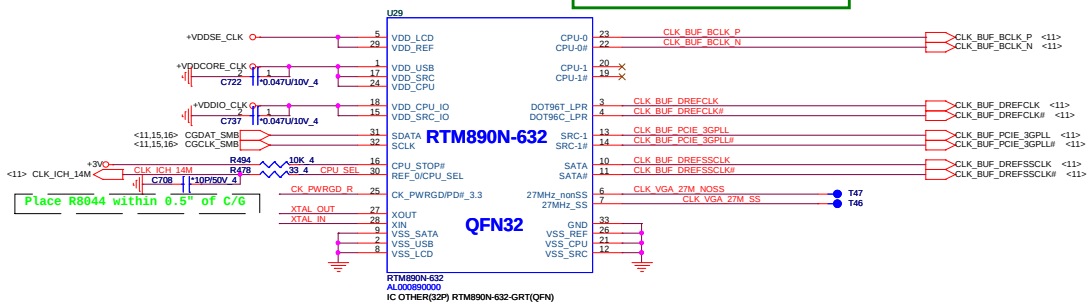


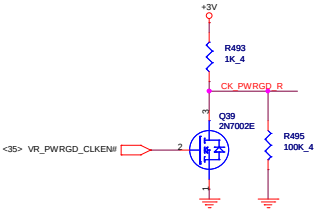






0510 add for WiMAX close to U13





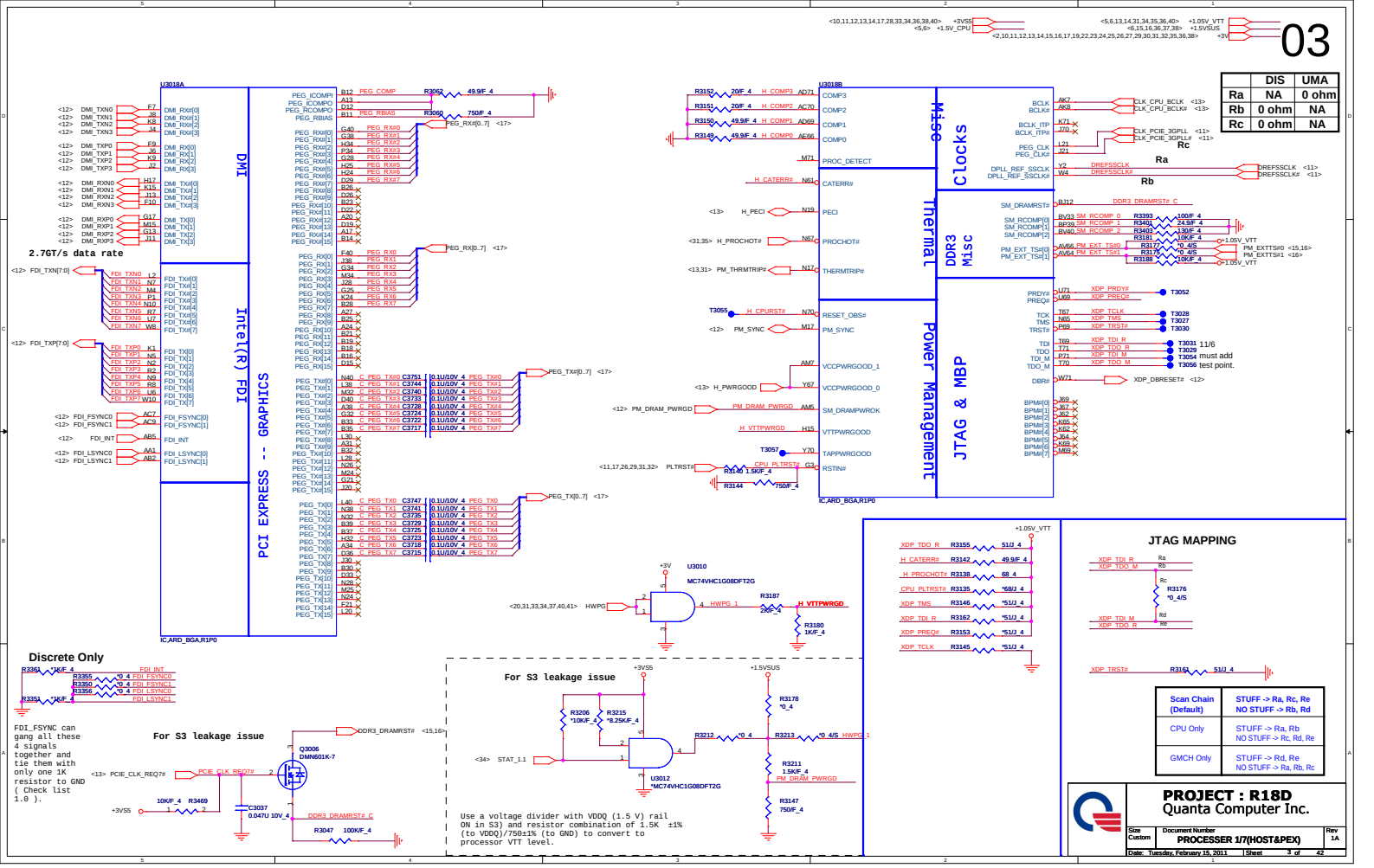
Vender	Part	Part Number	Part Description
ICS	ICS9LVS3197	AL003197001	IC OTHER(32P) ICS9LVS3197AKLFT(MLF)
Realtek	RTM890N-632	AL000890000	IC OTHER(32P) RTM890N-632-GRT(QFN)
Silego	SLG8LV595VTR	AL000595000	IC OTHER(32P)SLG8LV595VTR(QFN)

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Gen(9LRS3197)	1A

Date: Tuesday, February 15, 2011 Sheet 2 of 42

	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

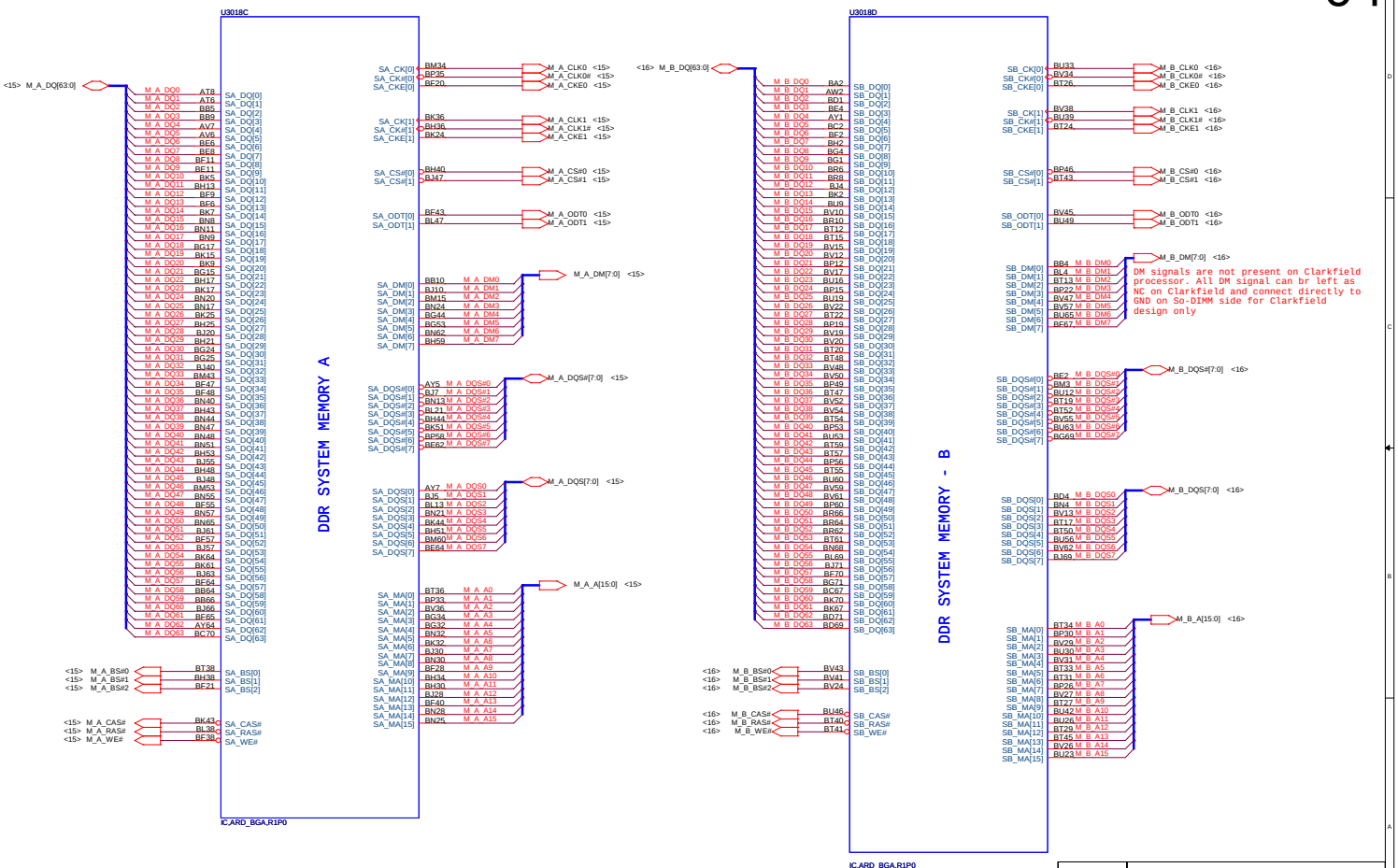


Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 1/7(HOST&PEX)	1A
Date: Tuesday, February 15, 2011	Sheet 3 of 42	

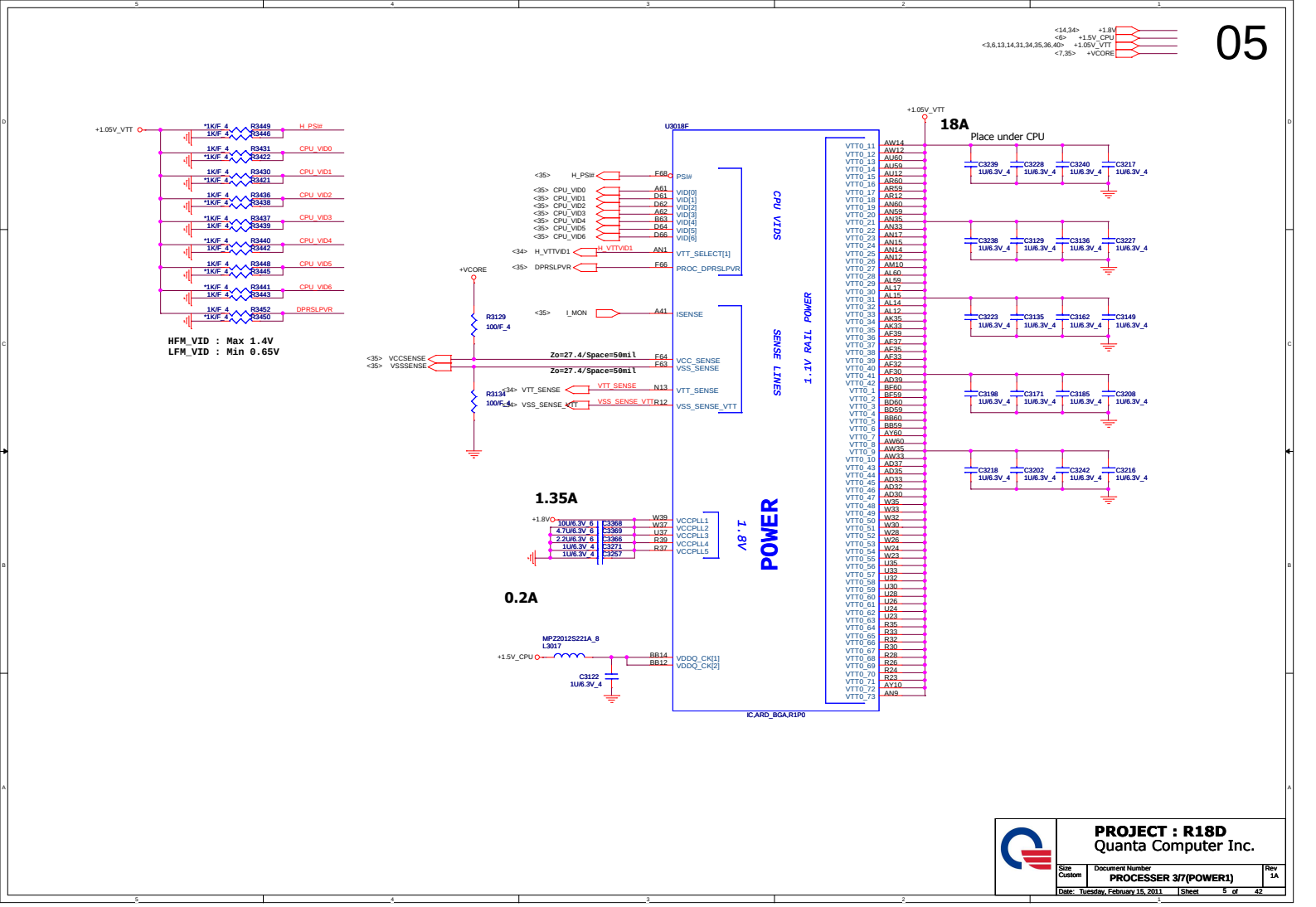
ARRANDALE/CLARKSFIELD PROCESSOR (DDR3)



PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 2/7(DDR3)	1A

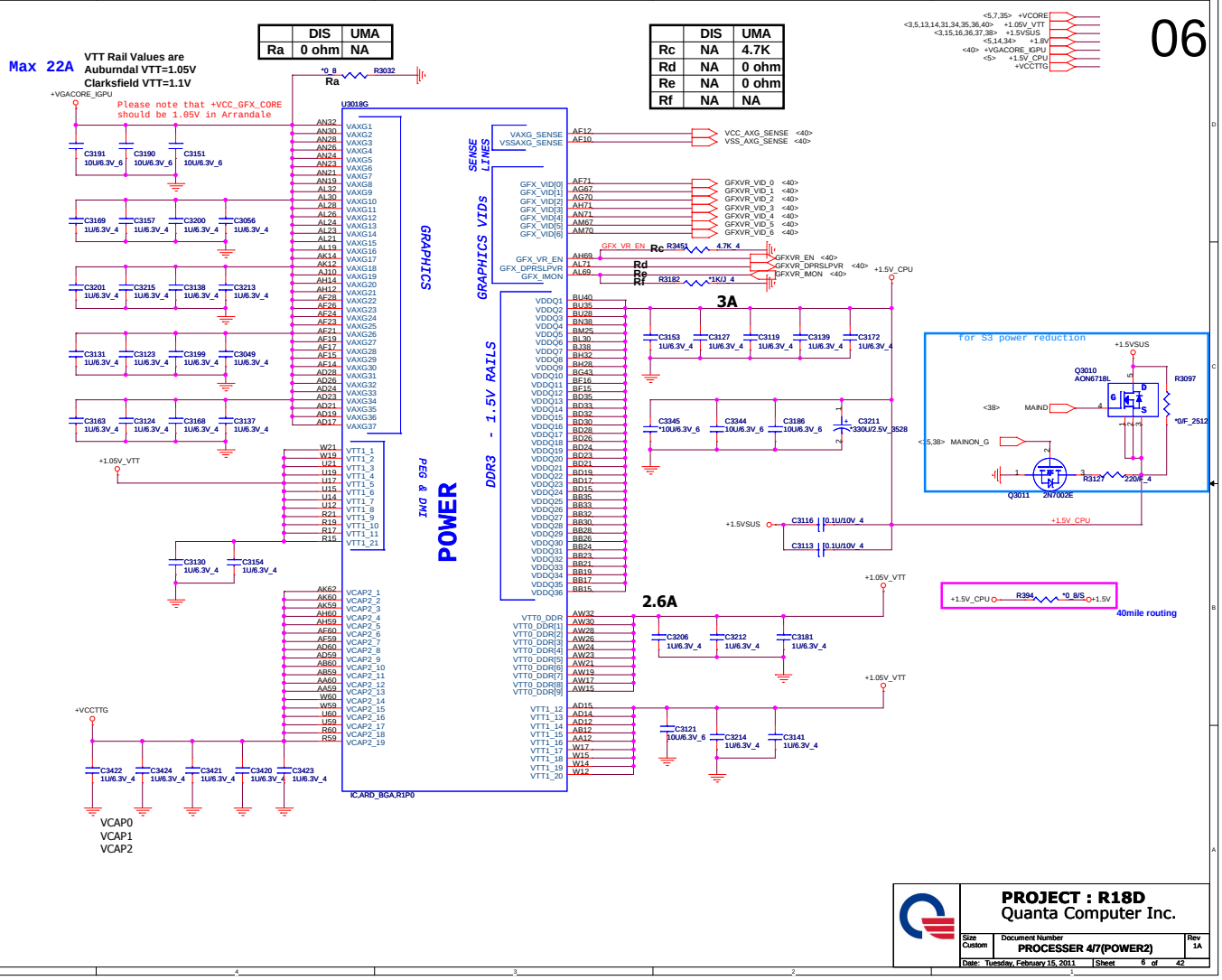
Date: Tuesday, February 15, 2011 | Sheet 4 of 42



PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 3/7(POWER1)	1A

Date: Tuesday, February 15, 2011 Sheet 5 of 42



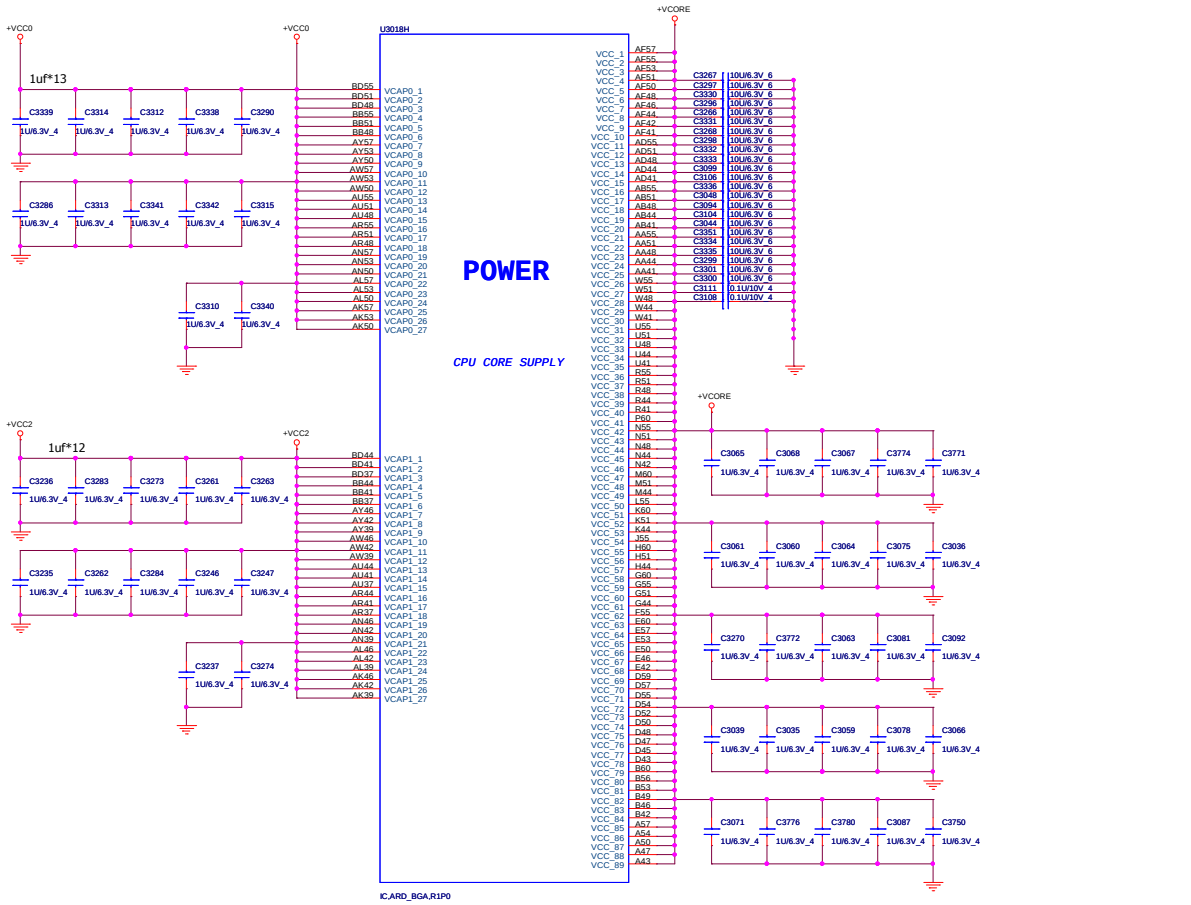
	DIS	UMA
Ra	0 ohm	NA

	DIS	UMA
Rc	NA	4.7K
Rd	NA	0 ohm
Re	NA	0 ohm
Rf	NA	NA

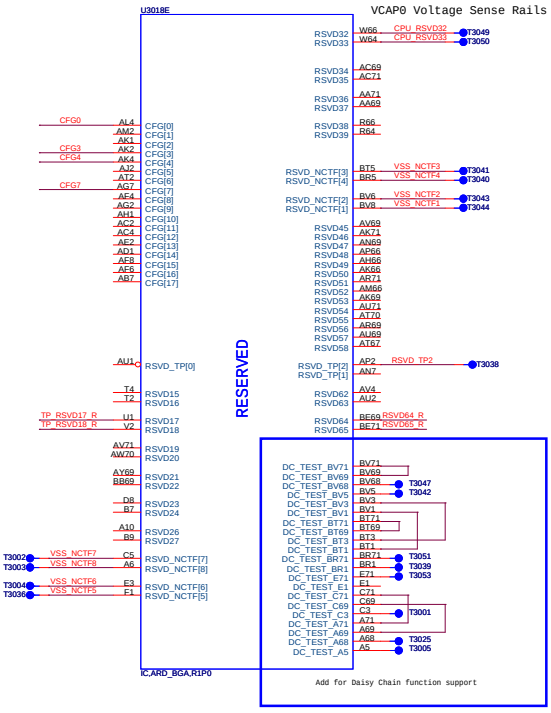
PROJECT : R18D
Quanta Computer Inc.

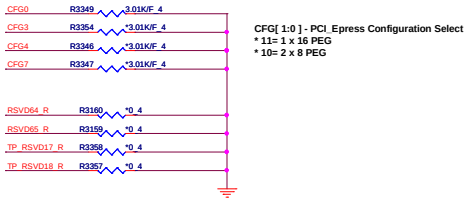
Size	Document Number	Rev
Custom	PROCESSER 4/7(POWER2)	1A

Date: Tuesday, February 15, 2011 | Sheet 6 of 42



PROJECT : R18D	
Quanta Computer Inc.	
Size: Custom	Document Number: PROCESSER 5/7(POWER3)
Rev: 1A	
Date: Tuesday, February 15, 2011	Sheet 7 of 42





	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

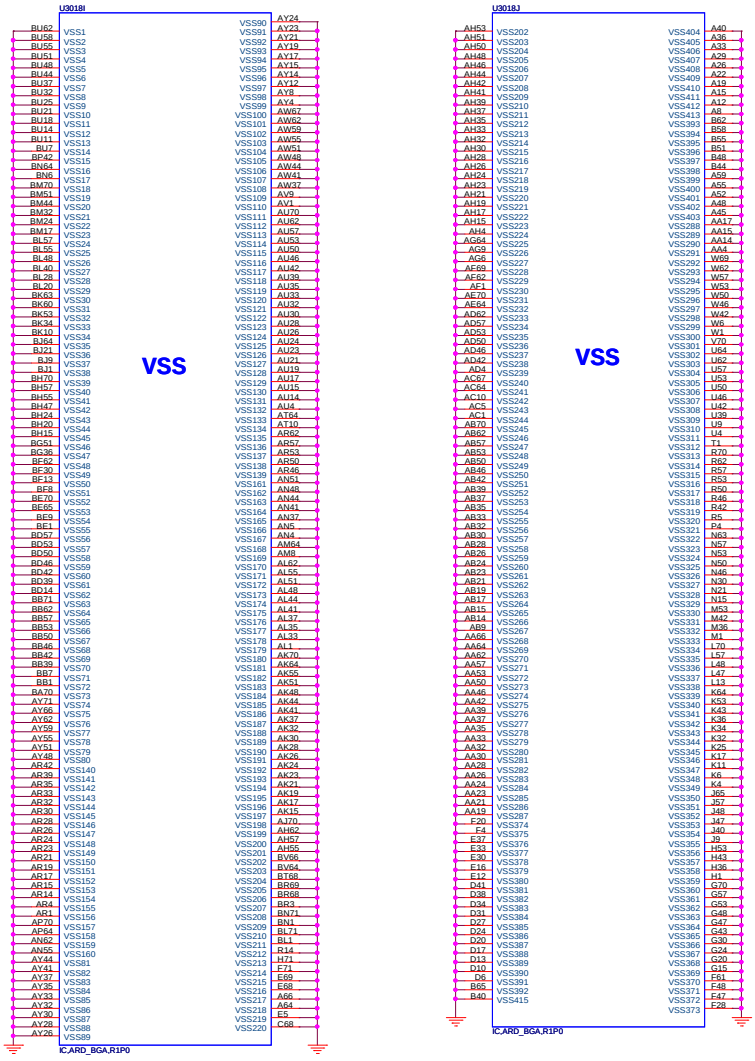
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 6/7(CFG)	1A

Date: Friday, January 14, 2011 | Sheet 8 of 42

ARRANDALE PROCESSOR (GND)



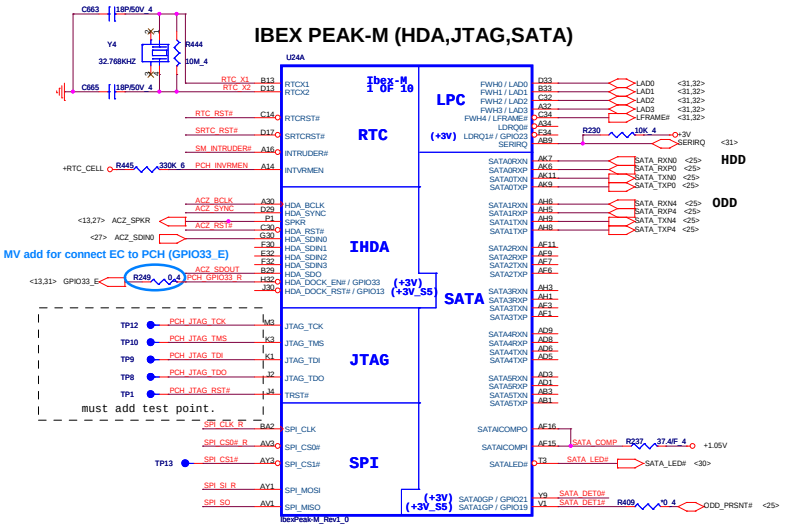
PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 7/7(GND)	1A

Date: Thursday, January 13, 2011 Sheet 9 of 42

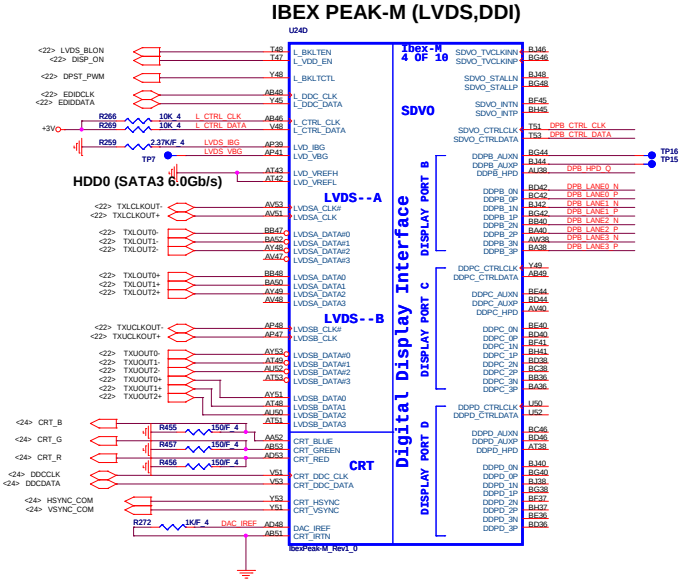
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)



UMA CRT,LVDS&HDMI signals

IBEX PEAK-M (LVDS,DDI)



1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

For ES1 ONLY.NI for ES2.

For ES1 ONLY.NI for ES2.

UMA HDMI signals

10/25 PV modify

10/25 PV modify

Part
Part Number
Part Description

For AUDIO

For MDC

RTC

1mA

8/25 SI for M/E.

4M byte SPI ROM

U22
W25Q32BVSSIG
AKE391P0N00
IC FLASH(8P) W25Q32BVSSIG(SOIC)

Vender
Socket DG008000031
EON - EN25F32-100HIP
AKE39FN0Q00 IC FLASH(8P) EN25F32-100HIP (SOIC)
WINBOND - W25Q32BVSSIG
AKE391P0N00 IC FLASH(8P) W25Q32BVSSIG(SOIC)

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/5 (SATA,HDA,LPC)	1A
Date: Tuesday, February 15, 2011	Sheet 10 of 42	

IBEX PEAK-M (GND)

U24I

AY2	VSS[159]	VSS[259]	H49
B11	VSS[160]	VSS[260]	H5
B15	VSS[161]	VSS[261]	J24
B19	VSS[162]	VSS[262]	K11
B23	VSS[163]	VSS[263]	K43
B31	VSS[164]	VSS[264]	K47
B35	VSS[165]	VSS[265]	K7
B39	VSS[166]	VSS[266]	L14
B43	VSS[167]	VSS[267]	L18
B47	VSS[168]	VSS[268]	L2
B7	VSS[169]	VSS[269]	L22
BC12	VSS[170]	VSS[270]	L32
BB12	VSS[171]	VSS[271]	L36
BB16	VSS[172]	VSS[272]	L40
BB20	VSS[173]	VSS[273]	L52
BB24	VSS[174]	VSS[274]	M12
BB30	VSS[175]	VSS[275]	M16
BB34	VSS[176]	VSS[276]	M20
BB38	VSS[177]	VSS[277]	N38
BB42	VSS[178]	VSS[278]	M34
BB46	VSS[179]	VSS[279]	M38
BB5	VSS[180]	VSS[280]	M42
BC10	VSS[181]	VSS[281]	M46
BC14	VSS[182]	VSS[282]	M49
BC18	VSS[183]	VSS[283]	M5
BC2	VSS[184]	VSS[284]	M8
BC22	VSS[185]	VSS[285]	N24
BC32	VSS[186]	VSS[286]	P11
BC36	VSS[187]	VSS[287]	AD15
BC40	VSS[188]	VSS[288]	P22
BC44	VSS[189]	VSS[289]	P30
BC52	VSS[190]	VSS[290]	P32
BH9	VSS[191]	VSS[291]	P34
BD48	VSS[192]	VSS[292]	P42
BD49	VSS[193]	VSS[293]	P45
BD5	VSS[194]	VSS[294]	P47
BE12	VSS[195]	VSS[295]	R2
BE16	VSS[196]	VSS[296]	R52
BE20	VSS[197]	VSS[297]	T12
BE24	VSS[198]	VSS[298]	T41
BE30	VSS[199]	VSS[299]	T46
BE34	VSS[200]	VSS[300]	T49
BE38	VSS[201]	VSS[301]	T5
BE42	VSS[202]	VSS[302]	T8
BE46	VSS[203]	VSS[303]	U30
BE48	VSS[204]	VSS[304]	U31
BE50	VSS[205]	VSS[305]	U32
BE6	VSS[206]	VSS[306]	U34
BE8	VSS[207]	VSS[307]	P38
BF3	VSS[208]	VSS[308]	V11
BF49	VSS[209]	VSS[309]	P16
BF51	VSS[210]	VSS[310]	V19
BG18	VSS[211]	VSS[311]	V20
BG24	VSS[212]	VSS[312]	V22
BG4	VSS[213]	VSS[313]	V30
BG50	VSS[214]	VSS[314]	V31
BH11	VSS[215]	VSS[315]	V32
BH15	VSS[216]	VSS[316]	V34
BH19	VSS[217]	VSS[317]	V35
BH23	VSS[218]	VSS[318]	V38
BH31	VSS[219]	VSS[319]	V43
BH35	VSS[220]	VSS[320]	V45
BH39	VSS[221]	VSS[321]	V46
BH43	VSS[222]	VSS[322]	V47
BH47	VSS[223]	VSS[323]	V49
BH7	VSS[224]	VSS[324]	V5
C12	VSS[225]	VSS[325]	V7
C50	VSS[226]	VSS[326]	V8
D51	VSS[227]	VSS[327]	W2
E12	VSS[228]	VSS[328]	W52
E16	VSS[229]	VSS[329]	Y11
E20	VSS[230]	VSS[330]	Y12
E24	VSS[231]	VSS[331]	Y15
E30	VSS[232]	VSS[332]	Y19
E34	VSS[233]	VSS[333]	Y23
E38	VSS[234]	VSS[334]	Y28
E42	VSS[235]	VSS[335]	Y30
E46	VSS[236]	VSS[336]	Y31
E48	VSS[237]	VSS[337]	Y32
E6	VSS[238]	VSS[338]	Y38
E8	VSS[239]	VSS[339]	Y43
F49	VSS[240]	VSS[340]	Y46
F5	VSS[241]	VSS[341]	Y49
G10	VSS[242]	VSS[342]	Y5
G14	VSS[243]	VSS[343]	Y6
G18	VSS[244]	VSS[344]	Y8
G2	VSS[245]	VSS[345]	P24
G22	VSS[246]	VSS[346]	T43
G26	VSS[247]	VSS[347]	AD51
G36	VSS[248]	VSS[348]	AT8
G40	VSS[249]	VSS[349]	AU7
G44	VSS[250]	VSS[350]	V47
G52	VSS[251]	VSS[351]	AT12
AE39	VSS[252]	VSS[352]	AM6
H16	VSS[253]	VSS[353]	AT13
H20	VSS[254]	VSS[354]	AM5
H30	VSS[255]	VSS[355]	AK45
H34	VSS[256]	VSS[356]	AK39
H38	VSS[257]	VSS[366]	AV14
H42	VSS[258]		

IbexPeak-M_Rev1_0

IBEX PEAK-M (PCI-E,SMBUS,CLK)

U24B

Ibex-M 2 OF 10

PCI-E*

[WLAN]
<32> PCIE_RXN1 — PCIE_RXN1 BG30
<32> PCIE_RXP1 — PCIE_RXP1 BJ30
<32> PCIE_TXN1 — C450 0.1U/10V_4 — PCIE_TXN1_C BC29
<32> PCIE_TXP1 — C449 0.1U/10V_4 — PCIE_TXP1_C BH29

[LAN]
<29> PCIE_RXN2_LAN — PCIE_RXN2_LAN AW30
<29> PCIE_RXP2_LAN — PCIE_RXP2_LAN BA30
<29> PCIE_TXN2_LAN — C458 0.1U/10V_4 — PCIE_TXN2_C BC30
<29> PCIE_TXP2_LAN — C459 0.1U/10V_4 — PCIE_TXP2_C BD30

Cardreader
<26> PCIE_RXN3_CARD — AU30
<26> PCIE_RXP3_CARD — AT30
<26> PCIE_TXN3_CARD — C460 0.1U/10V_4 — PCIE_TXN3_CARD_C AU32
<26> PCIE_TXP3_CARD — C461 0.1U/10V_4 — PCIE_TXP3_CARD_C AV32

PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6 PERP6 PETN6 PETP6
PERN7 PERP7 PETN7 PETP7
PERN8 PERP8 PETN8 PETP8

MiniWLAN
<32> CLK_PCIE_WLANN — AM43 CLKOUT_PCIE1N
<32> CLK_PCIE_WLANP — AM45 CLKOUT_PCIE1P
<32> PCIE_CLKREQ_WLAN# — U4 PCIECLKRQ1# / GPIO18 (+3V)

<26> CLK_PCIE_CARDN — AM47 CLKOUT_PCIE2N
<26> CLK_PCIE_CARDP — AM48 CLKOUT_PCIE2P
<26> CLK_PCIE_REQ2# — N4 PCIECLKRQ2# / GPIO20 (+3V)

LAN
<29> CLK_PCIE_LANN — AH42 CLKOUT_PCIE3N
<29> CLK_PCIE_LANP — AH41 CLKOUT_PCIE3P
<29> PCIE_CLKREQ_LAN# — A8 PCIECLKRQ3# / GPIO25 (+3V_S5)

AM51 CLKOUT_PCIE4N
AM53 CLKOUT_PCIE4P
PCIE_CLK_REQ4# — M9 PCIECLKRQ4# / GPIO26 (+3V_S5)

AJ50 CLKOUT_PCIE5N
AJ52 CLKOUT_PCIE5P
PCIE_CLK_REQ5# — H6 PCIECLKRQ5# / GPIO44 (+3V_S5)

AK53 CLKOUT_PEG_B_N
AK51 CLKOUT_PEG_B_P
PCIE_CLK_REQ8# R — P13 PEG_B_CLKRQ# / GPIO56 (+3V_S5)

PCIE_CLK_REQ0# — P9 PCIECLKRQ0# / GPIO73 (+3V_S5)

SMBus

(+3V_S5) SMBALERT# / GPIO11
SMBCLK
SMBDATA
(+3V_S5) SMBLOALERT# / GPIO60
SML0CLK
SML0DATA
(+3V_S5) SML1ALERT# / GPIO74
(+3V_S5) SML1CLK / GPIO58
(+3V_S5) SML1DATA / GPIO75

+3VS5
B9 SMBALERT# 10K_4 R442
H14 PCLK_SMB 2.2K_4 R189
C8 PDAT_SMB 2.2K_4 R208
J14 SMBLOALERT# 10K_4 R238
C6 SMB_CLK_ME0 2.2K_4 R229
G8 SMB_DATA_ME0 2.2K_4 R212
M14 SML1ALERT# 10K_4 R239
E10 SMB_CLK_ME1 4.7K_4 R216
G12 SMB_DATA_ME1 4.7K_4 R227

Controller Link

CL_CLK1 — T13
CL_DATA1 — T11
CL_RST1# — T9

PEG

(+3V_S5) PEG_A_CLKRQ# / GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N1
CLKOUT_DMI_P1

H1 PEG_CLKREQ# — PEG_CLKREQ# <17>
AD43 — CLK_PCIE_VGA# <17>
AD45 — CLK_PCIE_VGA <17>
AN4 — CLK_PCIE_3GPLL# <3>
AN2 — CLK_PCIE_3GPLL <3>

CLKOUT_DP_N / CLKOUT_BCLK1_N
CLKOUT_DP_P / CLKOUT_BCLK1_P
AT1 — DREFSSCLK# <3>
AT3 — DREFSSCLK <3>

From CLK BUFFER

CLKIN_DMI_N — AW24 — CLK_BUF_PCIE_3GPLL# <2>
CLKIN_DMI_P — BA24 — CLK_BUF_PCIE_3GPLL <2>

CLKIN_BCLK_N — AP3 — CLK_BUF_BCLK_N <2>
CLKIN_BCLK_P — AP1 — CLK_BUF_BCLK_P <2>

CLKIN_DOT_96N — F18 — CLK_BUF_DREFCLK# <2>
CLKIN_DOT_96P — E18 — CLK_BUF_DREFCLK <2>

CLKIN_SATA_N / CKSSCD_N — AH13 — CLK_BUF_DREFSSCLK# <2>
CLKIN_SATA_P / CKSSCD_P — AH12 — CLK_BUF_DREFSSCLK <2>

REFCLK14IN — P41 — CLK_ICH_14M <2>
C473 *5.6P/50V_4
CLKIN_PCILOOPBACK — J42 CLK_PCI_FB — CLK_PCI_FB <12>

XTAL25_IN — AH51 — XTAL25_IN
XTAL25_OUT — AH53 — XTAL25_OUT
DIS only
XCLK_RCOMP — AF38 — XCLK_RCOMP
R262 90.9/F_4 +1.05V

Clock Flex

(+3V) CLKOUTFLEX0 / GPIO64 — T45 CLK_FLEX0 — T36
(+3V) CLKOUTFLEX1 / GPIO65 — P43 CLK_FLEX1 — T35
(+3V) CLKOUTFLEX2 / GPIO66 — T42 CLK_FLEX2 — T34
(+3V) CLKOUTFLEX3 / GPIO67 — N50 CLK_FLEX3 — T37

IbexPeak-M_Rev1_0

PCIE_CLKREQ_WLAN# — R429 10K_4 — CLK_PCIE_REQ2# — R198 10K_4 — +3V
PCIE_CLK_REQ0# — R231 10K_4 — +3VS5
PCIE_CLKREQ_LAN# — R215 10K_4
PCIE_CLK_REQ4# — R193 10K_4
PCIE_CLK_REQ8# R — R240 10K_4
PCIE_CLK_REQ5# — R217 10K_4
PEG_CLKREQ# — Ra R417 *10K_4 — Rb R418 *10K_4
Ra: UMA
Rb: Muxless

SMB_CLK_ME1 — Q36 2N7002E — R446 2.2K_4 — MBCLK2 <16,31>
+3VO — R448 2.2K_4
SMB_DATA_ME1 — Q37 2N7002E — MBDATA2 <16,31>

PDAT_SMB — Q12 2N7002E — R191 10K_4 — CGDAT_SMB <2,15,16>
+3VO — R190 10K_4
PCLK_SMB — Q13 2N7002E — CGCLK_SMB <2,15,16>

+3VS5
U21 *MC74VHC1G08DFT2G
C658 *0.1U/10V_4
<12> PLT_RST-R# — PLTRST# <3,17,26,29,31,32>
R439 100K_4
R423 *0_4/S — 10/25 PV modify
R421 *100K_4

<2,10,12,14,41> +1.05V
<2,3,10,12,13,14,15,16,17,19,22,23,24,25,26,27,29,30,31,32,35,36,38> +3V

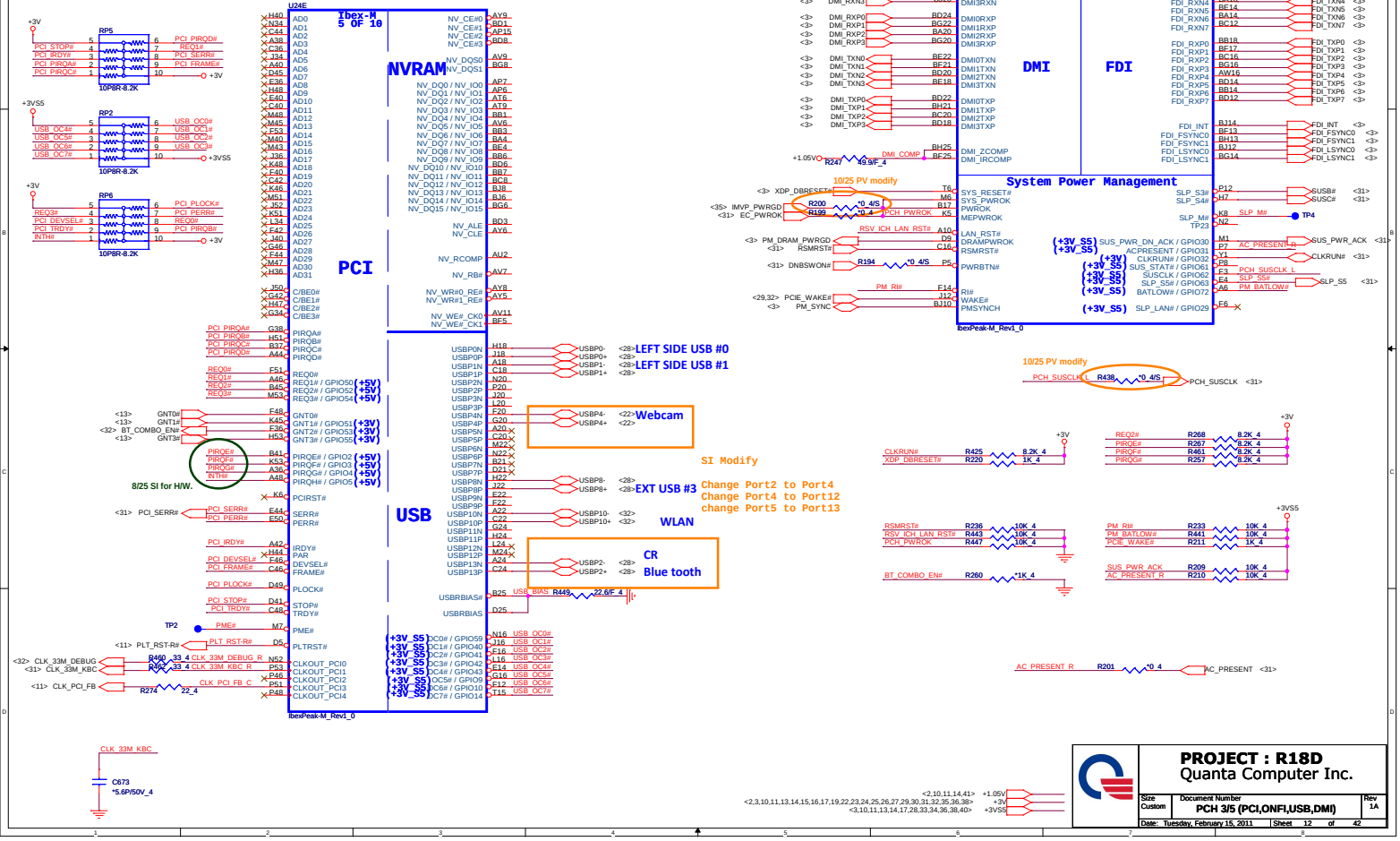
UMA only
XTAL25_IN — R454 1M_4 — Y5 25MHZ — XTAL25_OUT
C668 27P/50V_4
8/25 SI for TXC.
C669 33P/50V_4

PROJECT : R18D
Quanta Computer Inc.

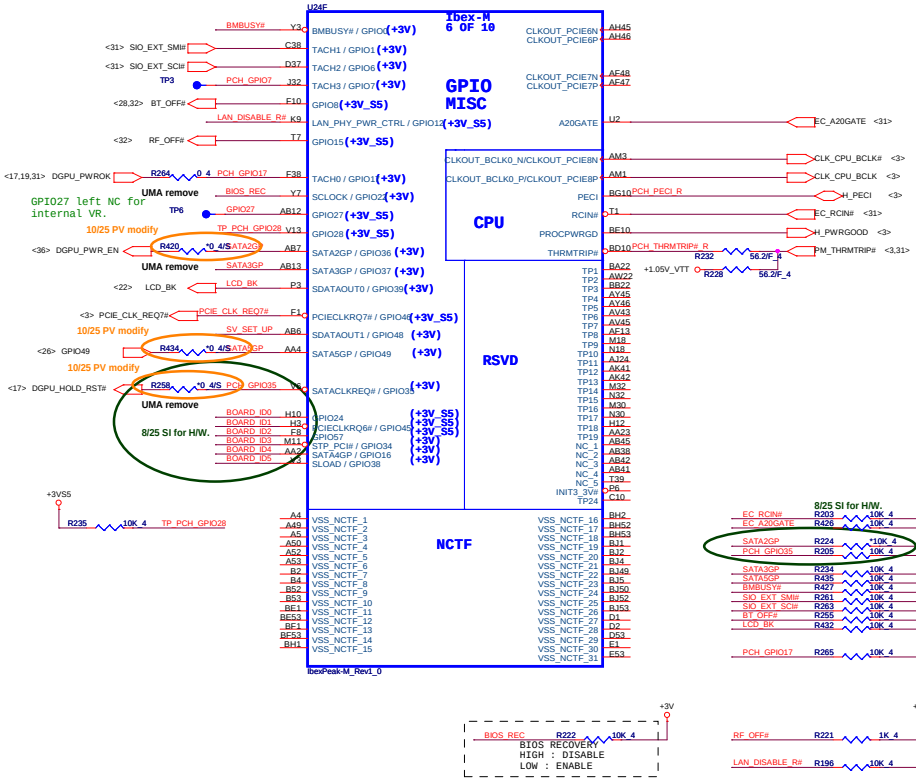
Size	Document Number	Rev
Custom	PCH 2/5 (PCIE, SMBUS, CK)	1A
Date: Tuesday, February 15, 2011	Sheet 11 of 42	

IBEX PEAK-M (DMI,FDI,GPIO)

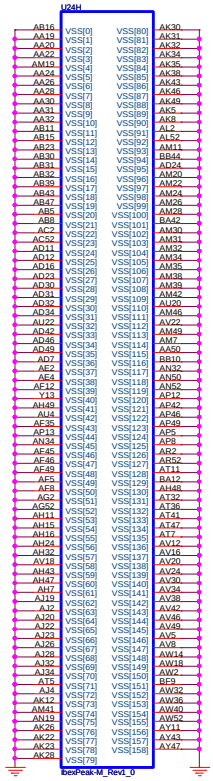
IBEX PEAK-M (PCI,USB,NVRAM)

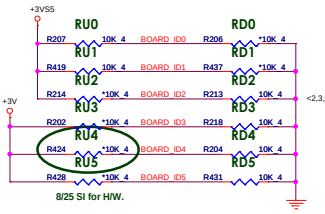


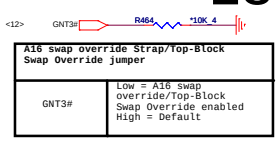
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

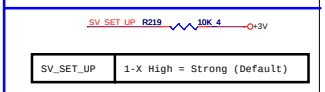


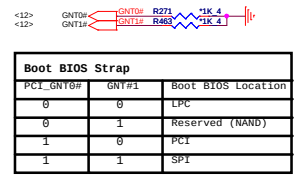
IBEX PEAK-M (GND)

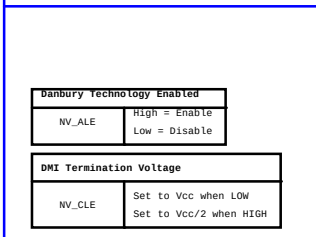










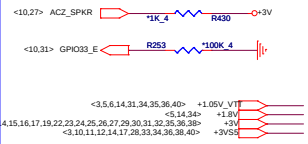


No Reboot Strap

R12 MB P/N	ID0	ID1	ID2	ID3	ID4	ID5
UMA						
31R12MB0000 (PIM)	0	0	0	0	0	0
31R12MB0010 (PDT)	0	0	0	0	0	0
Seymour XT Hynix 512						
31R12MB0020 (PIM)	1	0	0	0	0	0
31R12MB0030 (PDT)	1	0	0	0	0	0
Samsung 512						
31R12MB0040 (PIM)	1	0	0	0	0	0
31R12MB0050 (PDT)	1	0	0	0	0	0
Hynix 1G						
31R12MB0060 (PIM)	1	0	0	0	0	0
31R12MB0070 (PDT)	1	0	0	0	0	0
Samsung 1G						
31R12MB0080 (PIM)	1	0	0	0	0	0
31R12MB0090 (PDT)	1	0	0	0	0	0

Board ID	ID0 GPIO24	ID1 GPIO45	ID2 GPIO57	ID3 GPIO34	ID4 GPIO35	ID5 GPIO38
UMA/DIS	0=UMA 1=Dis.					
1.1/1.0		1=1.1 0=1.0				
Reserve			0=No 1=Yes			
Reserve				0=No 1=Yes		
Reserve					0=No 1=Yes	
Reserve						0=No 1=Yes

BOARD_ID1設成HIGH代表Rockey 1.1

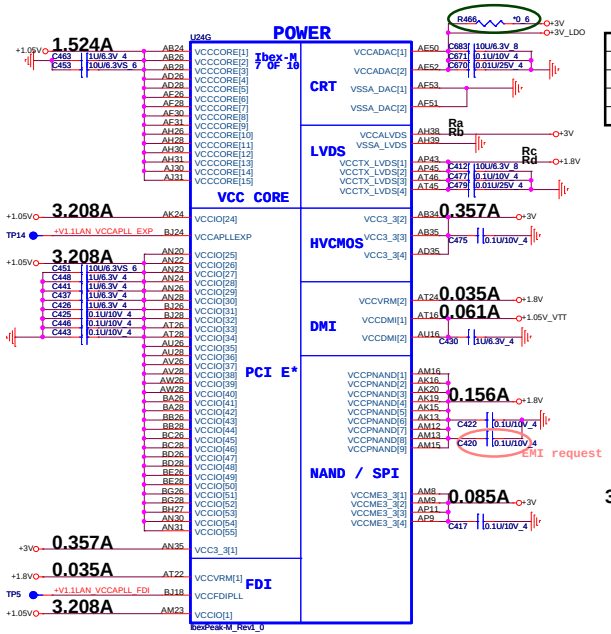


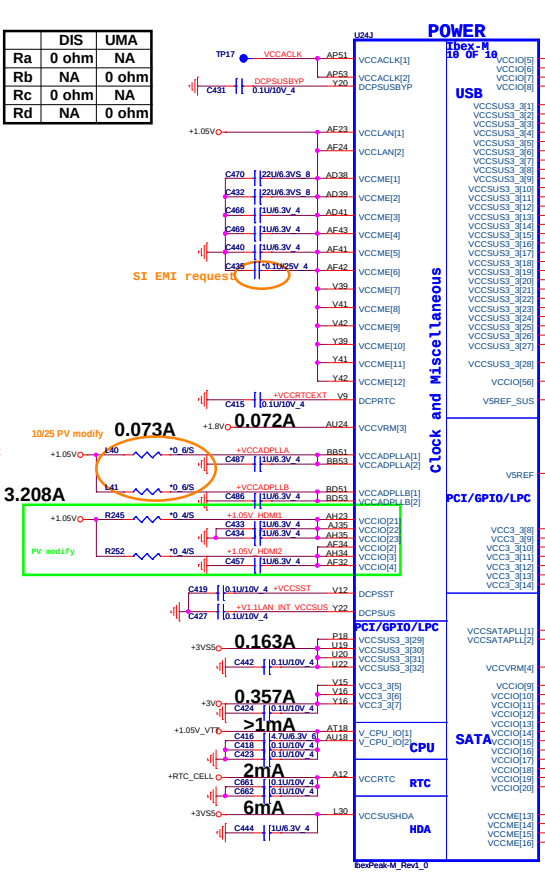
PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/5 (GPIO & Strap)	1A
Date: Tuesday, February 15, 2011	Sheet 13 of 42	

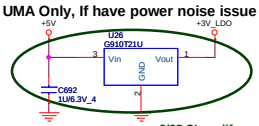
8/25 SI modify
Uninstall on UMA
Install on DIS

	DIS	UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm

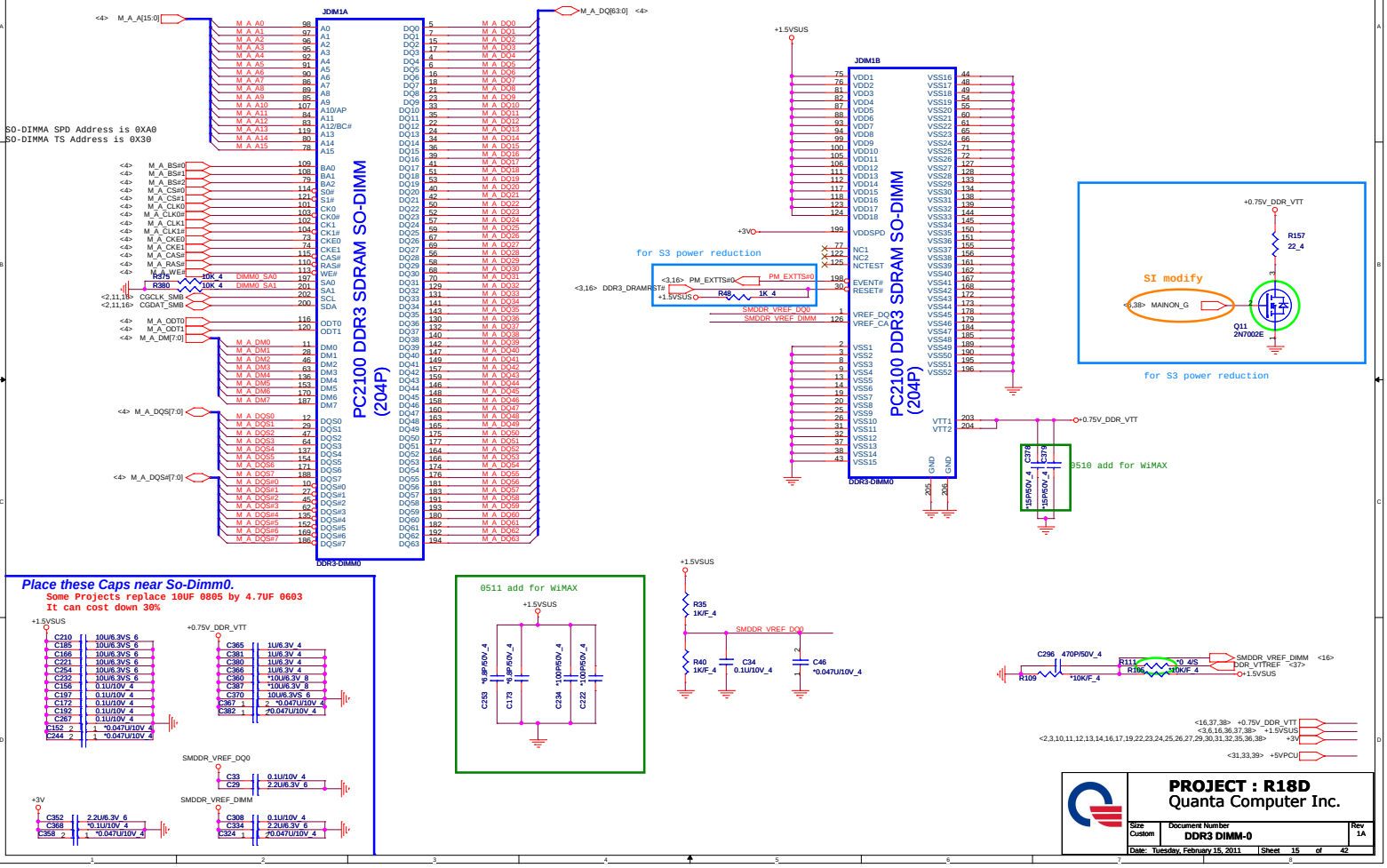


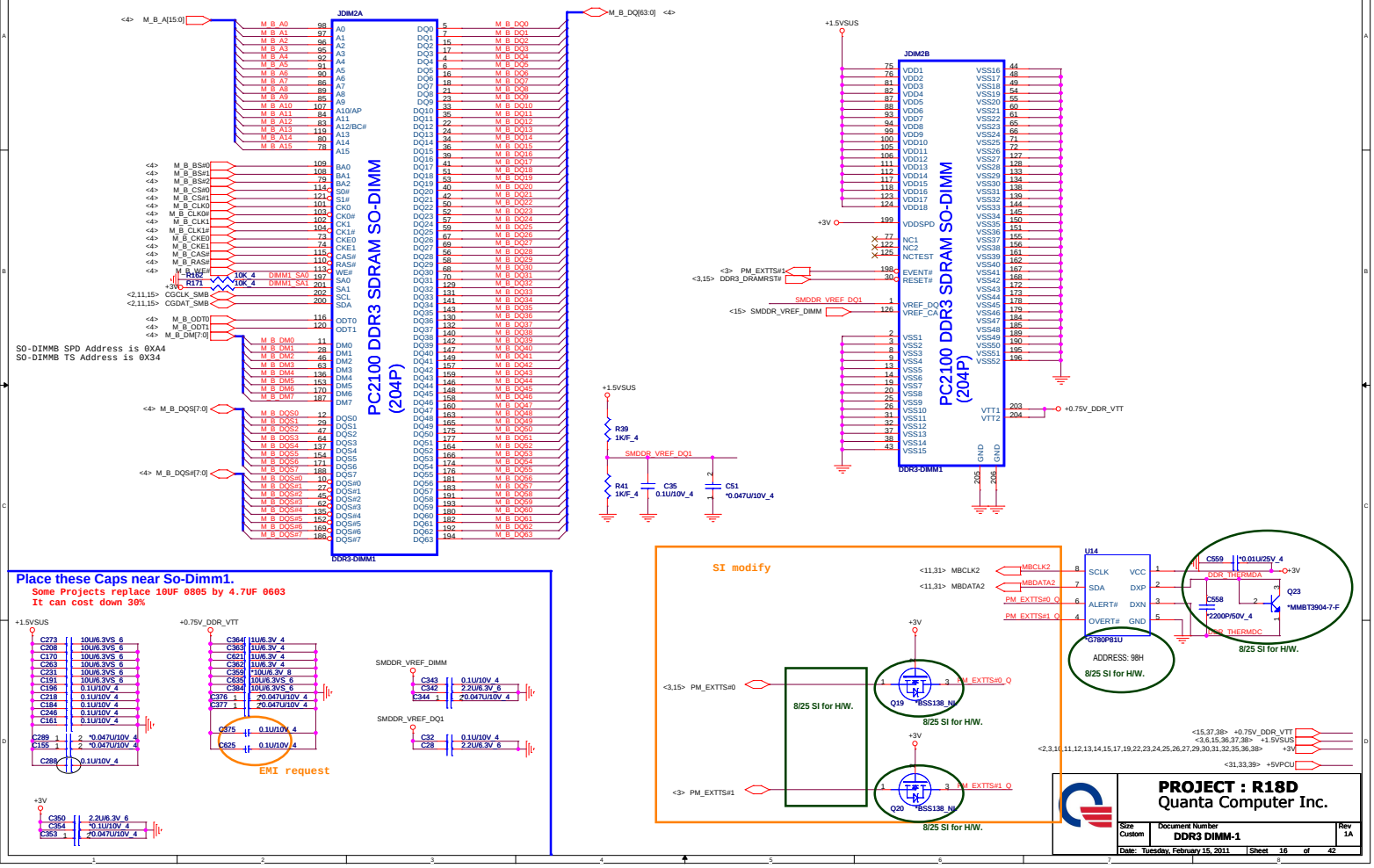


UMA Only, If have power noise issue then stuff it.



8/25 SI modify
Install LDO when UMA


JDIM1A
PC2100 DDR3 SDRAM SO-DIMM
(204P)
DDR3-DIMM0
SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30
JDIM1B
PC2100 DDR3 SDRAM SO-DIMM
(204P)
DDR3-DIMM0
for S3 power reduction
SI modify
for S3 power reduction
0510 add for WiMAX
0511 add for WiMAX
Place these Caps near So-Dimm0.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%
PROJECT : R18D
Quanta Computer Inc.
DDR3 DIMM-0
Tuesday, February 15, 2011

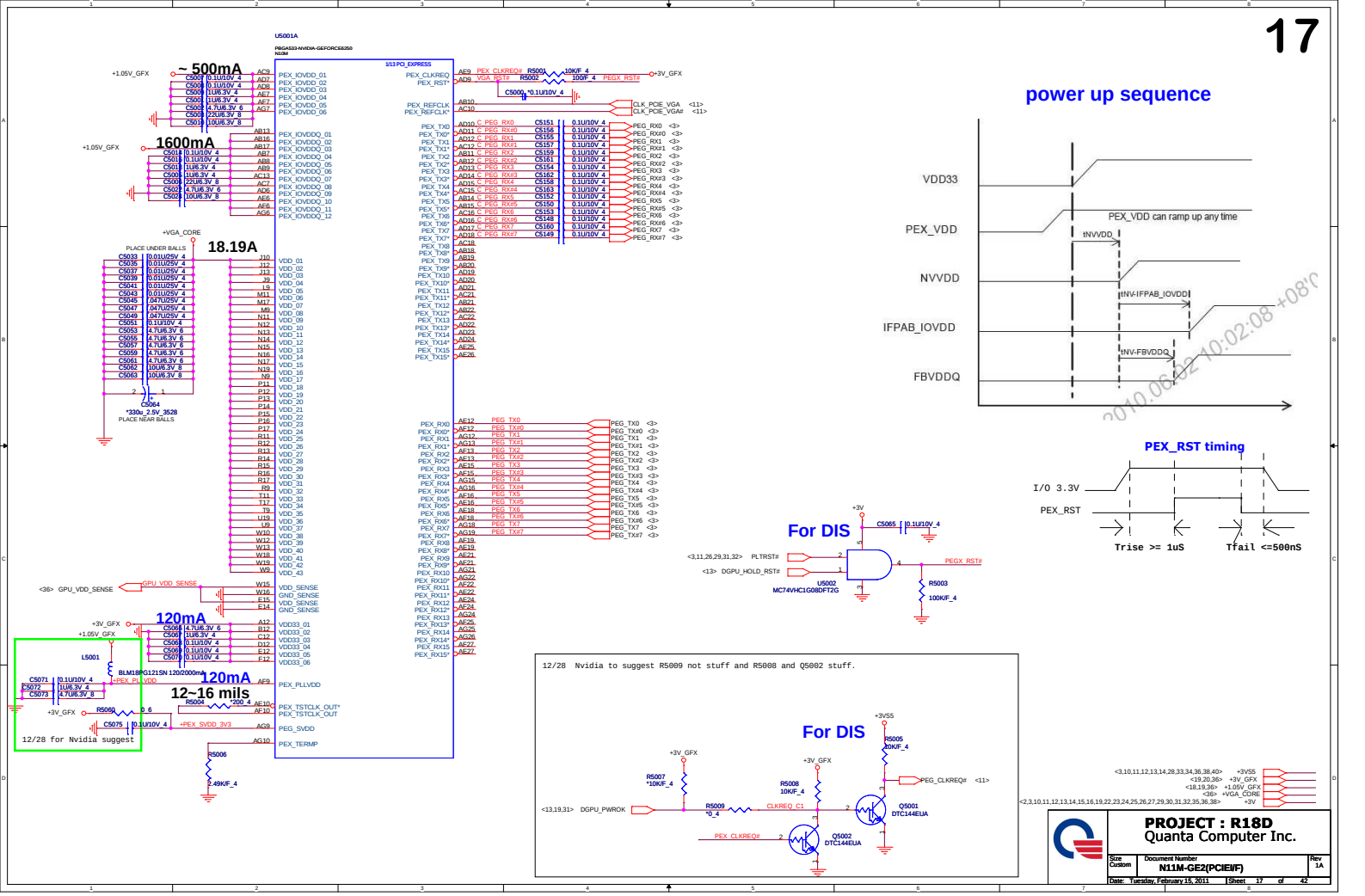


Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603

It can cost down 30%

Project	PROJECT : R18D Quanta Computer Inc.
Size / Custom	Document Number: DDR3 DIMM-1 / Rev 1A
Date: Tuesday, February 15, 2011	Sheet 16 of 42


~ 500mA
1600mA
18.19A
120mA
120mA
12~16 mils
12/28 for Nvidia suggest
power up sequence
VDD33
PEX_VDD
NVVDD
IFPAB_IOVDD
FBVDDQ
PEX_VDD can ramp up any time
tNVVDD
tNV-IFPAB_IOVDD
tNV-FBVDDQ
PEX_RST timing
I/O 3.3V
PEX_RST
Trise >= 1uS
Tfail <=500nS
For DIS
For DIS
12/28 Nvidia to suggest R5009 not stuff and R5008 and Q5002 stuff.
PROJECT : R18D
Quanta Computer Inc.
N11M-GE2(PCIEI/F)
Tuesday, February 15, 2011
Sheet 17 of 42

2.16A

+1.5V_GFX

U5001B

PBGA533-NVIDIA-GEFORCE6250

N10M

2/13 FRAME_BUFFER

C5076 .047U/25V_4
C5077 .047U/25V_4
C5083 .047U/25V_4
C5078 0.01U/25V_4
C5079 0.01U/25V_4
C5080 0.01U/25V_4
C5082 4.7U/6.3V_6
C5081 4.7U/6.3V_6

A13	FBVDDQ_01	FBA_D0	D22
B13	FBVDDQ_02	FBA_D1	E24
C13	FBVDDQ_03	FBA_D2	E22
D13	FBVDDQ_04	FBA_D3	D24
D14	FBVDDQ_05	FBA_D4	D26
E13	FBVDDQ_06	FBA_D5	D27
F13	FBVDDQ_07	FBA_D6	C27
E14	FBVDDQ_08	FBA_D7	B27
E15	FBVDDQ_09	FBA_D8	A21
F16	FBVDDQ_10	FBA_D9	B21
E17	FBVDDQ_11	FBA_D10	C21
F19	FBVDDQ_12	FBA_D11	C19
F22	FBVDDQ_13	FBA_D12	C18
H23	FBVDDQ_14	FBA_D13	D18
H26	FBVDDQ_15	FBA_D14	B18
J15	FBVDDQ_16	FBA_D15	C16
J16	FBVDDQ_17	FBA_D16	E21
J18	FBVDDQ_18	FBA_D17	F21
J19	FBVDDQ_19	FBA_D18	D20
L19	FBVDDQ_20	FBA_D19	F20
L23	FBVDDQ_21	FBA_D20	D17
L26	FBVDDQ_22	FBA_D21	F18
M19	FBVDDQ_23	FBA_D22	D16
N22	FBVDDQ_24	FBA_D23	E16
U22	FBVDDQ_25	FBA_D24	A22
Y22	FBVDDQ_26	FBA_D25	C24
		FBA_D26	D21
		FBA_D27	B22
		FBA_D28	C22
		FBA_D29	A25
		FBA_D30	B25
		FBA_D31	A26
		FBA_D32	U24
		FBA_D33	V24
		FBA_D34	V23
		FBA_D35	R24
		FBA_D36	T23
		FBA_D37	R23
		FBA_D38	P24
		FBA_D39	P22
		FBA_D40	AC24
		FBA_D41	AB23
		FBA_D42	AB24
		FBA_D43	W24
		FBA_D44	AA22
		FBA_D45	W23
		FBA_D46	W22
		FBA_D47	V22
		FBA_D48	AA25
		FBA_D49	W27
		FBA_D50	W26
		FBA_D51	W25
		FBA_D52	AB25
		FBA_D53	AB26
		FBA_D54	AD26
		FBA_D55	AD27
		FBA_D56	V25
		FBA_D57	R25
		FBA_D58	V26
		FBA_D59	V27
		FBA_D60	R26
		FBA_D61	T25
		FBA_D62	N25
		FBA_D63	N26

TP20 FBA_CMD1

<21> FBA_CMD0	G24	(FBA_CMD25)FBA_CMD0	FBA_D25
<21> FBA_CMD2	F25	(FBA_CMD23)FBA_CMD1	FBA_D29
<21> FBA_CMD3	F26	FBA_CMD2	FBA_D30
<21> FBA_CMD4	G26	(FBA_CMD0)FBA_CMD3	FBA_D31
<21> FBA_CMD5	G27	(FBA_CMD10)FBA_CMD4	FBA_D32
<21> FBA_CMD6	G25	(FBA_CMD26)FBA_CMD5	FBA_D33
<21> FBA_CMD7	J25	(FBA_CMD14)FBA_CMD6	FBA_D34
<21> FBA_CMD8	J24	FBA_CMD7	FBA_D35
<21> FBA_CMD9	H24	(FBA_CMD1)FBA_CMD8	FBA_D36
<21> FBA_CMD10	H27	(FBA_CMD22)FBA_CMD9	FBA_D37
<21> FBA_CMD11	J26	(FBA_CMD20)FBA_CMD10	FBA_D38
<21> FBA_CMD12	G22	(FBA_CMD24)FBA_CMD11	FBA_D39
<21> FBA_CMD13	G23	(FBA_CMD18)FBA_CMD12	FBA_D40
<21> FBA_CMD14	J22	(FBA_CMD9)FBA_CMD13	FBA_D41
<21> FBA_CMD15	J27	(FBA_CMD29)FBA_CMD14	FBA_D42
<21> FBA_CMD16	M24	(FBA_CMD8)FBA_CMD15	FBA_D43
<21> FBA_CMD18	L24	(FBA_CMD27)FBA_CMD16	FBA_D44
<21> FBA_CMD19	J23	(FBA_CMD15)FBA_CMD17	FBA_D45
<21> FBA_CMD20	K23	(FBA_CMD11)FBA_CMD18	FBA_D46
<21> FBA_CMD21	K22	(FBA_CMD16)FBA_CMD19	FBA_D47
<21> FBA_CMD22	M23	(FBA_CMD28)FBA_CMD20	FBA_D48
<21> FBA_CMD23	K24	(FBA_CMD3)FBA_CMD21	FBA_D49
<21> FBA_CMD24	M27	(FBA_CMD17)FBA_CMD22	FBA_D50
<21> FBA_CMD25	N27	(FBA_CMD5)FBA_CMD23	FBA_D51
<21> FBA_CMD26	M26	(FBA_CMD4)FBA_CMD24	FBA_D52
<21> FBA_CMD27	K26	(FBA_CMD21)FBA_CMD25	FBA_D53
<21> FBA_CMD28	K27	(FBA_CMD6)FBA_CMD26	FBA_D54
<21> FBA_CMD29	K25	(FBA_CMD13)FBA_CMD27	FBA_D55
<21> FBA_CMD30	M25	(FBA_CMD19)FBA_CMD28	FBA_D56
	L22	(FBA_CMD12)FBA_CMD29	FBA_D57
		FBA_CMD30	FBA_D58

TP19 FBA_CMD17

<21> VMA_CLK0	F24	FBA_CLK0	
<21> VMA_CLK0#	F23	FBA_CLK0*	
<21> VMA_CLK1	N24	FBA_CLK1	
<21> VMA_CLK1#	N23	FBA_CLK1*	

		FBA_DQM0	C26
		FBA_DQM1	B19
		FBA_DQM2	D19
		FBA_DQM3	D23
		FBA_DQM4	T24
		FBA_DQM5	AA23
		FBA_DQM6	AB27
		FBA_DQM7	T26

+1.5V_GFX R5016 40.2/F_4 FB_CAL_PD_VDDQ B15 → FB_CAL_PD_VDDQ

R5017 40.2/F_4 FB_CAL_PU_GND A15 → FB_CAL_PU_GND

R5018 60.4/F_4 FB_CAL_TERM_GND B16 → FB_CAL_TERM_GND

+1.5V_GFX R5019 10K/F_4 FBA_DEBUG M22 → (FBA_DEBUG)FBA_DEBUG0

For debug only

10mA

		FBA_DQS_WP0	C25
		FBA_DQS_WP1	A19
		FBA_DQS_WP2	E19
		FBA_DQS_WP3	A24
		FBA_DQS_WP4	T22
		FBA_DQS_WP5	AA24
		FBA_DQS_WP6	AA26
		FBA_DQS_WP7	T27

+1.05V_GFX 15mils width 200mA

L5002 PBY160808T-300Y-N +FB_PLLAVDD J19 → FB_PLLAVDD

30 ohm/100MHz ESR=0.03ohm

C5085 1U/6.3V_4 T19 → FB_DLLAVDD

C5086 0.1U/10V_4 AC19 → FB_PLLAVDD

C5087 10U/6.3V_8

		FBA_DQS_RN0	D25
		FBA_DQS_RN1	A18
		FBA_DQS_RN2	E18
		FBA_DQS_RN3	B24
		FBA_DQS_RN4	R22
		FBA_DQS_RN5	Y24
		FBA_DQS_RN6	AA27
		FBA_DQS_RN7	R27

FB_VREF A16 +FB_VREF1 TP18

12/28 Nvidia recommend

1.L5003 change to bead 30ohm (ESR=0.01) 0603.
2.C5085 change to 1uF_X7R_0603
3.Delete C5084.

<21> VMA_DQ[63..0]
<21> VMA_DM[7..0]
<21> VMA_WDQS[7..0]
<21> VMA_RDQS[7..0]

U5001I

N10M PBGA533-NVIDIA-GEFORCE6250

13/13 GND_NC

AC11	GND_01	NC_01	C15
AC14	GND_02	NC_02	D15
AC17	GND_03	(NC_03)PGOOD	R5011
AC2	GND_04		
AC20	GND_05		
AC23	GND_06		
AC26	GND_07		
AC5	GND_08		
AC8	GND_09		
AE11	GND_10		
AE14	GND_11		
AE17	GND_12		
AE2	GND_13		
AE20	GND_14		
AE23	GND_15		
AE26	GND_16		
AE5	GND_17		
AF8	GND_18		
B11	GND_19		
B14	GND_20		
B17	GND_21		
B2	GND_22		
B20	GND_23		
B23	GND_24		
B26	GND_25		
B5	GND_26		
B8	GND_27		
E11	GND_28		
E17	GND_30		
E2	GND_31		
E20	GND_32		
E23	GND_33		
E26	GND_34		
E5	GND_35		
E8	GND_36		
H2	GND_37		
H5	GND_38		
J11	GND_39		
J14	GND_40		
J17	GND_41		
K19	GND_42		
K9	GND_43		
L11	GND_44		
L12	GND_45		
L13	GND_46		
L14	GND_47		
L15	GND_48		
L16	GND_49		
L17	GND_50		
L2	GND_51		
L5	GND_52		
M12	GND_53		
M13	GND_54		
M14	GND_55		
M15	GND_56		
M16	GND_57		
P19	GND_58		
P2	GND_59		
P23	GND_60		
P26	GND_61		
P5	GND_62		
P9	GND_63		
T12	GND_64		
T13	GND_65		
T14	GND_66		
T15	GND_67		
T16	GND_68		
U11	GND_69		
U12	GND_70		
U13	GND_71		
U14	GND_72		
U15	GND_73		
U16	GND_74		
U17	GND_75		
U2	GND_76		
U23	GND_77		
U26	GND_78		
U5	GND_79		
V19	GND_80		
V9	GND_81		
W11	GND_82		
W14	GND_83		
W17	GND_84		
Y2	GND_85		
Y23	GND_86		
Y26	GND_87		
Y5	GND_88		

R5011 10K/F_4

nVIDIA comment 8/18

FBA_CMD0	R5012	10K/F_4	
FBA_CMD3	R5010	10K/F_4	
FBA_CMD16	R5013	10K/F_4	
FBA_CMD19	R5014	10K/F_4	
FBA_CMD20	R5015	10K/F_4	

<17,19,36> +1.05V_GFX
<19,21,36> +1.5V_GFX

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N11M-GE2(MEMORY/GND)	1A

Date: Tuesday, February 15, 2011 Sheet 18 of 42

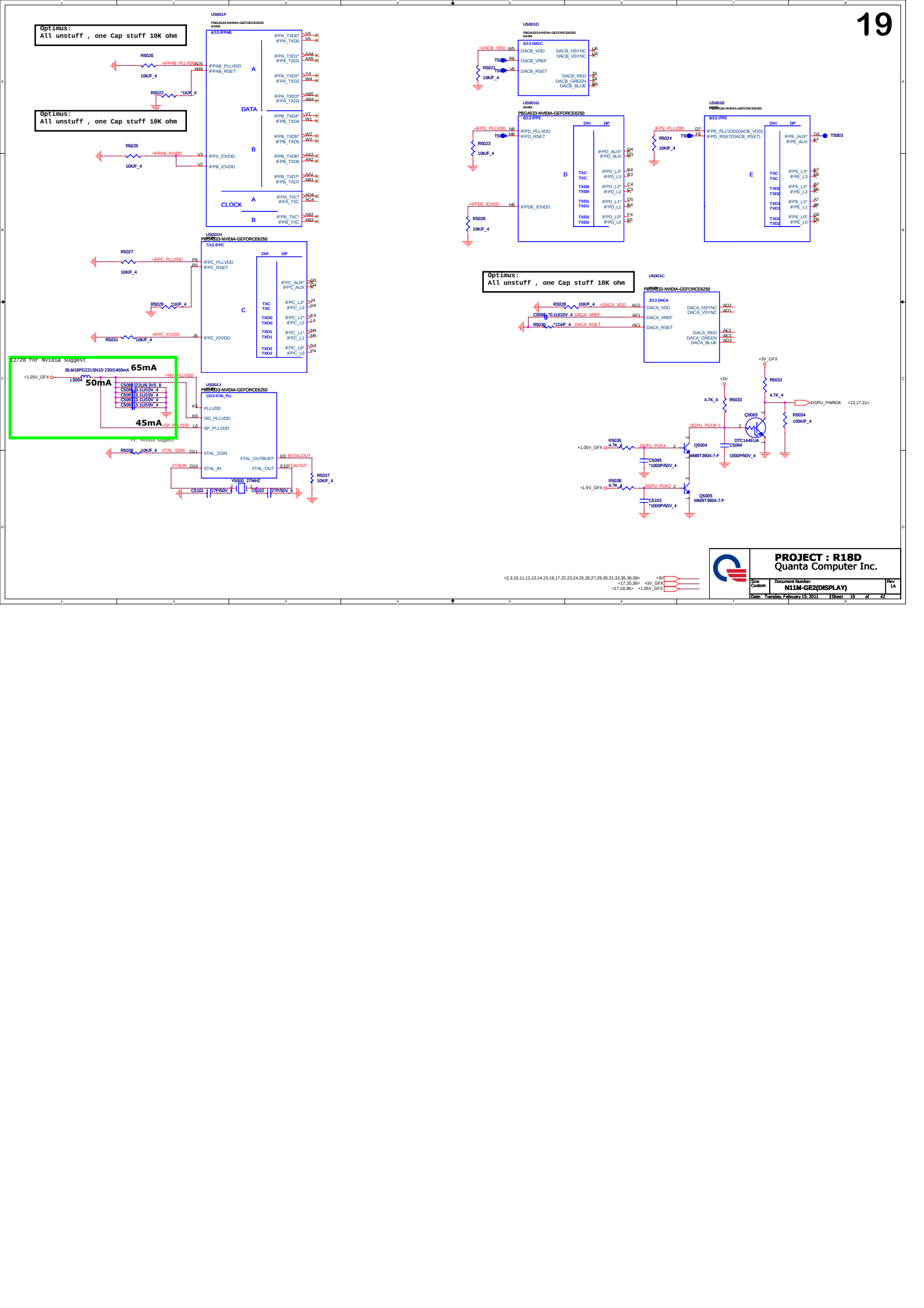
Optimus:
All unstuff , one Cap stuff 10K ohm

Optimus:
All unstuff , one Cap stuff 10K ohm

Optimus:
All unstuff , one Cap stuff 10K ohm

12/28 for Nvidia suggest

PV: Nvidia suggest



PROJECT : R18D Quanta Computer Inc.		
Size: Custom	Document Number: N11M-GE2(DISPLAY)	Rev: 1A
Date: Tuesday, February 15, 2011	Sheet 19 of 42	

4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

N12P-GV -> 0x17F

N12M-GE -> 0xA7A 1010 ->PU15K

ROM_SI -> based on VRAM.

ROM_SO -> PU 10K

ROM_SCLK -> PU 5K

STRAP0 -> PU 45K

STRAP1 -> PD 35K

STRAP2 -> PD 5K

STRAP3 -> PD 5K

STRAP 4 -> PD 10K.

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

CS31502FB24 15K 1%

PCI_DEVID[4]/SUBVENDOR

+3V_GFX

12/28: Change as nVidia setting

R5042 *4.99K/F_4 · R5043 10K/F_4 · R5047 4.99K/F_4

R5048 45.3K/F_4 · R5044 5.7K/F_4 · R5045 *45.3K/F_4

ROM_SI · ROM_SO · ROM_SCLK

STRAP0 · STRAP1 · STRAP2

(Ra)

R5051 35.7K/F_4 · R5052 *10K/F_4 · R5053 *10K/F_4

R5054 *10K/F_4 · R5055 35.7K_4 · R5056 4.99K/F_4

Default: Hynix VRAM

PV: Change as nVidia setting

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix		PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung		PD 20K
0110	DDR3 128Mx16x4, 128bit, 1GB,800MHz	Hynix		PD 35K
0111	DDR3 128Mx16x4, 128bit, 1GB,800MHz	Samsung		PD 45K
XXXX				
XXXX				

(Ra)

JTAG_TMS R5075 *10K/F_4 · JTAG_TDI R5076 *10K/F_4 · VGA_OVT# R5077 10K/F_4 · ALERT R5079 10K/F_4

12/28 for Nvidia suggest

JTAG_TRST# R5080 10K/F_4 · JTAG_TCK R5084 *10K/F_4

GFX_CORE_CNTRL0 R5085 10K/F_4 · GFX_CORE_CNTRL1 R5086 10K/F_4

12/28 for Nvidia suggest

N12P-GV default boot up voltage
Should be set to 0.85V.
Therefore, please add 10K pull down
resistors to GFX_CORE_CNTRL0 and
GFX_CORE_CNTRL1

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	Memory VREF SELECT
11	I/O	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	THERM_LOAD_STEP_DOWN
14	OUT	N/A	THERM_LOAD_STEP_UP

12/29 Nvidia suggest for AC/Batt# function

12/29 Nvidia suggest

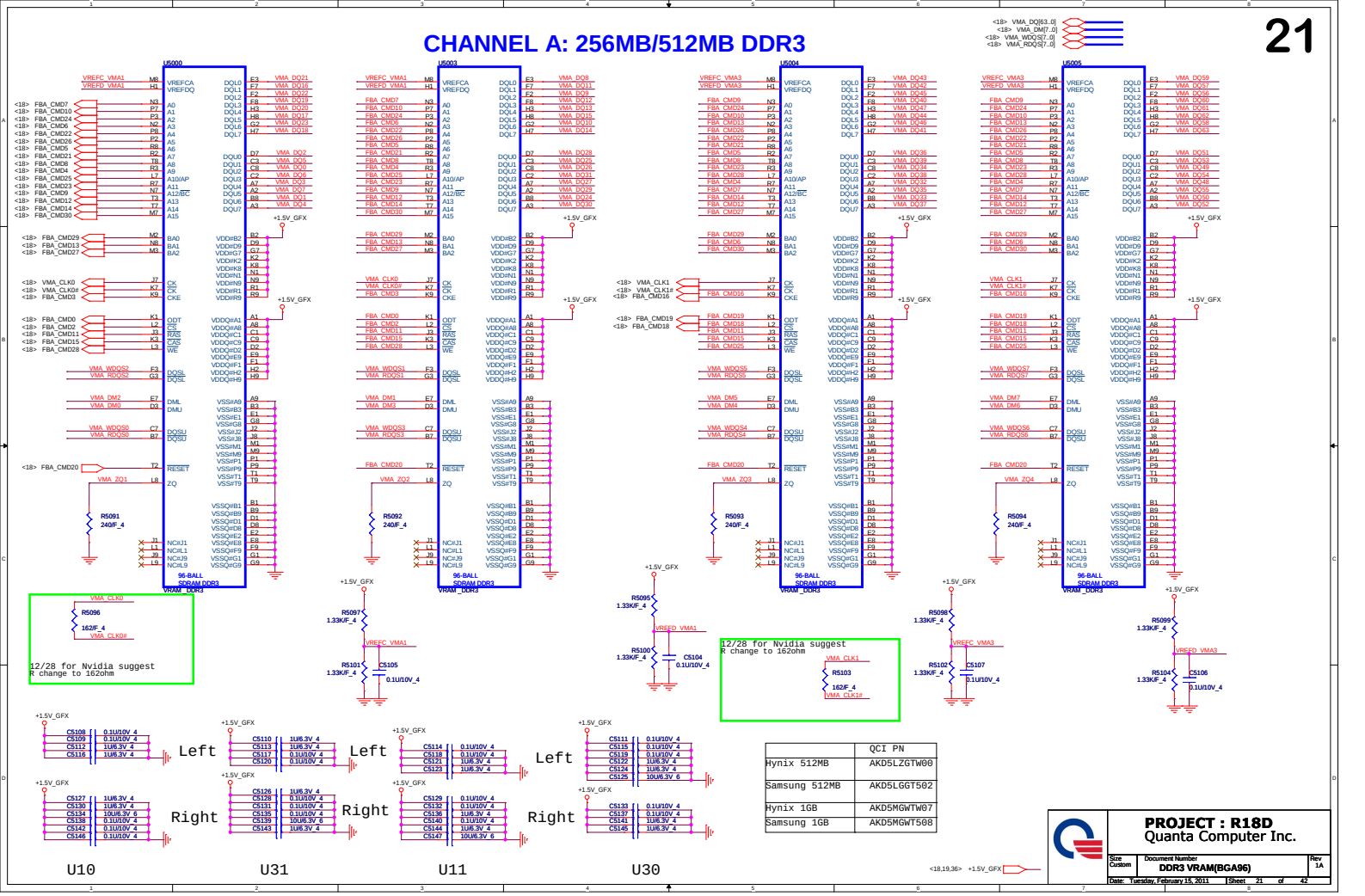
<17,19,36> +3V_GFX

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N12P-GV(GPIO/STRAPS)	1A

Date: Tuesday, February 15, 2011 Sheet 20 of 42

CHANNEL A: 256MB/512MB DDR3



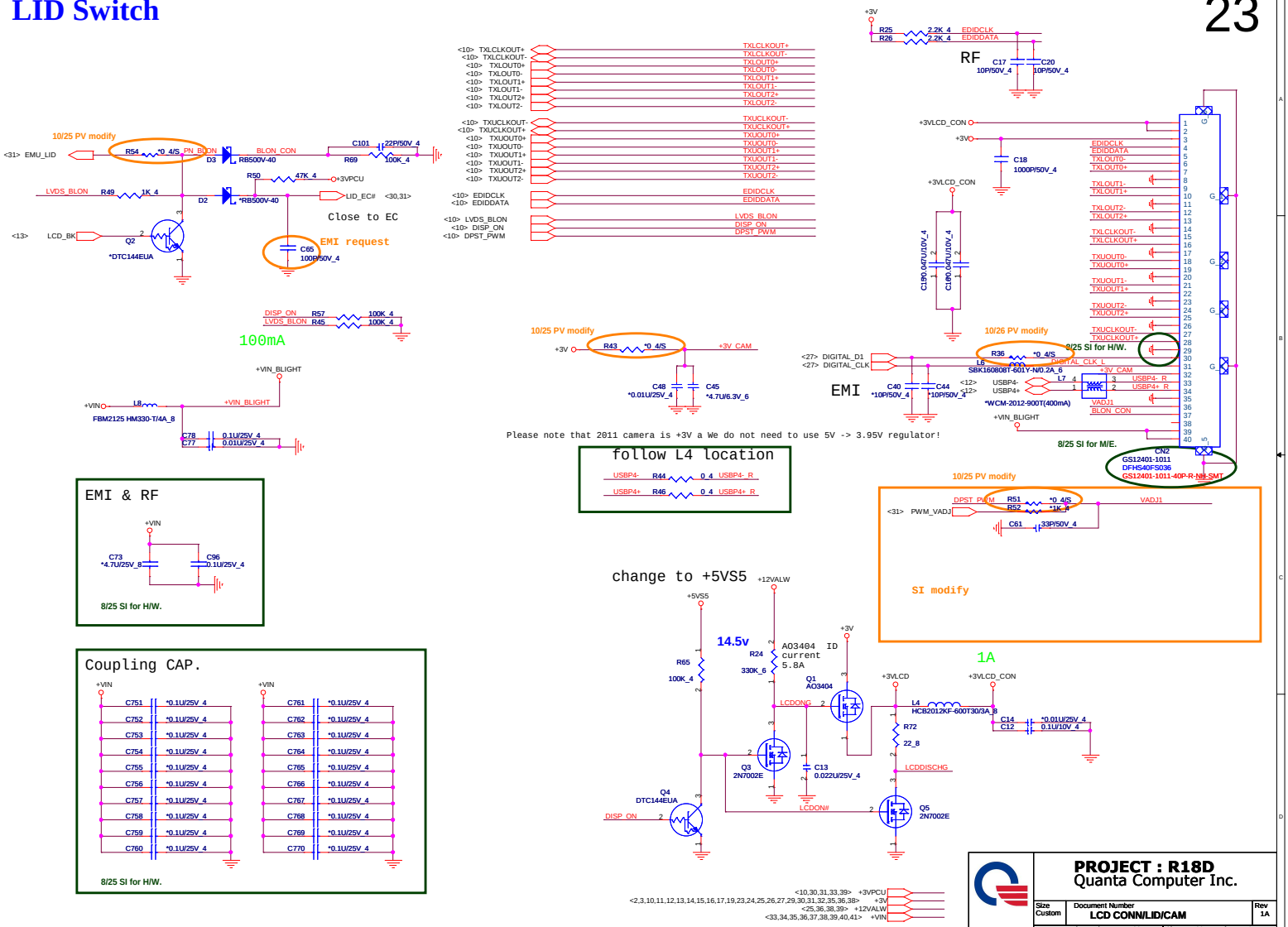
	QCI PN
Hynix 512MB	AKD5LZGTW00
Samsung 512MB	AKD5LGGT502
Hynix 1GB	AKD5MGWTW07
Samsung 1GB	AKD5MGWT508

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 VRAM(BGA96)	1A

Date: Tuesday, February 15, 2011 Sheet 21 of 42

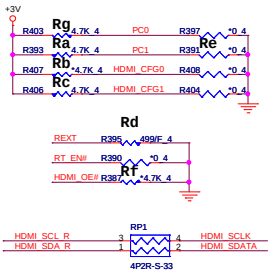
LID Switch

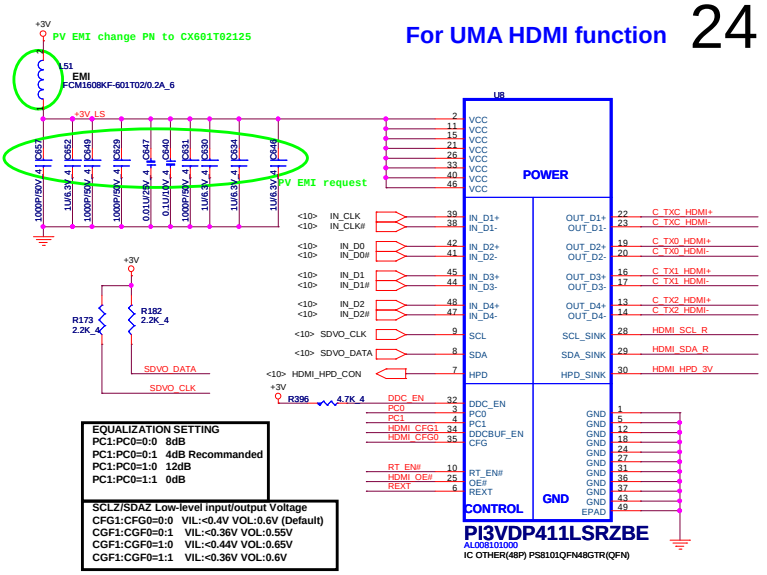


PROJECT : R18D Quanta Computer Inc.			
Size Custom	Document Number LCD CONN/LID/CAM		Rev 1A
Date: Tuesday, February 15, 2011	Sheet 22	of	42

For UMA HDMI function

Signals		PDT	PIM	CHR
PC1	Ra	4.7K	4.7K	NC
HDMI_CFG0	Rb	NC	NC	NC
HDMI_CFG1	Rc	4.7K	NC	NC
REXT	Rd	499	4.7K	1.2K
PC1	Re	NC	NC	4.7K
HDMI_OE#	Rf	NC	NC	4.7K
PC0	Rg	4.7K	4.7K	4.7K





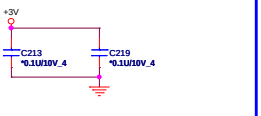
Vender	Part	Part Number	Part Description
PDT	PS8101	AL008101000	IC OTHER(48P) PS8101QFN48GTR(QFN)
PIM	PI3VDP411LSRZBE	ALP411LS004	IC OTHER(48P) PI3VDP411LSRZBE(TQFN)
CHR	CH7318C	AL007318002	IC OTHER(48P) CH7318C-BF-TR(QFN)

9/16 : PIM: need use ALP411LS000 or ALP411LS004 for capella

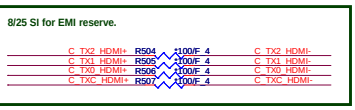
CHR : need Na R1182, add R1027 for capella

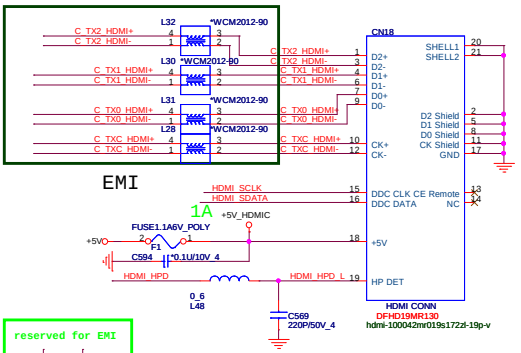
EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

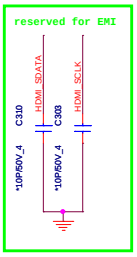
SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

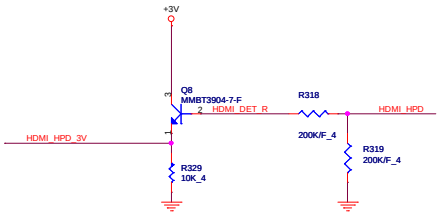


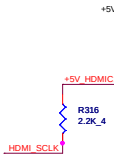
8/25 SI for EMI reserve.









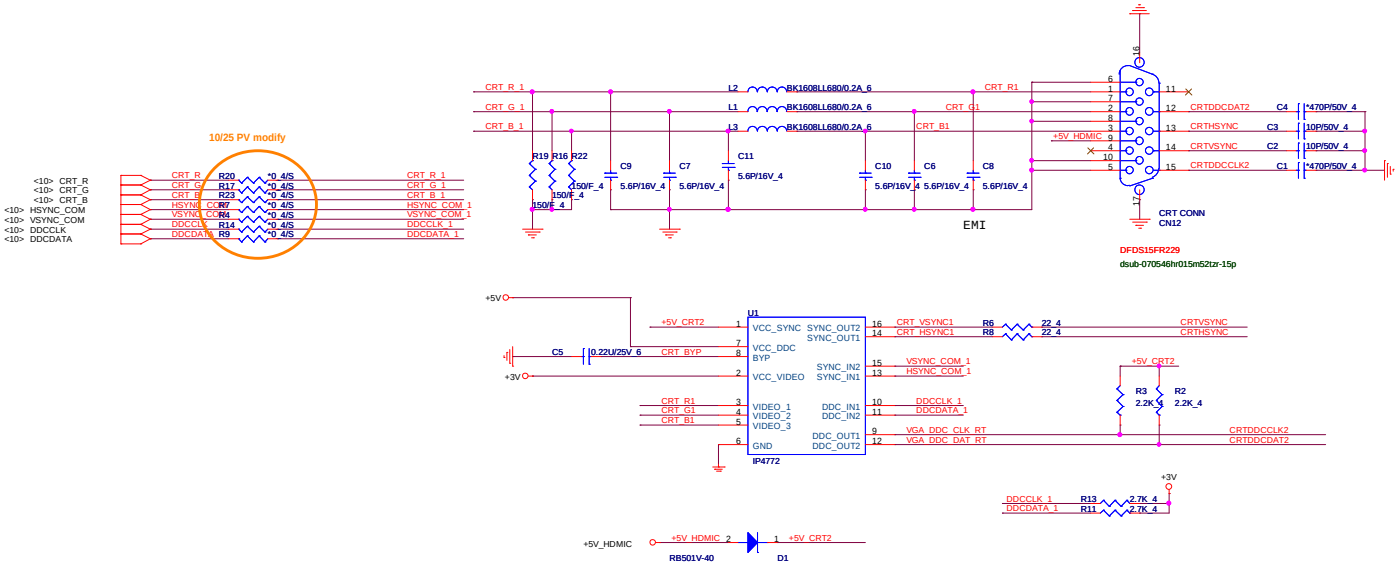


PROJECT : R18D
Quanta Computer Inc.

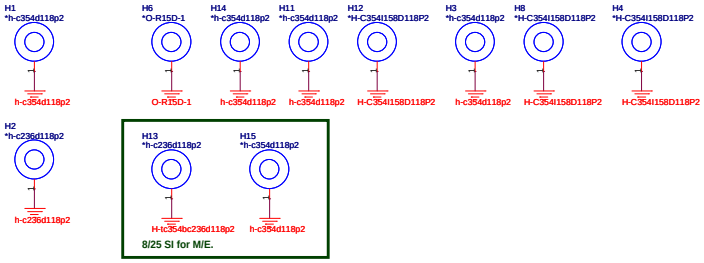
Size	Document Number	Rev
Custom	HDMI CONN	1A

Date: Tuesday, February 15, 2011 Sheet 23 of 42

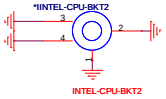
CRT PORT



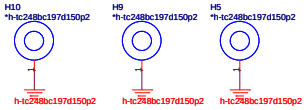
HOLE



CPU



VGA

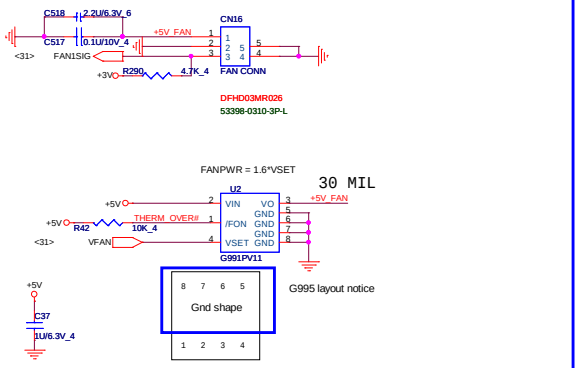


PROJECT : R18D
Quanta Computer Inc.

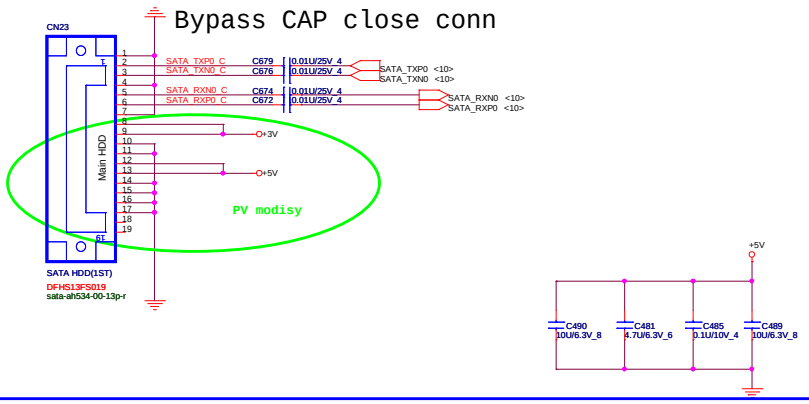
Size	Document Number	Rev
Custom	CRT,Hole	1A

Date: Tuesday, February 15, 2011 Sheet 24 of 42

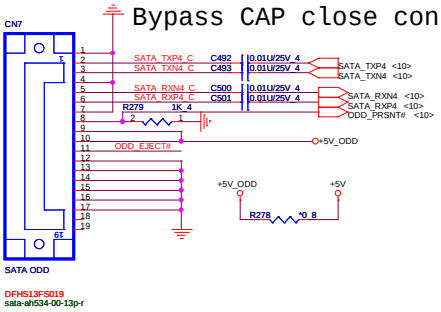
CPU FAN

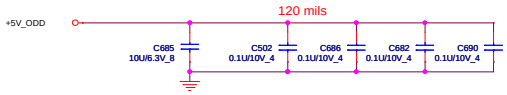


SATA HDD CONNECTOR

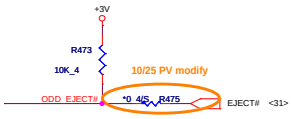


SATA ODD CONNECTOR

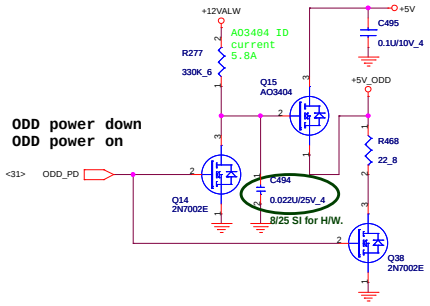




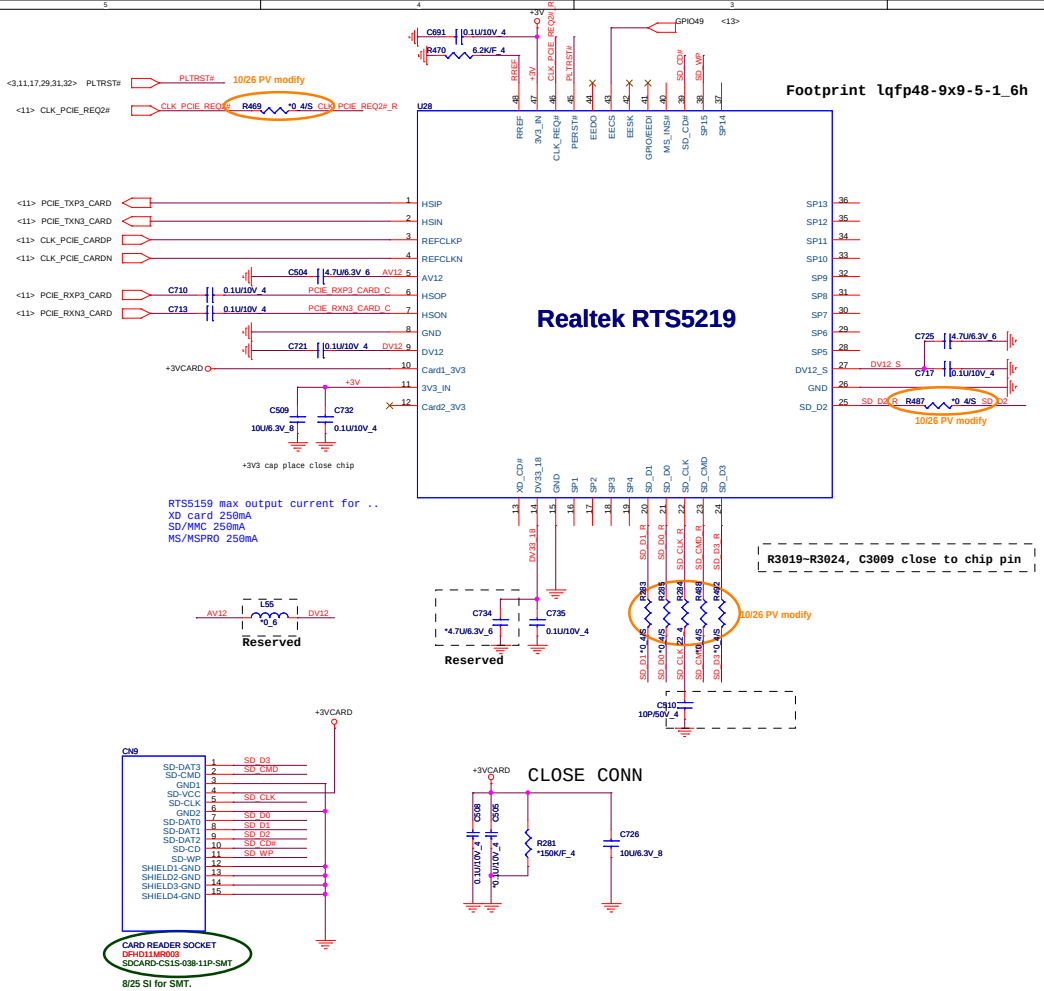
follow INTEL DG change eject PU to +3V.



High : ODD power down
Low : ODD power on



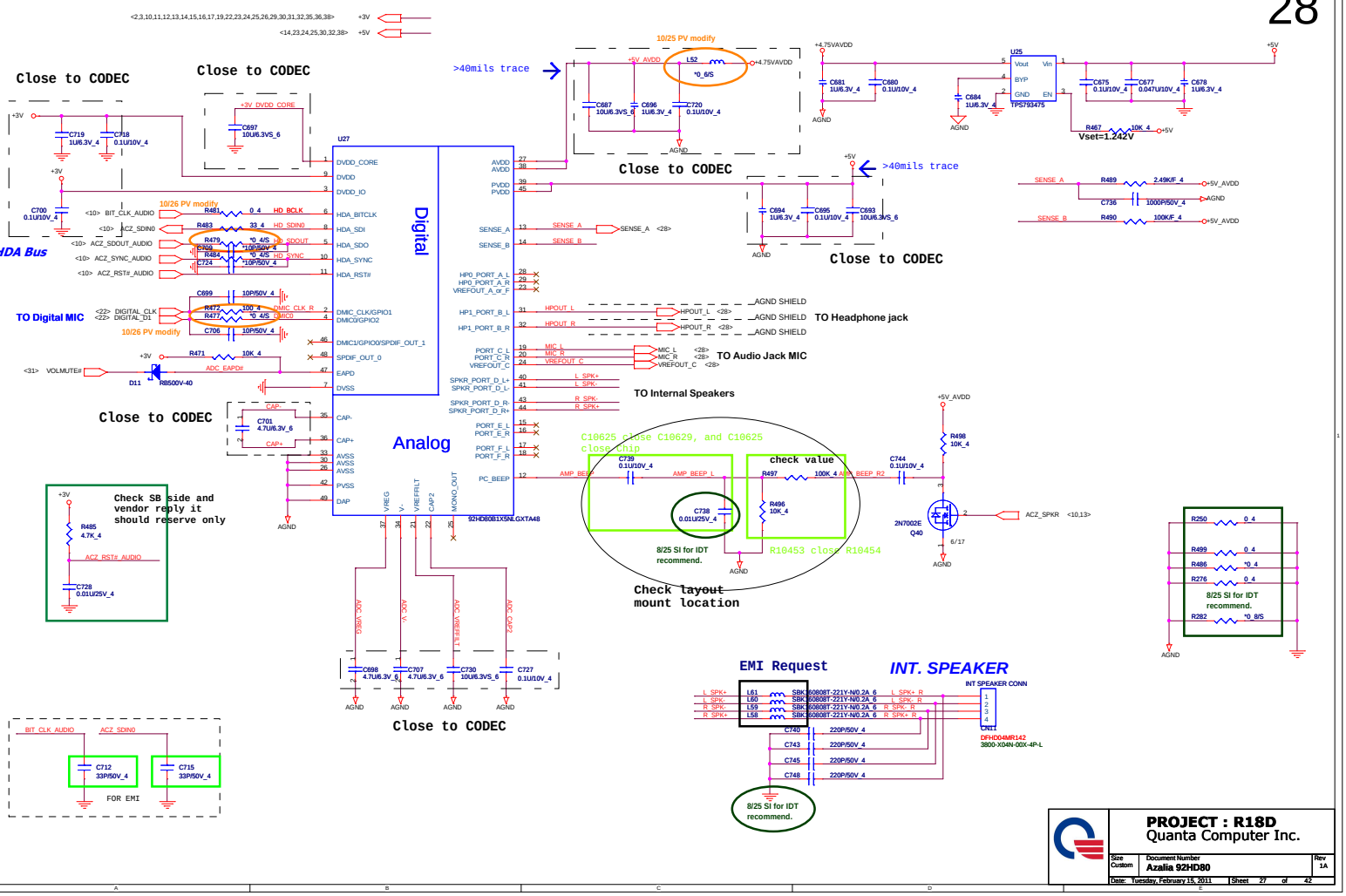
PROJECT : R18D Quanta Computer Inc.		
Size: Custom	Document Number: HDD/ODD/FAN	Rev: 1A
Date: Tuesday, February 15, 2011	Sheet 25 of 42	



PROJECT : R18D
Quanta Computer Inc.

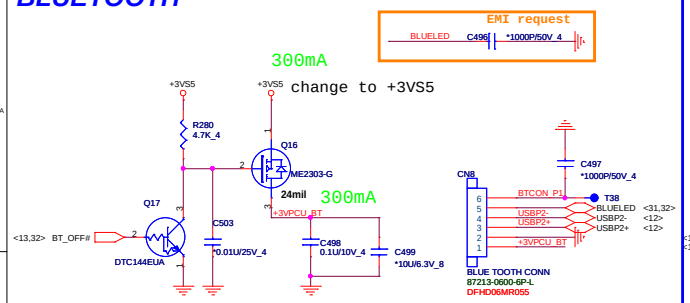
Size	Document Number	Rev
Custom	RTS5219 & CR SOCKET &HOLE	1A

Date: Tuesday, February 15, 2011 Sheet 26 of 42



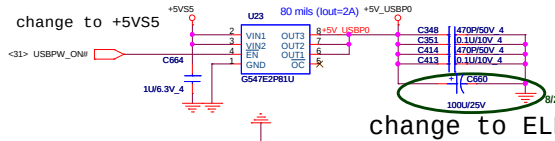
PROJECT : R18D			
Quanta Computer Inc.			
Size: Custom	Document Number: Azalia 92HD80		Rev: 1A
Date: Tuesday, February 15, 2011	Sheet 27 of 42		

BLUETOOTH

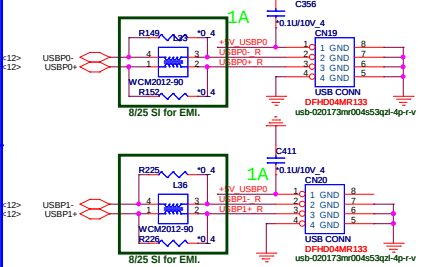


LEFT SIDE USBX2

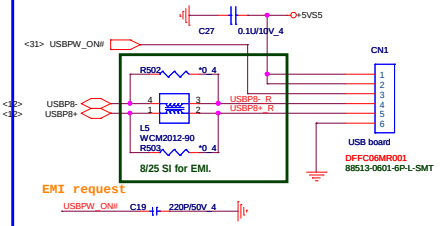
change to AL000547005



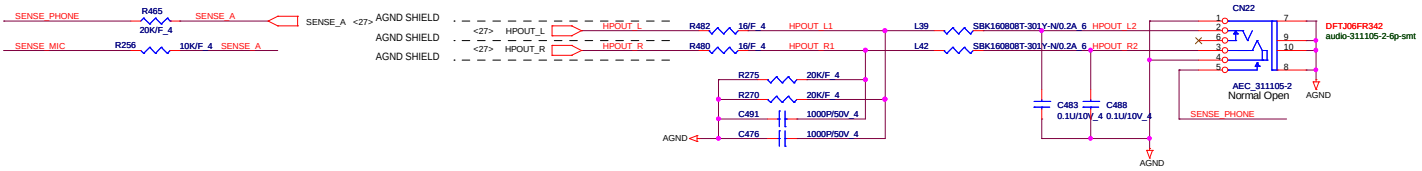
change to ELEC CAP



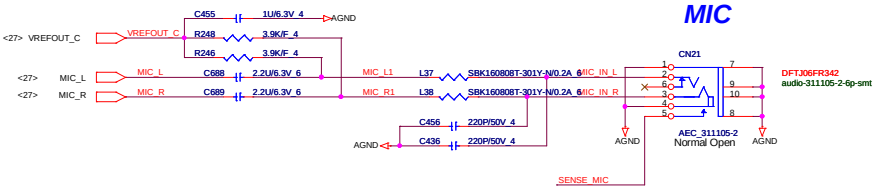
Right SIDE USBX1



Line out

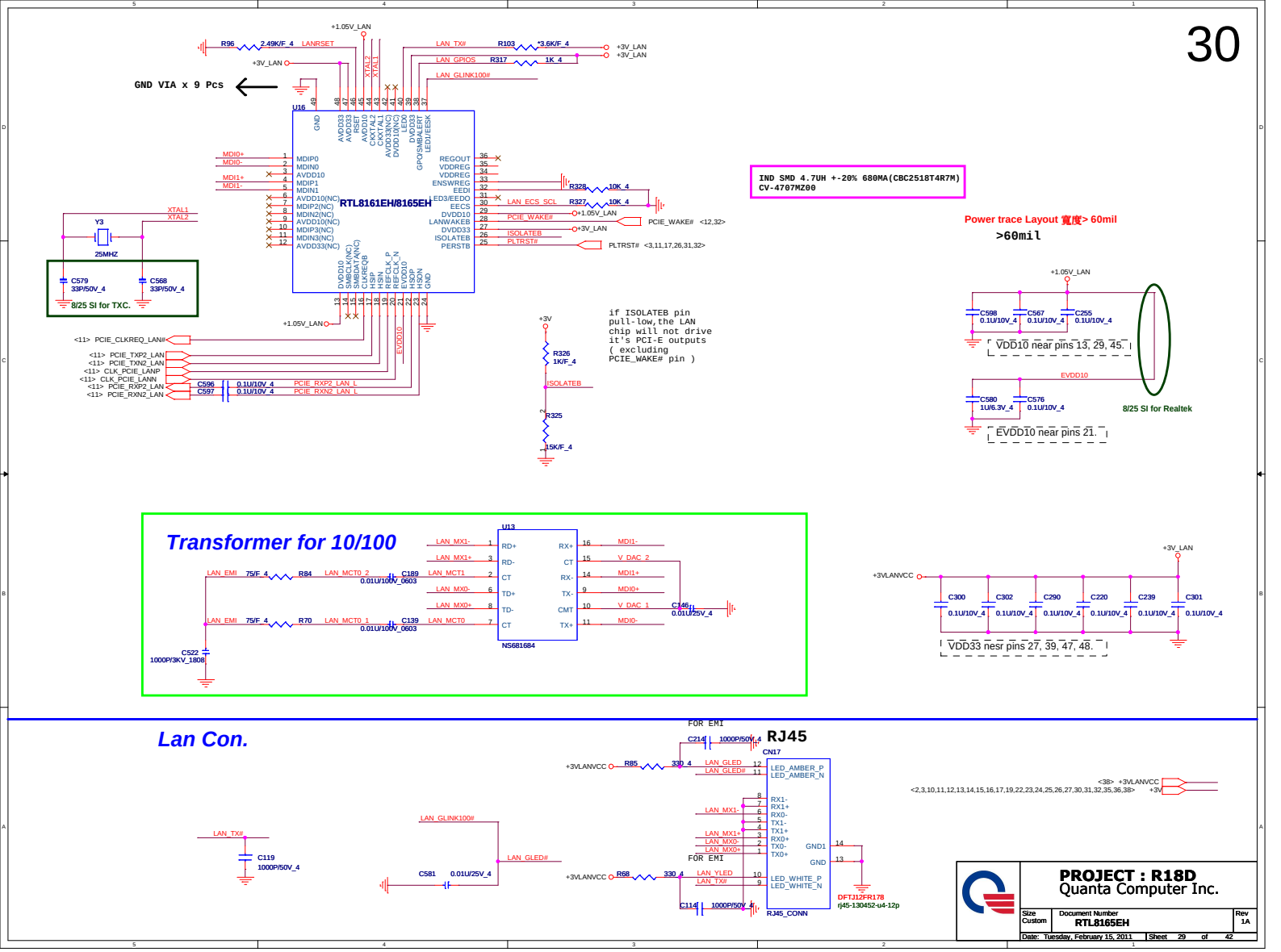


MIC

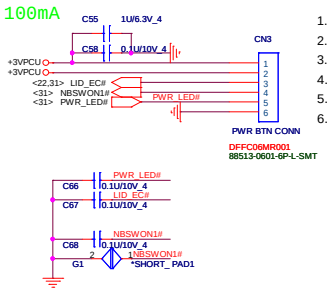


PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB/BT/Audio JacK	1A
Date: Tuesday, February 15, 2011	Sheet 28 of 42	

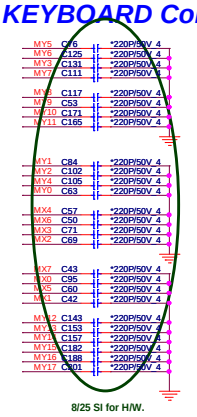

GND VIA x 9 Pcs
RTL8161EH/8165EH
IND SMD 4.7UH +-20% 680MA(CBC2518T4R7M)
CV-4707MZ00
Power trace Layout 寬度> 60mil
>60mil
VDD10 near pins 13, 29, 45.
EVDD10 near pins 21.
8/25 SI for Realtek
8/25 SI for TXC.
if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)
Transformer for 10/100
NS681684
VDD33 nesr pins 27, 39, 47, 48.
Lan Con.
RJ45
FOR EMI
DFTJ12FR178
rj45-130452-u4-12p
R345_CONN
PROJECT : R18D
Quanta Computer Inc.
RTL8165EH
Tuesday, February 15, 2011

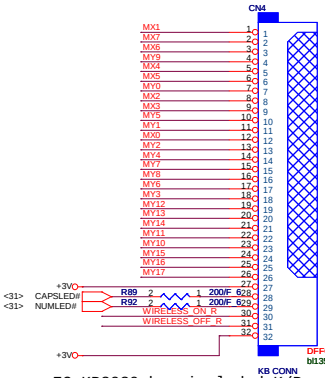
POWER BOTTON CONNECT



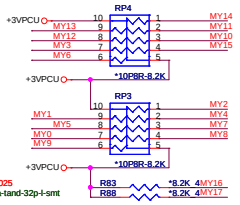
1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

KEYBOARD Con.



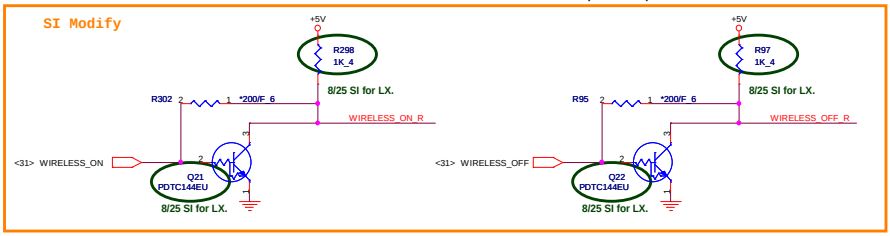


KEYBOARD PULL-UP

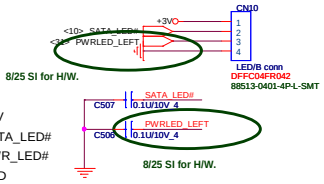


EC KB3930 has included K/B pull-up resistor and function

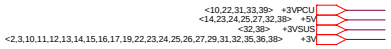
SI Modify



LED Con.

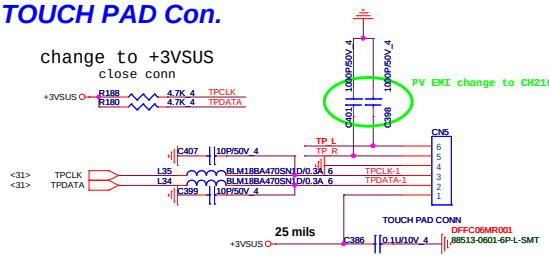


1. +3V
2. SATA_LED#
3. PWR_LED#
4.GND

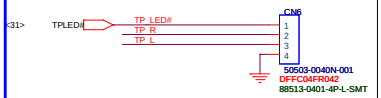


TOUCH PAD Con.

change to +3VSUS
close conn



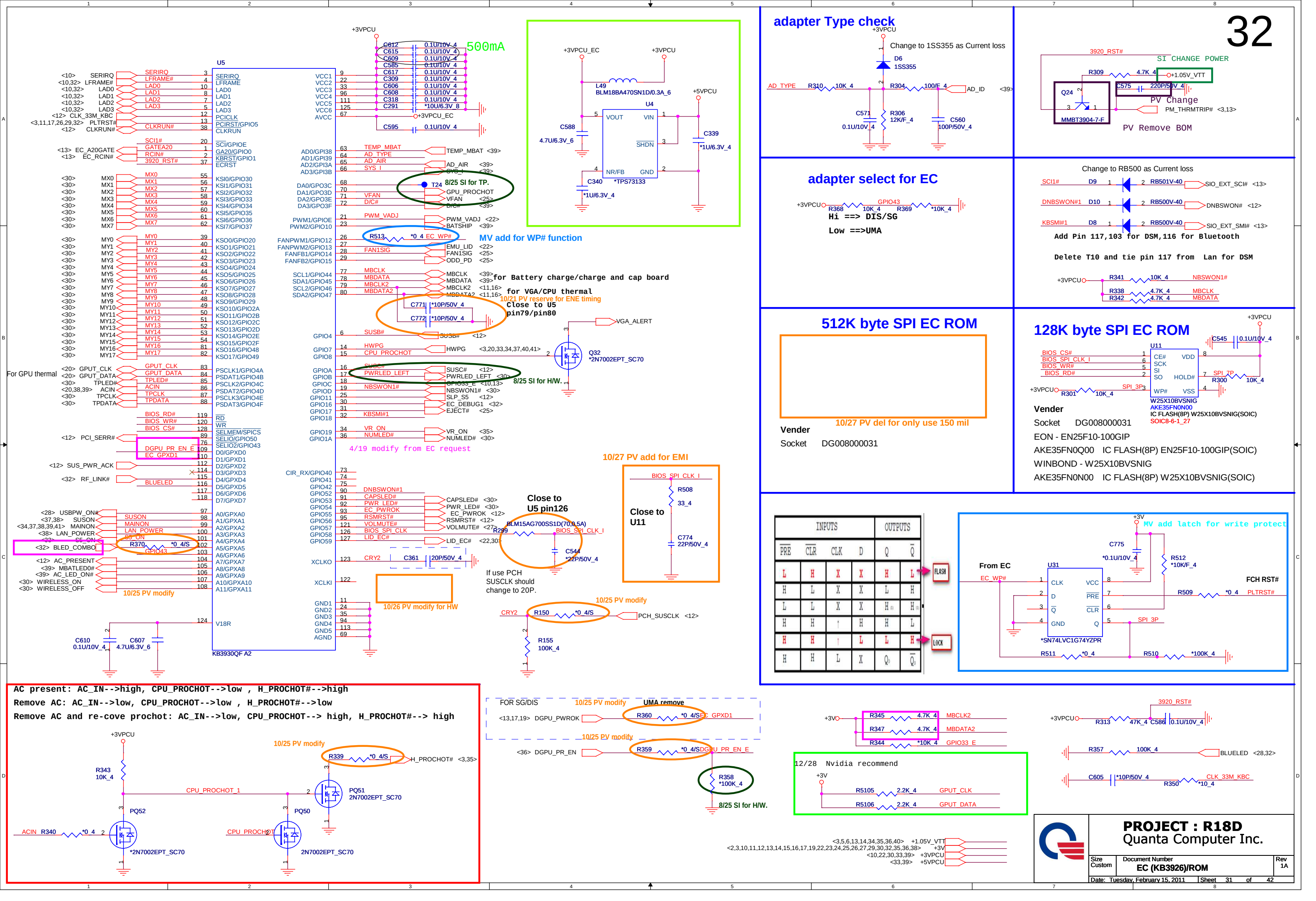
To TOUCH PAD SW board



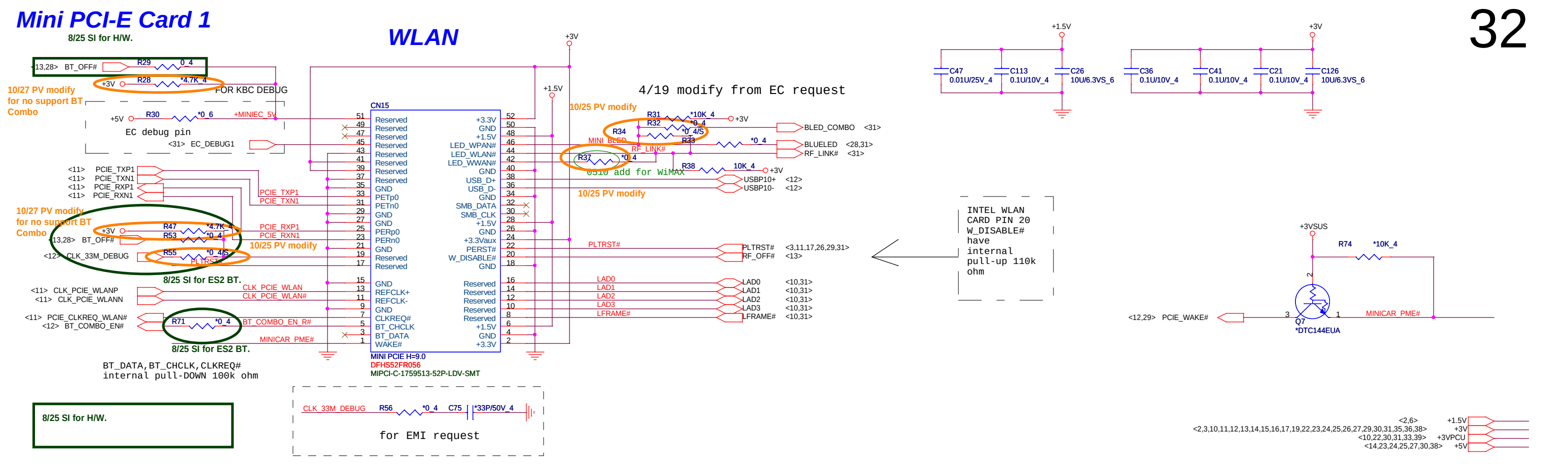
PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KB/SW/TP	1A

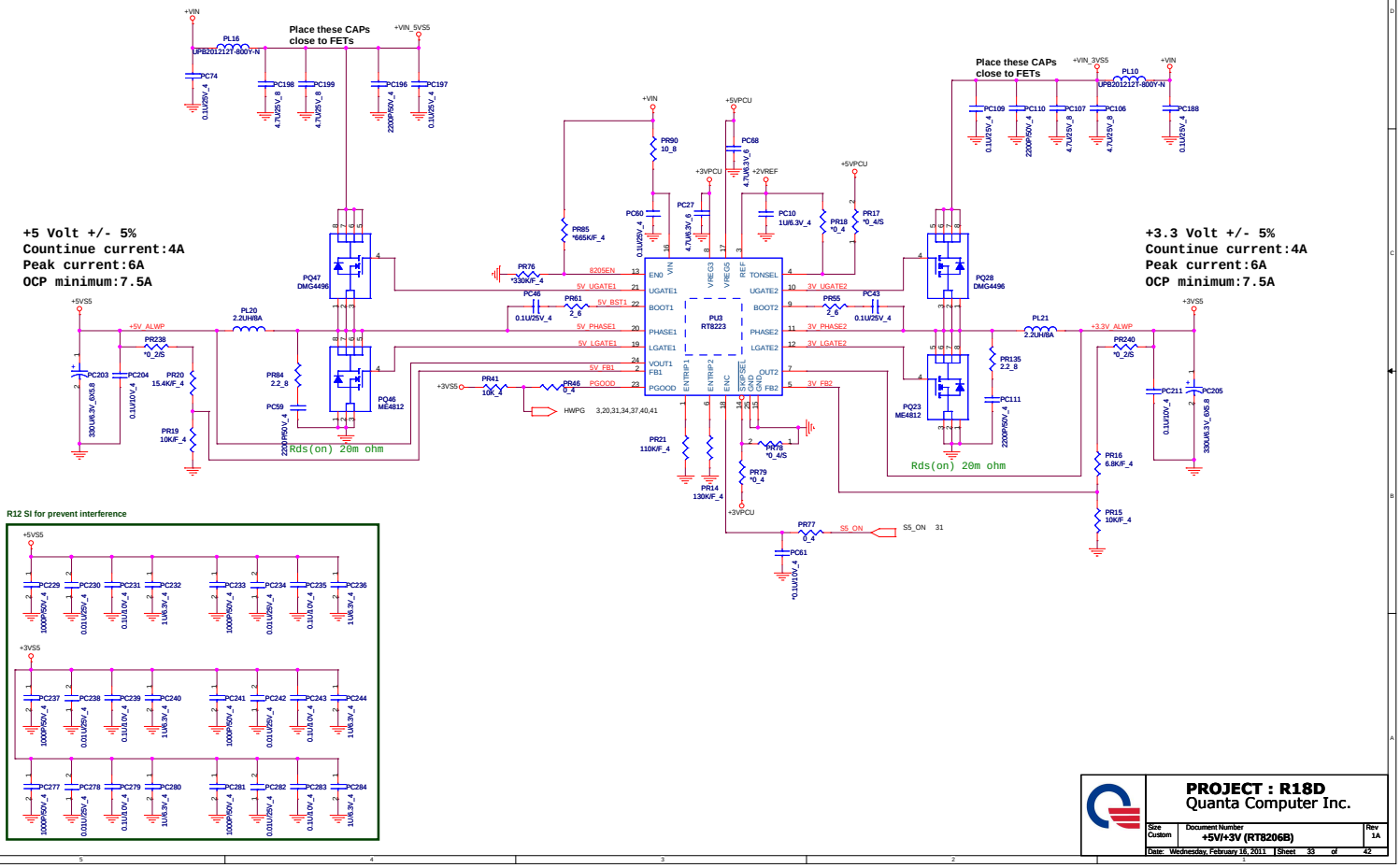
Date: Tuesday, February 15, 2011 | Sheet 30 of 42


32
adapter Type check
Change to 1SS355 as Current loss
D6 1SS355
AD_TYPE R310 10K_4 R304 100/F_4 AD_ID <39>
C571 0.1U/10V_4 R306 12K/F_4 C560 100P/50V_4
3920_RST#
SI CHANGE POWER
R309 4.7K_4 +1.05V_VTT
Q24 C575 220P/50V_4
PV Change
MMBT3904-7-F PM_THRMTRIP# <3,13>
PV Remove BOM
500mA
U5
KB3930QF A2
+3VPCU_EC +3VPCU +5VPCU
L49 BLM18BA470SN1D/0.3A_6
U4 *TPS73133
C588 4.7U/6.3V_6
C339 *1U/6.3V_4
C340 *1U/6.3V_4
adapter select for EC
+3VPCU R368 10K_4 GPIO43 R369 *10K_4
Hi ==> DIS/SG
Low ==>UMA
Change to RB500 as Current loss
SCI1# D9 RB501V-40 SIO_EXT_SCI# <13>
DNBSWON#1 D10 RB500V-40 DNBSWON# <12>
KBSMI#1 D8 RB500V-40 SIO_EXT_SMI# <13>
Add Pin 117,103 for DSM,116 for Bluetooth
Delete T10 and tie pin 117 from Lan for DSM
+3VPCU R341 10K_4 NBSWON1#
R338 4.7K_4 MBCLK
R342 4.7K_4 MBDATA
512K byte SPI EC ROM
10/27 PV del for only use 150 mil
Vender
Socket DG008000031
128K byte SPI EC ROM
U11
W25X10BVSNIG
AKE35FN0N00
IC FLASH(8P) W25X10BVSNIG(SOIC)
SOIC8-6-1_27
Vender
Socket DG008000031
EON - EN25F10-100GIP
AKE35FN0Q00 IC FLASH(8P) EN25F10-100GIP(SOIC)
WINBOND - W25X10BVSNIG
AKE35FN0N00 IC FLASH(8P) W25X10BVSNIG(SOIC)
MV add for WP# function
8/25 SI for TP.
for Battery charge/charge and cap board
for VGA/CPU thermal
10/21 PV reserve for ENE timing
Close to U5 pin79/pin80
Q32 *2N7002EPT_SC70
VGA_ALERT
8/25 SI for H/W.
For GPU thermal
4/19 modify from EC request
10/27 PV add for EMI
Close to U5 pin126
Close to U11
If use PCH SUSCLK should change to 20P.
10/26 PV modify for HW
10/25 PV modify
R150 *0_4/S PCH_SUSCLK <12>
R155 100K_4
MV add latch for write protect
From EC
EC_WP#
U31 *SN74LVC1G74YZPR
FCH RST#
R509 *0_4 PLTRST#
R511 *0_4 R510 *100K_4
AC present: AC_IN-->high, CPU_PROCHOT-->low , H_PROCHOT#-->high
Remove AC: AC_IN-->low, CPU_PROCHOT-->low , H_PROCHOT#-->low
Remove AC and re-cove prochot: AC_IN-->low, CPU_PROCHOT--> high, H_PROCHOT#--> high
R343 10K_4
PQ52 *2N7002EPT_SC70
PQ50 2N7002EPT_SC70
PQ51 2N7002EPT_SC70
R339 *0_4/S H_PROCHOT# <3,35>
ACIN R340 *0_4
FOR SG/DIS
UMA remove
<13,17,19> DGPU_PWROK R360 *0_4/S EC_GPXD1
<36> DGPU_PR_EN R359 *0_4/S DGPU_PR_EN_E
R358 *100K_4
12/28 Nvidia recommend
R5105 2.2K_4 GPUT_CLK
R5106 2.2K_4 GPUT_DATA
R345 4.7K_4 MBCLK2
R347 4.7K_4 MBDATA2
R344 *10K_4 GPIO33_E
R313 47K_4 C586 0.1U/10V_4
R357 100K_4 BLUELED <28,32>
C605 *10P/50V_4 R350 *10_4 CLK_33M_KBC
PROJECT : R18D
Quanta Computer Inc.
Size Custom
Document Number EC (KB3926)/ROM
Rev 1A
Date: Tuesday, February 15, 2011 Sheet 31 of 42

Mini PCI-E Card 1

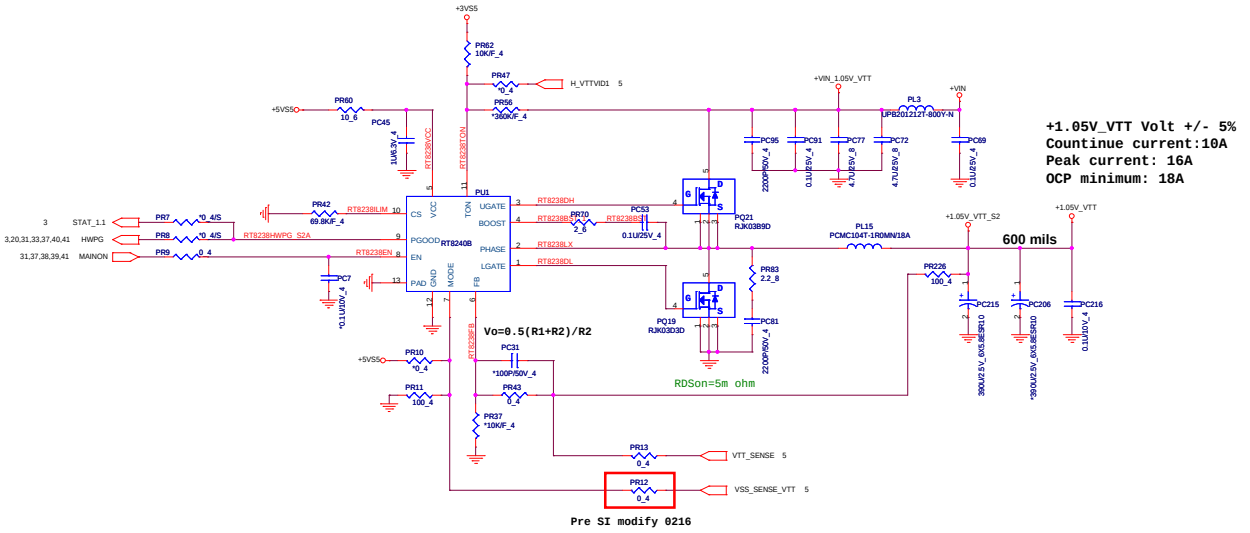


PROJECT : R18D		
Quanta Computer Inc.		
Size: Custom	Document Number: MINI PCIE CONN X1	Rev: 1A
Date: Tuesday, February 15, 2011	Sheet 32 of 42	



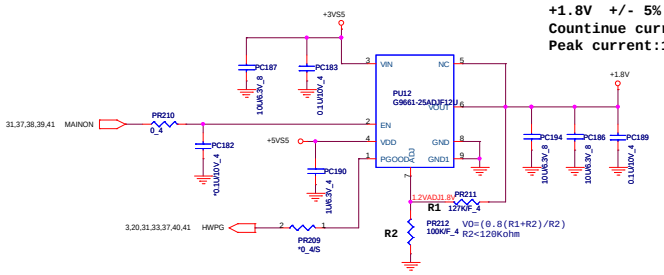
R12 SI for prevent interference

PROJECT : R18D		
Quanta Computer Inc.		
Size: Custom	Document Number: +5V/+3V (RT8206B)	Rev: 1A
Date: Wednesday, February 16, 2011	Sheet 33 of 42	



+1.05V_VTT Volt +/- 5%
Countinue current:10A
Peak current: 16A
OCP minimum: 18A

Pre SI modify 0216

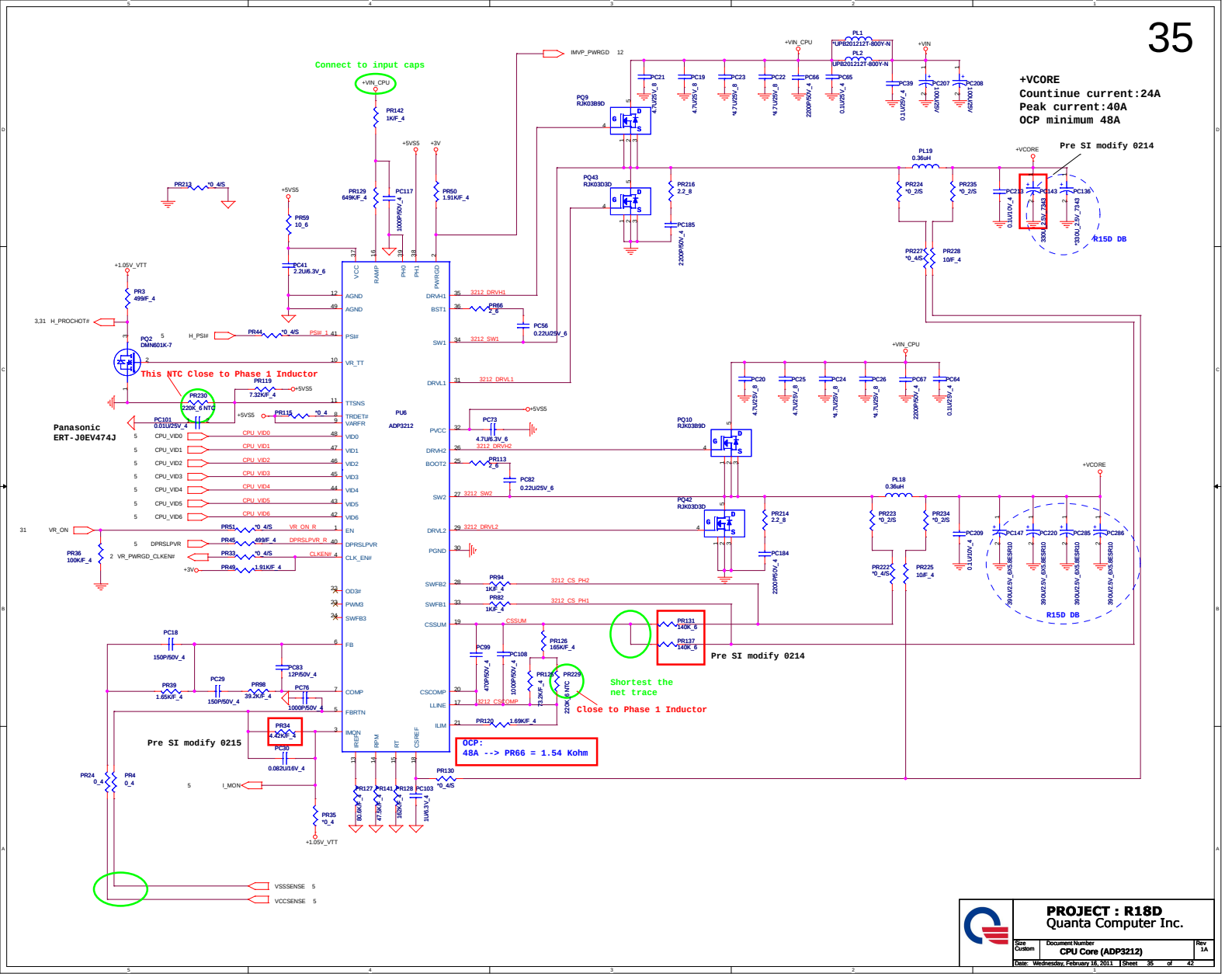


+1.8V +/- 5%
Countinue current:0.7A
Peak current:1A

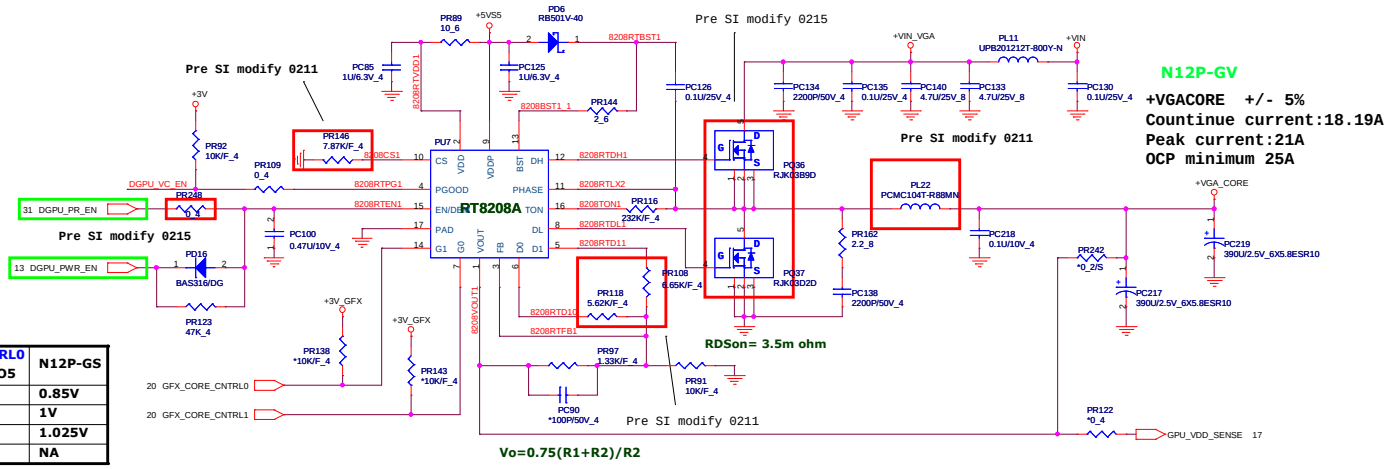
PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1V VTT / PCH	1A

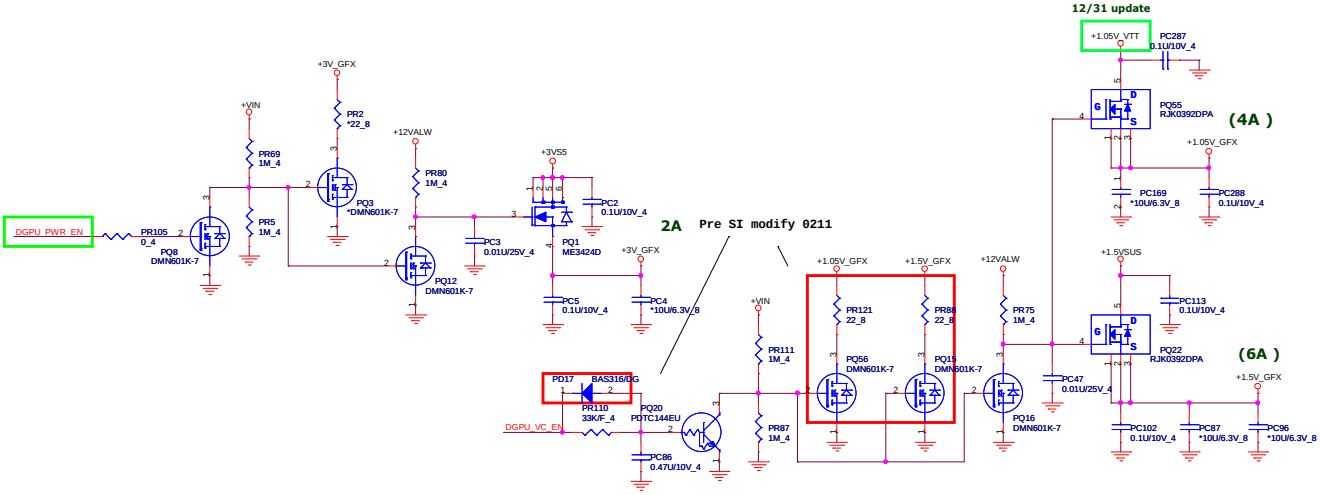
Date: Wednesday, February 16, 2011 | Sheet 34 of 42


Connect to input caps
+VCORE
Countinue current:24A
Peak current:40A
OCP minimum 48A
Pre SI modify 0214
R15D DB
This NTC Close to Phase 1 Inductor
Panasonic
ERT-J0EV474J
Pre SI modify 0215
Pre SI modify 0214
Shortest the
net trace
Close to Phase 1 Inductor
OCP:
48A --> PR66 = 1.54 Kohm
PROJECT : R18D
Quanta Computer Inc.
CPU Core (ADP3212)
Wednesday, February 16, 2011

VGA Core



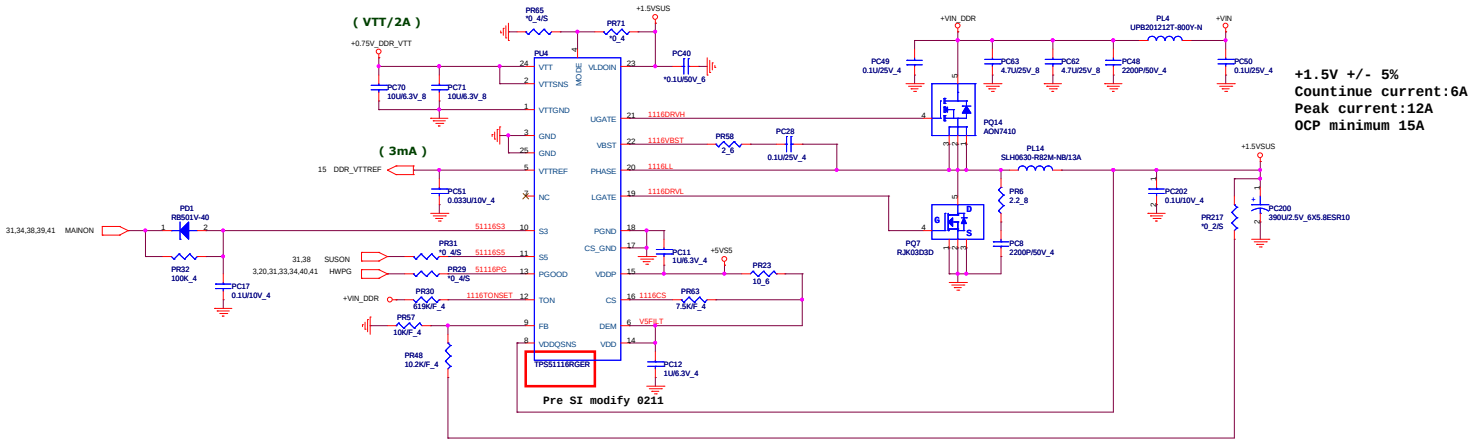
CNTRL1 GPIO6	CNTRL0 GPIO5	N12P-GS
0	0	0.85V
0	1	1V
1	0	1.025V
1	1	NA



PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8208/1.8V)	1A

Date: Wednesday, February 16, 2011 | Sheet 36 of 42



+1.5V +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8207)	1A

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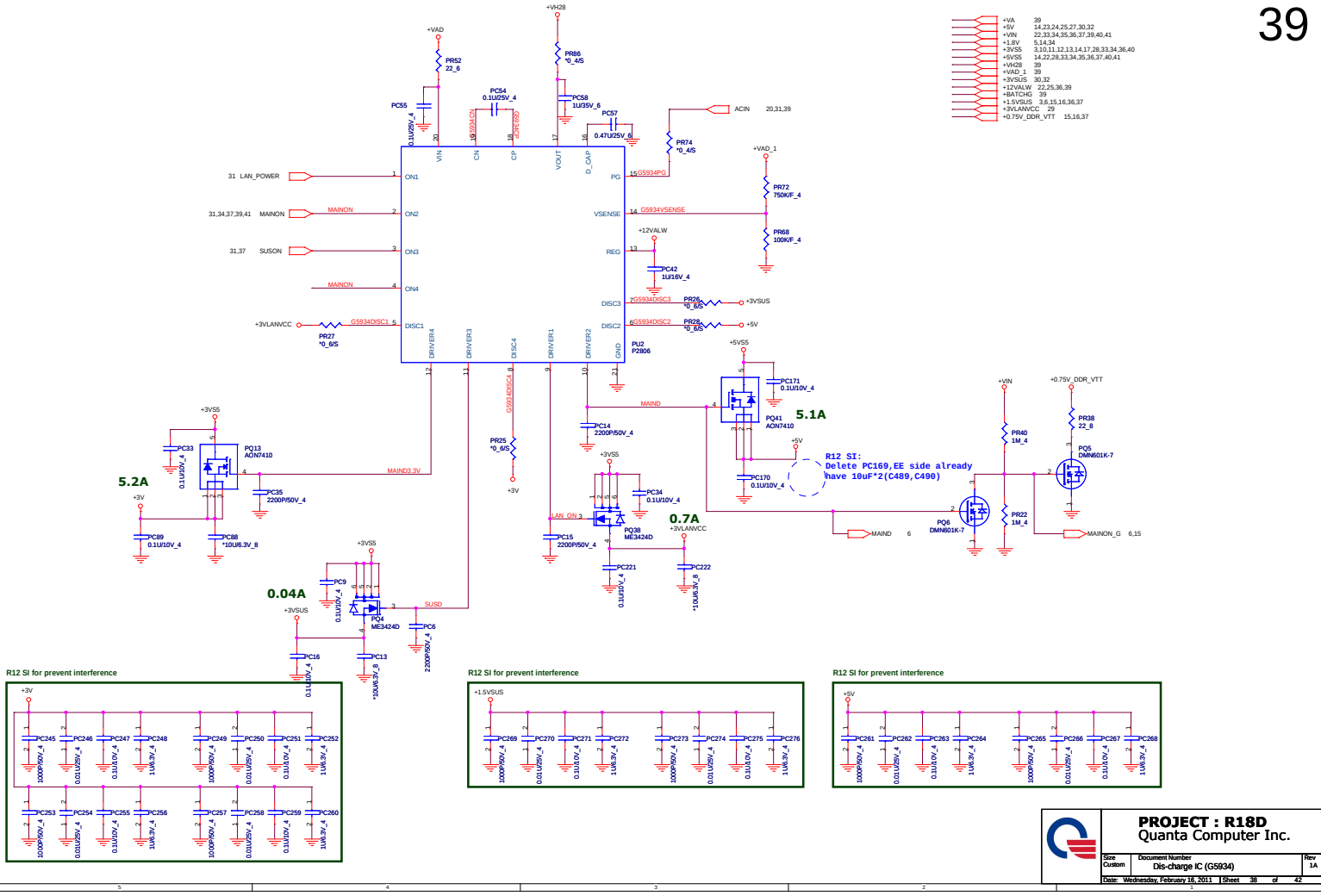

R12 SI for prevent interference

R12 SI for prevent interference

R12 SI for prevent interference

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (G5934)	1A

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DC_JACK
90W

R12 PV:
change footprint.
R12 SI:
M/E modify.

Do Not add test pad on BATDIS_G signal

R12 SI:
M/E modify.

To PWR LED

Place this ZVS close to
Diode away +VIN

Place this ZVS close to
Far-Far away +VIN

Place this cap
close to EC

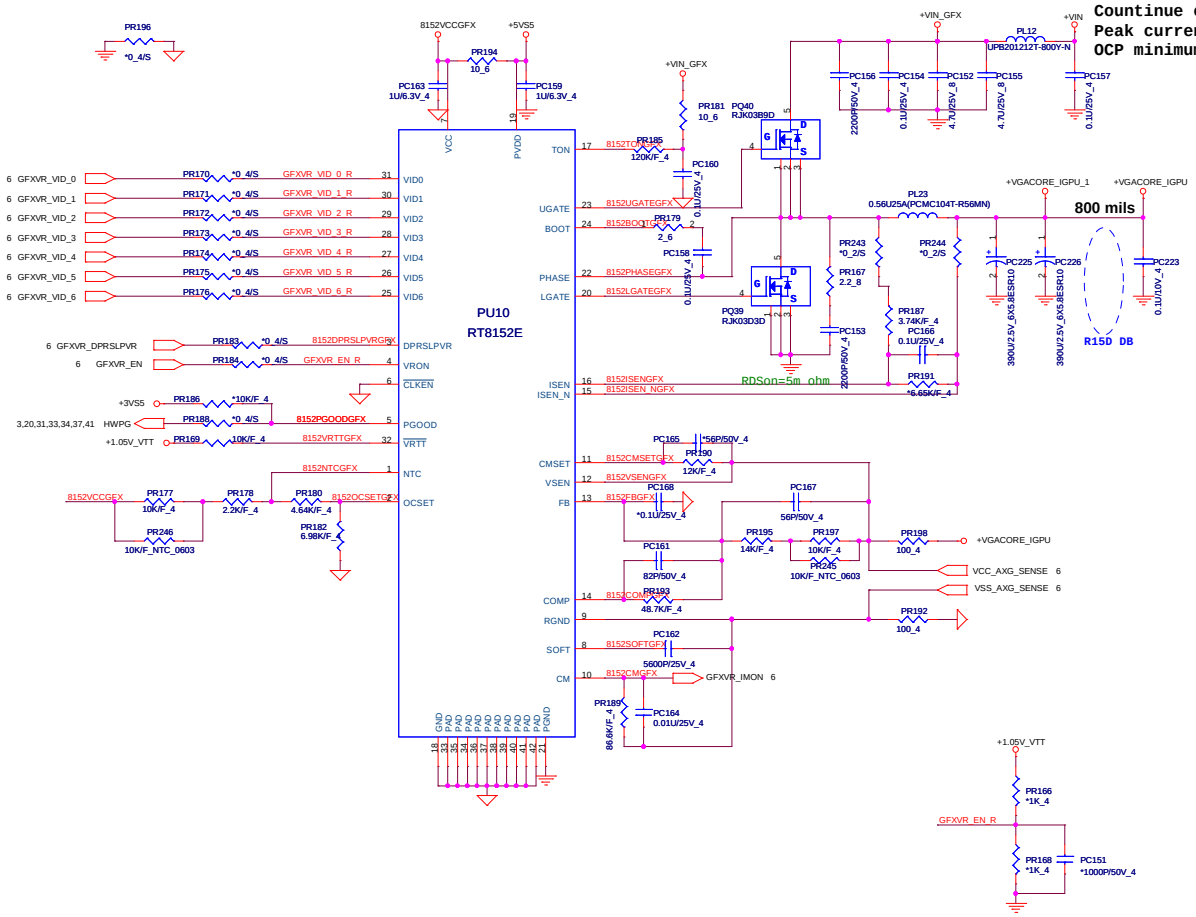
Place this cap
close to EC

Place this cap
close to EC

PU9
OZ8681

PROJECT : R18D		
Quanta Computer Inc.		
Size: Custom	Document Number: Charger (OZ8681)	Rev: 1A
Date: Wednesday, February 16, 2011	Sheet 39 of 42	

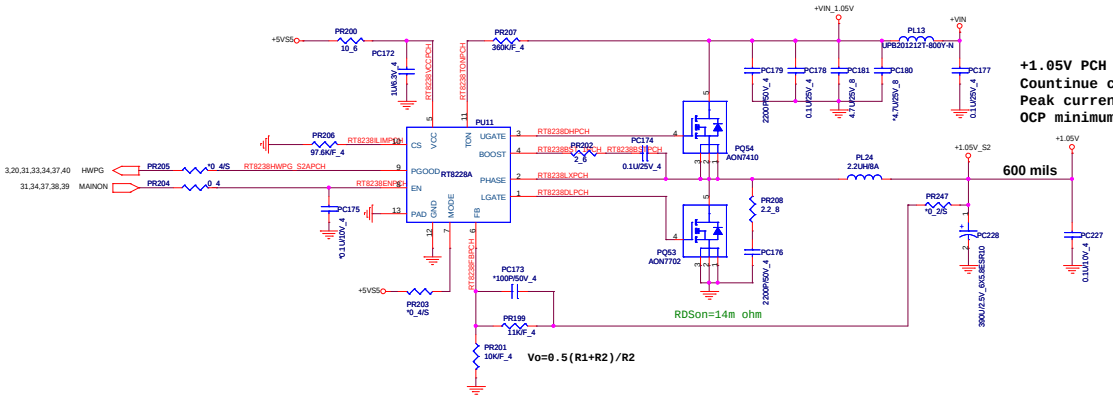
+VGA_UMA +/- 5%
Countinue current:12A
Peak current:18A
OCP minimum 22A



PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	UMA GPU CORE (RT8152C)	1A

Date: Wednesday, February 16, 2011 | Sheet 40 of 42



+1.05V PCH Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.05V (RT8238A)	1A

Date: Wednesday, February 16, 2011 | Sheet 41 of 42

-->Pre SI

Page 19

1.Delete L5005, C5096,C5097,C5098,C5099,C5100 and connect +SP_PLLVDD to +NV_PLLVDD

2.L5004 change to bead 220ohm (ESR=0.5) 0603.
3.C5089 change to 22uF_0805

Page 11

1.delete Q35.

Page 17

1.delete L5000 and C5074.
2.connect +3V_GFX to GPU ball AG9 with a 0.1uF cap C5075.
3.New add R5060 for test

4.L5001 change to bead 120ohm@100MHz (ESR=0.18ohm) 0603.
5.C5073 should be 4.7uF_X7R_0805.
6.C5072 should be 1uF_X7R_0603.
7.C5071 should be 0.1uF_X7R_0402.

8.PCIE change to PEX_TX0~7 and PEX_RX0~7 on GPU side for X8 lane configuration
9.unstuff R5009 and R5008 Q5002 stuff for test
9.delete L5002 for Nvidai recommend

Page 18

1.L5003 change to bead 30ohm (ESR=0.01) 0603.
2.C5085 change to 1uF_X7R_0603
3.Delete C5084.

Page 21

1.R5096 and R5103 change to 162ohm_1%.

Page 31

1.New add R5105 and R5106 2.2K pull up resistors to +3V for GPUT_CLK and GPUT_DATA on EC side.

2.Delete D20,Q25,D19,R500.

Page 20

1.delete R5081,R5082,R5082.

2.New add R5085 and R5086 10K pull down resistors to GFX_CORE_CNTRL0 and GFX_CORE_CNTRL1

3.Change R5047 to 5K pull up for ROM_SCLK

4.Change R5080 to 10K for JTAG_TRST# pull down.
5.R5084 can be no stuff for JTAG_TCK
6.New add Q5010 for AC/Batt# function.

7.New add Q5011.

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
C	Change list	2A

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