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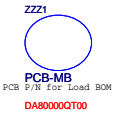
QCL40 MB Schematic Document

LA-8224P

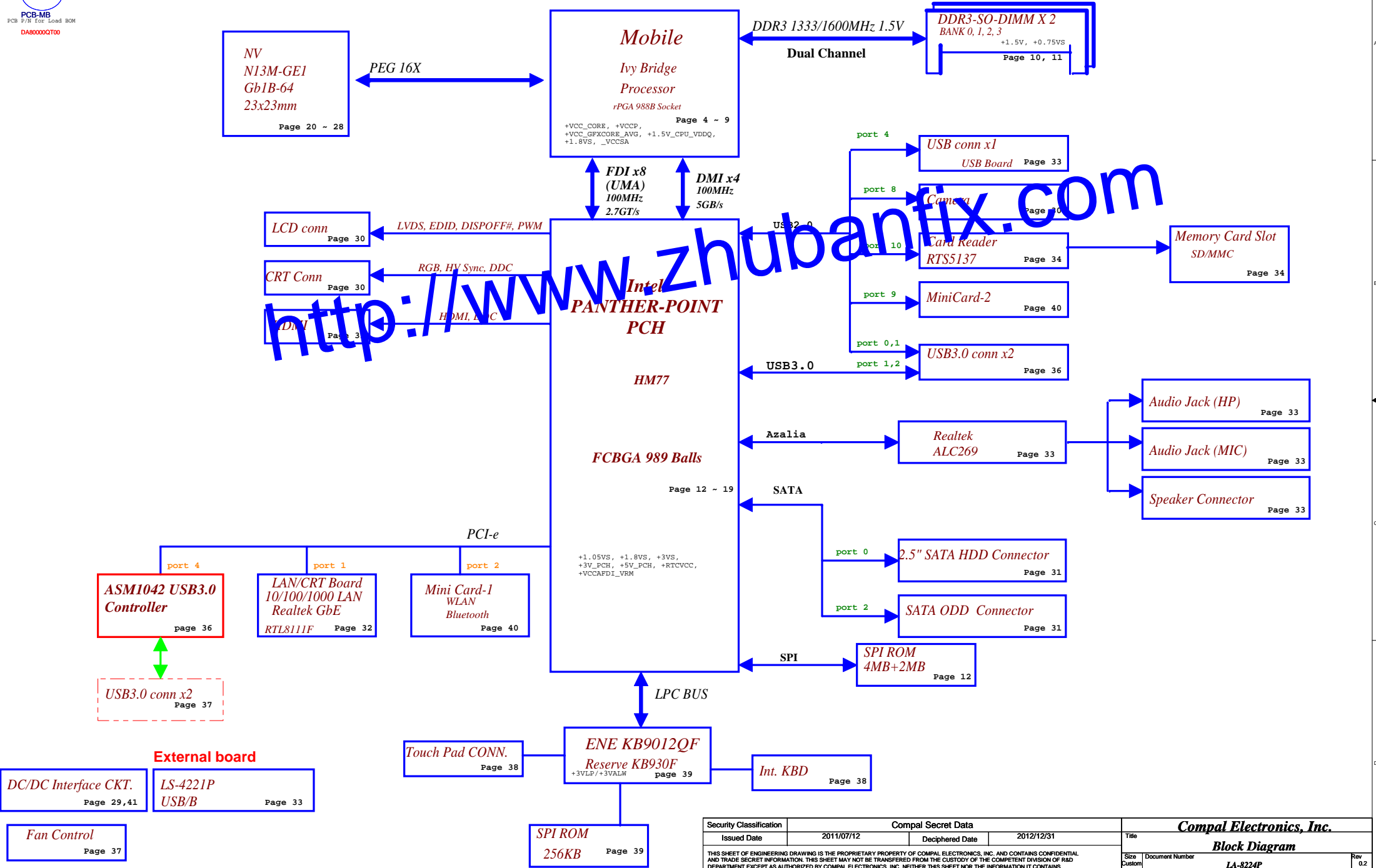
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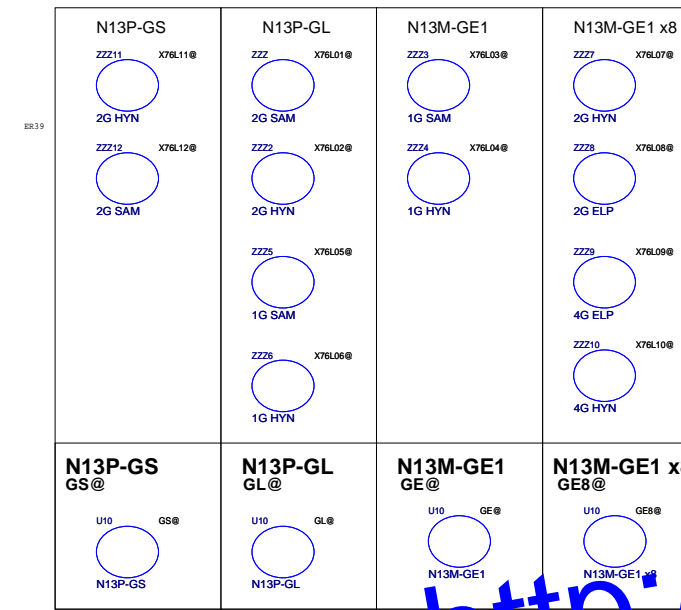
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Issued Date	2011/07/12	Deciphered Date	2012/12/31	Size Document Number <i>Cover Sheet</i>	
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				Date: Thursday, October 27, 2011	



QCL40



X76@: VRAMX16X8 VRAMX16X4 VRAMX8X8



DIS@: VGA componet
GE8@: N13M-GE1_GB1b



9012@: EC(ENE 9012 chip)
930@: EC(ENE 930 chip)
XDP@: Intel debug port

IU3@: USB3.0 by PCH
USB30@:USB3.0 controller IC

AI@: AI Charger
NAI@: Non AI Charger

SMBUS Control Table							
	SOURCE	MINI1	BATT	PCH	EC	SODIMM	DGPU
EC_SMB_CK1 EC_SMB_DA1	KB930	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	V	X	X	V
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	X	X	V	X
PCH_SMLCLK PCH_SMLDATA	PCH	X	X	X	V	X	V

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	CLK_SD_48M
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	USB3.0 controller	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

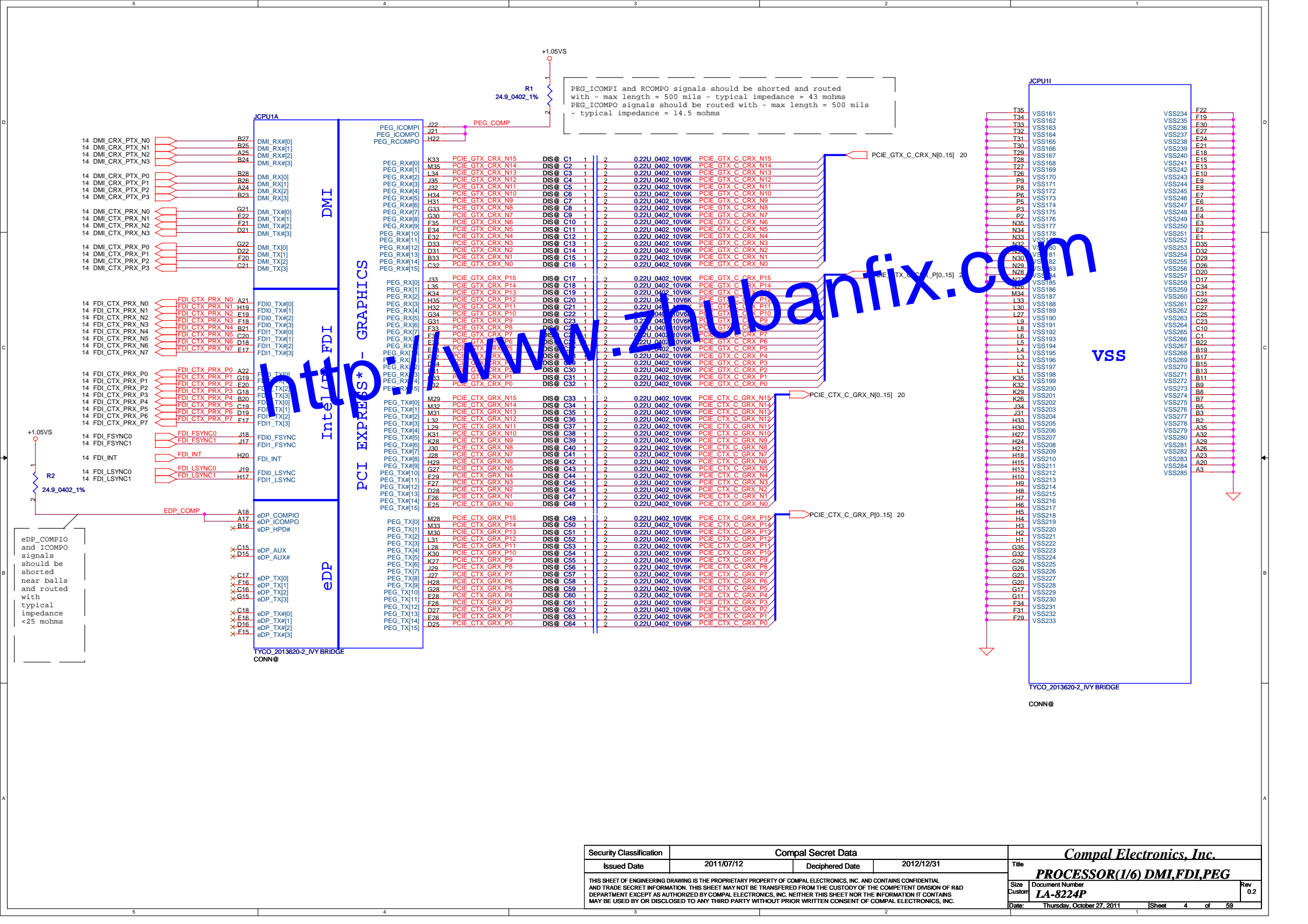
Symbol Note :
 : means Digital Ground
 : means Analog Ground

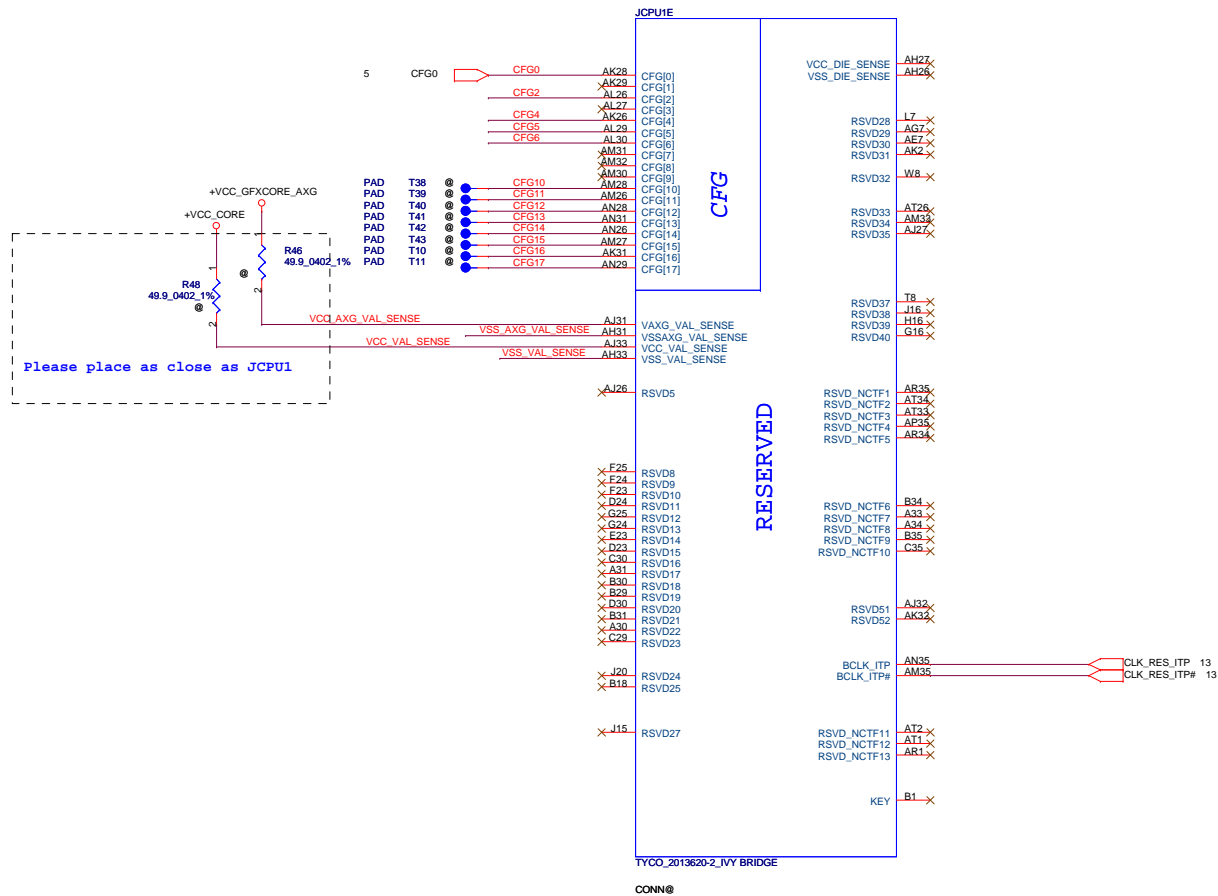
CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	LPC Debug Port
PCI4	None

Voltage Rails

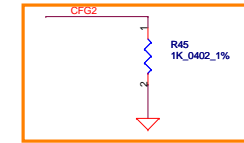
Power Plane	Description	S1	S3	Deep S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A
+3VLP	3.3V power rail for 510N power management	ON	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+LAN_IO	3.3V power rail for ethernet	ON	OFF	OFF	OFF
+3VS_WLAN	3.3V power rail for WLAN/BT Combo	ON	OFF	OFF	OFF
+3V_PCH	3.3V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+3VS	3.3V power rail for CPU, PCH, HDD, Audio, Card Reader	ON	OFF	OFF	OFF
+3VSG	3.3V power rail for VDDQ	ON	OFF	OFF	OFF
+LVDDQ	1.5V power rail for LCD	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+5V_PCH	5V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+5VS	5V power rail for HDD, AUDIO, FAN, Touch PAD	ON	OFF	OFF	OFF
+5VS_ODD	5V power rail for SATA ODD	ON	OFF	OFF	OFF
+1.8VS	1.8V power rail for CPU, PCH	ON	OFF	OFF	OFF
+1.05VS	1.05V power rail for PCH	ON	OFF	OFF	OFF
+VCCP	1.05V power rail for CPU VCCIO, PCH	ON	OFF	OFF	OFF
+1.05VSG	1.05V power rail for N13P	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR3 system memory	ON	ON	ON	OFF
+1.5V_CPU_VDDQ	1.5V power rail CPU VDDQ	ON	OFF	OFF	OFF
+1.5VSG	1.5V power rail for N13P, VRAM	ON	OFF	OFF	OFF
+1.5VS	1.5V power rail for PCH, WLAN/BT combo	ON	OFF	OFF	OFF
+0.75VS	0.75V power rail for DDR VREF	ON	OFF	OFF	OFF
+VCCSA	VCCSA for CPU system agent	ON	OFF	OFF	OFF
+VCC_CORE	CORE Voltage for CPU	ON	OFF	OFF	OFF
+VCC_GFXCORE_AXG	1.5V power rail for N13P, VRAM	ON	OFF	OFF	OFF
+VGA_CORE	CORE Voltage for N13P Graphics ON OFF OFF	ON	OFF	OFF	OFF

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None



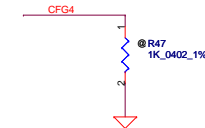


CFG Straps for Processor



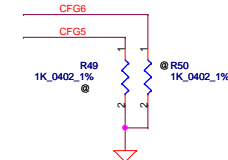
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed
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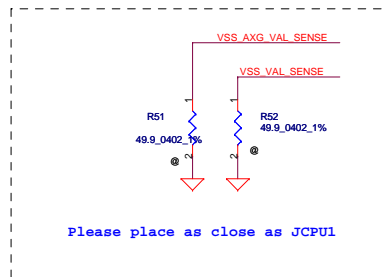
Display Port Presence Strap

CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
------	--



PCIE Port Bifurcation Straps

CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
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POWER

+VCC_CORE

97A

AG35 VCC1
AG34 VCC2
AG33 VCC3
AG32 VCC4
AG31 VCC5
AG30 VCC6
AG29 VCC7
AG28 VCC8
AG27 VCC9
AF36 VCC10
AF35 VCC11
AF34 VCC12
AF33 VCC13
AF32 VCC14
AF31 VCC15
AF30 VCC16
AF29 VCC17
AF28 VCC18
AF27 VCC19
AD35 VCC20
AD34 VCC21
AD33 VCC22
AD32 VCC23
AD31 VCC24
AD30 VCC25
AD29 VCC26
AD27 VCC27
AD26 VCC28
AC35 VCC29
AC34 VCC30
AC33 VCC31
AC32 VCC32
AC31 VCC33
AC30 VCC34
AC29 VCC35
AC28 VCC36
AC27 VCC37
AC26 VCC38
AA35 VCC39
AA34 VCC40
AA33 VCC41
AA32 VCC42
AA31 VCC43
AA30 VCC44
AA29 VCC45
AA28 VCC46
AA27 VCC47
AA26 VCC48
Y35 VCC49
Y34 VCC50
Y33 VCC51
Y32 VCC52
Y31 VCC53
Y30 VCC54
Y29 VCC55
Y28 VCC56
Y27 VCC57
Y26 VCC58
Y25 VCC59
Y24 VCC60
Y23 VCC61
Y22 VCC62
Y21 VCC63
Y20 VCC64
Y19 VCC65
Y18 VCC66
Y17 VCC67
Y16 VCC68
Y15 VCC69
Y14 VCC70
Y13 VCC71
Y12 VCC72
Y11 VCC73
Y10 VCC74
Y09 VCC75
Y08 VCC76
Y07 VCC77
Y06 VCC78
Y05 VCC79
Y04 VCC80
Y03 VCC81
Y02 VCC82
Y01 VCC83
Y00 VCC84
Y00 VCC85
Y00 VCC86
Y00 VCC87
Y00 VCC88
Y00 VCC89
Y00 VCC90
Y00 VCC91
Y00 VCC92
Y00 VCC93
Y00 VCC94
Y00 VCC95
Y00 VCC96
Y00 VCC97
Y00 VCC98
Y00 VCC99
Y00 VCC100

TYCO_2013620-2_IVY BRIDGE

CONN@

PEG AND DDR

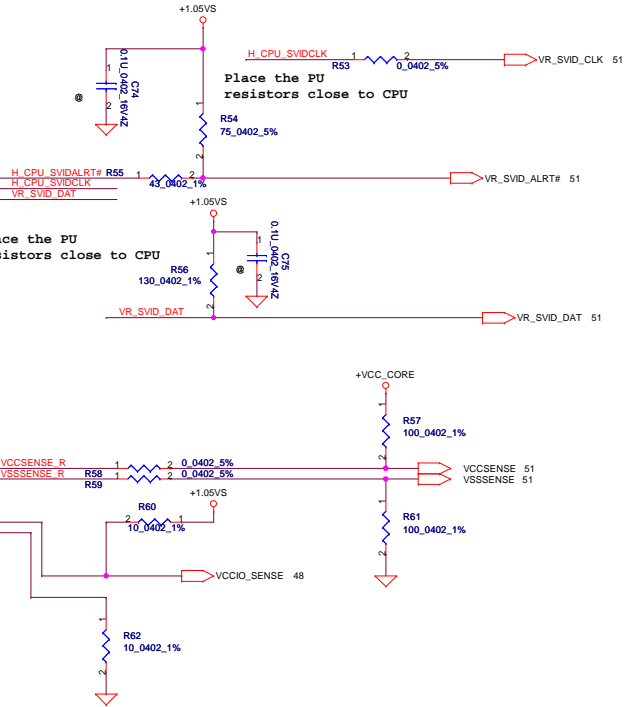
SVID

SENSE LINES

8.5A

AH13 VCCIO1
AH10 VCCIO2
AG10 VCCIO3
AC10 VCCIO4
Y10 VCCIO5
U10 VCCIO6
F10 VCCIO7
I10 VCCIO8
J14 VCCIO9
J13 VCCIO10
J12 VCCIO11
H11 VCCIO12
H14 VCCIO13
H12 VCCIO14
H11 VCCIO15
G14 VCCIO16
G13 VCCIO17
G12 VCCIO18
F14 VCCIO19
F13 VCCIO20
F12 VCCIO21
E11 VCCIO22
E14 VCCIO23
E12 VCCIO24

E11 VCCIO25
D14 VCCIO26
D13 VCCIO27
D12 VCCIO28
D11 VCCIO29
C14 VCCIO30
C13 VCCIO31
C12 VCCIO32
C11 VCCIO33
B14 VCCIO34
B12 VCCIO35
A14 VCCIO36
A13 VCCIO37
A12 VCCIO38
A11 VCCIO39
J23 VCCIO40

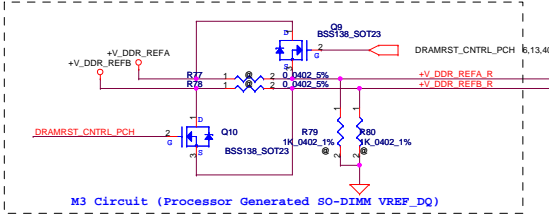
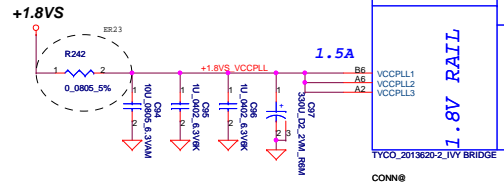
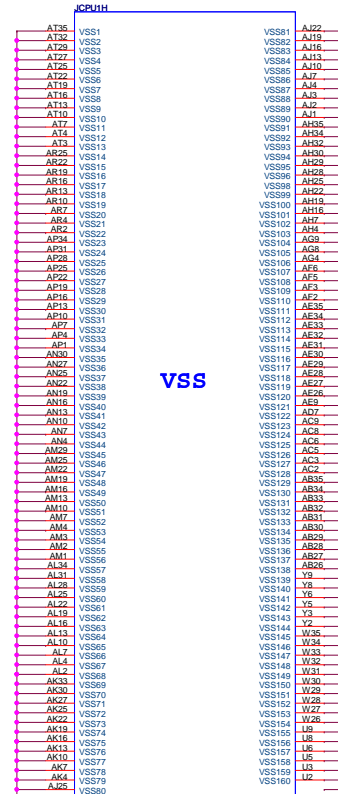
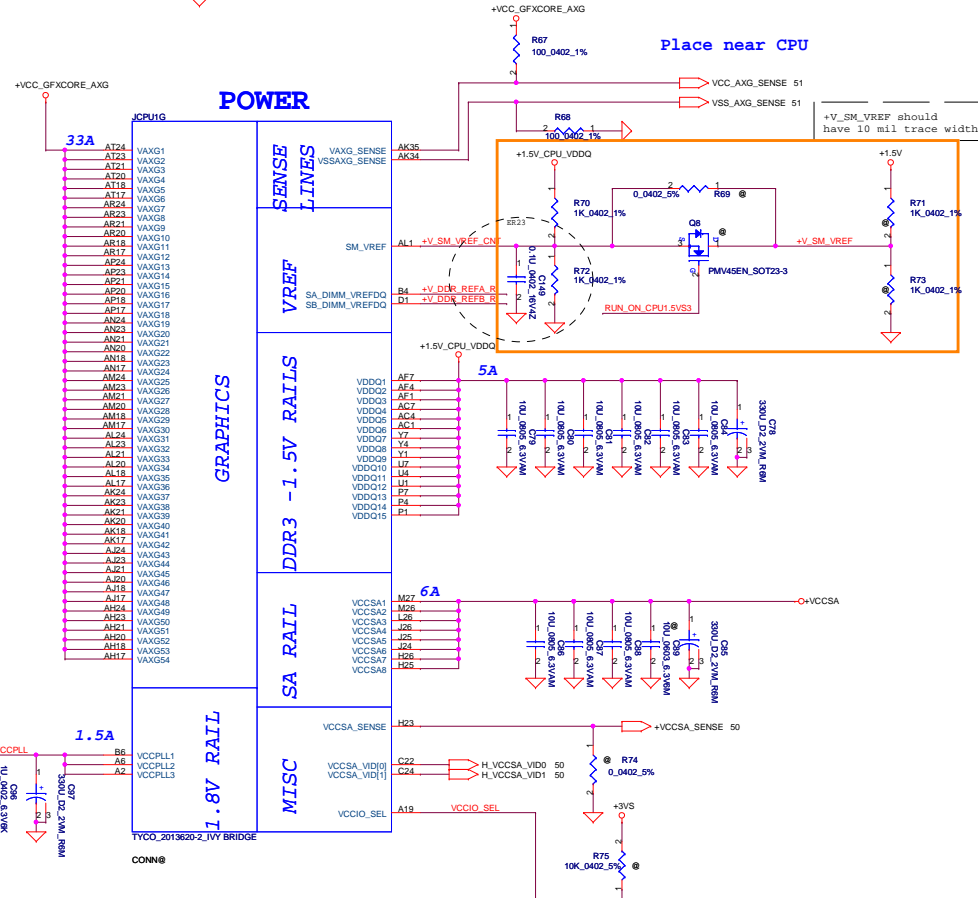
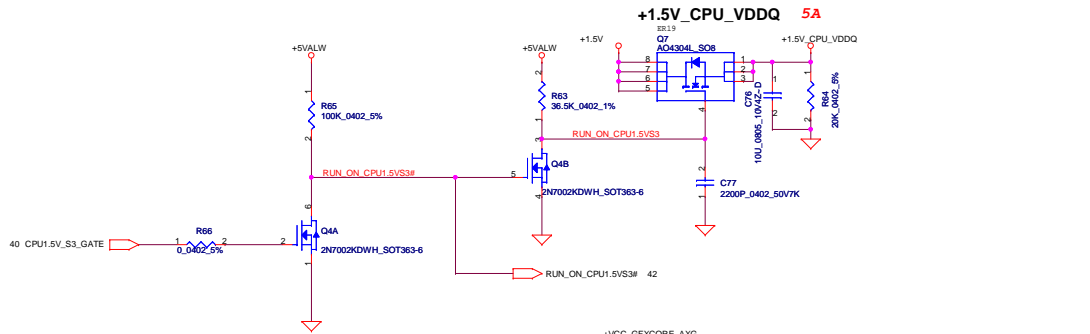


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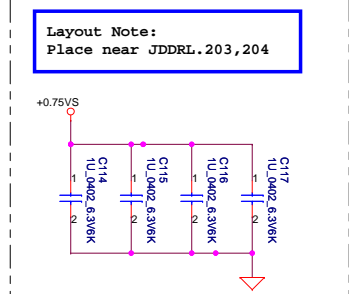
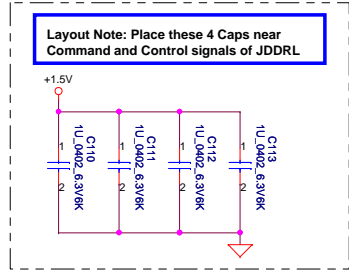
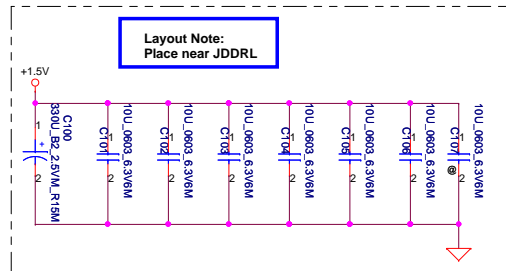
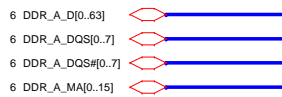
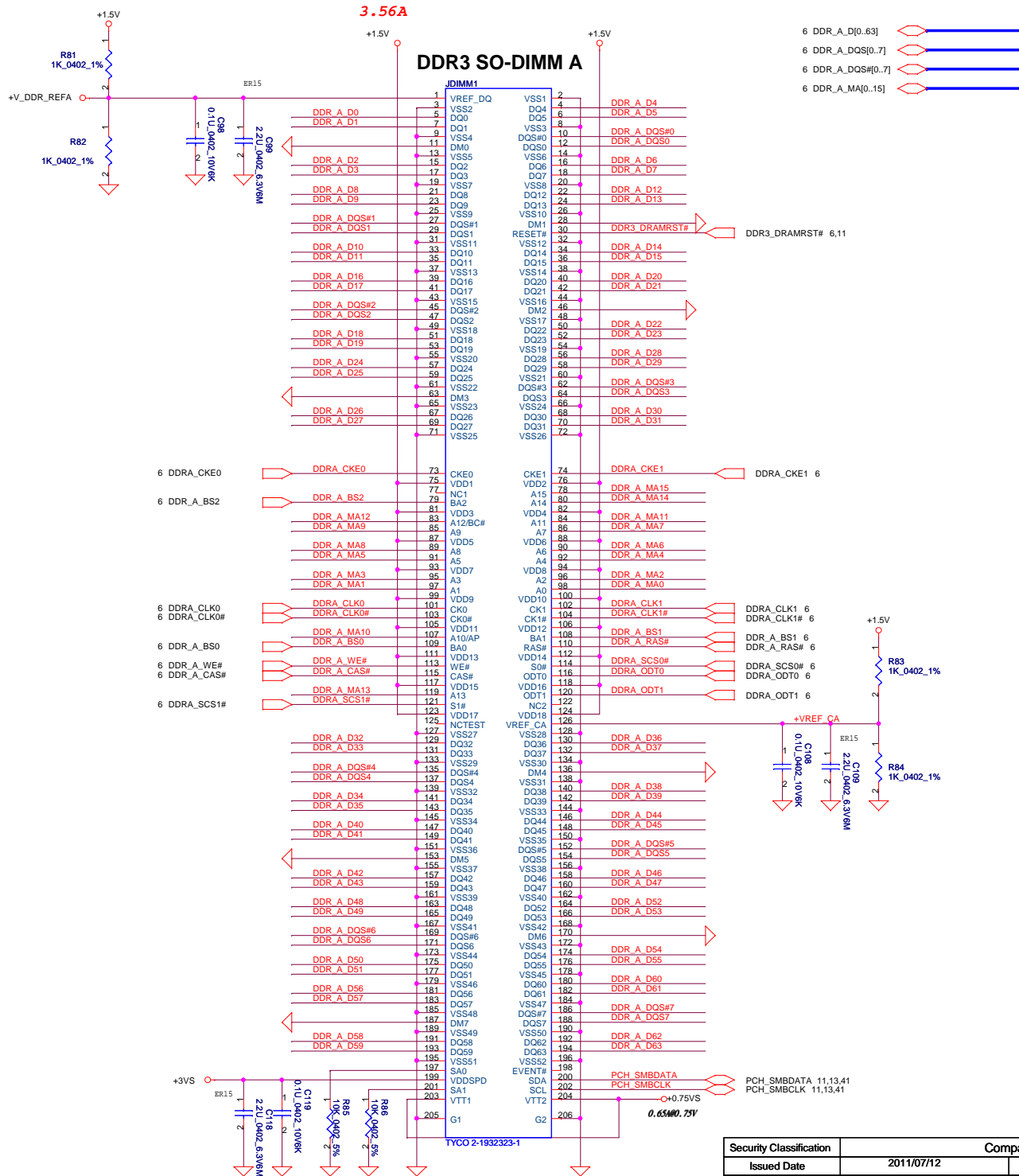
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PROCESSOR(5/6) PWR,BYPASS

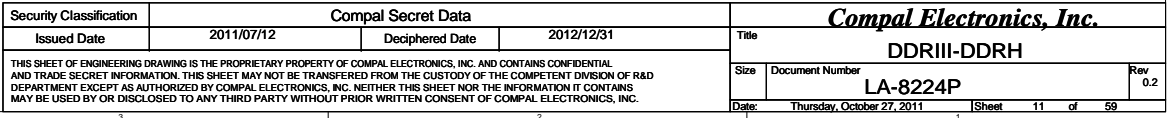
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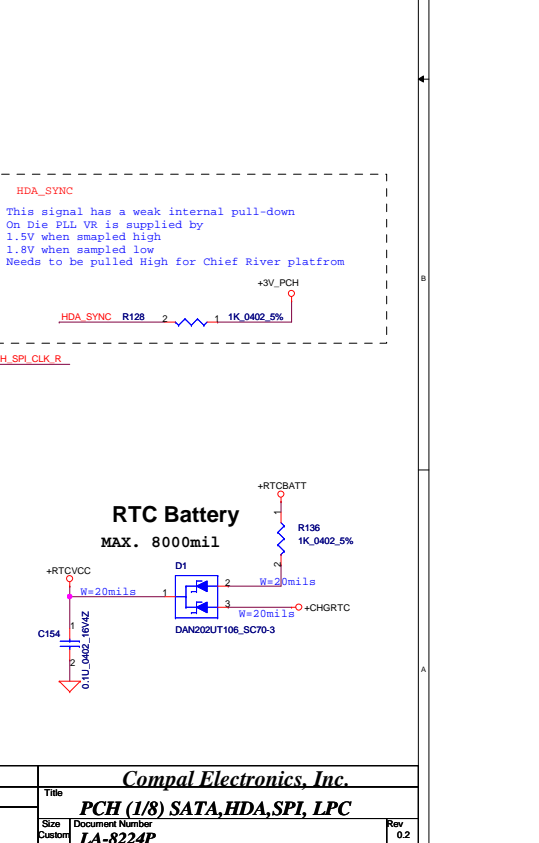
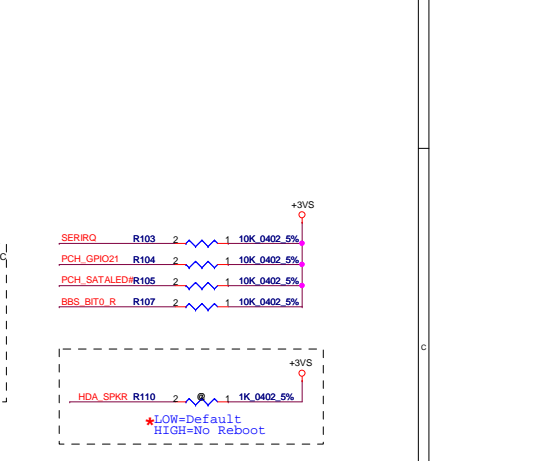
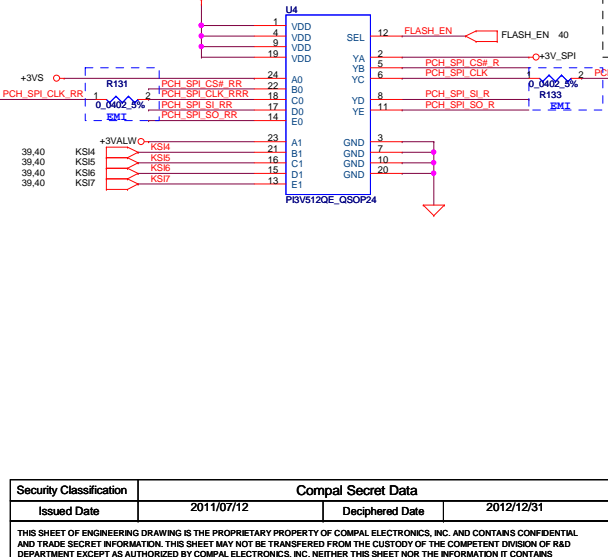
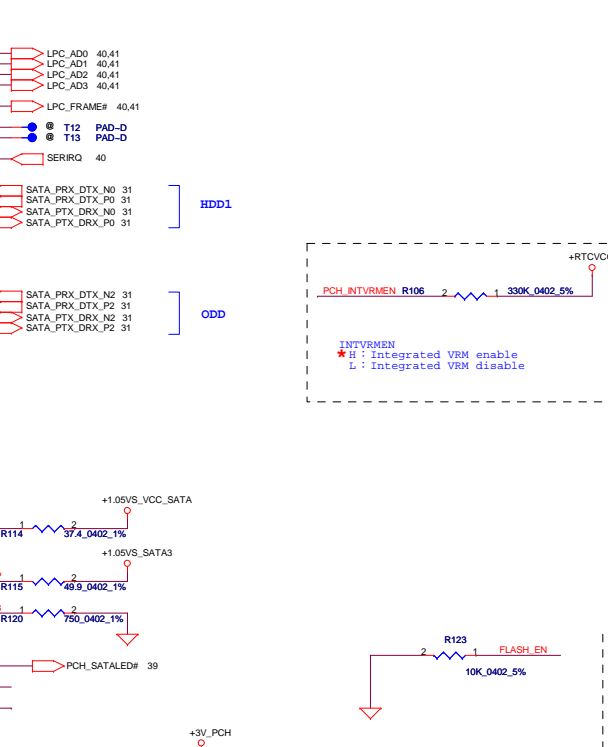
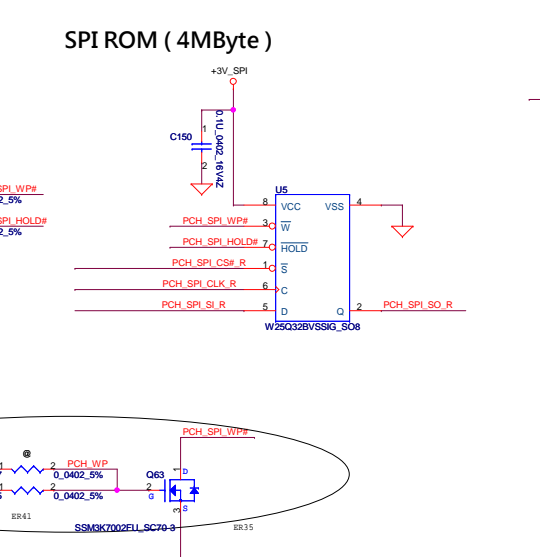
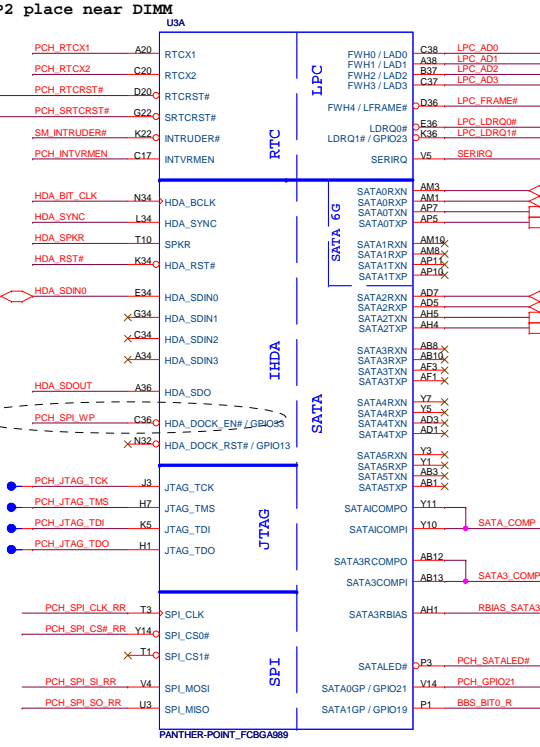
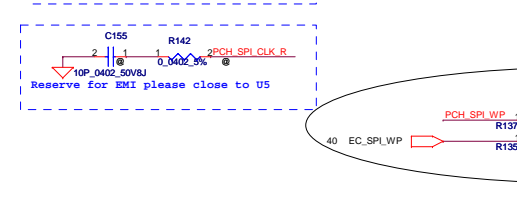
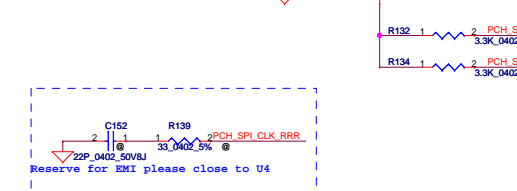
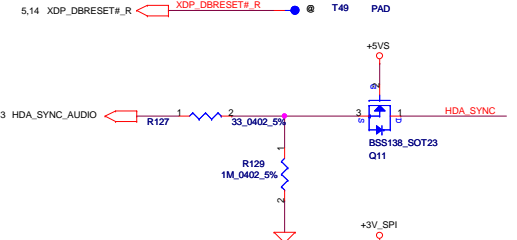
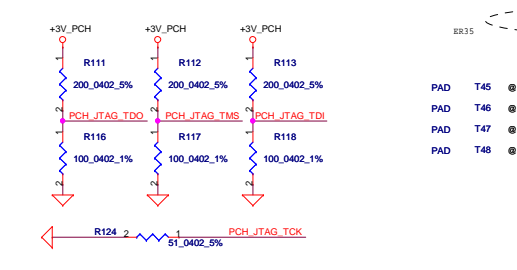
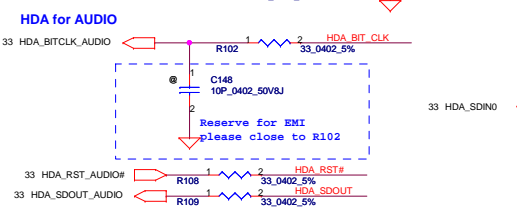
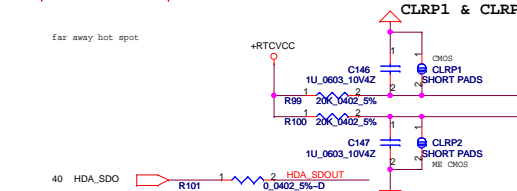
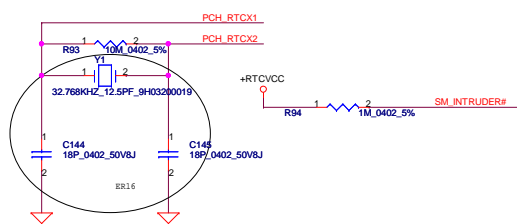


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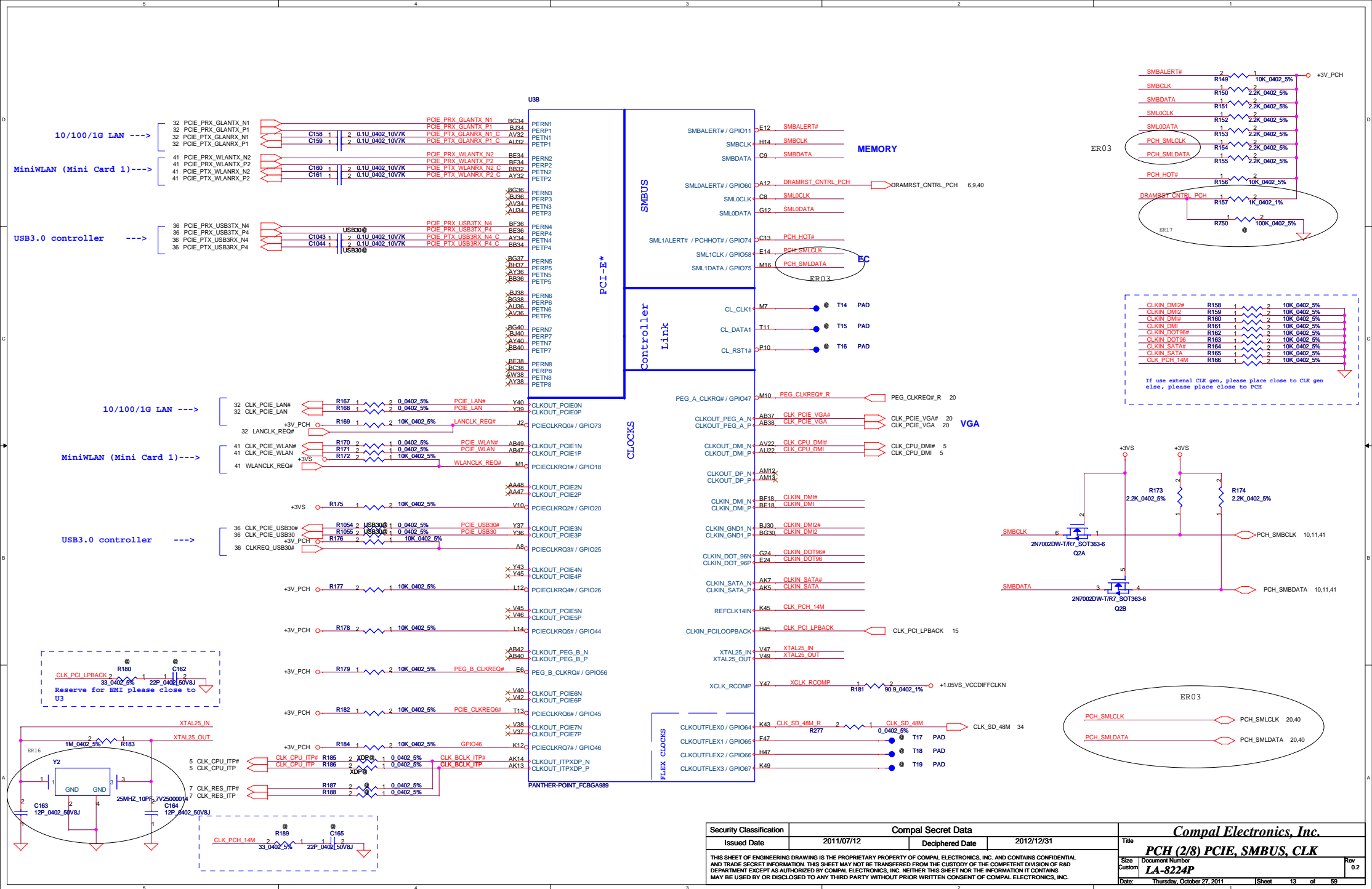


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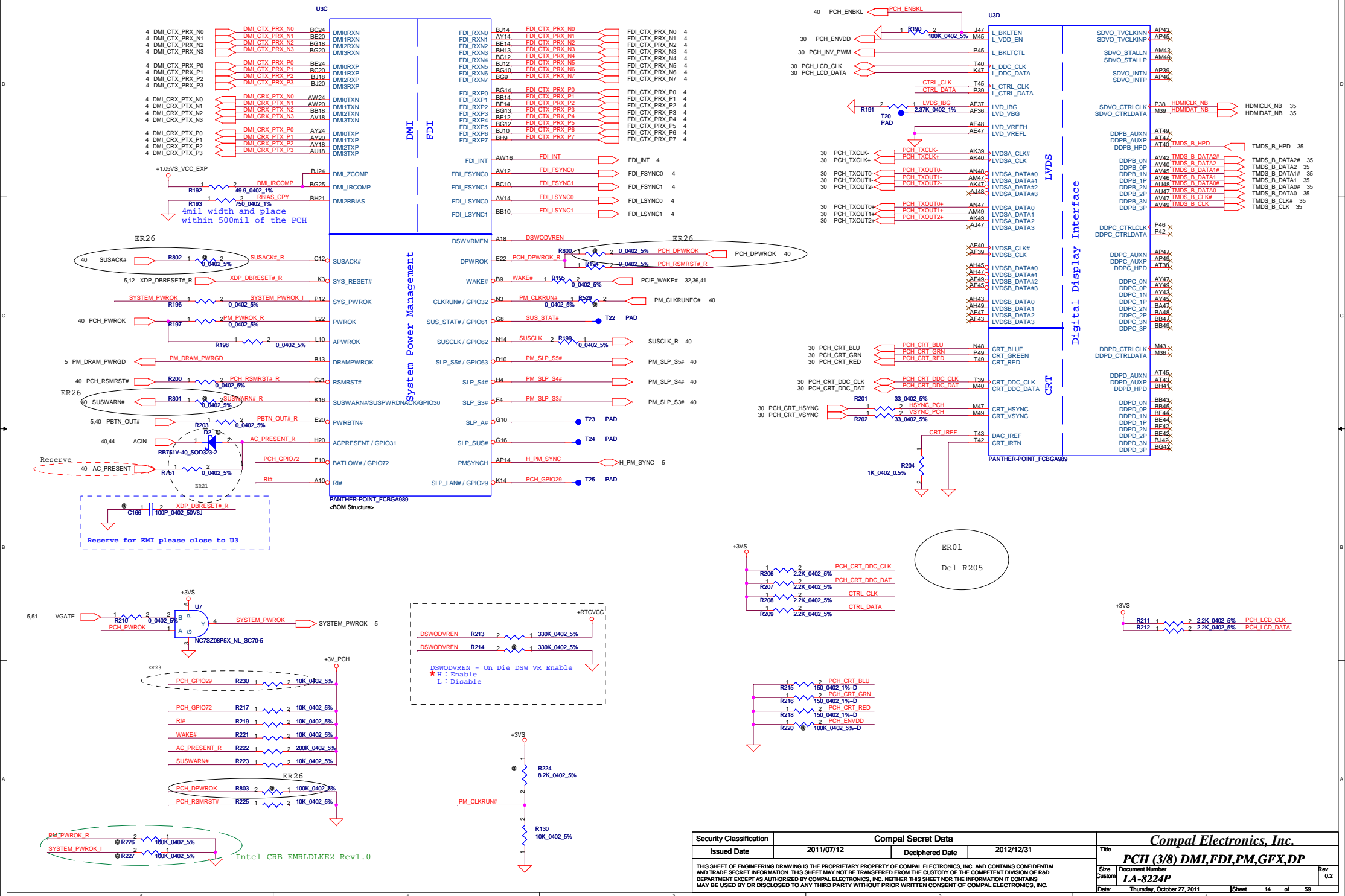


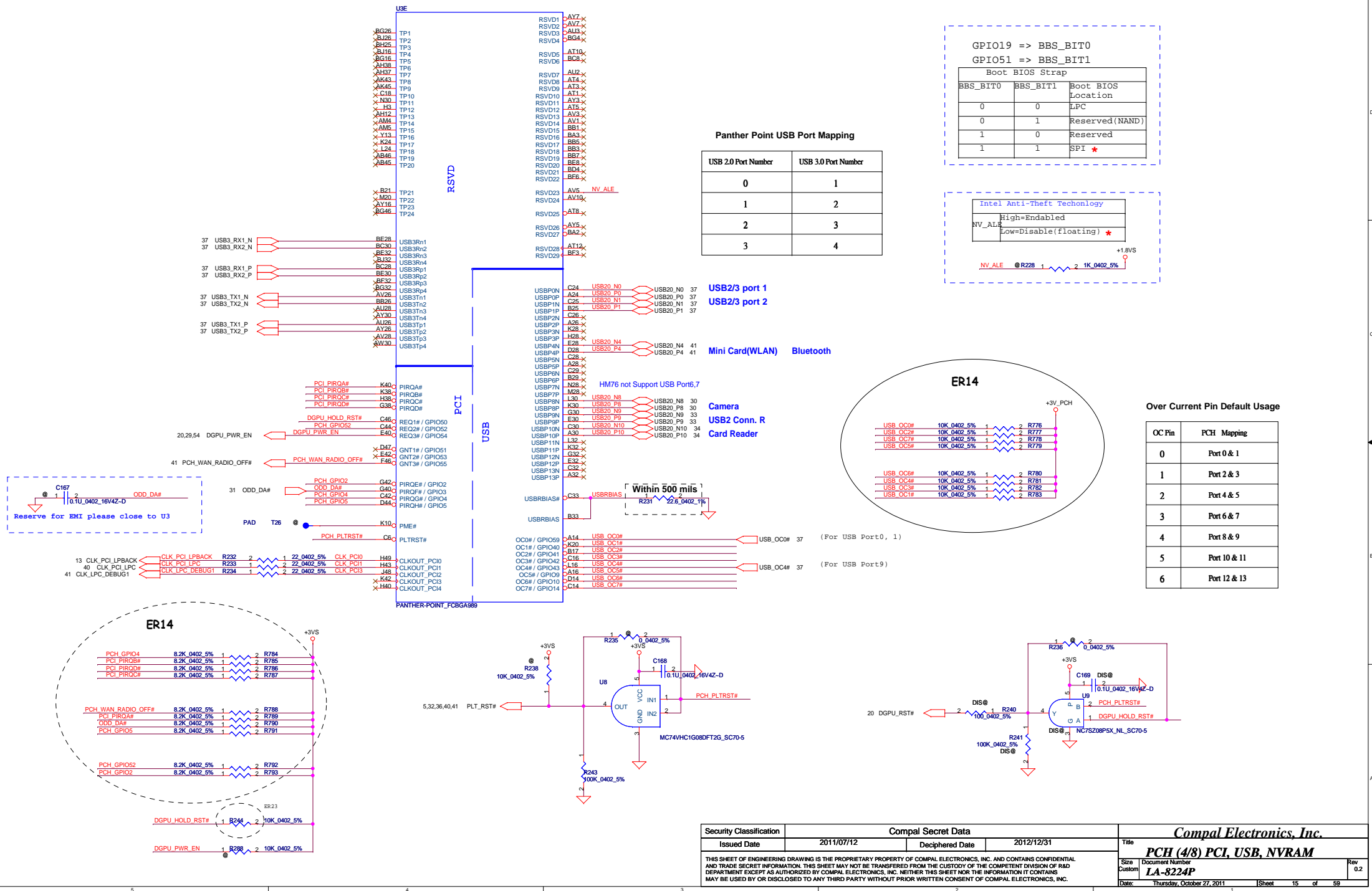


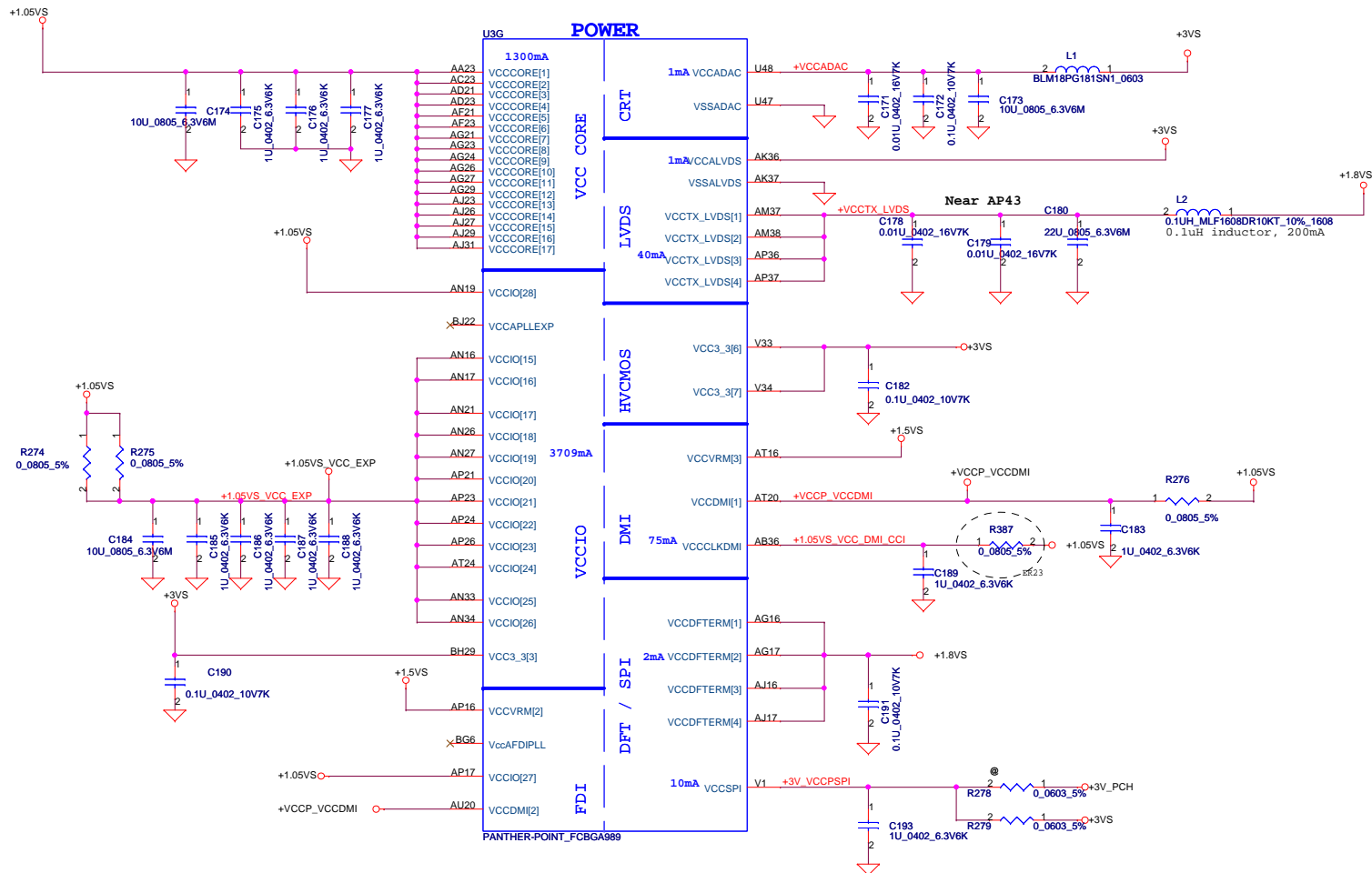
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		PCH (1/8) SATA,HDA,SPI, LPC	
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PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	60 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

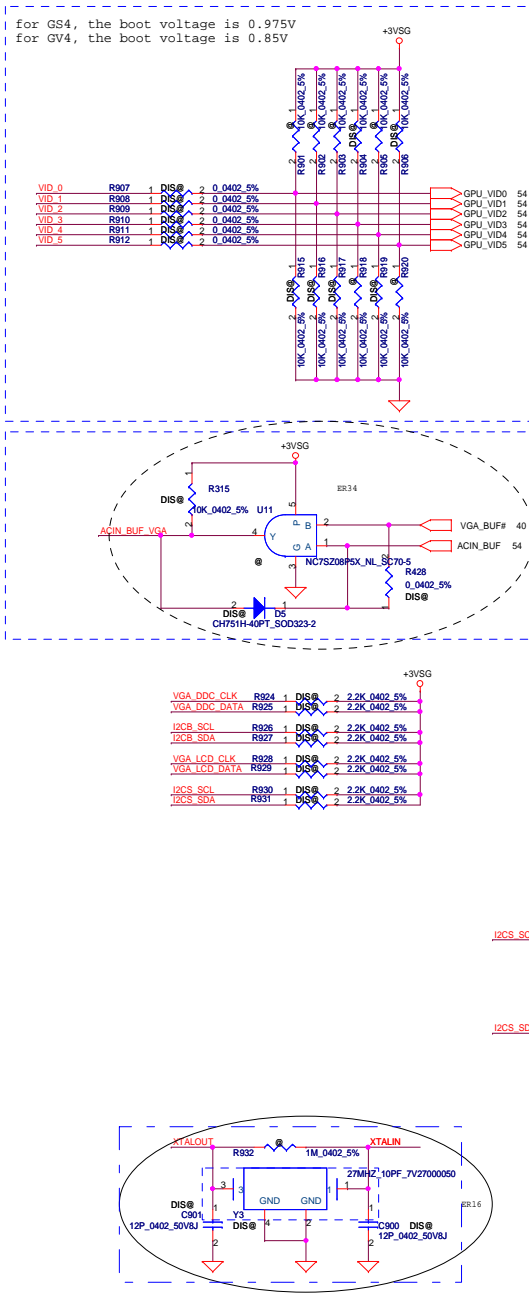
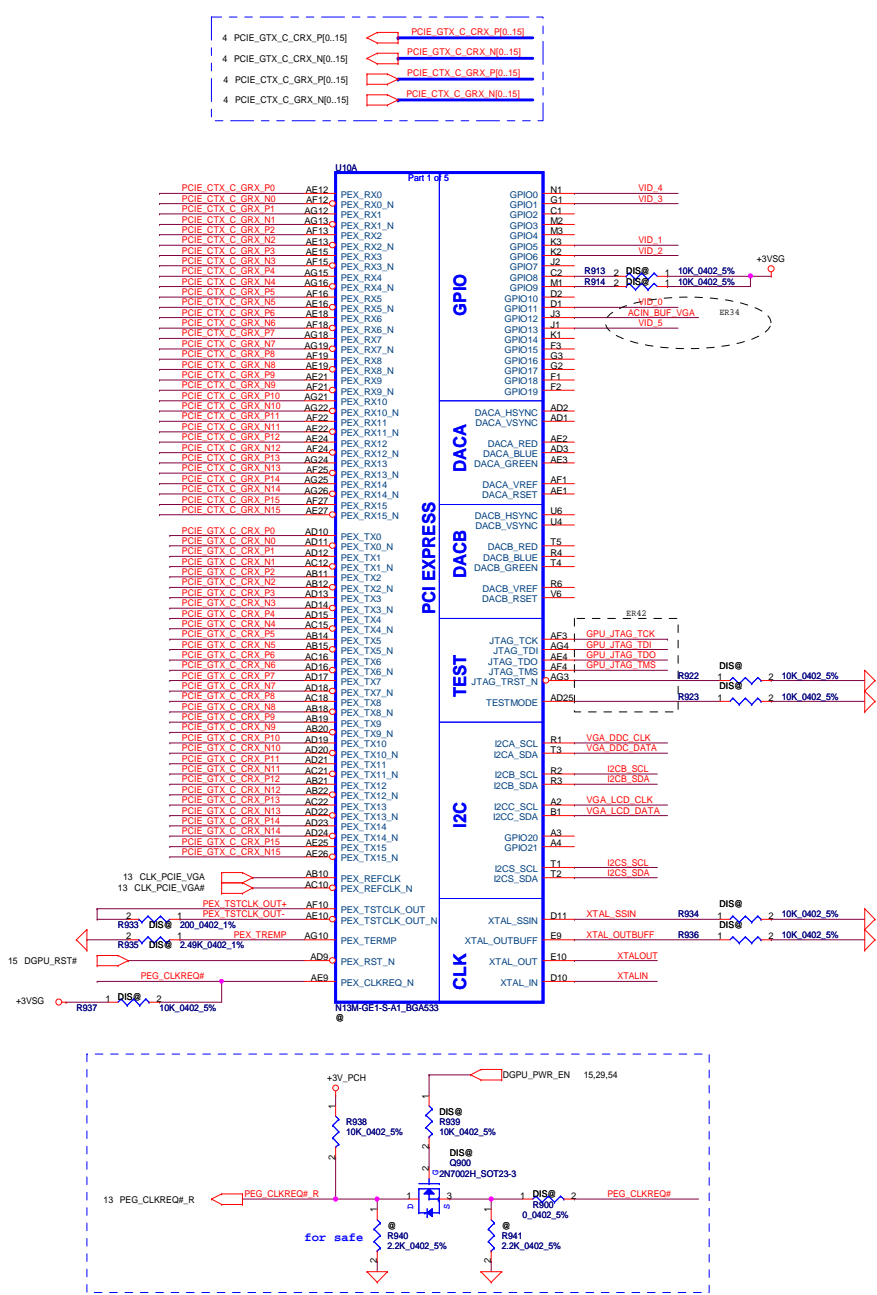
U3H		
H5	VSS[0]	
AA17	VSS[1]	VSS[80]
AA2	VSS[2]	VSS[81]
AA3	VSS[3]	VSS[82]
AA33	VSS[4]	VSS[83]
AA34	VSS[5]	VSS[84]
AB11	VSS[6]	VSS[85]
AB14	VSS[7]	VSS[86]
AB39	VSS[8]	VSS[87]
AB4	VSS[9]	VSS[88]
AB43	VSS[10]	VSS[89]
AB5	VSS[11]	VSS[90]
AB7	VSS[12]	VSS[91]
AC19	VSS[13]	VSS[92]
AC2	VSS[14]	VSS[93]
AC21	VSS[15]	VSS[94]
AC24	VSS[16]	VSS[95]
AC33	VSS[17]	VSS[96]
AC34	VSS[18]	VSS[97]
AC48	VSS[19]	VSS[98]
AD10	VSS[20]	VSS[99]
AD11	VSS[21]	VSS[100]
AD12	VSS[22]	VSS[101]
AD13	VSS[23]	VSS[102]
AD19	VSS[24]	VSS[103]
AD24	VSS[25]	VSS[104]
AD26	VSS[26]	VSS[105]
AD27	VSS[27]	VSS[106]
AD33	VSS[28]	VSS[107]
AD34	VSS[29]	VSS[108]
AD36	VSS[30]	VSS[109]
AD37	VSS[31]	VSS[110]
AD38	VSS[32]	VSS[111]
AD39	VSS[33]	VSS[112]
AD4	VSS[34]	VSS[113]
AD40	VSS[35]	VSS[114]
AD42	VSS[36]	VSS[115]
AD43	VSS[37]	VSS[116]
AD45	VSS[38]	VSS[117]
AD46	VSS[39]	VSS[118]
AD8	VSS[40]	VSS[119]
AE2	VSS[41]	VSS[120]
AE3	VSS[42]	VSS[121]
AE10	VSS[43]	VSS[122]
AE12	VSS[44]	VSS[123]
AD14	VSS[45]	VSS[124]
AD16	VSS[46]	VSS[125]
AF16	VSS[47]	VSS[126]
AF19	VSS[48]	VSS[127]
AF24	VSS[49]	VSS[128]
AF26	VSS[50]	VSS[129]
AF27	VSS[51]	VSS[130]
AF29	VSS[52]	VSS[131]
AF31	VSS[53]	VSS[132]
AF38	VSS[54]	VSS[133]
AF4	VSS[55]	VSS[134]
AF42	VSS[56]	VSS[135]
AF46	VSS[57]	VSS[136]
AF5	VSS[58]	VSS[137]
AF7	VSS[59]	VSS[138]
AF8	VSS[60]	VSS[139]
AG19	VSS[61]	VSS[140]
AG2	VSS[62]	VSS[141]
AG31	VSS[63]	VSS[142]
AG48	VSS[64]	VSS[143]
AH11	VSS[65]	VSS[144]
AH3	VSS[66]	VSS[145]
AH36	VSS[67]	VSS[146]
AH39	VSS[68]	VSS[147]
AH40	VSS[69]	VSS[148]
AH42	VSS[70]	VSS[149]
AH46	VSS[71]	VSS[150]
AH7	VSS[72]	VSS[151]
AJ19	VSS[73]	VSS[152]
AJ21	VSS[74]	VSS[153]
AJ24	VSS[75]	VSS[154]
AJ33	VSS[76]	VSS[155]
AJ34	VSS[77]	VSS[156]
AK12	VSS[78]	VSS[157]
AK3	VSS[79]	VSS[158]

PANTHER-POINT_FCBGA989

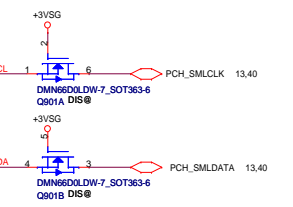
U3I		
AY4	VSS[159]	VSS[259]
AY42	VSS[160]	VSS[260]
AY46	VSS[161]	VSS[261]
AY8	VSS[162]	VSS[262]
B11	VSS[163]	VSS[263]
B15	VSS[164]	VSS[264]
B19	VSS[165]	VSS[265]
B23	VSS[166]	VSS[266]
B27	VSS[167]	VSS[267]
B31	VSS[168]	VSS[268]
B35	VSS[169]	VSS[269]
B39	VSS[170]	VSS[270]
B7	VSS[171]	VSS[271]
F45	VSS[172]	VSS[272]
BB12	VSS[173]	VSS[273]
BB16	VSS[174]	VSS[274]
BB20	VSS[175]	VSS[275]
BB22	VSS[176]	VSS[276]
BB24	VSS[177]	VSS[277]
BB28	VSS[178]	VSS[278]
BB30	VSS[179]	VSS[279]
BB38	VSS[180]	VSS[280]
BB4	VSS[181]	VSS[281]
BB46	VSS[182]	VSS[282]
BC14	VSS[183]	VSS[283]
BC18	VSS[184]	VSS[284]
BC2	VSS[185]	VSS[285]
BC22	VSS[186]	VSS[286]
BC26	VSS[187]	VSS[287]
BC32	VSS[188]	VSS[288]
BC34	VSS[189]	VSS[289]
BC36	VSS[190]	VSS[290]
BC40	VSS[191]	VSS[291]
BC42	VSS[192]	VSS[292]
BC48	VSS[193]	VSS[293]
BD46	VSS[194]	VSS[294]
BD5	VSS[195]	VSS[295]
BE22	VSS[196]	VSS[296]
BE26	VSS[197]	VSS[297]
BE40	VSS[198]	VSS[298]
BF10	VSS[199]	VSS[299]
BF12	VSS[200]	VSS[300]
BF16	VSS[201]	VSS[301]
BF20	VSS[202]	VSS[302]
BF22	VSS[203]	VSS[303]
BF24	VSS[204]	VSS[304]
BF26	VSS[205]	VSS[305]
BF28	VSS[206]	VSS[306]
BF3	VSS[207]	VSS[307]
BF30	VSS[208]	VSS[308]
BF38	VSS[209]	VSS[309]
BF40	VSS[210]	VSS[310]
BF8	VSS[211]	VSS[311]
BG17	VSS[212]	VSS[312]
BG21	VSS[213]	VSS[313]
BG33	VSS[214]	VSS[314]
BG44	VSS[215]	VSS[315]
BG8	VSS[216]	VSS[316]
BH11	VSS[217]	VSS[317]
BH15	VSS[218]	VSS[318]
BH17	VSS[219]	VSS[319]
BH19	VSS[220]	VSS[320]
H10	VSS[221]	VSS[321]
BH27	VSS[222]	VSS[322]
BH33	VSS[223]	VSS[323]
BH35	VSS[224]	VSS[324]
BH39	VSS[225]	VSS[325]
BH43	VSS[226]	VSS[326]
BH7	VSS[227]	VSS[327]
D3	VSS[228]	VSS[328]
D12	VSS[229]	VSS[329]
D18	VSS[230]	VSS[330]
D22	VSS[231]	VSS[331]
D24	VSS[232]	VSS[332]
D26	VSS[233]	VSS[333]
D30	VSS[234]	VSS[334]
D32	VSS[235]	VSS[335]
D34	VSS[236]	VSS[336]
D38	VSS[237]	VSS[337]
D42	VSS[238]	VSS[338]
D8	VSS[239]	VSS[339]
E18	VSS[240]	VSS[340]
E26	VSS[241]	VSS[341]
G18	VSS[242]	VSS[342]
G20	VSS[243]	VSS[343]
G26	VSS[244]	VSS[344]
G28	VSS[245]	VSS[345]
G36	VSS[246]	VSS[346]
G48	VSS[247]	VSS[347]
H12	VSS[248]	VSS[348]
H18	VSS[249]	VSS[349]
H22	VSS[250]	VSS[350]
H24	VSS[251]	VSS[351]
H26	VSS[252]	VSS[352]
H30	VSS[253]	
H32	VSS[254]	
H34	VSS[255]	
F3	VSS[256]	
	VSS[257]	
	VSS[258]	

PANTHER-POINT_FCBGA989

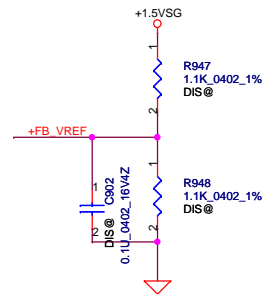
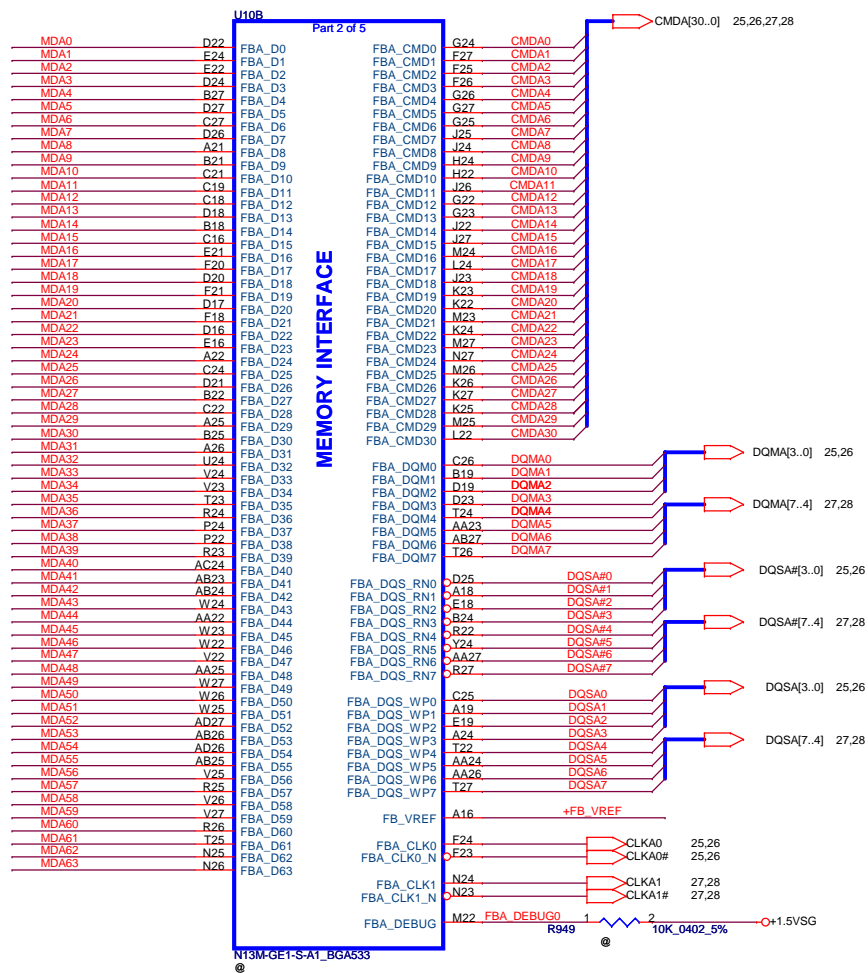
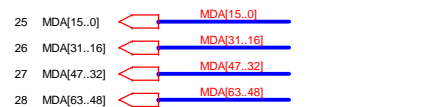
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				Date: Thursday, October 27, 2011	Rev 0.2
				Sheet 19 of 59	



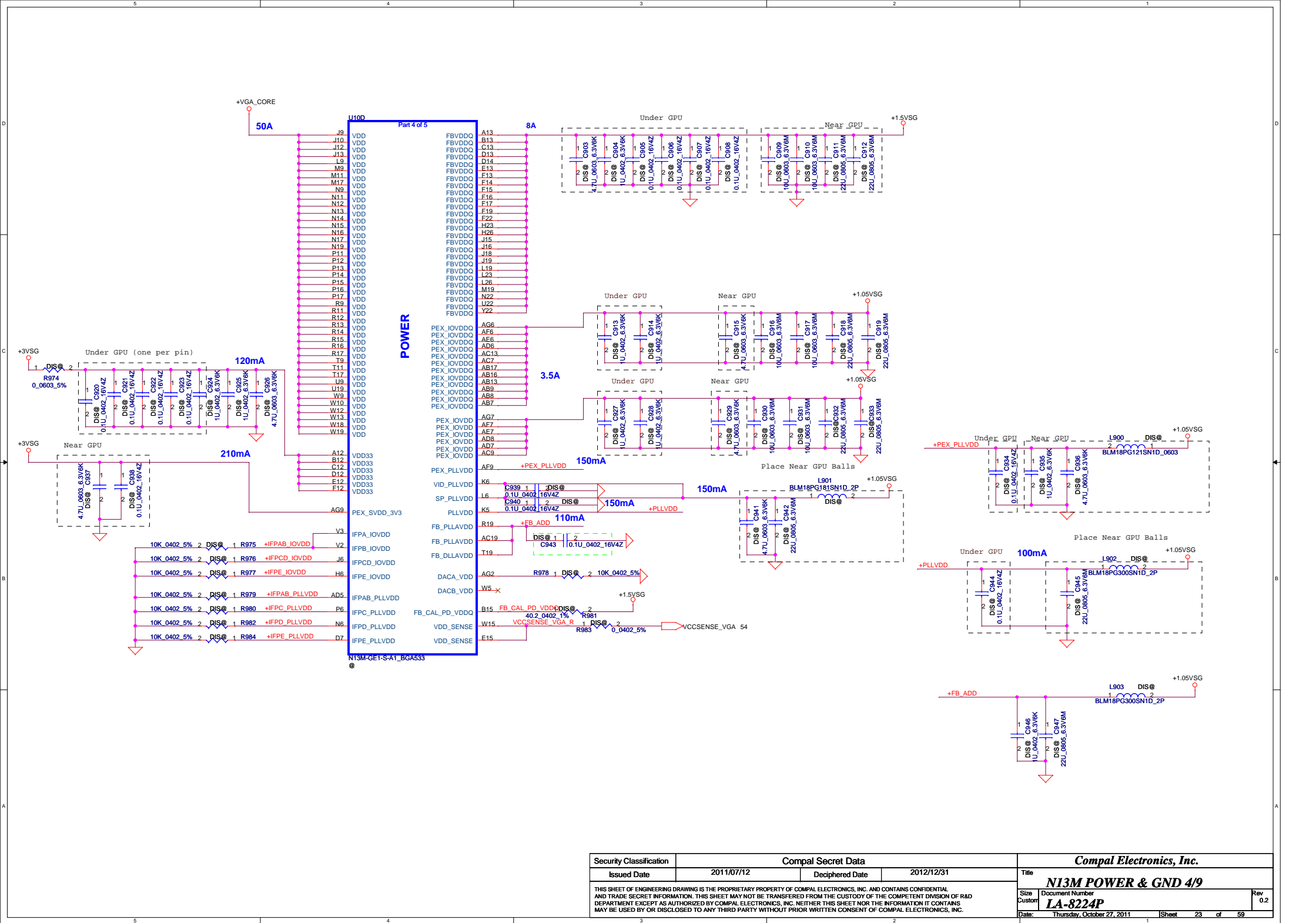
GPIO	I/O	USAGE
GPIO0	O	GPU_VID4
GPIO1	O	GPU_VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VDD
GPIO4	O	LCD_BLEN
GPIO5	O	GPU_VID1
GPIO6	O	GPU_VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT#
GPIO9	I/O	ALERT#
GPIO10	O	MEM_VREF_CTL
GPIO11	O	GPU_VID0
GPIO12	I	PWR_LEVEL
GPIO13	O	GPU_VID5
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	MEM_VDD_CTL
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved

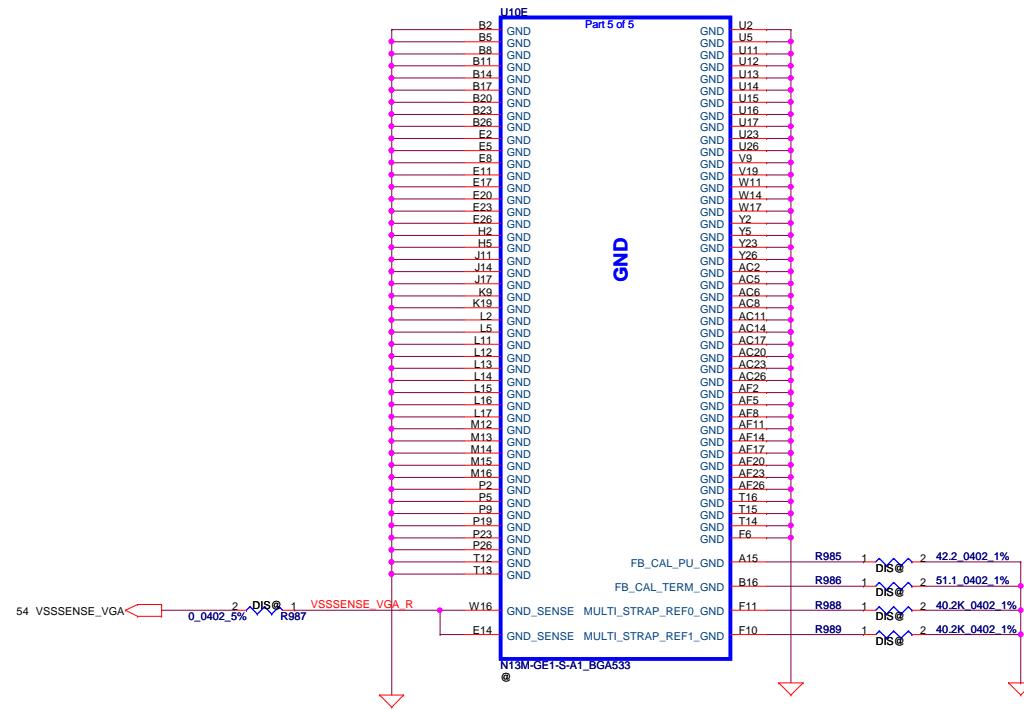


VRAM Interface



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				Size Custom	Document Number
				LA-8224P	
Date:				Thursday, October 27, 2011	Sheet 21 of 59

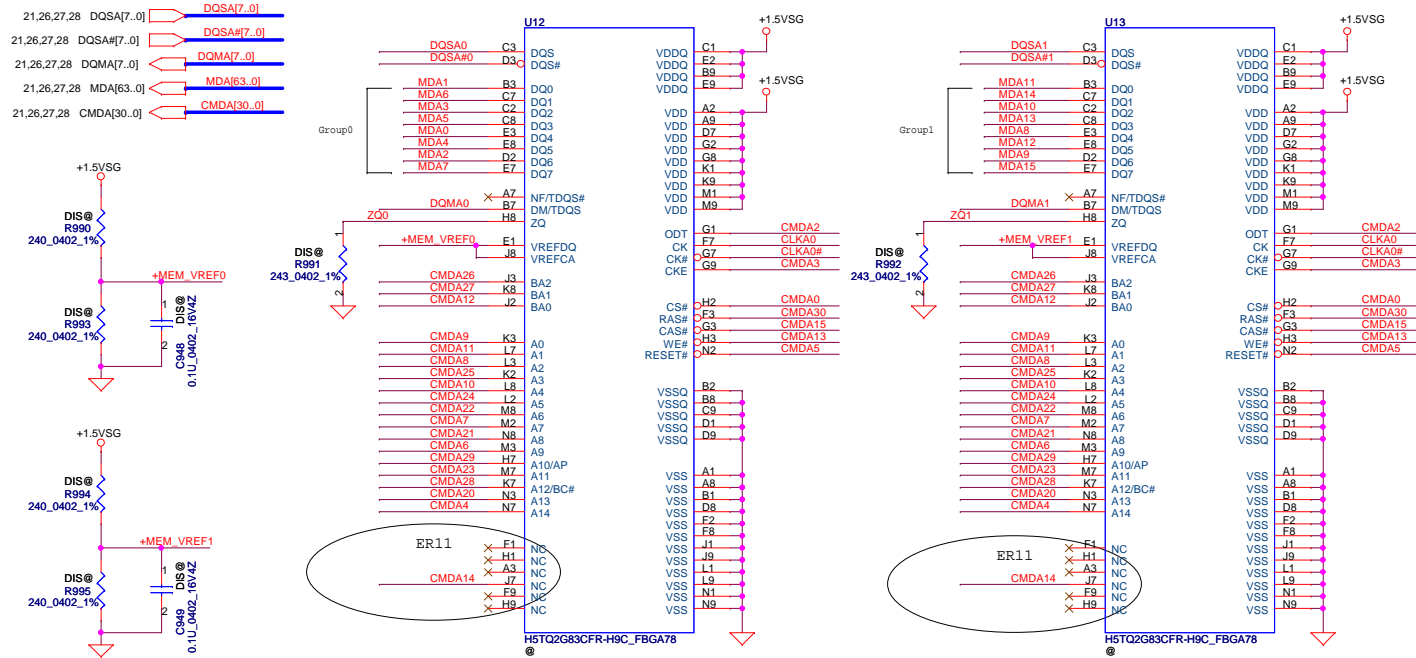




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				Size	Rev
				Custom	0.2
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VRAM DDR3 chips

256Mx8 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

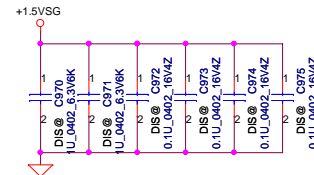
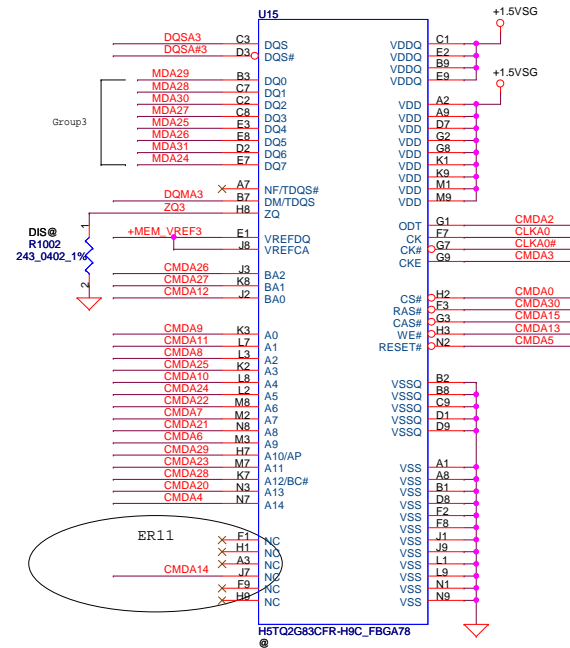
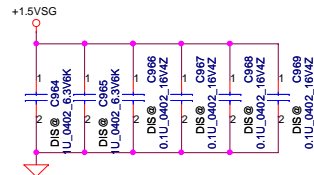
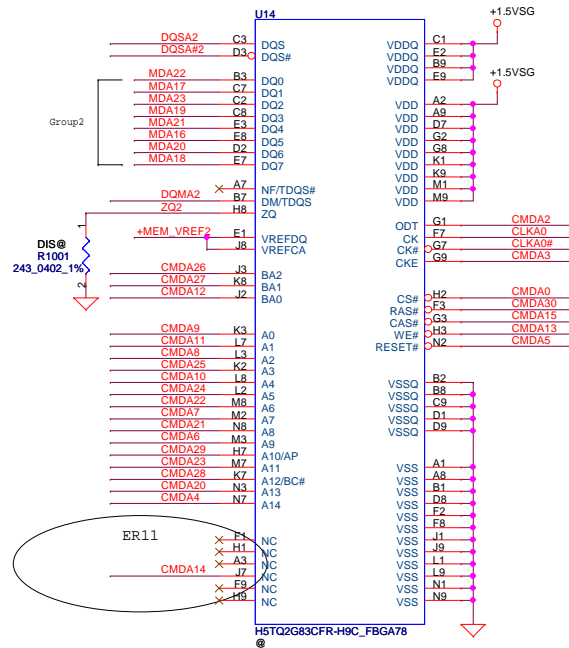
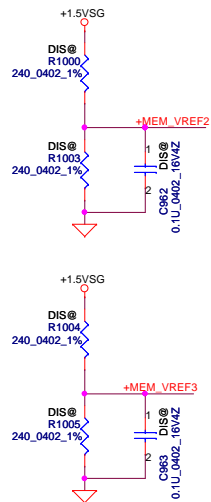
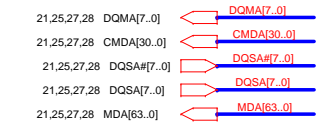
Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CS*	No Termination

Hynix : SA000054600 (S IC D3 256MX8/1333 H5TQ2G83CFR-H9C FBGA)
Elpida : SAxxxxxxx (S IC D3 256MX8/1333 xxxxxxxxxxxxxxxxx)

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Hynix : SA000054600 (S IC D3 256MX8/1333 H5TQ2G83CFR-H9C FBGA) Elpida : SAxxxxxxx (S IC D3 256MX8/1333 xxxxxxxxxxxxxxxxx)				
Compal Electronics, Inc.				
N13M DDR3 6/9				
Size	Document Number	Rev		
Custom	LA-8224P	0.2		
Date:	Thursday, October 27, 2011	Sheet	25	of 59

VRAM DDR3 chips

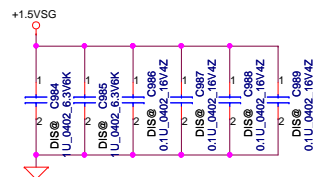
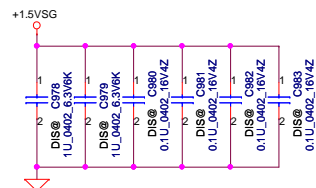
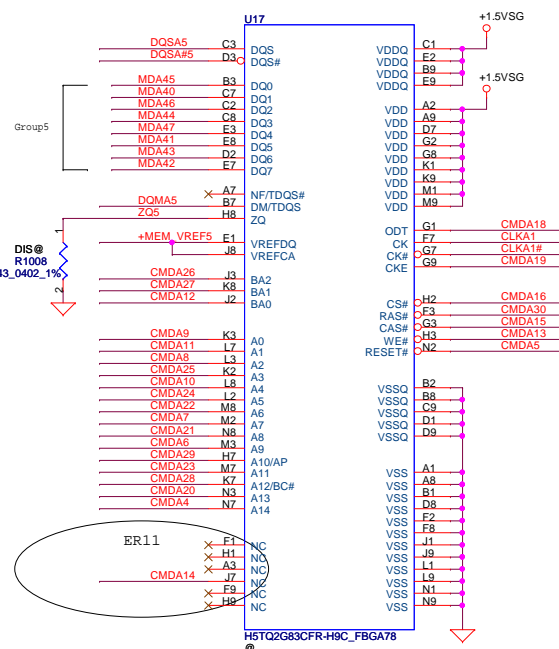
256Mx8 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
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				Customer LA-8224P		
				Date:	Thursday, October 27, 2011	Sheet 26 of 59

256Mx8 DDR3 *8==>2GB



LOW	HIGH
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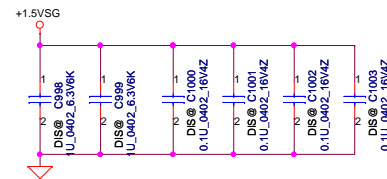
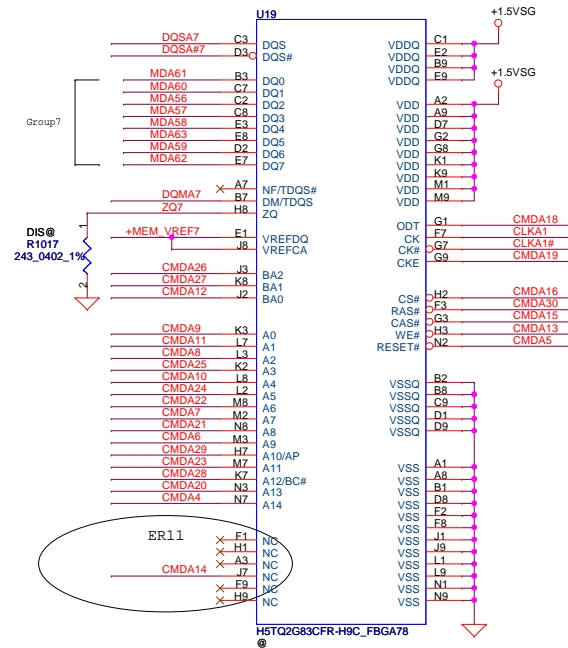
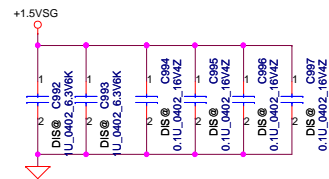
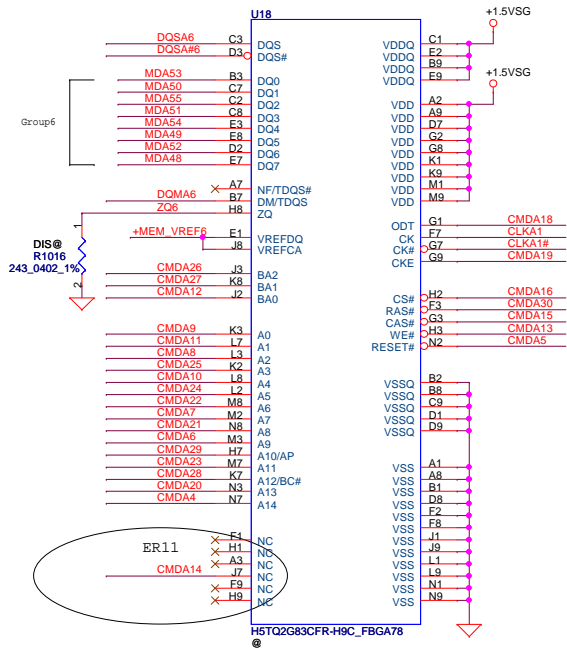
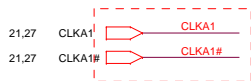
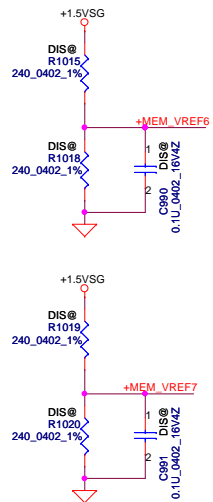
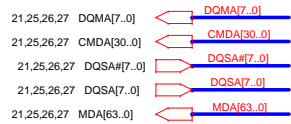
		DIS@			
CMDA18	R1013	1	2	10K	0402 5%
CMDA19	R1014	1	2	10K	0402 5%

Hynix : SA000054600 (S IC D3 256MX8/1333 H5TQ2G83CFR-H9C FBGA)
Elpida : SAxxxxxxxxx (S IC D3 256MX8/1333 xxxxxxxxxxxxxxxxx)

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				Date:	Thursday, October 27, 2011	Sheet 27 of 59

VRAM DDR3 chips

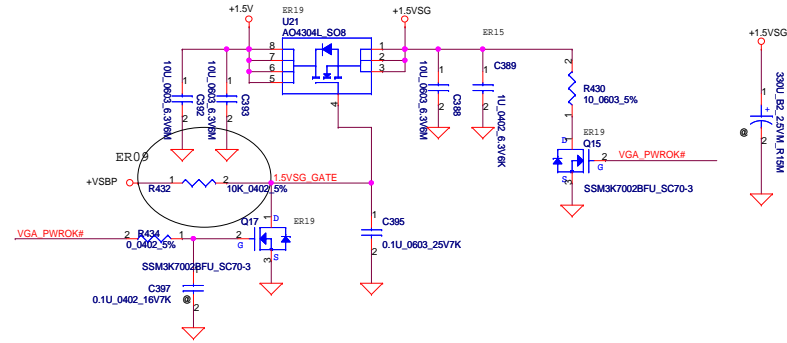
256Mx8 DDR3 *8==>2GB



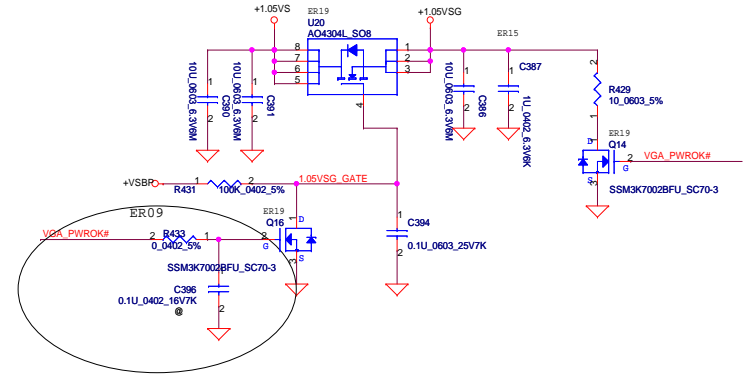
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
LOW		HIGH

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				LA-8224P		
				Date:	Thursday, October 27, 2011	Sheet 26 of 59

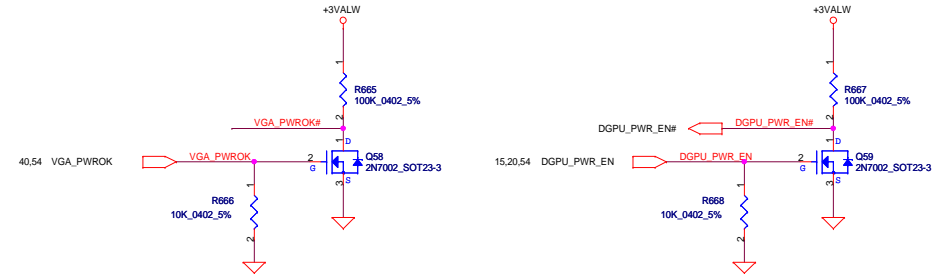
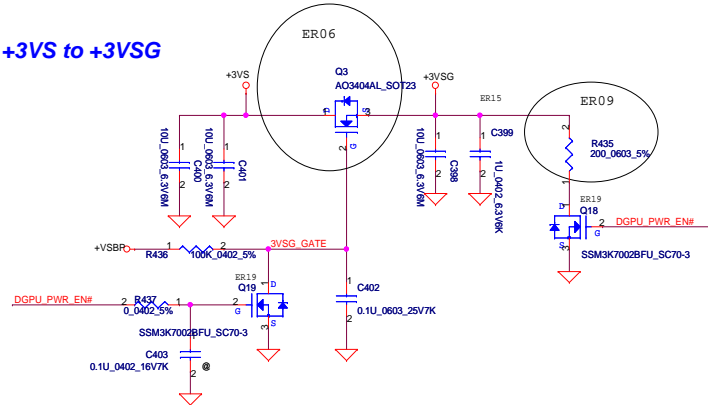
+1.5V to +1.5VSG



+VCCP to +1.05VSG



+3VS to +3VSG

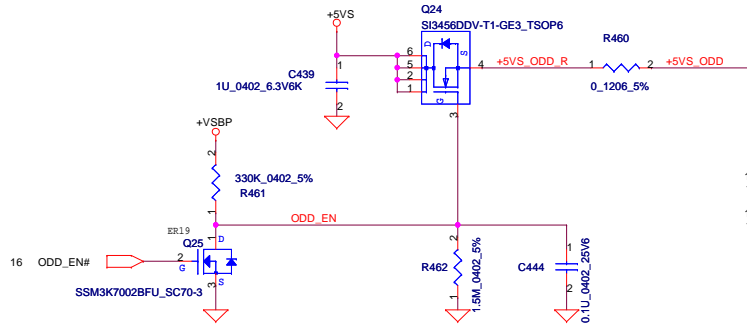
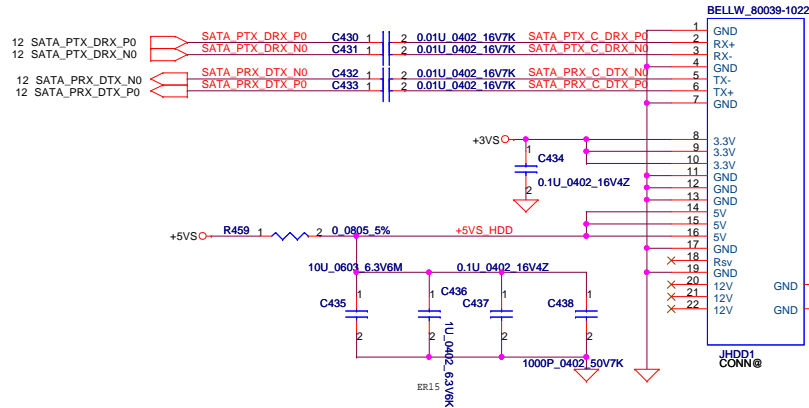


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Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title	
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Size	Custom	Document Number	LA-8224P	Rev	02
Date	Thursday, October 27, 2011	Sheet	29	of	59

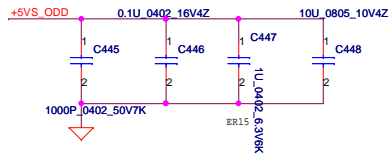
[illegible]

Security Classification		Compal Secret Data		Compal Electronics, Inc. Title LVDS/CRT CONN	
Issued Date	2011/07/12	Deciphered Date	2012/12/31	Size C	Document Number LA-8224P
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				Date:	Thursday, October 27, 2011 Sheet 30 of 59

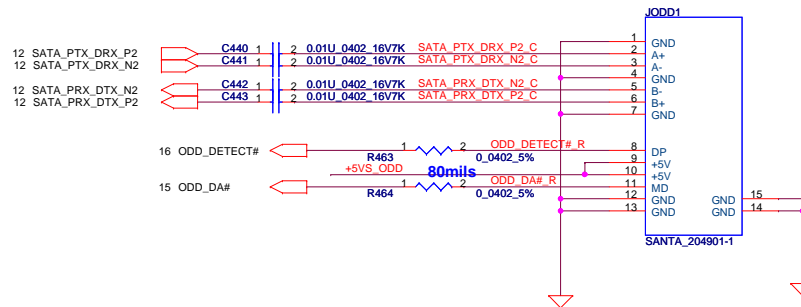
SATA HDD Conn.



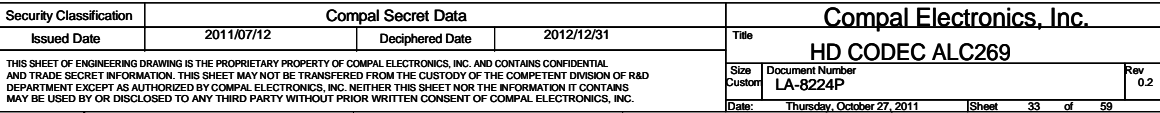
Placea caps. near ODD CONN.

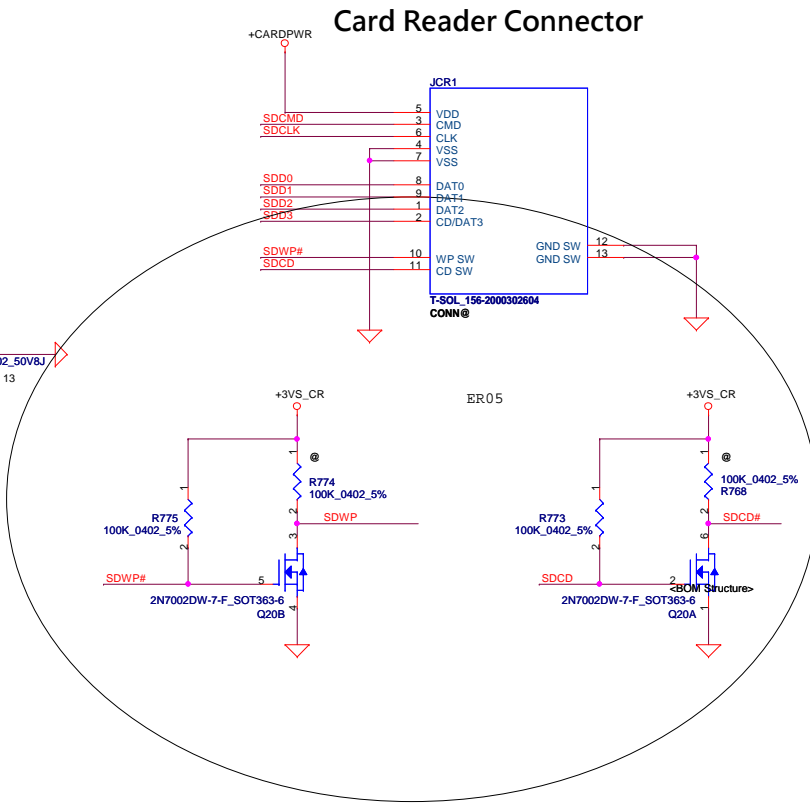
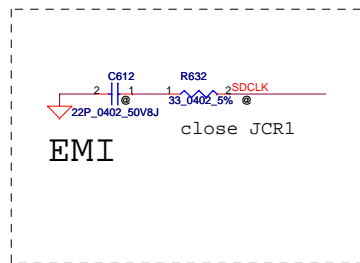
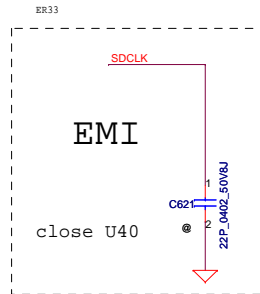
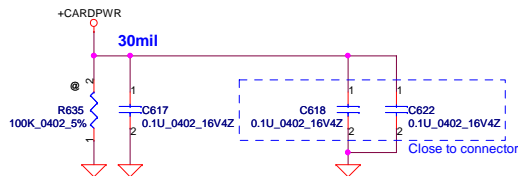
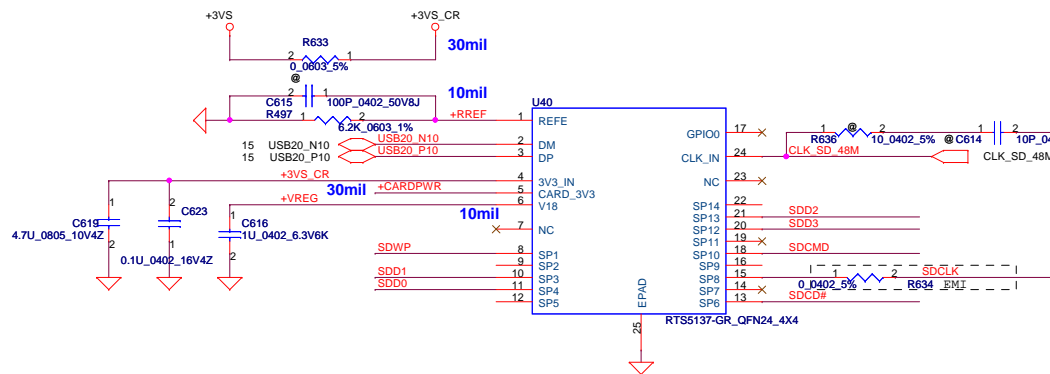


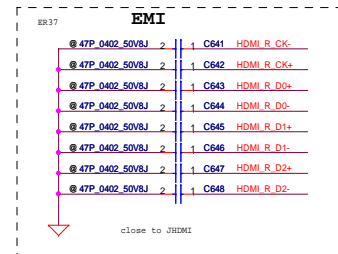
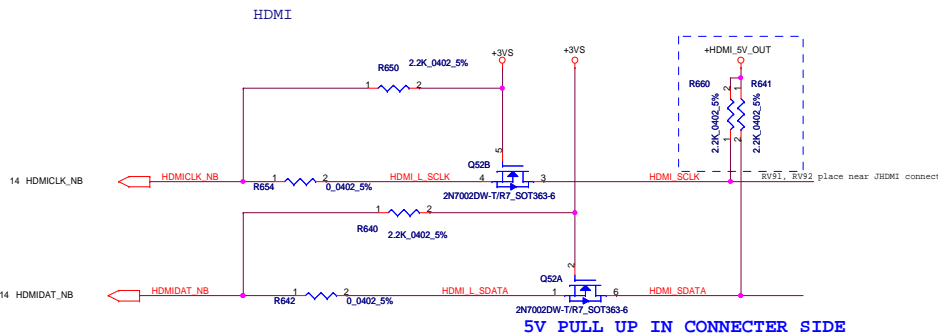
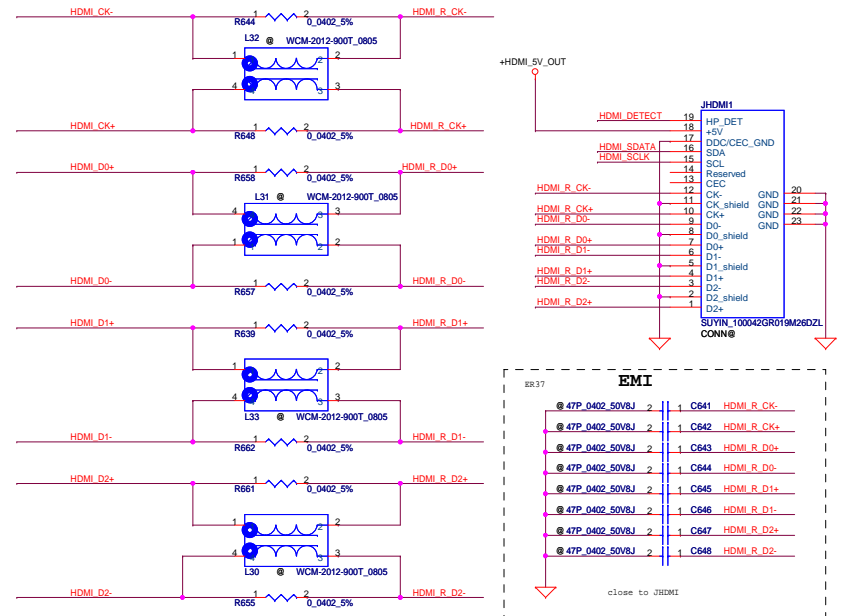
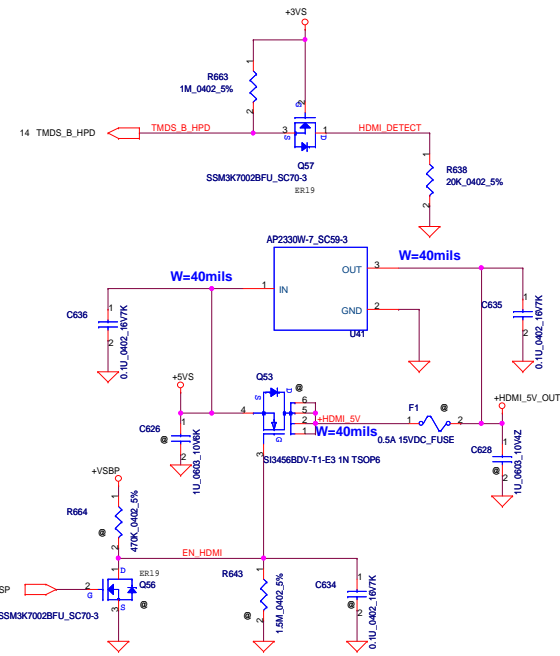
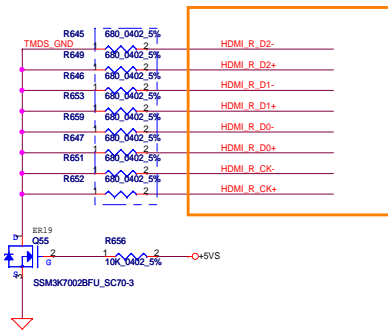
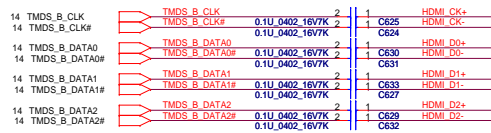
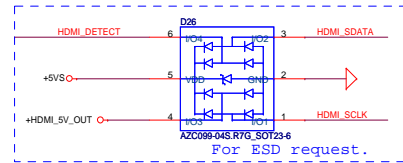
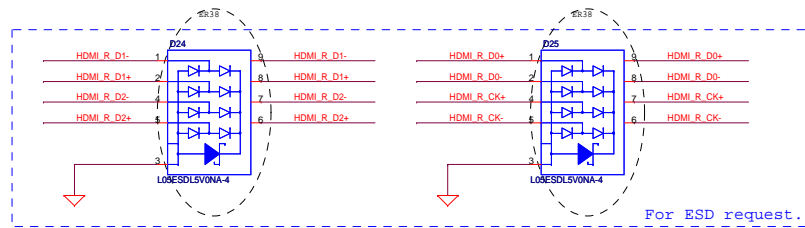
SATA ODD Conn.



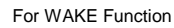
Security Classification		Compal Secret Data		Compal Electronics, Inc.				
Issued Date		2011/07/12		Deciphered Date		2012/12/31		
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				HDD & ODD CONN				
				Size B	Document Number LA-8224P			Rev 0.2
				Date: Thursday, October 27, 2011				Sheet 31 of 59







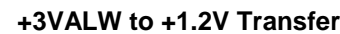
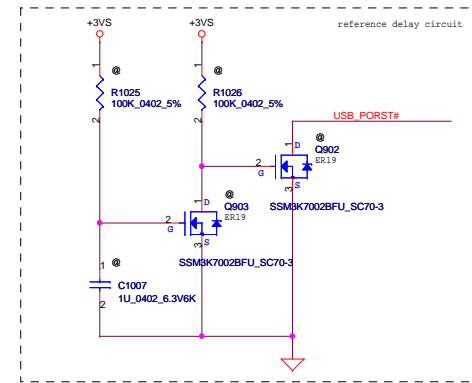
Power Sequence



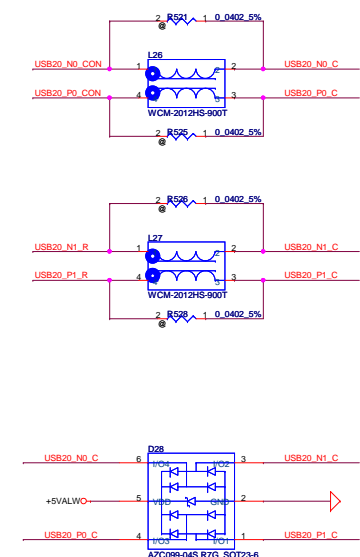
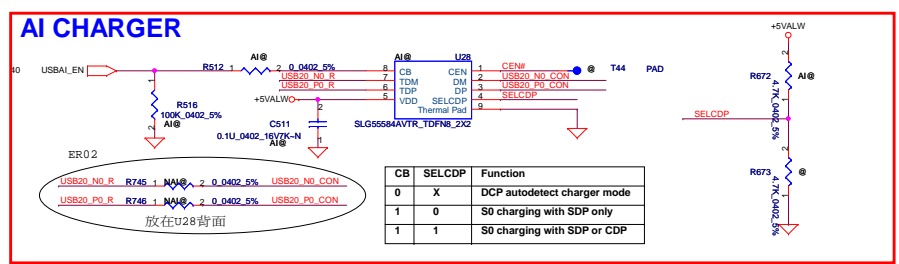
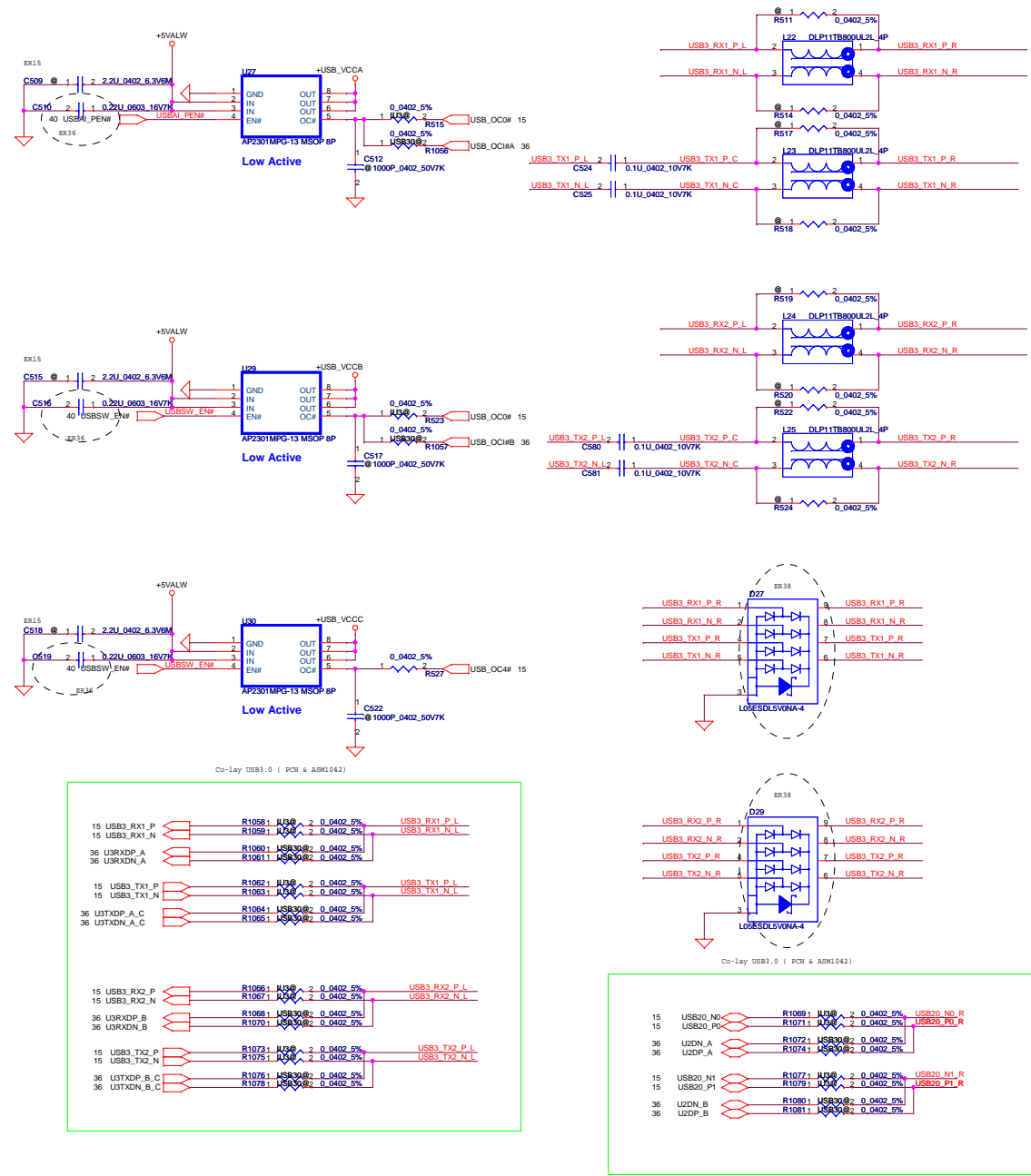
USB_PEPWRDET

USB_PESSEL

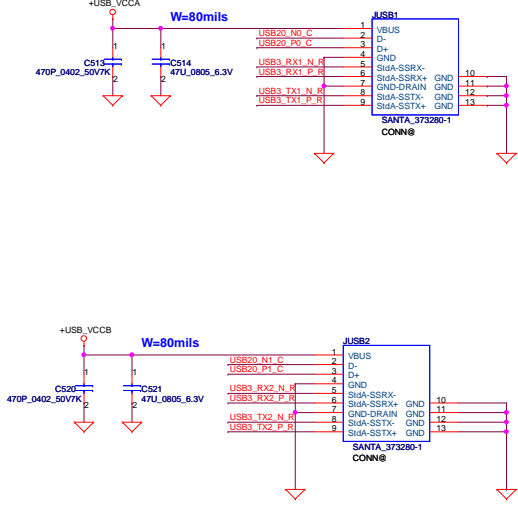
* Other applaction	@
Express Card/Mini Card	Mount



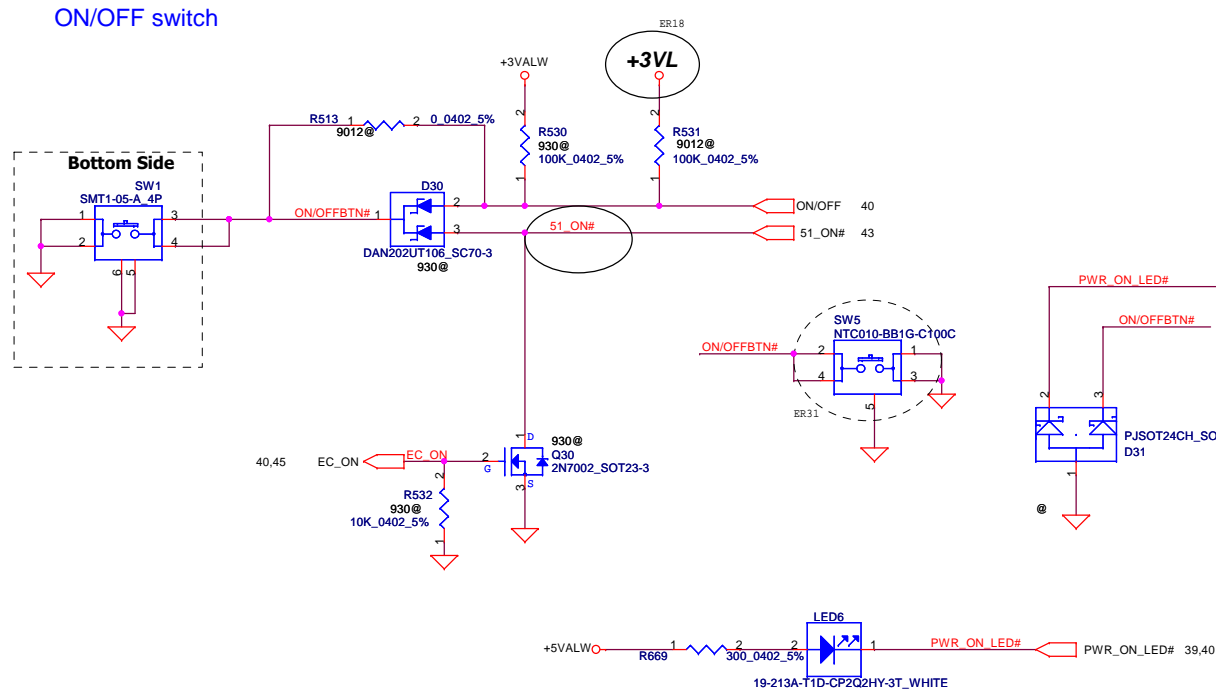
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2010/10/1	Deciphered Date	2012/06/30	Title USB3.0 controller		
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				Custom	LA-8224P	0.2
Date:				Thursday	October 27, 2011	Sheet 36 of 50



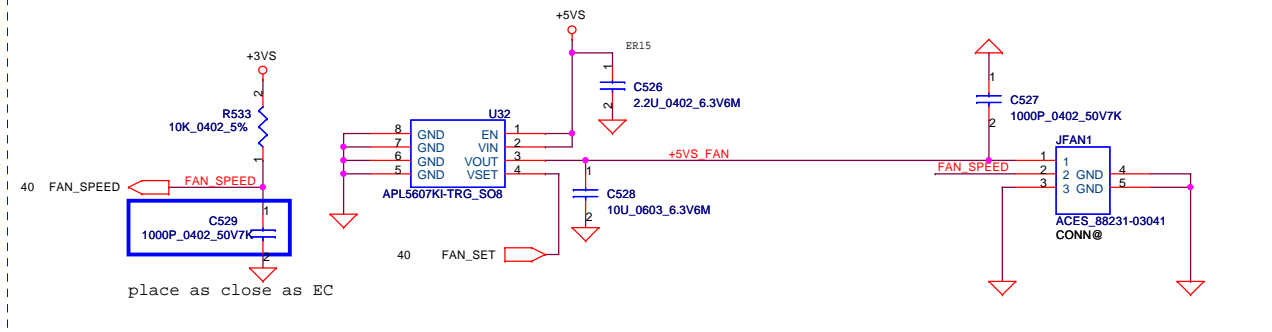
charger port: left side & near user



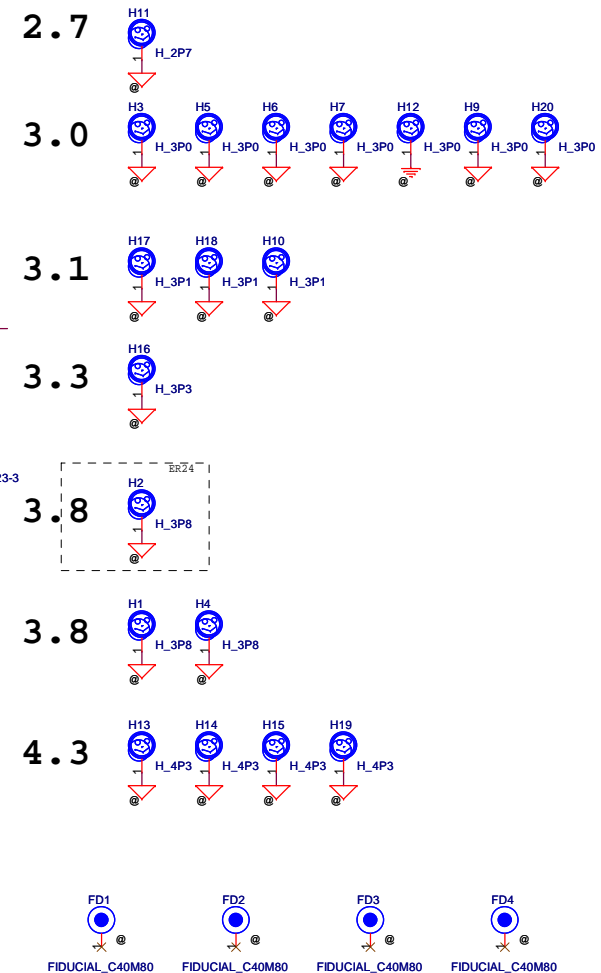
Power Button



Fan Control Circuit

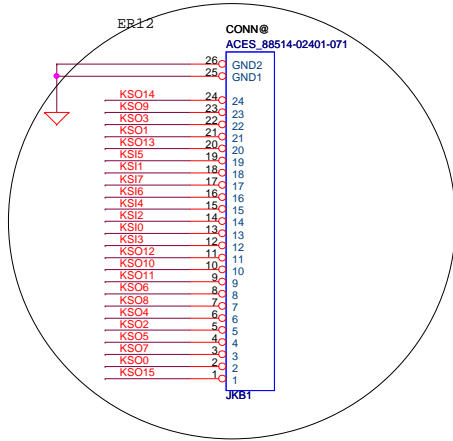
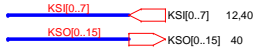
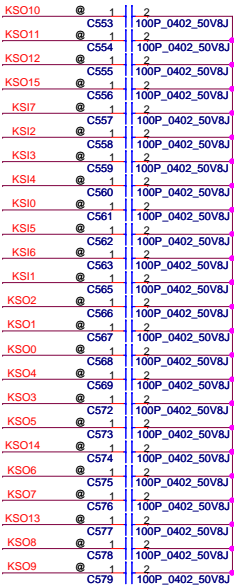


Screw Hole

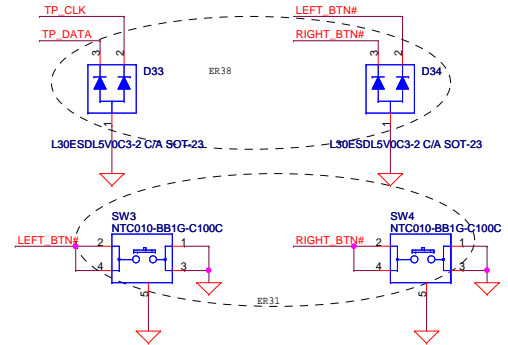
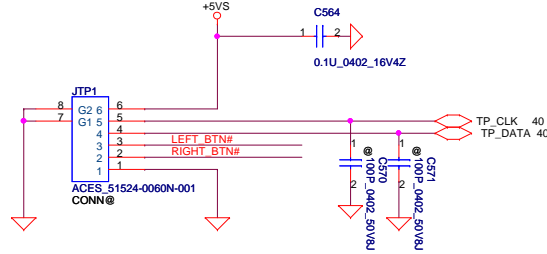


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Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title	
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				Custord	0.2
				LA-8224P Date: Thursday, October 27, 2011 Sheet 38 of 59	

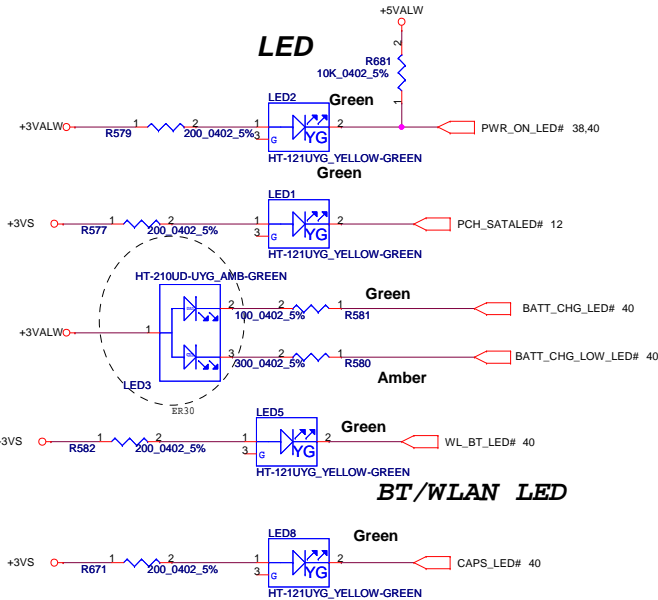
INT_KBD Conn.



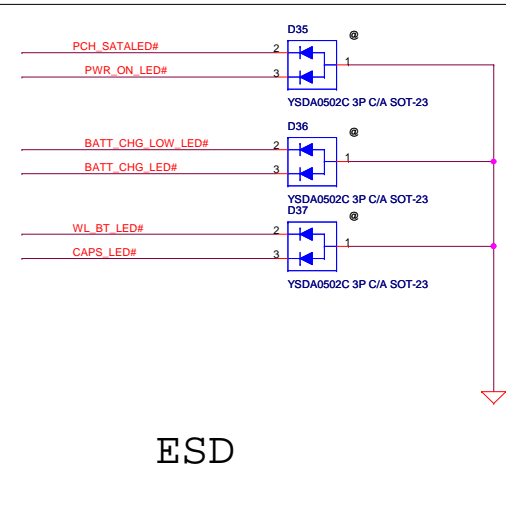
Touch/B Connector



LED



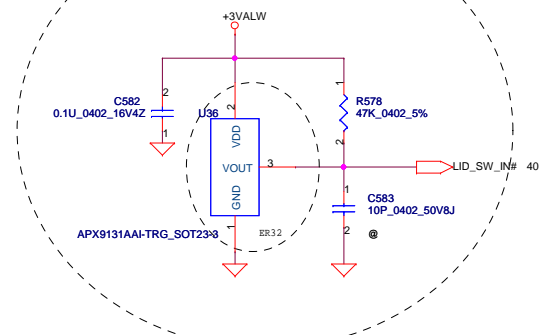
BT/WLAN LED



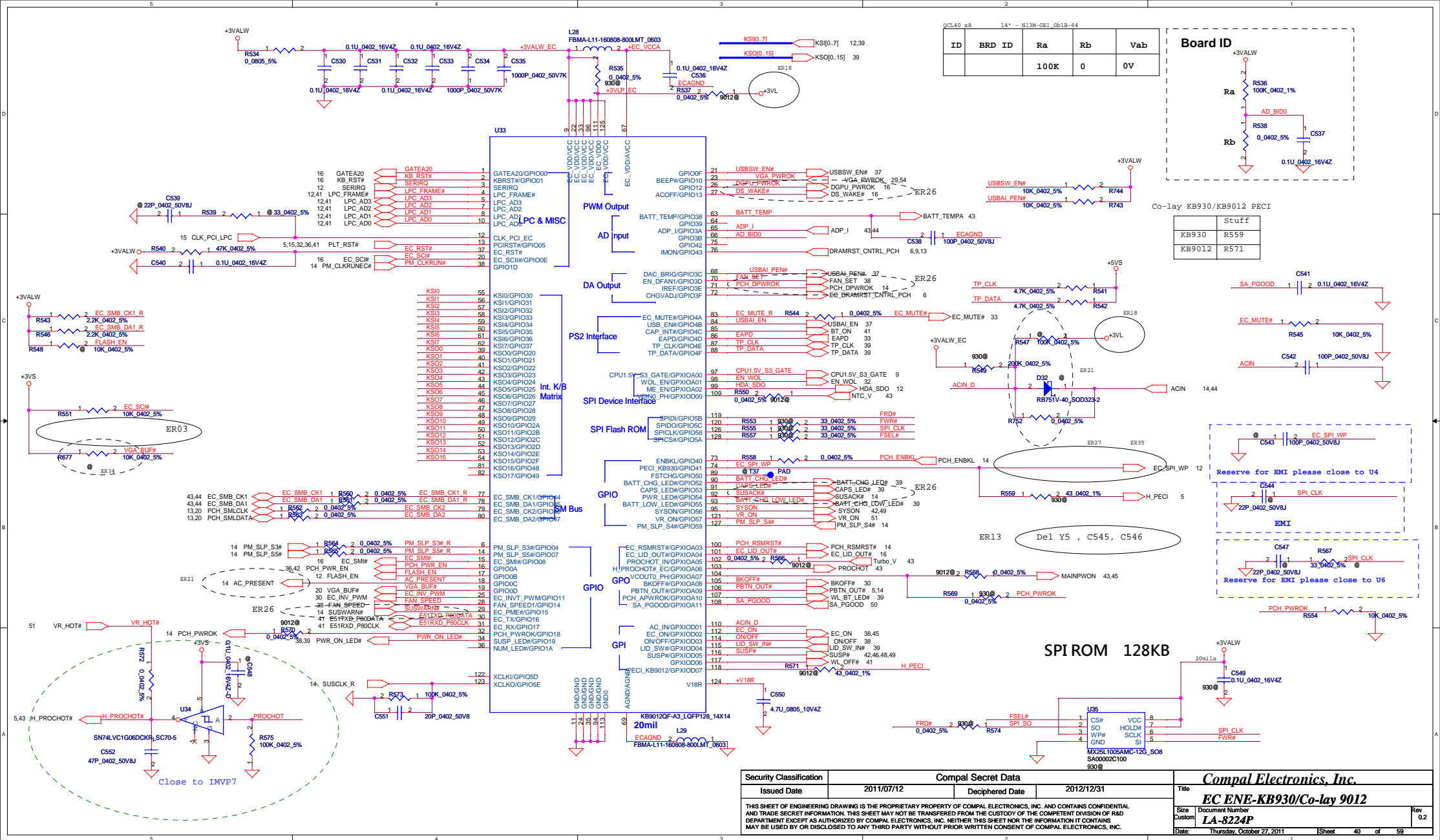
ESD

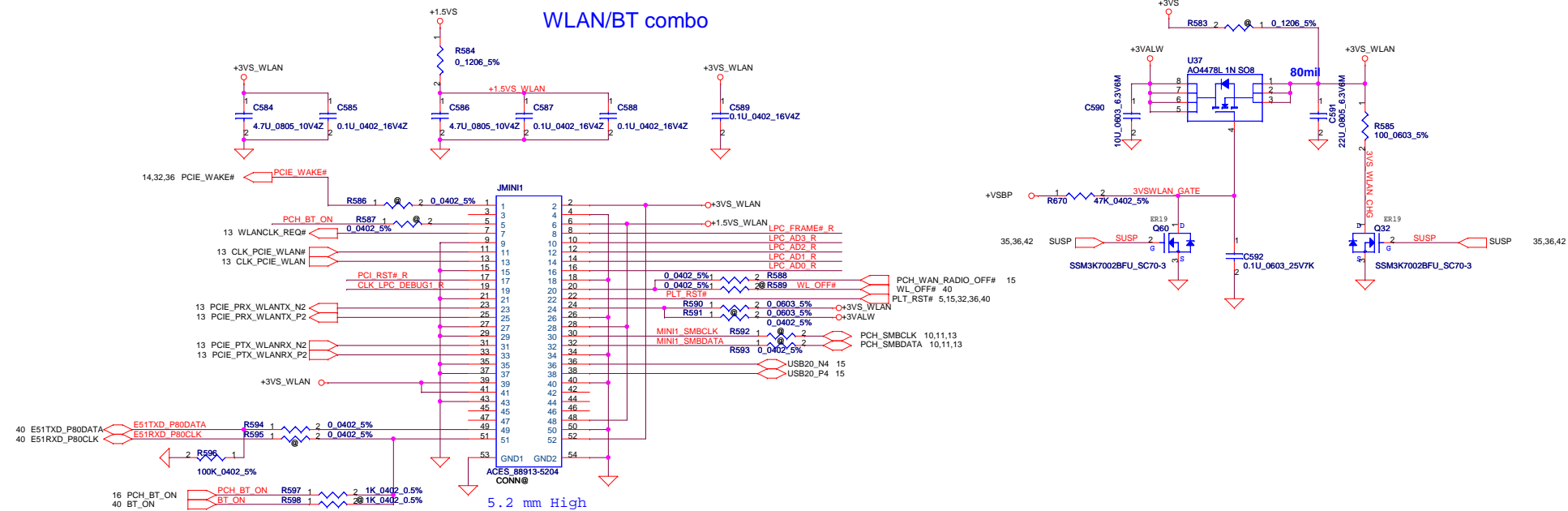
Lid Switch

(Hall Effect Switch)



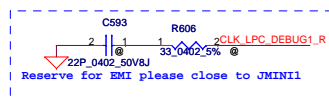
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title	KB/EC ROM/TP/FUN/LED
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				Rev	0.2





Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

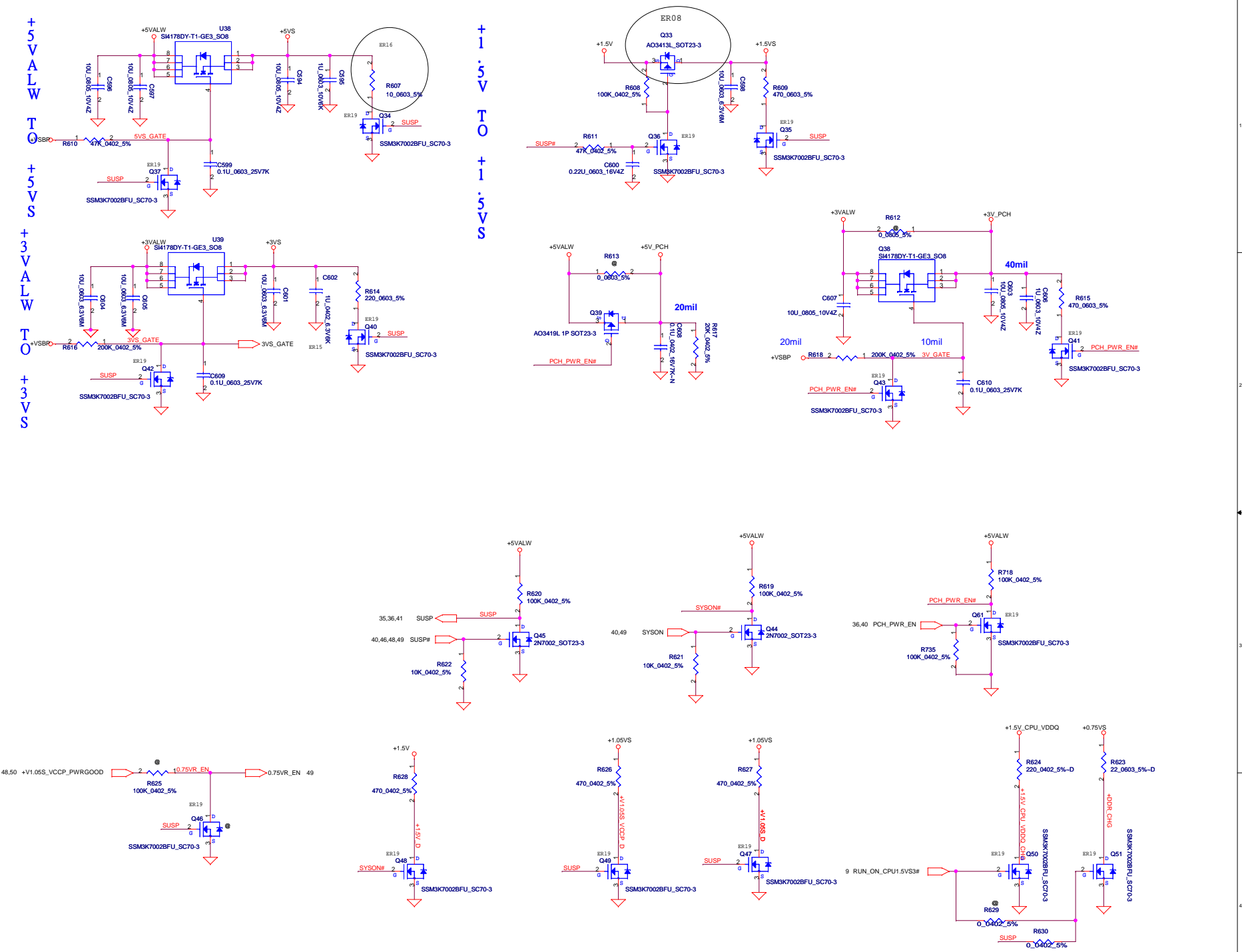
LPC_FRAME#_R	R599	1	2	0.0402 5%	LPC_FRAME#	LPC_FRAME#	12,40
LPC_AD3_R	R600	1	2	0.0402 5%	LPC_AD3	LPC_AD3	12,40
LPC_AD2_R	R601	1	2	0.0402 5%	LPC_AD2	LPC_AD2	12,40
LPC_AD1_R	R602	1	2	0.0402 5%	LPC_AD1	LPC_AD1	12,40
LPC_AD0_R	R603	1	2	0.0402 5%	LPC_AD0	LPC_AD0	12,40
PLT_RST#_R	R604	1	2	0.0402 5%	PLT_RST#	PLT_RST#	5,15,32,36,40
CLK_LPC_DEBUG1_R	R605	1	2	0.0402 5%	CLK_LPC_DEBUG1	CLK_LPC_DEBUG1	15



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				Date: Thursday, October 27, 2011	Sheet 41 of 59

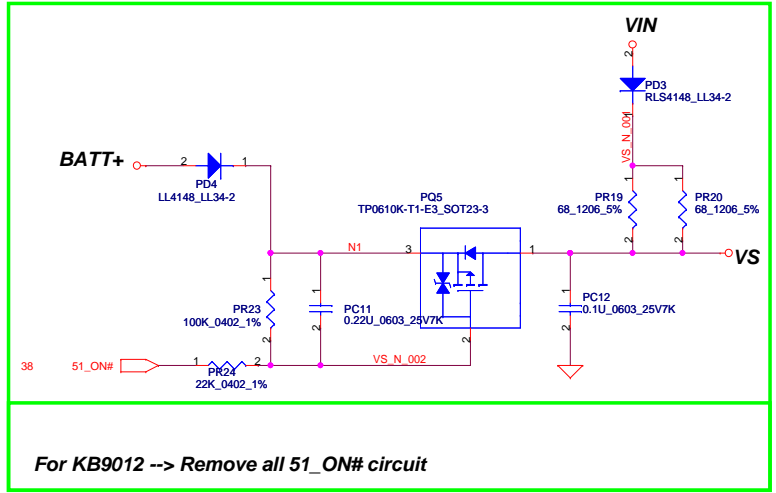
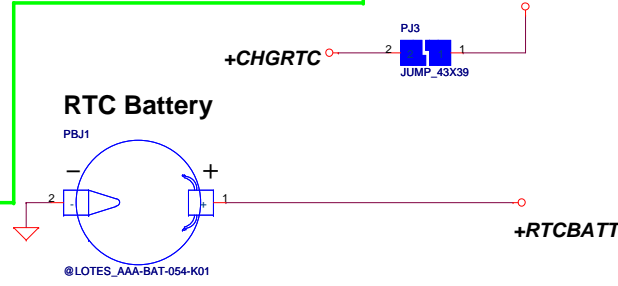
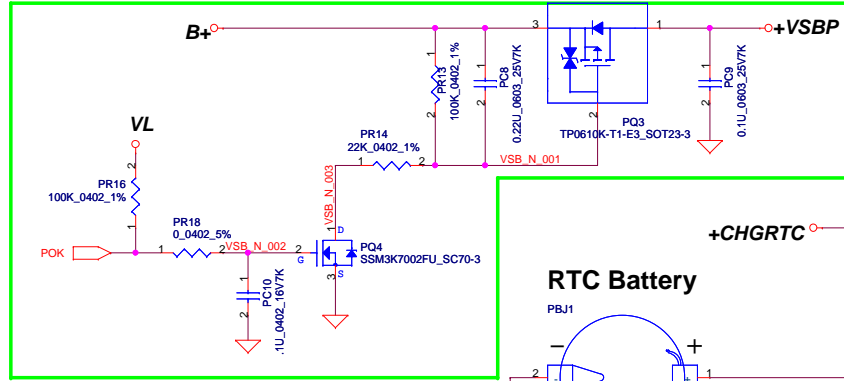
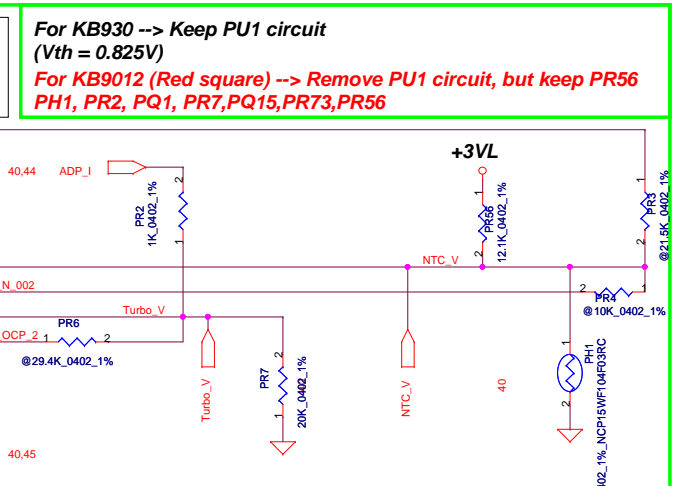
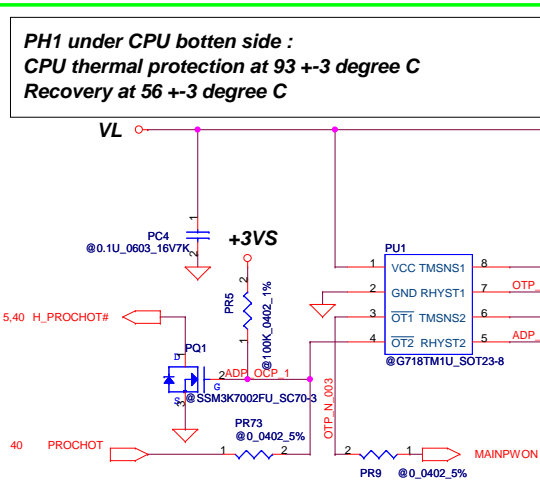
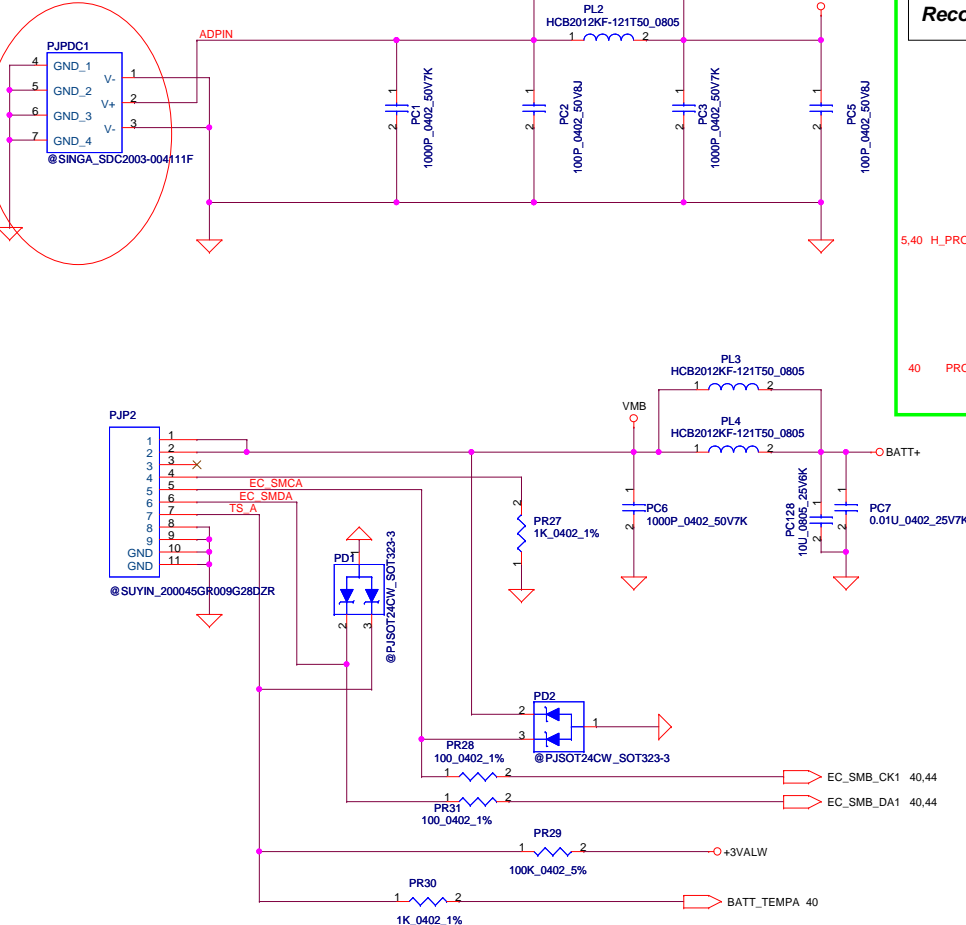
+5VALW
TO
+5VS
+3VALW
TO
+3VS

+5VALW
TO
+5VS
+3VALW
TO
+3VS



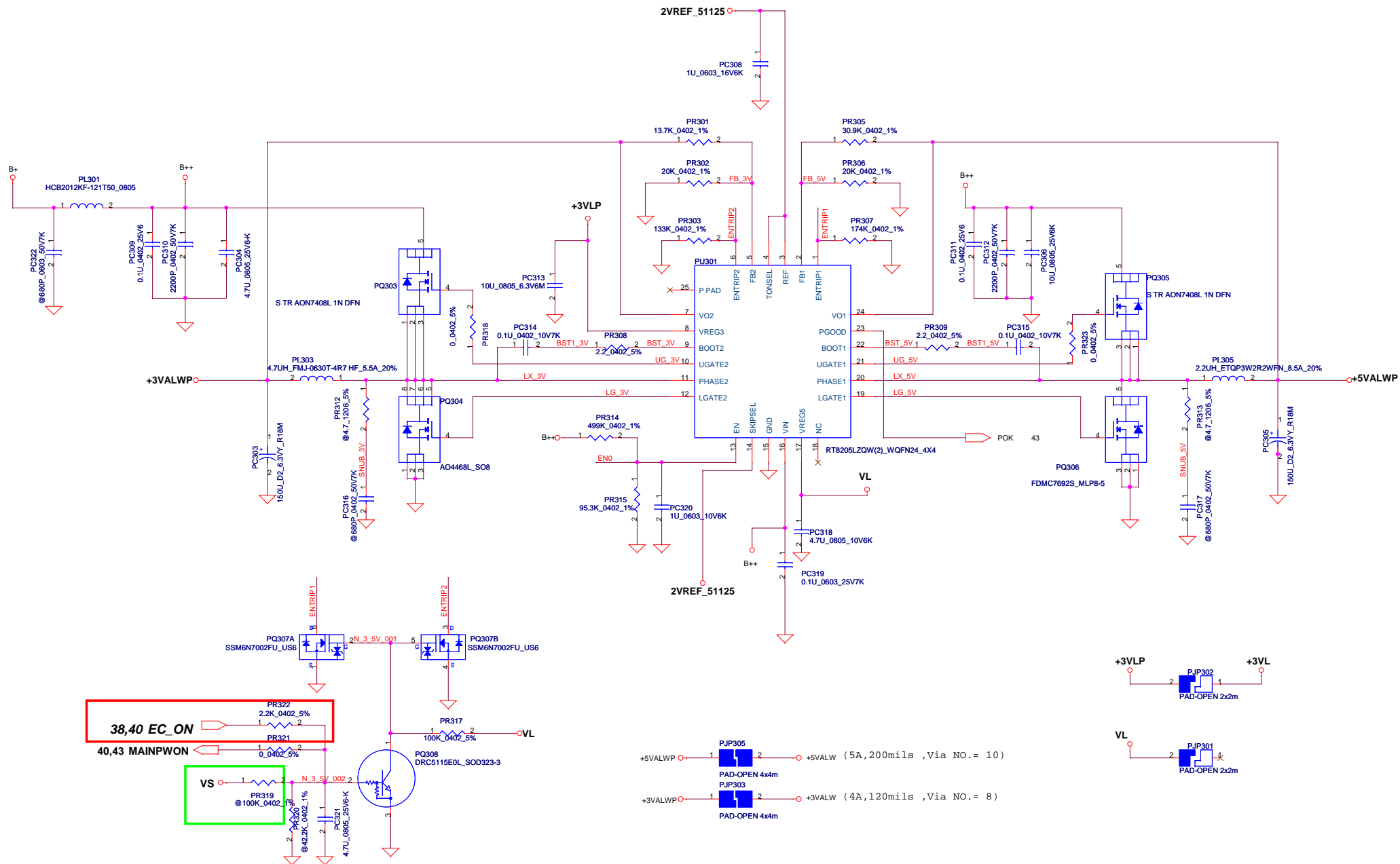
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title
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Size	Custom	Document Number	LA-8224P	Rev 0.2
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DCIN jack P/N:DC301008L00,
need doble confirm P/N with ME



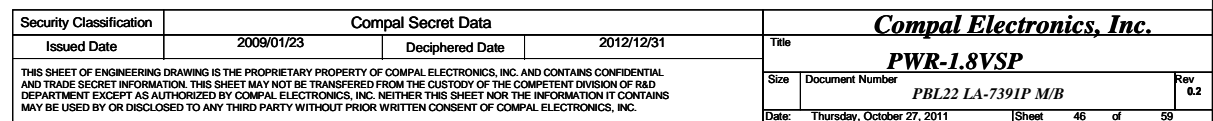
For KB9012 --> Remove all 51_ON# circuit

Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2009/01/23		Deciphered Date		2010/01/23		Title			
								PWR-DCIN / BATT CONN / OTP			
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For KB930 --> Keep PR319, Remove PR322
 For KB9012 (Red square) --> Remove PR319
 Keep PR322

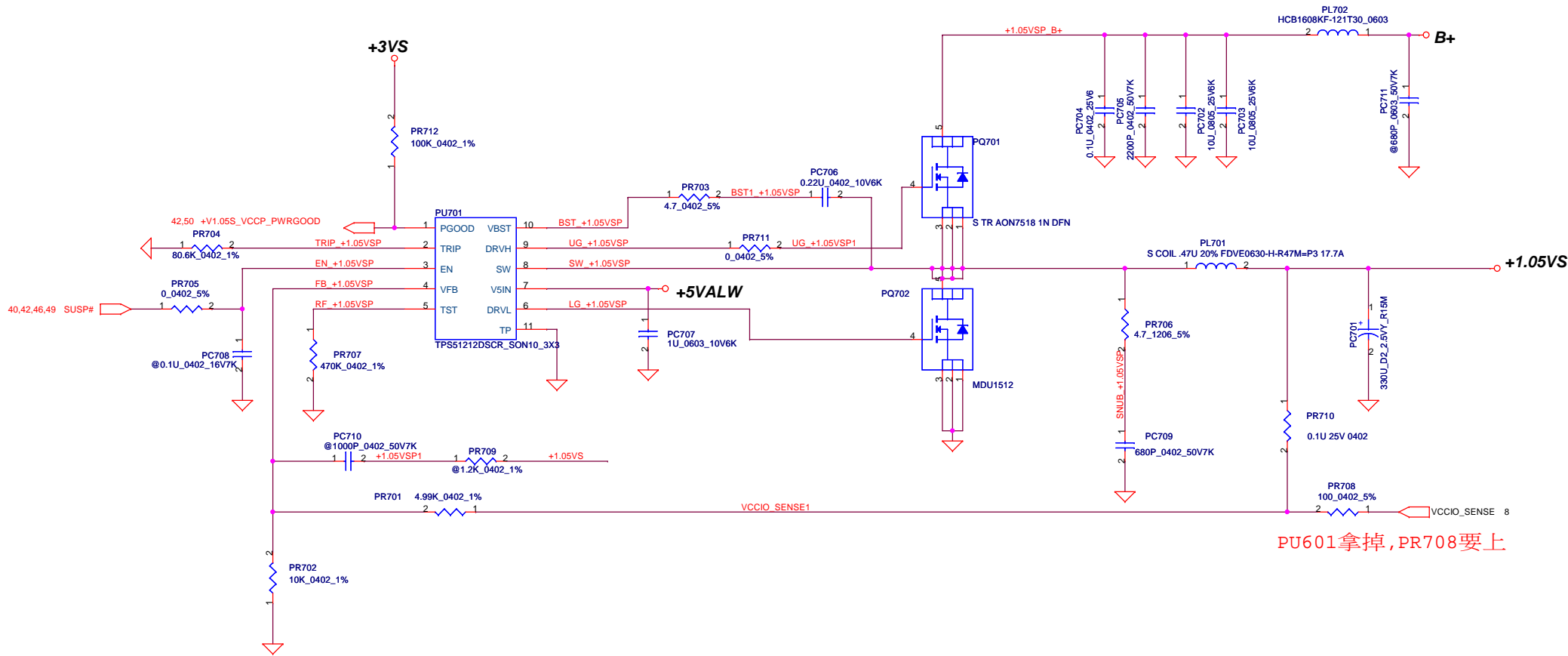
Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	Compal Electronics, Inc.	
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				Custort	LA-8224P
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				Sheet	45 of 59



(8.5A,360mils ,Via NO.= 17)

PJP606,PJP607先斷開,確定拿掉PU605再接上

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/20	Deciphered Date	2012/12/31	Title	PWR-V1.05S VCCP
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				Custom	PBL22 LA-7391P M/B
				Date:	Thursday, October 27, 2011
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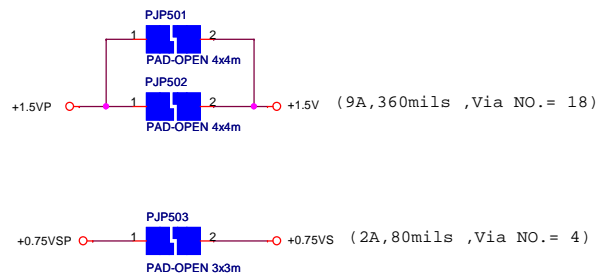


(12A,480mils ,Via NO.= 24)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/20	Deciphered Date	2012/12/31	Title	
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Size		Document Number		Rev	
Custom		PBL22 LA-7391P M/B		0.2	
Date:		Thursday, October 27, 2011		Sheet 48 of 59	

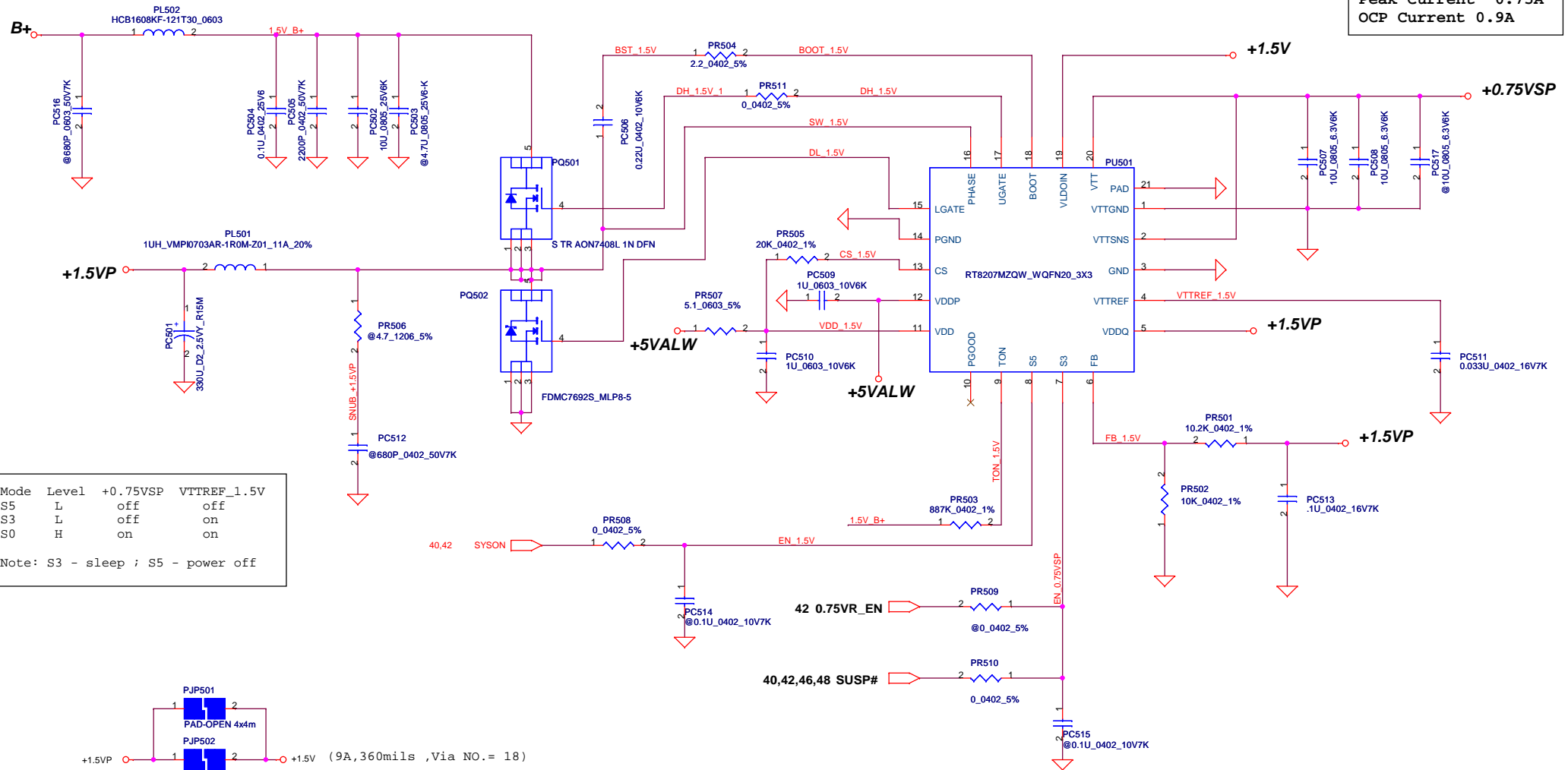
Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off



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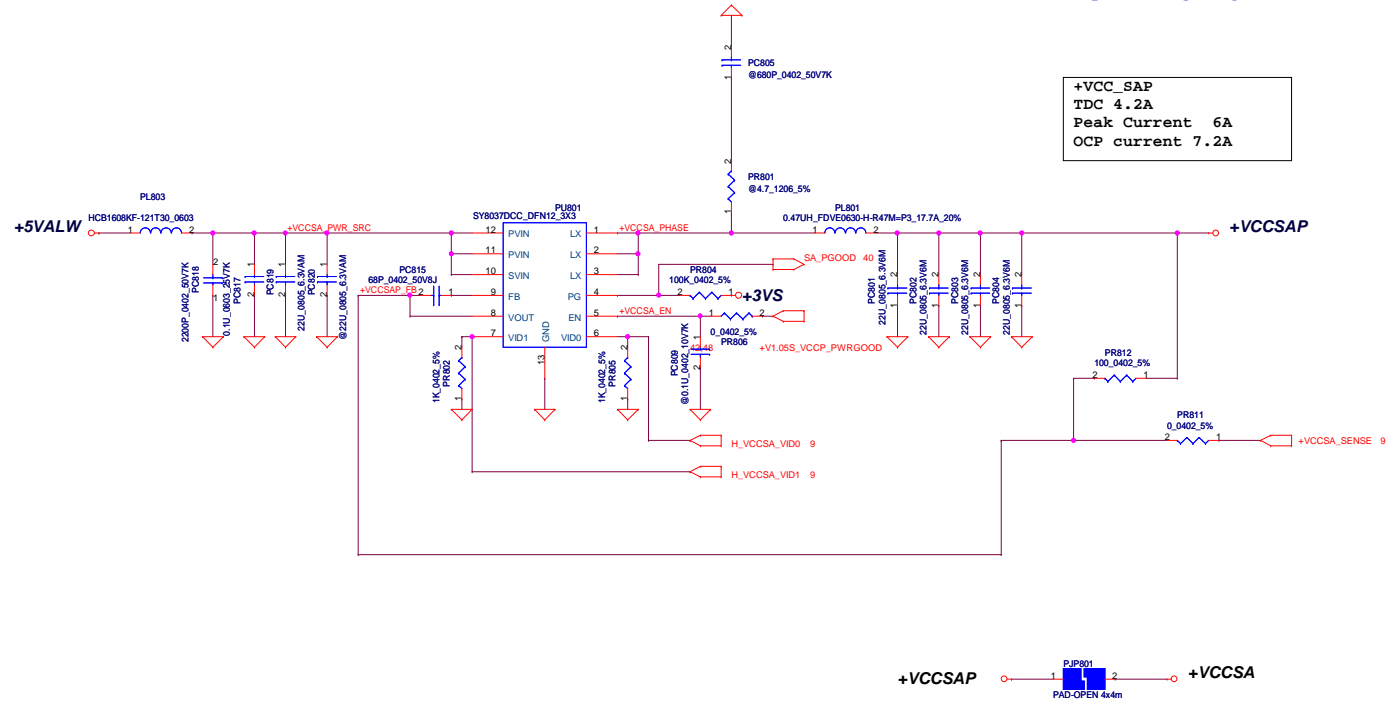
0.75Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A



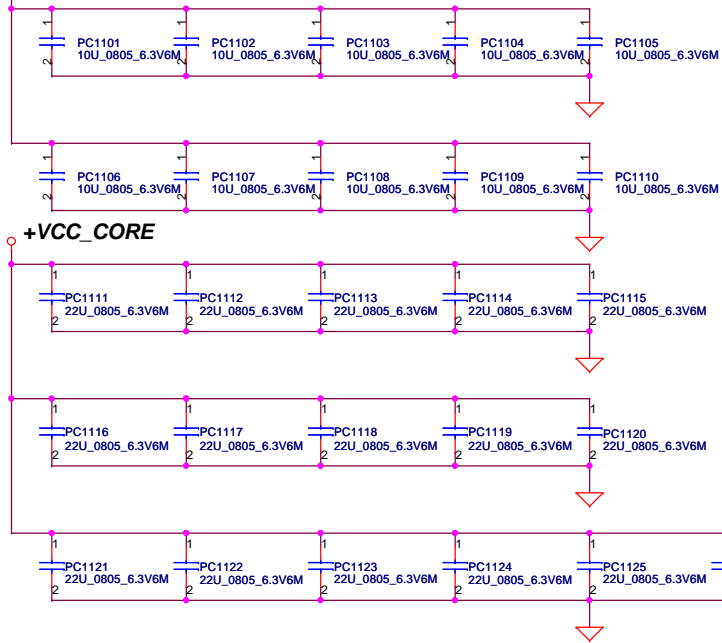
The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network



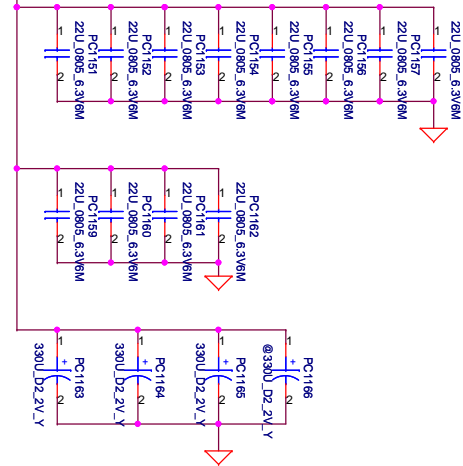
+VCC_CORE



+VCC_CORE

+VCC_GFXCORE_AXG

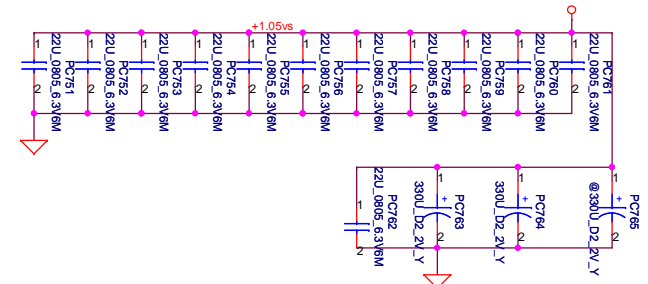
+VCC_GFXCORE_AXG



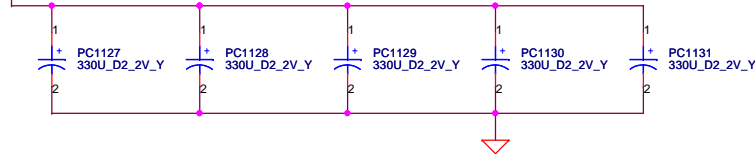
Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+1.05vs

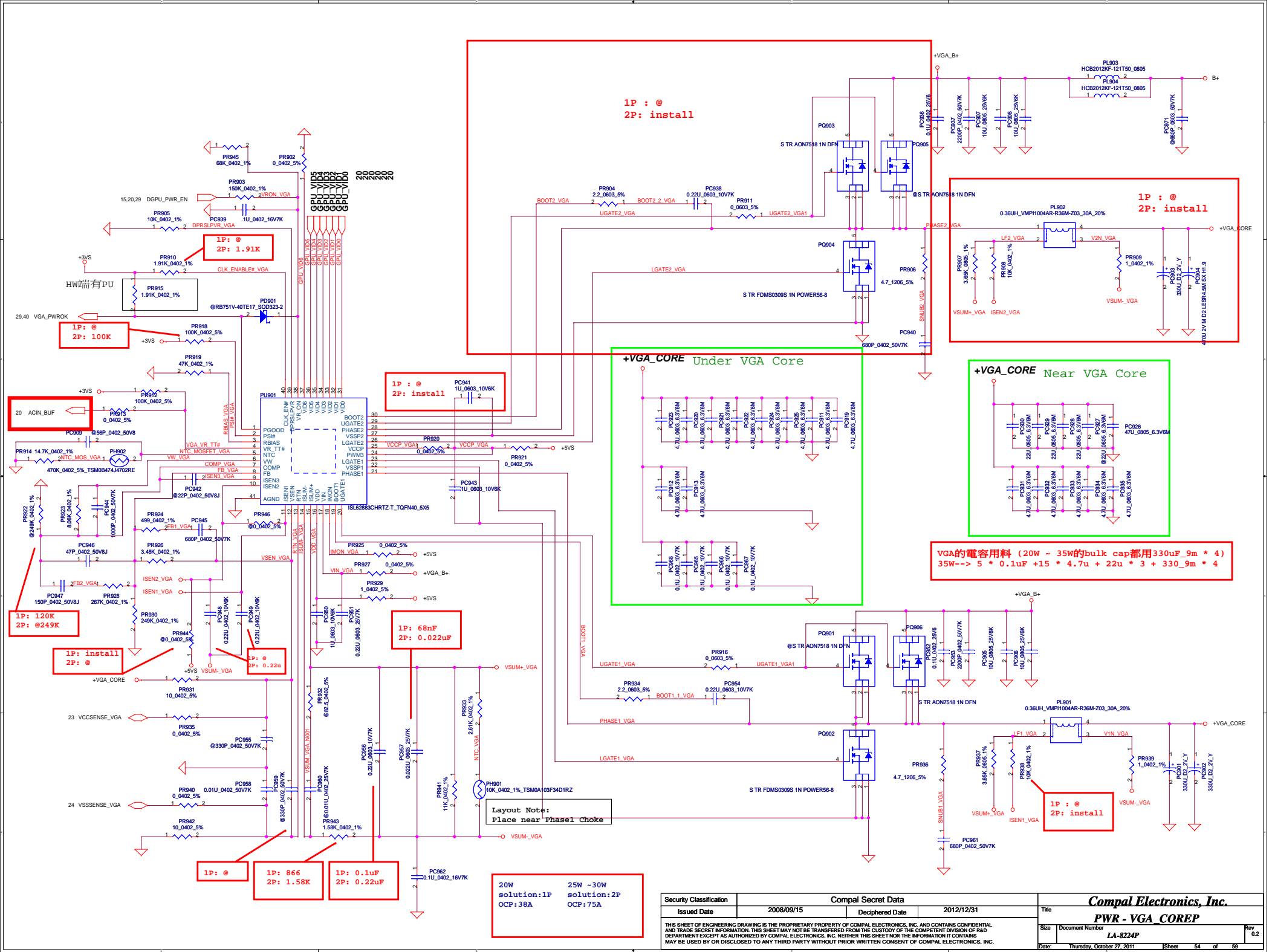


+VCC_CORE



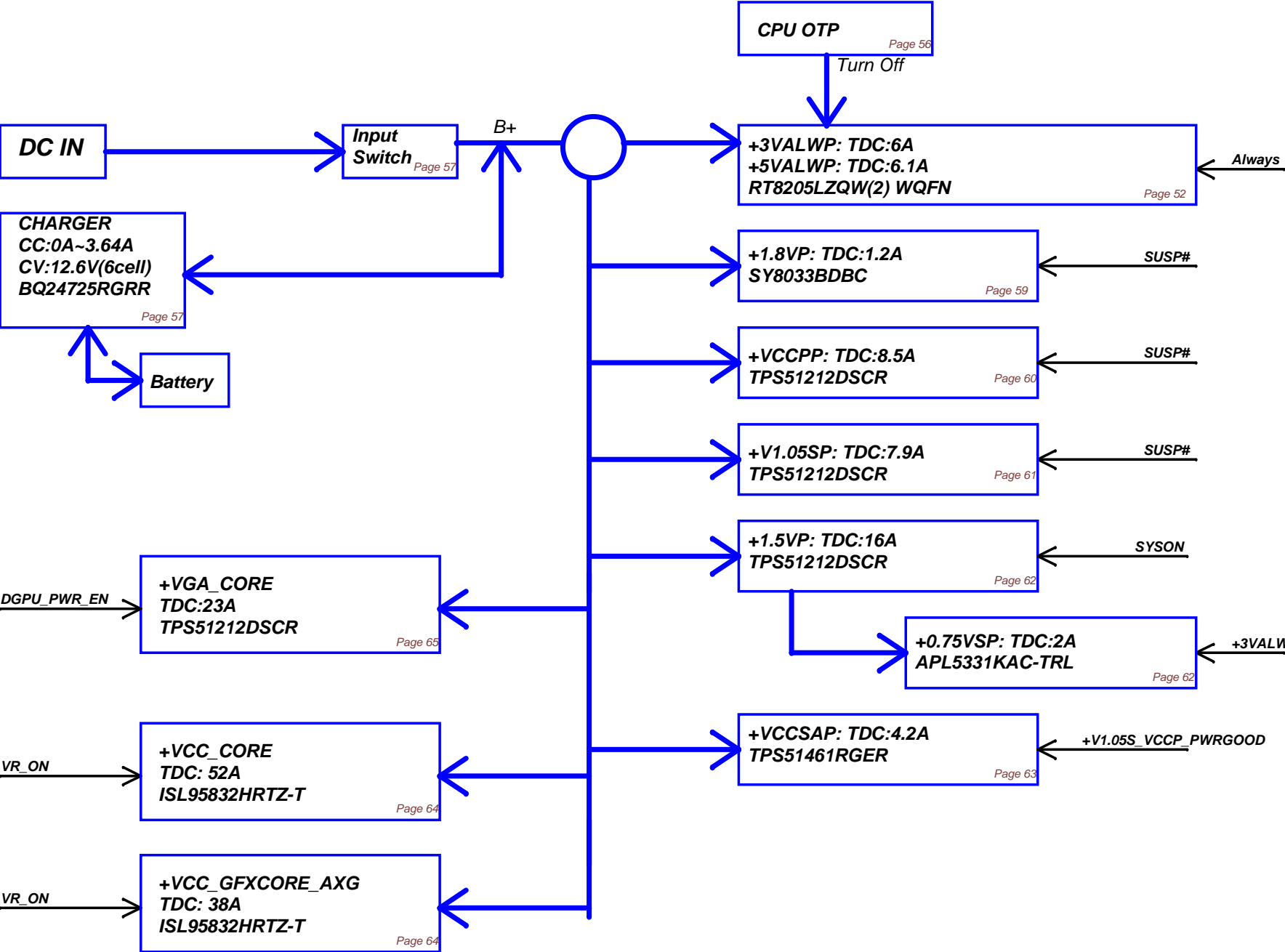
Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	

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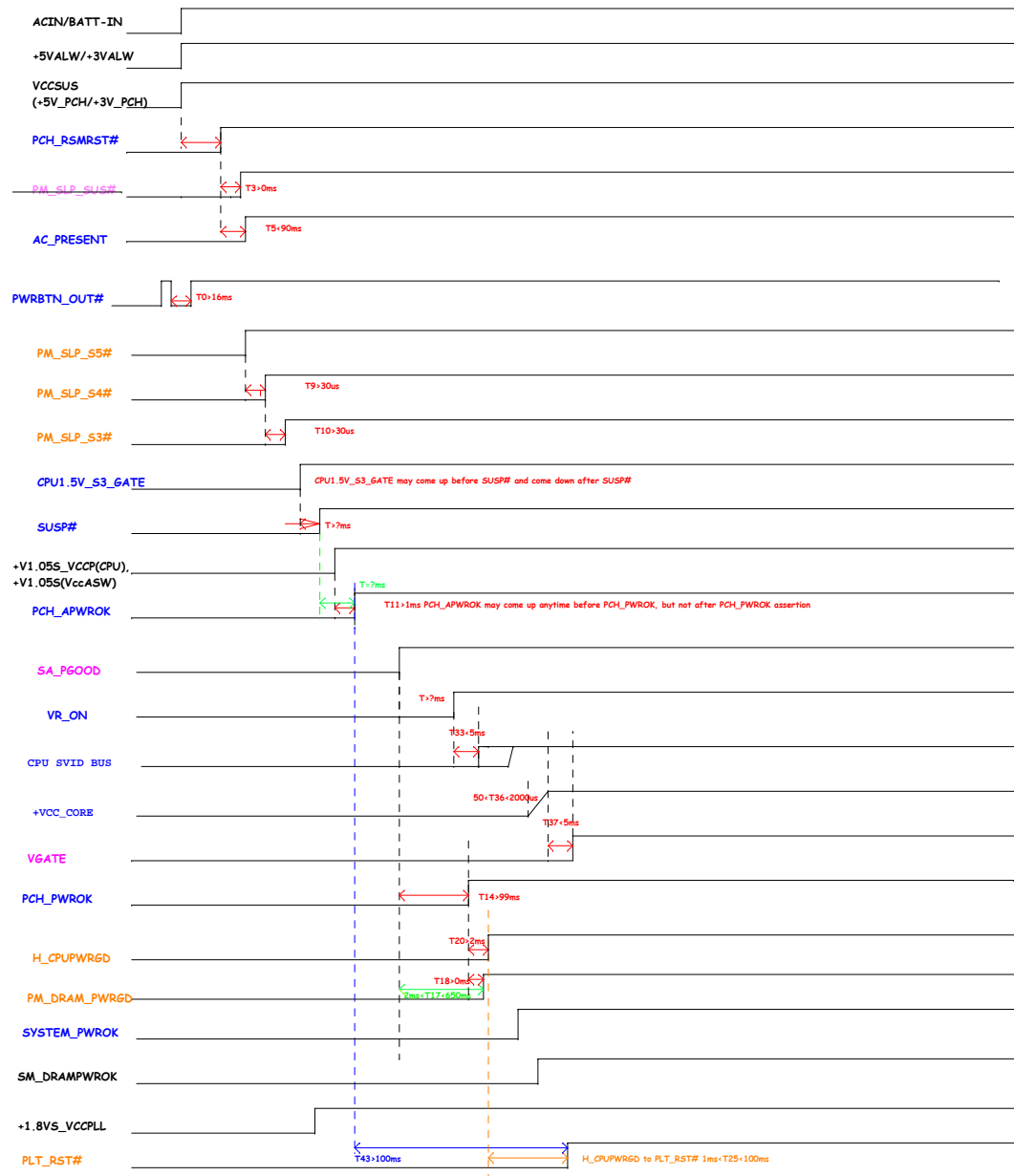
Power block



Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

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Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER01		HW Design (TMDS_B_HPD)	0.2	14	Delete R205	09/21	
ER02		For non AI co-lay	0.2	37	Add R745,R746 for non AI	09/21	
ER03	+3VS Leakage	HW Design (SMBus leakage)	0.2	13	AI parts change to AI@	09/21	
ER04	Can't detect USB30 (JUSB2)	HW Design (PCB2)	0.2	40	Delete Q3. (connect pin S & D) remove R135, R137	09/21	
ER05		Design change for card reader	0.2	34	Del R552, R556	09/21	
ER06		HW Design (PURC demand)	0.2	29	Swap U90,39/40 to U90,36/37 net	09/21	
ER07		HW Design(PCB2)	0.2	36	Change R1040 to 47K from 4.7K ohm	09/21	
ER08		HW Design (PURC demand)	0.2	42	Reserve R1029	09/21	
ER09		Fine-tune GPU timing	0.2	29	Add Q20, R773, R775	09/22	
ER10		HW Design (reserve)	0.2	18	Reserve R768, R774	09/21	
ER11		HW Design(PCB2) for add VRAM DDR3 512MX8	0.2	25,26,27,28	Change Net name at Card reader Conn	09/21	
ER12		HW Design (change)	0.2	39	Change to Q3(A03404L) from U22(A04430L)	09/21	
ER13		HW Design	0.2	40	Change R1049 to 330k	09/21	
ER14		HW Design (PURC demand)	0.2	15	Change Q904 to A03404L from AP2301GN	09/21	
ER15		HW Design (PURC demand)	0.2	29,31,37,38,10,11	Change R1046 to 1.5M	09/21	
ER16		HW Design(XTAL fine-tune)	0.2	42,12,13,32,20,36	Change Q33 to A03413L from AP2301GN	09/21	
ER17		HW Design for instant on function	0.2	13	Change R433 to 0 ohm un-stuff C396	09/21	
ER18		HW Design (power jumper change to +3VL)	0.2	38	Change R432 to 10K	09/21	
ER19		HW Design (PURC demand)	0.2	40	Change R435 to 200 ohm	09/21	
ER20		EMI solution	0.2	5	Reserve R290	09/21	
ER21		Refer to ORB design	0.2	14	Add CMDA14 signal (U12-U19 pin J7)	09/28	
ER22		change for GPU H/W strapping STRAP1 to PL 45K ohm to enhanced the PCIe PEG driving.	0.2	22	Reverse JKB1 connector	09/30	
			0.2	40	Del Y5 , C545 , C546	09/30	
			0.2	15	Del R229,R230 (10K) Add R776-R783 (10K)	09/30	
			0.2	29,31,37,38,10,11	Del R237,R239,R242 (8.2K) Add R784-R793 (8.2K)	09/30	
			0.2	42,12,13,32,20,36	Change P/N C387,C389,C399,C436,C447,C602	10/03	
			0.2	13,32,20,36	Change P/N C509,C515,C518,C526,(0402)	10/07	
			0.2	13	Change P/N C99,C109,C118,C120,C140,C141.(0402)	10/07	
			0.2	5	Change R607 to 10 ohm Change Y1,C144,C145 Change Y4,C469,C473.	10/07	
			0.2	40	Change Y2,C163,C164 Change Y9	10/07	
			0.2	14	Reserve R750	10/07	
			0.2	40	R576 pin2 change to +3V_PCH from +3VS	10/07	
			0.2	40	Change R576 to 0	10/07	
			0.2	40	jumper PJP302 (change +3VLP to +3VL @P38,P40)	10/07	
			0.2	40	Change P/N Q7,U20,U21.	10/14	
			0.2	40	Change P/N Q14-Q19,Q25,Q27-Q29,Q32,Q34-Q37,Q40-Q43,Q46-Q51,Q55-Q57,Q60,Q61,Q902,Q903,Q905.	10/14	
			0.2	40	Change P/N Q23	10/14	
			0.2	40	Add R684 to 0 (H_CPUPWRGD)	10/14	
			0.2	40	un-stuff D2, Add R751	10/14	
			0.2	40	un-stuff D32, R547, Add R752	10/14	
			0.2	40	Assign U33.18 to AC_PRESENT signal.	10/14	
			0.2	40	Change R349 from 34.8K to 45.3K	10/14	

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER23		modify parts for Intel review feedback message.	0.2	09 18 17 14 15	Add R289 , Add C149 0.1uf Del L6, Add R289 , un-stuff C212 Del L4, Add R387 Add R230 Stuff R244	10/14	
ER24		Modify H2 size	0.2	38	Modify H2 size	10/17	
ER25		Refer to Intel review feedback item 45.	0.2	16	Add R807	10/19	
ER26		Reserve for Deep Sx	0.2	14,16 40	Add unstuff R800,R801,R802,R803,R804,R805 Add PCH_DPWROK,DS_WAKE#,SUSACK#,SUSWARN#	10/19	
ER27		Reserve for ROM protect	0.2	40	Add unstuff R806	10/19	
ER28		For Instant On function control by EC	0.2	06	Stuff R44, Unstuff R43	10/19	
ER29		RF request	0.2	36	Reserve R1082 , C1045	10/19	
ER30		For LED issue	0.2	39	change LED3 footprint to LED_HT-210UD-UYG_3P	10/20	
ER31		PRUC request	0.2	38 39	Change SW3,SW4,SW5 P/N	10/20	
ER32		PRUC request	0.2	39	Change U36 P/N	10/20	
ER33		For EMI request (without MS_CLK)	0.2	34	Remove R637,C611,R631,C620.	10/20	
ER34		dGPU thermal throttling.	0.2	20 40	Add R428, Revise U11 I/O signal. Un-stuff R730.	10/20	
ER35		SPI flash data crisis prevention.	0.2	12 40	Add Q63, R135, R137. Change U33.41 net to EC_SPI_WP. remove R806.	10/20	
ER36		Power switch EOS issue prevention.	0.2	37	Change C510, C516, C519 to 0.22uF/16V.	10/20	
ER37		For EMI request	0.2	32 35	Change R485 , R486 to 0.1uF Reserve C641~C648	10/20	
ER38		For ESD request	0.2	37,35 30,39	Change D27,D29,D24,D25. Change D6,D7,D9,D10,D33,D34.	10/20	
ER39		Modify X76 table (N13P-GS & N13M-GE1 x8)	0.2	3	update X76 table (add ZZZ9 ~ZZZ12 for N13P-GS & N13M-GE1 x8) & P/N	10/25	
ER40		update Power circuit	0.2	43~56	update Power circuit. (PC211)	10/26	
ER41		Modify PCH_SPI_WP# singal control by EC	0.2	12	Stuff R135	10/26	
ER42		Add test point for DFT	0.2	20	Add GPU_JTAG_TCK,GPU_JTAG_TDI,GPU_JTAG_TDO, GPU_JTAG_TMS	10/27	
ER43		For ASM1042 OC# pull-up	0.2	37	Reserve R1023,R1024 un-stuff	10/27 b	

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