

# First International Computer, Inc

## Portable Computer Group HW Department

Board name : MotherBoard Schematic

Project : TY640

Version : 0.3

Initial Date : JAN. 25 , 2008

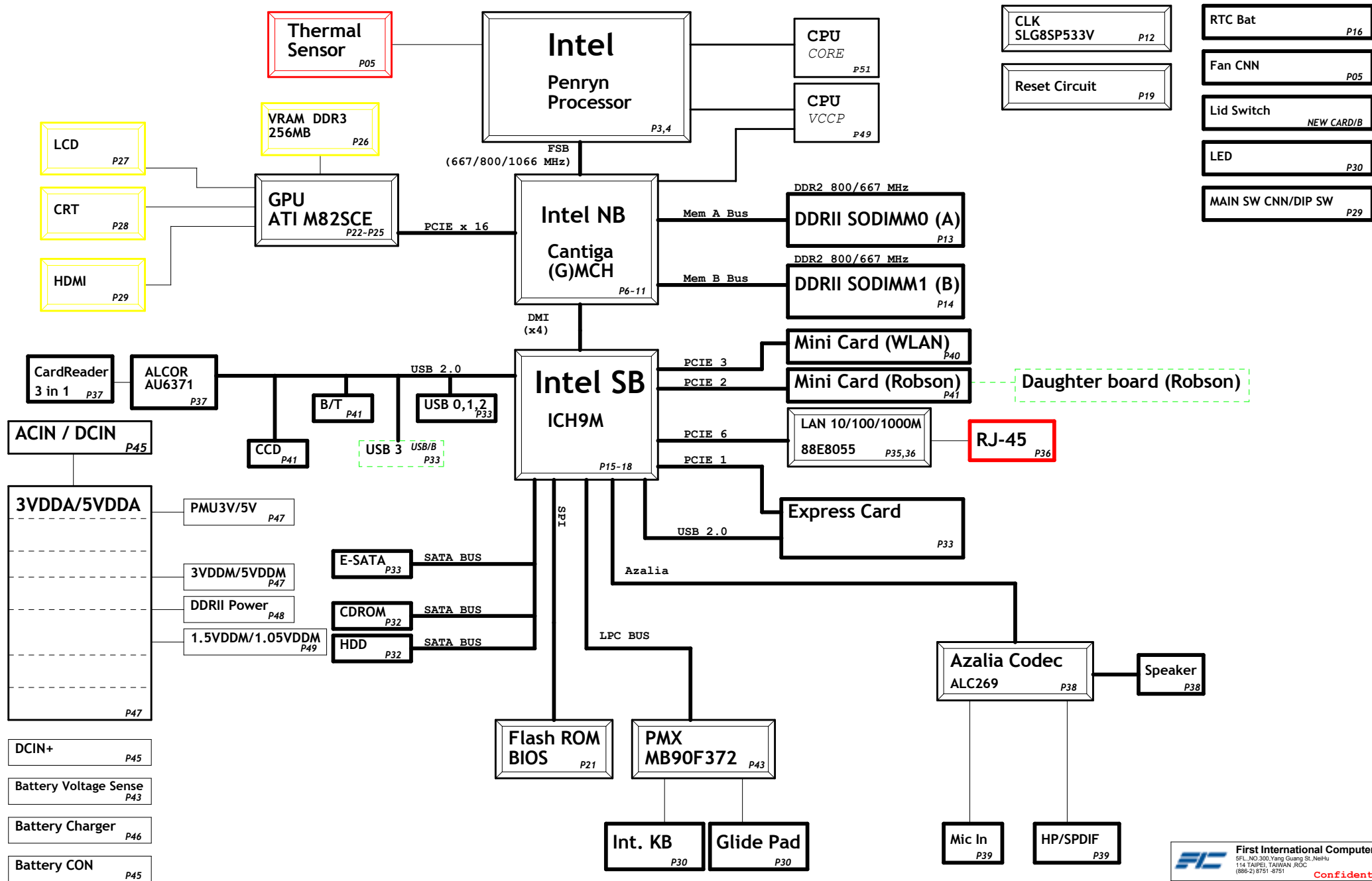
Manager Sign by: AVERY

Drawing by : Jason\_Hsu

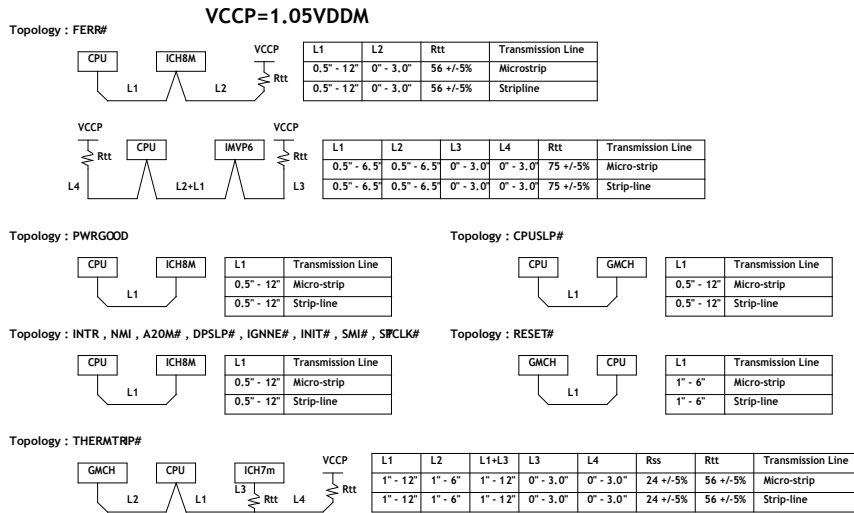
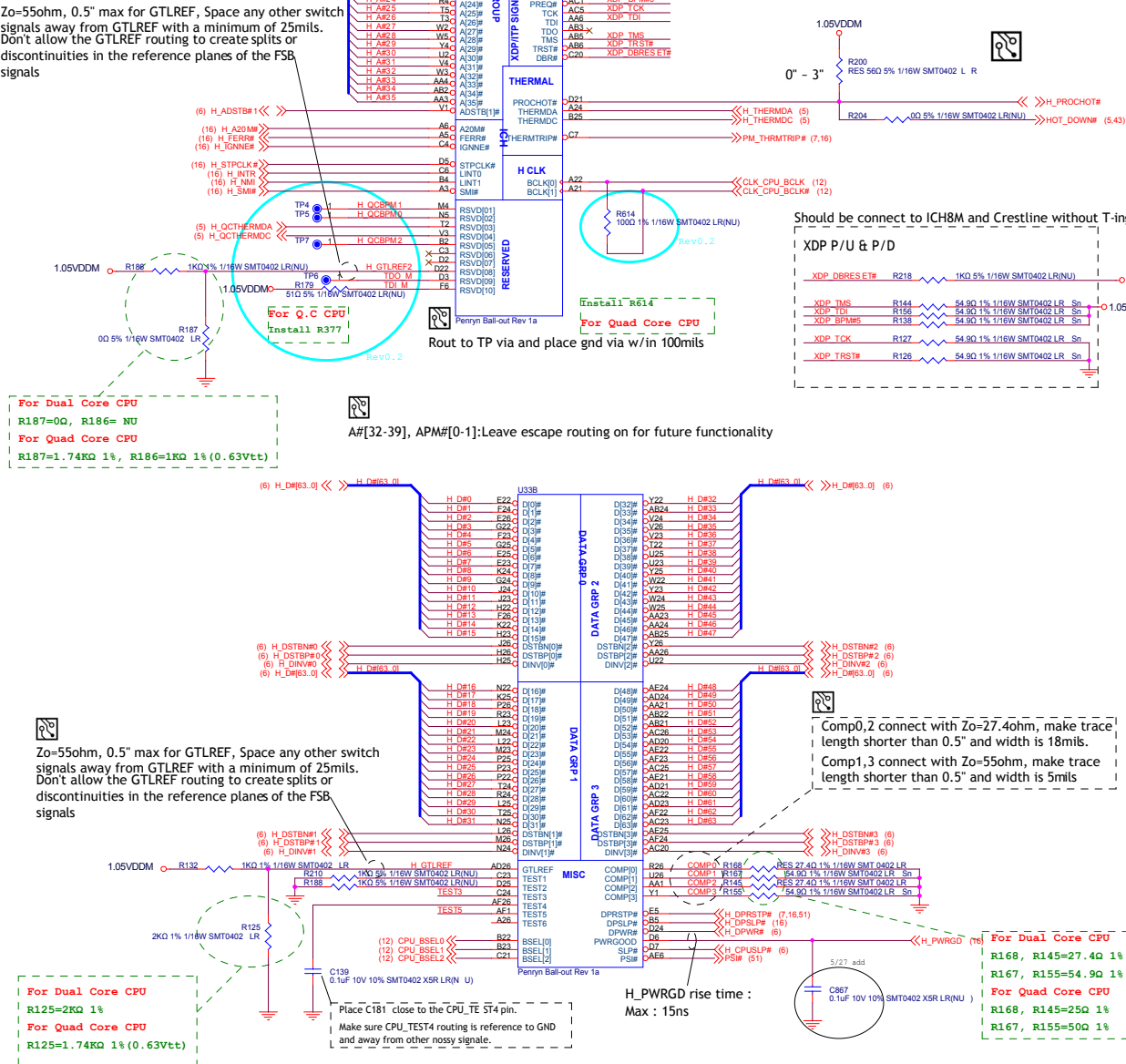
Total confirm by: Spurge

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### 3. Block Diagram :



Zo=55ohm, 0.5" max for GTLREF, Space any other switch signals away from GTLREF with a minimum of 25mils. Don't allow the GTLREF routing to create splits or discontinuities in the reference planes of the FSB signals



Processor ITP Signal Default Strapping When ITP-XDP & ITP700FLEX Debug Port Not Used.

Signal	Resistor Value	Connect To	Resistor Placement
TDI	54.9 OHM +/-5%	VCCP	Within 2.0" of the CPU
TMS	54.9 OHM +/-5%	VCCP	Within 2.0" of the CPU
TRST#	649 OHM +/-5%	GND	Within 2.0" of the CPU
TCK	54.9 OHM +/-5%	GND	Within 2.0" of the CPU
TDO	OPEN	NC	N/A

FSB Common Clock Signal Layout Guide :

ADS#, BNR#, BPR#, BRO#, DBSY#, DEFER#, DPWR#, DRDY#, HIT#, HIM#, LOCK#, RS[2..0]#, TRDY#, RESET#	Total Trace Length	Normal Impedance	Spacing (mils)
Transmission Line Type	1.0 - 6.5 inch	55 +/-15%	4 & 8 mils
Strip-line(Int. Layer)			5 & 10 mils
Micro-strip(Ext. Layer)			

FSB Source Synchronous Data Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe-to-Strobe Complement Matching
DATA#[15..0], DINV0#	+/- 100 mils	DSTBP0#, DSTBN0#	+/- 25 mils
DATA#[31..16], DINV1#	+/- 100 mils	DSTBP1#, DSTBN1#	+/- 25 mils
DATA#[47..32], DINV2#	+/- 100 mils	DSTBP2#, DSTBN2#	+/- 25 mils
DATA#[63..48], DINV3#	+/- 100 mils	DSTBP3#, DSTBN3#	+/- 25 mils

FSB Source Synchronous Data Signal Routing Topology#1 :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)
DINV#[3..0]	Strip-line	0.5 - 5.5 inch	55 +/-15%	4 & 8 mils
DATA#[63..0]	Strip-line	0.5 - 5.5 inch	55 +/-15%	4 & 8 mils
DSTBN#[3..0]	Strip-line	0.5 - 5.5 inch	55 +/-15%	4 & 12 mils
DSTBP#[3..0]	Strip-line	0.5 - 5.5 inch	55 +/-15%	4 & 12 mils

FSB Source Synchronous Address Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe to Assoc. Address Signal Matching
ADDR#[16..3], REQ#4..0]	+/- 200 mils	ADSTB0#	+/- 200 mils
ADDR#[31..17]	+/- 200 mils	ADSTB1#	+/- 200 mils

\*\*\* No length matching requirements exist between ADSTB0# and ADSTB1#

FSB Source Synchronous Address Signal Routing :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)
Address#[31..3]	Strip-line	0.5 - 6.5 inch	55 +/-15%	4 & 8 mils
REQ#[4..0]	Strip-line	0.5 - 6.5 inch	55 +/-15%	4 & 8 mils
ADSTB#[1..0]	Strip-line	0.5 - 6.5 inch	55 +/-15%	4 & 8 mils

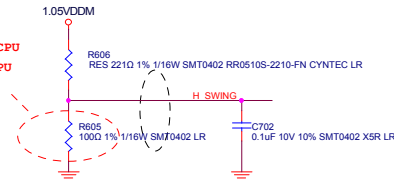




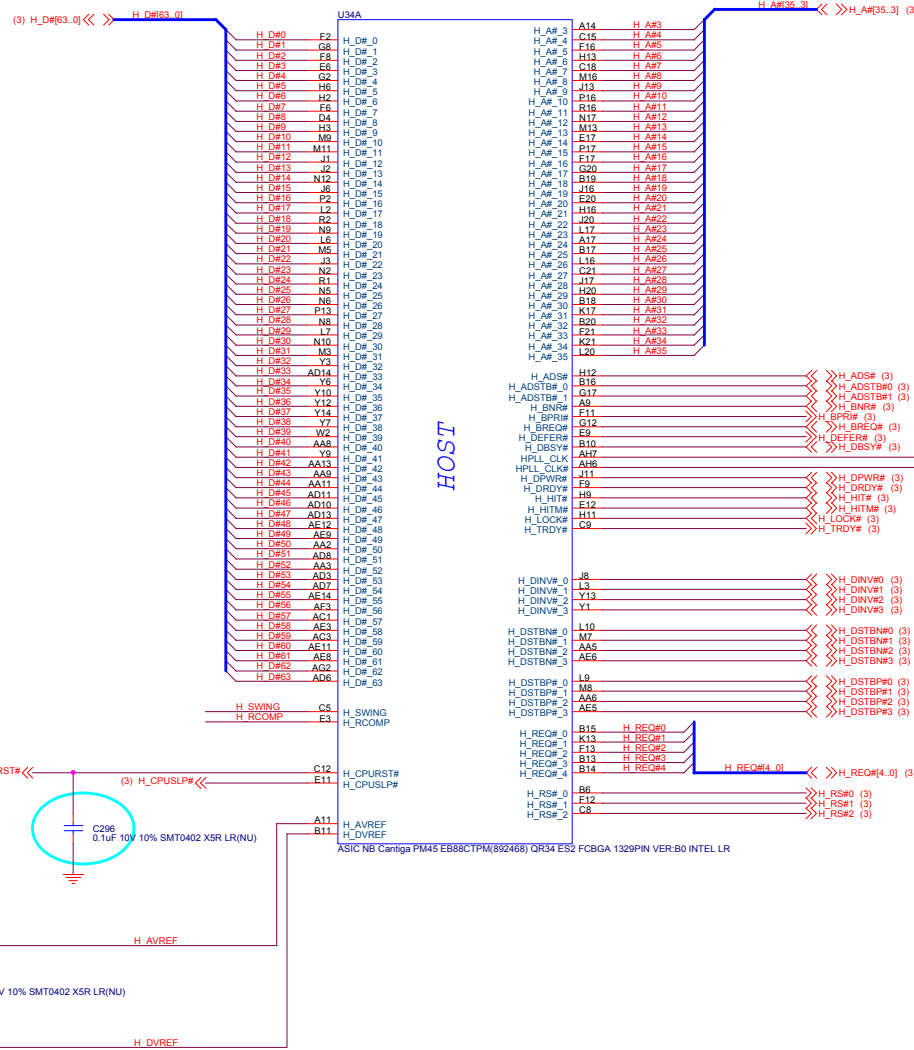
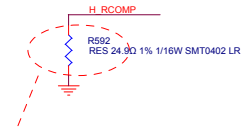
## C



R600=100Q for Dual core CPU  
R600=75Q for Quad core CPU  
Checklist 1.1



R589=24.9Q for Dual core CPU  
R589=16.9Q for Quad core CPU  
Checklist 1.1



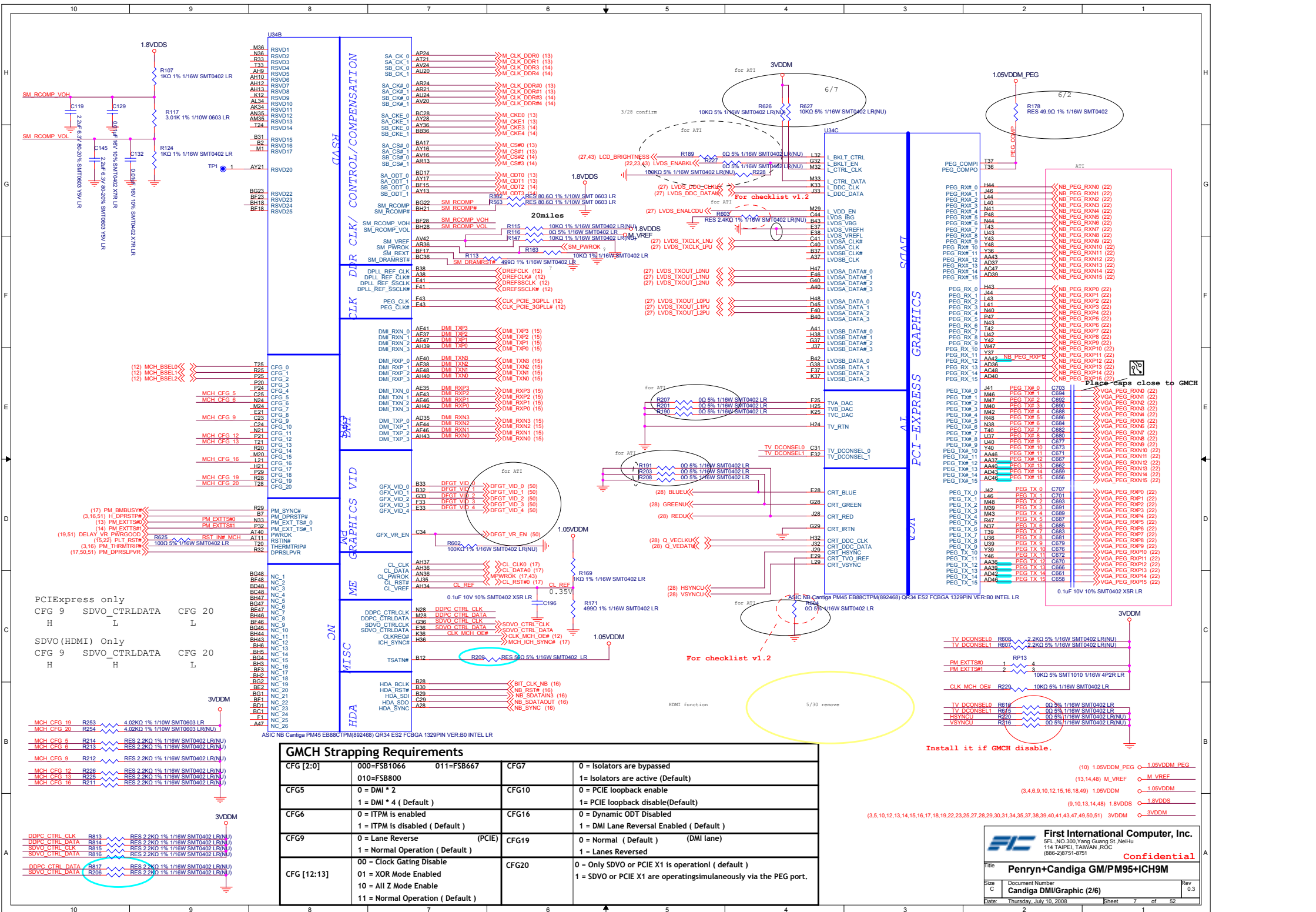
(3,4,7,9,10,12,15,16,18,49) 1.05VDDM 1.05VDDM

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Penryn+Candiga GM/PM95+ICH9M  
Candiga Host (1/6)

Date: Thursday, July 10, 2008 Sheet: 6 of 52  
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(13) M\_A\_DQ[63..0] << >> M\_A\_DQ[63..0]

M_A_DQ00	A138	SA_DQ_0
M_A_DQ01	A441	SA_DQ_1
M_A_DQ02	AN38	SA_DQ_2
M_A_DQ03	AM38	SA_DQ_3
M_A_DQ04	A136	SA_DQ_4
M_A_DQ05	A140	SA_DQ_5
M_A_DQ06	AM44	SA_DQ_6
M_A_DQ07	AM42	SA_DQ_7
M_A_DQ08	AM43	SA_DQ_8
M_A_DQ09	AM44	SA_DQ_9
M_A_DQ10	AU40	SA_DQ_10
M_A_DQ11	A138	SA_DQ_11
M_A_DQ12	AN41	SA_DQ_12
M_A_DQ13	AN39	SA_DQ_13
M_A_DQ14	AU44	SA_DQ_14
M_A_DQ15	AU42	SA_DQ_15
M_A_DQ16	AV39	SA_DQ_16
M_A_DQ17	AY44	SA_DQ_17
M_A_DQ18	BA40	SA_DQ_18
M_A_DQ19	BD43	SA_DQ_19
M_A_DQ20	AV41	SA_DQ_20
M_A_DQ21	AY43	SA_DQ_21
M_A_DQ22	BA41	SA_DQ_22
M_A_DQ23	BC40	SA_DQ_23
M_A_DQ24	AV37	SA_DQ_24
M_A_DQ25	BD38	SA_DQ_25
M_A_DQ26	AV37	SA_DQ_26
M_A_DQ27	AT38	SA_DQ_27
M_A_DQ28	AY38	SA_DQ_28
M_A_DQ29	BD38	SA_DQ_29
M_A_DQ30	AV38	SA_DQ_30
M_A_DQ31	AW36	SA_DQ_31
M_A_DQ32	BD13	SA_DQ_32
M_A_DQ33	AU11	SA_DQ_33
M_A_DQ34	BC11	SA_DQ_34
M_A_DQ35	BA12	SA_DQ_35
M_A_DQ36	AU13	SA_DQ_36
M_A_DQ37	AV13	SA_DQ_37
M_A_DQ38	BD12	SA_DQ_38
M_A_DQ39	BC12	SA_DQ_39
M_A_DQ40	BD9	SA_DQ_40
M_A_DQ41	BA9	SA_DQ_41
M_A_DQ42	AU10	SA_DQ_42
M_A_DQ43	AV9	SA_DQ_43
M_A_DQ44	BA11	SA_DQ_44
M_A_DQ45	BD9	SA_DQ_45
M_A_DQ46	AV8	SA_DQ_46
M_A_DQ47	BA6	SA_DQ_47
M_A_DQ48	AV6	SA_DQ_48
M_A_DQ49	AV7	SA_DQ_49
M_A_DQ50	AT9	SA_DQ_50
M_A_DQ51	AN8	SA_DQ_51
M_A_DQ52	AU5	SA_DQ_52
M_A_DQ53	AU6	SA_DQ_53
M_A_DQ54	AT5	SA_DQ_54
M_A_DQ55	AN10	SA_DQ_55
M_A_DQ56	AM11	SA_DQ_56
M_A_DQ57	AM5	SA_DQ_57
M_A_DQ58	A9	SA_DQ_58
M_A_DQ59	A8	SA_DQ_59
M_A_DQ60	AN12	SA_DQ_60
M_A_DQ61	AM13	SA_DQ_61
M_A_DQ62	AJ11	SA_DQ_62
M_A_DQ63	AJ12	SA_DQ_63

ASIC NB Cantiga PM45 EB88CTPM(892468) QR34 ES2 FCBGA 1329PIN VER:B0 INTEL LR

DDR SYSTEM MEMORY A

SA_BS_0	BD21	>>>M_A_BS0 (13)
SA_BS_1	BC16	>>>M_A_BS1 (13)
SA_BS_2	AT25	>>>M_A_BS2 (13)
SA_RAS#	BB20	>>>M_A_RAS# (13)
SA_CAS#	BD20	>>>M_A_CAS# (13)
SA_WE#	AY20	>>>M_A_WE# (13)
SA_DM_0	AM37	M_A_DM0 >>>M_A_DM7..0] (13)
SA_DM_1	AT41	M_A_DM1
SA_DM_2	AY41	M_A_DM2
SA_DM_3	AU39	M_A_DM3
SA_DM_4	BB12	M_A_DM4
SA_DM_5	AY5	M_A_DM5
SA_DM_6	AT7	M_A_DM6
SA_DM_7	AJ6	M_A_DM7
SA_DQS_0	AJ44	M_A_DQS0
SA_DQS_1	AT44	M_A_DQS1
SA_DQS_2	BA43	M_A_DQS2
SA_DQS_3	BC37	M_A_DQS3
SA_DQS_4	AW12	M_A_DQS4
SA_DQS_5	BC8	M_A_DQS5
SA_DQS_6	AU8	M_A_DQS6
SA_DQS_7	AM7	M_A_DQS7
SA_DQS_8	AJ43	M_A_DQS8
SA_DQS_9	AT43	M_A_DQS9
SA_DQS_10	BA44	M_A_DQS10
SA_DQS_11	BD37	M_A_DQS11
SA_DQS_12	AY12	M_A_DQS12
SA_DQS_13	BD8	M_A_DQS13
SA_DQS_14	AU8	M_A_DQS14
SA_DQS_15	AM6	M_A_DQS15
SA_DQS_16	BA21	M_A_A0
SA_DQS_17	BC24	M_A_A1
SA_DQS_18	BD24	M_A_A2
SA_DQS_19	BH24	M_A_A3
SA_DQS_20	BG25	M_A_A4
SA_DQS_21	BD4	M_A_A5
SA_DQS_22	BG27	M_A_A6
SA_DQS_23	BE25	M_A_A7
SA_DQS_24	AW24	M_A_A8
SA_DQS_25	BC21	M_A_A9
SA_DQS_26	BC26	M_A_A10
SA_DQS_27	BH26	M_A_A11
SA_DQS_28	BH17	M_A_A12
SA_DQS_29	AY25	M_A_A13
SA_DQS_30	AY25	M_A_A14

(14) M\_B\_DQ[63..0] << >> M\_B\_DQ[63..0]

M_B_DQ00	AK47	SB_DQ_0
M_B_DQ01	AH46	SB_DQ_1
M_B_DQ02	AP47	SB_DQ_2
M_B_DQ03	AK46	SB_DQ_3
M_B_DQ04	AH46	SB_DQ_4
M_B_DQ05	AH46	SB_DQ_5
M_B_DQ06	AM48	SB_DQ_6
M_B_DQ07	AP48	SB_DQ_7
M_B_DQ08	AU47	SB_DQ_8
M_B_DQ09	AH46	SB_DQ_9
M_B_DQ10	BA48	SB_DQ_10
M_B_DQ11	AY48	SB_DQ_11
M_B_DQ12	AT47	SB_DQ_12
M_B_DQ13	AK47	SB_DQ_13
M_B_DQ14	BA47	SB_DQ_14
M_B_DQ15	BC47	SB_DQ_15
M_B_DQ16	BC46	SB_DQ_16
M_B_DQ17	BC44	SB_DQ_17
M_B_DQ18	BC43	SB_DQ_18
M_B_DQ19	BE43	SB_DQ_19
M_B_DQ20	BE45	SB_DQ_20
M_B_DQ21	BC41	SB_DQ_21
M_B_DQ22	BE40	SB_DQ_22
M_B_DQ23	BE41	SB_DQ_23
M_B_DQ24	BC38	SB_DQ_24
M_B_DQ25	BE38	SB_DQ_25
M_B_DQ26	BH35	SB_DQ_26
M_B_DQ27	BC35	SB_DQ_27
M_B_DQ28	BC36	SB_DQ_28
M_B_DQ29	BC34	SB_DQ_29
M_B_DQ30	BH34	SB_DQ_30
M_B_DQ31	BH34	SB_DQ_31
M_B_DQ32	BH14	SB_DQ_32
M_B_DQ33	BC12	SB_DQ_33
M_B_DQ34	BH11	SB_DQ_34
M_B_DQ35	BC5	SB_DQ_35
M_B_DQ36	BH12	SB_DQ_36
M_B_DQ37	BE11	SB_DQ_37
M_B_DQ38	BE8	SB_DQ_38
M_B_DQ39	BC7	SB_DQ_39
M_B_DQ40	BC5	SB_DQ_40
M_B_DQ41	BC6	SB_DQ_41
M_B_DQ42	AV3	SB_DQ_42
M_B_DQ43	AV1	SB_DQ_43
M_B_DQ44	BE6	SB_DQ_44
M_B_DQ45	BE5	SB_DQ_45
M_B_DQ46	BA1	SB_DQ_46
M_B_DQ47	BD3	SB_DQ_47
M_B_DQ48	AV2	SB_DQ_48
M_B_DQ49	AU3	SB_DQ_49
M_B_DQ50	AS3	SB_DQ_50
M_B_DQ51	AN2	SB_DQ_51
M_B_DQ52	AY2	SB_DQ_52
M_B_DQ53	AV1	SB_DQ_53
M_B_DQ54	AP3	SB_DQ_54
M_B_DQ55	AR1	SB_DQ_55
M_B_DQ56	AL1	SB_DQ_56
M_B_DQ57	AL2	SB_DQ_57
M_B_DQ58	AJ11	SB_DQ_58
M_B_DQ59	AH1	SB_DQ_59
M_B_DQ60	AM2	SB_DQ_60
M_B_DQ61	AM3	SB_DQ_61
M_B_DQ62	AH3	SB_DQ_62
M_B_DQ63	AJ3	SB_DQ_63

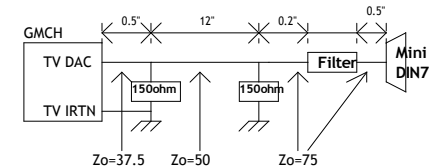
ASIC NB Cantiga PM45 EB88CTPM(892468) QR34 ES2 FCBGA 1329PIN VER:B0 INTEL LR

DDR SYSTEM MEMORY B

SB_BS_0	BC16	>>>M_B_BS0 (14)
SB_BS_1	BB17	>>>M_B_BS1 (14)
SB_BS_2	BB33	>>>M_B_BS2 (14)
SB_RAS#	AU17	>>>M_B_RAS# (14)
SB_CAS#	BC16	>>>M_B_CAS# (14)
SB_WE#	BE14	>>>M_B_WE# (14)
SB_DM_0	AM47	M_B_DM0 >>>M_B_DM7..0] (14)
SB_DM_1	AY47	M_B_DM1
SB_DM_2	BA40	M_B_DM2
SB_DM_3	BE35	M_B_DM3
SB_DM_4	BC11	M_B_DM4
SB_DM_5	BA3	M_B_DM5
SB_DM_6	AP1	M_B_DM6
SB_DM_7	AK2	M_B_DM7
SB_DQS_0	AL47	M_B_DQS0
SB_DQS_1	AV48	M_B_DQS1
SB_DQS_2	BC41	M_B_DQS2
SB_DQS_3	BC37	M_B_DQS3
SB_DQS_4	BH9	M_B_DQS4
SB_DQS_5	BE2	M_B_DQS5
SB_DQS_6	AU1	M_B_DQS6
SB_DQS_7	AN6	M_B_DQS7
SB_DQS_8	AL46	M_B_DQS8
SB_DQS_9	AV47	M_B_DQS9
SB_DQS_10	BH41	M_B_DQS10
SB_DQS_11	BE37	M_B_DQS11
SB_DQS_12	BH41	M_B_DQS12
SB_DQS_13	BC2	M_B_DQS13
SB_DQS_14	AT2	M_B_DQS14
SB_DQS_15	AN5	M_B_DQS15
SB_MA_0	AV17	M_B_A0
SB_MA_1	BA25	M_B_A1
SB_MA_2	BC25	M_B_A2
SB_MA_3	AU25	M_B_A3
SB_MA_4	AW25	M_B_A4
SB_MA_5	BD28	M_B_A5
SB_MA_6	AU28	M_B_A6
SB_MA_7	AW28	M_B_A7
SB_MA_8	AT33	M_B_A8
SB_MA_9	BD33	M_B_A9
SB_MA_10	BB16	M_B_A10
SB_MA_11	AW33	M_B_A11
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SB_MA_13	BH15	M_B_A13
SB_MA_14	AU33	M_B_A14

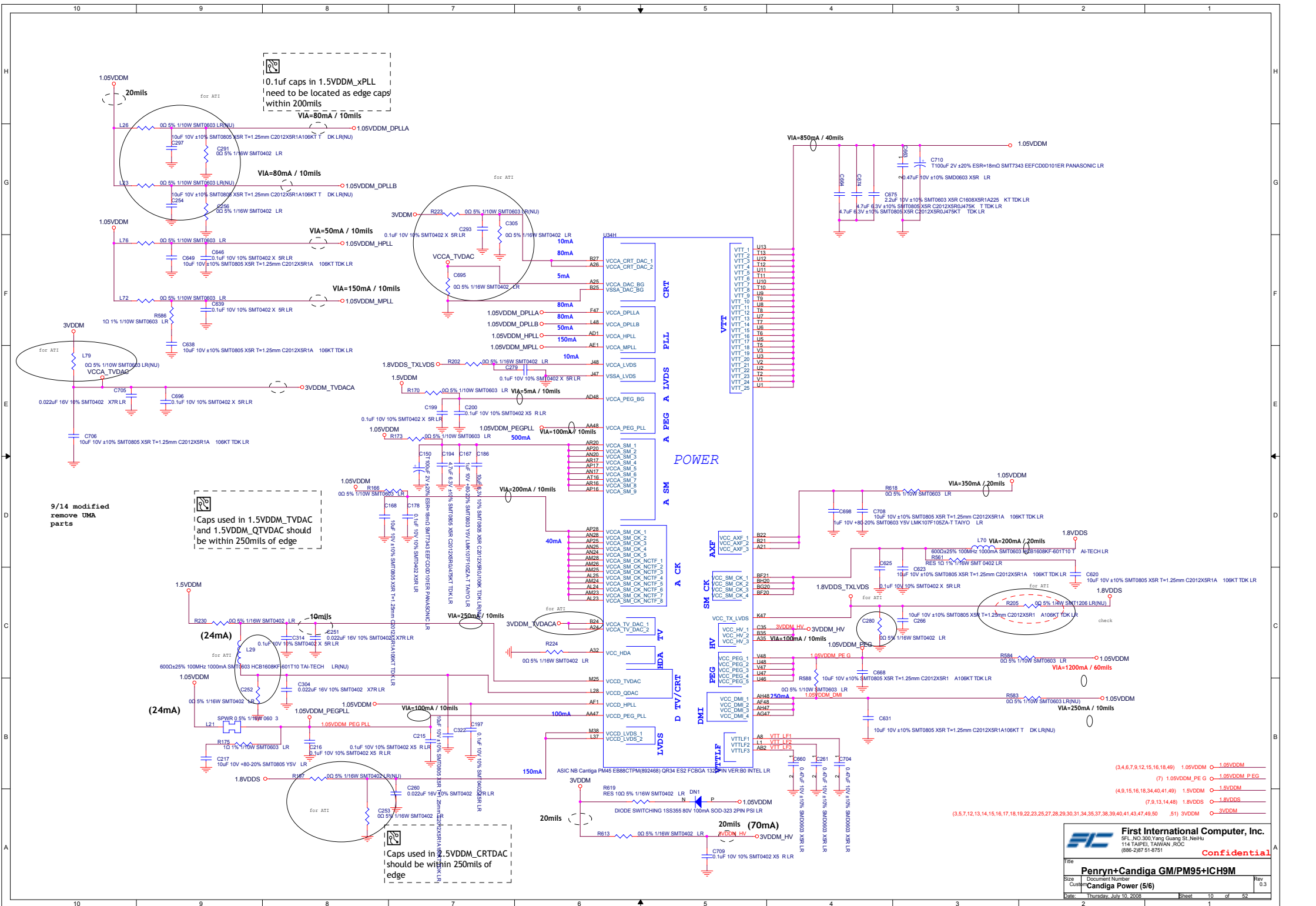
### TV DAC Routing Guideline

1. The minimum spacing between each RGB is 40-mils while 50-mils is preferred
2. RGB signals should be routed on the same layer, have a similar number of bends, same number of vias
3. All routing should be done with ground referencing as well
4. TV DAC route lengths should be length match to within 200 mils



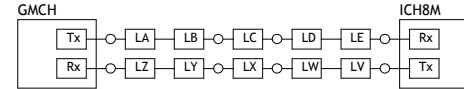






U341	U34J	U34J	AHR
AU48 VSS 1	AM36 VSS 100	BG21 VSS 189	VSS 297
AR48 VSS 2	AE36 VSS 101	VSS 200	Y8 VSS 298
AL48 VSS 3	VSS 102	AW21 VSS 201	VSS 299
BM47 VSS 4	VSS 103	AP21 VSS 202	VSS 300
AM47 VSS 5	VSS 104	VSS 203	VSS 301
AM47 VSS 6	VSS 105	VSS 204	VSS 302
AM47 VSS 7	VSS 106	VSS 205	VSS 303
AF47 VSS 8	VSS 107	VSS 206	VSS 304
AD47 VSS 9	VSS 108	VSS 207	VSS 305
AB47 VSS 10	VSS 109	VSS 208	VSS 306
Y47 VSS 11	VSS 110	VSS 209	VSS 307
T47 VSS 12	VSS 111	VSS 210	VSS 308
N47 VSS 13	VSS 112	VSS 211	VSS 309
G47 VSS 14	VSS 113	VSS 212	VSS 310
VSS 15	VSS 114	VSS 213	VSS 311
BD46 VSS 16	VSS 115	VSS 214	VSS 312
BA46 VSS 17	VSS 116	VSS 215	VSS 313
AY46 VSS 18	VSS 117	VSS 216	VSS 314
AM46 VSS 19	VSS 118	VSS 217	VSS 315
AM46 VSS 20	VSS 119	VSS 218	VSS 316
AM46 VSS 21	VSS 120	VSS 219	VSS 317
VSS 22	VSS 121	VSS 220	VSS 318
R46 VSS 23	VSS 122	VSS 221	VSS 319
PM46 VSS 24	VSS 123	VSS 222	VSS 320
H46 VSS 25	VSS 124	VSS 223	VSS 321
F46 VSS 26	VSS 125	VSS 224	VSS 322
BF44 VSS 27	VSS 126	VSS 225	VSS 323
AH44 VSS 28	VSS 127	VSS 226	VSS 324
AD44 VSS 29	VSS 128	VSS 227	VSS 325
AA44 VSS 30	VSS 129	VSS 228	VSS 326
Y44 VSS 31	VSS 130	VSS 229	VSS 327
U44 VSS 32	VSS 131	VSS 230	VSS 328
T44 VSS 33	VSS 132	VSS 231	VSS 329
M44 VSS 34	VSS 133	VSS 232	VSS 330
F44 VSS 35	VSS 134	VSS 233	VSS 331
BC43 VSS 36	VSS 135	VSS 234	VSS 332
AM43 VSS 37	VSS 136	VSS 235	VSS 333
AM43 VSS 38	VSS 137	VSS 236	VSS 334
AM43 VSS 39	VSS 138	VSS 237	VSS 335
VSS 40	VSS 139	VSS 238	VSS 336
CA3 VSS 41	VSS 140	VSS 239	VSS 337
BG42 VSS 42	VSS 141	VSS 240	VSS 338
AT42 VSS 43	VSS 142	VSS 241	VSS 339
AM42 VSS 44	VSS 143	VSS 242	VSS 340
AM42 VSS 45	VSS 144	VSS 243	VSS 341
AE42 VSS 46	VSS 145	VSS 244	VSS 342
AE42 VSS 47	VSS 146	VSS 245	VSS 343
VSS 48	VSS 147	VSS 246	VSS 344
L42 VSS 49	VSS 148	VSS 247	VSS 345
BD41 VSS 50	VSS 149	VSS 248	VSS 346
AM41 VSS 51	VSS 150	VSS 249	VSS 347
AM41 VSS 52	VSS 151	VSS 250	VSS 348
AD41 VSS 53	VSS 152	VSS 251	VSS 349
AM41 VSS 54	VSS 153	VSS 252	VSS 350
AM41 VSS 55	VSS 154	VSS 253	VSS 351
Y41 VSS 56	VSS 155	VSS 254	VSS 352
U41 VSS 57	VSS 156	VSS 255	VSS 353
T41 VSS 58	VSS 157	VSS 256	VSS 354
M41 VSS 59	VSS 158	VSS 257	VSS 355
G41 VSS 60	VSS 159	VSS 258	VSS 356
B41 VSS 61	VSS 160	VSS 259	VSS 357
BG40 VSS 62	VSS 161	VSS 260	VSS 358
BM40 VSS 63	VSS 162	VSS 261	VSS 359
AM40 VSS 64	VSS 163	VSS 262	VSS 360
AM40 VSS 65	VSS 164	VSS 263	VSS 361
H40 VSS 66	VSS 165	VSS 264	VSS 362
E40 VSS 67	VSS 166	VSS 265	VSS 363
AT39 VSS 68	VSS 167	VSS 266	VSS 364
AM39 VSS 69	VSS 168	VSS 267	VSS 365
AE39 VSS 70	VSS 169	VSS 268	VSS 366
VSS 71	VSS 170	VSS 269	VSS 367
N39 VSS 72	VSS 171	VSS 270	VSS 368
L39 VSS 73	VSS 172	VSS 271	VSS 369
B39 VSS 74	VSS 173	VSS 272	VSS 370
BH38 VSS 75	VSS 174	VSS 273	VSS 371
BC38 VSS 76	VSS 175	VSS 274	VSS 372
BA38 VSS 77	VSS 176	VSS 275	VSS 373
AU38 VSS 78	VSS 177	VSS 276	VSS 374
AH38 VSS 79	VSS 178	VSS 277	VSS 375
AD38 VSS 80	VSS 179	VSS 278	VSS 376
AA38 VSS 81	VSS 180	VSS 279	VSS 377
Y38 VSS 82	VSS 181	VSS 280	VSS 378
T38 VSS 83	VSS 182	VSS 281	VSS 379
M38 VSS 84	VSS 183	VSS 282	VSS 380
F38 VSS 85	VSS 184	VSS 283	VSS 381
BF37 VSS 86	VSS 185	VSS 284	VSS 382
C38 VSS 87	VSS 186	VSS 285	VSS 383
BB37 VSS 88	VSS 187	VSS 286	VSS 384
AW37 VSS 89	VSS 188	VSS 287	VSS 385
AT37 VSS 90	VSS 189	VSS 288	VSS 386
AN37 VSS 91	VSS 190	VSS 289	VSS 387
AJ37 VSS 92	VSS 191	VSS 290	VSS 388
C37 VSS 93	VSS 192	VSS 291	VSS 389
H37 VSS 94	VSS 193	VSS 292	VSS 390
BG36 VSS 95	VSS 194	VSS 293	VSS 391
BD36 VSS 96	VSS 195	VSS 294	VSS 392
VSS 97	VSS 196	VSS 295	VSS 393
AK15 VSS 98	VSS 197	VSS 296	VSS 394
AU36 VSS 99	VSS 198	VSS 297	VSS 395
VSS 100	VSS 199	VSS 298	VSS 396

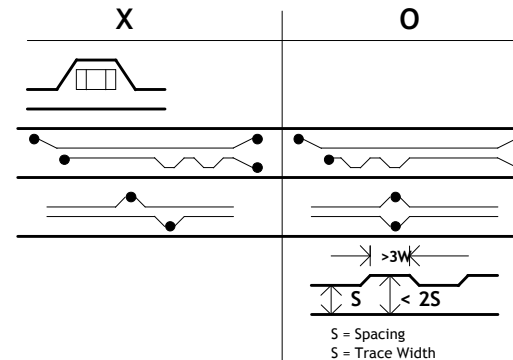
## DMI Routing Guideline



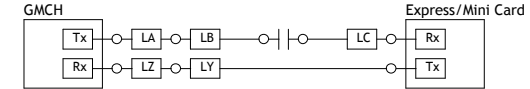
Breakout/in LA/LZ	Main Route LB/LY	Main Route LD/LW	Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Diderential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 27 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 400 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-LF (LA+LB+LC+LD+LE)	Max = 8000 mils	
Trace Length-LV ( ICH7m Breakout)	Max = 400 mils	
Trace Length-LW ( ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-LZ (LV+LW+LX+LY+LZ)	Max = 8000 mils	

\*\*\* When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane  
\*\*\* Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



## PCIE Routing Guideline

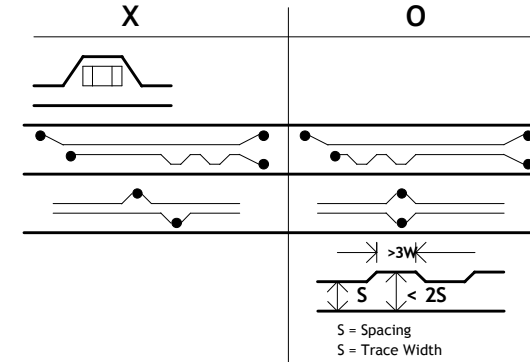


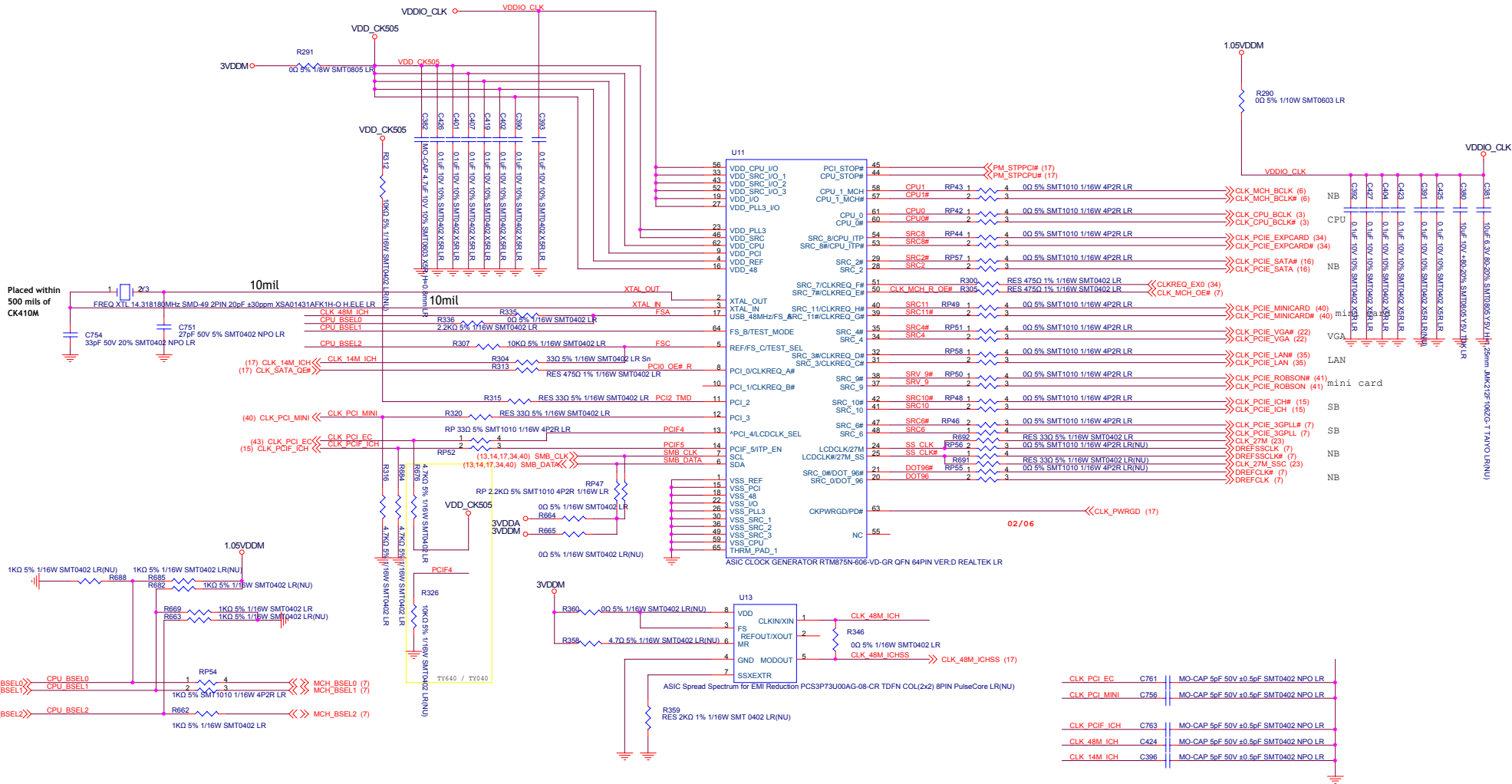
Breakout/in LA/LZ	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe CN)	Max = 12000 mils	
Trace Length-LY (PCIe CN to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-LZ (LY+LZ)	Max = 12000 mils	

\*\*\* When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane  
\*\*\* Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils





FSC	FSB	FSA	Host Clock Frequency MHz
CPU_BSEL2	CPU_BSEL1	CPU_BSEL0	
0	1	1	166
0	1	0	200

SS3	SS2	SS1	SS0	Spread Mode	Spread Amount %
0	0	0	0	DOWN	0.8
0	0	0	1	DOWN	1.0
0	0	1	0	DOWN	1.25
0	0	1	1	DOWN	1.5
0	1	0	0	DOWN	1.75
0	1	0	1	DOWN	2.0
0	1	1	0	DOWN	2.5
0	1	1	1	DOWN	3.0

SS3	SS2	SS1	SS0	Spread Mode	Spread Amount %
1	0	0	0	Center	+/- 0.3
1	0	0	1	Center	+/- 0.4
1	0	1	0	Center	+/- 0.5
1	0	1	1	Center	+/- 0.6
1	1	0	0	Center	+/- 0.8
1	1	0	1	Center	+/- 1.0
1	1	1	0	Center	+/- 1.25
1	1	1	1	Center	+/- 1.5

# SO-DIMMO



Place one cap close to every 2 pullup resistors terminated to 0.9VDDT\_DDRII

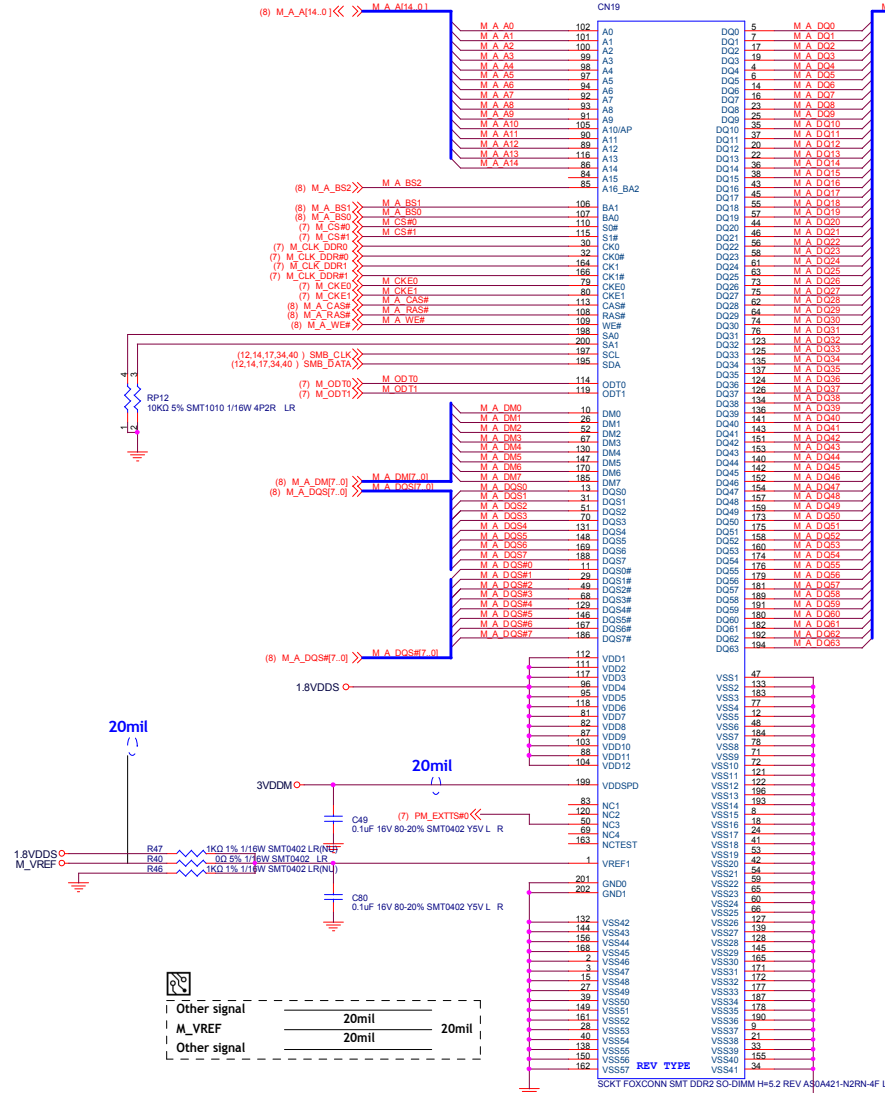
40 mils



Place these 0.1uF caps near So-Dimm0 pin79-pin15 area

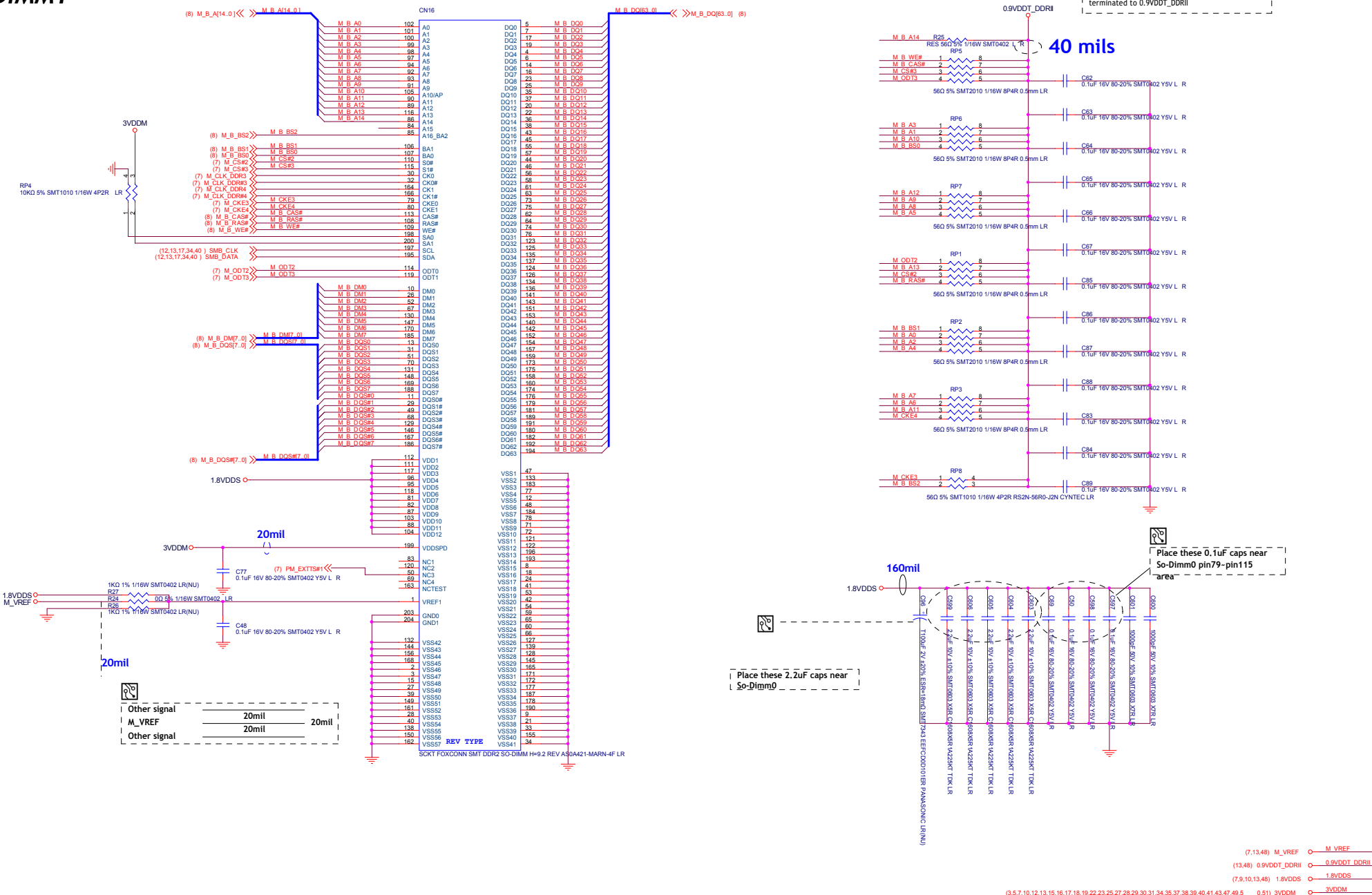


Place these 2.2uF caps near So-Dimm0

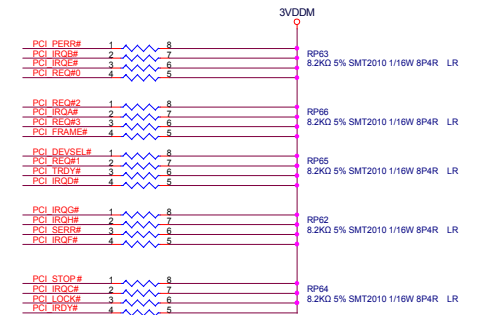


Other signal	20mil	20mil
M_VREF	20mil	20mil
Other signal	20mil	20mil

- (7,14,48) M\_VREF 0.1uF
- (14,48) 0.9VDDT\_DDRII 0.1uF
- (7,9,10,14,48) 1.8VDDOS 0.1uF
- (3,5,7,10,12,14,15,16,17,18,19,22,23,25,27,28,29,30,31,34,35,37,38,39,40,41,43,47,49,5) 3VDDOM 0.1uF

**SO-DIMM1**



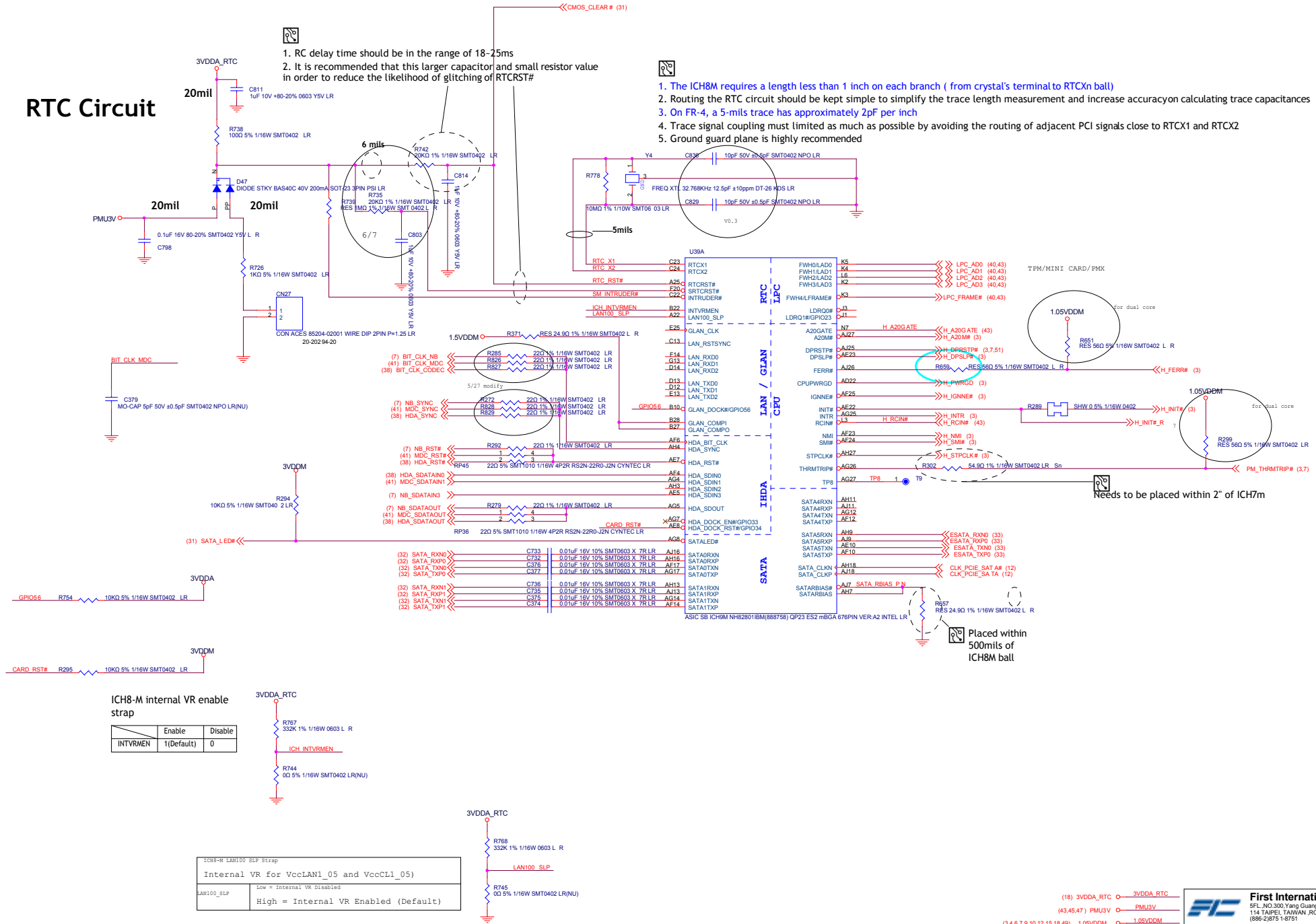


A16 swap override Strap	
PCI_GNT#3	Low = A16 swap override enabled High = Default

## RTC Circuit

1. RC delay time should be in the range of 18-25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

1. The ICH8M requires a length less than 1 inch on each branch ( from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended



ICH8-M internal VR enable strap

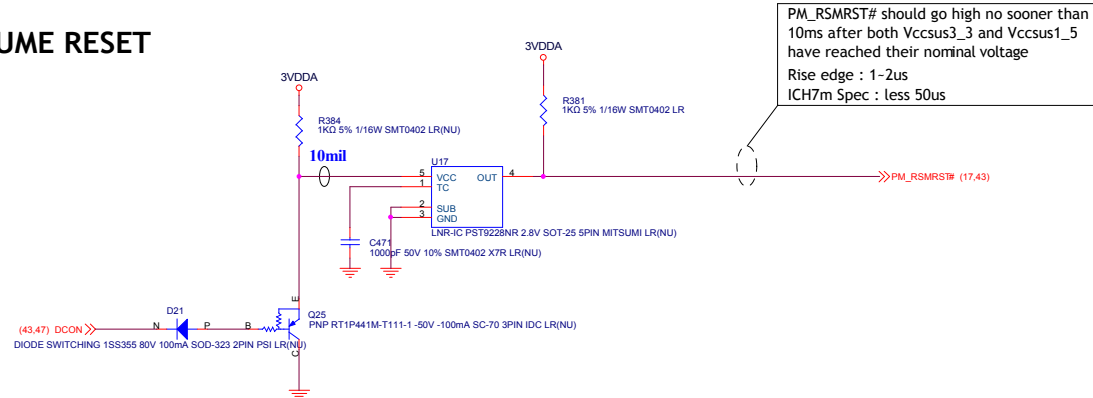
	Enable	Disable
INTVRMEN	1(Default)	0

IC98-W LAN100 SLP Strap	
Internal VR for VccLAN1_05 and VccCL1_05)	
LAN100_SLP	Low = Internal VR Disabled
	High = Internal VR Enabled (Default)

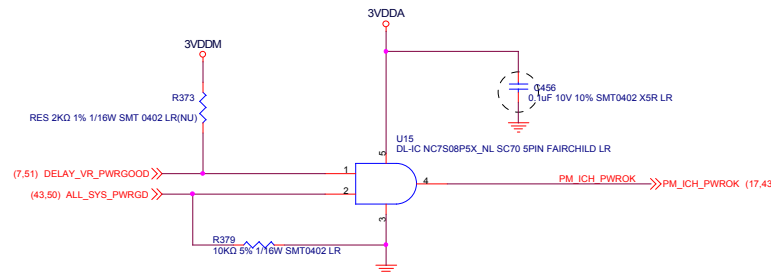
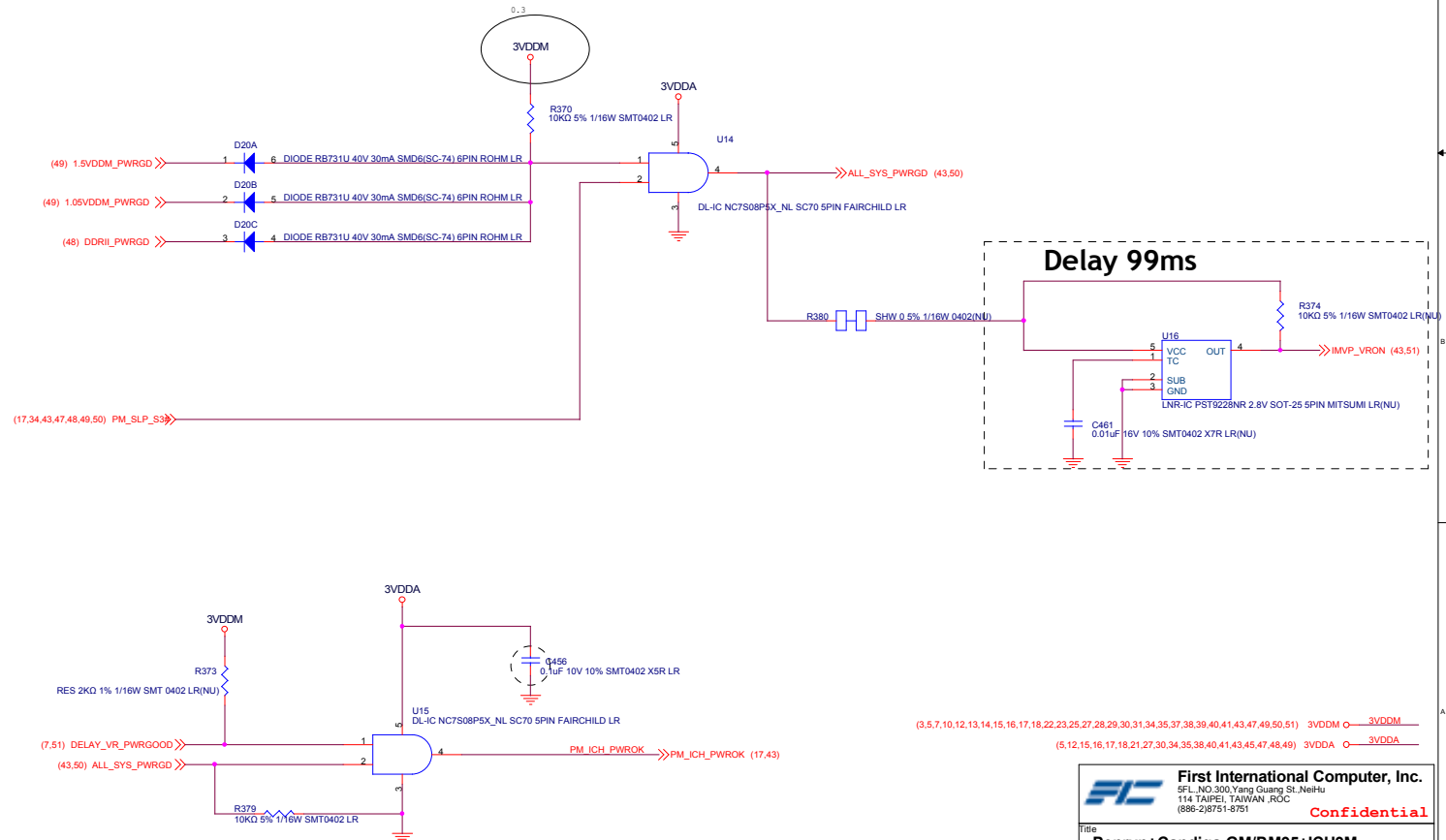




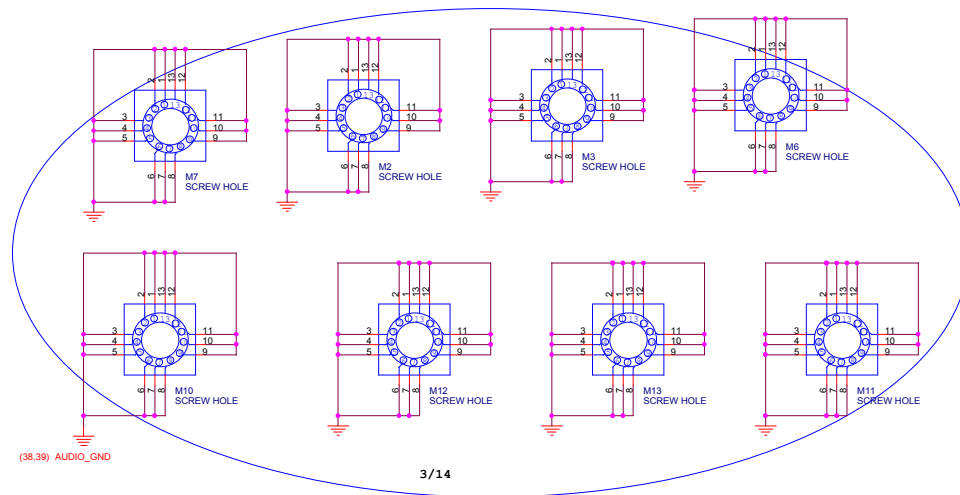
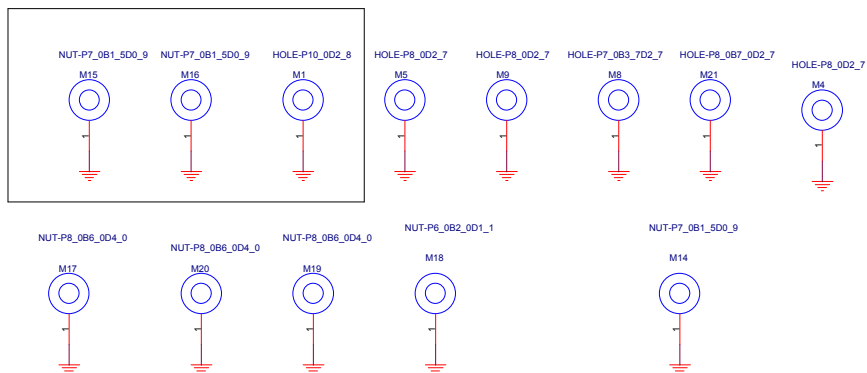
## RESUME RESET



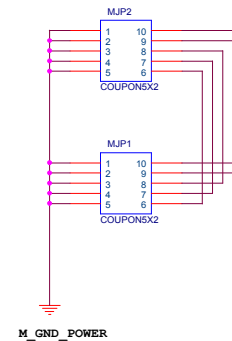
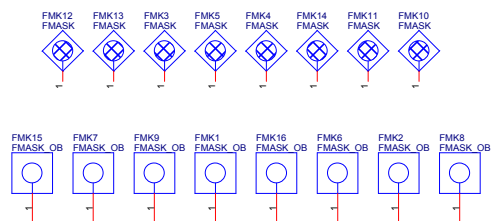
## NAPA Platform Power Good Circuit



3/27 modify

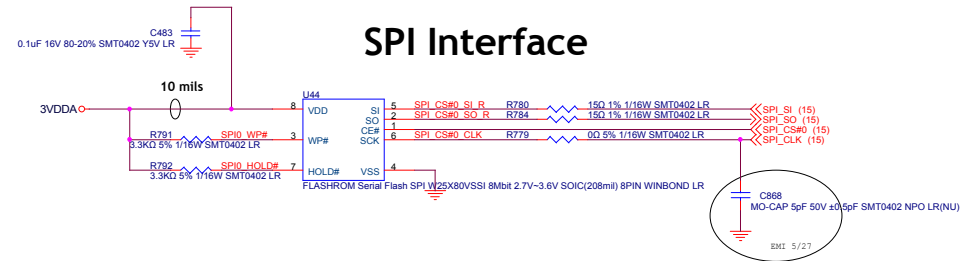


## COUPON 4X2





## SPI Interface



(5,12,15,16,17,18,19,27,30,34,35,38,40,41,43,45,47,48,49) 3VDDA 3VDDA

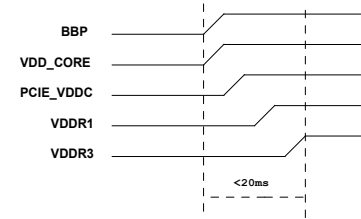
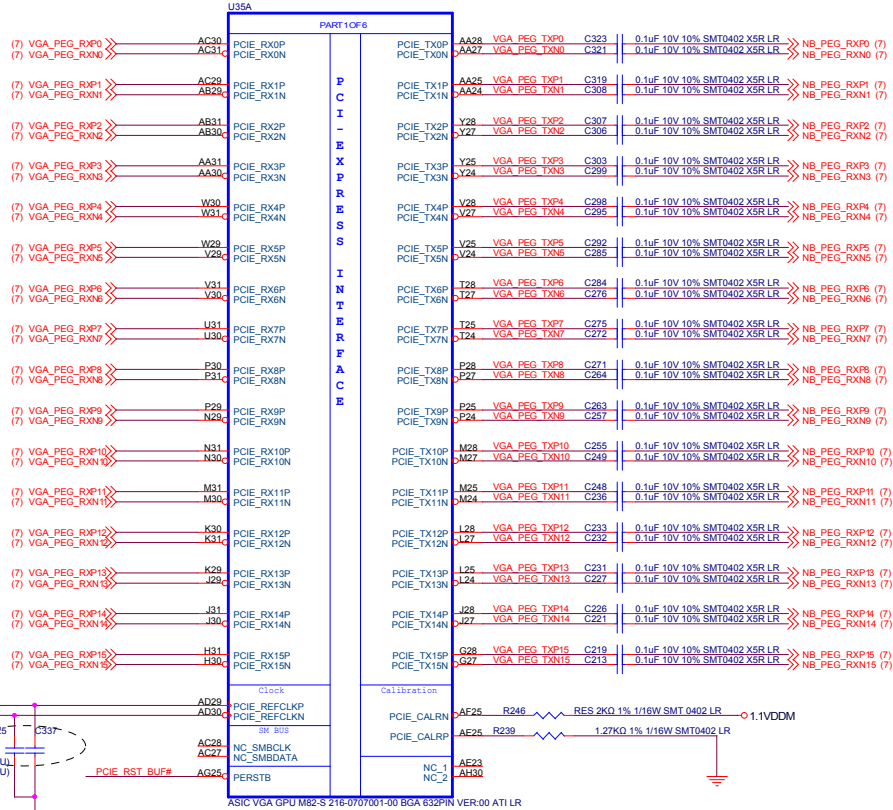
# PCI-E LAYOUT GUIDE

Trace Length	Group Mismatch	Space
L<12"	<5mil	20:5:7:5:20 (L1,L6) 20:4:7:4:20 (L3,L4)

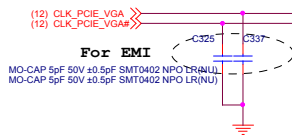
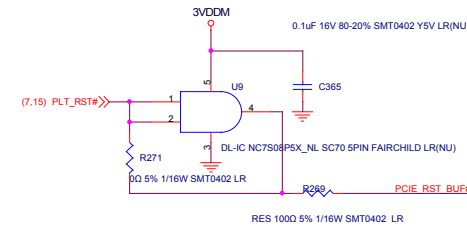
PCI-E clock must 100 ohms  
 PCI-E Trace length CONN to ATI chip L<3"  
 PCI-E data & control signals 5:20  
 PCI-E differential strobe pair  
 20:5:7:5:20

## PCI-E Clock Layout and Routing Guidelines

PCI-E CLK	Clock --> NB&VGA	5 mils/20 mils	20:5:5:5:20
PCI Express Bus Interface			
Pin Group	ADDRESS DATA & COMMAND		
	PWRGD & PWRGD_MASK		
PCI Express Reference Clocks	PCIE_REFCLKP & PCIE_REFCLKN		
PCI Express Module 0	PCIE_TX[3:0]P & PCIE_TX[3:0]N		
	PCIE_RX[3:0]P & PCIE_RX[3:0]N		
PCI Express Module 1	PCIE_TX[7:4]P & PCIE_TX[7:4]N		
	PCIE_RX[7:4]P & PCIE_RX[7:4]N		
PCI Express Module 2	PCIE_TX[11:8]P & PCIE_TX[11:8]N		
	PCIE_RX[11:8]P & PCIE_RX[11:8]N		
PCI Express Module 3	PCIE_TX[15:12]P & PCIE_TX[15:12]N		
	PCIE_RX[15:12]P & PCIE_RX[15:12]N		
PCI Express Calibration Macro	PCIE_CALRN & PCIE_CALRP & PCIE_CALI		

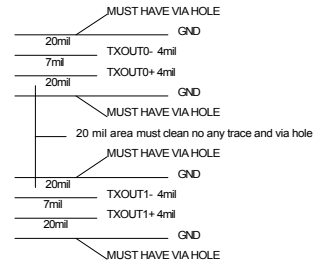


	M82S
VDD_CORE	0.95~1.1V
1.1VDDM	1.2V
VDDR1	1.8V
VDDR3	3.3V

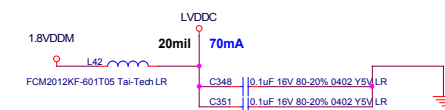
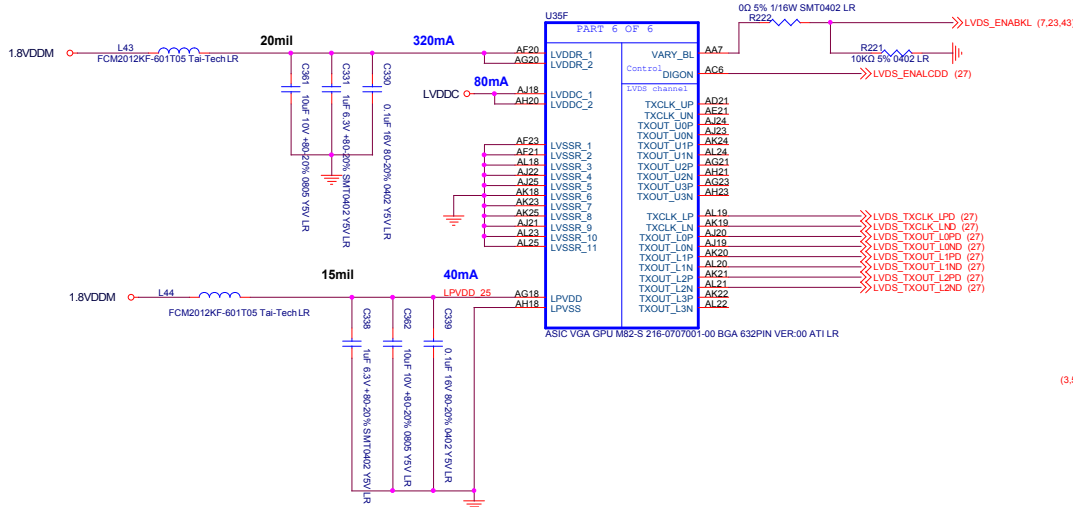


The trace length of TXOUT0- should be equal to TXOUT0+  
 The trace length of TXOUT1- should be equal to TXOUT1+  
 The trace length of TXOUT2- should be equal to TXOUT2+  
 The trace length of TXCLK- should be equal to TXCLK+

Mismatch between TXCLK+/- and TXOUT+/- not exceed 25 mil



## LVDS Interface

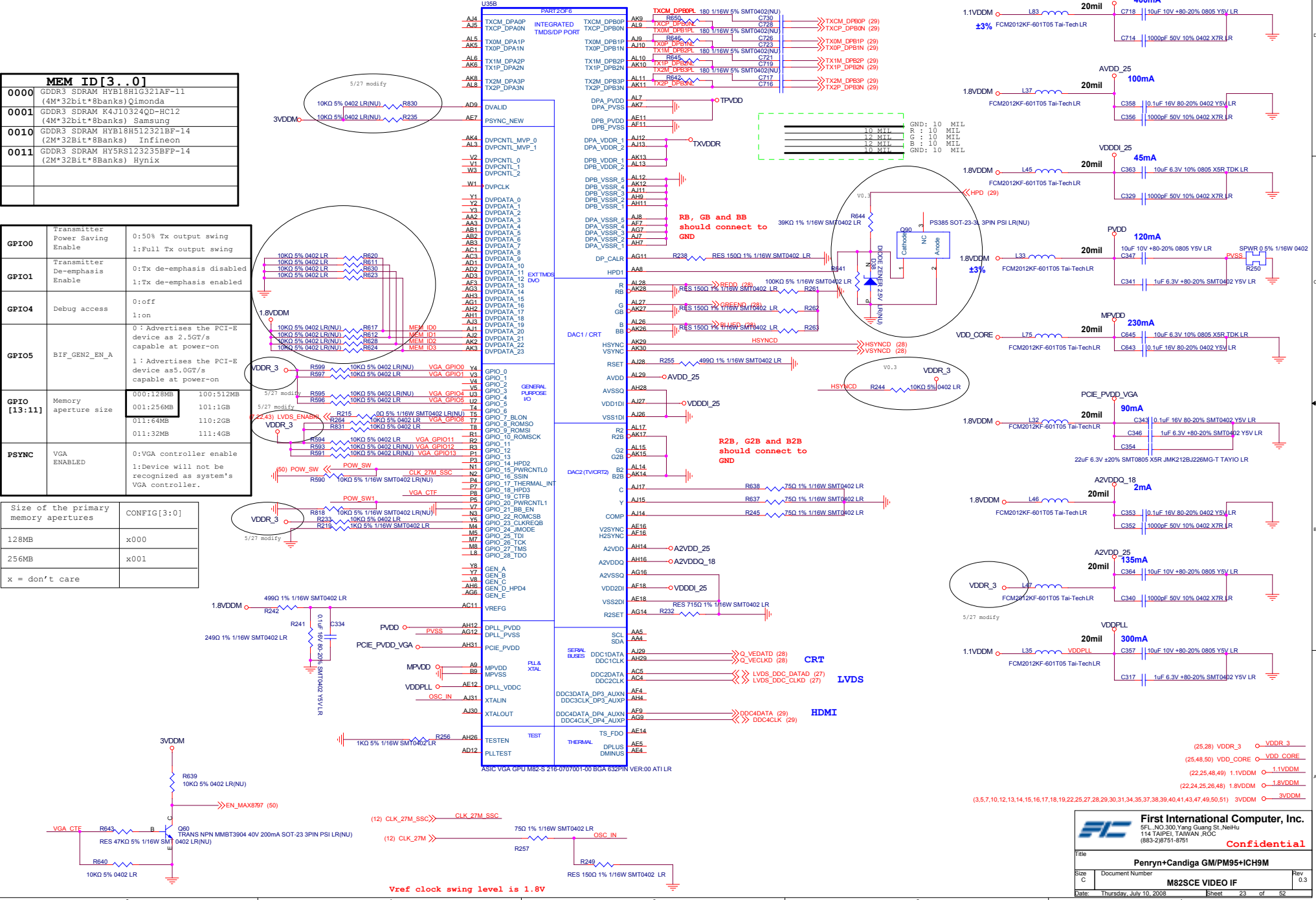


(23,25,48,49) 1.1VDDM 1.1VDDM  
 (23,24,25,26,48) 1.8VDDM 1.8VDDM  
 (3,5,7,10,12,13,14,15,16,17,18,19,23,25,27,28,29,30,31,34,35,37,38,39,40,41,43,47,49,50,51) 3VDDM 3VDDM

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5FL NO.300,Yang Guang St.,NaiHu 114 TAIPEI, TAIWAN, R.O.C (886)28751-8751	
<b>Confidential</b>	
Title Penryn+Candiga GM/PM95+ICH9M	
Size C	Document Number M82SCE PCI-E / LVDS IF
Date Thursday, July 10, 2008	Sheet 22 of 52


<b>GPI00</b>	Transmitter Power Saving Enable	0:50% Tx output swing 1:Full Tx output swing
<b>GPI01</b>	Transmitter De-emphasis Enable	0:Tx de-emphasis disabled 1:Tx de-emphasis enabled
<b>GPI04</b>	Debug access	0:off 1:on
<b>GPI05</b>	BIF_GEN2_EN_A	0: Advertises the PCI-E device as 2.5GT/s capable at power-on 1: Advertises the PCI-E device as 5.0GT/s capable at power-on
<b>GPI0 [13:11]</b>	Memory aperture size	000:128MB      100:512MB 001:256MB      101:1GB 011:64MB      110:2GB 011:32MB      111:4GB
<b>PSYNC</b>	VGA ENABLED	0:VGA controller enable 1:Device will not be recognized as system's VGA controller.

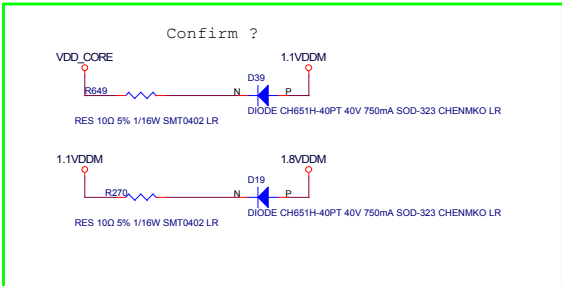
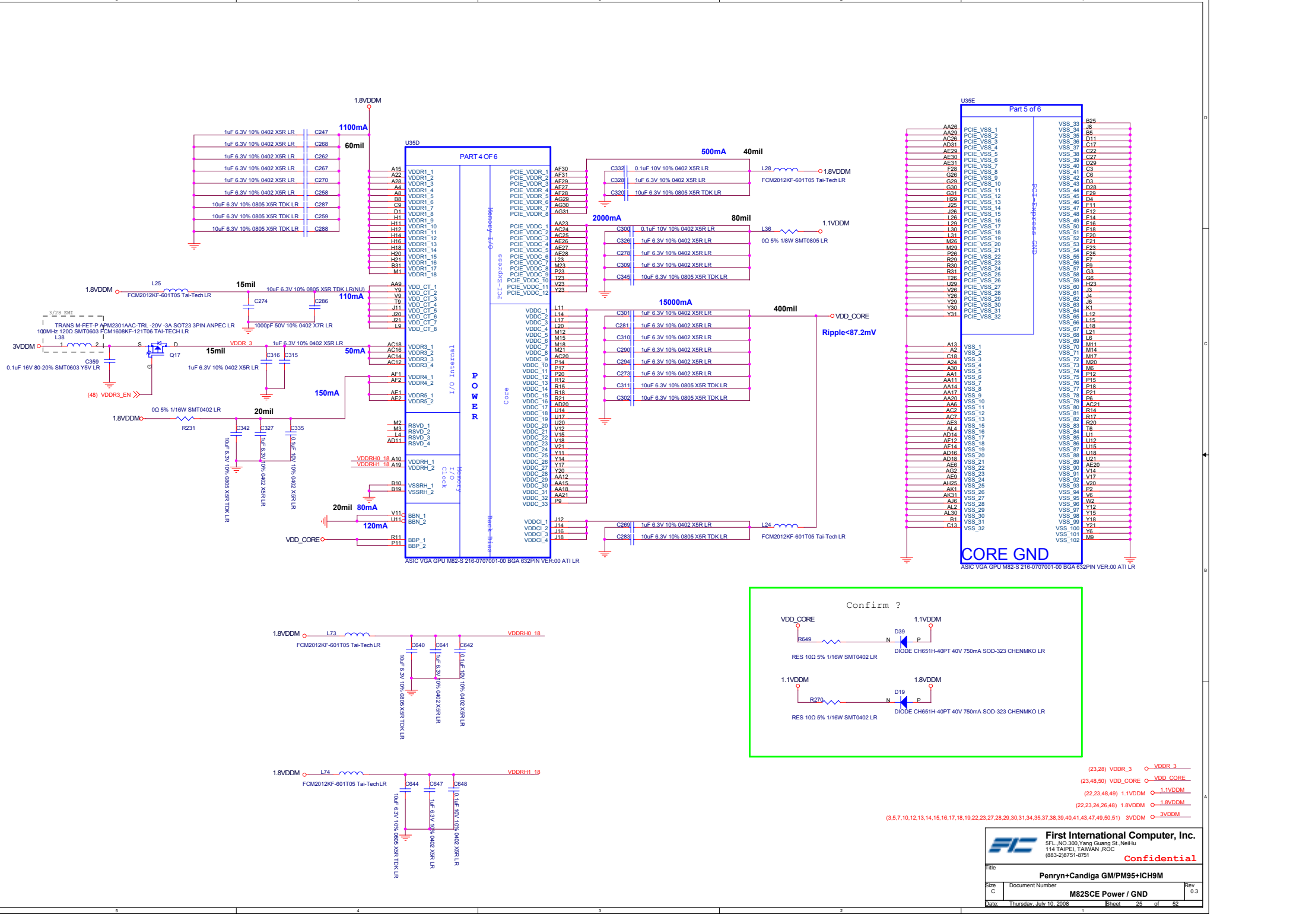
Size of the primary memory apertures	CONFIG[3:0]
128MB	x000
256MB	x001
x = don't care	





(22.23,25,26,48) 1.8VDOM ○ 1.8VDOM

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<b>Penryn+Candiga GM/PM95+ICH9M</b>		
Size C	Document Number	Rev 0.3
<b>M82SCSE Memory 2F</b>		
Date:	Thursday, July 10, 2008	Sheet 24 of 52



(23.28) VDD\_3    VDD\_3  
(23.48,50) VDD\_CORE    VDD\_CORE  
(22.23,48,49) 1.1VDD    1.1VDD  
(22.23,24,26,48) 1.8VDD    1.8VDD  
(3.5,7,10,12,13,14,15,16,17,18,19,22,23,27,28,29,30,31,34,35,37,38,39,40,41,43,47,49,50,51) 3VDD    3VDD

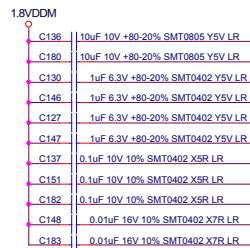
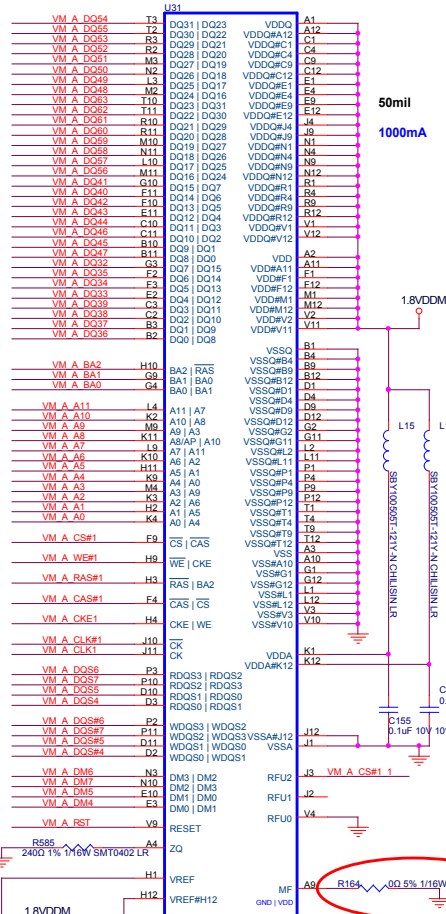
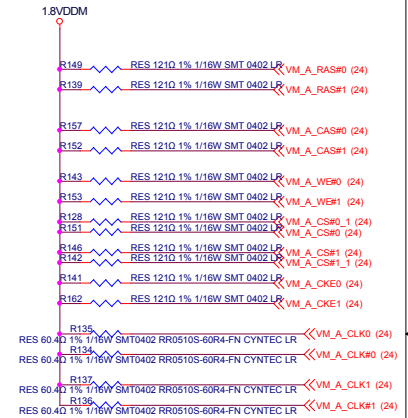
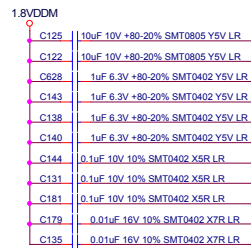
VM\_A\_DQS[63..0] <<>> VM\_A\_DQ[63..0] (24)


VM\_A\_A[11..0] <<>> VM\_A\_A[11..0] (24)

VM\_A\_DQS#[7..0] <<>> VM\_A\_DQS#[7..0] (24)

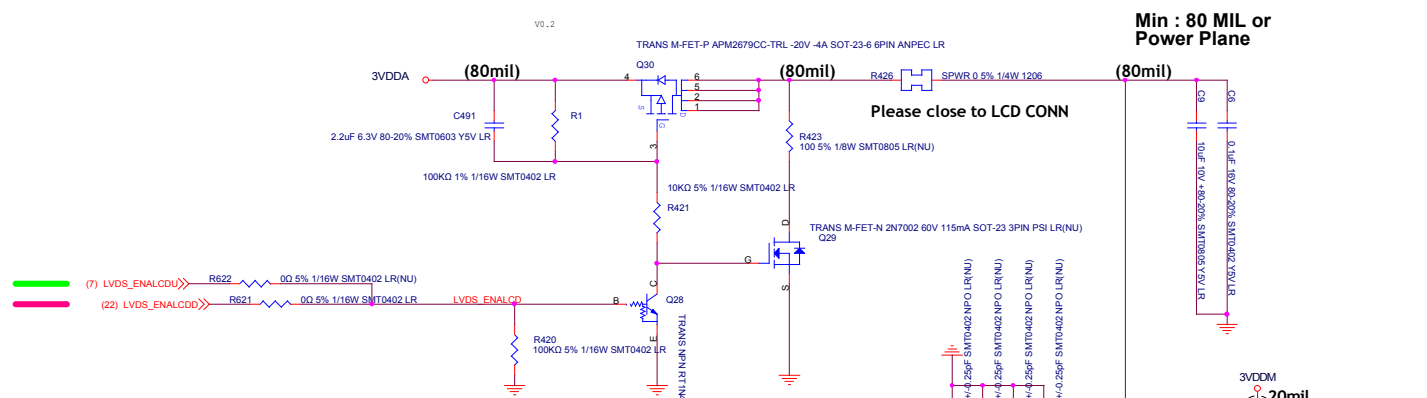
VM\_A\_DQS[7..0] <<>> VM\_A\_DQS[7..0] (24)

VM\_A\_DM[7..0] <<>> VM\_A\_DM[7..0] (24)

[illegible]

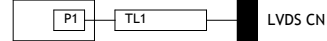
 <b>First International Computer, Inc.</b> 5FL NO.300, Yang Guang St., NeiHu 114 TAIPEI TAIWAN ROC (886-2)8751-8751		<b>Confidential</b>
Title <b>Penryn+Candiga GM/PM95+ICH9M</b>		
Size C	Document Number	Rev 0.3
<b>VRAM GDDR3</b>		
Date:	Thursday, July 10, 2008	Sheet 26 of 52





LVDS Signal Group Routing Guideline

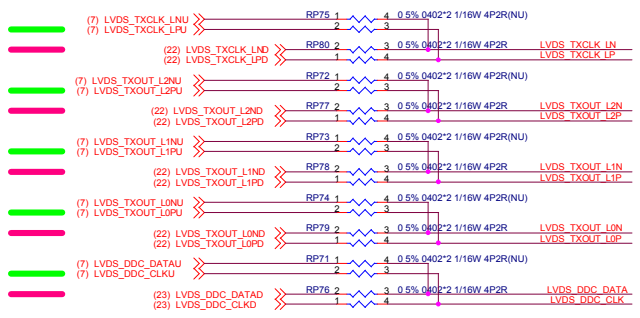
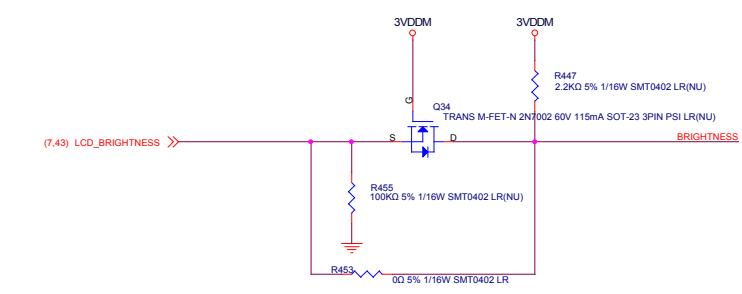
GMCH




Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Differential Mode Impedance	100 +/- 20%
Nominal Trace Width	4 mils
Nominal Pair Spacing (Edge to edge)	7 mils
Minimum Pair-to-Pair Spacing	20 mils
Minimum Serpentine Spacing	20 mils
Minimum Spacing to Other LVDS	20 mils
Minimum Isolation Spacing to non-LVDS	20 mils
Maximim Via Count	2 (per line)
Package Length Range - P1	750 mils +/- 250 mils
Total MB Length - TL1	Max = 10"
Length Matching with Pair	Matching to within +/- 20mils
Clock to Data Length Matching (Total Length)	Matching Data to Clock within +/- 20mils
Clock A to Clock B Length Matching	Match Clock A to B within +/- 20mils
Breakout Exceptions (Reduce geometries for GMCH break-out region)	4/4 mils spacing allowed and 10 mils Pair-to-Pair spacing allowed Max. breakout length is 500 mils

\*\*\*Cable Length must be less than 16"

LCD brightness control from N.B.





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(886-2)8751-8751

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Title

Penryn+Candiga GM/PM95+CH9M

Size

C

Document Number

LCD CNN

Rev

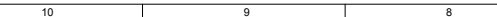
0.3

Date

Thursday, July 10, 2008

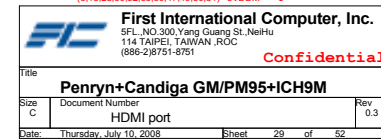
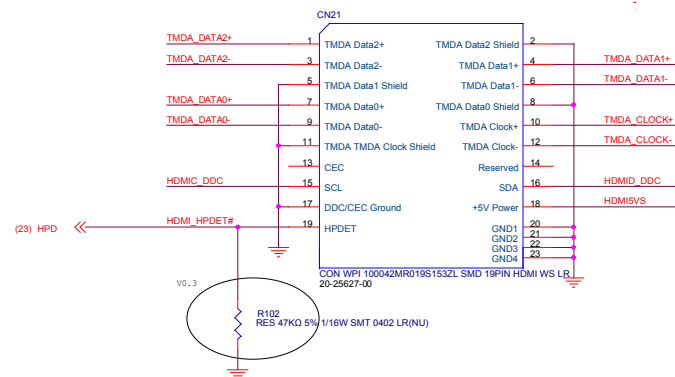
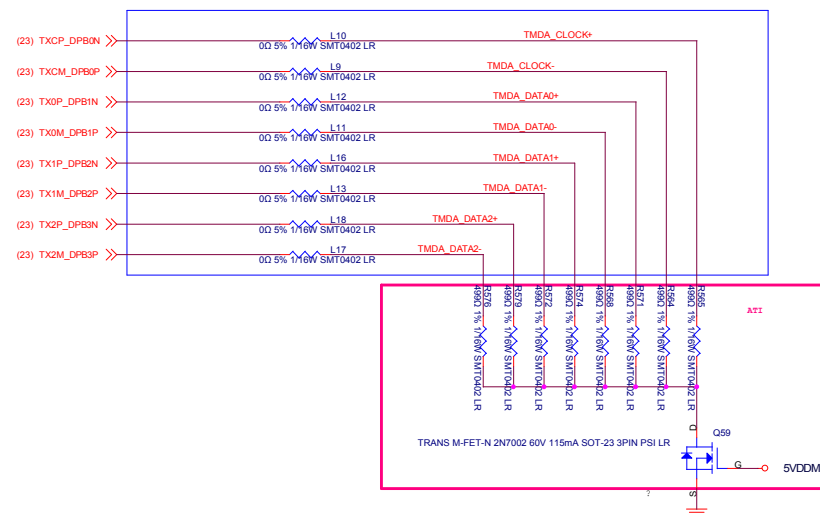
Sheet

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For VESA SPEC , R/G/B should be 665mV ~ 770mV

Title <b>Penryn+Candiga GM/PM95+ICH9M</b>		
Size <b>C</b>	Document Number <b>CRT port</b>	Rev <b>0</b>
Date: <b>Thursday, July 10, 2008</b>	Sheet <b>28 of 52</b>	

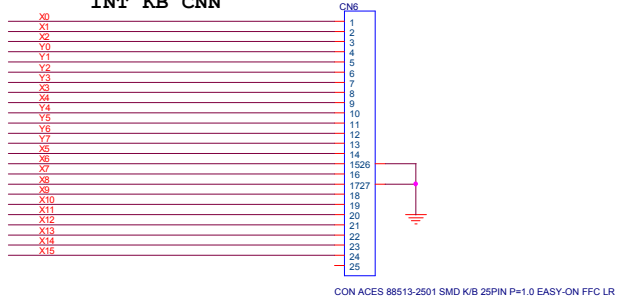


Same as CTx projects

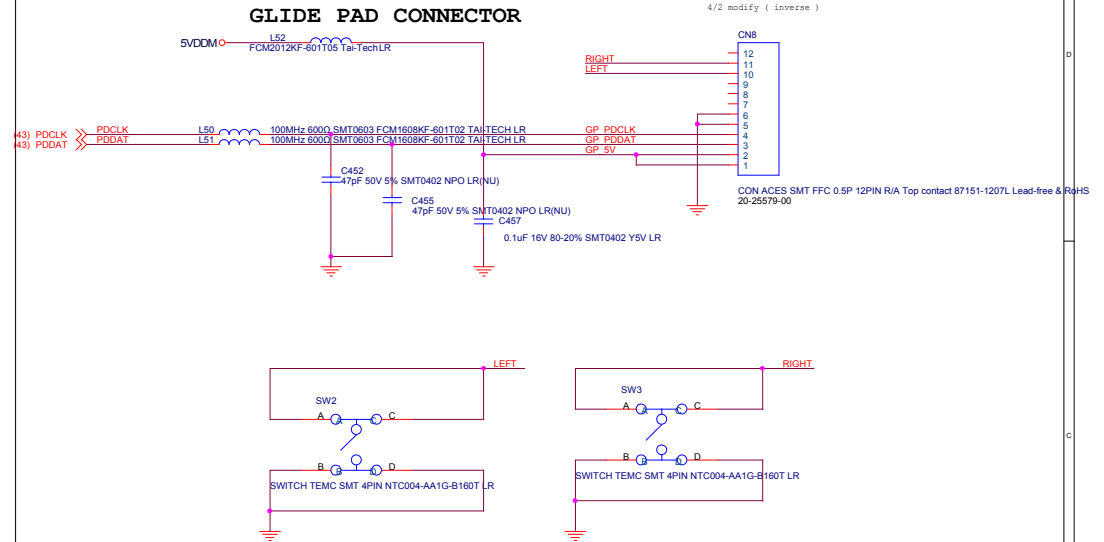
## INT KB CNN

(43) X[0..15] << X[0..15]  
(43) Y[0..7] << Y[0..7]

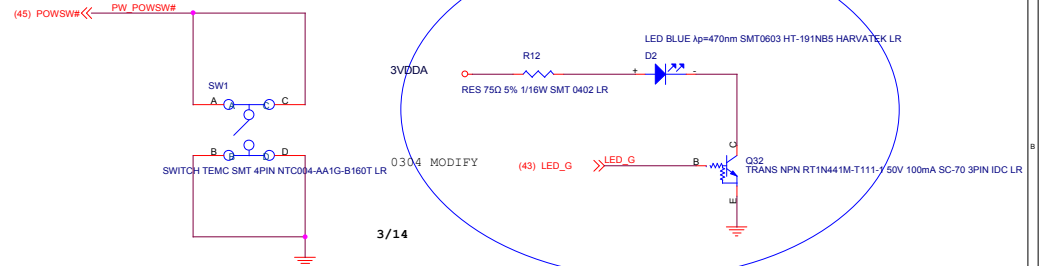
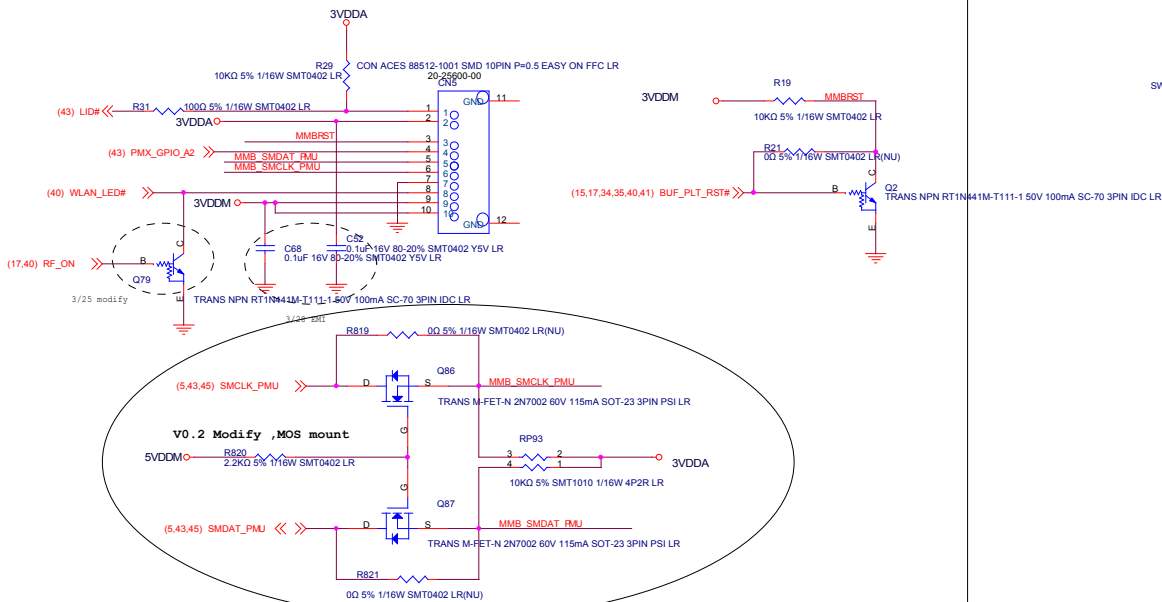
## INT KB CNN



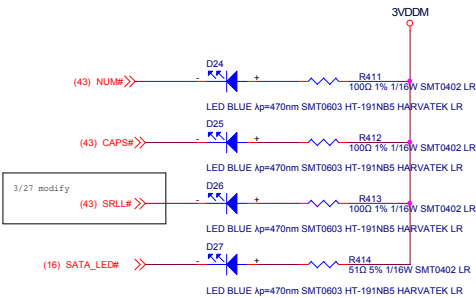
## GLIDE PAD CONNECTOR



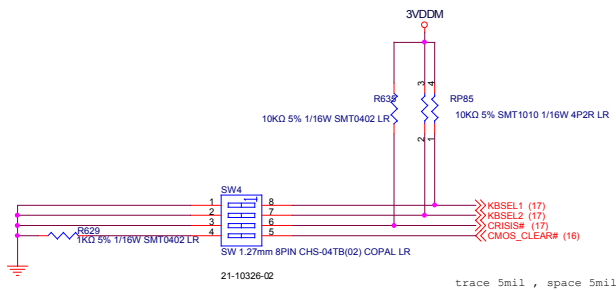
## SWITCH BOARD CONNECTOR



LED indicator control logic

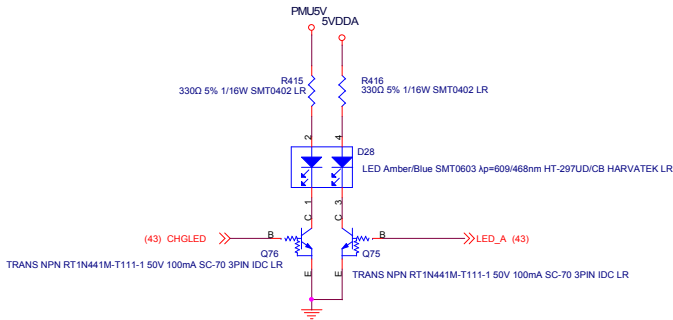


DIP SWITCH



KBSEL2	KBSEL1	
ON	ON	UK Keyboard
OFF	OFF	Reserved
OFF	OFF	JP Keyboard
OFF	OFF	US Keyboard

CRISIS#	ON	CRISIS mode
	OFF	Normal
CMOS_CLEAR#	ON	Reset RTC
	OFF	NONE



Left

Right

D24	D25	D26	D27	D28
NUM	CAP	SCR	HDD	BAT

(3,5,7,10,12,13,14,15,16,17,18,19,22,23,25,27,28,29,30,34,35,37,38,39,40,41,43,47,49,50,51) 3VDDM 3VDDM

(18,33,41,47,48) 5VDDA 5VDDA

(43,47) PMU5V PMU5V

## NOTE

SATA differential stripline 20:5:6:5:20  
 SATA differential microstripline 20:6:6:6:20  
 請包GROUND



## SATA Layout Note:

MS or SL:

6mils 6mils 6mils 6mils  
 20mils 6mils 20mils 6mils 20mils

TX

RX

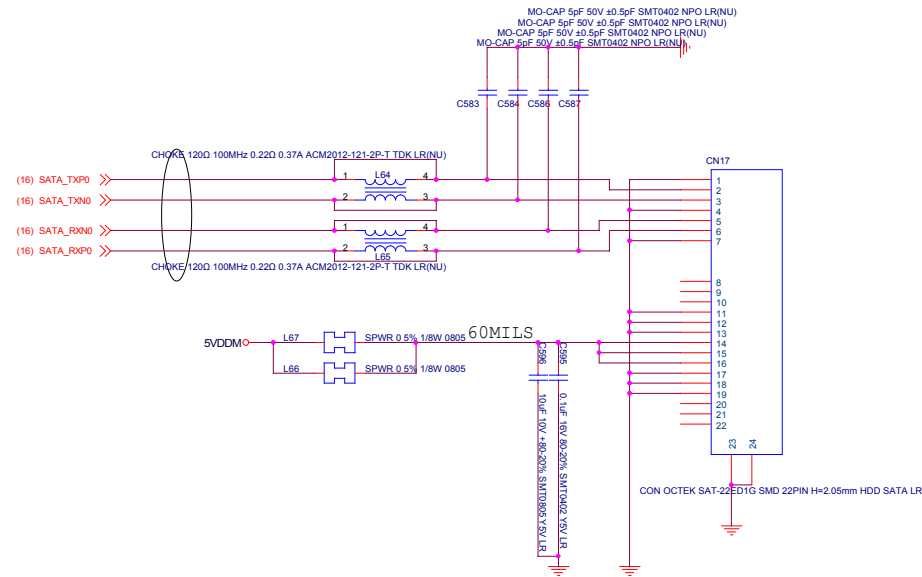
\* Zdif = 100 Ohm +/- 10%. TX & RX should refer GND.No via & stubs.The Best layer is Top.

\* TX/RX trace length < 2 inches.

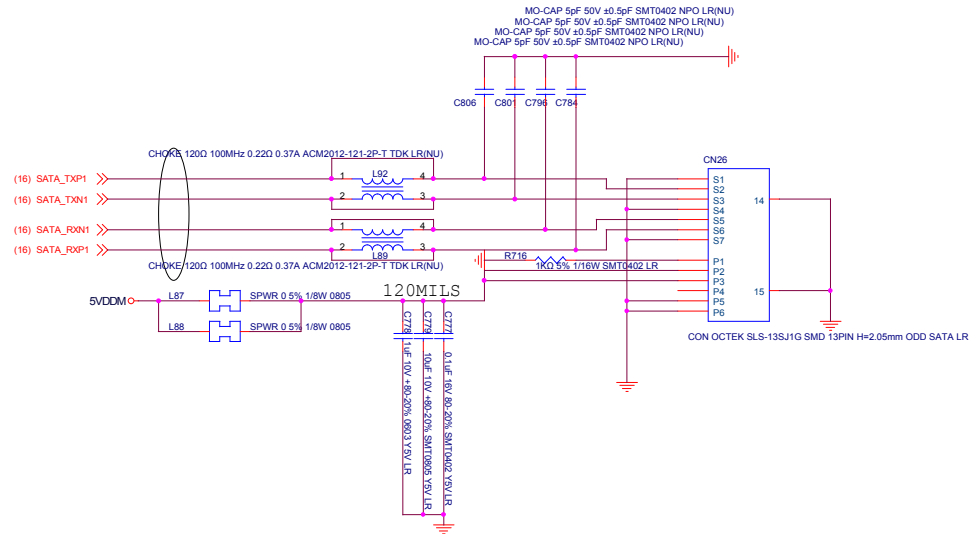
\* TX+/- need matching trace ±10 mils length.

\* RX+/- need matching trace ±10 mils length.

\* SATA Pair to Pair Trace matching trace ±10 mils length.



## CD-ROM CNN

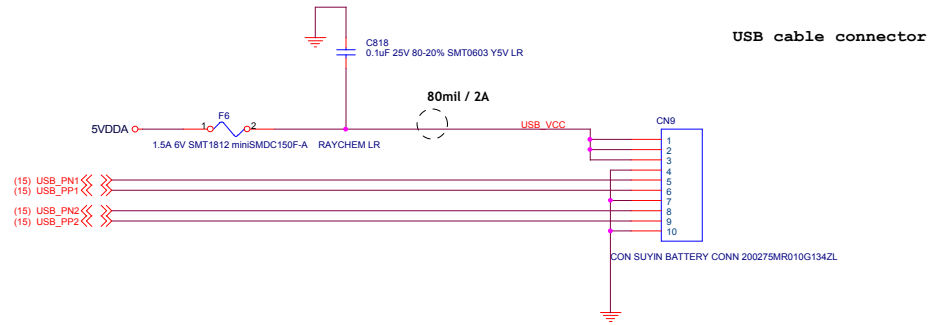


(5,18,28,29,30,38,39,47,49,50,51) 5VDDM 5VDDM

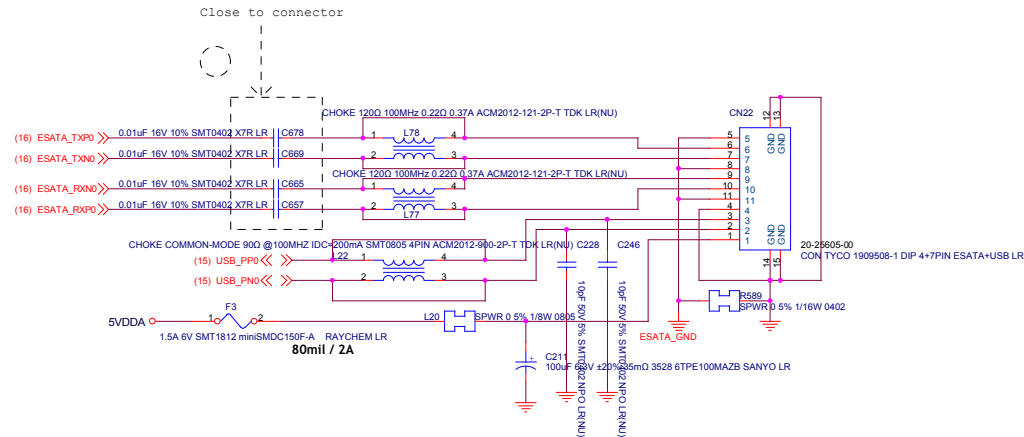
		<b>First International Computer, Inc.</b> 5FL NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN, R.O.C (886-2)8751-8751	
Title: <b>Penryn+Candiga GM/PM95+ICH9M</b>		Confidential	
Size: <b>C</b>	Document Number: <b>S-ATA HDD/ODD</b>	Rev: <b>0.3</b>	
Date: <b>Thursday, July 10, 2008</b>		Sheet: <b>32</b>	of: <b>52</b>

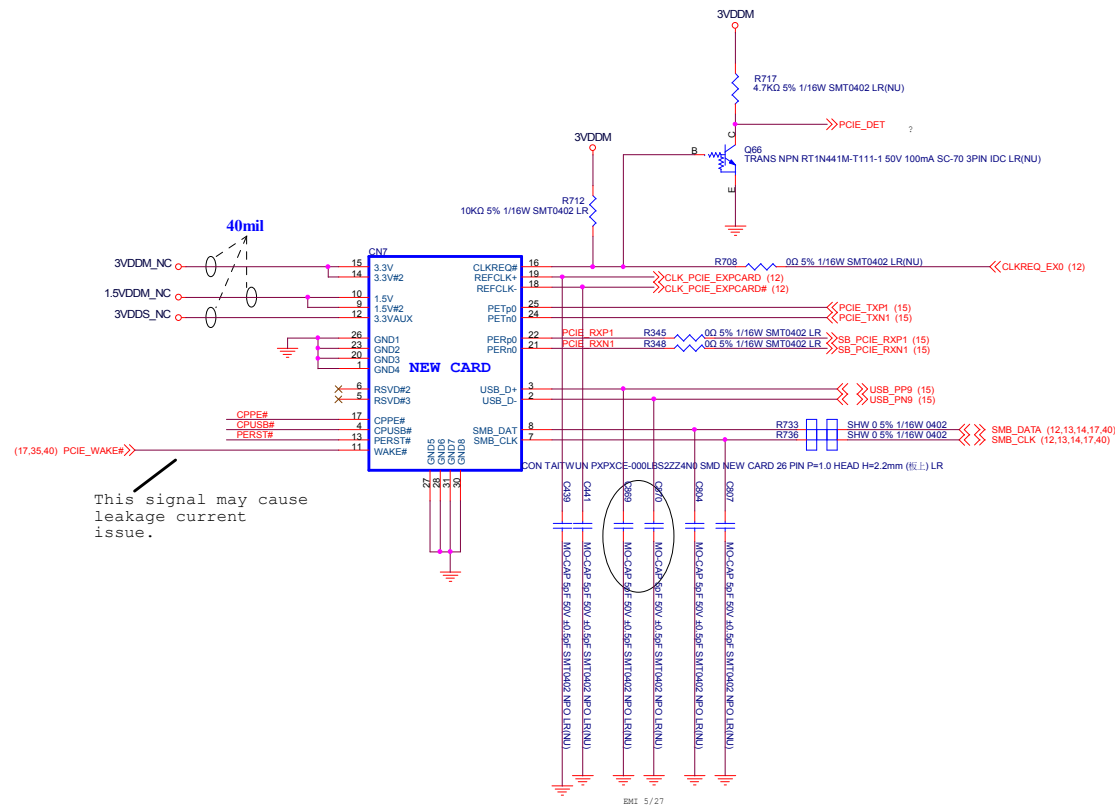
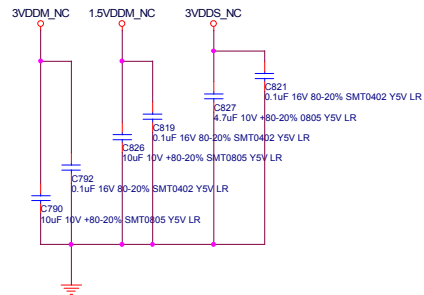
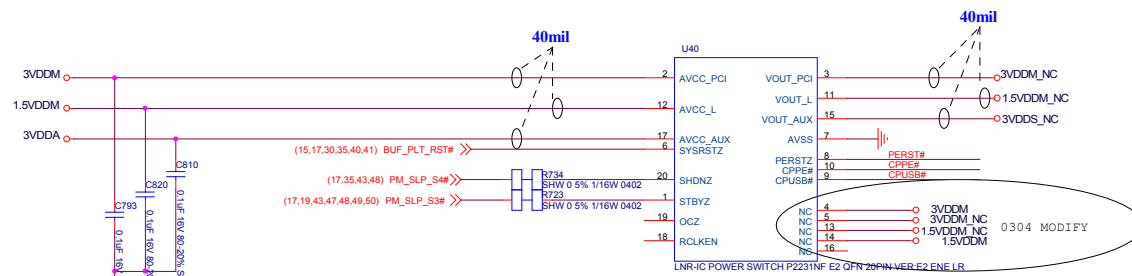


## USB Board



## E-SATA

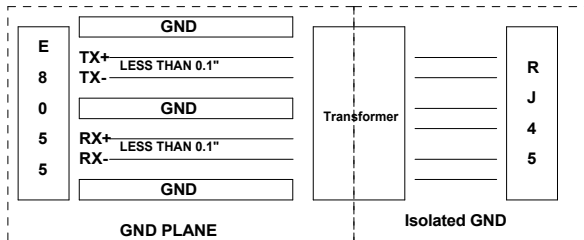




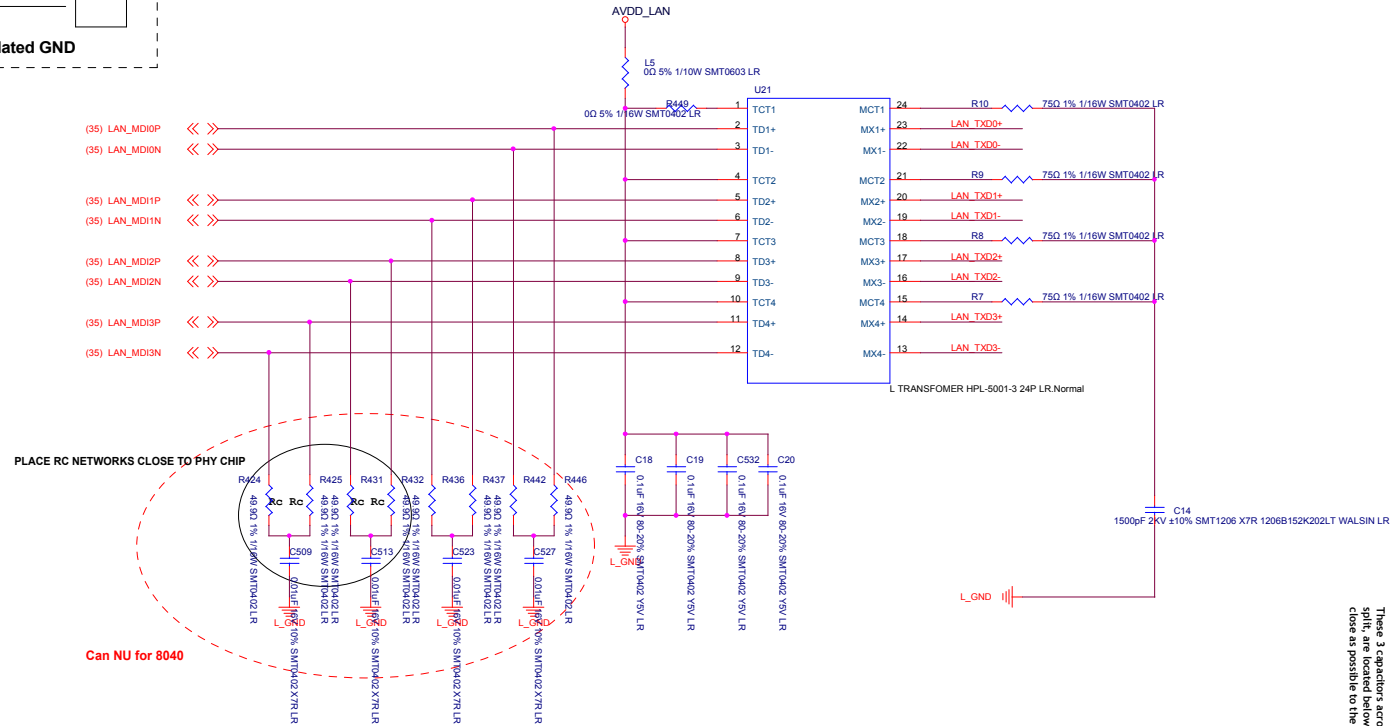
(5,12,15,16,17,18,19,21,27,30,35,38,40,41,43,45,47,48,49) 3VDDA ○ 3VDDA  
(4,9,10,15,16,18,40,41,49) 1.5VDDM ○ 1.5VDDM  
(3,5,7,10,12,13,14,15,16,17,18,19,22,23,25,27,28,29,30,31,35,37,38,39,40,41,43,47,49,50,51) 3VDDM ○ 3VDDM



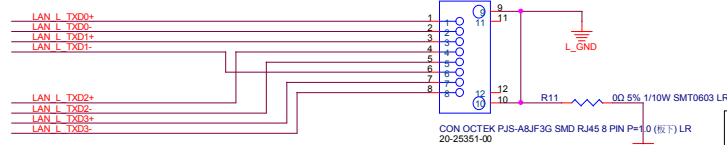
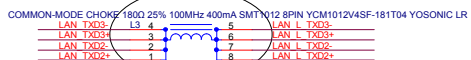
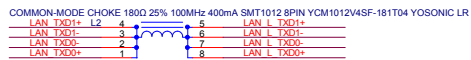
TX 100 ohm ---> trace 4 mil , space 10 mil  
RX 50 mil space from other signals  
Total Trace Length no more thans 4.8"  
2 Differential pairs must have the same length



Xa: Transformer use LFE9248(12-01904-01)  
Pa: Transformer use LFE8450(12-01905-01)

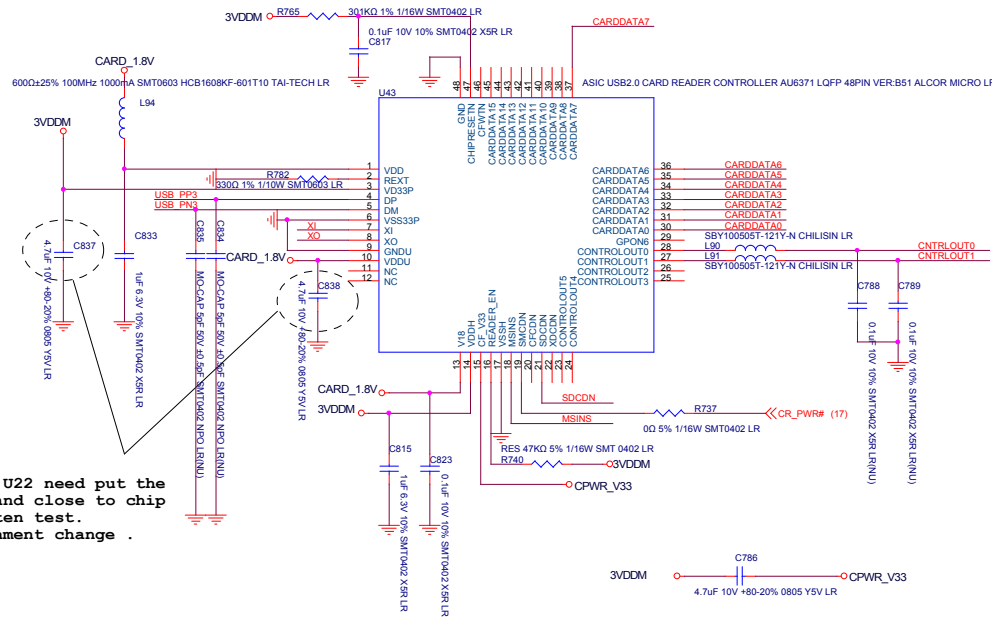


	for 88E8055	for 88E8039
Rc	STUFF	NU
La	STUFF	NU



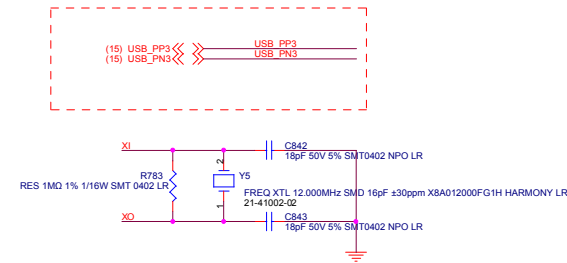
These 3 capacitors across the CHASSIS GND to GND split, are located below the magnetics module. Place as close as possible to the magnetics module.

Pa: Stuff  
Xa: No Stuff

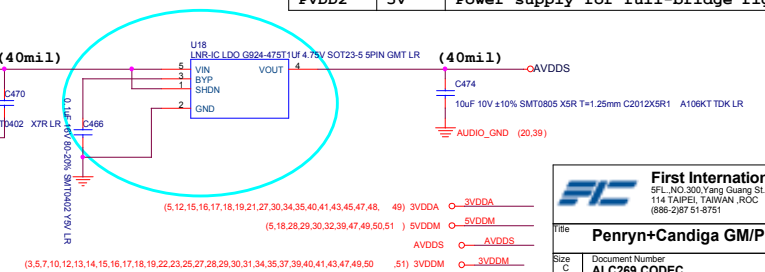


- 1.C516,C904,U22 need put the same plane and close to chip for eye-patten test.
- 2.Pin assignment change .

## INTERFACE

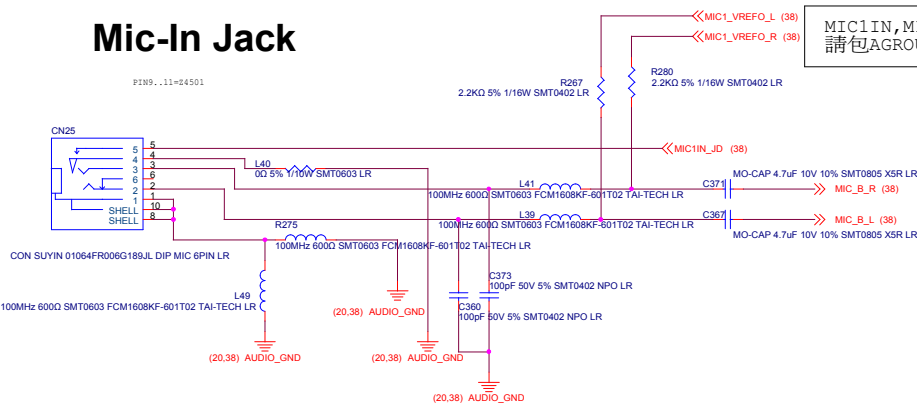


(3,5,7,10,12,13,14,15,16,17,18,19,22,23,25,27,28,29,30,31,34,35,38,39,40,41,43,47,49,50,51) 3VDDM 3VDDM





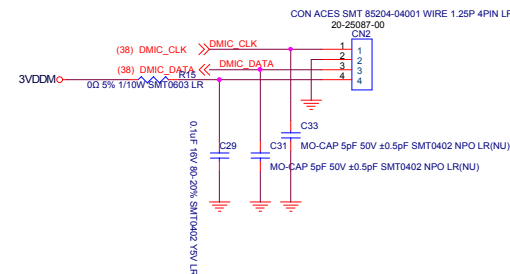
# Mic-In Jack



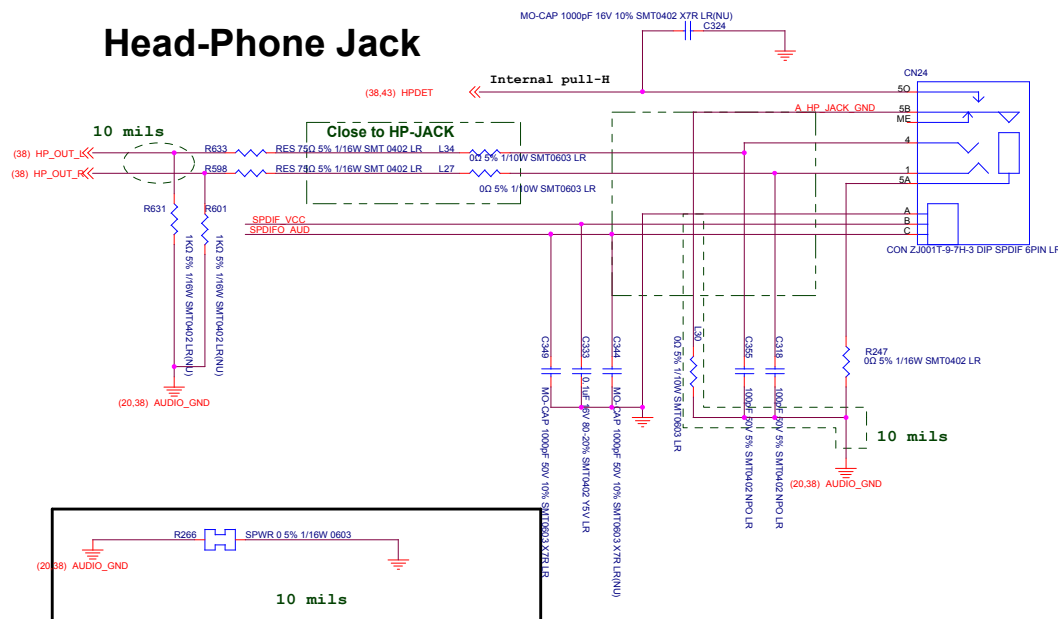
NOTE

MIC1IN, MIC2IN, INTERNAL\_MIC  
請包AGROUND

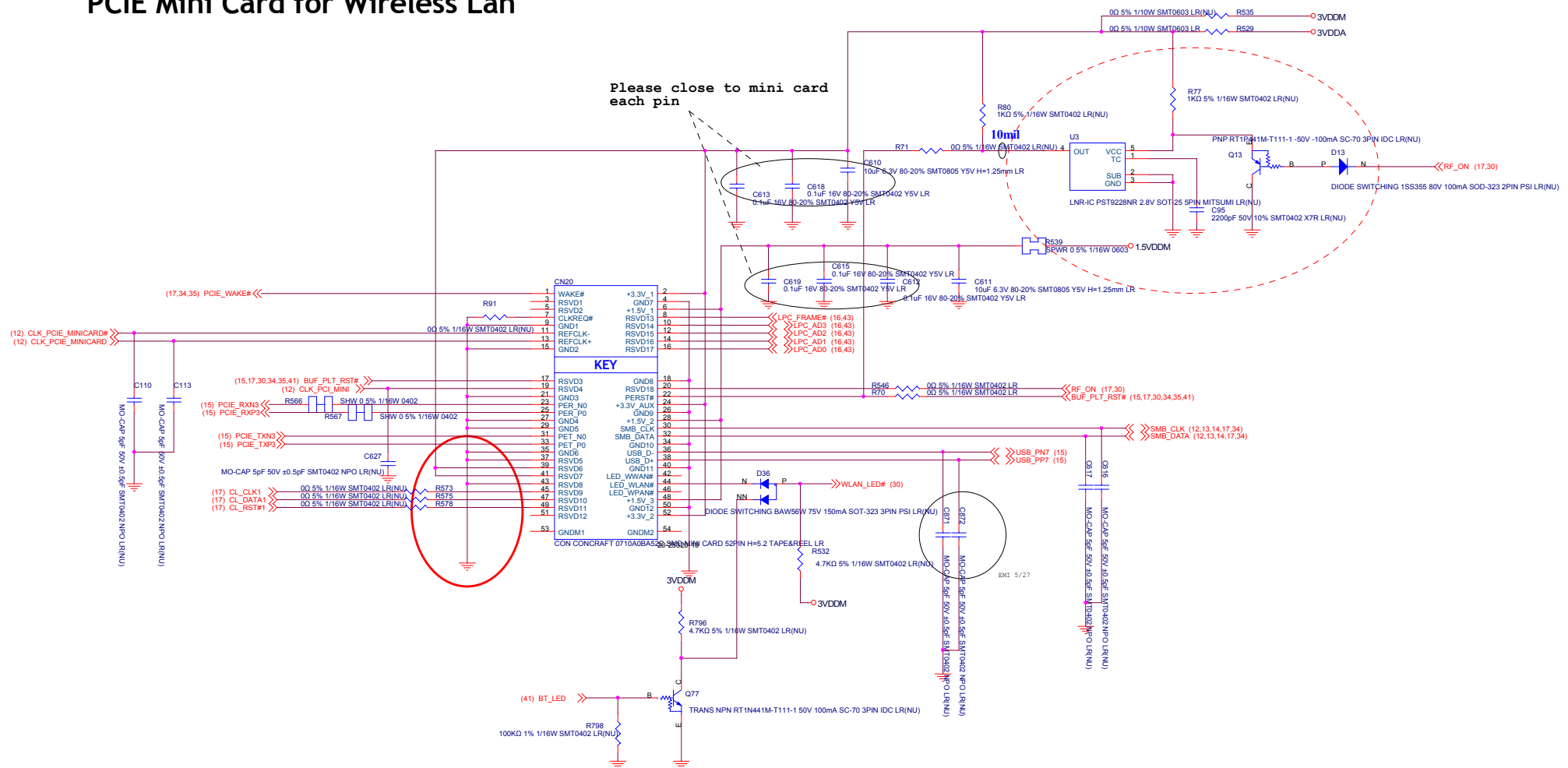
# Internal Micphone



# Head-Phone Jack



## PCIE Mini Card for Wireless Lan



(5,12,15,16,17,18,19,21,27,30,34,35,38,41,43,45,47,48,49) 3VDDA ○ 3VDDA

(5,18,28,29,30,32,38,39,47,49,50,51) 5VDDM  5VDDM

(4,9,10,15,16,18,34,41,49) 1.5VDDMO 1.5VDDM

(3,5,7,10,12,13,14,15,16,17,18,19,22,23,25,27,28,29,30,31,34,35,37,38,39,41,43,47,49,50,51) 3VDDM  3VDDM

**First International Computer, Inc.**  
5FL., NO. 300, Yang Guang St., NeiHu  
114 TAIPEI, TAIWAN, ROC

(886-2)8751-8751 **Confidential**

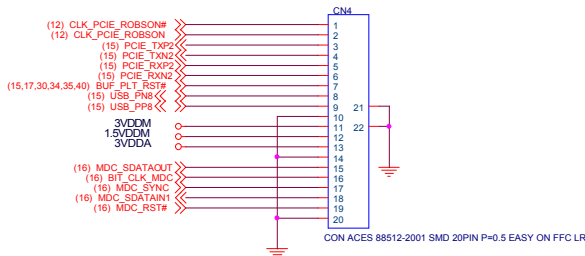
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Size	Document Number	Rev
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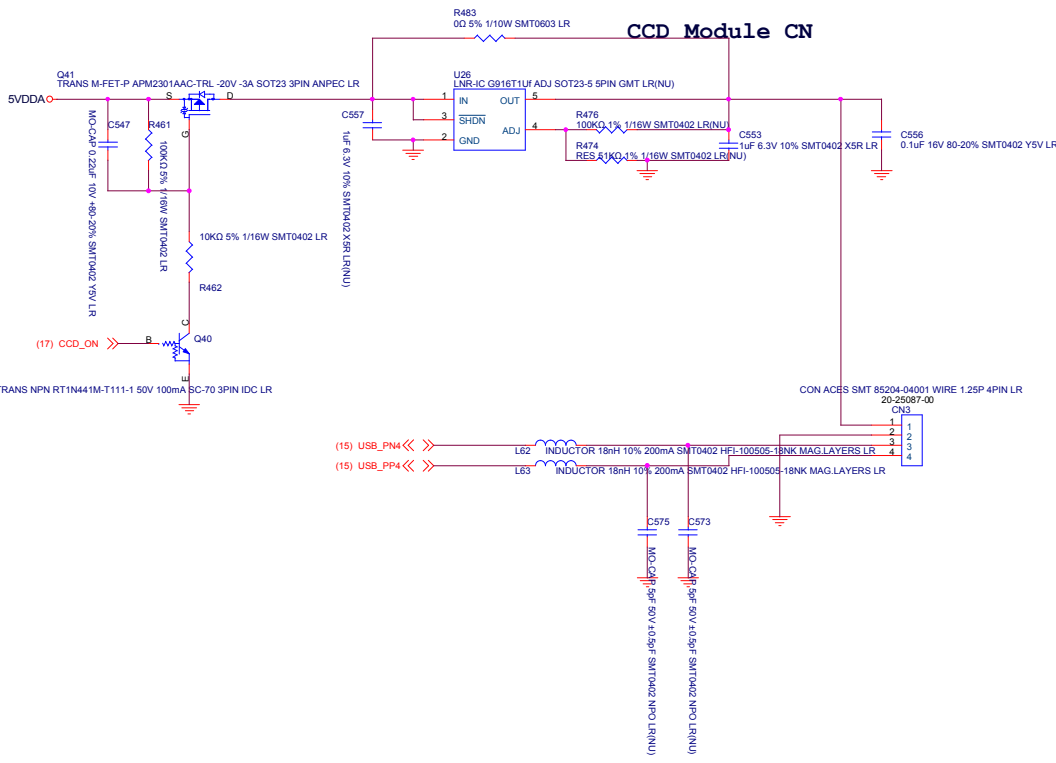
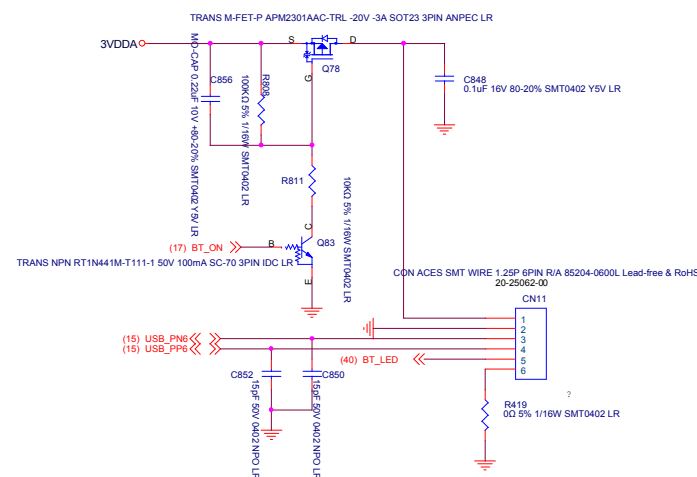
C	PCIE Mini / W-LAN	0.3
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Robson board CNN

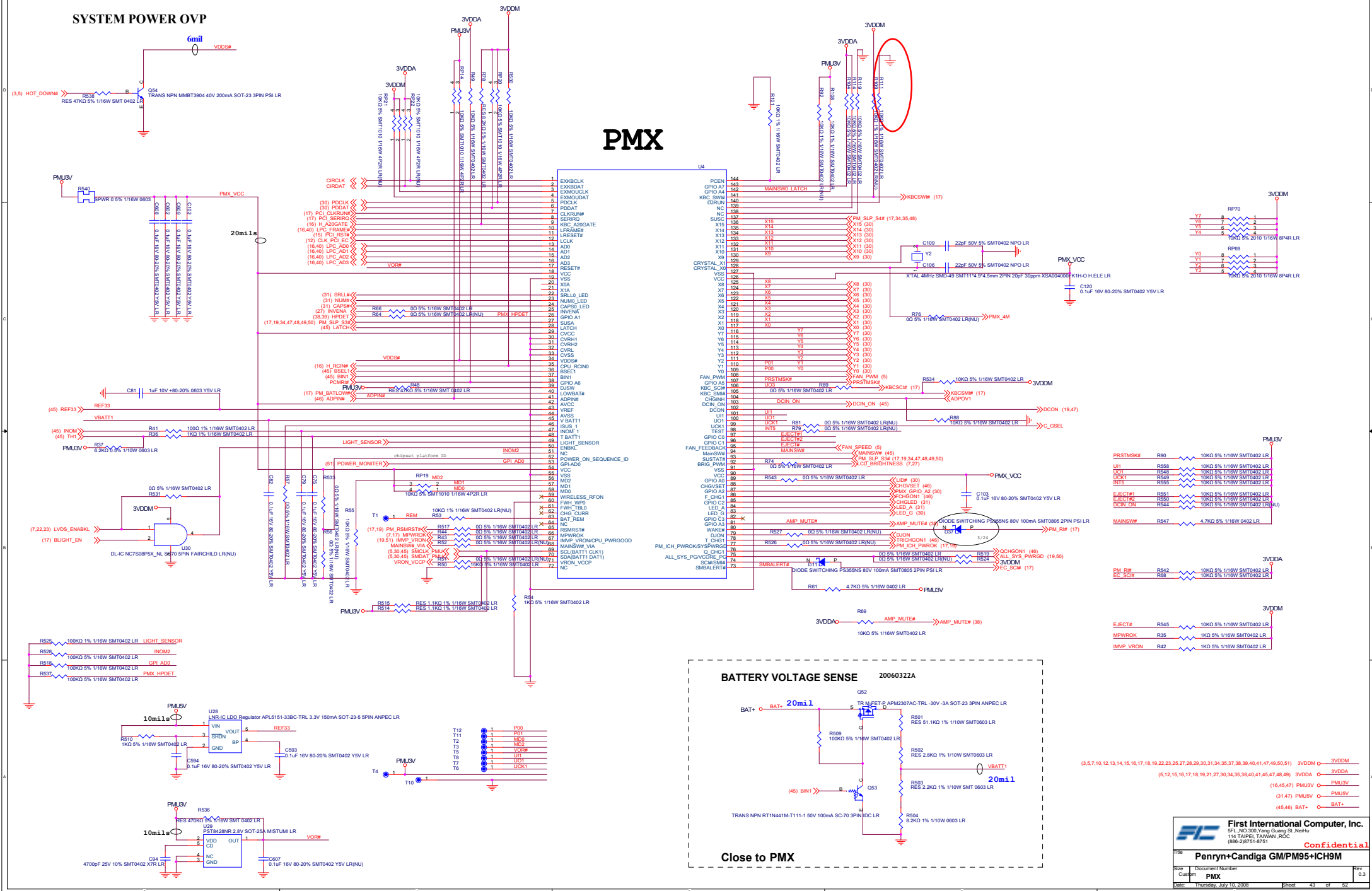


USI Bluetooth USB Module CN

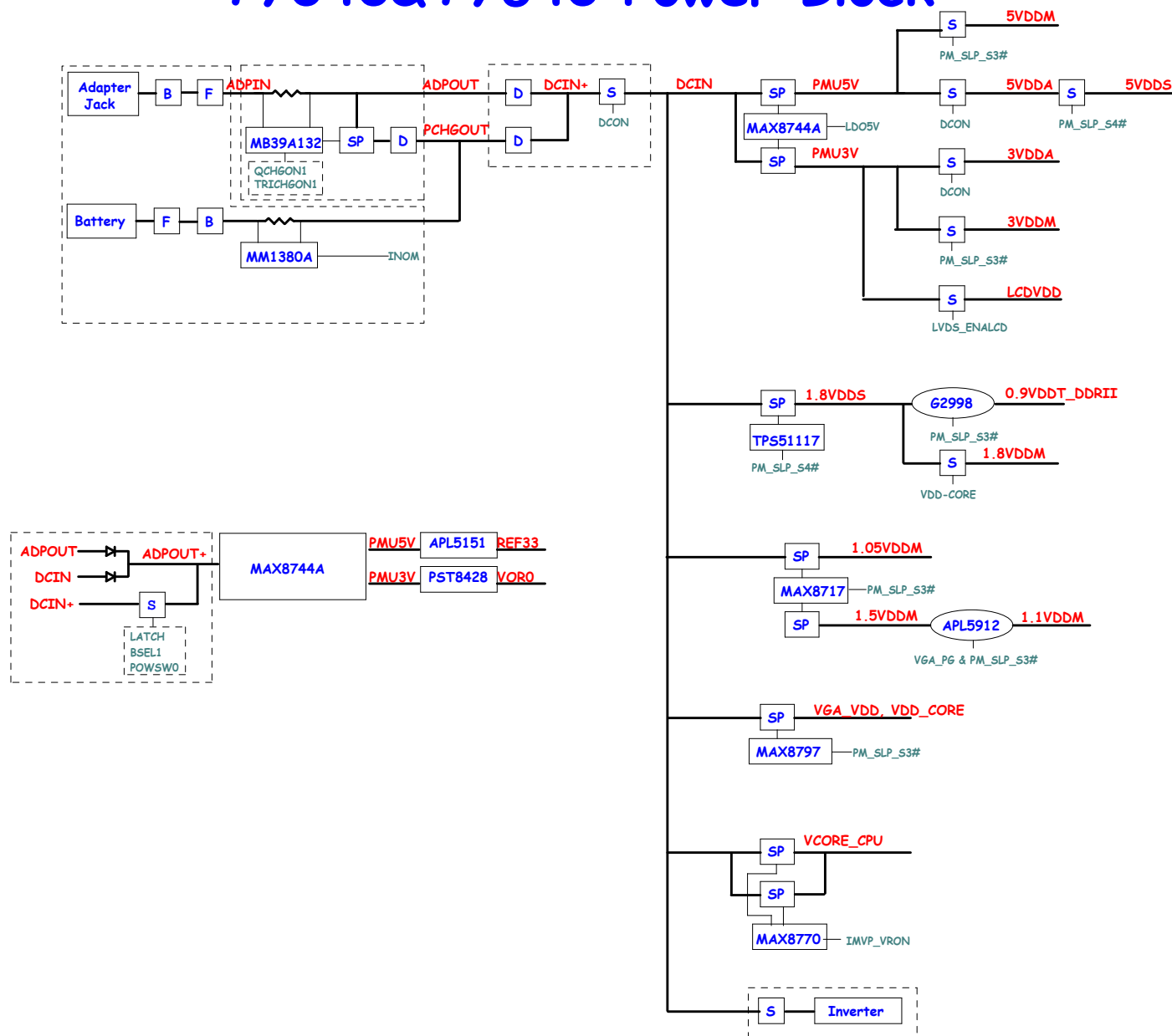




# SYSTEM POWER OVP



# TY040&TY640 Power Block



— Signal  
— Power Path

○ LDO

**B** Bead

**D** Diode

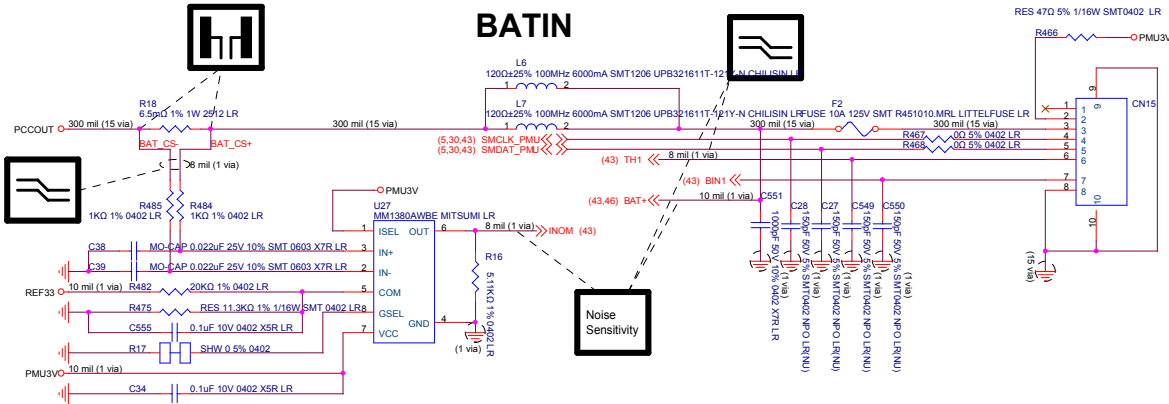
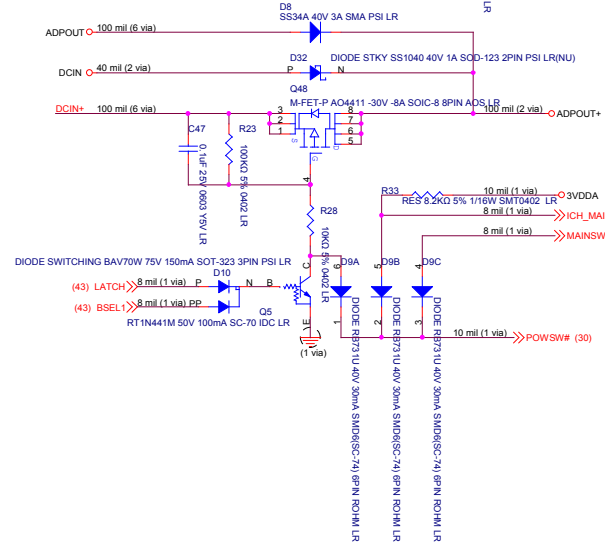
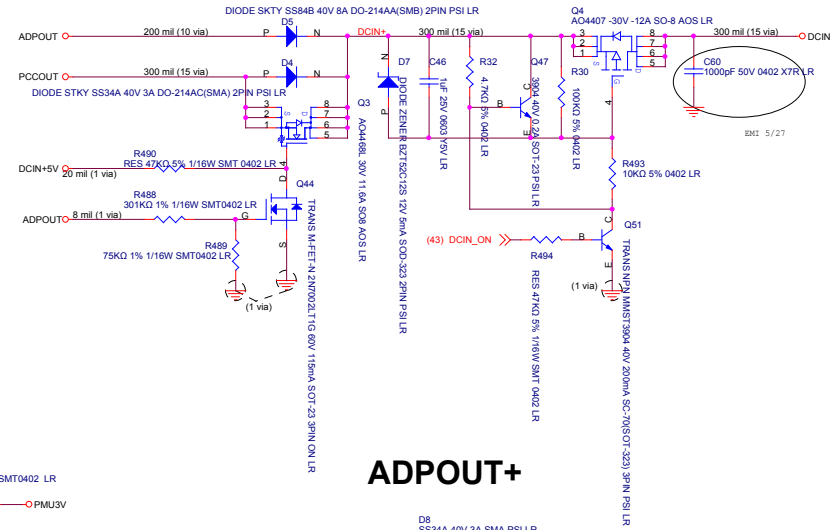
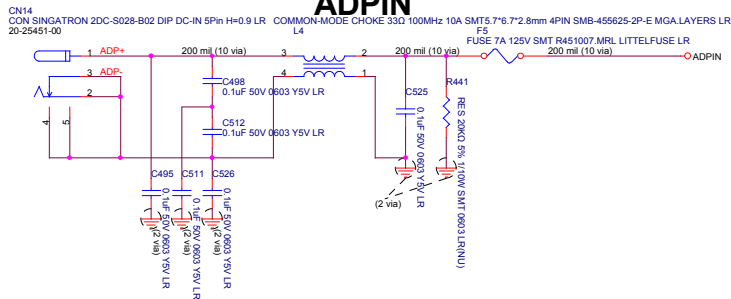
**F** Fuse

**S** Switch

**SP** Switching Power Converter

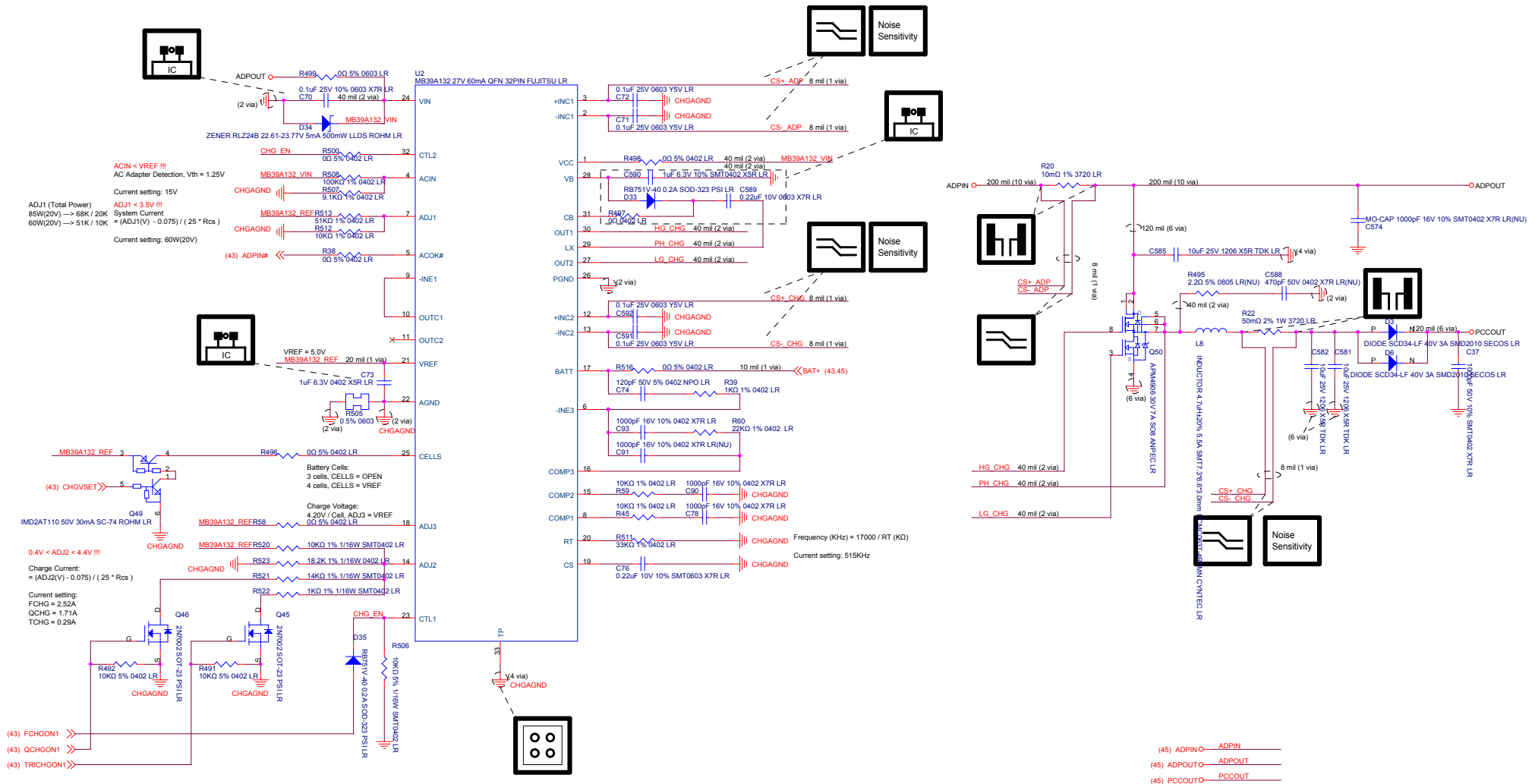


## ADPIN, BATIN, DCIN, ADPOUT+

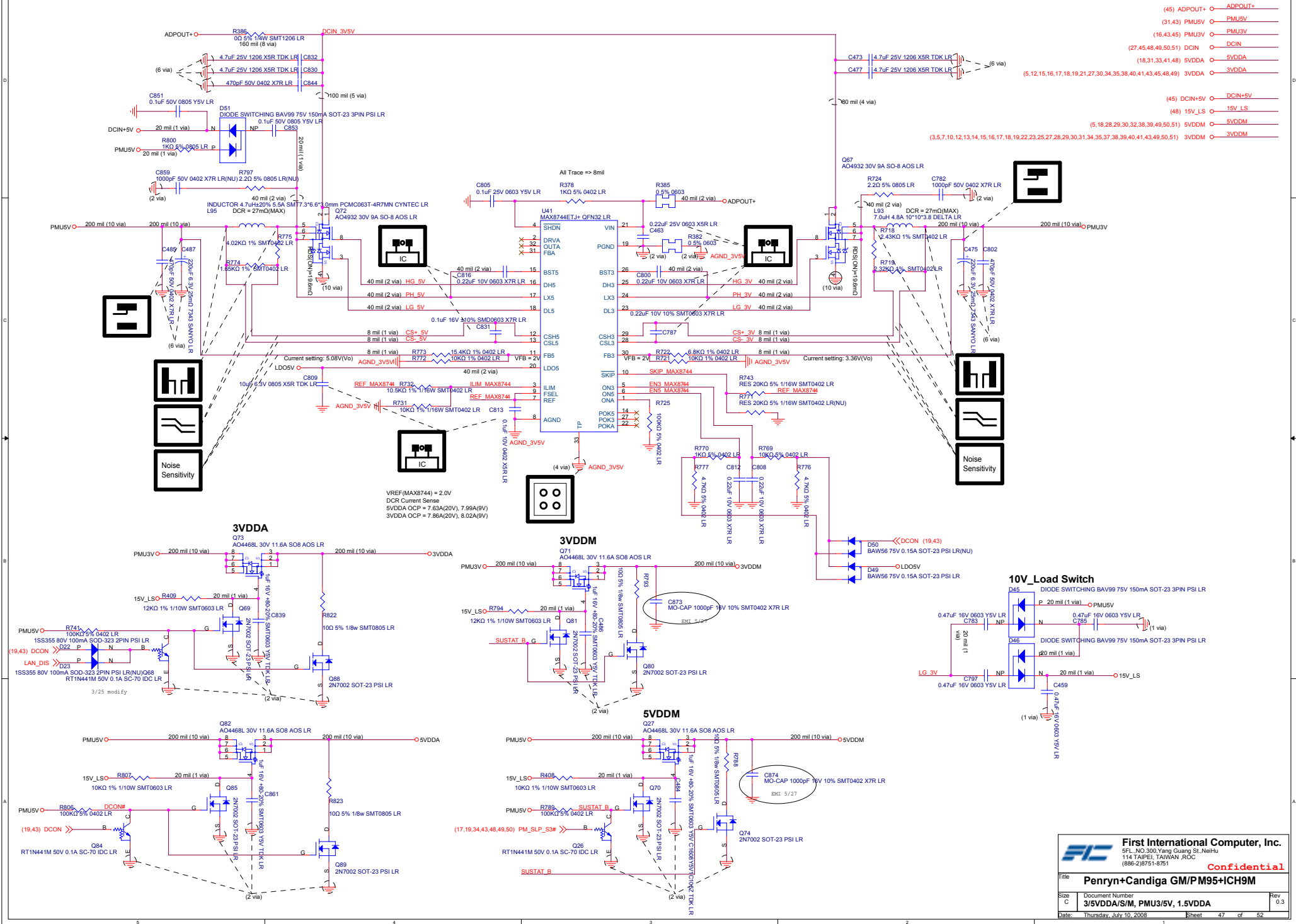


- (5,12,15,16,17,18,19,21,27,30,34,35,38,40,41,43,47,48,49) 3VDDA ○ — 3VDDA

# Charger

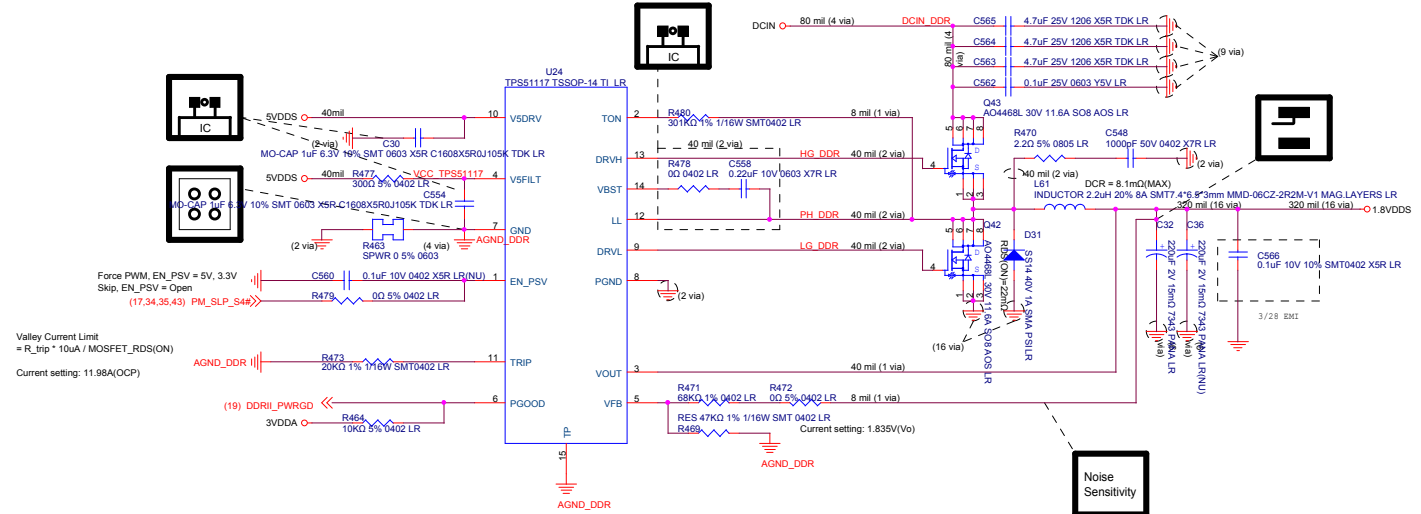
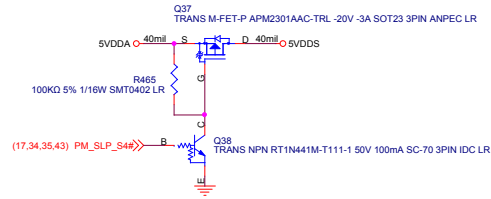


# PMU5V/3V, 5VDDA/S/M, 3VDDA/S/M

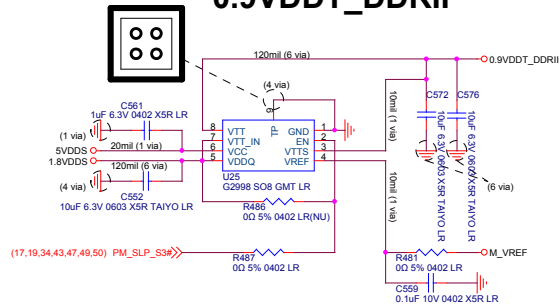


# 1.8VDDS/M, 0.9VDDT\_DDRII

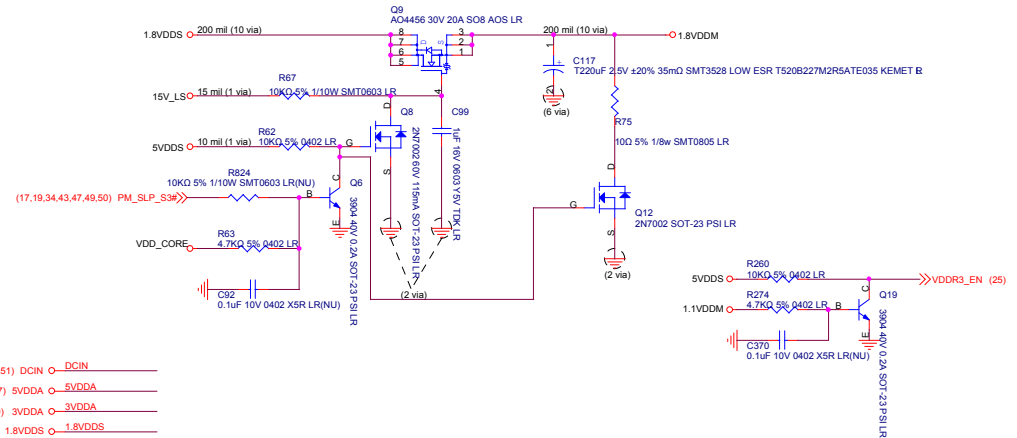
## 1.8VDDS



## 0.9VDDT\_DDRII

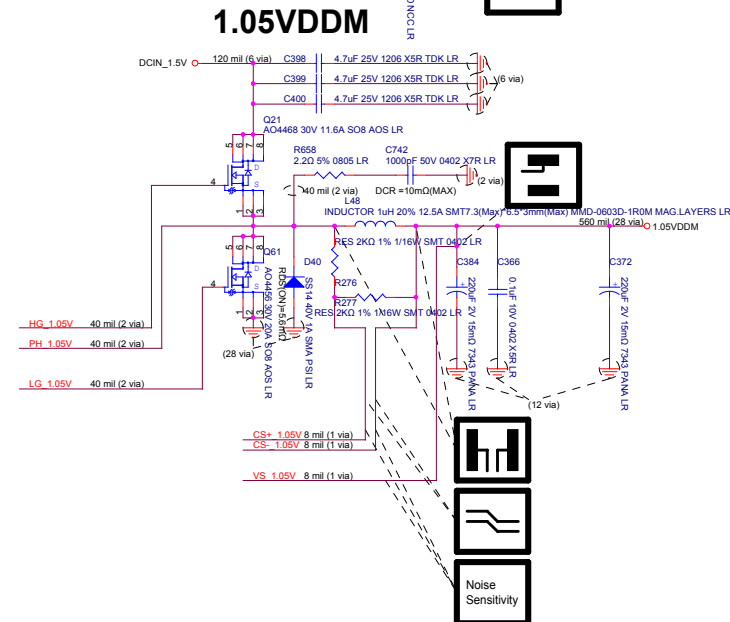
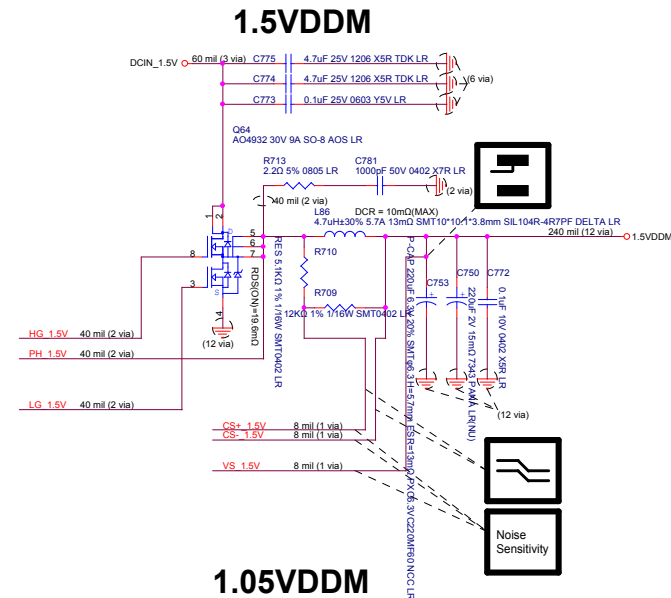
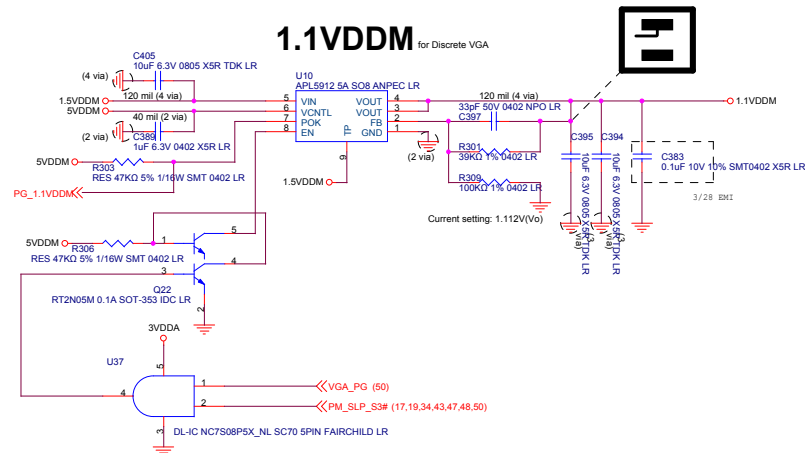
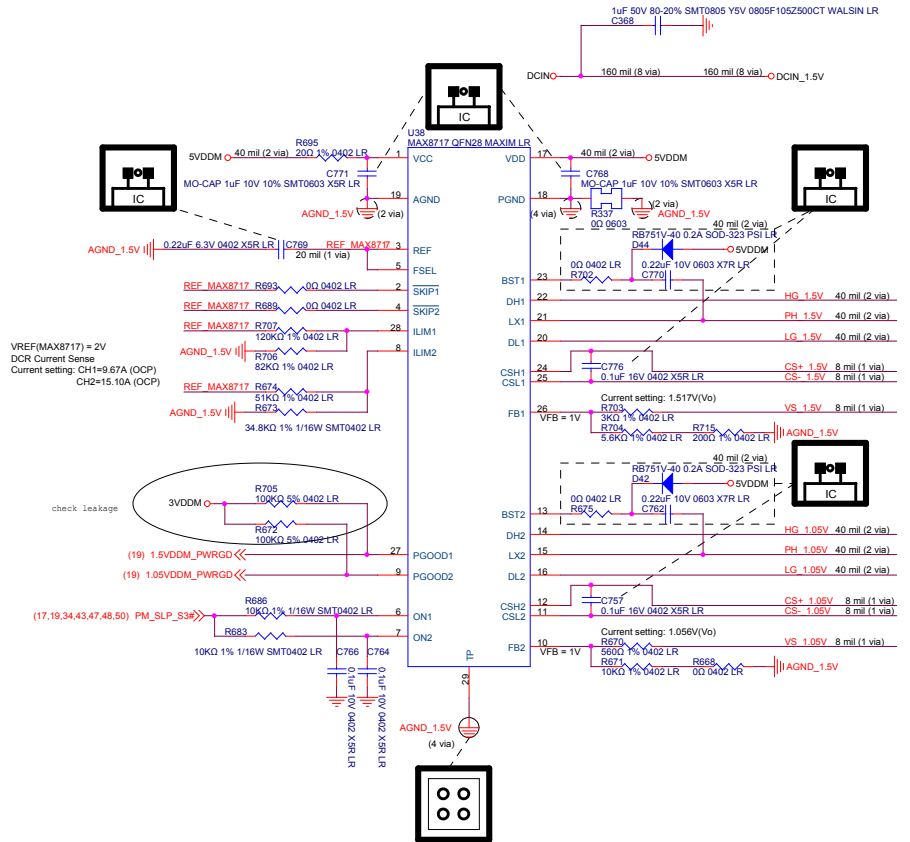


## 1.8VDDM



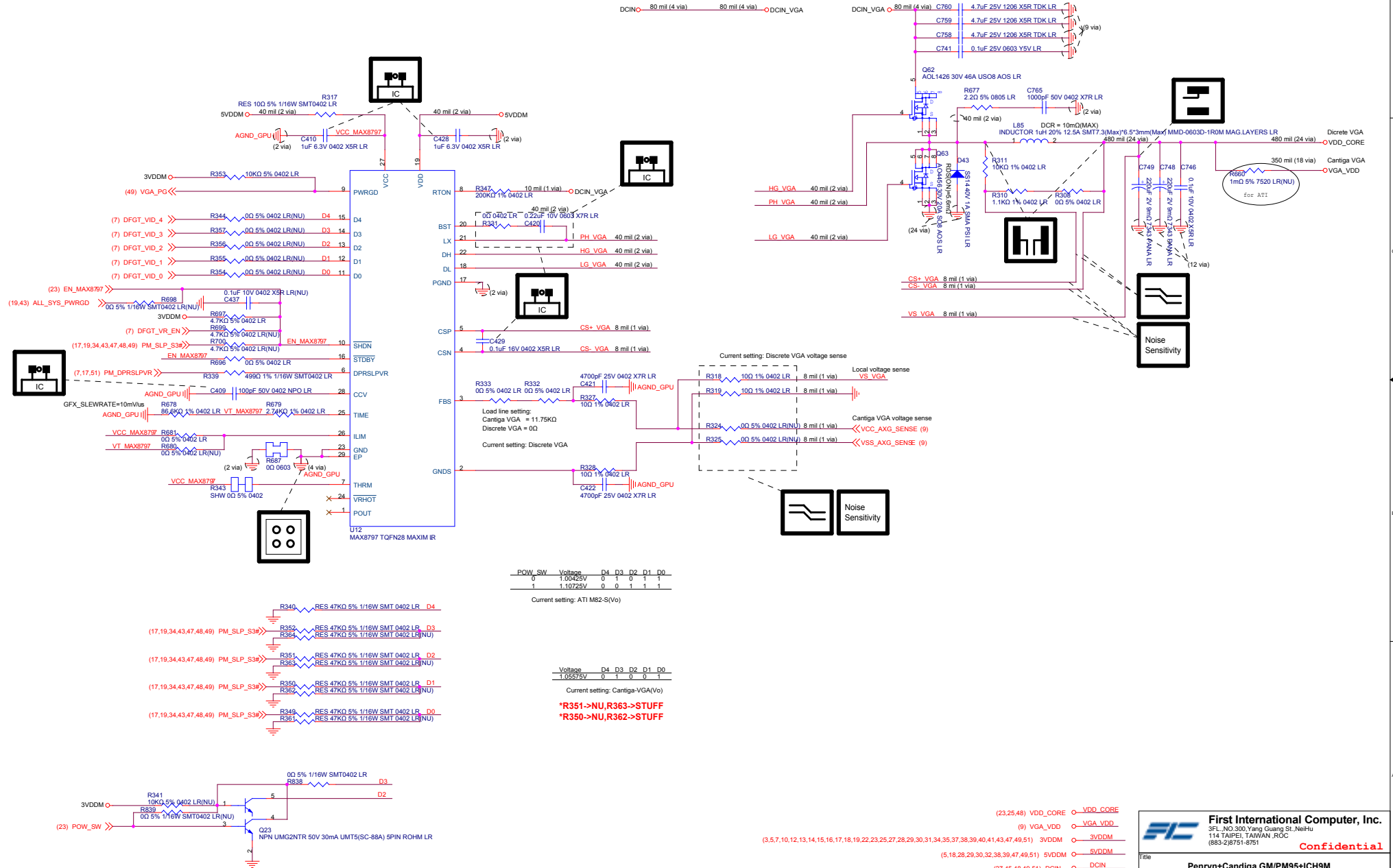
(27,45,49,50,51) DCIN → DCIN  
(18,31,33,41,47) 5VDDA → 5VDDA  
(5,12,15,16,17,18,19,21,27,30,35,38,40,41,43,45,47,49) 3VDDA → 3VDDA  
(7,9,10,13,14) 1.8VDDS → 1.8VDDS  
(13,14) 0.9VDDT\_DDRII → 0.9VDDT\_DDRII  
(7,13,14) M\_VREF → M\_VREF  
(47) 15V\_LS → 15V\_LS  
(22,23,24,25,26) 1.8VDDM → 1.8VDDM  
(23,25,50) VDD\_CORE → VDD\_CORE  
(22,23,25,49) 1.1VDDM → 1.1VDDM

1.5VDDM / 1.05VDDM / 1.1VDDM



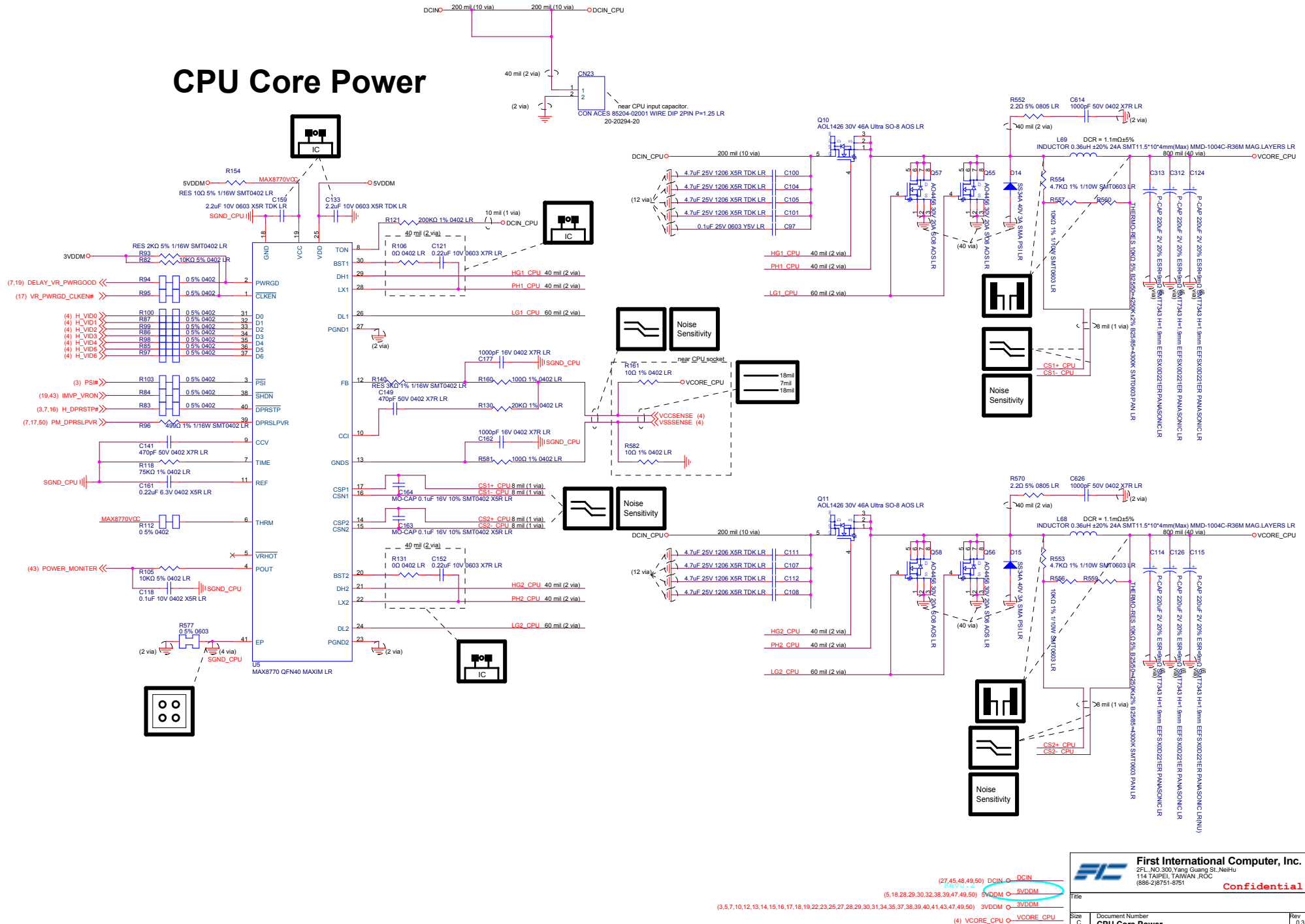
(5, 12, 15, 16, 17, 18, 19, 21, 27, 30, 35, 38, 40, 41, 43, 45, 47, 48)	3VDDA	3VDDA
(27, 45, 48, 50, 51)	DCIN	DCIN
(5, 18, 28, 29, 30, 32, 38, 39, 47, 50, 51)	5VDDM	5VDDM
(3, 5, 7, 10, 12, 13, 14, 15, 16, 17, 18, 22, 23, 25, 28, 29, 30, 31, 34, 35, 37, 38, 39, 40, 41, 43, 47, 50, 51)	3VDDM	3VDDM
(4, 9, 10, 15, 16, 18, 34, 40, 41)	1.5VDDM	1.5VDDM
(3, 4, 6, 7, 9, 10, 12, 15, 16, 18)	1.05VDDM	1.05VDDM
(22, 23, 25, 48)	1.1VDDM	1.1VDDM

## VGA Core (Cantiga VGA, ATI M82-S)



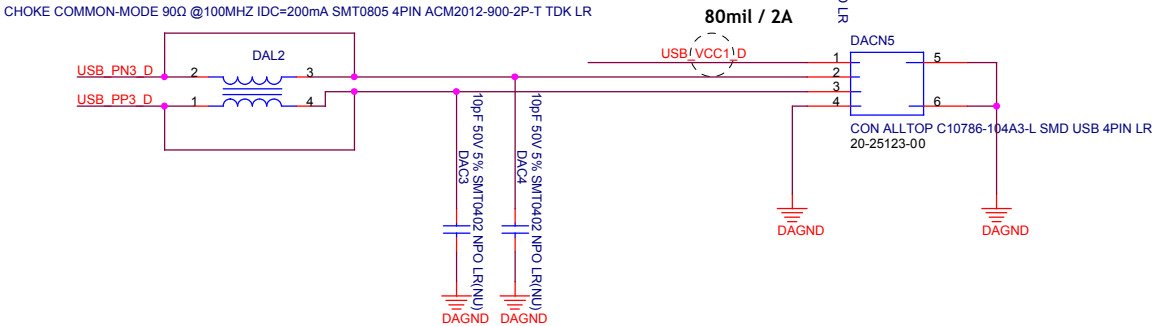
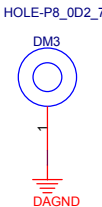
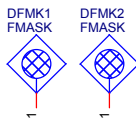
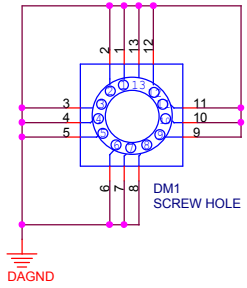
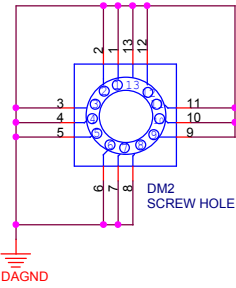
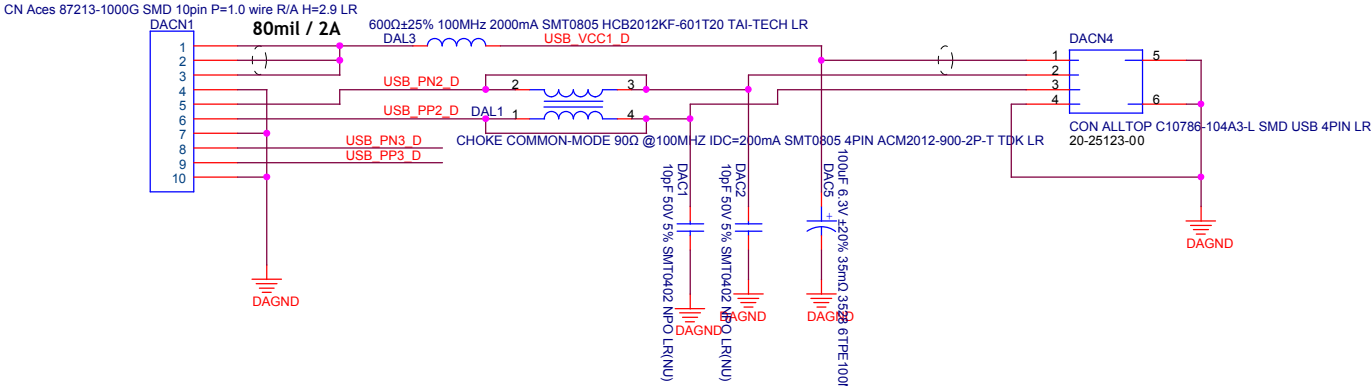


## CPU Core Power

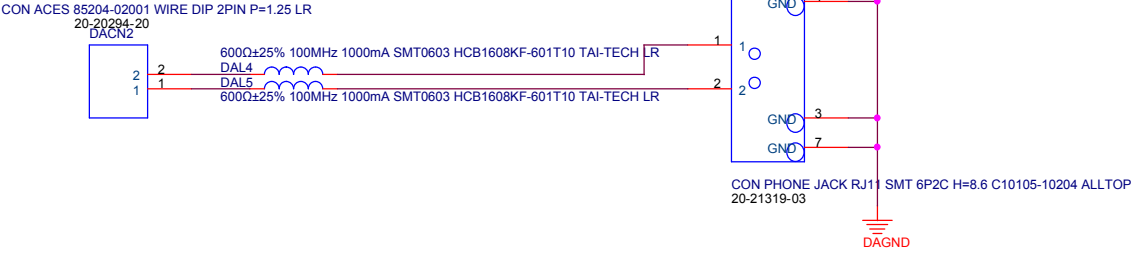



# USB Board

80mil / 2A



For MDC modem





**First International Computer, Inc.**  
5FL, NO.300, Yang Guang St., NeiHu  
114 TAIPEI, TAIWAN, R.O.C  
(886-2)8751-8751

**Confidential**

Title <b>Penryn+Candiga GM/PM95+ICH9M</b>		
Size B	Document Number <b>TY640 USB Board</b>	Rev 0.3
Date: Thursday, July 10, 2008	Sheet 52	of 52