CT8 BLOCK DIAGRAM

CLAW HAMMER / RS480 / SB400

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

DDR-SODIMM1

DDR-SODIMM2

DDR 266,333,400MHz

CPU CLAW HAMMER

754 Pins (uPGA)

CPU THERMAL SENSOR GMT-781

14.318MHz

CPUCLK, CPUCLK#

CLOCK GEN

CY28RS480/ ICS951412

SBLINKCLK, SBLINKCLK#

NBSRCCLK, NBSRCCLK#

HTREFCLK

OSC14M

HyperThansport I/O BUS Link 16x16

CABLE DOCK

AV BOARD

Daughter Board

TV, USB, BLUE TOOTH

Power Board

CRT port — R.G,B

LCD Panel — LVDS X1

S-VIDEO — TV-OUT

NORTH BRIDGE RS480M

705 BGA

INTEGRADED VGA FUNCTION

Based on Redeon 9600

A-LINK 2X PCI-E

32.768KHz

USB PORT 0, 1, 2 — USB 2.0

1st IDE - HDD — ATA 66/100/133

2nd IDE - CDROM — ATA 66/100/133

SB400

564 BGA

NBSRCCLK, NBSRCCLK#

33MHZ, 3.3V PCI

PCLK_7411

PCLK_MINI

PCLK_LAN

AC97

24.576MHz

48MHz

PWRCLKP
PWRCLKN
DIB_DATAN
DIB_DATAP

AC97

CX20468-31

MBAMC20493-010

LAN

Realtek

8100CL

MINI-PCI

CARDBUS / IEEE 1394 CONTROLLER/CF

TI 7411

24.576MHz

25MHz

32.768KHz

PCLK_591

3.3V LPC, 33MHz

PC97551

TQFP 176

SMARTDAA MODEM,

AMP

TPA0312

WIRE

5 IN 1

CARD READER SD/MMC, SM, MS, XD

CARDBUS SLOT X1

1394 CONN

FAN

Touchpad

Keyboard

FLASH

RJ11 JACK

JACK

HEADPHONE,
2ND HEADPHONE,
MIC

RJ45 JACK

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
GBIT ETHERNET	AD16	2	C
MINIPCI SLOT	AD18	1	E,F
CardBus/1394	AD25	4	B,D,G

SYSTEM POWER MAX1845 (1.2V/NB_CORE/1.25V)

CPU CORE MAX1544 POWER 1.2V

SYSTEM MAX1999 POWER(3/5V)

SYSTEM POWER MAX1845 (2.5VSUS/1.8VSUS)

BATT CHARGER MAX1722

DISCHARGE

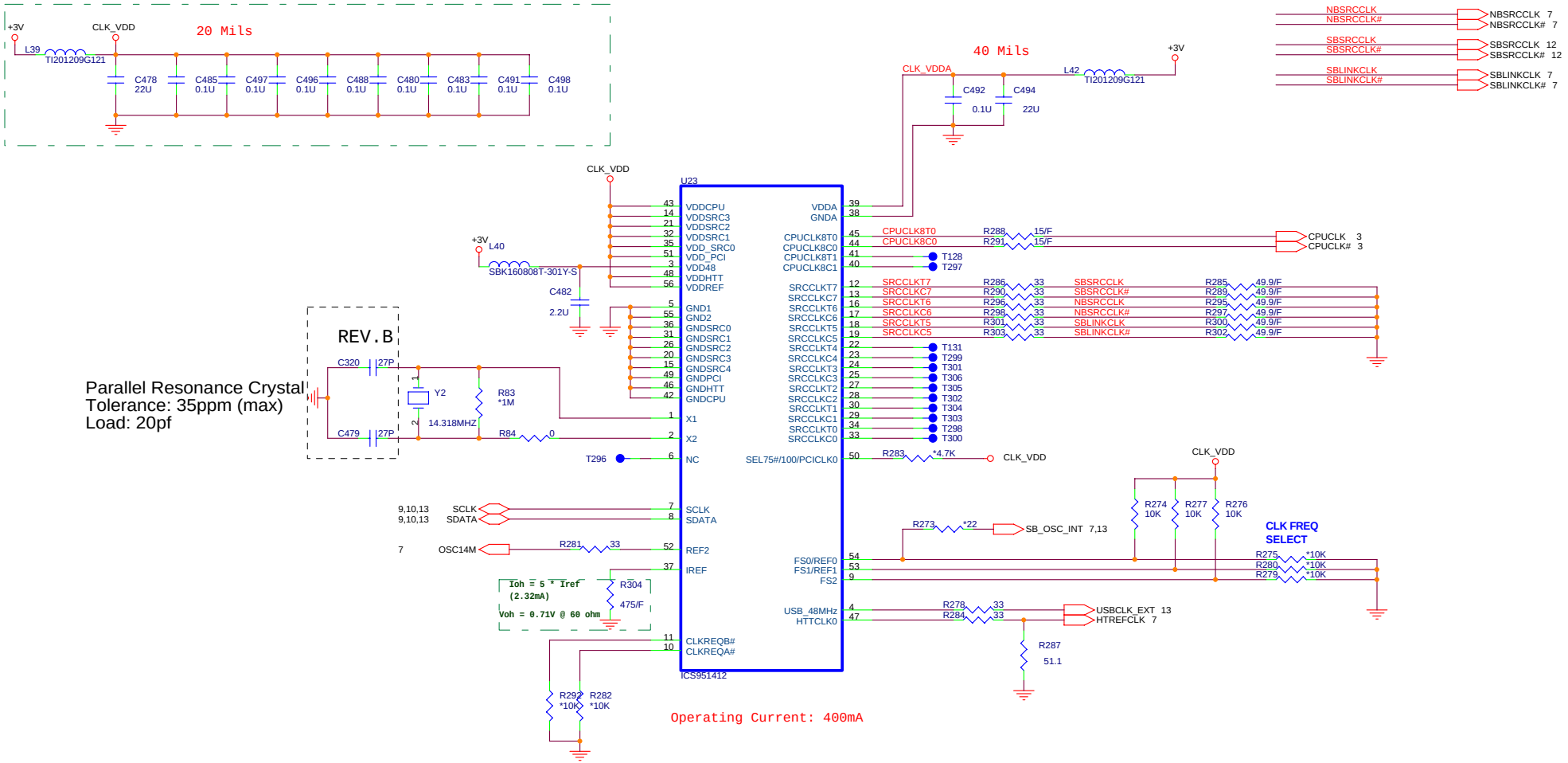
PROJECT : CT8

Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Monday, December 13, 2004 Sheet 1 of 42

CLK



Operating Current: 400mA

Layout Note:

1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS CKG. AS POSSIBLE

2- ROUTE ALL CPUCLK/#, NBSRCCLK/#, SBSRCCLK/#, SBLINKCLK/# AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO CKG. POWER PIN

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation

PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EXT CLOCK GENERATOR	1A

Date: Monday, December 13, 2004 Sheet 2 of 42

CPU

20 Mils width to pin
100 Mils width to capacitor
250 Mils width to PWM

Near Socket754

STUFF WHEN CONFIGURED AS 16-BIT LINK

H/W MONITOR

U18
MAX6657/GMT-781

REV.B

50 Mils, routing as 15 mils width if the distance from bead to cpu pin less than 1000 mils.

Output current(Max): 300mA

Ra
Rb

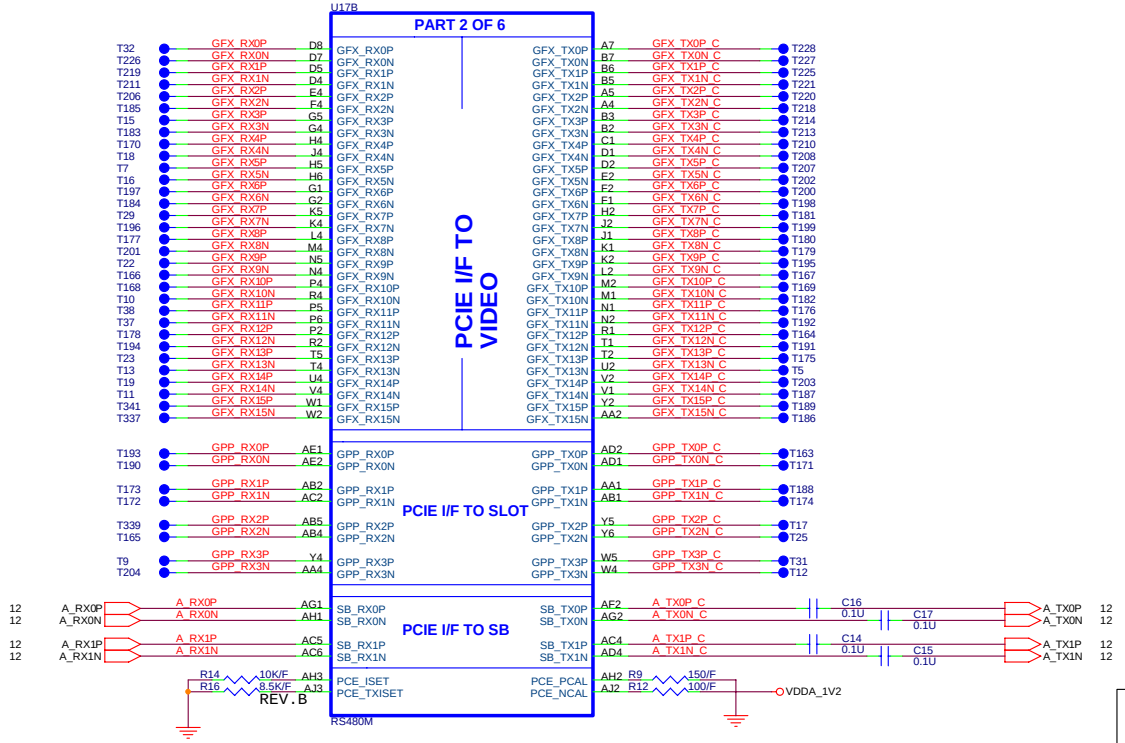
Vout=1.25(1+Ra/Rb)
Ra=Rb(Vout/1.25-1)

REV.B

PROJECT : CT8			
Quanta Computer Inc.			
Size: Custom	Document Number: CPU H.T/CTL I/F		Rev: 1A
Date: Monday, December 13, 2004	Sheet 3 of 42		

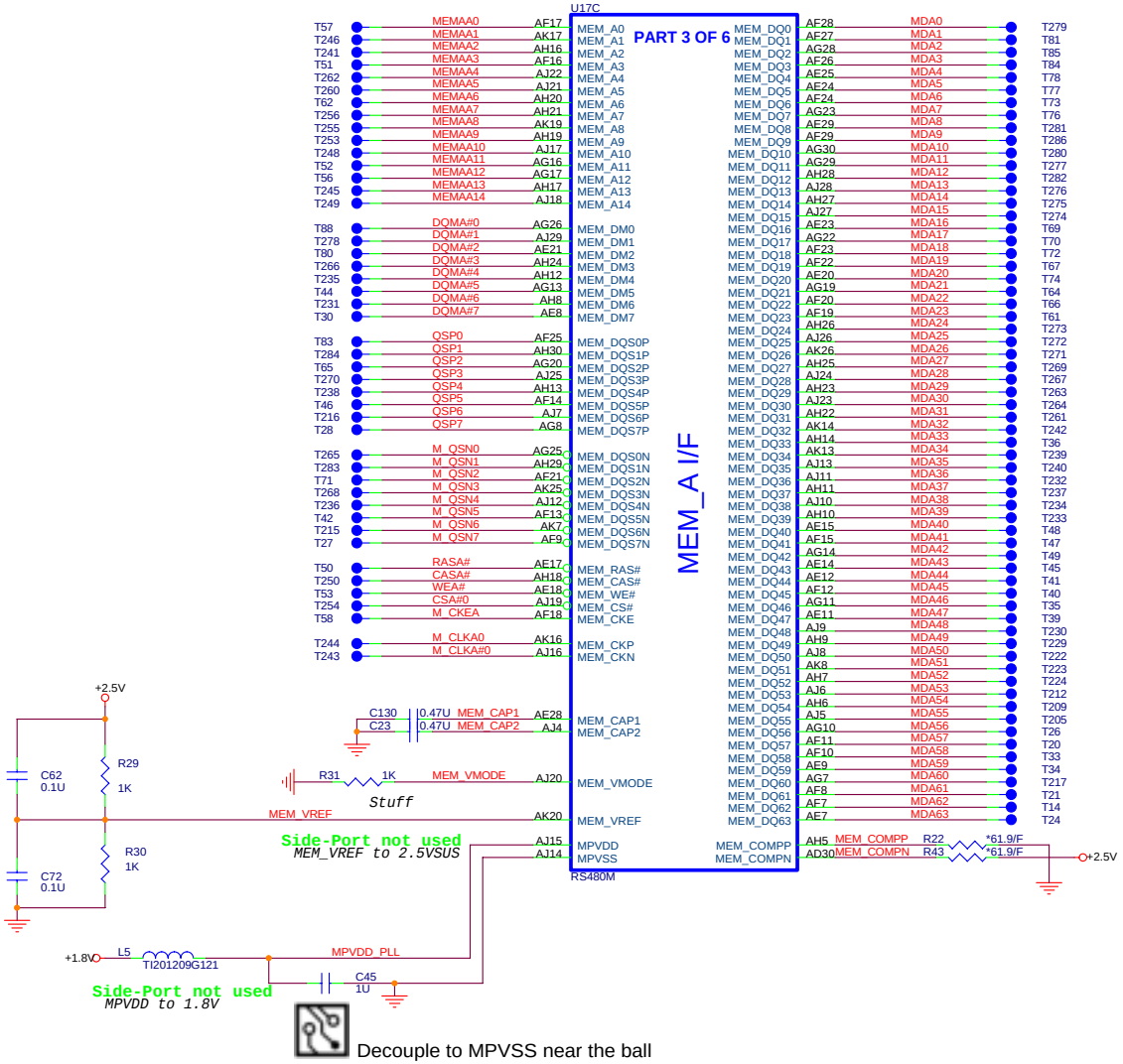
CLG

Link 0 Is Clawhammer <--> RS480



PROJECT : CT8	
Quanta Computer Inc.	
Size: Custom	Document Number: RS480M-HT A-LINK0
Rev: 1A	
Date: Monday, December 13, 2004	Sheet 5 of 42

CLG



PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS480M-SIDE PORT MEM I/F	1A

Date: Monday, December 13, 2004 Sheet 6 of 42

CLG

EMI
REV.B

EMI
REV.B

AVDD	DAC VDD (2.5V)
AVDDDI	DIGITAL VDD (1.8V)
AVDDQ	DAC2 BANDGAP REF (1.8V)
PLLVDD	PLL VDD (1.8V)
HTPVDD	HT PLL VDD (1.8V)

PUT AVDD, AVDDDI, AVDDQ,PLVDD,HTPVDD DECOUPLING CAPS ON THEBOTTOM, CLOSE TO BALLS

DO NOT SHARE GND VIA ON JOINT

ROUTING H_THRMDA AND HW_AGND AS DIFFERENTIAL PAIR

REV.B DEL Y1 AND U3 CIRCUIT.

LOAD_ROM#:LOAD ROM STRAP ENABLE strap

High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE

SPMEM_EN#:SIDE PORT MEMORY ENABLE strap

NC, SIDE PORT MEMORY DISABLE
Low, SIDE PORT MEMORY ENABLE

DO NOT SHARE GND VIA ON JOINT

PROJECT : CT8
Quanta Computer Inc.

Size: Custom	Document Number: RS480M-VIDEO & CLKGEN	Rev: 1A
Date: Monday, December 13, 2004	Sheet 7 of 42	

CLG

NB RS480 POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR,VDDRCK	ON	ON	ON	ON	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

PUT DECOUPLING CAPS ON THE TOP, CLOSE TO BALLS
CONNECT VSSA22,VSSA59,VSS30,VSS89 to the ground.

Notice the trace width.

PROJECT : CT8
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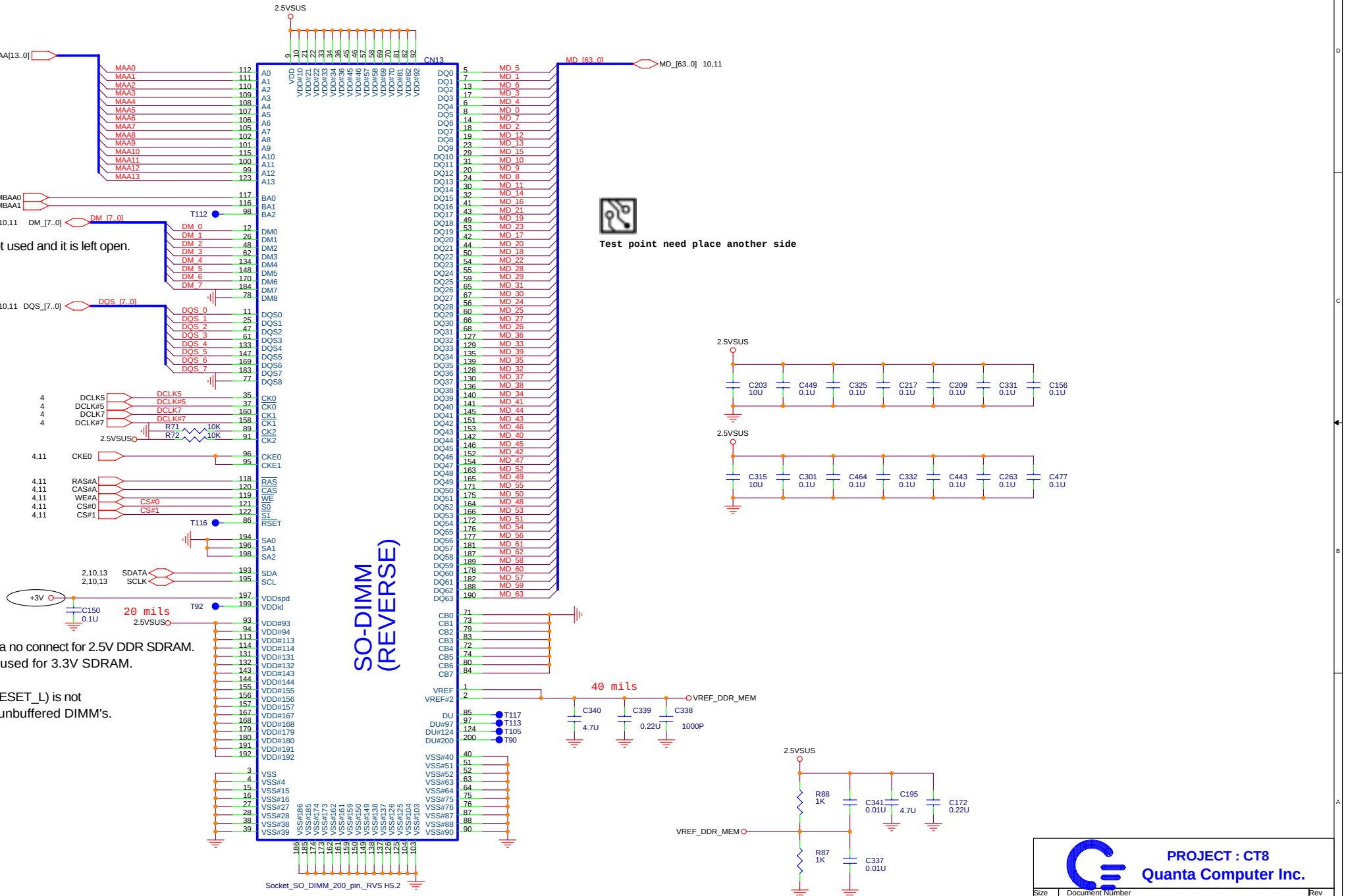
Size	Document Number	Rev
Custom	RS480M-POWER	1A
Date: Monday, December 13, 2004	Sheet 8 of 42	

DDR

Unbuffered DDR Near SODIMM Socket

ALLEGRO ROOM PROPERTY
AMD CPU



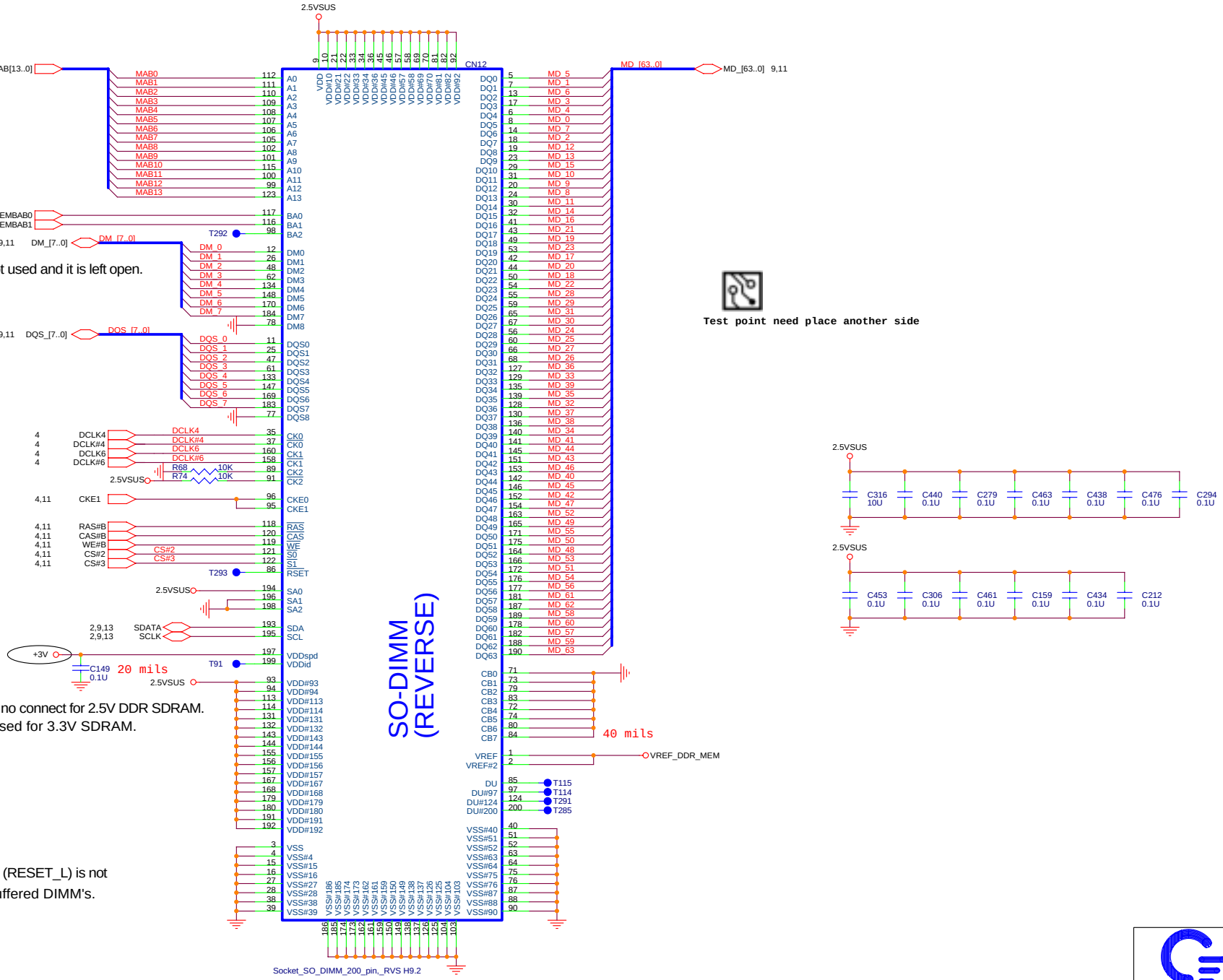
PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR NEAR SO-DIMM	1A
Date: Monday, December 13, 2004	Sheet 9 of 42	

DDR

Unbuffered DDR Far SODIMM Socket

ALLEGRO ROOM PROPERTY
AMD CPU



PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR FAR SO-DIMM	1A
Date: Monday, December 13, 2004	Sheet 10 of 42	

DDR

MD[63..0]
DQS[7..0]
DM[7..0]

MD62 MD58 MD56 MD61 MD59 MD63 MD60 MD57 MD55 MD50 MD48 MD53 MD51 MD54 MD49 MD52 MD42 MD47 MD45 MD40 MD43 MD46 MD41 MD44 MD38 MD34 MD32 MD37 MD39 MD35 MD36 MD33 MD27 MD26 MD25 MD24 MD31 MD30 MD28 MD29 MD22 MD18 MD17 MD20 MD19 MD23 MD16 MD21 MD11 MD14 MD9 MD8 MD10 MD15 MD12 MD13 MD7 MD2 MD4 MD0 MD6 MD3 MD5 MD1

RN55 10X2
RN61 10X2
RN57 10X2
RN60 10X2
RN65 10X2
RN72 10X2
RN74 10X2

MD_62 MD_58 MD_56 MD_61 MD_59 MD_63 MD_60 MD_57 MD_55 MD_50 MD_48 MD_53 MD_51 MD_54 MD_49 MD_52 MD_42 MD_47 MD_45 MD_40 MD_43 MD_46 MD_41 MD_44 MD_38 MD_34 MD_32 MD_37 MD_39 MD_35 MD_36 MD_33 MD_27 MD_26 MD_25 MD_24 MD_31 MD_30 MD_28 MD_29 MD_22 MD_18 MD_17 MD_20 MD_19 MD_23 MD_16 MD_21 MD_11 MD_14 MD_9 MD_8 MD_10 MD_15 MD_12 MD_13 MD_7 MD_2 MD_4 MD_0 MD_6 MD_3 MD_5 MD_1

DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7

R271 10-0402
R252 10-0402
R236 10-0402

DQS_0 DQS_1 DQS_2 DQS_3 DQS_4 DQS_5 DQS_6 DQS_7

DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7

R239 10-0402

DM_0 DM_1 DM_2 DM_3 DM_4 DM_5 DM_6 DM_7

DQS_[7..0]
DM_[7..0]

MD_2 MD_7 MD_6 MD_3 MD_5 MD_1 MD_0 MD_4 MD_14 MD_11 MD_15 MD_10 MD_8 MD_9 MD_12 MD_13 MD_18 MD_22 MD_23 MD_19 MD_16 MD_21 MD_17 MD_20 MD_26 MD_31 MD_30 MD_27 MD_29 MD_28 MD_25 MD_24 MD_39 MD_35 MD_38 MD_34 MD_36 MD_33 MD_32 MD_37 MD_47 MD_42 MD_46 MD_43 MD_44 MD_41 MD_45 MD_40 MD_55 MD_50 MD_51 MD_54 MD_52 MD_49 MD_48 MD_53 MD_63 MD_59 MD_62 MD_58 MD_61 MD_56 MD_57 MD_60

DM_7 DQS_7 DM_5 DQS_5 DM_3 DQS_3 DM_1 DQS_1

DQS_6 DM_6 DQS_4 DM_4 DM_2 DQS_2 DM_0 DQS_0

RN33 68X4
RN35 68X4
RN27 68X4
RN29 68X4
RN10 68X4
RN2 68X4

VTT_DDR

MAA0 MAA2 MAA8 MAA11 MAA1 MAA3 MAA5

MAA7 MAA9 MAA4 MAA6 MAA12 MAA13

RN16 47X4

MAA10 MAA13 CS#0

CS#1

VTT_DDR

MAB2 MAB4 MAB6 MAB5 MAB3 MAB1 MAB10

MAB11 MAB8 MAB9 MAB7 MAB12

CS#3 CS#2 MAB13

RN17 47X4

MAB0

03/19 Modify ->Quanta stock haven't 68x4 (8P4R-0402)

Place on each end of the VTT island.

VTT_DDR

C127 10U

LAYOUT: Locate close to Clawhammer socket.

VTT_DDR 2.5VSUS

REV.B

C280 220U

LAYOUT: Place on VTT fill near Clawhammer and near DIMMs

VTT_DDR

C169 100P

C459 1000P

LAYOUT: Place a cap every 1 in. on VTT traces between Clawhammer and DDR.

VTT_DDR

C319 0.22U

LAYOUT: Place alternating caps to GND and VDD_2.5_SUS in a single line along VTT_DDR_SUS island.

VTT_DDR

C335 0.1U

C201 0.1U

C241 0.1U

C289 0.1U

C330 0.1U

C264 0.1U

VTT_DDR

2.5VSUS

C346 0.1U

C274 0.1U

C185 0.1U

C227 0.1U

C309 0.1U

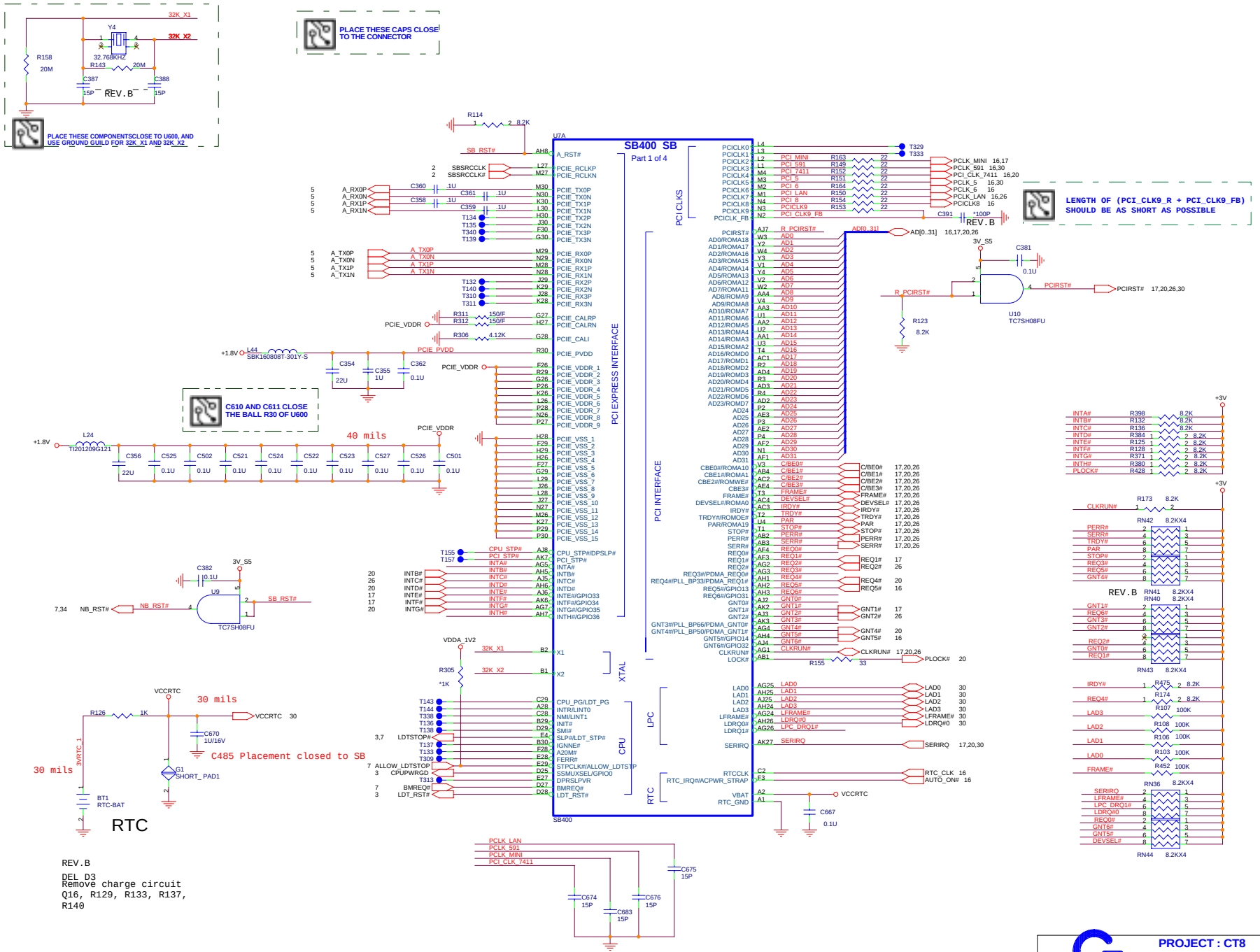
C317 0.1U

C173 0.1U

C333 0.1U

Size: Custom	Document Number: DDR SO-DIMM TERMINATION	Rev: 1A
Date: Monday, December 13, 2004	Sheet 11 of 42	

CLG


32K_X1
32K_X2
Y4
32.768KHZ
R158
20M
R143
20M
C387
15P
C388
15P
REV.B
PLACE THESE COMPONENTSCLOSE TO U600, AND USE GROUND GUILD FOR 32K_X1 AND 32K_X2
PLACE THESE CAPS CLOSE TO THE CONNECTOR
SB400 SB
Part 1 of 4
U7A
SB400
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
XTAL
LPC
CPU
RTC
LENGTH OF (PCI_CLK9_R + PCI_CLK9_FB) SHOULD BE AS SHORT AS POSSIBLE
C610 AND C611 CLOSE THE BALL R30 OF U600
40 mils
C485 Placement closed to SB
30 mils
RTC
REV.B
DEL D3
Remove charge circuit
Q16, R129, R133, R137,
R140

CLG

Please double check SB400 pin D5 & pin A27 define,
because cann't meet ATI library/symbols.

PWROK_SB is 33ms ~ 500ms after NB_PWRGD

R503 STUFF IS FULL FEATURE.
R504 STUFF IS DE-FEATURE.

REV.B

C641 AND C642 CLOSE THE BALL A16 OF U600

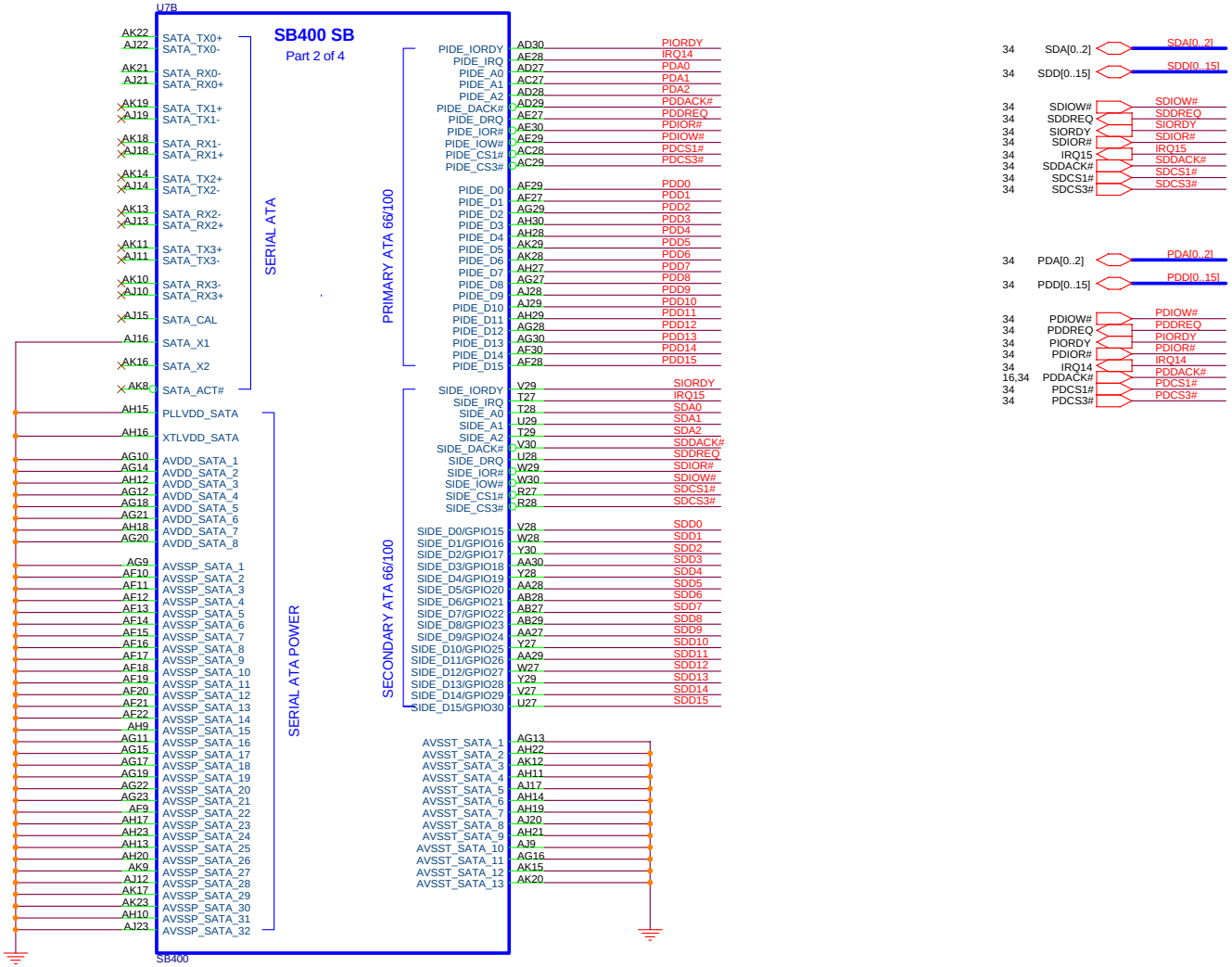
04/06 Modify

PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB400-ACPI/GPIO/USB/AC97	1A

Date: Monday, December 13, 2004 Sheet 13 of 42

CLG

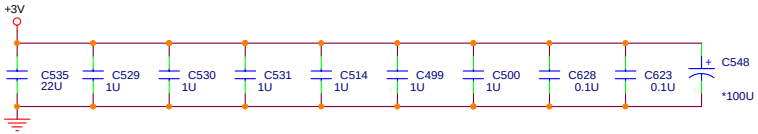


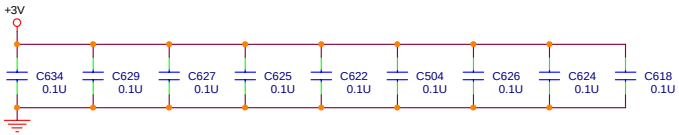
PROJECT : CT8
Quanta Computer Inc.

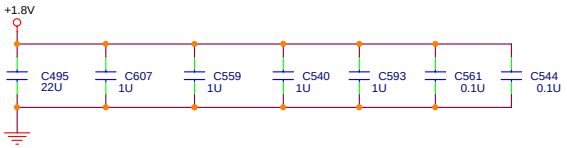
Size	Document Number	Rev
Custom	SB400-SATA/IDE	1A
Date: Monday, December 13, 2004	Sheet 14 of 42	

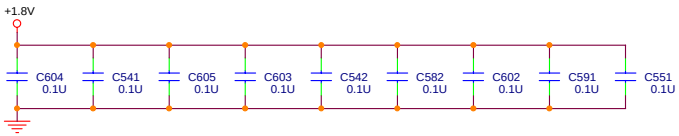
CLG

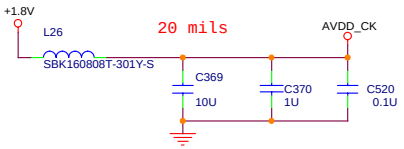
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

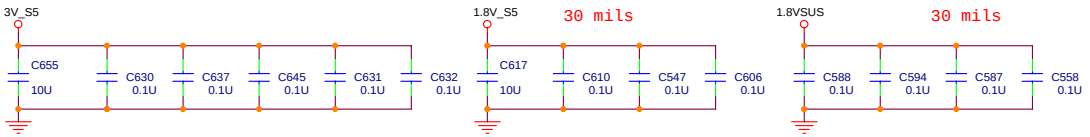


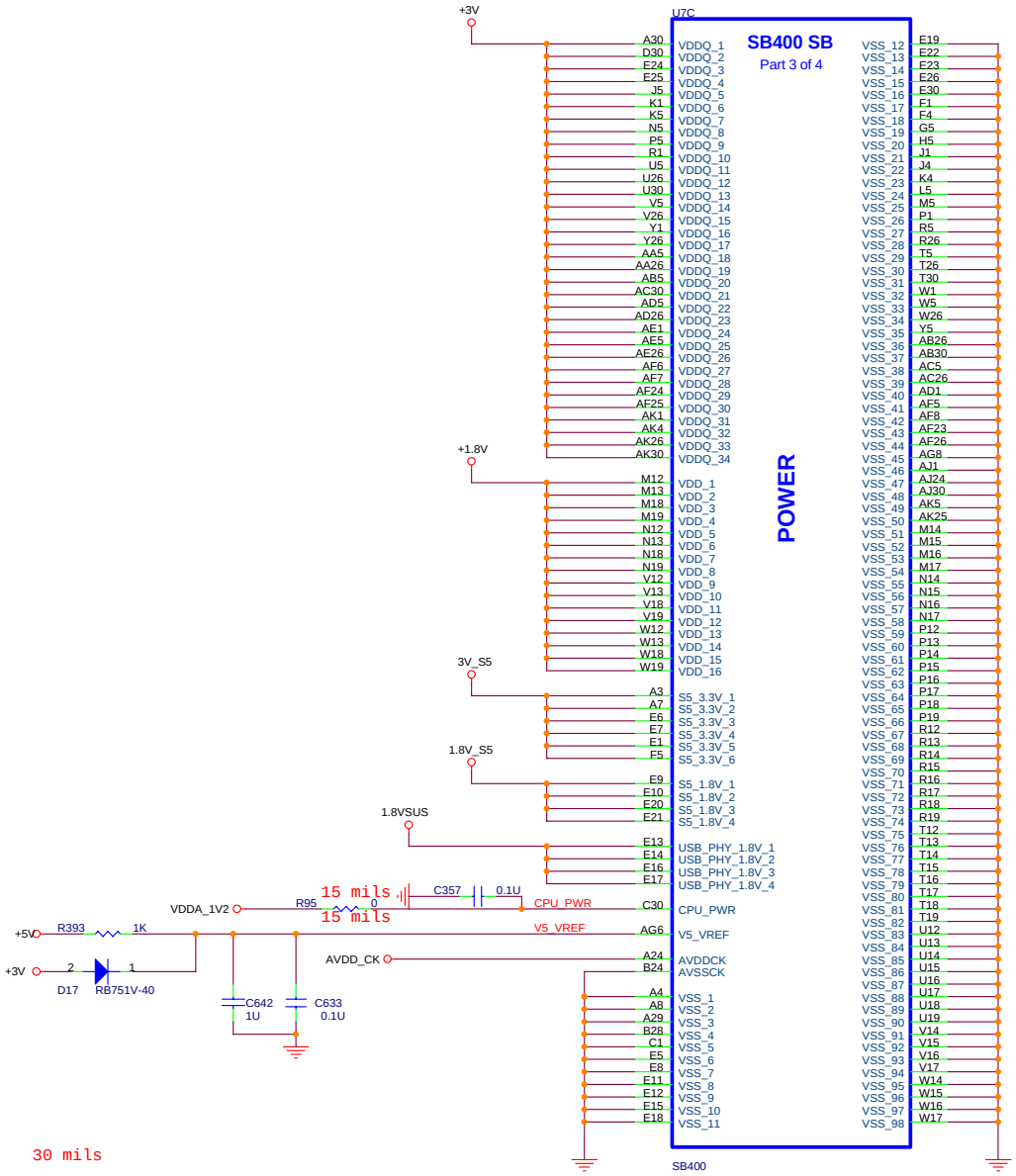










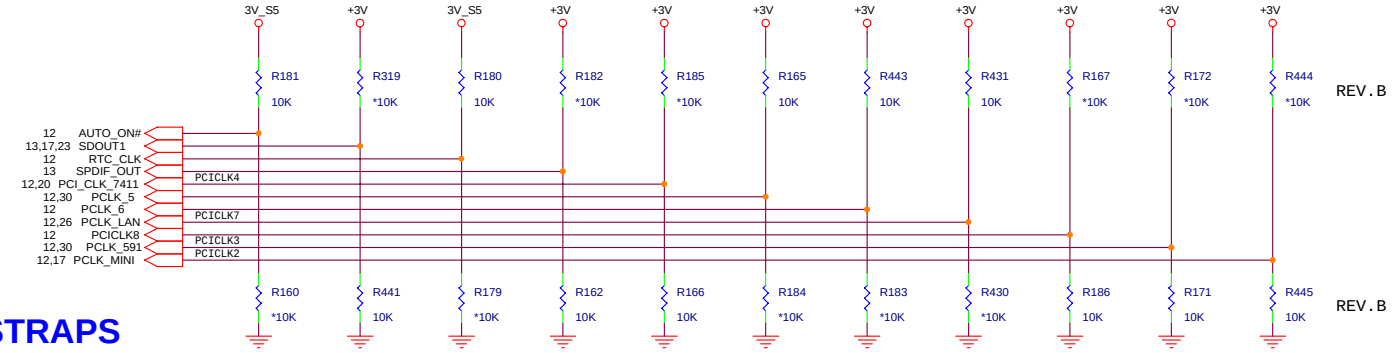


PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB400-POWER & DECOUPLING	1A

Date: Monday, December 13, 2004 Sheet 15 of 42

CLG



REQUIRED STRAPS

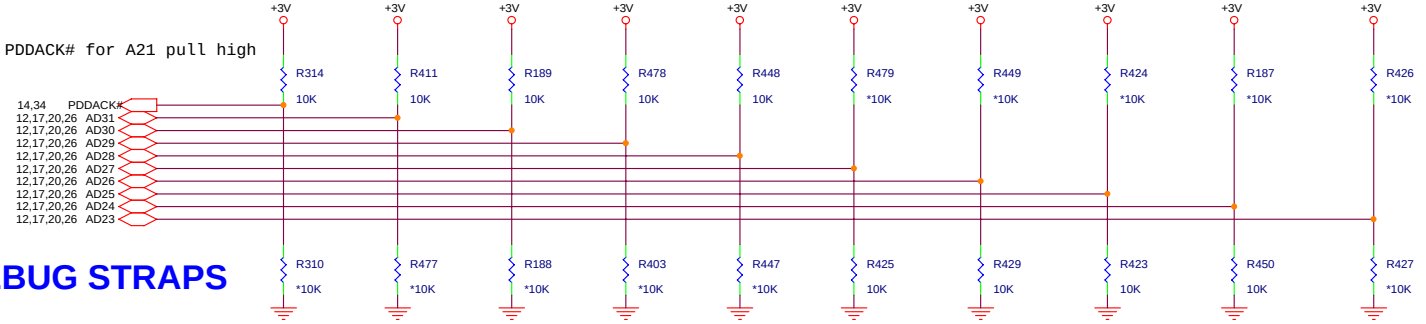
	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK_7411 (PCI_CLK4)	PCLK_5 (PCI_CLK5)	PCLK_6 (PCI_CLK6)	PCLK_LAN (PCI_CLK7)	PCI_CLK8	PCLK_591 (PCI_CLK3)
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz OSC MODE DEFAULT	14MHz OSC MODE DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = PMC LPC ROM L,H = NORMAL LPC ROM DEFAULT L,L = FWH ROM		USB PHY PWRDOWN DISABLE DEFAULT
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	48MHz XTAL MODE	14MHz XTAL MODE	CPU I/F = P4			USB PHY PWRDOWN ENABLE

Need to check

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

DEBUG STRAPS

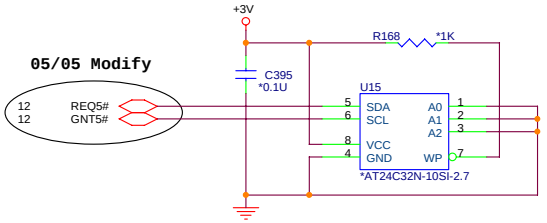
PDDACK# for A21 pull high



	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE SHORT RESET	PLL CHARGE PUMP CTRL BIT 1 HI DEFAULT	PLL CHARGE PUMP CTRL BIT 0 HI DEFAULT	PLL VCO CTRL BIT 1 HI DEFAULT	PLL VCO CTRL BIT 0 HI DEFAULT	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BY PASS USB PLL
PULL LOW	USE LONG RESET DEFAULT	PLL CHARGE PUMP CTRL BIT 1 LO	PLL CHARGE PUMP CTRL BIT 0 LO	PLL VCO CTRL BIT 1 LO	PLL VCO CTRL BIT 0 LO	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	USE USB PLL DEFAULT

Need to check

05/05 Modify

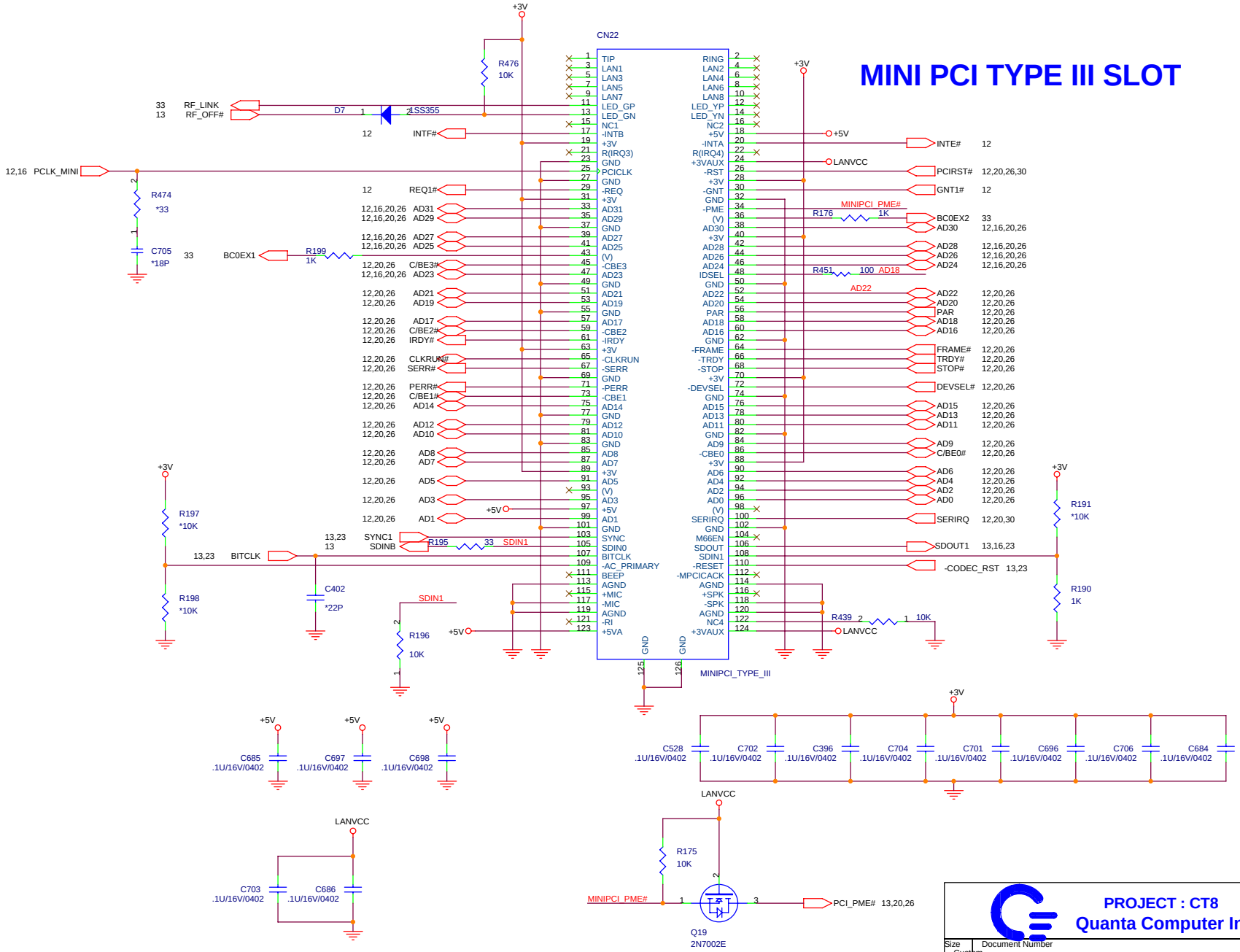


SB PCIE EEPROM STRAPS

PROJECT : CT8
Quanta Computer Inc.

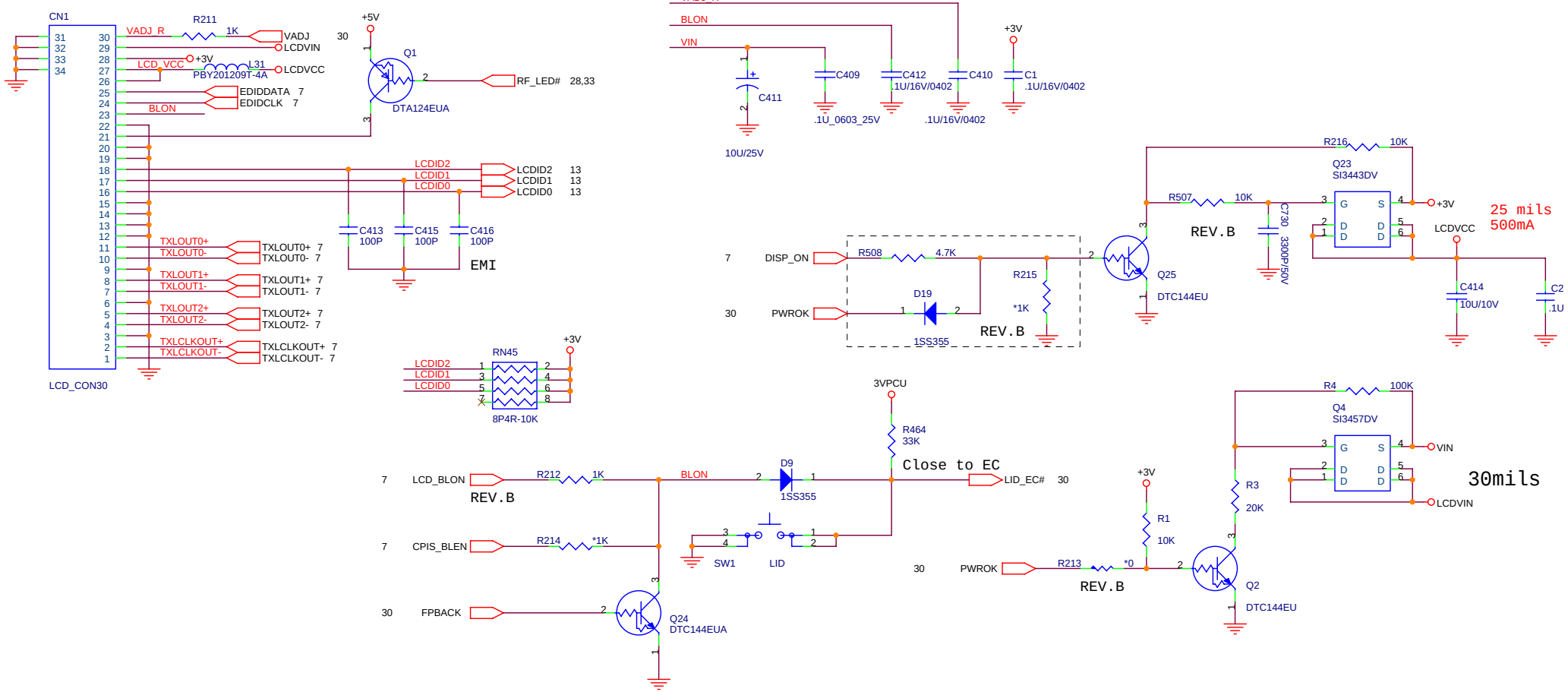
Size	Document Number	Rev
Custom	SB400-STRAPS	1A
Date: Monday, December 13, 2004	Sheet 16 of 42	

MINI PCI TYPE III SLOT



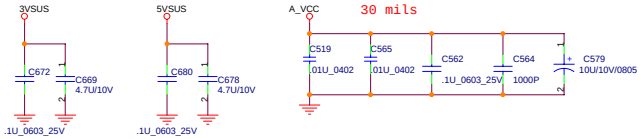
Size: Custom	Document Number		Rev: 1A
Date: Monday, December 13, 2004	Sheet 17 of 42		

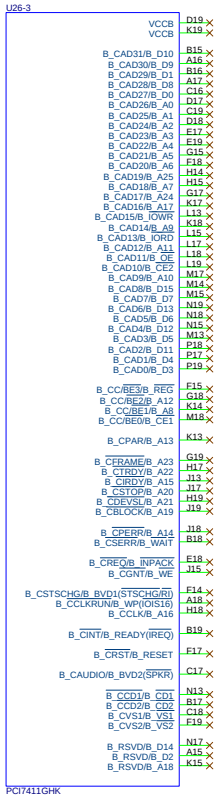
PROJECT : CT8
Quanta Computer Inc.

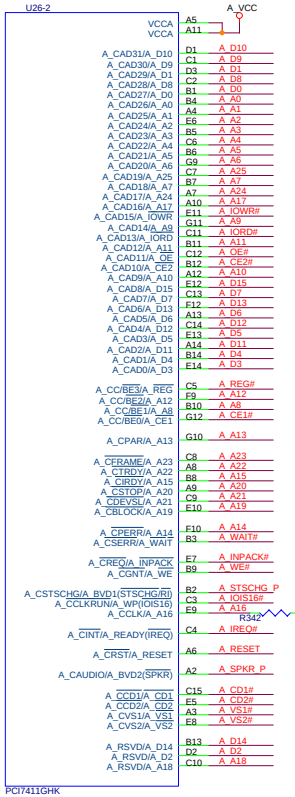


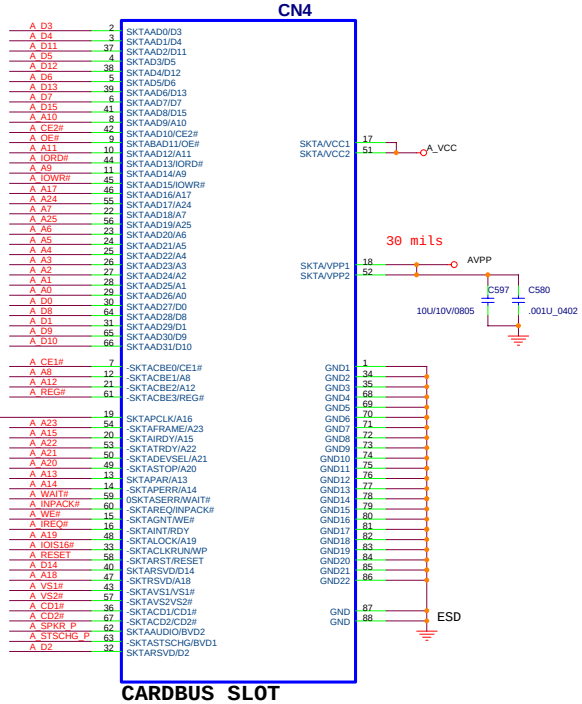
PROJECT : CT8			
Quanta Computer Inc.			
Size B	Document Number		Rev 1A
Date: Monday, December 13, 2004		Sheet 18 of 42	

CardBus Connector





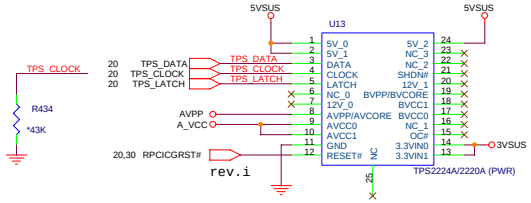




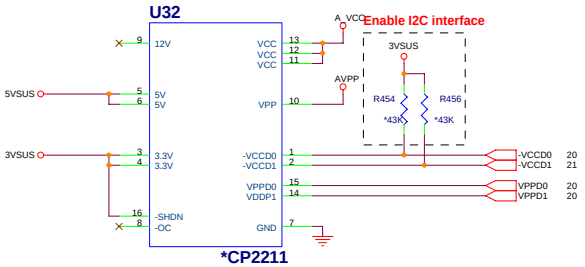
CARDBUS SLOT

FOX=WZ21131-G2

For PCI7411



For PCI1510

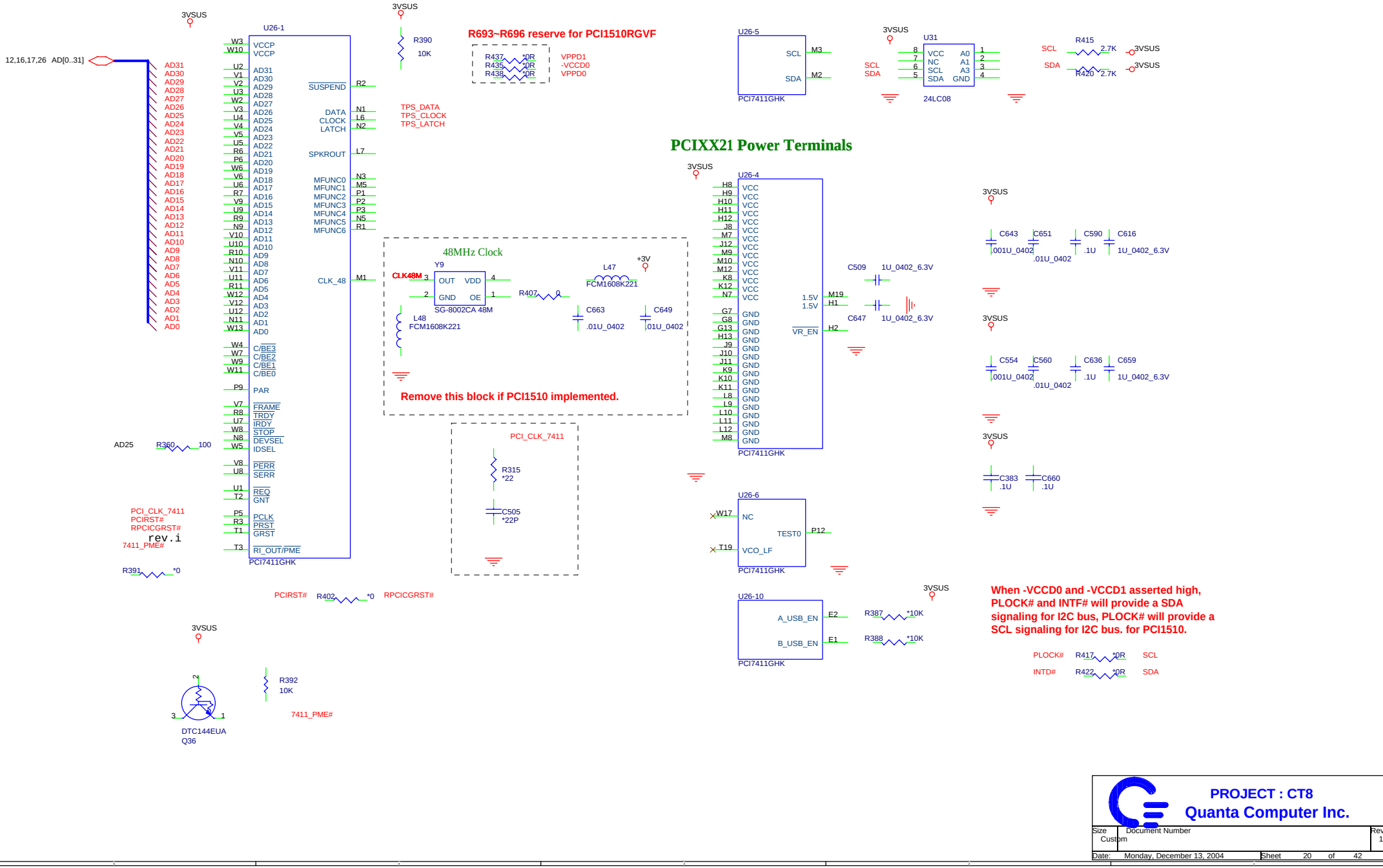


PROJECT : CT8

Quanta Computer Inc.

Size	Document Number	Rev
C		1A
Date: Monday, December 13, 2004	Sheet 19 of 42	

CardBus



PROJECT : CT8

Quanta Computer Inc.

Size	Document Number	Rev
Custom		1A
Date: Monday, December 13, 2004	Sheet 20 of 42	

CARD POWER CONTROL

For PCI1510

MC_PWR_CTRL_0#

SD_CDZ
MS_CDZ
SM_CDZ

MS_CLK_SD_CLK_SM_ELWPZ_R R406 22MS_CLK_SD_CLK_SM_ELWPZ
MS_BS_SD_CMD_SM_WEZ
MS_DATA3_SD_DAT3_SM_D3
MS_DATA2_SD_DAT2_SM_D2
MS_DATA1_SD_DAT1_SM_D1
MS_DATA0_SD_DAT0_SM_D0

SM_REZ
SM_ALE
SM_D4
SM_D5
SM_D6
SM_D7
SD_WP_SM_CEZ

SM_CLE
SM_RBZ

3VSUS

3VSUS

3VSUS

MC_PWR_CTRL_0#

30 mils

VCC_XD

CLOSE TO XD SOCKET

VCC_XD

VCC_XD

REV.B

SM_CDZ

SD_WP_SM_CEZ
MS_DATA1_SD_DAT1_SM_D1
MS_DATA0_SD_DAT0_SM_D0
MS_CLK_SD_CLK_SM_ELWPZ

R489 0
R492 0
R499 0

MS_BS_SD_CMD_SM_WEZ
MS_DATA3_SD_DAT3_SM_D3
MS_DATA2_SD_DAT2_SM_D2
MS_BS_SD_CMD_SM_WEZ
MS_DATA1_SD_DAT1_SM_D1
MS_DATA0_SD_DAT0_SM_D0
MS_DATA2_SD_DAT2_SM_D2
MS_CDZ
MS_DATA3_SD_DAT3_SM_D3
MS_CLK_SD_CLK_SM_ELWPZ

SM_D4
SM_D5

SD-DAT1
SD-DAT0
SD-CLK

SD-CMD
SD-DAT3
SD-DAT2
MS-BS
MS-DATA1
MS-DATA0
MS-DATA2

MS-DATA3
MS-CLK

XD-D4
XD-D5

XD-D6
XD-D7

XD-RE# R421 0
XD-CE# R416 0

XD-D3
XD-D2
XD-D1
XD-D0
XD-WP#
XD-WE#
XD-ALE R383 0
XD-CLE

SM_D6
SM_D7

SM_RBZ
SM_REZ
SD_WP_SM_CEZ

MS_DATA3_SD_DAT3_SM_D3
MS_DATA2_SD_DAT2_SM_D2
MS_DATA1_SD_DAT1_SM_D1
MS_DATA0_SD_DAT0_SM_D0

MS_BS_SD_CMD_SM_WEZ
SM_ALE
SM_CLE
SM_CDZ
SD_WP_SM_CEZ

SD_CDZ
MS_CLK_SD_CLK_SM_ELWPZ

SM-WP-SW

SD_CDZ

D14
1 2
*1SS355

SM_CDZ

REV.B

VCC_XD

R494
22

MC_PWR_CTRL_0#

REV.B

REV.B

rev.f

5 IN1 CARD READER

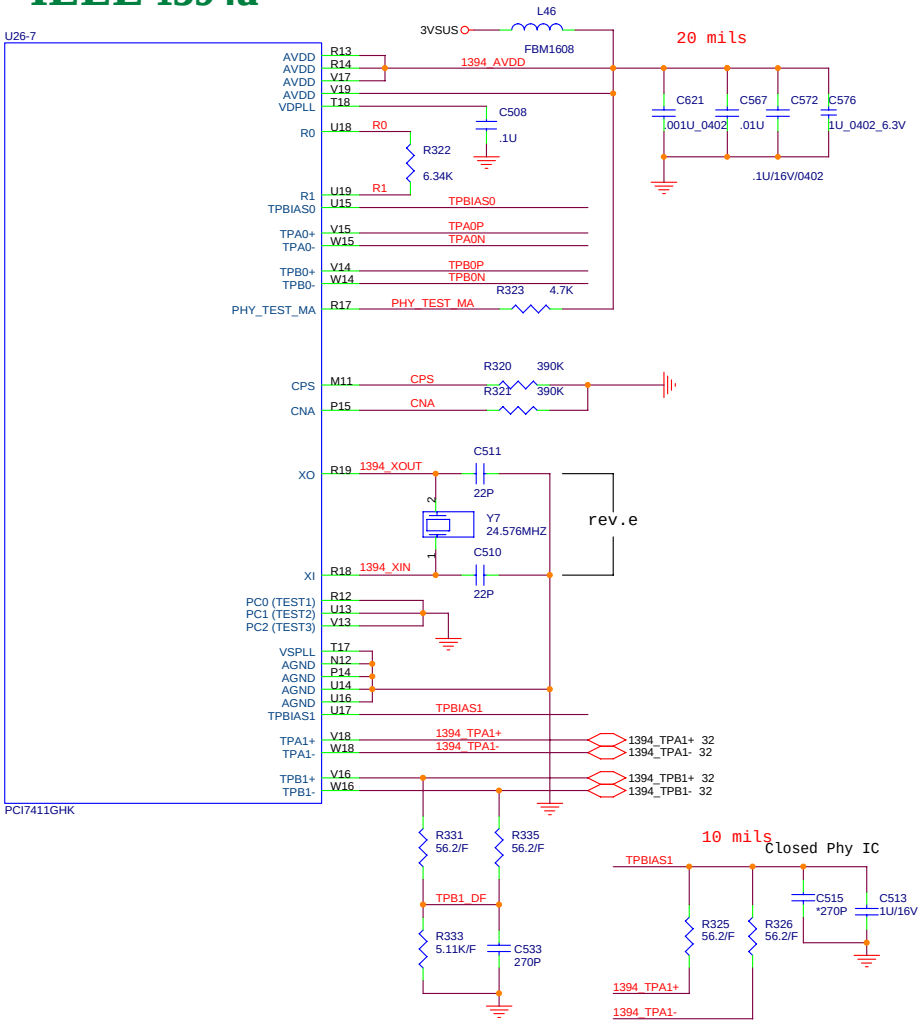
VCC_XD

XD-WP#

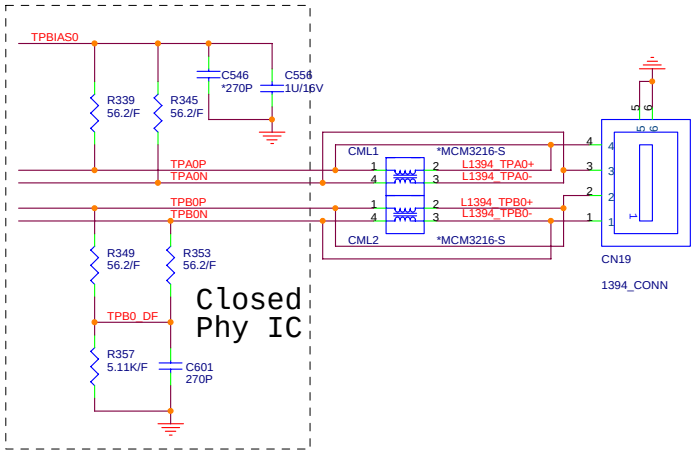
MS_CLK_SD_CLK_SM_ELWPZ

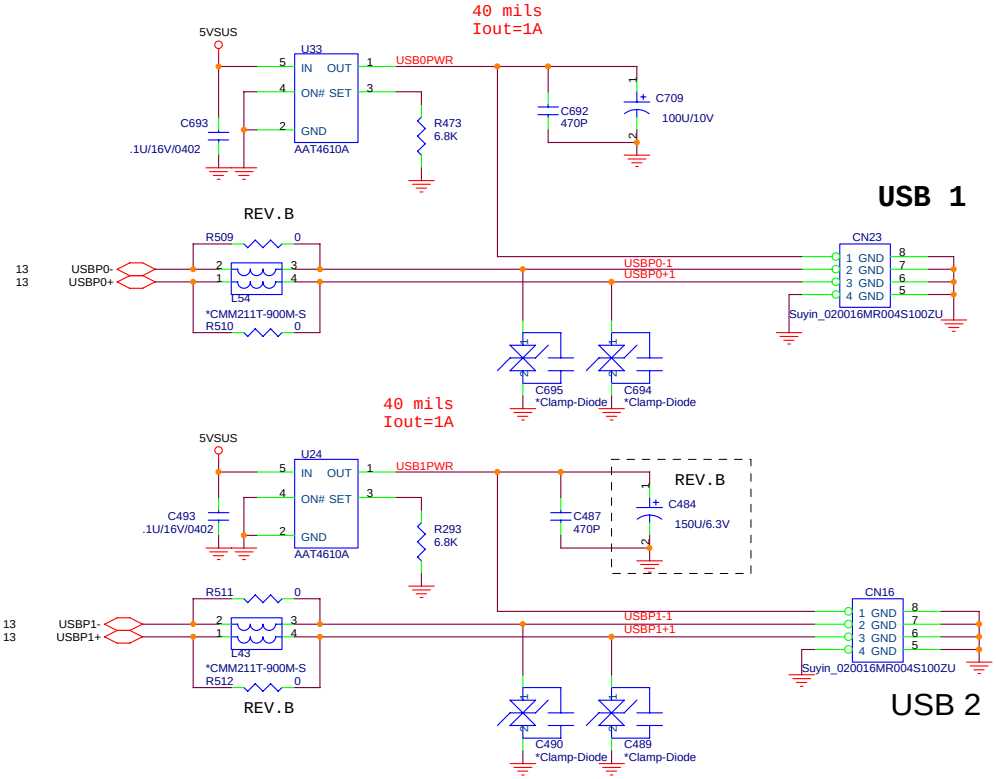
Size	Document Number	Rev
Custom		1A
Date: Monday, December 13, 2004	Sheet 21 of 42	

IEEE 1394a



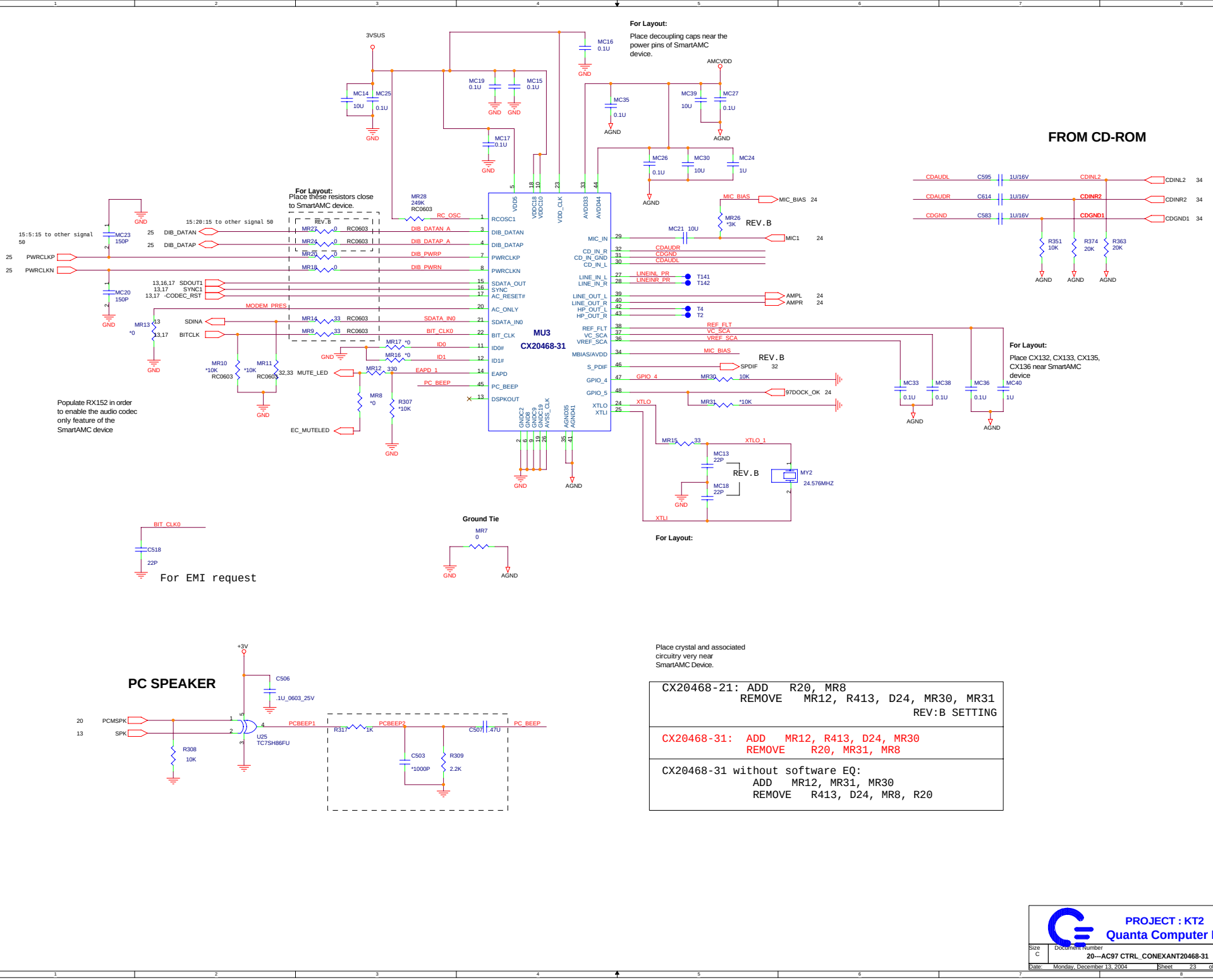
IEEE 1394 CONNECTOR





PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom		1A
Date: Monday, December 13, 2004	Sheet 22 of 42	


For Layout:
Place decoupling caps near the power pins of SmartAMC device.
FROM CD-ROM
For Layout:
Place these resistors close to SmartAMC device.
MU3
CX20468-31
REV.B
Populate RX152 in order to enable the audio codec only feature of the SmartAMC device
For Layout:
Place CX132, CX133, CX135, CX136 near SmartAMC device
Ground Tie
For EMI request
PC SPEAKER
U25
TC7SH86FU
Place crystal and associated circuitry very near SmartAMC Device.
CX20468-21: ADD R20, MR8
REMOVE MR12, R413, D24, MR30, MR31
REV:B SETTING
CX20468-31: ADD MR12, R413, D24, MR30
REMOVE R20, MR31, MR8
CX20468-31 without software EQ:
ADD MR12, MR31, MR30
REMOVE R413, D24, MR8, R20
PROJECT : KT2
Quanta Computer Inc.
Size C
Document Number 20---AC97 CTRL_CONEXANT20468-31
Rev 1A
Date: Monday, December 13, 2004
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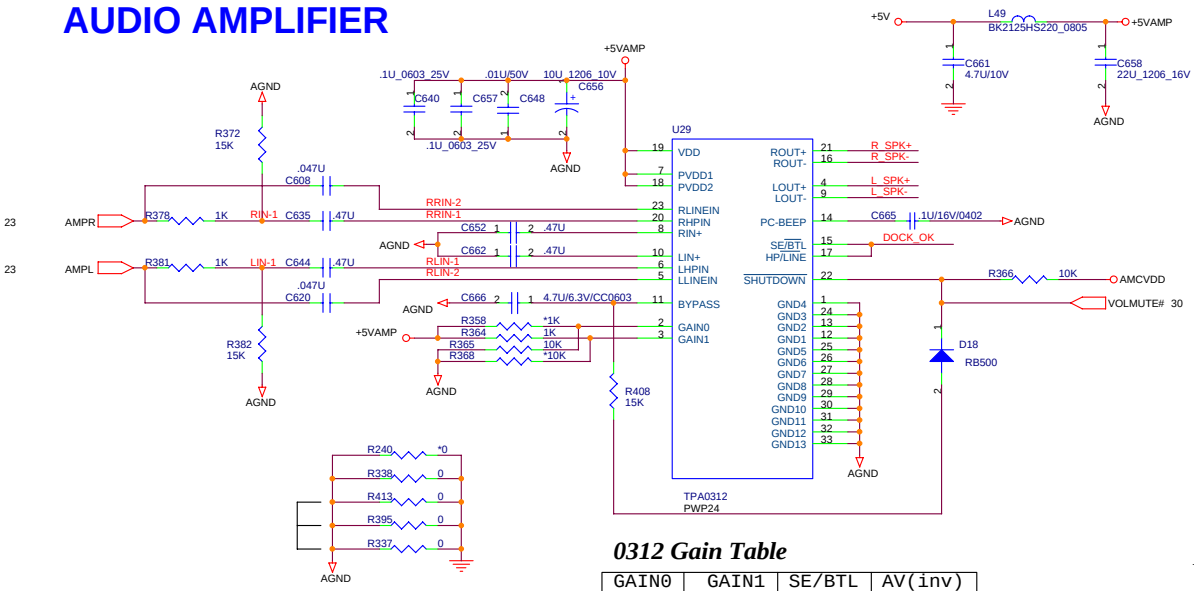
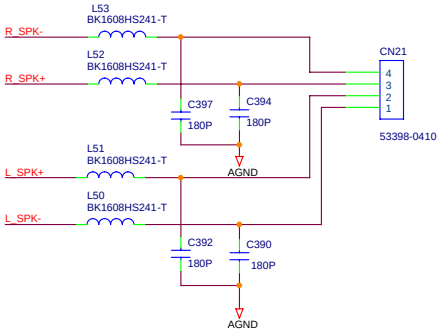
AUDIO AMPLIFIER

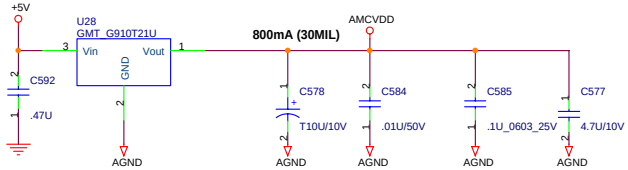


0312 Gain Table

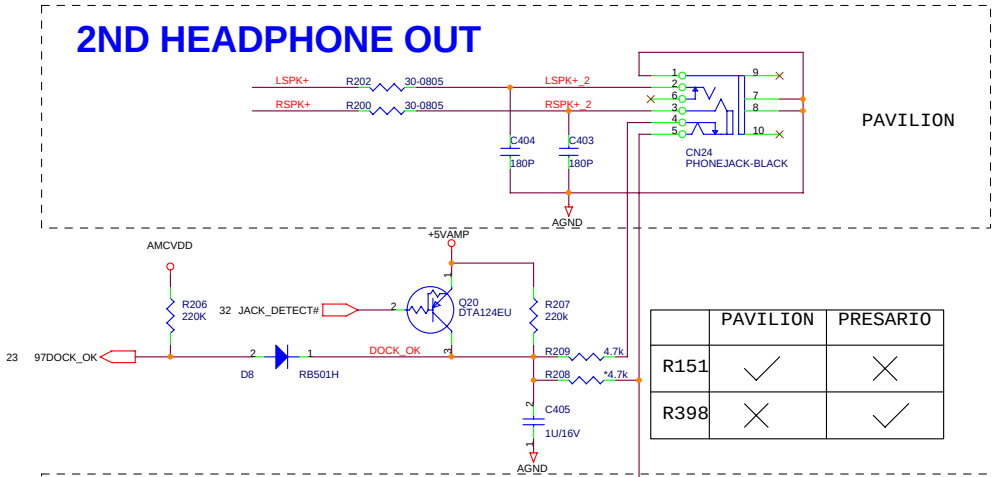
GAIN0	GAIN1	SE/BTL	AV(inv)
0	0	0	6 dB
0	1	0	10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB

SPEAKER OUT



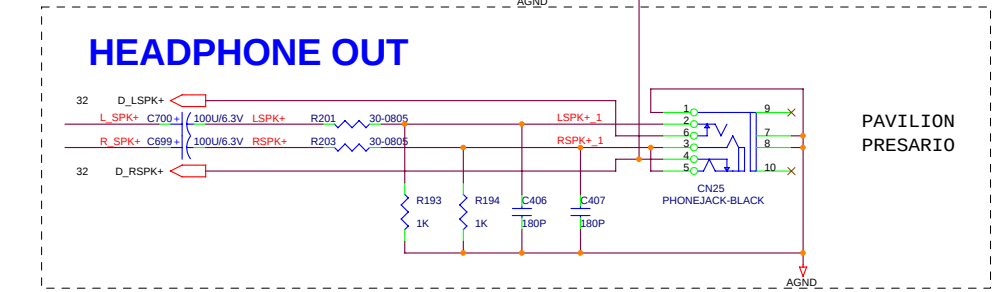


2ND HEADPHONE OUT

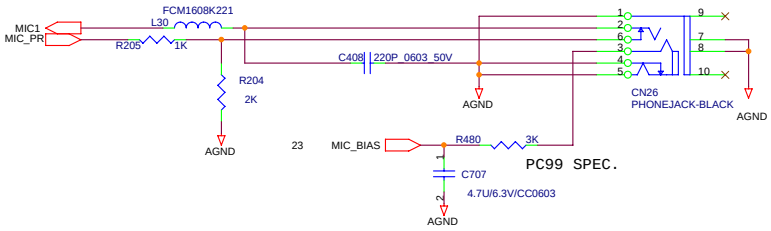


	PAVILION	PRESARIO
R151	✓	✗
R398	✗	✓

HEADPHONE OUT



MICROPHONE



PROJECT : CT1
Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO AMP_ TI-TPA0312	1A
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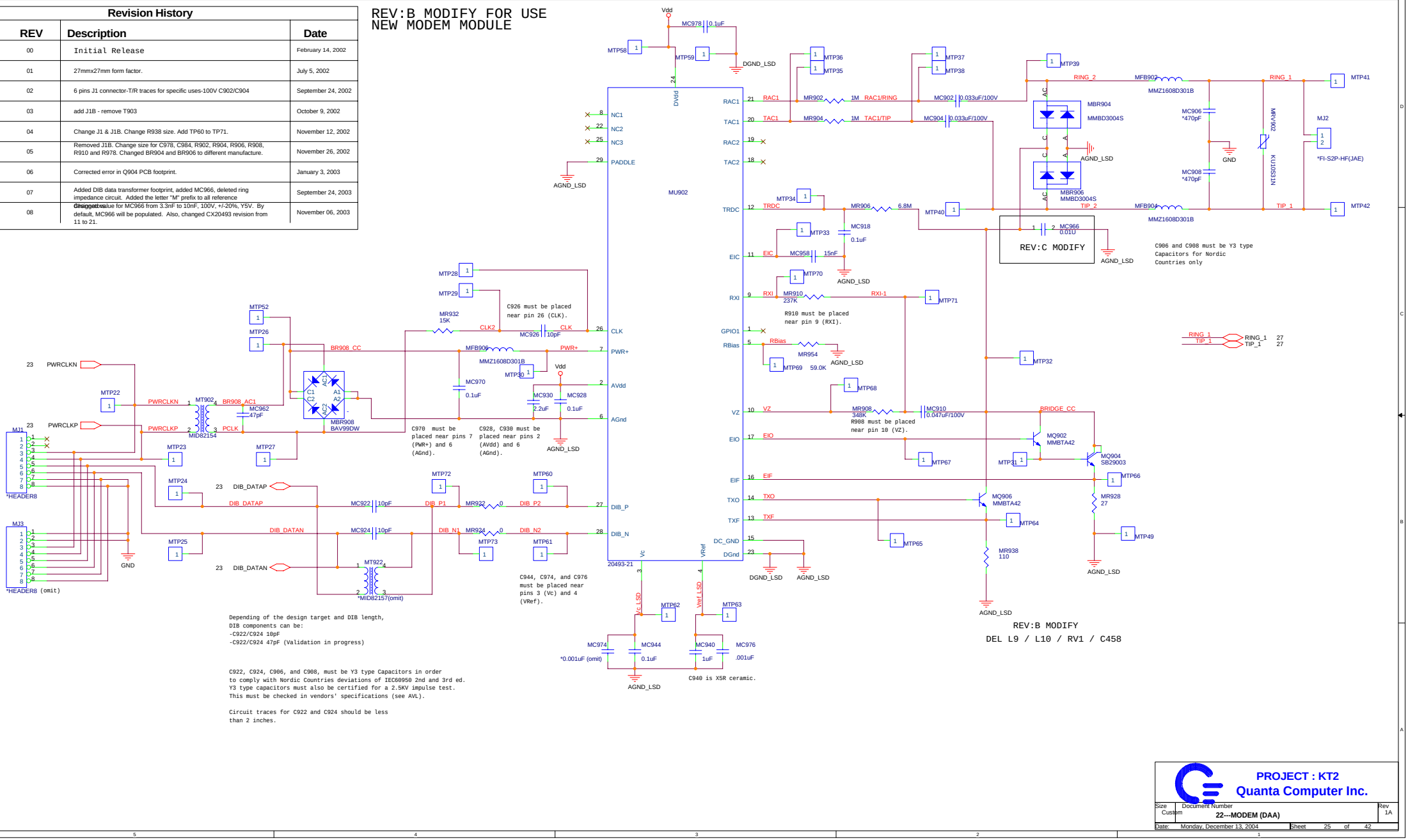
Revision History

REV	Description	Date
00	Initial Release	February 14, 2002
01	27mmx27mm form factor.	July 5, 2002
02	6 pins J1 connector-T/R traces for specific uses-100V C902/C904	September 24, 2002
03	add J1B - remove T903	October 9, 2002
04	Change J1 & J1B. Change R938 size. Add TP60 to TP71.	November 12, 2002
05	Removed J1B. Change size for C978, C984, R902, R904, R906, R908, R910 and R978. Changed BR904 and BR906 to different manufacture.	November 26, 2002
06	Corrected error in Q904 PCB footprint.	January 3, 2003
07	Added DIB data transformer footprint, added MC966, deleted ring impedance circuit. Added the letter "M" prefix to all reference designations.	September 24, 2003
08	Changed value for MC966 from 3.3nF to 10nF, 100V, +/-20%, Y5V. By default, MC966 will be populated. Also, changed CX20493 revision from 11 to 21.	November 06, 2003

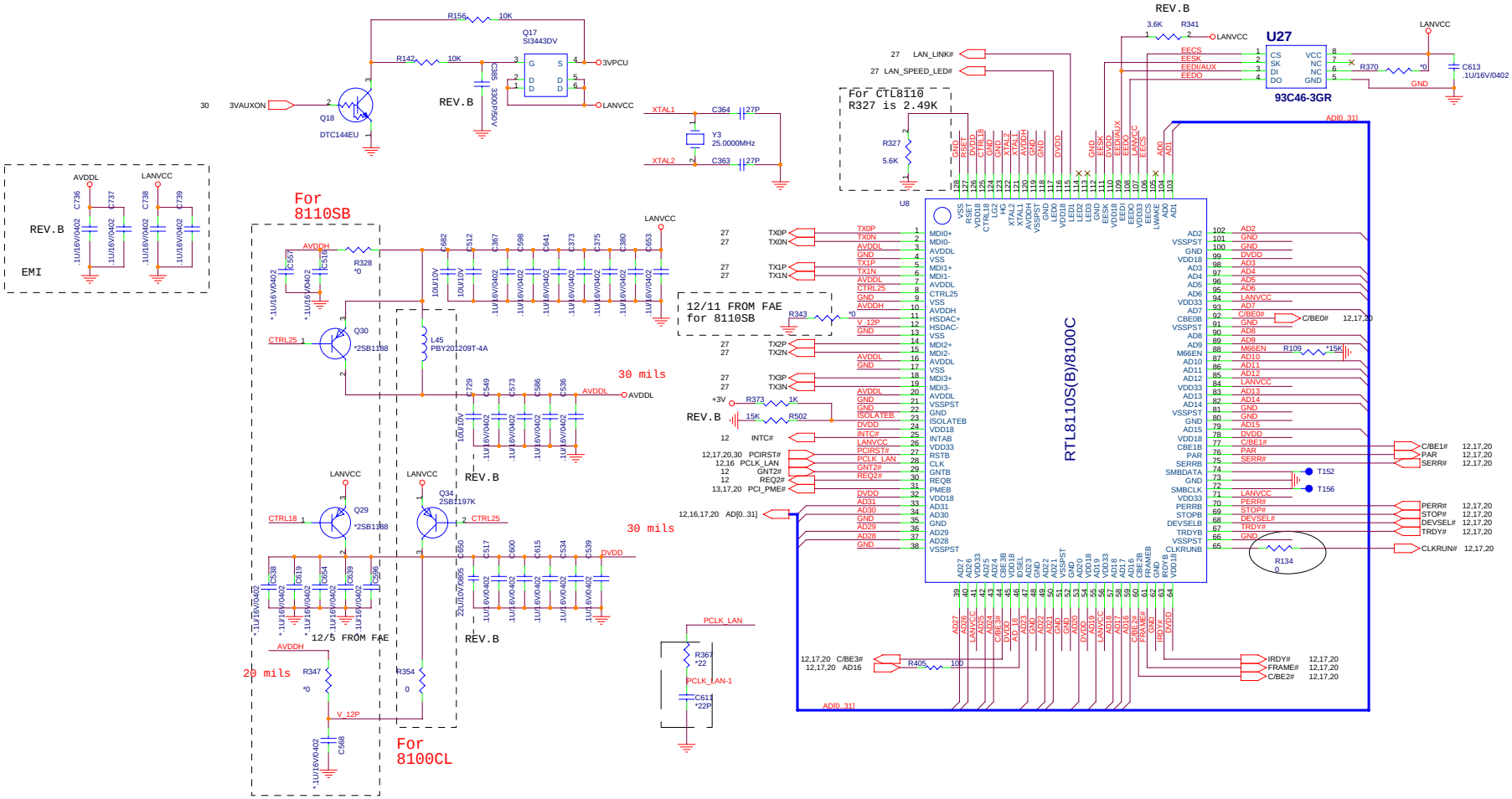
REV:B MODIFY FOR USE
NEW MODEM MODULE



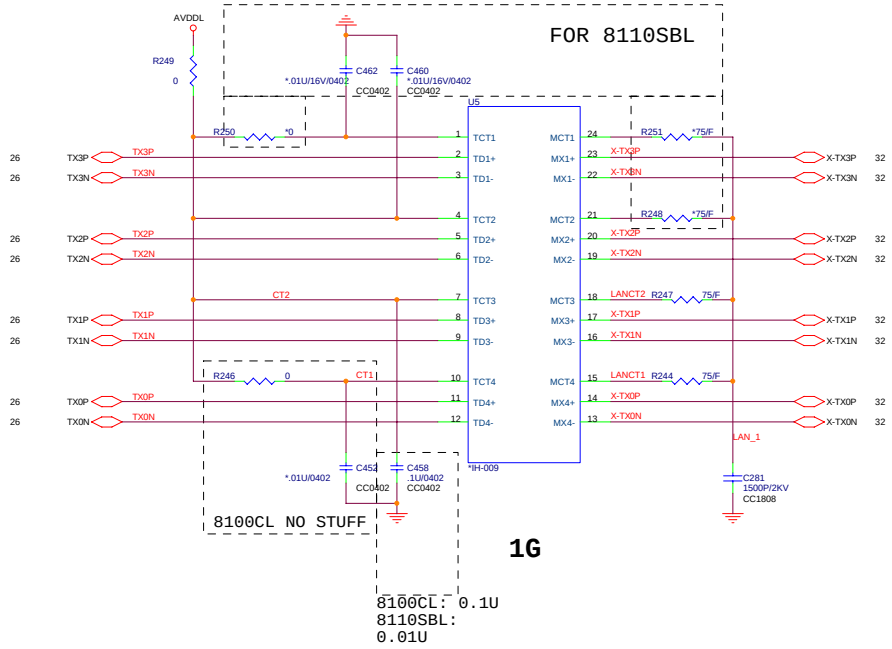
PROJECT : KT2
Quanta Computer Inc.

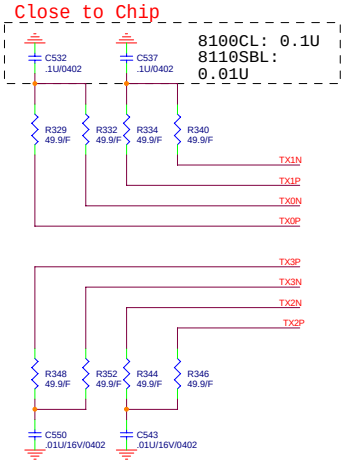
Size	Document Number	Rev
Custom	22---MODEM (DAA)	1A
Date: Monday, December 13, 2004	Sheet 25 of 42	

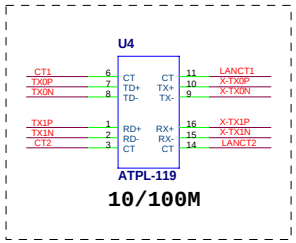
	8100CL(10/100M)	8110SB(1G)
DVDD33	3.3VD 26,41,56,71,84,94,107	3.3VD 26,41,56,71,84,94,107
AVDDL	3.3VA 3,7,20	2.5VA 3,7,20,16
DVDD	2.5VD 32,54,78,99	1.8VD 32,54,78,99,24,45,64,110,116,126
AVDD25	2.5VA 12	NC
AVDDH	NC	3.3VA 10,120

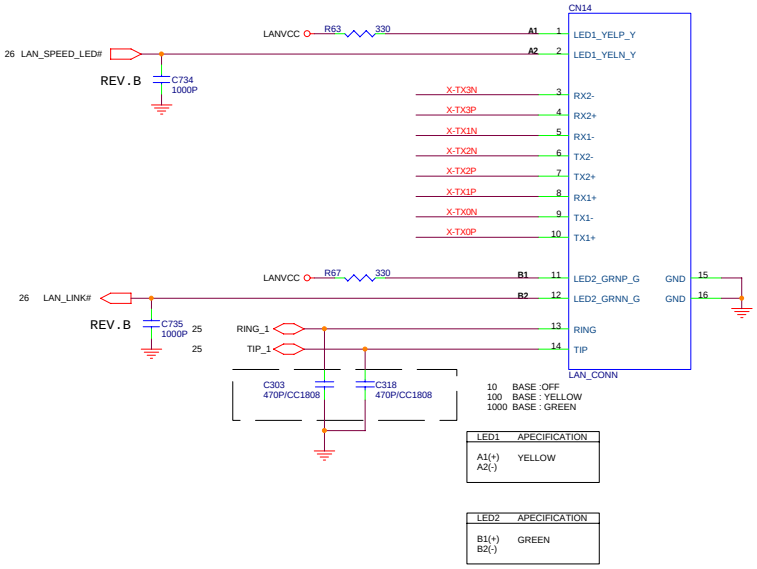


PROJECT : CT8 Quanta Computer Inc.			
Size C	Document Number RTL8100CL		Rev 1A
Date: Monday, December 13, 2004		Sheet 26 of 42	









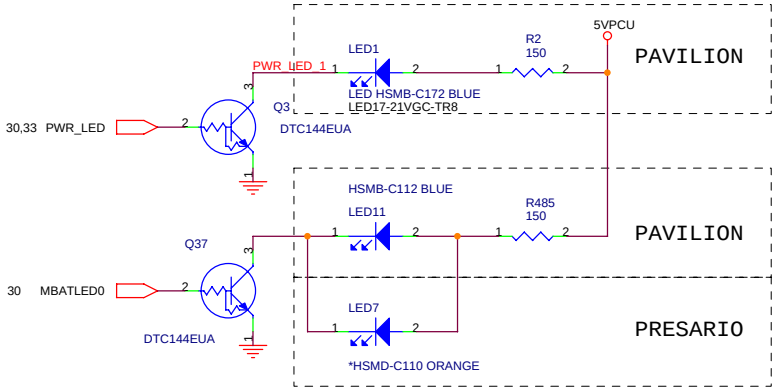
LED1	APECIFICATION
A1(+) A2(-)	YELLOW

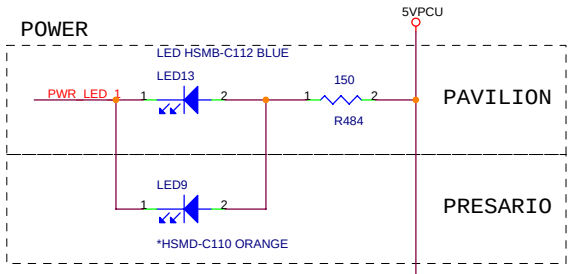
LED2	APECIFICATION
B1(+) B2(-)	GREEN

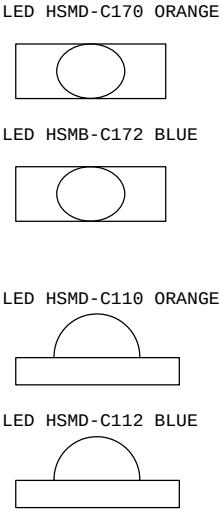
PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
C		1A

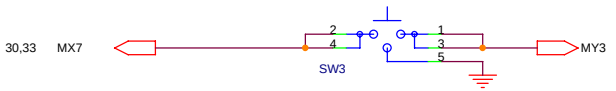
Date: Monday, December 13, 2004 Sheet 27 of 42

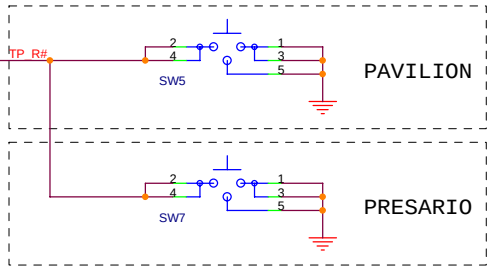


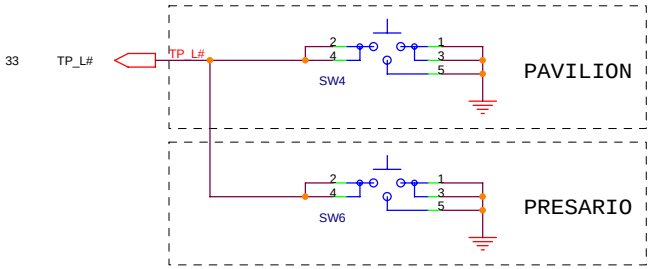


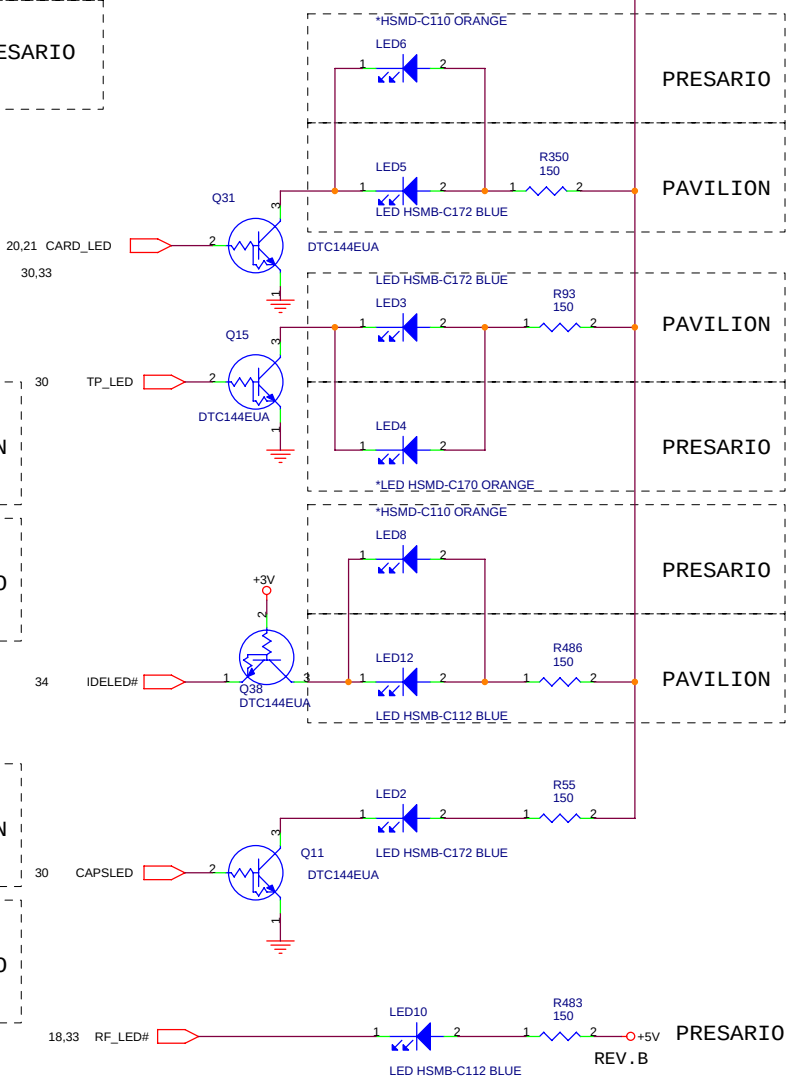


Touchpad control







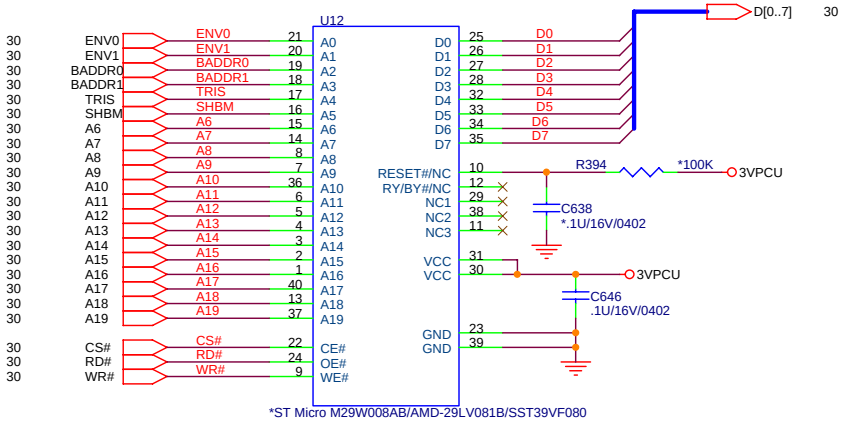


REV.B: LED7 AND LED8 SWAP

PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom		1A
Date: Monday, December 13, 2004	Sheet 28 of 42	

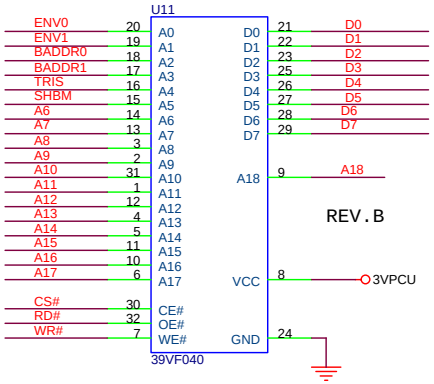
8Mbit (1M Byte), TSSOP40



AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC

1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326_UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
2.SIO has internal 20 mS delay of VCC1_PWROK

4Mbit (512k Byte), TSSOP32



PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
B		1A

Date: Monday, December 13, 2004 Sheet 29 of 42

KBC-NS87551L

LDRQ#(pin 8) internal is no use

U30 — PC97551

Host interface: SERIRQ, LDRQ, LFRAME, LAD0–LAD3, LCLK, LRESET, SMI, PWUREQ

AD Input: AD0–AD3, DP/AD8, DN/AD9

DA output: DA0–DA3

PWM or PORT-A: IOPA0/PWM0 – IOPA7/PWM7

PORT-B: IOPB0/URXD, IOPB1/UTXD, IOPB2/USCLK, IOPB3/SCL1, IOPB4/SDA1, IOPB7/RING/PFAIL

Key matrix scan: KBSIN0–KBSIN7, KBSOUT0–KBSOUT15

PORT-C: IOPC0–IOPC7/CLKOUT

PORT-D-1: IOPD0/RI1#/EXWINT20, IOPD1/RI2/EXWINT21, IOPD2/EXWINT24

PORT-E: IOPE4/SWIN, IOPE5/EXWINT40, IOPE6/LPCPD/EXWIN45, IOPE7/CLKRUN/EXWINT46

JTAG debug port: TINT, TCK, TDO, TDI, TMS

PORT-H: IOPH0/A0/ENV0 – IOPH7/A7

PS2 interface: PSCLK1/IOPF0, PSDAT1/IOPF1, PSCLK2/IOPF2, PSDAT2/IOPF3, PSCLK3/IOPF4, PSDAT3/IOPF5, PSCLK4/IOPF6, PSDAT4/IOPF7

PORT-I: IOPI0/D0 – IOPI7/D7

PORT-J-1: IOPJ0/RD#, IOPJ1/WR#

PORTJ-2: IOPJ2/BST0, IOPJ3/BST1, IOPJ4/BST2, IOPJ5/PFS, IOPJ6/PLI, IOPJ7/BRKL_RSTO

PORT-D-2: IOPD4–IOPD7

PORT-K: IOPK0/A8 – IOPK7/A15/CBRST

PORT-M: IOPM0/D8 – IOPM7/D15

PORT-L: IOPL0/A16 – IOPL4/WR1

SELIO, SELO, SEL1, CLK

GND1–GND7, AGND, NC1–NC10

RESERCE FOR 97551

Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

I/O Address

BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

SHBM=1: Enable shared memory with host BIOS

REV.B

PRESARIO

PAVILION

Pin 24 if no pull-high, will can't reboot.

Pin 103 internal is "A19",Can't use to GPIO

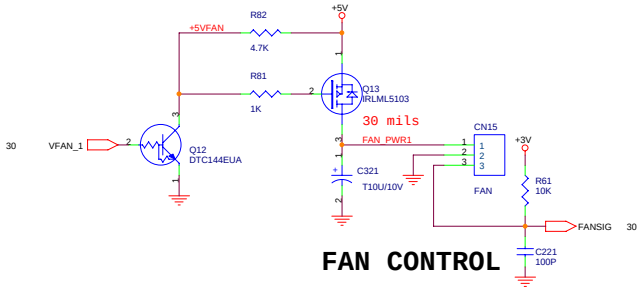
CLOSE TO U28

07/19

LPC Debug Port

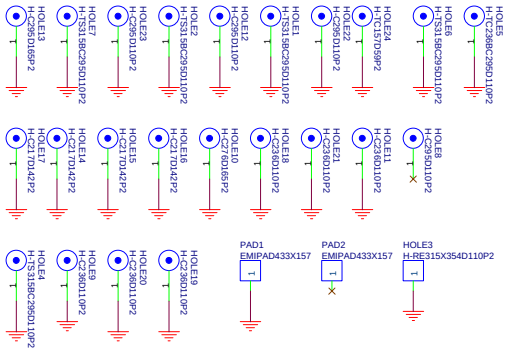
*EIC-3801-15

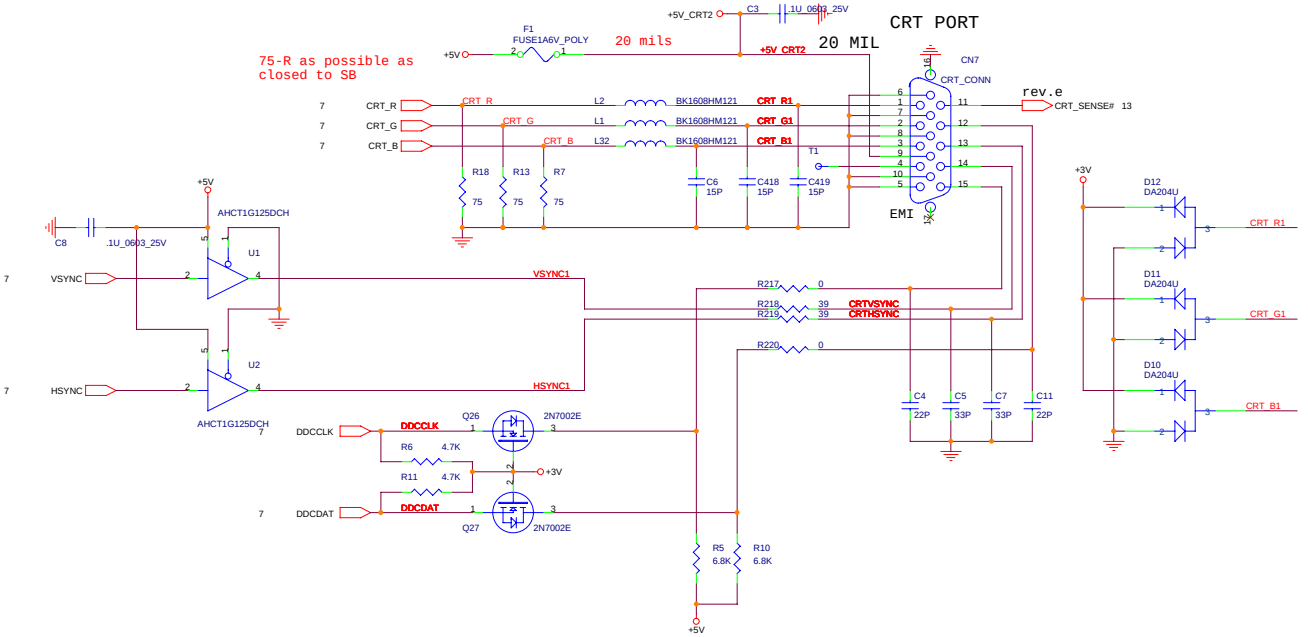
PROJECT : CT8		
Quanta Computer Inc.		
Size: C	Document Number	Rev: 1A
Date: Monday, December 13, 2004	Sheet 30 of 42	

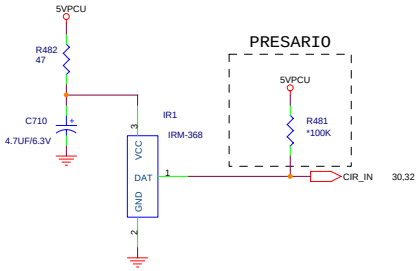


FAN CONTROL

REV.B







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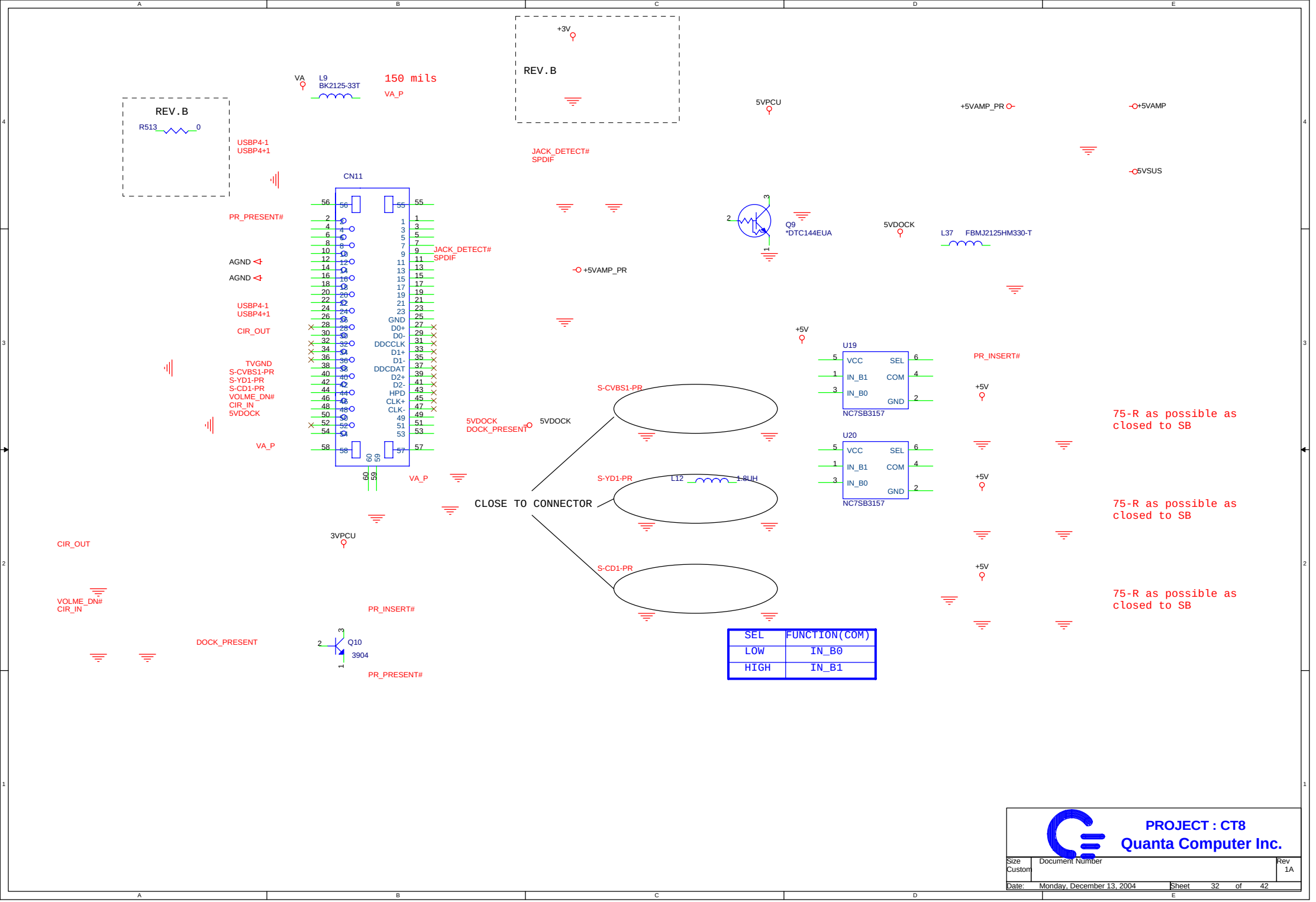
REV.B
R513
0
USBP4-1
USBP4+1
PR_PRESENT#
AGND
AGND
USBP4-1
USBP4+1
CIR_OUT
TVGND
S-CVBS1-PR
S-YD1-PR
S-CD1-PR
VOLME_DN#
CIR_IN
5VDOCK
VA_P
CIR_OUT
VOLME_DN#
CIR_IN
DOCK_PRESENT
VA
L9
BK2125-33T
150 mils
VA_P
CN11
JACK_DETECT#
SPDIF
VA_P
3VPCU
PR_INSERT#
Q10
3904
PR_PRESENT#
+3V
REV.B
5VPCU
JACK_DETECT#
SPDIF
+5VAMP_PR
5VDOCK
DOCK_PRESENT
5VDOCK
S-CVBS1-PR
S-YD1-PR
S-CD1-PR
CLOSE TO CONNECTOR
L12
1.8UH
3VPCU
PR_INSERT#
Q10
3904
PR_PRESENT#
+5VAMP_PR
Q9
*DTC144EUA
5VDOCK
L37
FBMJ2125HM330-T
+5V
U19
VCC
IN_B1
IN_B0
SEL
COM
GND
NC7SB3157
U20
VCC
IN_B1
IN_B0
SEL
COM
GND
NC7SB3157
PR_INSERT#
+5V
+5V
+5V
+5VAMP_PR
+5VAMP
5VSUS
75-R as possible as closed to SB
75-R as possible as closed to SB
75-R as possible as closed to SB
SEL
FUNCTION(COM)
LOW
IN_B0
HIGH
IN_B1
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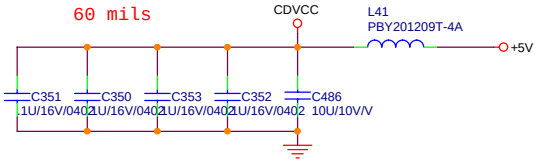
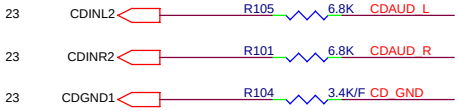
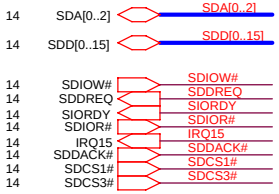
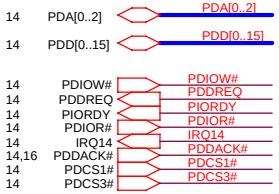
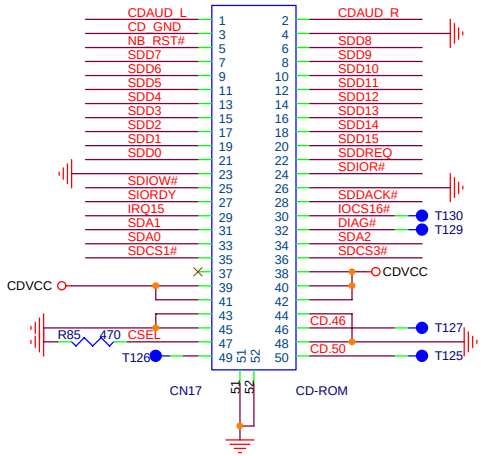
CD-ROM

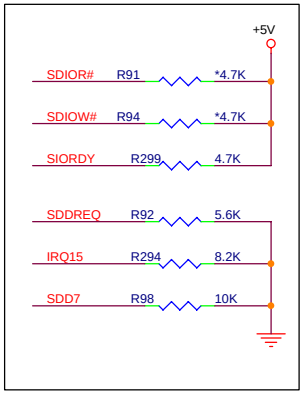




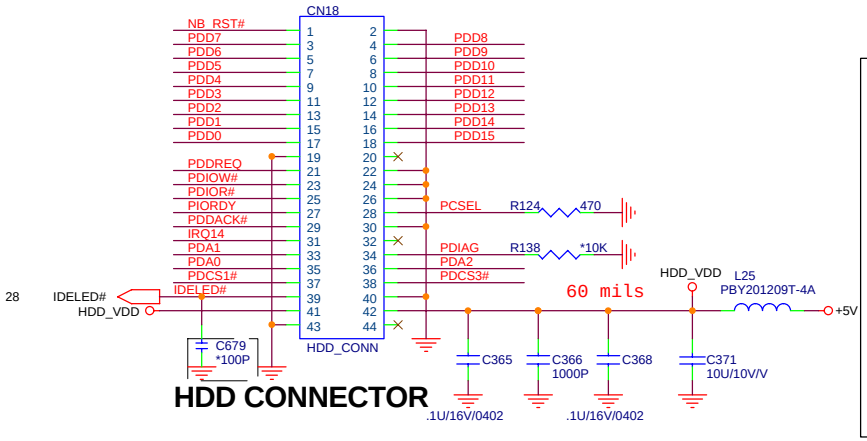


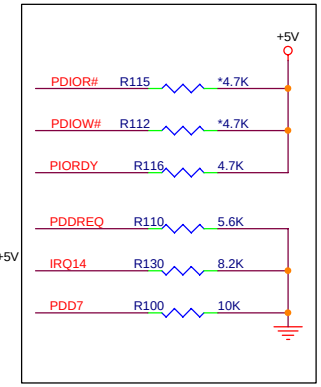






HDD CONNECTOR





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Custom	HDD CD-ROM	1A
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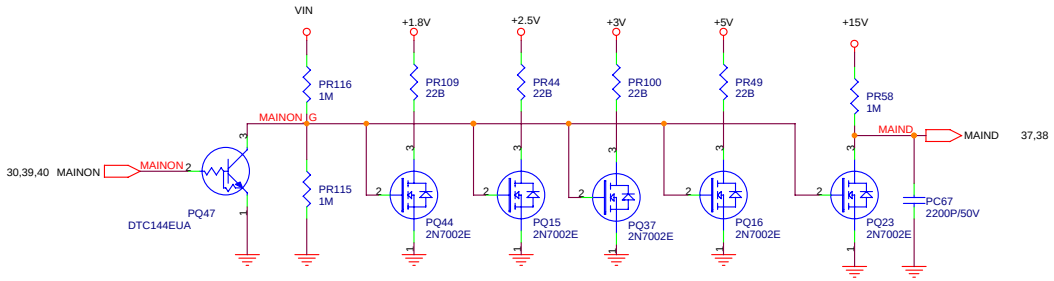
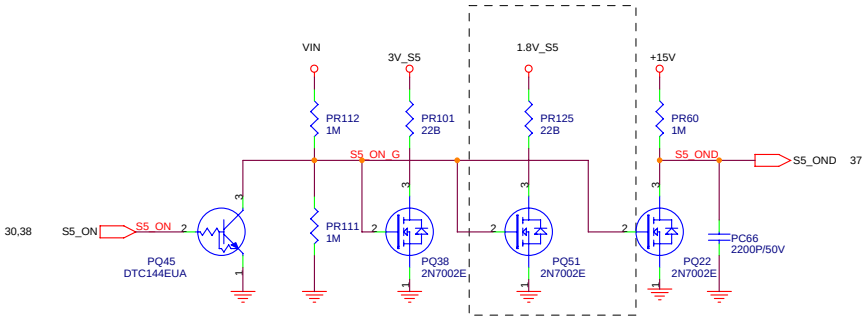
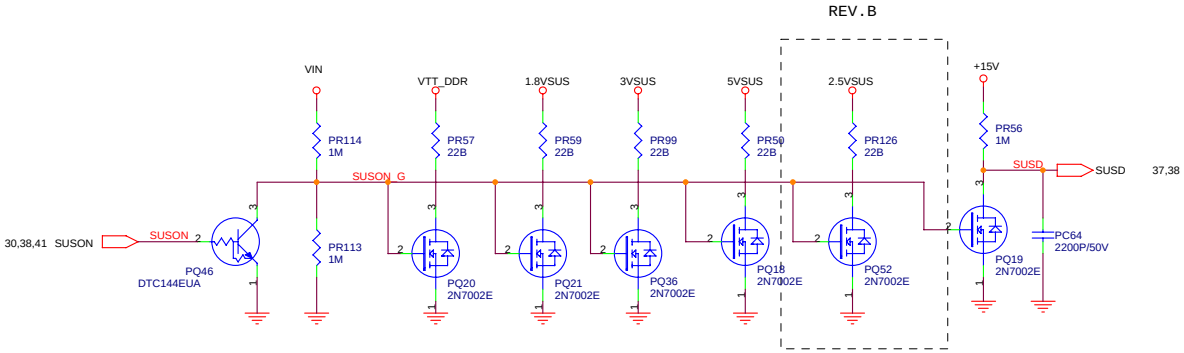


REV.B



REV.B



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Custom	**30---DISCHARGE**	1A
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BATTERY CHARGER

ADAPTER 18.5V 65W 3.51A

From Docking CNN

VA — PD2 SBM1040 — PR25 10K

VA2 — PD8 SBM1040 — PR66 10K — PC73 .1U/50V — PC75 .1U/50V

JP1 POWER JACK — PL8 FBMJ3216HS480NT(6A) — PL1 FBMJ3216HS480NT(6A)

VA3

REV.B

PR63 0.033/1W/3720 — PQ24 AO4407 — PQ10 DTA124EUA — PC47 1U/50V — PC37 .1U/50V

VIN — 18,32,35,37,38,39,40

20 MIL TO CABLE DOCK

REV.B

PQ33 AO4407

PR30 200K — PR31 100K — PQ8 SI4814 — PC18 .1U/50V

PL10 15uH/4.4A/CDRH104R — PR89 0.05/1W/3720 — PR24 4.7 — PR22 4.7 — PC29 .1U/50V — PC26 .1U/50V

PC99 10U/25V — PC100 10U/25V MBAT+ — PC98 10U/25V

PR38 4.7 — PR32 4.7 — PC38 .1U/50V — PC44 .1U/50V — PR43 10K

PL4 FBMJ3216HS800 — PC19 10U/25V — PC16 10U/25V — PC17 10U/25V — PC34 .1U/50V

PC32 1U/10V/X7R — CSIP — CSIN

1772_5.4V — PR42 33 — PD6 SW2020C

ACOK — PR11 100K — PD1 CH501H-40 — PQ11 2N7002E — D/C# — D/C# 30 — PQ50 2N7002E — PR120 47K

5VPCU — PD16 SW2020C — VIN — PR117 47.5K/F — PR118 37.4K/F — PU8 LMV331 — PR119 100K — BL/C# — BL/C# 30 — PQ48 2N7002E

Battery Low 7.5V

CSSN — CSSP — SYS_I 30 — PR39 12.4K/F

MAX1772EEI

INP CSSP CSSN BST DHI LX DLOV DLO PGND CSIP CSIN BATT CELLS VCTL

DCIN LDO CLS REF CCS CCI CCV GND GND ICHG ACIN ACOK REFIN ICTL

PU1

10K/F — PR14 — REF4.096 — PR13 2.61K/F

1772_5.4V — PR15 100K — PR12 100K — 3VPCU — PQ49 2N7002E — CELL-SET 30

VA — PD3 CH501H-40 — VA2 — PD9 CH501H-40

AD_AIR 30 — PR62 12.4K/F — PR61 75K/F — PR41 75K/F — PR40 13.7K/F

REV.B

PQ53 2N7002E — PD17 CH501H-40 — PB127 30 — PR127 1M — PC144 1U/25V

ACOK — PQ6 DTA124EUA — PR121 10K — PR122 15K — ACIN

PC101 1U/50V — 1772_5.4V — PC46 1U/10V/X7R — REF4.096 — PR35 100K/F — PR36 121K/F

PR23 1K — PC36 — PC33 — PC30 — PC23 .1U/50V — .01U/50V — .1U/10V/X7R

REV.B

3VPCU — 3VPCU 18,26,29,30,32,37 — PC22 .1U/50V

PR17 10K — CC-SET — CC-SET 30

CC-SET = 1.05V/A

CELL-SET

HI = LDO = 4 CELL

LOW = LDO/2 = 3 CELL

3VPCU — PR18 10K/F — PC25 .01U/50V

1ST_BAT_CONN — CN9

PL9 FBMJ3216HS480NT(6A) — MBAT+ — PR27 100K/F — PC24 .01U/50V — TEMP_MBAT 30

PR20 100 — PR19 100

MBDATA — 3,30 MBDATA — PD5 ZD5.6V

MBCLK — MBCLK 3,30 — PD4 ZD5.6V

MBATV — MBATV 30 — PC31 .01U/50V — PR28 14K/F

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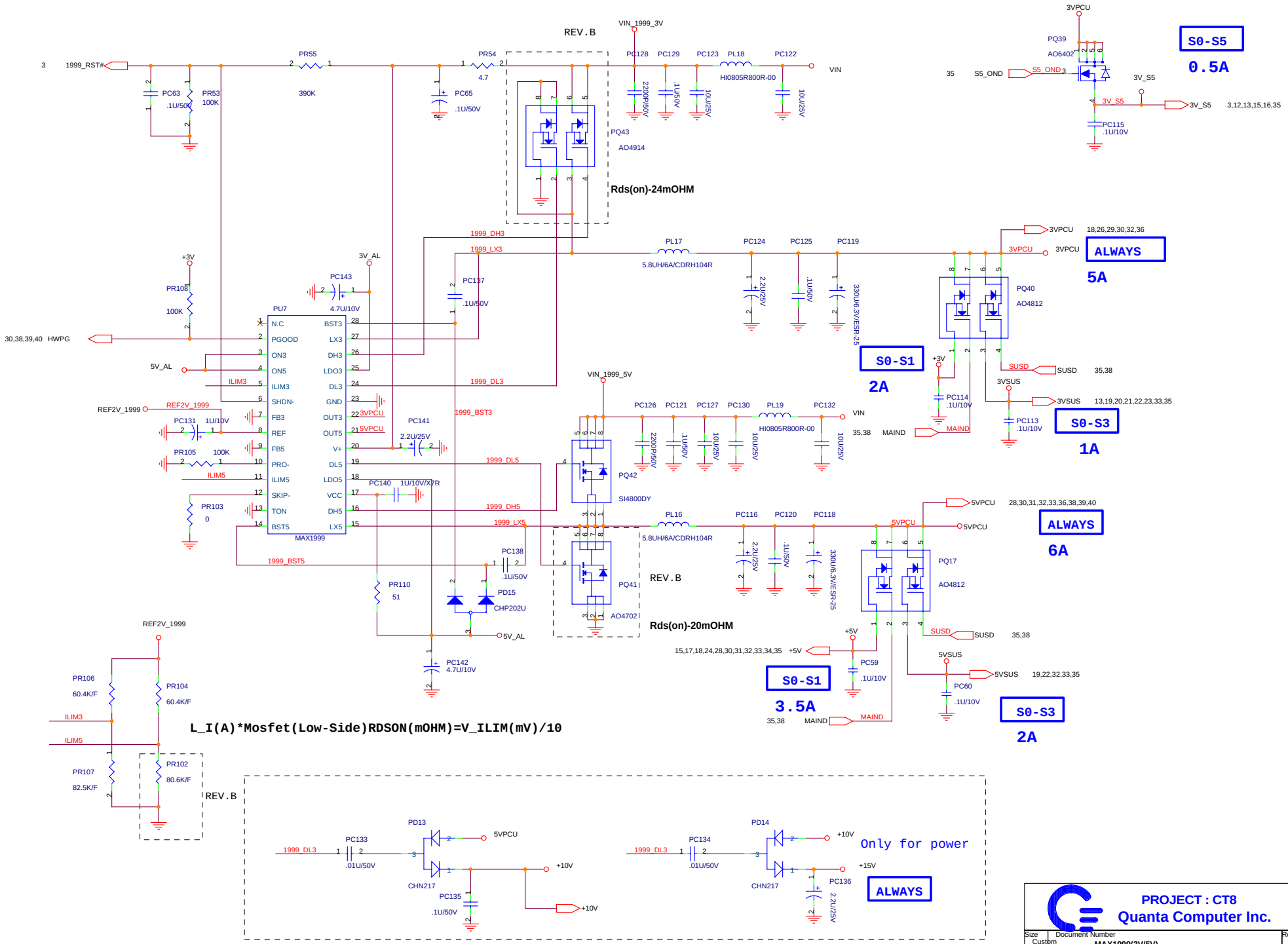
REV.B
VIN_1999_3V
1999_RST#
PR55
390K
PR54
4.7
PC63
.1U/50V
PR53
100K
PC65
.1U/50V
PC128
PC129
PC123
PL18
PC122
HI0805R800R-00
220P/50V
.1U/50V
10U/25V
10U/25V
VIN
PQ43
AO4914
Rds(on)-24mOHM
3VPCU
PQ39
AO6402
S5_OND
35
S5_OND
3V_S5
3V_S5
3V_S5
3,12,13,15,16,35
PC115
.1U/10V
S0-S5
0.5A
1999_DH3
1999_LX3
PL17
5.8UH/6A/CDRH104R
PC124
PC125
PC119
2.2U/25V
.1U/50V
330U/6.3V/ESR-25
3VPCU
3VPCU
18,26,29,30,32,36
ALWAYS
5A
PQ40
AO4812
+3V
PR108
100K
30,38,39,40 HWPG
3V_AL
PC143
4.7U/10V
PC137
.1U/50V
PU7
N.C
PGOOD
ON3
ON5
ILIM3
SHDN-
REF
FB3
FB5
PRO-
ILIM5
SKIP-
TON
BST5
BST3
LX3
DH3
LDO3
DL3
GND
OUT3
OUT5
V+
DL5
LDO5
VCC
DH5
LX5
MAX1999
5V_AL
ILIM3
REF2V_1999
PC131
1U/10V
PR105
100K
ILIM5
PR103
0
3VPCU
5VPCU
PC141
2.2U/25V
PC140
1U/10V/X7R
1999_BST3
1999_DL3
1999_DL5
1999_DH5
1999_LX5
1999_BST5
PR110
51
PC138
.1U/50V
PD15
CHP202U
PC142
4.7U/10V
VIN_1999_5V
PC126
PC121
PC127
PC130
PL19
PC132
HI0805R800R-00
220P/50V
.1U/50V
10U/25V
10U/25V
VIN
35,38
MAIND
PQ42
SI4800DY
PL16
5.8UH/6A/CDRH104R
PC116
PC120
PC118
2.2U/25V
.1U/50V
330U/6.3V/ESR-25
5VPCU
5VPCU
28,30,31,32,33,36,38,39,40
ALWAYS
6A
PQ17
AO4812
PQ41
AO4702
REV.B
Rds(on)-20mOHM
S0-S1
2A
+3V
PC114
.1U/10V
SUSD
SUSD
35,38
3VSUS
3VSUS
13,19,20,21,22,23,33,35
PC113
.1U/10V
S0-S3
1A
+5V
15,17,18,24,28,30,31,32,33,34,35
+5V
PC59
.1U/10V
5VSUS
5VSUS
19,22,32,33,35
PC60
.1U/10V
S0-S1
3.5A
35,38
MAIND
MAIND
S0-S3
2A
REF2V_1999
PR106
60.4K/F
PR104
60.4K/F
ILIM3
ILIM5
PR107
82.5K/F
PR102
80.6K/F
REV.B
L_I(A)*Mosfet(Low-Side)RDSON(mOHM)=V_ILIM(mV)/10
PD13
1999_DL3
PC133
.01U/50V
5VPCU
CHN217
PC135
.1U/50V
+10V
+10V
PD14
1999_DL3
PC134
.01U/50V
+10V
+15V
CHN217
PC136
2.2U/25V
Only for power
ALWAYS
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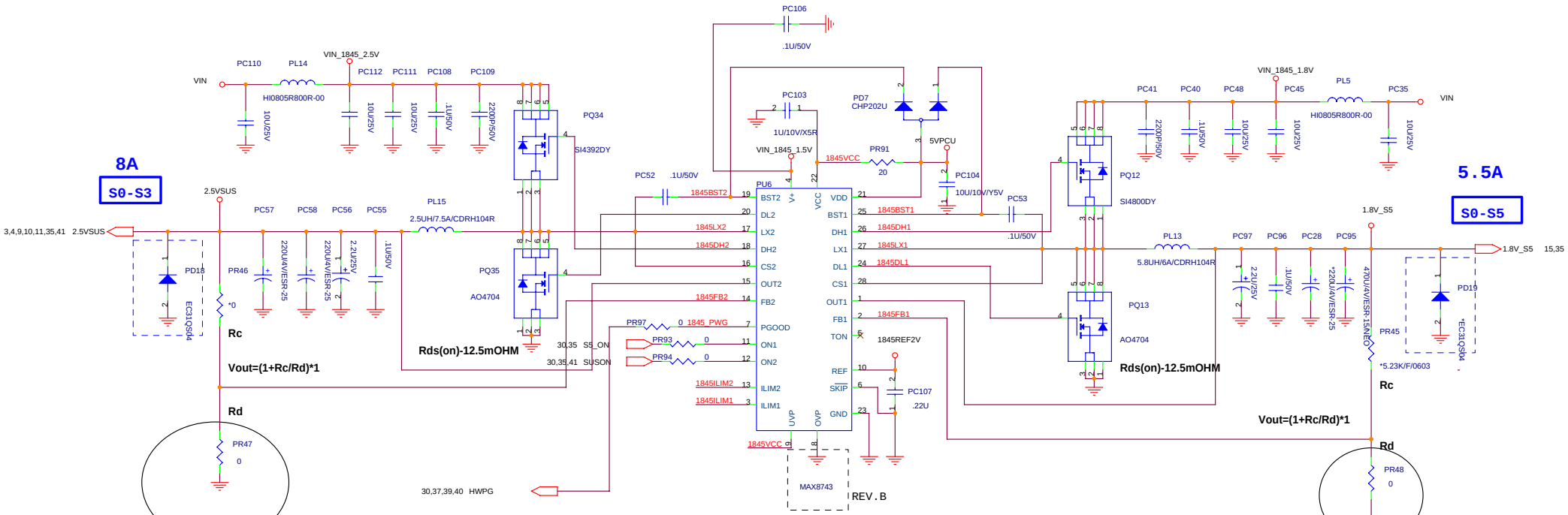

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Custom	MAX1845(2.5VSUS/1.5V_S5)	1A
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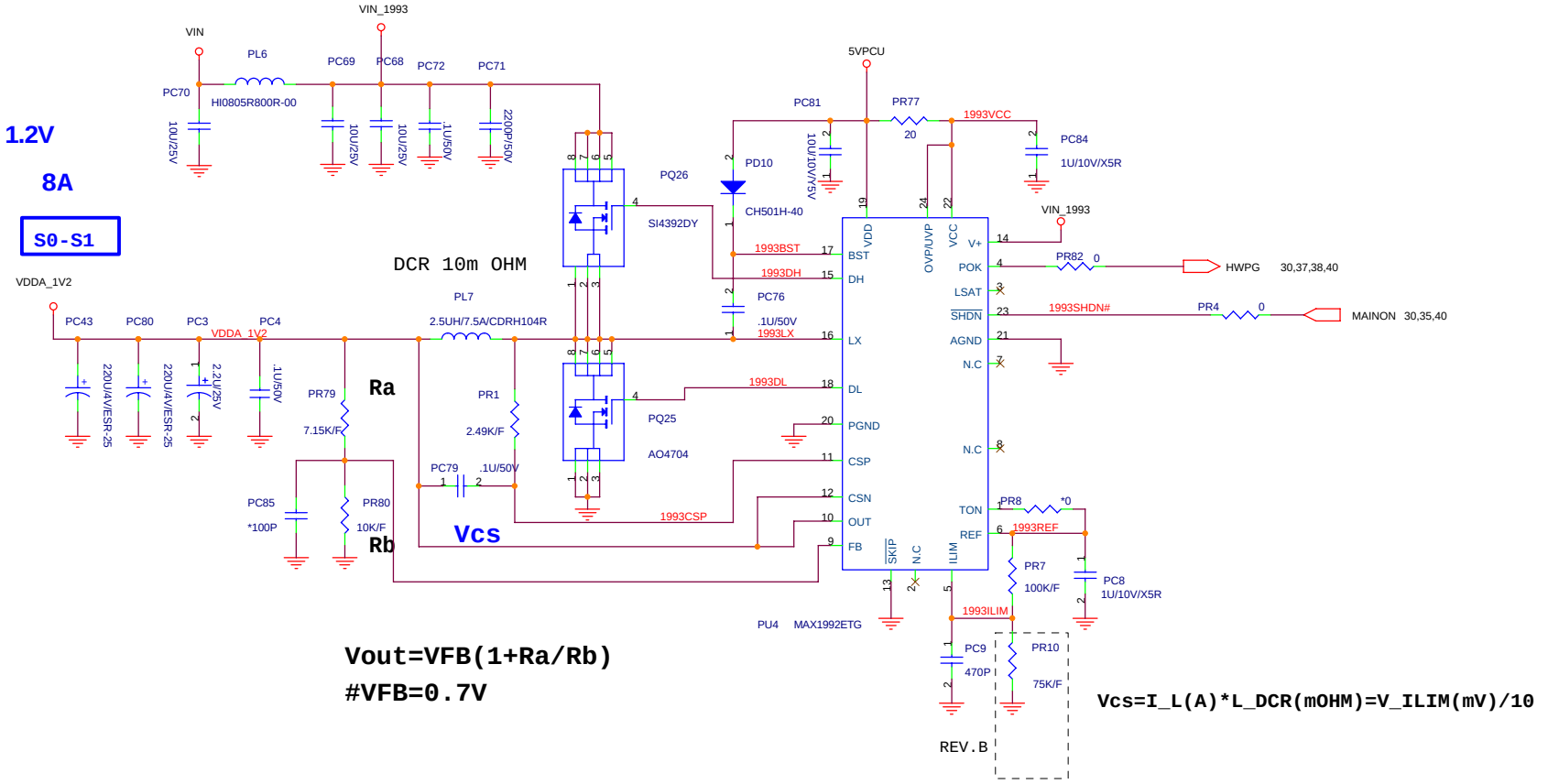

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A3	MAX1993/VCC_NB	1A
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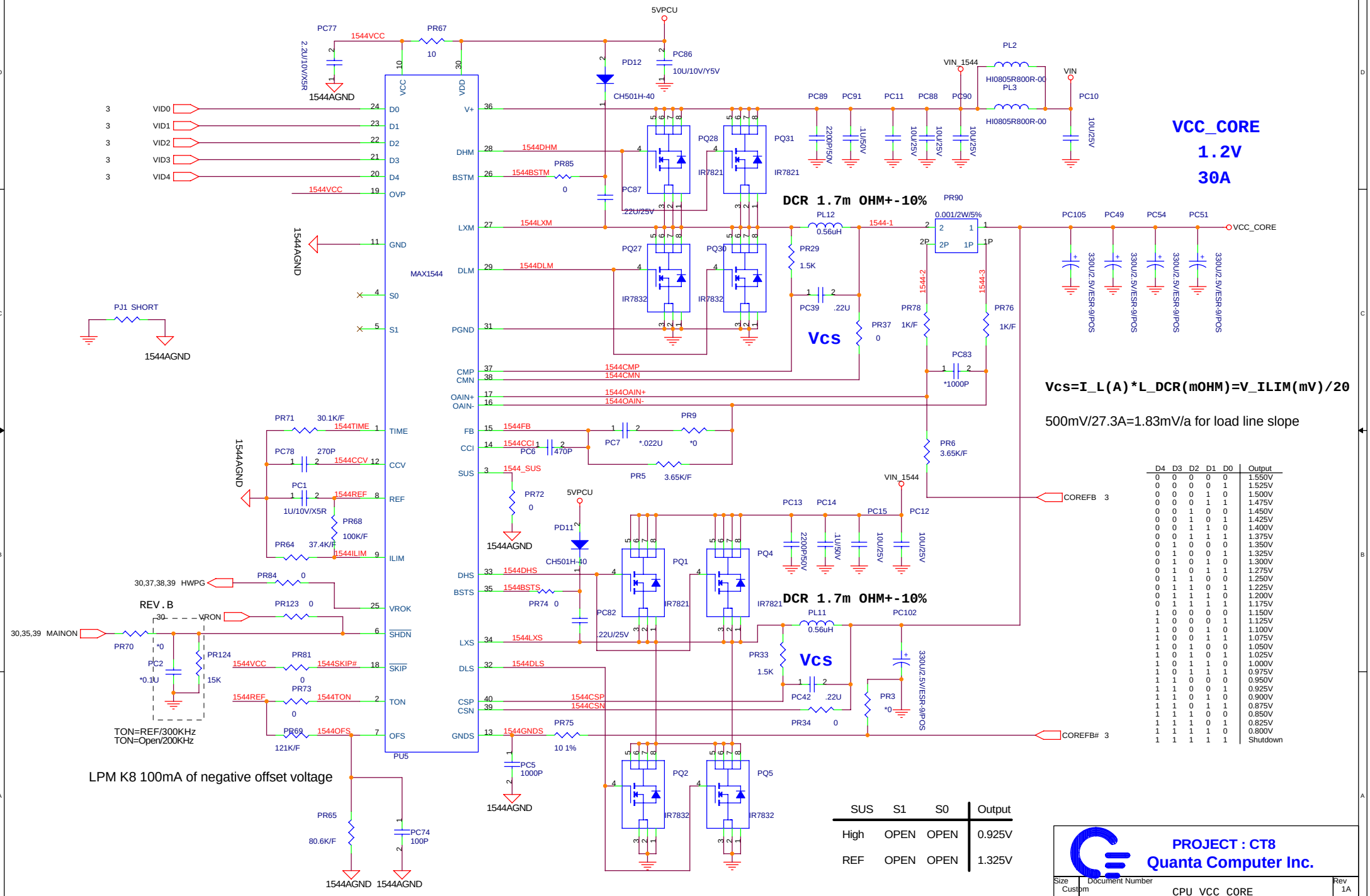

SUS	S1	S0	Output
High	OPEN	OPEN	0.925V
REF	OPEN	OPEN	1.325V

D4	D3	D2	D1	D0	Output
0	0	0	0	0	1.550V
0	0	0	0	1	1.525V
0	0	0	1	0	1.500V
0	0	0	1	1	1.475V
0	0	1	0	0	1.450V
0	0	1	0	1	1.425V
0	0	1	1	0	1.400V
0	0	1	1	1	1.375V
0	1	0	0	0	1.350V
0	1	0	0	1	1.325V
0	1	0	1	0	1.300V
0	1	0	1	1	1.275V
0	1	1	0	0	1.250V
0	1	1	0	1	1.225V
0	1	1	1	0	1.200V
0	1	1	1	1	1.175V
1	0	0	0	0	1.150V
1	0	0	0	1	1.125V
1	0	0	1	0	1.100V
1	0	0	1	1	1.075V
1	0	1	0	0	1.050V
1	0	1	0	1	1.025V
1	0	1	1	0	1.000V
1	0	1	1	1	0.975V
1	1	0	0	0	0.950V
1	1	0	0	1	0.925V
1	1	0	1	0	0.900V
1	1	0	1	1	0.875V
1	1	1	0	0	0.850V
1	1	1	0	1	0.825V
1	1	1	1	0	0.800V
1	1	1	1	1	Shutdown

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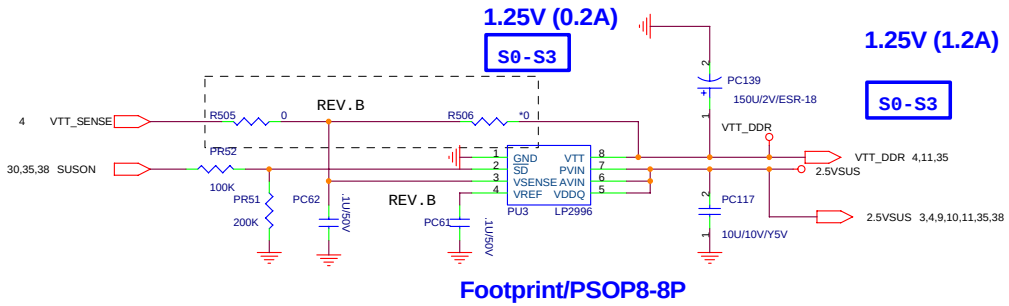

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