ZZZ1 PCB 14"DAZ@

ZZZ2 LA-7011P 14"DA@

ZZZ3 LS-7011P 14"DA@

ZZZ4 LS-7013P 14"DA@

ZZZ5 LS-7014P 14"DA@

Compal Confidential

Schematics Document

PAW10

Montevina

with Intel Cantiga + ICH9 core logic

REV:1.0A

2010-12-24

Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics,Ltd.

Title: Cover Sheet

Size: Custom | Document Number: LA7011P | Rev: 1.0

Date: Friday, December 24, 2010 | Sheet 1 of 41

Compal confidential
File Name :

For 14"	For 15"
LS-7011P 4PIN PWR/B	LS-7012P 8PIN PWR/B
LS7013P Audio/B	LS7013P Audio/B
LS7014P Touch/B	LS7014P Touch/B

Clock Generator
SLG8SP556VTR
page16

Mobile Penryn
uPGA-478 CPU
page4,5,6

H_A#(3..35)
H_D#(0..63)
FSB
667/800MHz

Intel Cantiga GMCH
GM45
uFCBGA 1329
page 7,8,9,10,11,12,13

CRT Connector page21

LVDS Connector page22

Dual Channel
DDR3-667/800(1.5V)

DDR3-SO-DIMM X2
BANK 0, 1, 2, 3 page 14,15
up to 4G

DMI *4

C-Link

Intel ICH9-M
page 17,18,19,20

AZALIA

Audio Codec
CONEXTAN
CX20671 page26

2Channel Speaker page26

Analog MIC_Int page26

Wire Less Mini card Slot 1
page23

6*PCI-E BUS

14*USB2.0

6*SATA serial

SPI ROM BIOS

LPC BUS

CMOS Camera page22

BlueTooth CONN page30

USB CONN X1(Right) page29

USB PORT X1(Left) page29

USB PORT X1(Left) page29

Audio Jack SB CONN
HP X 1+
MIC_Ext X1 page30
Card Reader RTS5139

AR8151/8152
10/100/Giga LAN
page24

RJ45 CONN page25

EC
ENE KB926 E0
page27

Int.KBD page32

SPI ROM BIOS page28

Touch Pad page32

SATA HDD CONN page28

SATA ODD CONN page32

Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.
Title: MB Block Diagram
Size: Custom | Document Number: LA7011P | Rev: 1.0
Date: Friday, December 24, 2010 | Sheet 2 of 41

DDR3 Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	BATT	KB926	SODIMM	CLK CHIP	WLAN WWAN	ICH9	Therml
EC_SMB_CK1 EC_SMB_DA1	KB926 +3VALW	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926 +3VALW	X	X	X	X	X	X	V +3VS
ICH_SMBCLK ICH_SMBDATA	ICH +3VALW	X	X	V +3VS	V +3VS	V +3VALW	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

@ FUNCTION

Structure	Description	NON-USE
45@	45 BOM	
BT@	Blue Tooth function	
CMOS@	CMOS CAMERA function	

PCIE PORT LIST

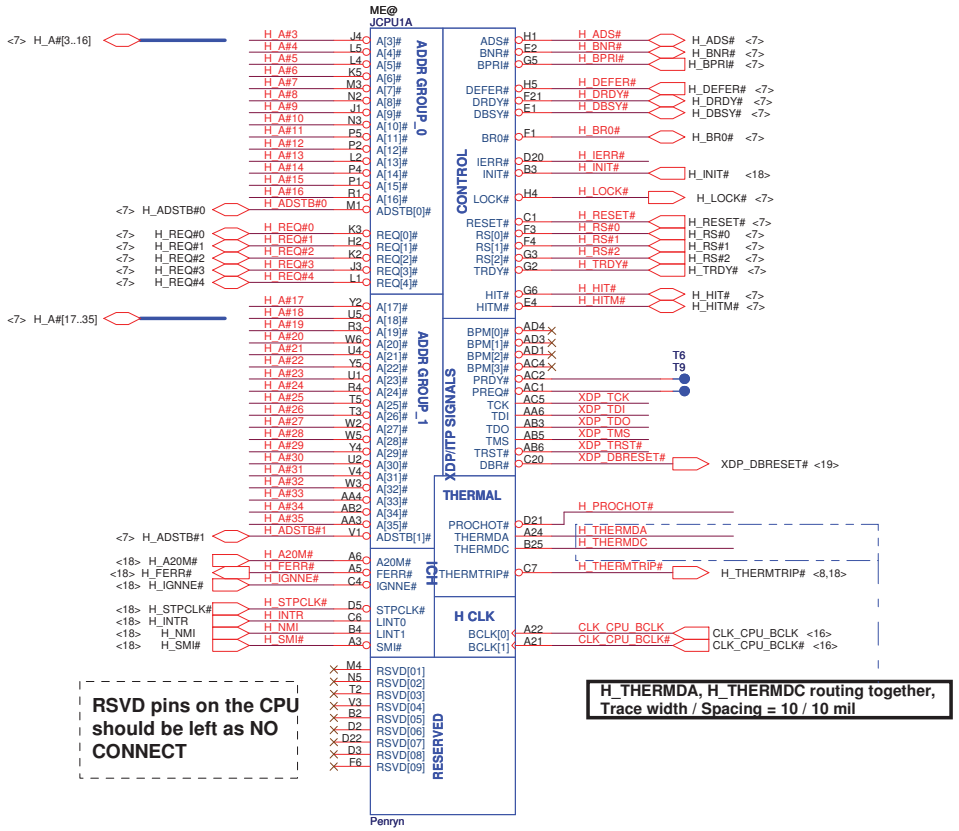
PORT	DEVICE
1	LAN
2	
3	WLAN
4	
5	
6	
7	
8	

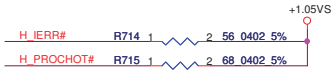
USB PORT LIST

PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	
4	CARD READER
5	WIRELESS
6	BT
7	USB PORT(ESATA)
8	
9	
10	
11	
12	
13	

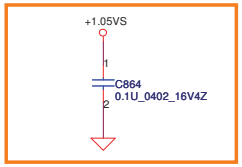
Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

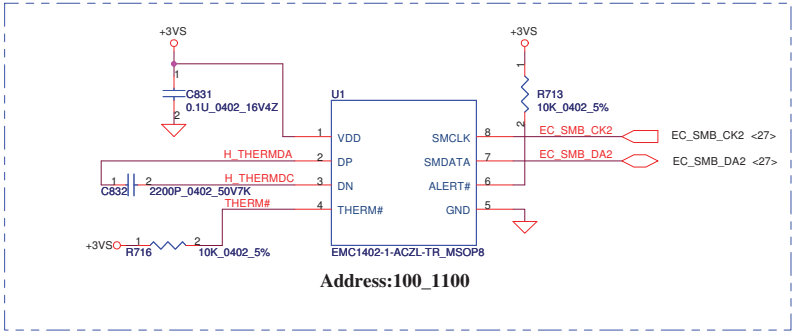
Compal Electronics, Inc.		
Title: MB Notes List		
Size: B	Document Number: LA7011P	Rev: 1.0
Date: Friday, December 24, 2010	Sheet 3 of 41	





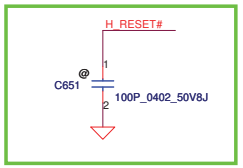
PVT ESD solution.
Please close to R715





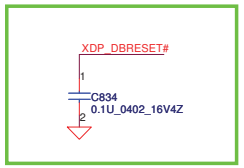
Address:100_1100

10/01 Add for reduce noise



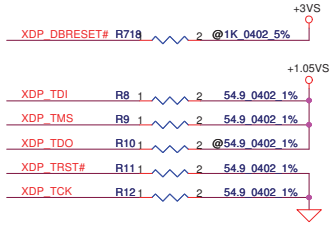
Place closely pin C1

09/16 Add C834 For ESD



Place closely pin C20

XDP Reserve for debug , Please close to CPU side



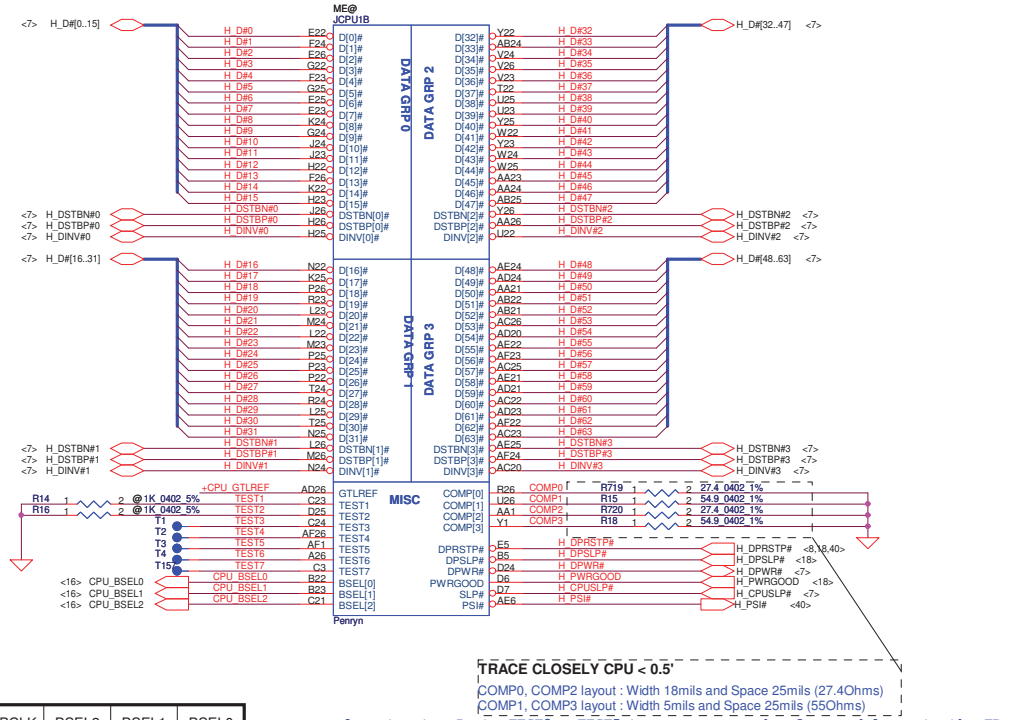
Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

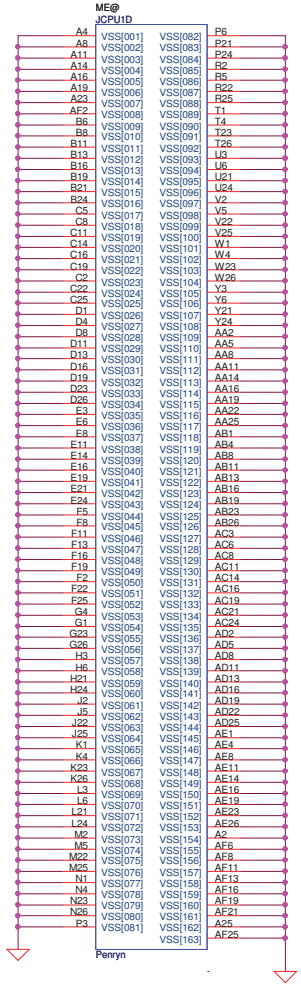
Compal Electronics, Inc.

Title: Penryn(1/3)-AGTL+THM,FAN

Size	Document Number	Rev
Custom	LA7011P	1.0

Date: Friday, December 24, 2010 Sheet 4 of 41





TRACE CLOSELY CPU < 0.5'

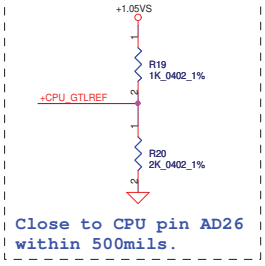
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)

COMP1, COMP3 layout : Width 5mils and Space 25mils (55Ohms)

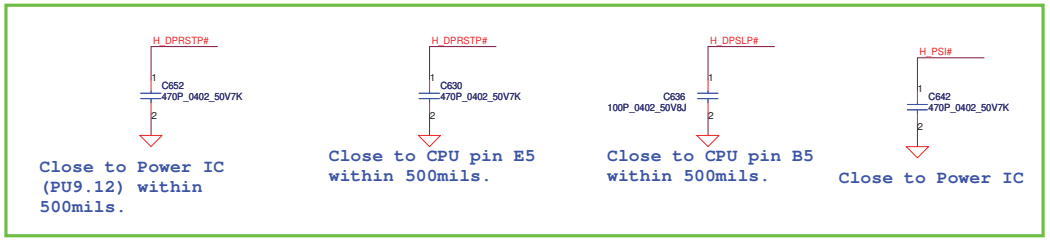
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

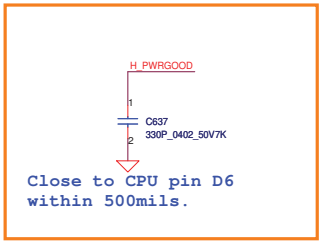
Layout note: Z0=55 ohm
0.5" max for GTLREF.



09/29 Add for power noise

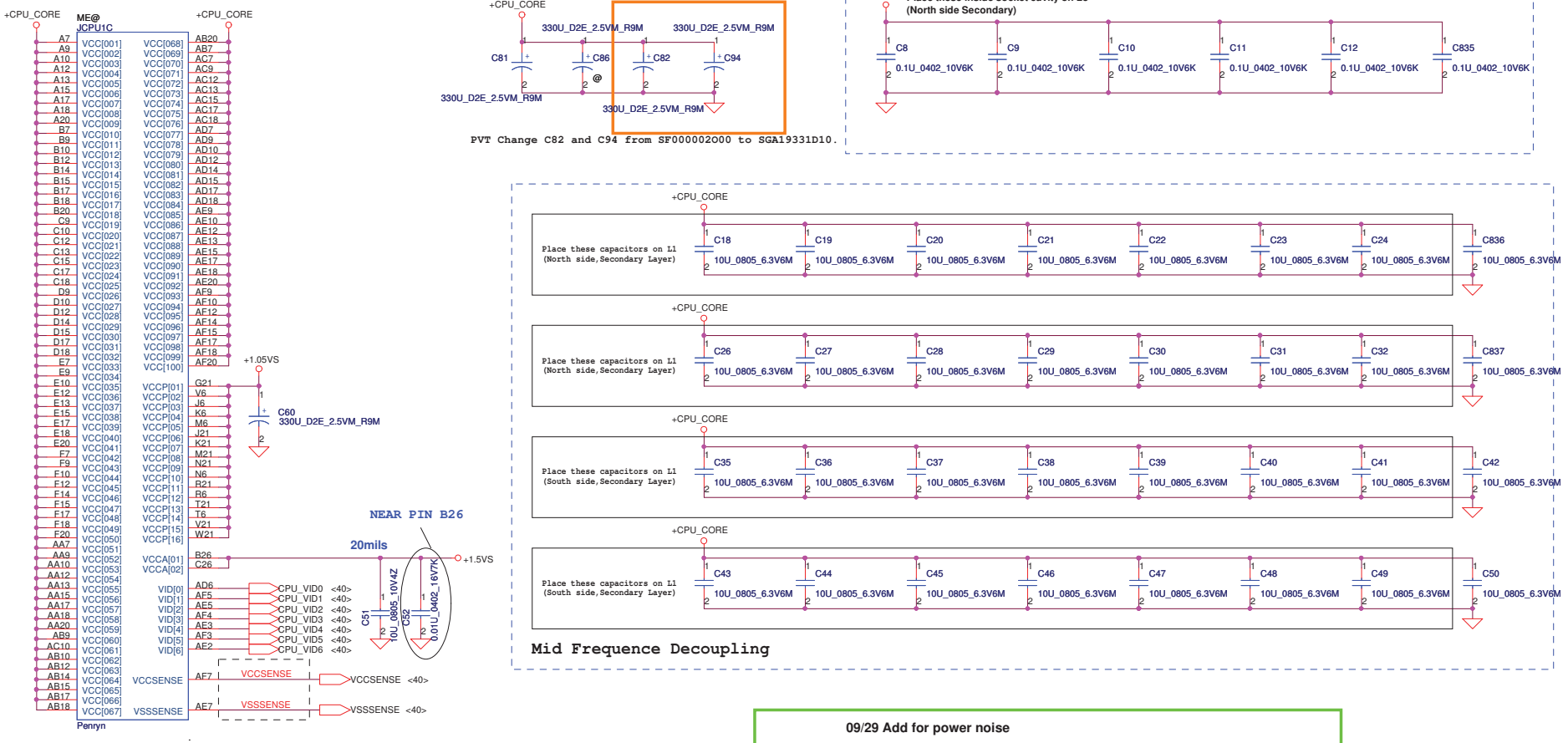


PVT for ESD solution



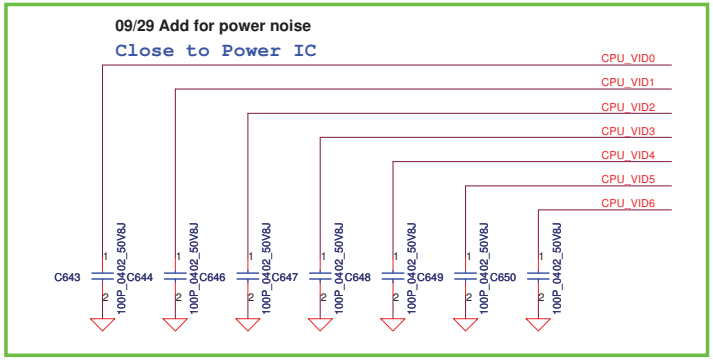
Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

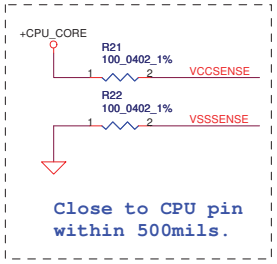
Title	Compal Electronics, Inc.		
	Penryn(2/3)-AGTL+GND		
Size: Custom	Document Number: LA7011P		Rev: 1.0
Date: Friday, December 24, 2010	Sheet 5 of 41		



PVT Change C82 and C94 from SF000002O00 to SGA19331D10.

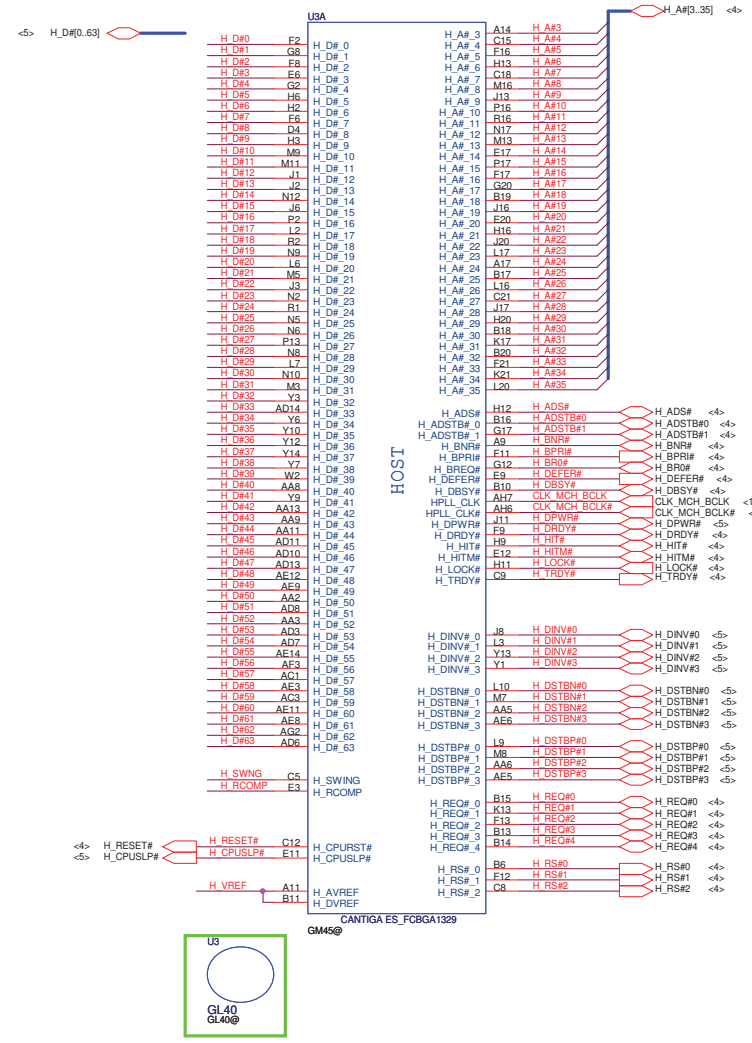
Mid Frequence Decoupling



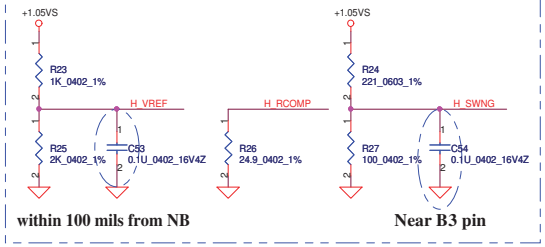


Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.			
Title	Penryn(3/3)-PWR+Bypass		
Size: Custom	Document Number: LA7011P		Rev: 1.0
Date: Friday, December 24, 2010	Sheet 6 of 41		



Layout Note:
H_RCOMP / H_VREF / H_SWNG trace width and spacing is 10/20

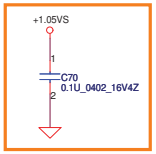


within 100 mils from NB

Near B3 pin

PVT ESD solution.

Please close to R23



Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.		
Title: Cantiga(1/7)-AGTL+		
Size: Custom	Document Number: LA7011P	Rev: 1.0
Date: Friday, December 24, 2010	Sheet 7 of 41	

Strap Pin Table

CFG[2:0]		011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	Internal pull-up	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6	Internal pull-up	0 = iTPM Host Interface is enabled can support disble by SW. 1 = iTPM Host Interface is Disabled * (Default)
CFG7	Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9	Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10	Internal pull-up	0 = PCIe Loopback Enable 1 = Disable*(Default)
CFG[13:12]	Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation *(Default)
CFG16	Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19	Internal pull-down	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select)	Internal pull-down	0 = Only PCIE or [SDVO/DP/HDMI] is operational. * (Default) 1 = PCIE/[SDVO/DP/HDMI] are operating simu.

Layout Note:
+DDR_MCH_REF trace width and spacing is 20/20. CLOSE TO PIN.AV42

For DDR3 : 1.5V power rail
For DDR2 : 1.8V power rail

For Crestline: 20ohm
For Calero: 80.6ohm
For Cantiga: 80.6ohm

SM_DRAMRST# is only for DDR3. DDR2 left it No Connect

For independent Power Rail : connect to PWM CORE VID
For Common Power Rail : left it No Connect

For AMT function

09/16 Add C838 For noise

Place closely pin U3.R32
Place closely pin PR132.2
Place closely pin AT11
Place closely pin B7
Place closely pin AR36

Strap Pin Table

SDVO_CTRLDATA (Internal pull-down)	0 = SDVO interface disabled *(Default) 1 = SDVO interface enabled
DDPC_CTRLDATA (Internal pull-down)	0 = Digital display (iHDMI/DP) interface disabled *(Default) 1 = Digital display (iHDMI/DP) interface enabled

Notice: Please check HDA power rail to select HDA controller.

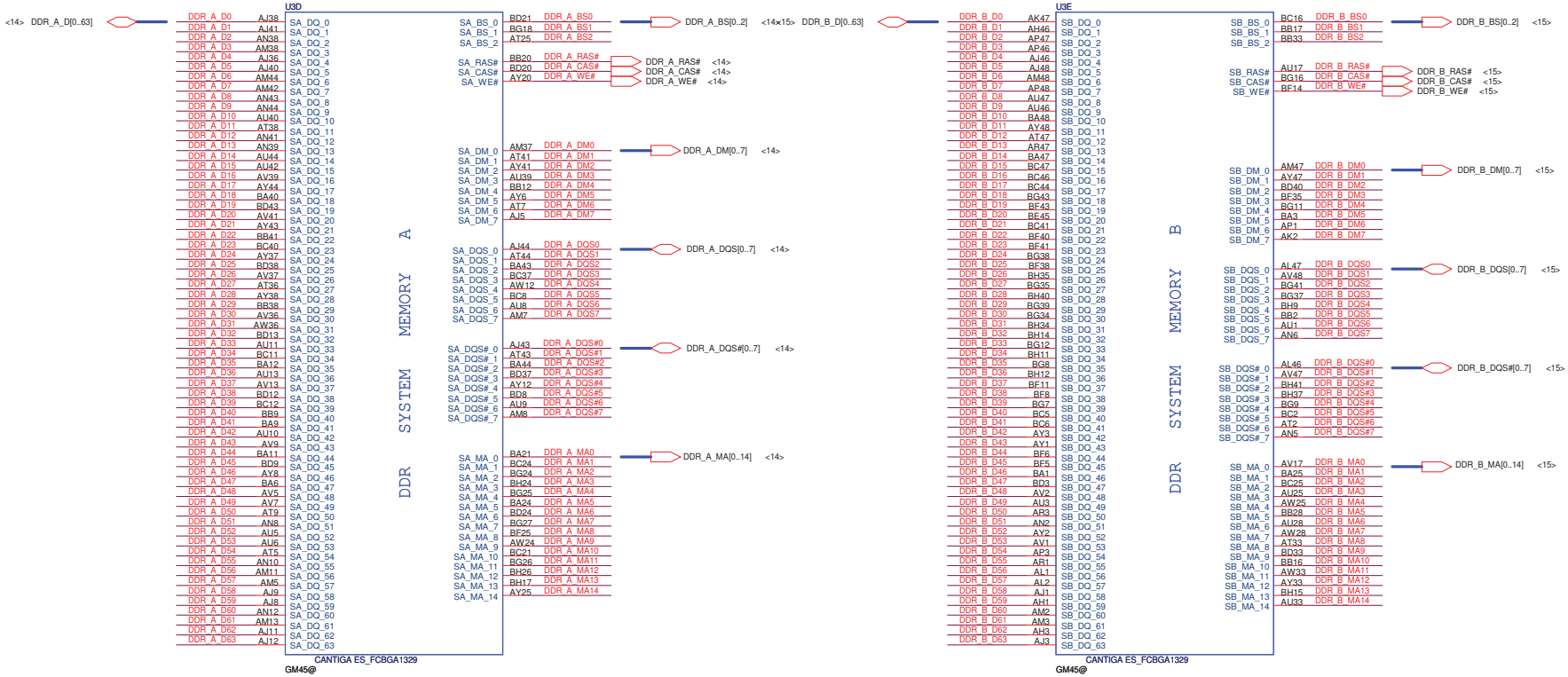
Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.

Title: Cantiga(2/7)-DMI/DDR/STRP

Size: Custom | Document Number: LA7011P | Rev: 1.0

Date: Friday, December 24, 2010 | Sheet 8 of 41



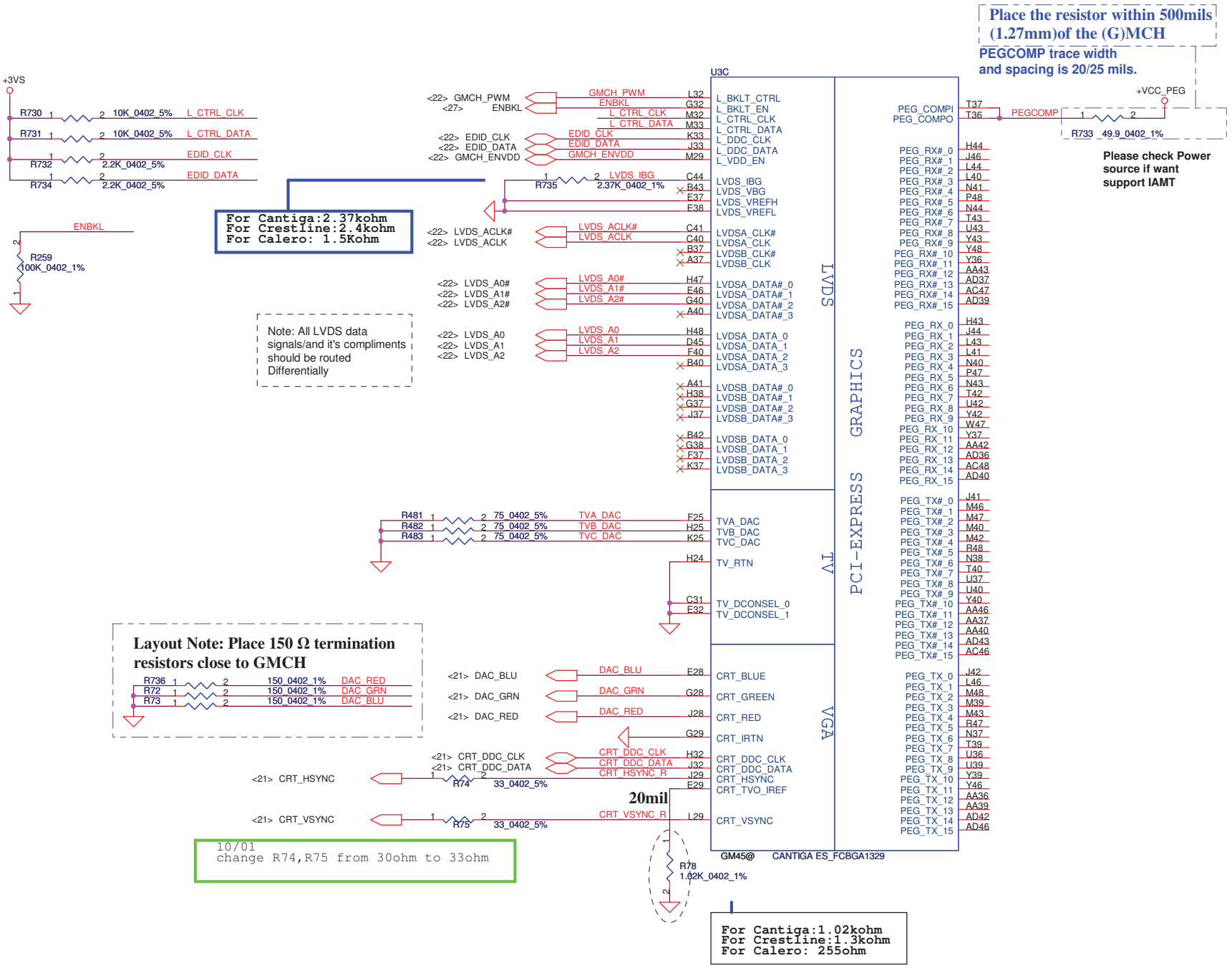
Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.

Title: **Cantiga(3/7)-DDR3 A/B CH**

Size	Document Number	Rev
Custom	LA7011P	1.0

Date: Friday, December 24, 2010 | Sheet 9 of 41



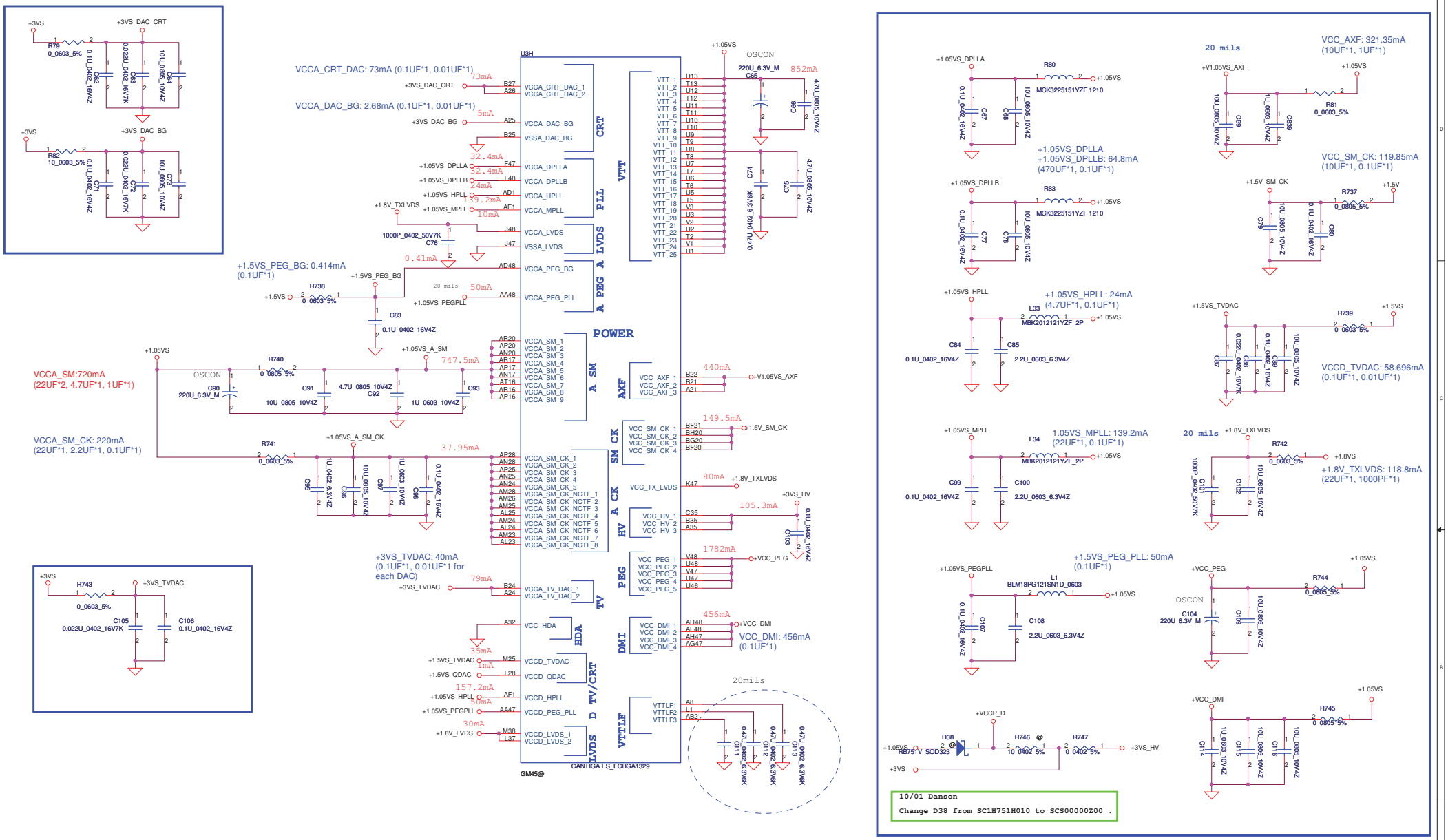
Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.

Title: Cantiga(4/7)-VGA/LVDS

Size	Document Number	Rev
Custom	LA7011P	1.0

Date: Friday, December 24, 2010 Sheet 10 of 41



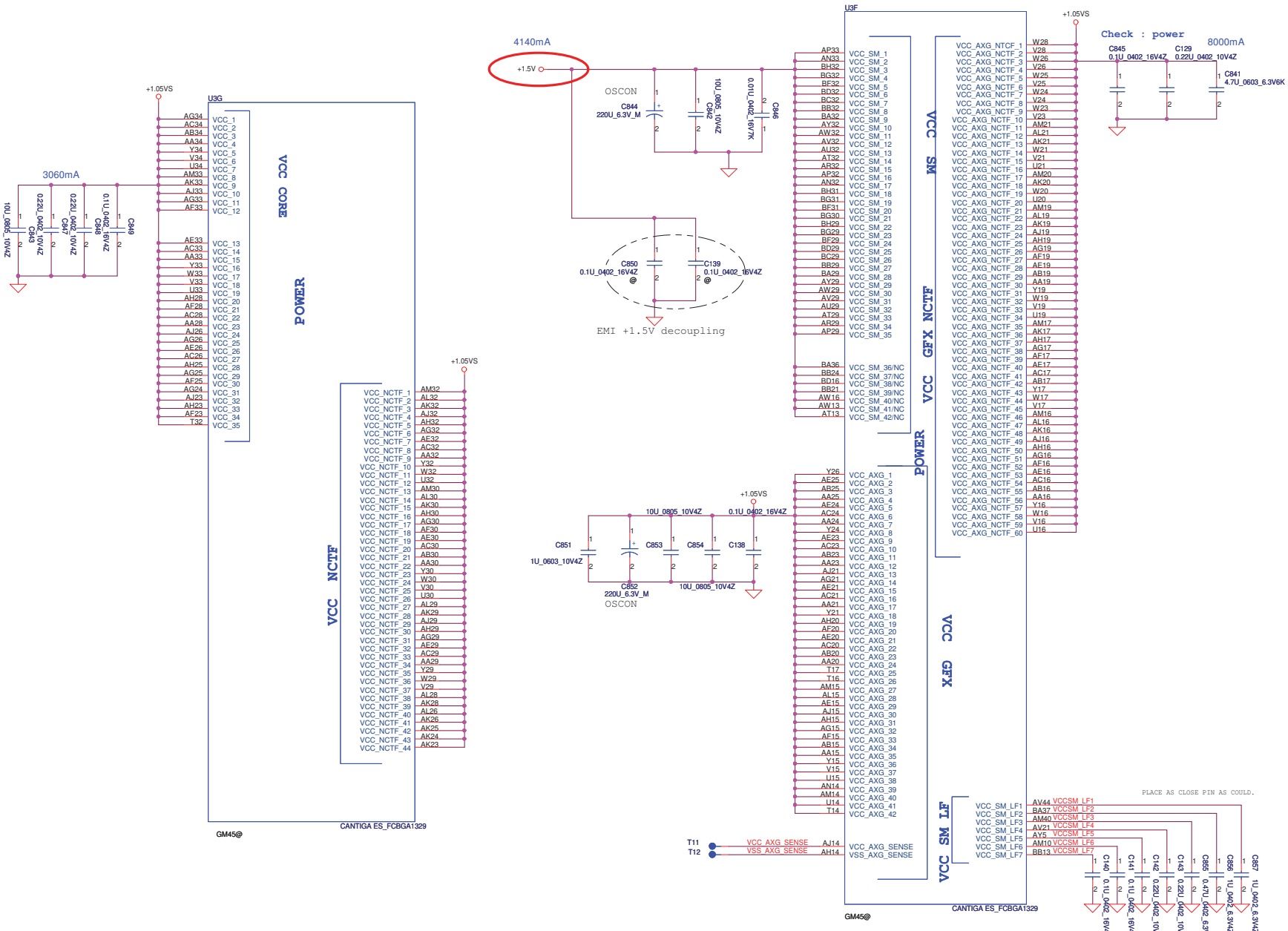
Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.

Title: *Cantiga(6/7)-VCC-1*

Size	Document Number	Rev
	LA7011P	1.0

Date: Friday, December 24, 2010 Sheet 11 of 41



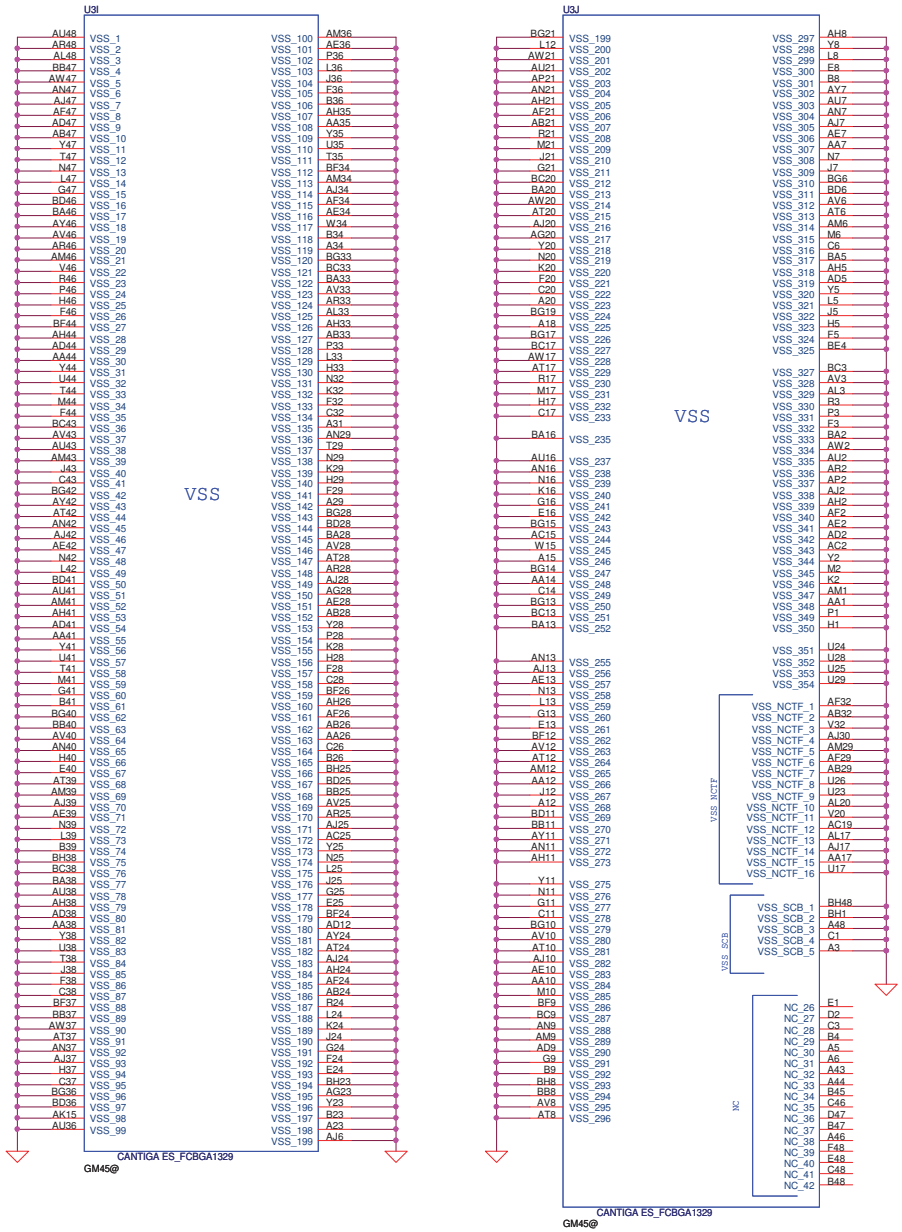
Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.

Title: *Cantiga(6/7)-VCC-1*

Size	Document Number	Rev
	LA7011P	1.0

Date: Friday, December 24, 2010 | Sheet 12 of 41



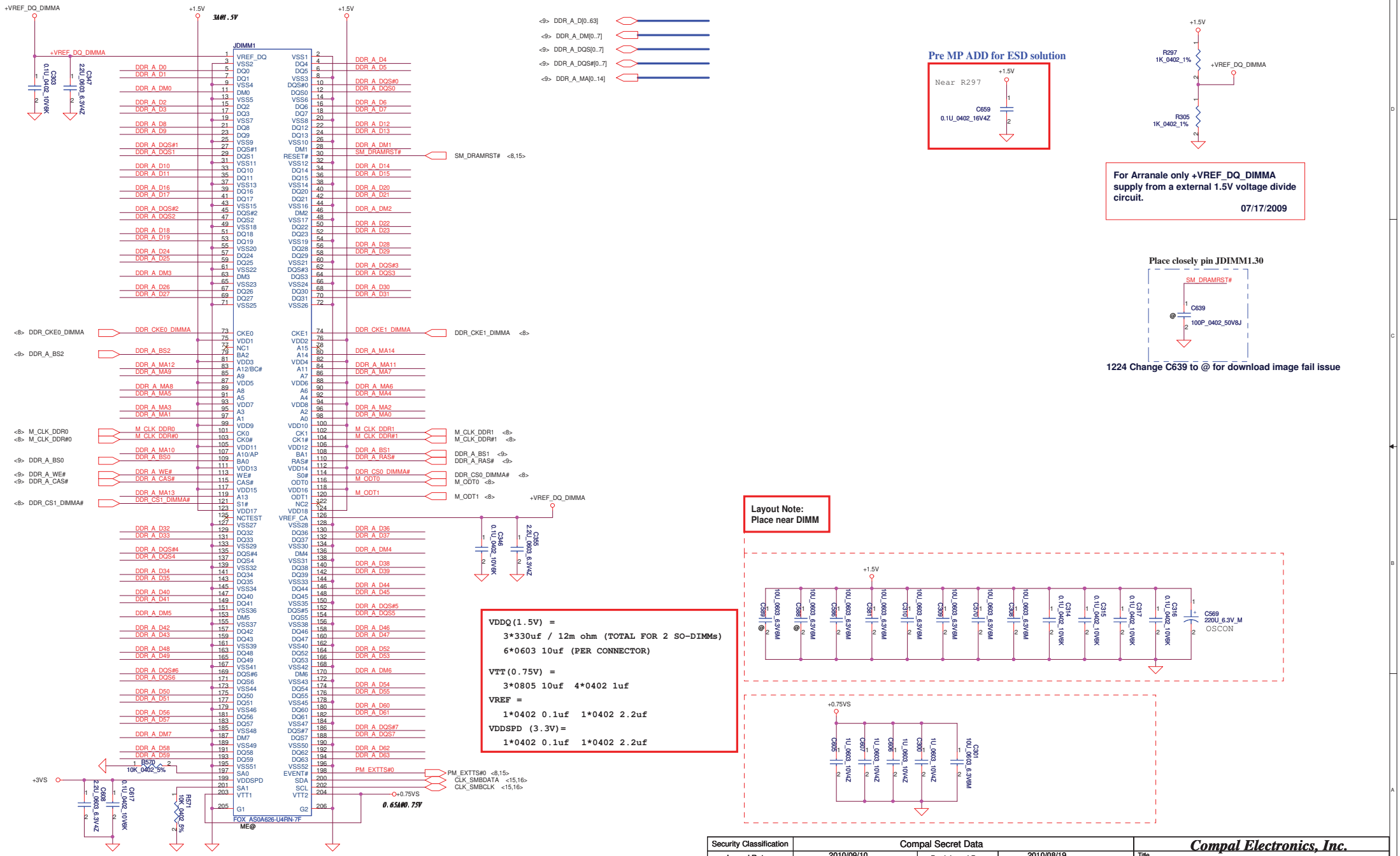
Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.

Title: *Cantiga(7/7)-GND*

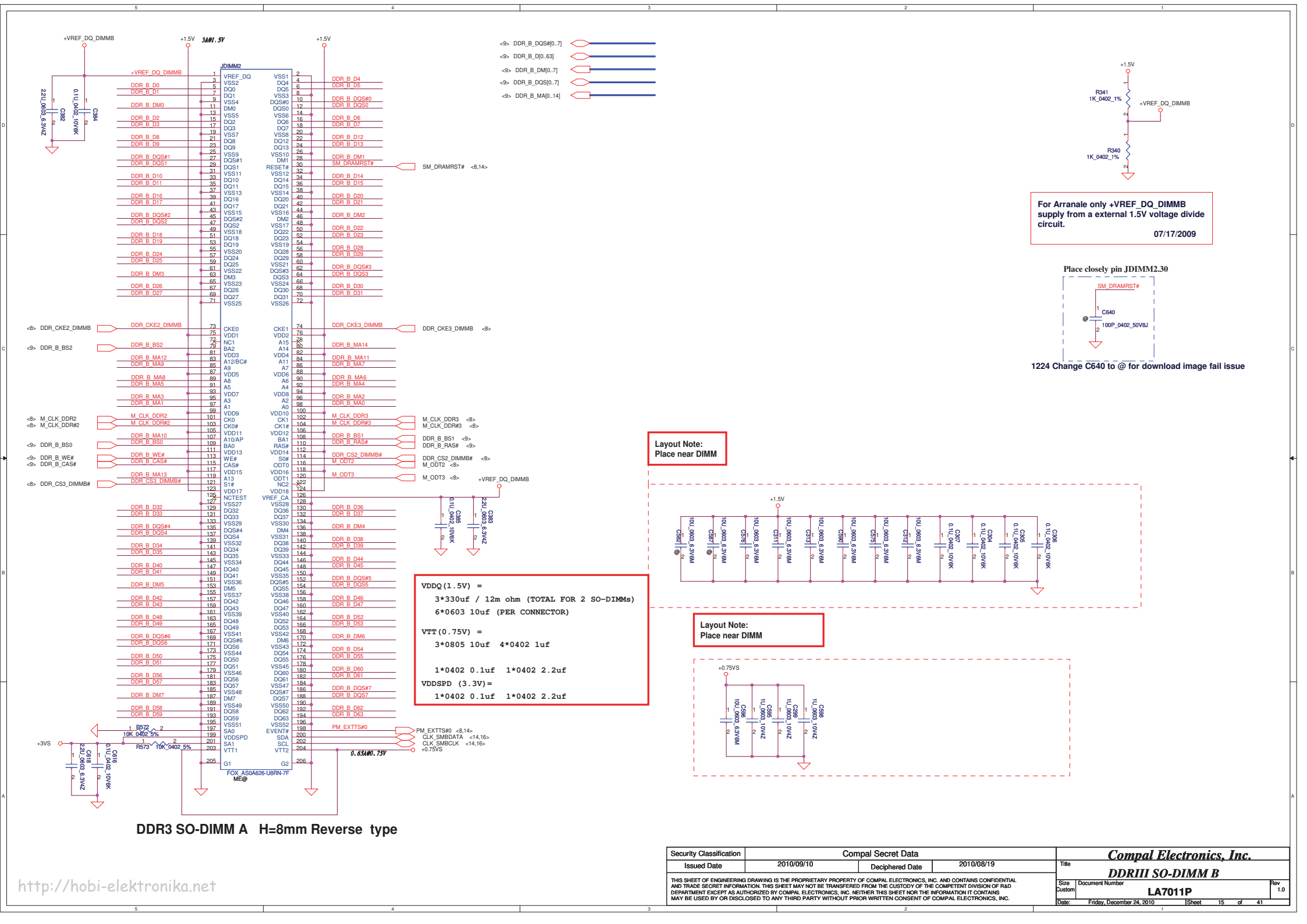
Size	Document Number	Rev
Custom	LA7011P	1.0

Date: Friday, December 24, 2010 Sheet 13 of 41



Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

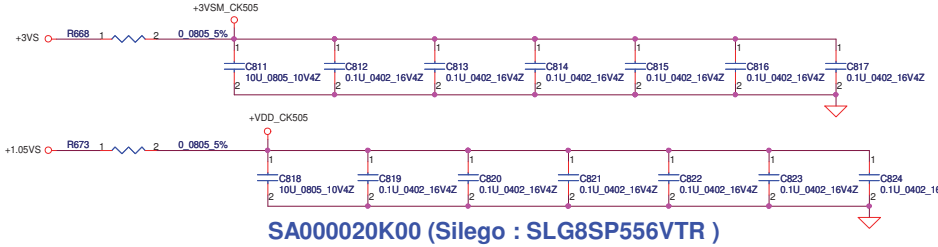
Compal Electronics, Inc.			
Title: DDRIII SO-DIMM A			
Size: Custom	Document Number: LA7011P		Rev: 1.0
Date: Friday, December 24, 2010	Sheet 14 of 41		

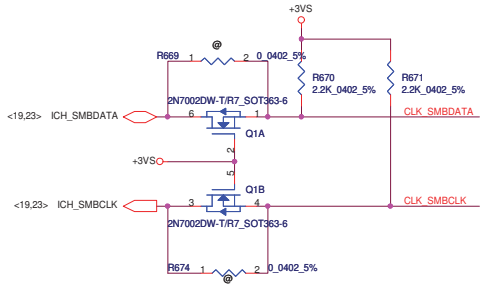


Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.			
Title	DDRIII SO-DIMM B		
Size: Custom	Document Number: LA7011P		Rev: 1.0
Date: Friday, December 24, 2010	Sheet 15 of 41		

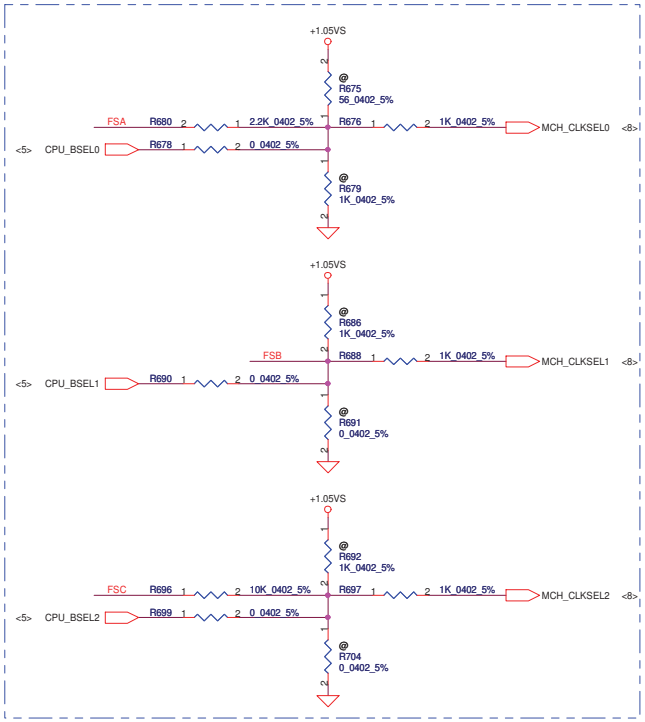
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

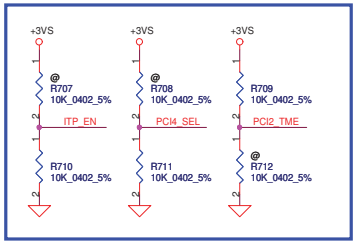




SA000020K00 (Silego : SLG8SP556VTR)

SA000020H00 (ICS : ICS9LPRS387AKLFT)



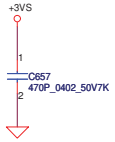


For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#

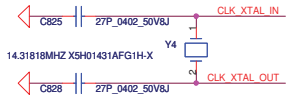
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

PVT

Close to CLK_PCI_LPC signal.



Change Y4 from SJ114P3M720 to SJ100002600.



Routing the trace at least 10mil

CPU

NB

NB(96MHz)

NB_SSC(100MHz)

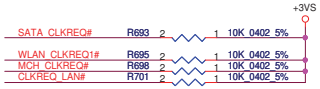
MCH_PEGPLL

WLAN

LAN

ICH-DMIPCIE

ICH-SATA



SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	
SRC4	
SRC6	
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

REQ PORT LIST

PORT	DEVICE
REQ_3#	
REQ_4#	
REQ_6#	
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

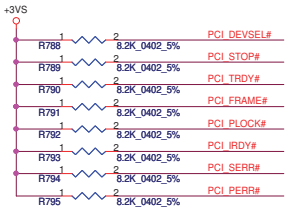
Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

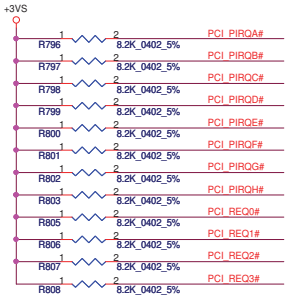
Compal Electronics, Inc.

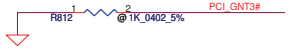
Title: **Clock Generator CK505**

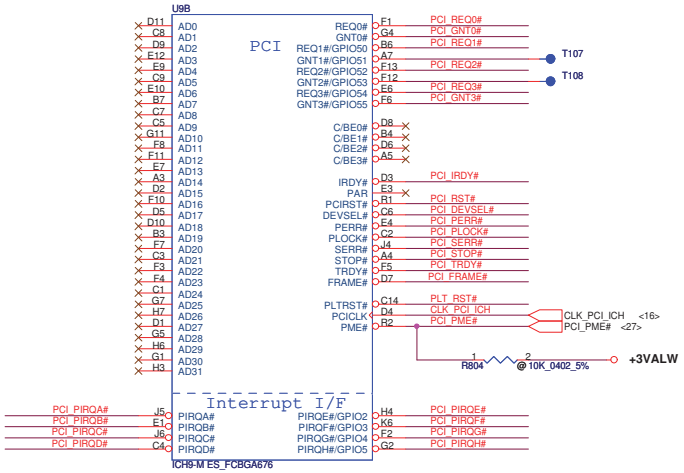
Size: Custom | Document Number: **LA7011P** | Rev: 1.0

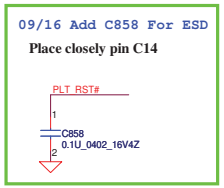
Date: Friday, December 24, 2010 | Sheet 16 of 41

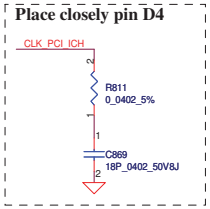


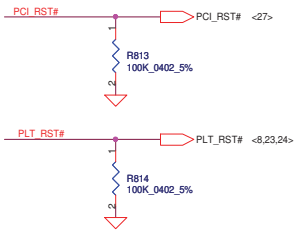










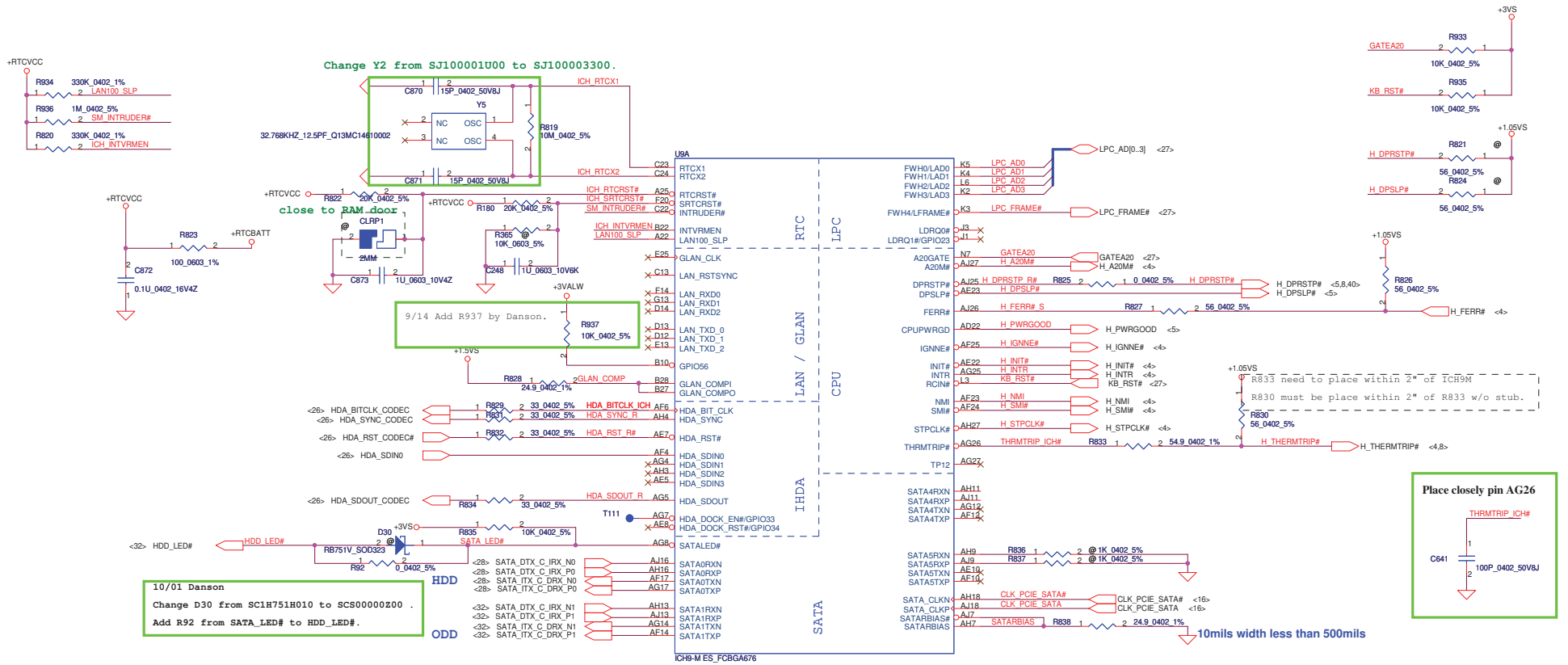


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

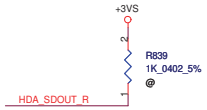
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.			
Title: ICH9M(1/4)-PCI			
Size: Custom	Document Number: LA7011P		Rev: 1.0
Date: Friday, December 24, 2010	Sheet 17 of 41		



Need check



XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

Flash Descriptor Security Override Strap	
GPIO33	Low= Descriptor Security override High= Default* (Internal pull-up)

SATA PORT LIST

PORT	DEVICE
0	HDD
1	ODD
4	
5	

Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.

Title: ICH9M(2/4)-LAN,ATA,LPC,RTC

Size: Custom | Document Number: LA7011P | Rev: 1.0

Date: Friday, December 24, 2010 | Sheet 18 of 41

09/10 Add for Project ID

Place closely pin B2

Place closely pin AC1

Place closely pin G19

09/16 Add C833 For ESD

Place closely pin D21

11/5 Add C860 For Noise

10/01

Change D31 from SC1H751H010 to SCS00000Z00 .

Change Lan from Port6 to Port 1 for power consumption.

RSMRST circuit

Change Q8 from SB000009S80 to SB000006780

PCIE PORT LIST

PORT	DEVICE
1	LAN
2	
3	WLAN
4	
5	
6	

USB PORT LIST

PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	
4	CARD READER
5	WIRELESS
6	BT
7	LEFT SIDE
8	
9	
10	
11	

SPI Flash (16Mb*1)

FOR SB 16M SPI ROM

Change U33 footprint from N1E90_66179-100000_8P to MX25L1606EM2I-12G_SO8 0920

Change Value from MX25L8005M2C-15G SOP 8P to MX25L1606EM2I-12G_SO8 0920

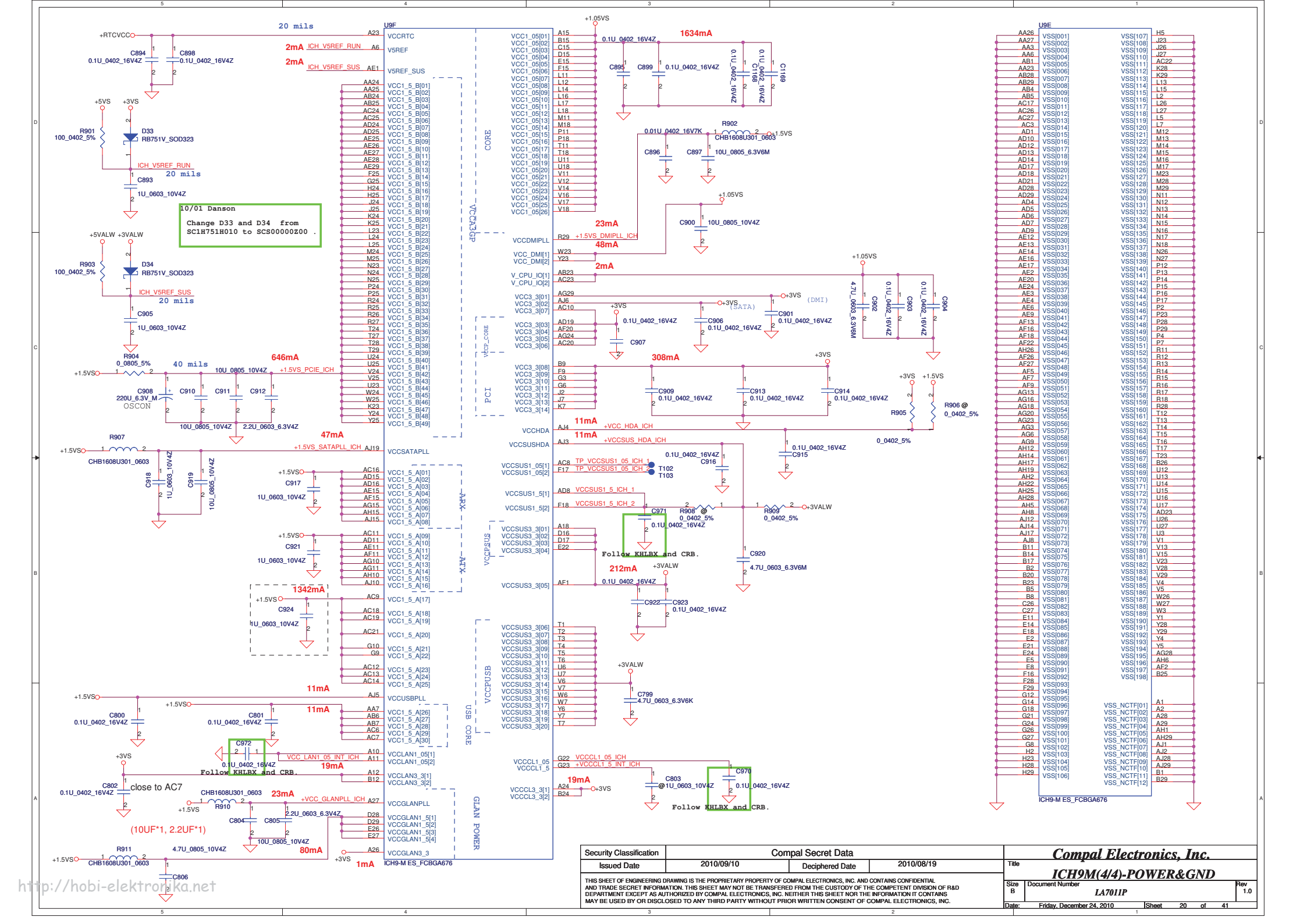
Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.

Title: ICH9M(3/4)-USB,GPIO,PCIE

Size: C | Document Number: LA7011P | Rev: 1.0

Date: Friday, December 24, 2010 | Sheet 19 of 41


U9F
U9E
20 mils
2mA ICH_V5REF_RUN
2mA ICH_V5REF_SUS
ICH_V5REF_RUN
ICH_V5REF_SUS
10/01 Danson
Change D33 and D34 from SC1H751H010 to SCS00000Z00 .
646mA
+1.5VS_PCIE_ICH
47mA
+1.5VS_SATAPLL_ICH
1342mA
11mA
19mA
23mA
80mA
1mA
1634mA
23mA
48mA
2mA
308mA
11mA
11mA
+VCC_HDA_ICH
+VCCSUS_HDA_ICH
212mA
Follow KHLBX and CRB.
close to AC7
(10UF*1, 2.2UF*1)
ICH9-M ES_FCBGA676
CORE
VCCA3GP
VCCP_CORE
PCI
ATX
VCCPSUS
USB CORE
VCCPUSB
GLAN POWER
Security Classification
Compal Secret Data
Issued Date
2010/09/10
Deciphered Date
2010/08/19
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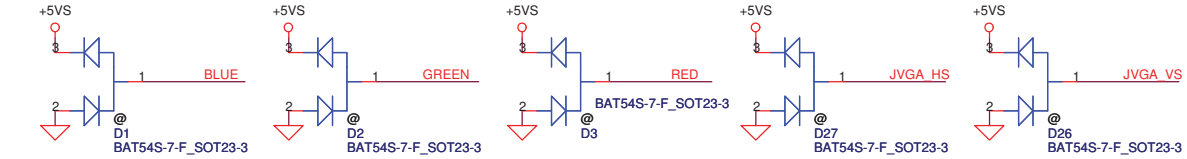
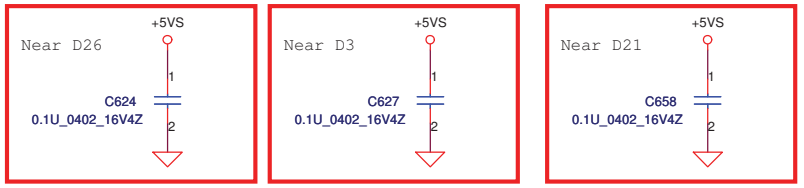
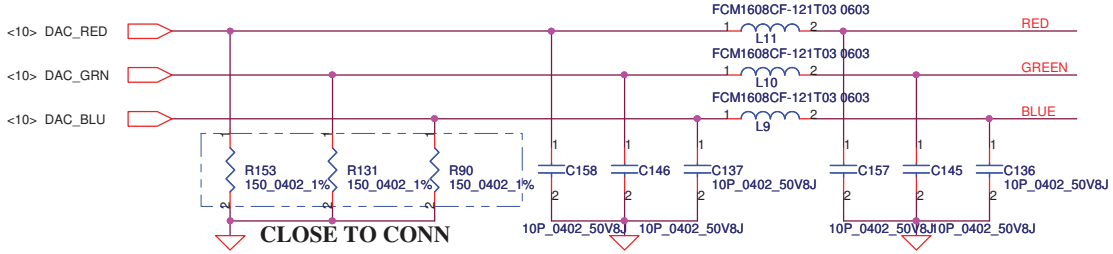
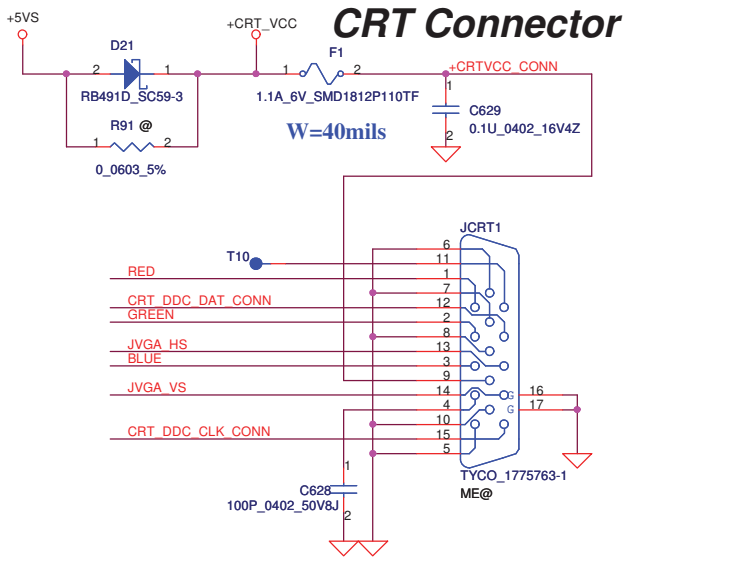
Compal Electronics, Inc.
Title
ICH9M(4/4)-POWER&GND
Size B
Document Number
LA7011P
Rev 1.0
Date: Friday, December 24, 2010
Sheet 20 of 41
http://hobi-elektronika.net

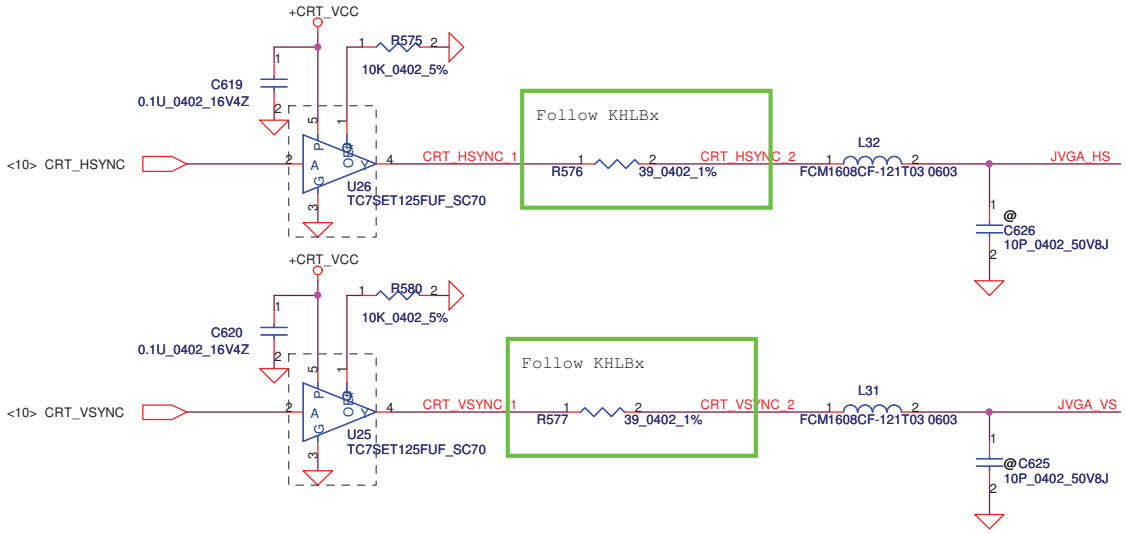


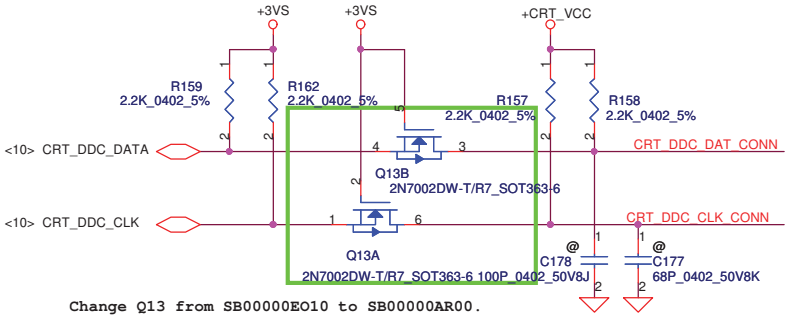
Pre MP ADD for ESD solution











Change Q13 from SB00000EO10 to SB00000AR00.

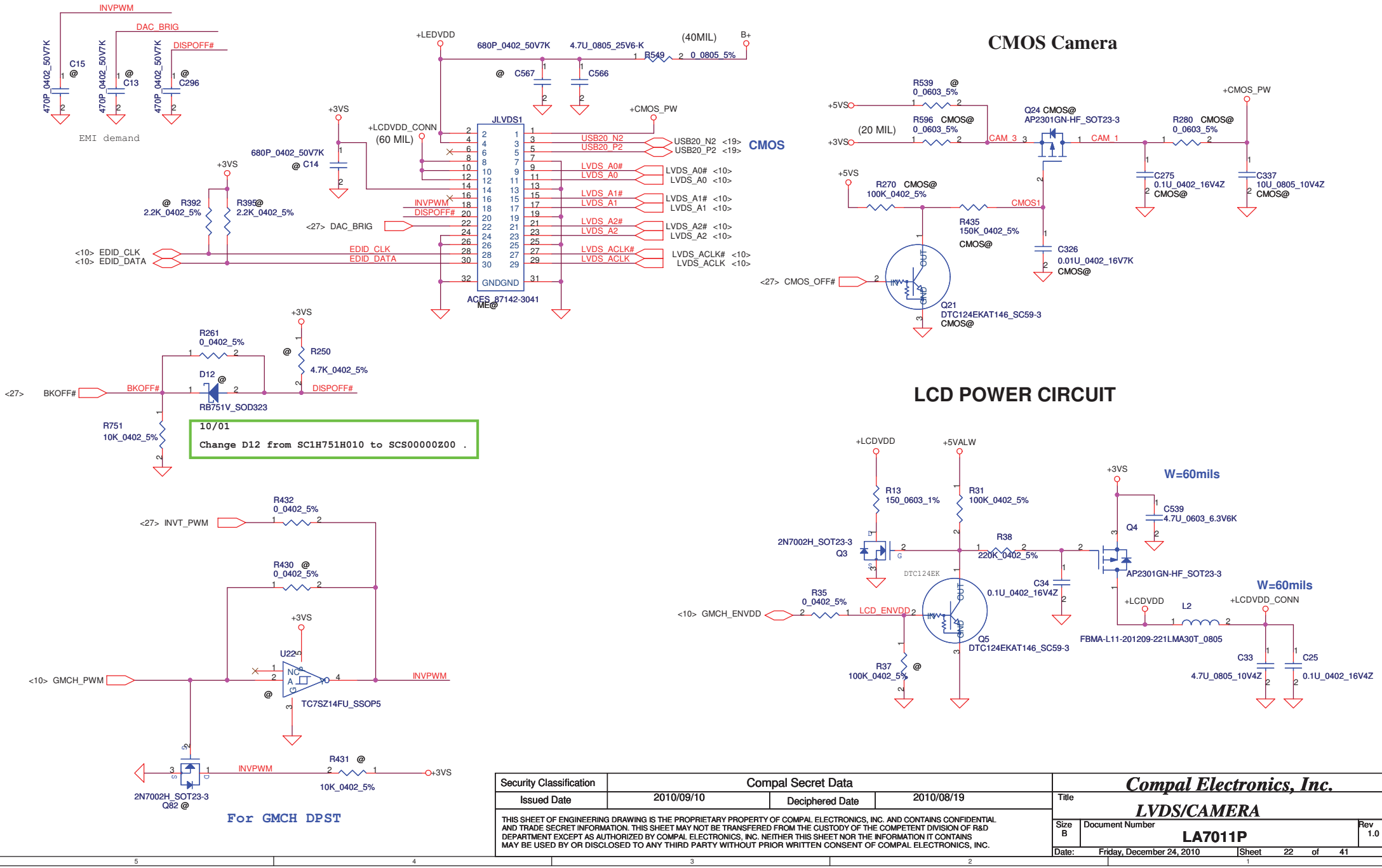
Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.

Title: **CRT Connector**

Size	Document Number	Rev
B	LA7011P	1.0

Date: Friday, December 24, 2010 Sheet 21 of 41



Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

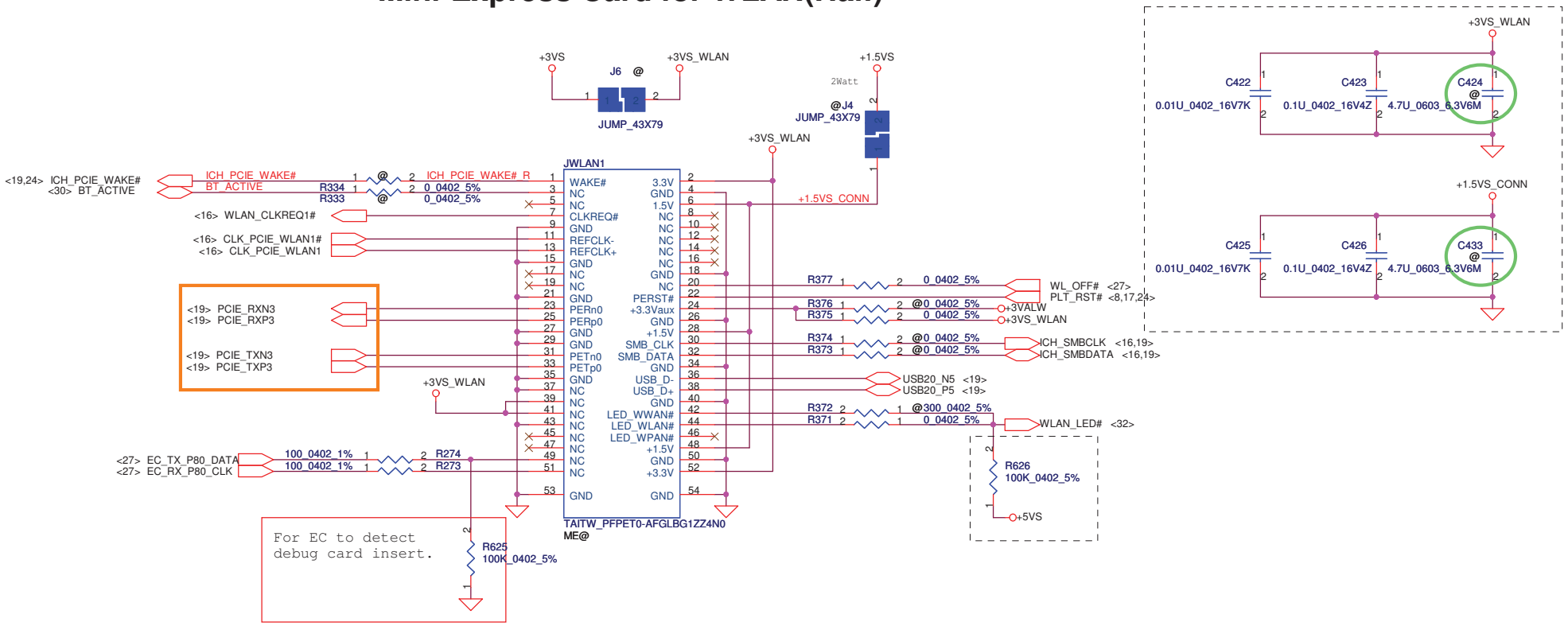
Compal Electronics, Inc.

Title: LVDS/CAMERA

Size	Document Number	Rev
B	LA7011P	1.0

Date: Friday, December 24, 2010 Sheet 22 of 41

Mini-Express Card for WLAN(Half)



Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.

Title: **Mini-Card/DEBUG-PORT**

Size	Document Number	Rev
	LA7011P	1.0

Date: Friday, December 24, 2010 Sheet 23 of 41

+3VALW

+3V_LAN

Layout Notice : Place as close chip as possible.

J8

JUMP_43X79

Atheros request can't disable LAN power

Atheros request reserve

+3V_LAN

R251 @ 4.7K_0402_5% PLT_RST#

R252 @ 4.7K_0402_5% PCIE_WAKE#_R

R253 @ 4.7K_0402_5% CLKREQ_LAN#

+1.7_VDDCT

Close together

+1.7_LX

L39 4.7UH_SIA4012-4R7M_20%

C549 GIGA@ 1000P_0402_50V7K

C548 0.1U_0402_16V4Z

C547 10U_0805_10V4Z

Note: Place Close to LAN chip
L39 DCR< 0.15 ohm
Rate current > 1A

Close to Pin40

Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
LED1	H:SWR Switch mode regulator Select * AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--

Place Close to LAN chip

MDI0+ R526 49.9_0402_1% C594 1000P_0402_50V7K

MDI0- R527 49.9_0402_1% C592 0.1U_0402_16V4Z

MDI1+ R528 49.9_0402_1% C577 1000P_0402_50V7K

MDI1- R529 49.9_0402_1% C593 0.1U_0402_16V4Z

MDI2+ R530 GIGA@ 49.9_0402_1% C580 1000P_0402_50V7K

MDI2- R531 GIGA@ 49.9_0402_1% C591 0.1U_0402_16V4Z GIGA@

MDI3+ R532 GIGA@ 49.9_0402_1% C599 1000P_0402_50V7K

MDI3- R533 GIGA@ 49.9_0402_1% C583 0.1U_0402_16V4Z GIGA@

Note 1 : 8152 no mount MDI3+, MDI3-, MDI2-, MDI2+ resister and cap

Note 2 : C594, C577, C580, C599, reserved for EMI.

R1160 0_0402_5% NONSURGE@

R1161 0_0402_5% NONSURGE@

R1162 0_0402_5% NONSURGE@

R1163 0_0402_5% NONSURGE@

U29 8152@

S IC AR8152-AL1E QFN 40P E-LAN CTRL

Place Close to Chip

U29 Atheros 8151-AL1A

<19> PCIE_IRX_PTX_N1 C553 0.1U_0402_16V7K PCIE_PRX_LANTX_N1

<19> PCIE_IRX_PTX_P1 C552 0.1U_0402_16V7K PCIE_PRX_LANTX_P1

<19> PCIE_ITX_C_PRX_N1

<19> PCIE_ITX_C_PRX_P1

<16> CLK_PCIE_LAN# R517 0_0402_5% CLK_PCIE_LAN#_C

<16> CLK_PCIE_LAN R518 0_0402_5% CLK_PCIE_LAN_C

<8,17,23> PLT_RST# PLT_RST#

<19,23> ICH_PCIE_WAKE# R519 @ 0_0402_5% PCIE_WAKE#_R

<27> LAN_WAKE# R521 0_0402_5%

8152@ C559 0.1U_0402_16V4Z LAN_XTALO LAN_XTALI

<16> CLKREQ_LAN# CLKREQ_LAN# GIGA@ R525 0_0402_5% CLKREQ_LAN#_R

TX_N TX_P RX_N RX_P REFCLK_N REFCLK_P PERST# WAKE# SMCLK SMDATA TEST_RST TESTMODE XTLO XTLI CLKREQ# AVDDL AVDDL AVDDL AVDDL AVDDL_REG GND

AR8151-AL1A_QFN40_5X5 GIGA@

LED_0 LED_1 LED_2

no overclocking PD 5.1K R515 5.1K_0402_5%

LED0,1,2 intel Pull UP

ACTIVITY LAN_LINK# CLKREQ_LAN#

R516 8152@ 0_0402_5%

ACTIVITY <25> LAN_LINK# <25>

Pre MP Add it for EMI

TRXN0 TRXP0 TRXN1 TRXP1 TRXN2 TRXP2 TRXN3 TRXP3

MDI0- SURGE@ R1160 3.9_0402_1%

MDI0+ SURGE@ R1161 3.9_0402_1%

MDI1- SURGE@ R1162 3.9_0402_1%

MDI1+ SURGE@ R1163 3.9_0402_1%

MDI0-_R MDI0+_R MDI1-_R MDI1+_R MDI2- MDI2+ MDI3- MDI3+ <25>

RBIAS LAN_RBIAS R522 2.37K_0402_1% Close Pin 10

C554 & C555 Close pin1 < 200mil
C557 & C558 Close pin < 400mil

VDD33 +3V_LAN

LX +1.7_LX

VDDCT +1.7_VDDCT C561 0.1U_0402_16V4Z

DVDDL DVDDL_REG +1.1_DVDDL

AVDDH AVDDH AVDDH_REG +2.7_AVDDH_R 0_0402_5% R520 +2.7_AVDDH GIGA@

+1.1_AVDDL

Near Pin13 Near Pin19 Near Pin31 Near Pin34 Near Pin6

Near Pin9 Near Pin22 Near Pin16 Near Pin37 Near Pin24

LAN_XTALI LAN_XTALO Y6 25MHZ_20PF_7A25000012 C578 27P_0402_50V8J C579 27P_0402_50V8J

9/27 Add it for avoid to be struck by lightning

Part Number = SC300001J00

D16 TCLAMP3304N.TCT_SLP2626P10-10 SURGE@

MDI0+ MDI0- MDI1- MDI1+

Customer Lan surge Suggesttion

Will used Semtech 3304N

Part Number = SC300001J00

D17 TCLAMP3304N.TCT_SLP2626P10-10 @

MDI2+ MDI2- MDI3- MDI3+

	Pin4	Configure R525	Configure C559		Pin23	Configure R516
AR8152	VDDCT_REG		*		CLKREQn	*
AR8151	CLKREQn	*			LED[2]	

Security Classification	Compal Secret Data	
Issued Date	2010/09/10	Deciphered Date 2010/08/19

Compal Electronics, Inc.

Title: LAN-AR8151/8152

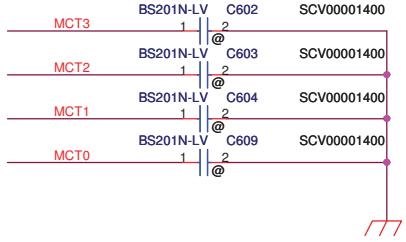
Size: Custom | Document Number: LA7011P | Rev: 1.0

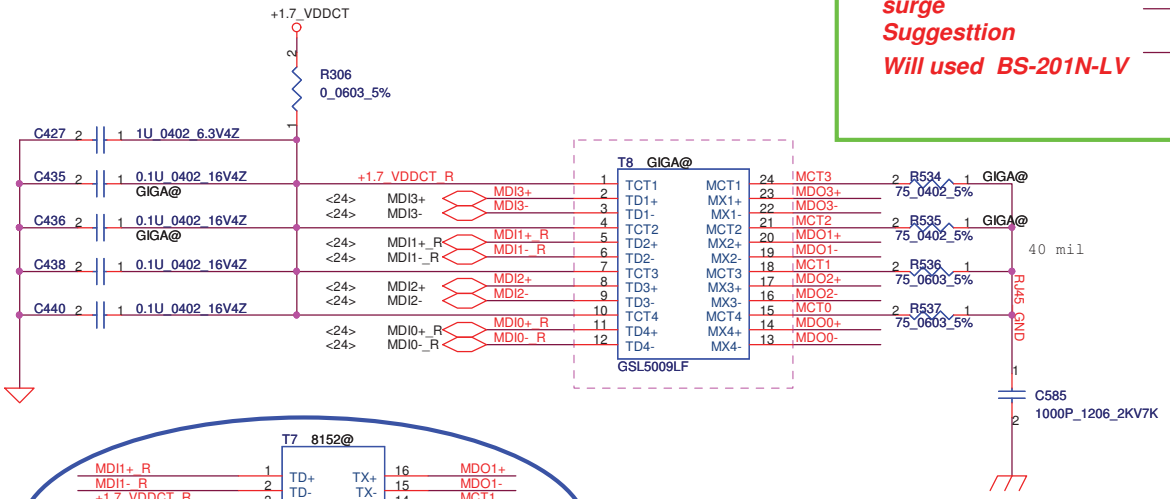
Date: Friday, December 24, 2010 | Sheet 24 of 41

9/27 Add it for avoid to be struck by lightning

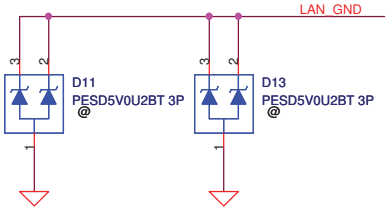
Customer Lan surge Suggesttion

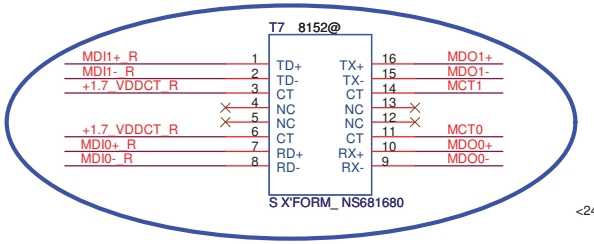
Will used BS-201N-LV





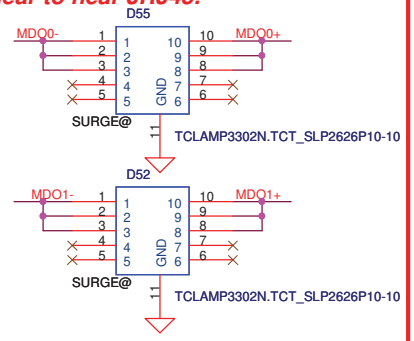
Place closely JRJ45



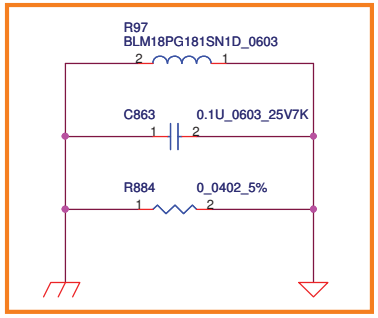


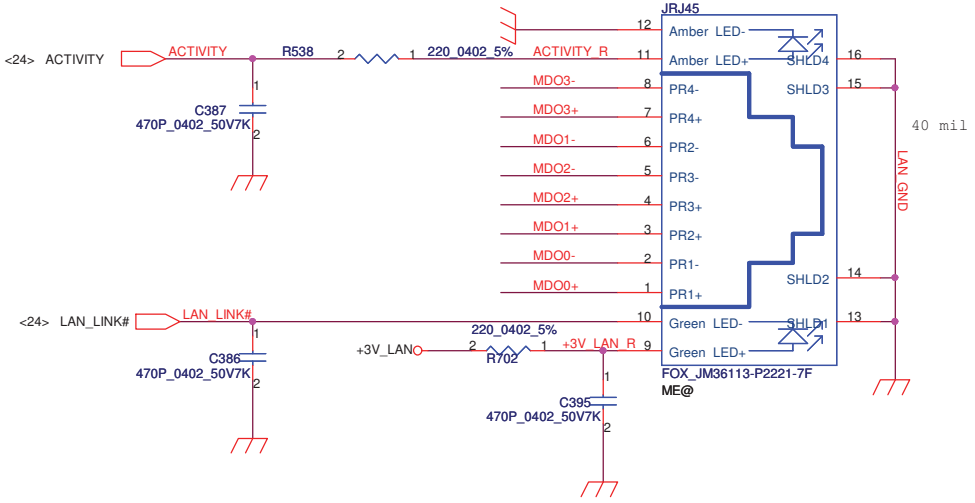
12/13 PreMP Add it for avoid to be struck by lightning

Near to near JRJ45.



PVT Add EMI solution.





Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

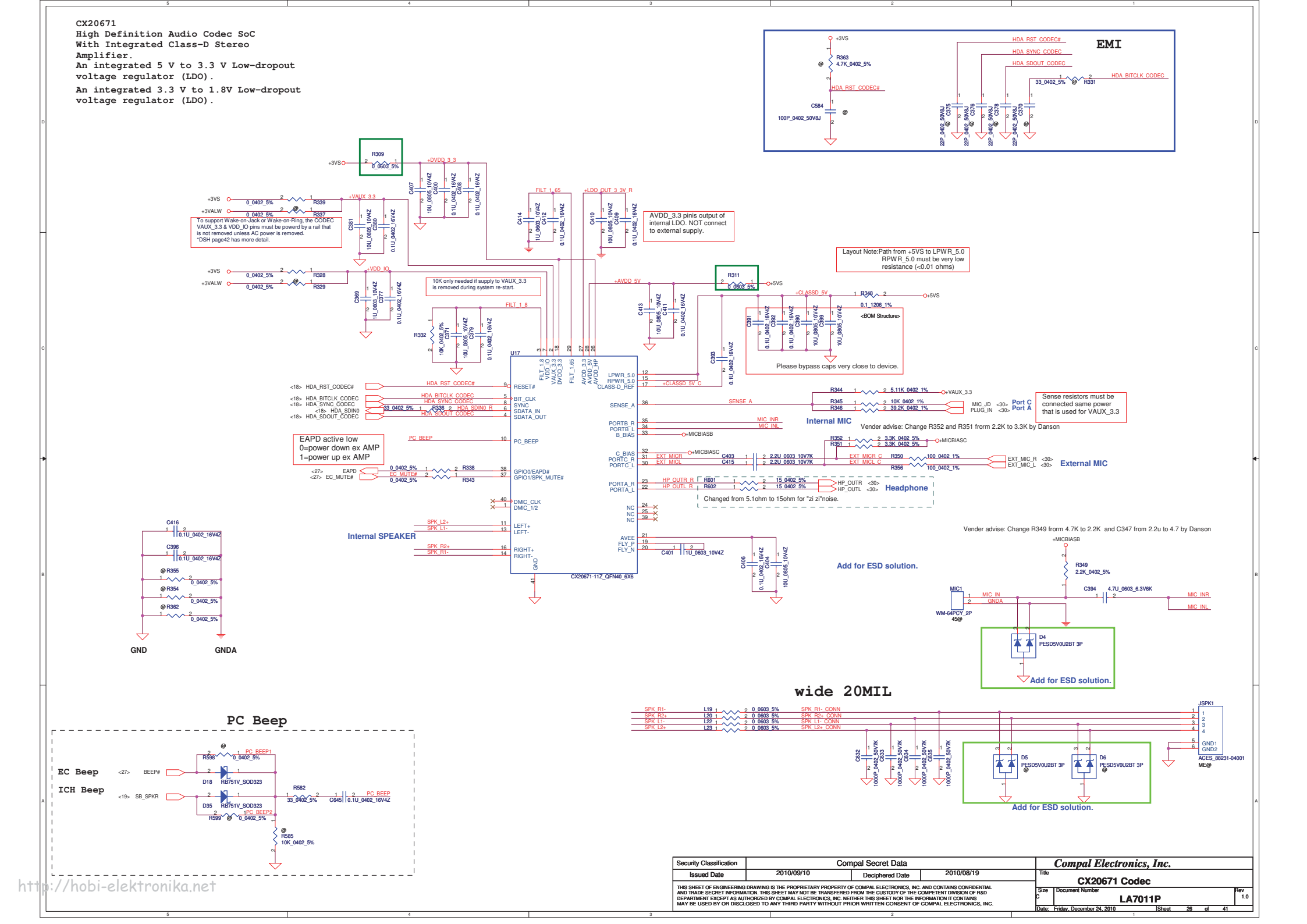
Compal Electronics, Inc.

Title: **LAN_Transformer**

Size	Document Number	Rev
B	LA7011P	1.0

Date: Friday, December 24, 2010 Sheet 25 of 41

CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



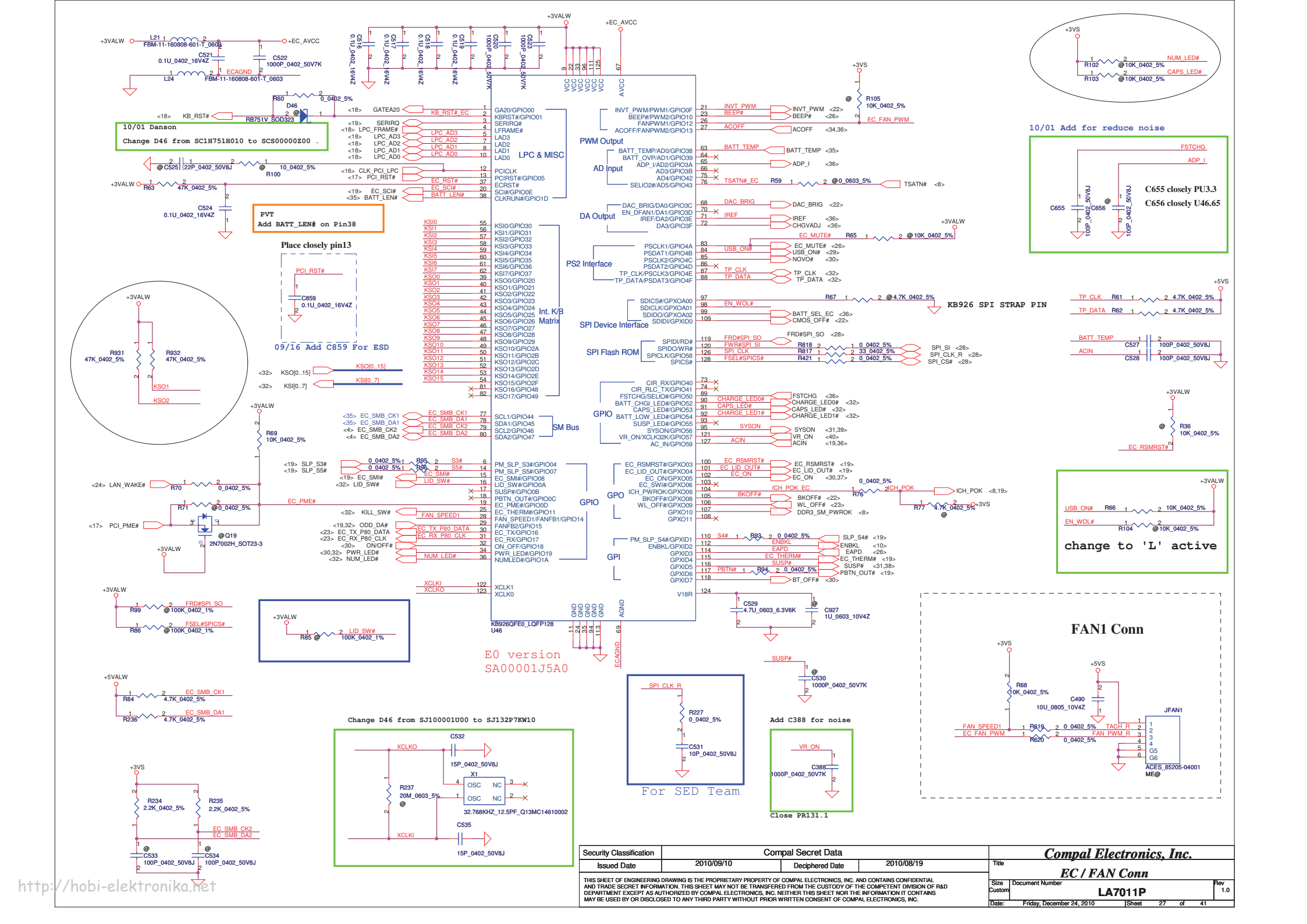
Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.

Title: CX20671 Codec

Size	Document Number	Rev
C	LA7011P	1.0

Date: Friday, December 24, 2010 Sheet 26 of 41



Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.

Title: **EC / FAN Conn**

Size	Document Number	Rev
Custom	LA7011P	1.0

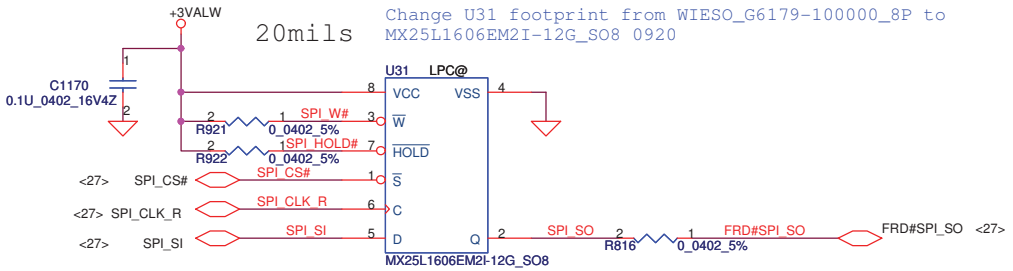
Date: Friday, December 24, 2010 | Sheet 27 of 41

SPI Flash (16Mb*1)

FOR EC 16M SPI ROM

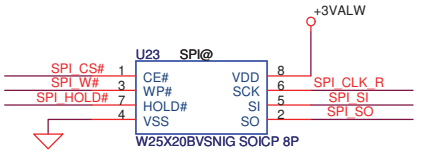
Change U31 P/N from SA00000XT00 to SA000041N00 0915

Change U31 footprint from WIESO_G6179-100000_8P to MX25L1606EM2I-12G_SO8 0920



FOR EC 256K SPI ROM (NONShare ROM)

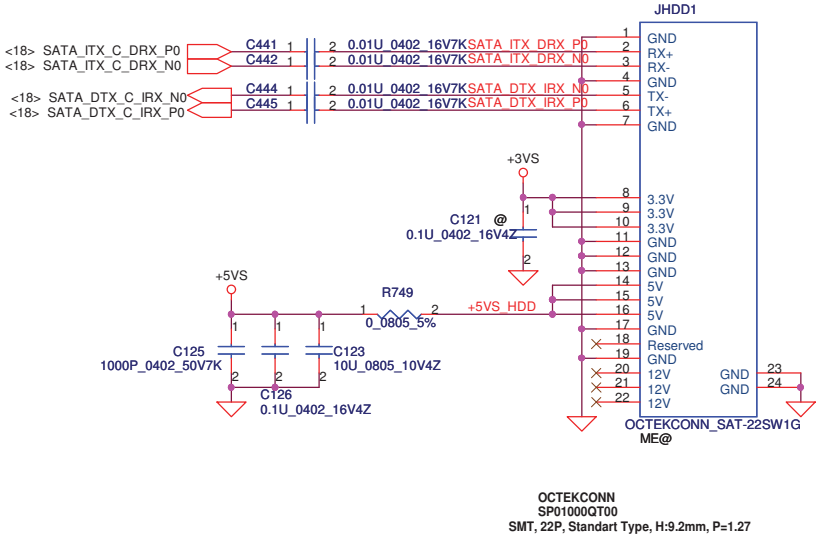
2010/09/24 Add U23 for NONShare SPI ROM.



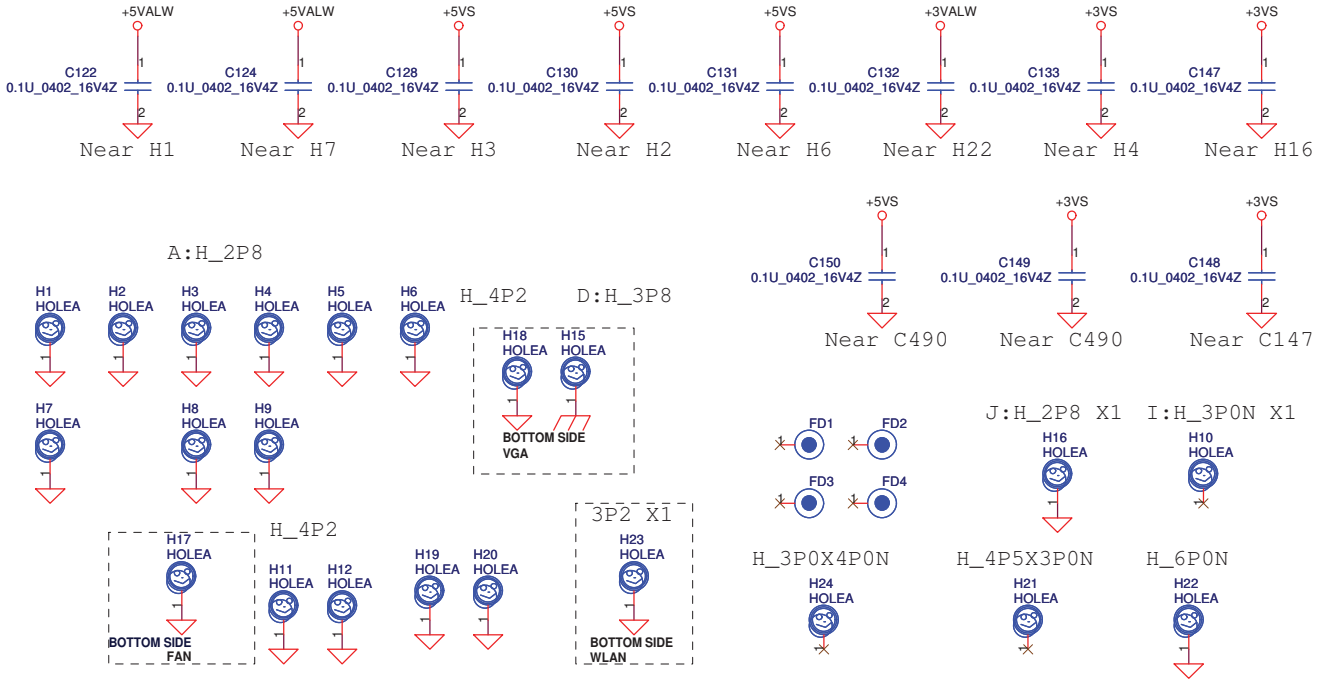
SA00003GM10

256kB(NAU00 2nd)

SATA HDD Conn.



OCTEKCONN
SP01000QT00
SMT, 22P, Standart Type, H:9.2mm, P=1.27



Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

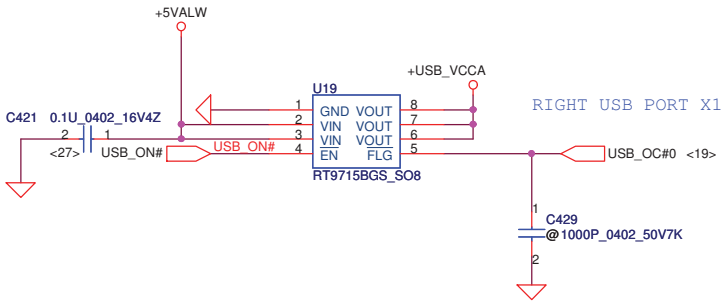
Compal Electronics, Inc.

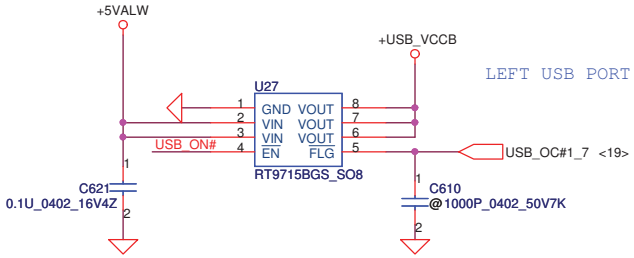
Title: HDD / SPI ROM / Hold

Size	Document Number	Rev
B	LA7011P	1.0

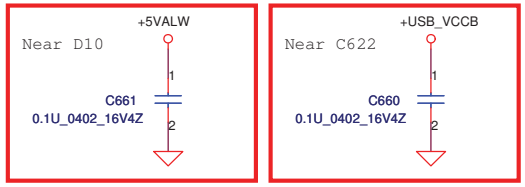
Date: Friday, December 24, 2010 Sheet 28 of 41

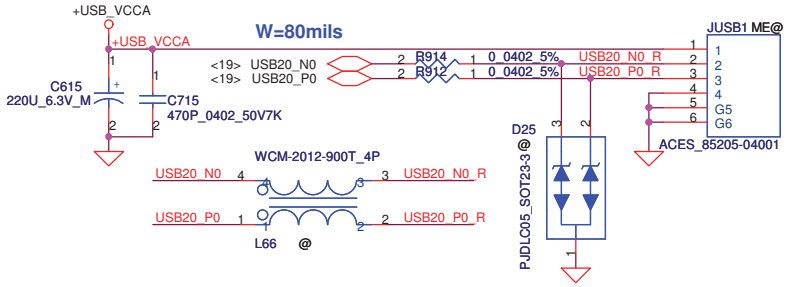
PVT Change U19 and U27 part number from SA000039E00 to SA00002XX00

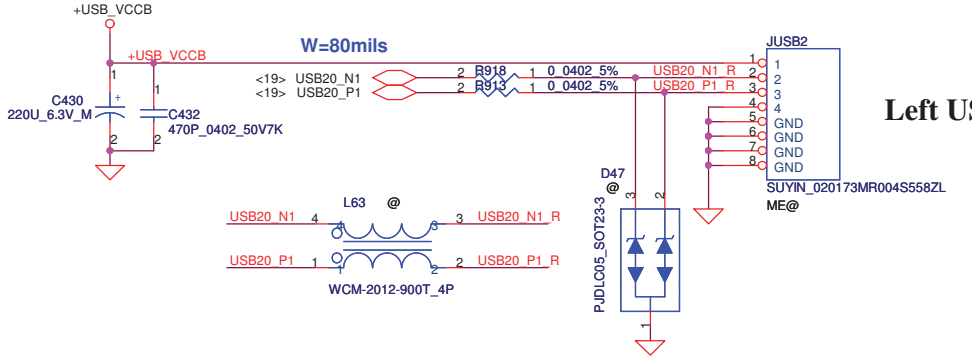


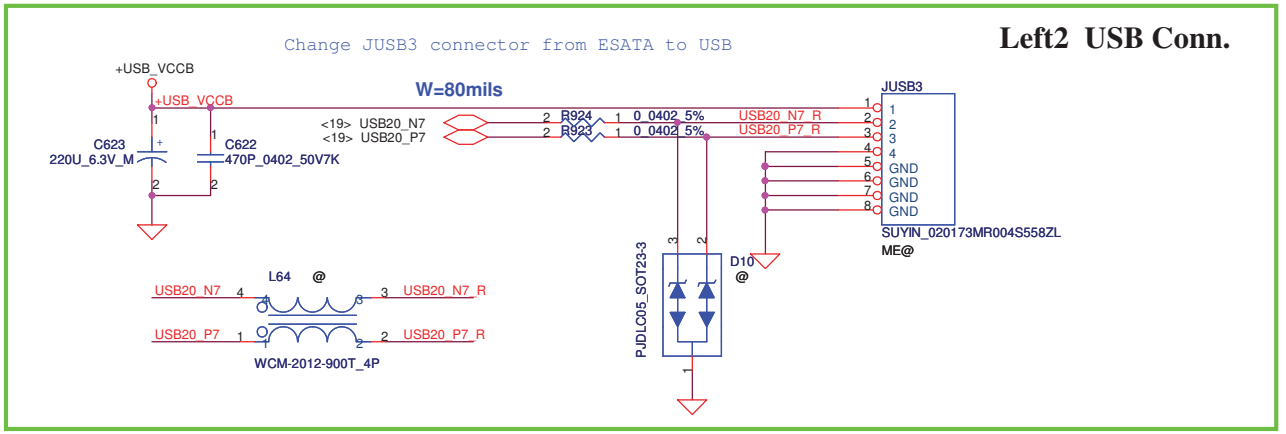


Pre MP ADD for ESD solution









Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

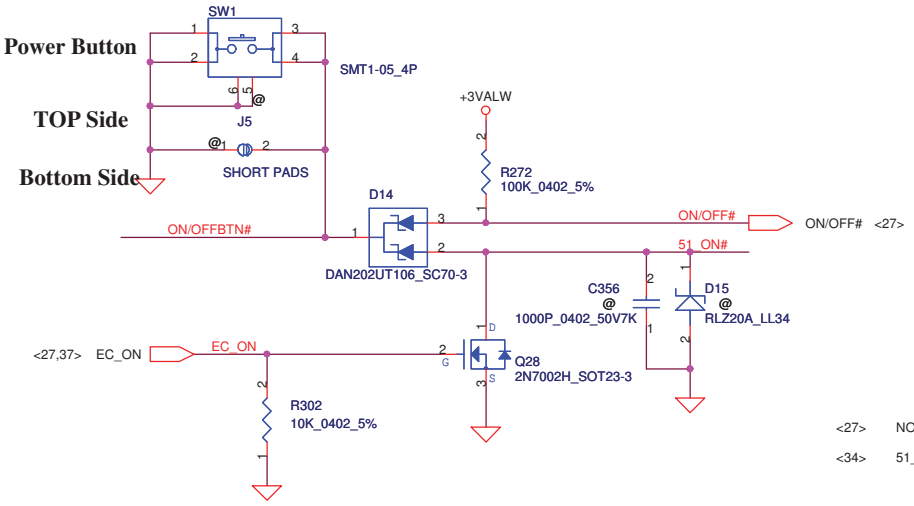
Compal Electronics, Inc.

Title: USB ports/BT

Size	Document Number	Rev
B	LA7011P	1.0

Date: Friday, December 24, 2010 Sheet 29 of 41

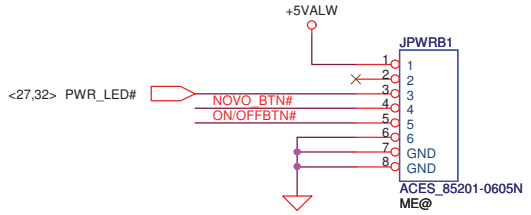
ON/OFF switch

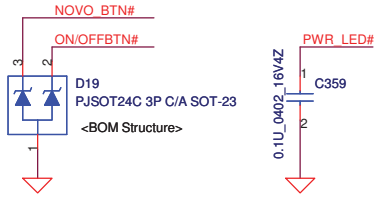


Power Bottom Board Conn. 6pin

10/11 Change JPWRB1 P/N from SP010009O10 to SP01000LB00

Add C359 to PWR_LED# for ESD solution.

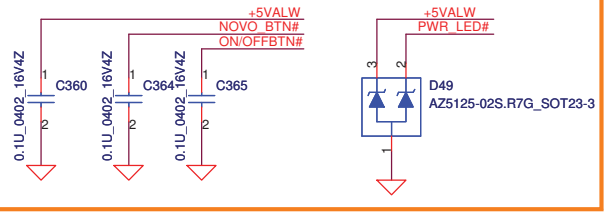


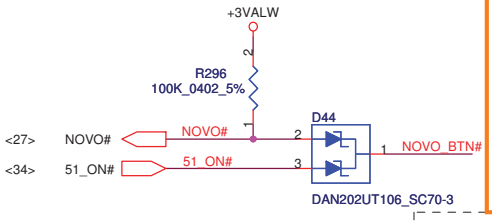


EMI REQUEST 1ST = SCA00000E00

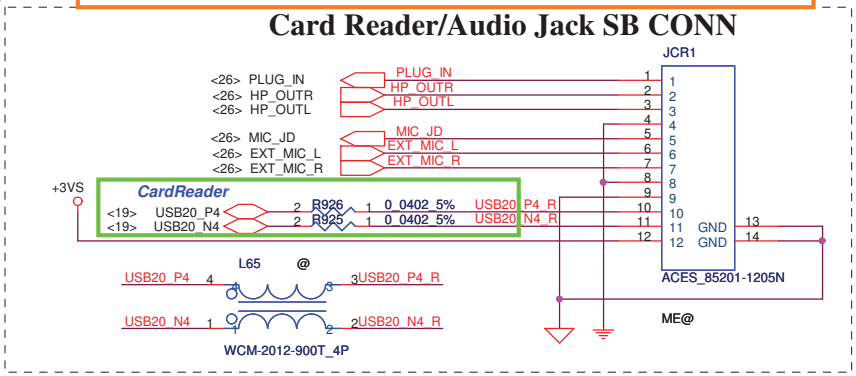
2ST = SCA00000R00

PVT ESD solution.

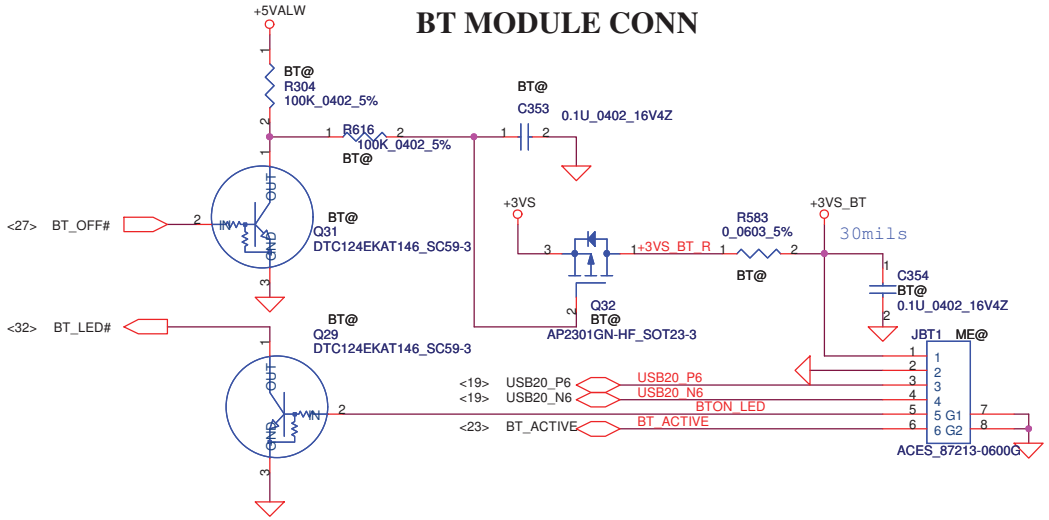


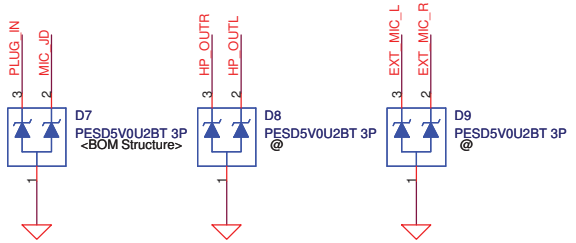


Card Reader/Audio Jack SB CONN



BT MODULE CONN





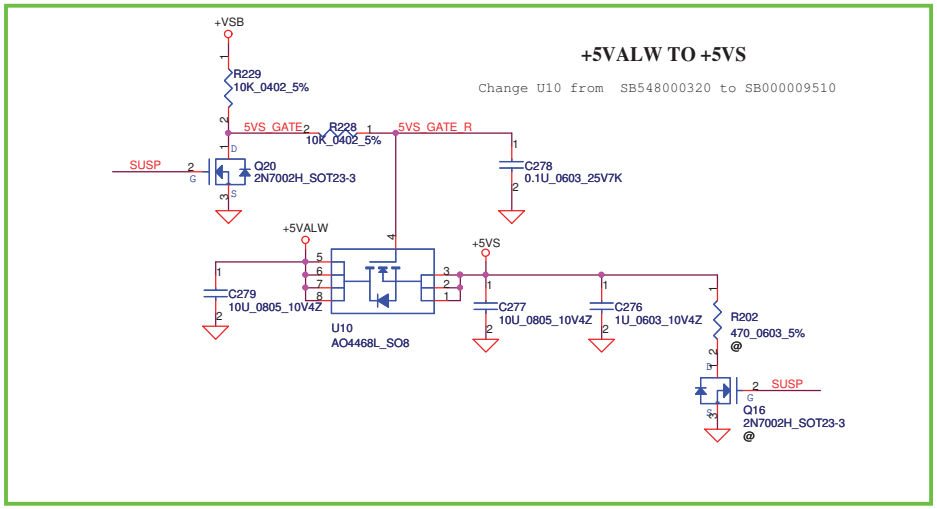
Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

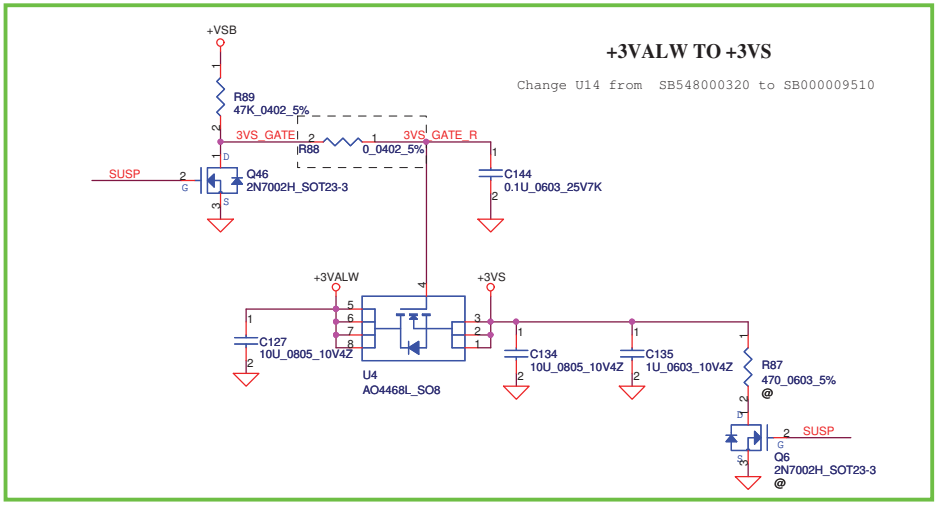
Compal Electronics,Ltd.

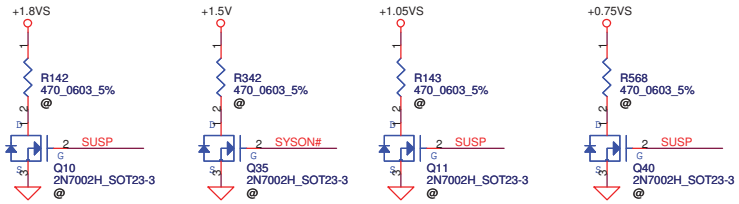
Title: **Audio Jack & SW & BT Conn.**

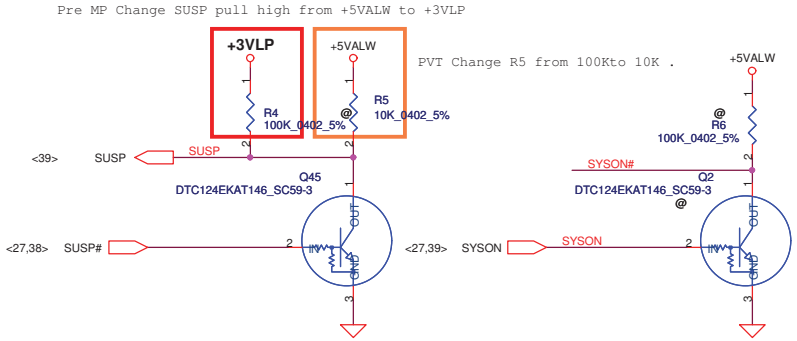
Size	Document Number	Rev
B	LA7011P	1.0

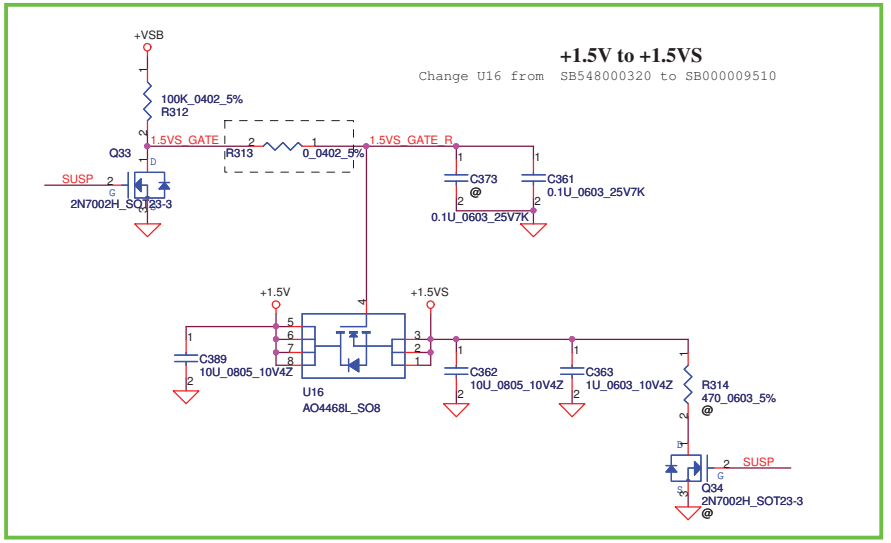
Date: Friday, December 24, 2010 Sheet 30 of 41











Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

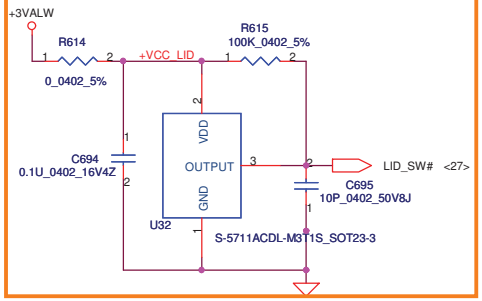
Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA7011P	1.0

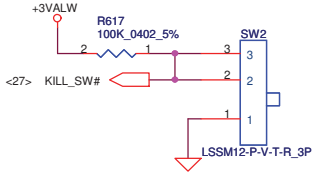
Date: Friday, December 24, 2010 | Sheet 31 of 41

Lid Switch



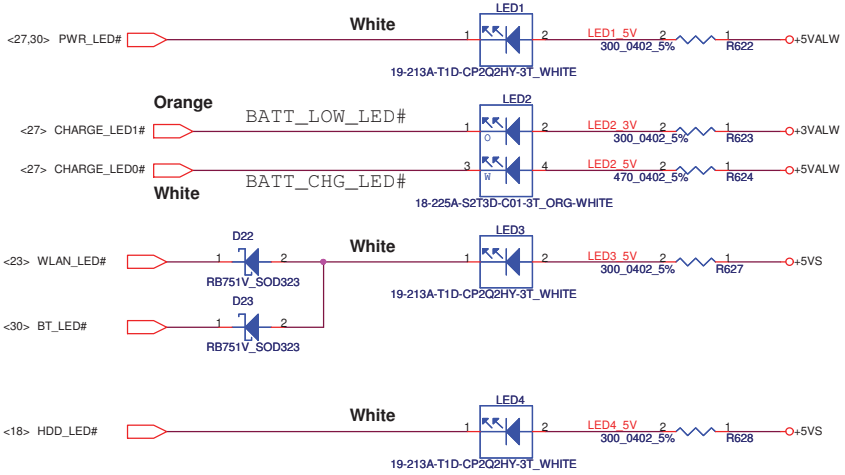
Kill Switch

STATUS	
1,2(LOW)	OFF
2,3(HI)	ON



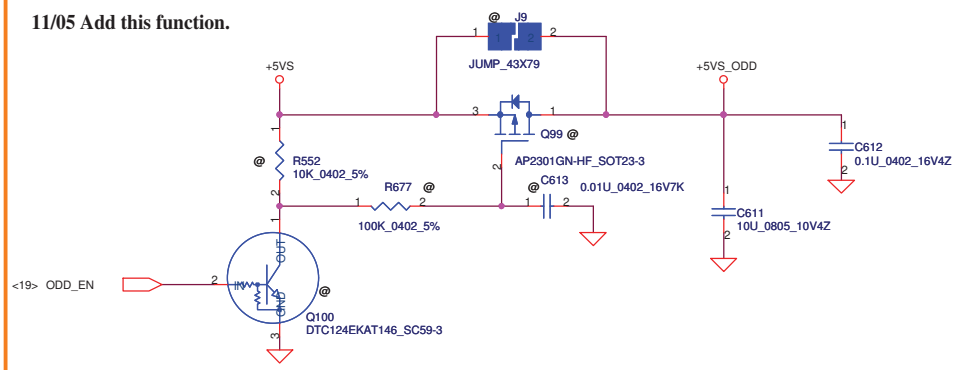
PVT Change U32 part number from SA032120010 to SA000031C00

LED

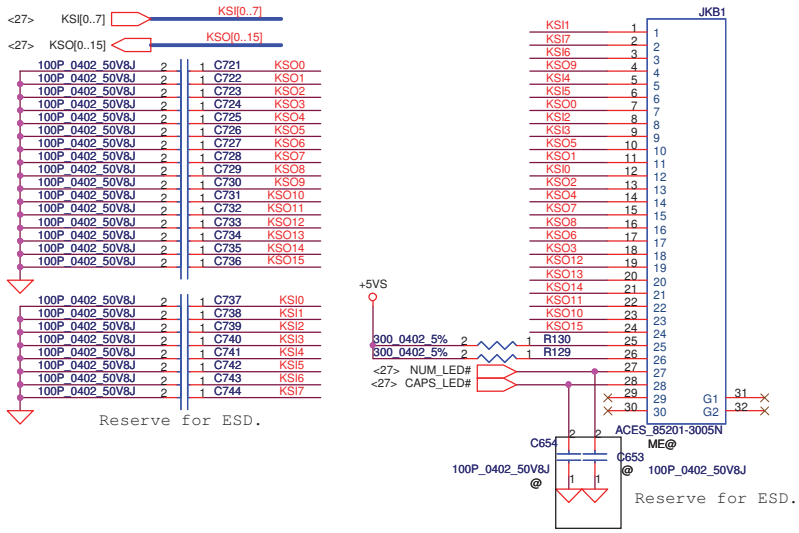


ODD Power Control

11/05 Add this function.



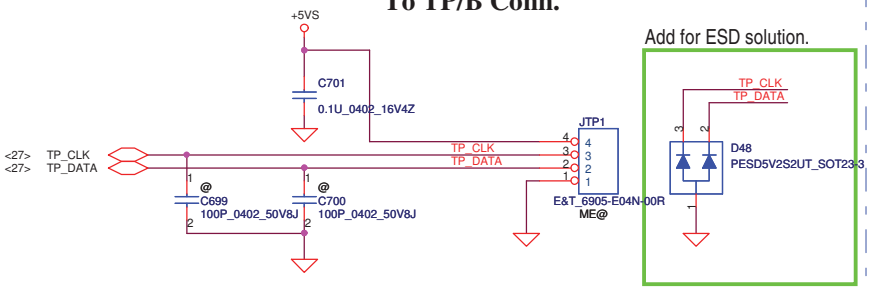
INT_KBD Conn.



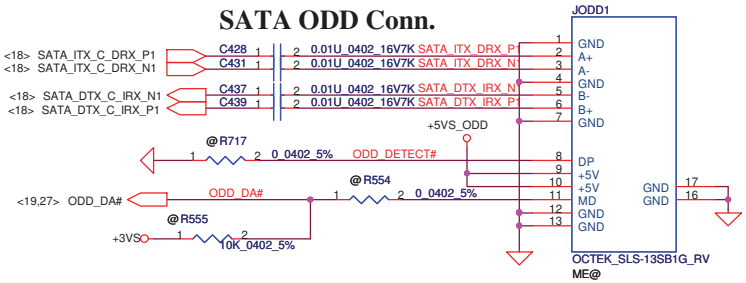
check connector & pin define.

CONN PIN define need double check

To TP/B Conn.



SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.

Title: KB/TP/LID/KLL/ODD/LED FOR 14

Size: Custom | Document Number: LA7011P | Rev: 1.0

Date: Friday, December 24, 2010 | Sheet 32 of 41

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
5							
6							
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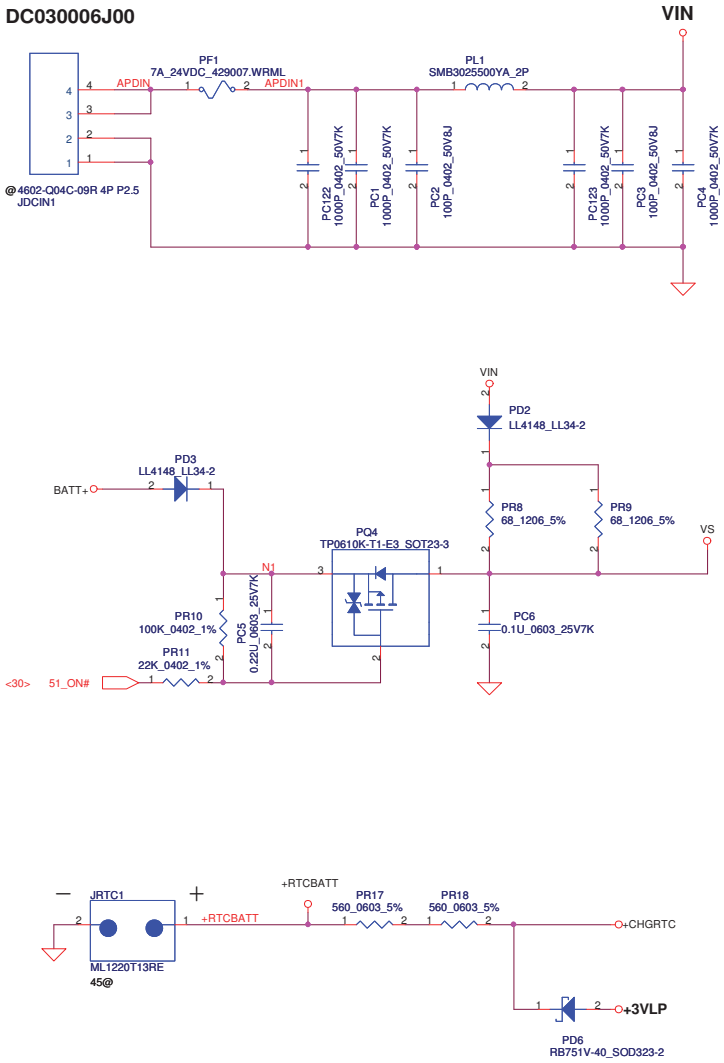
27							
28							
29							
30							
31							

Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

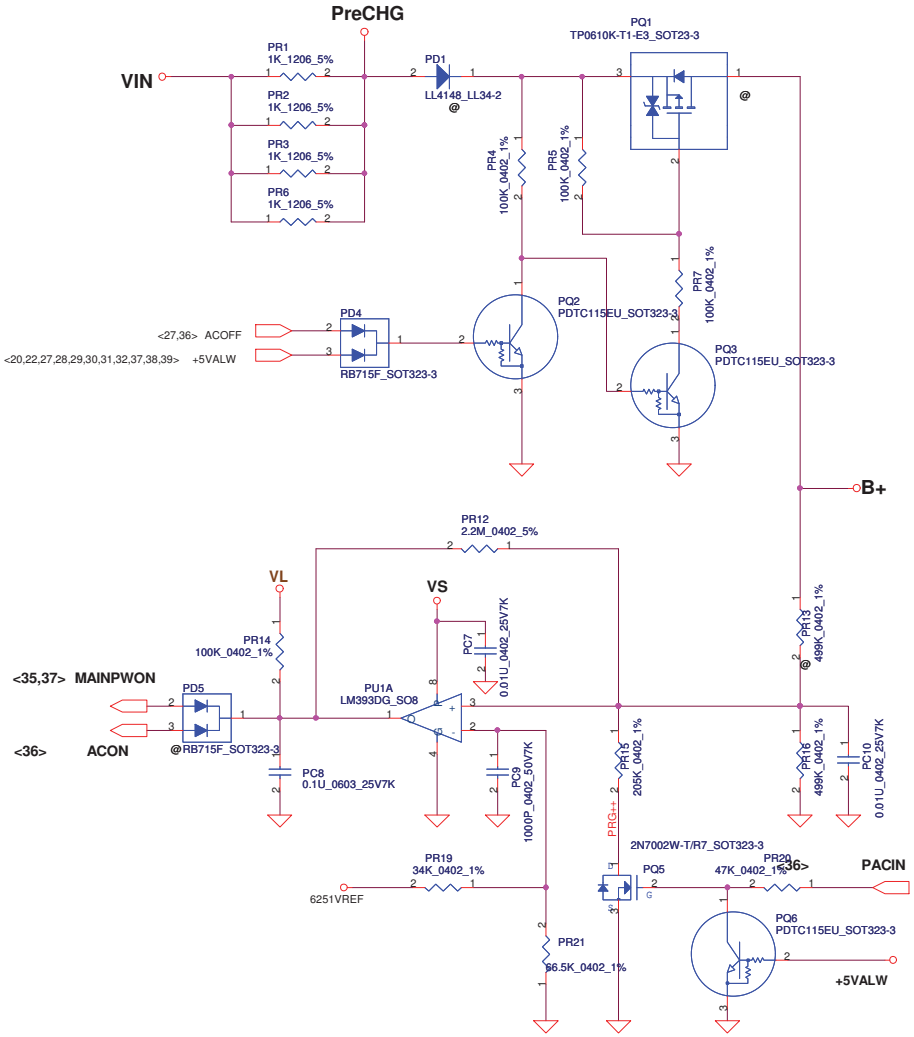
Compal Electronics, Inc.

Title	HW PIR	
Size: Custom	Document Number: LA7011P	Rev: 1.0
Date: Friday, December 24, 2010	Sheet 33 of 41	

DC030006J00



Precharge detector 15.97V/14.84V FOR ADAPTOR



ACIN

Precharge detector	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.

Title: DCIN / Vin Detector /Pre-charge

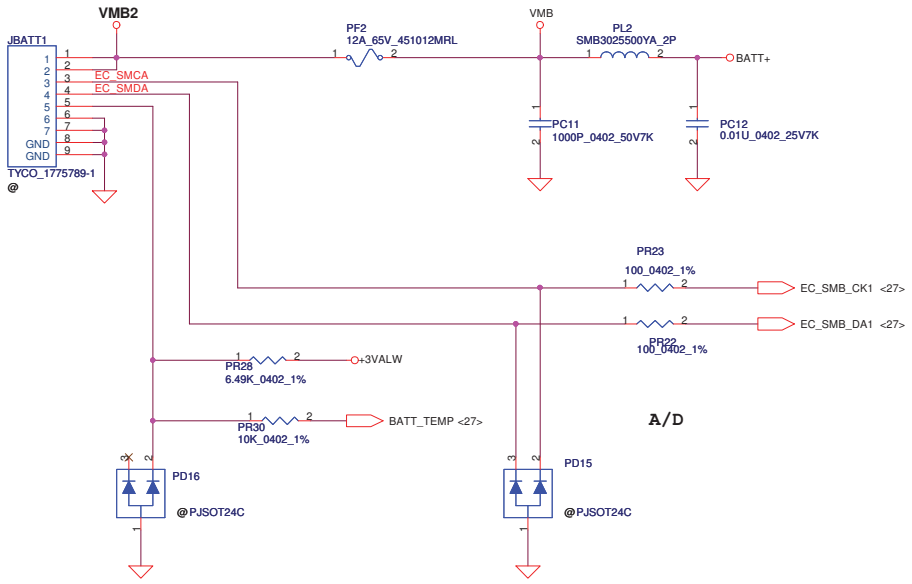
Size: Custom | Document Number | Rev: 1.0

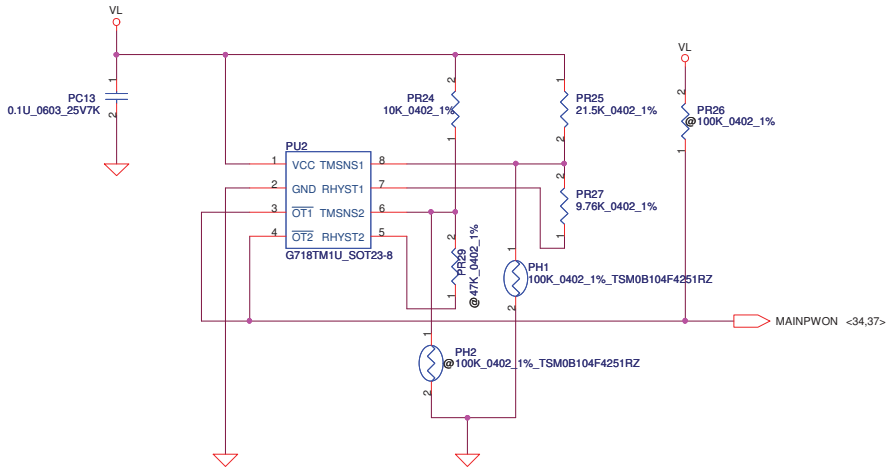
Date: Friday, December 24, 2010 | Sheet 34 of 41

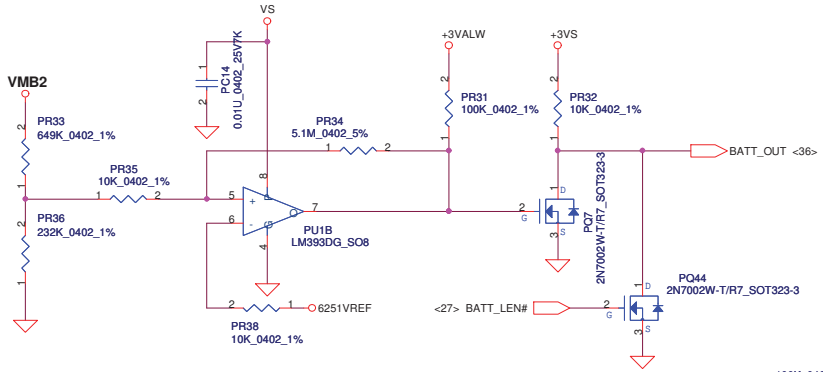
PH1 under CPU botten side :

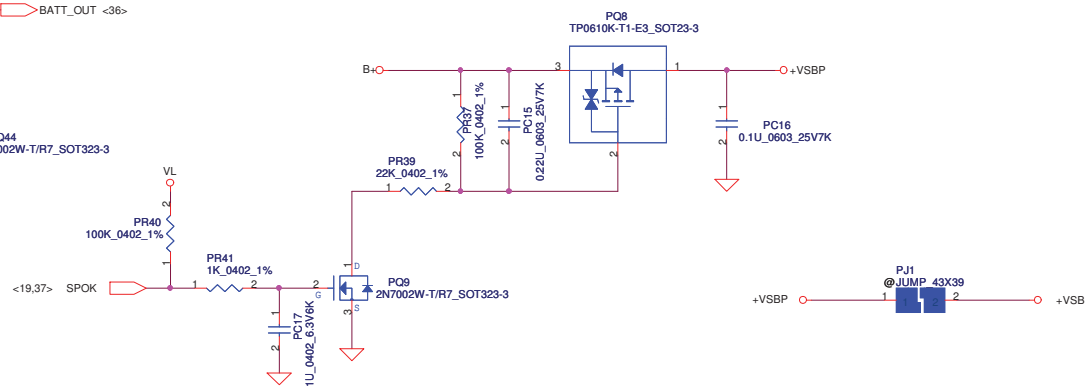
CPU thermal protection at 92 degree C

Recovery at 56 degree C









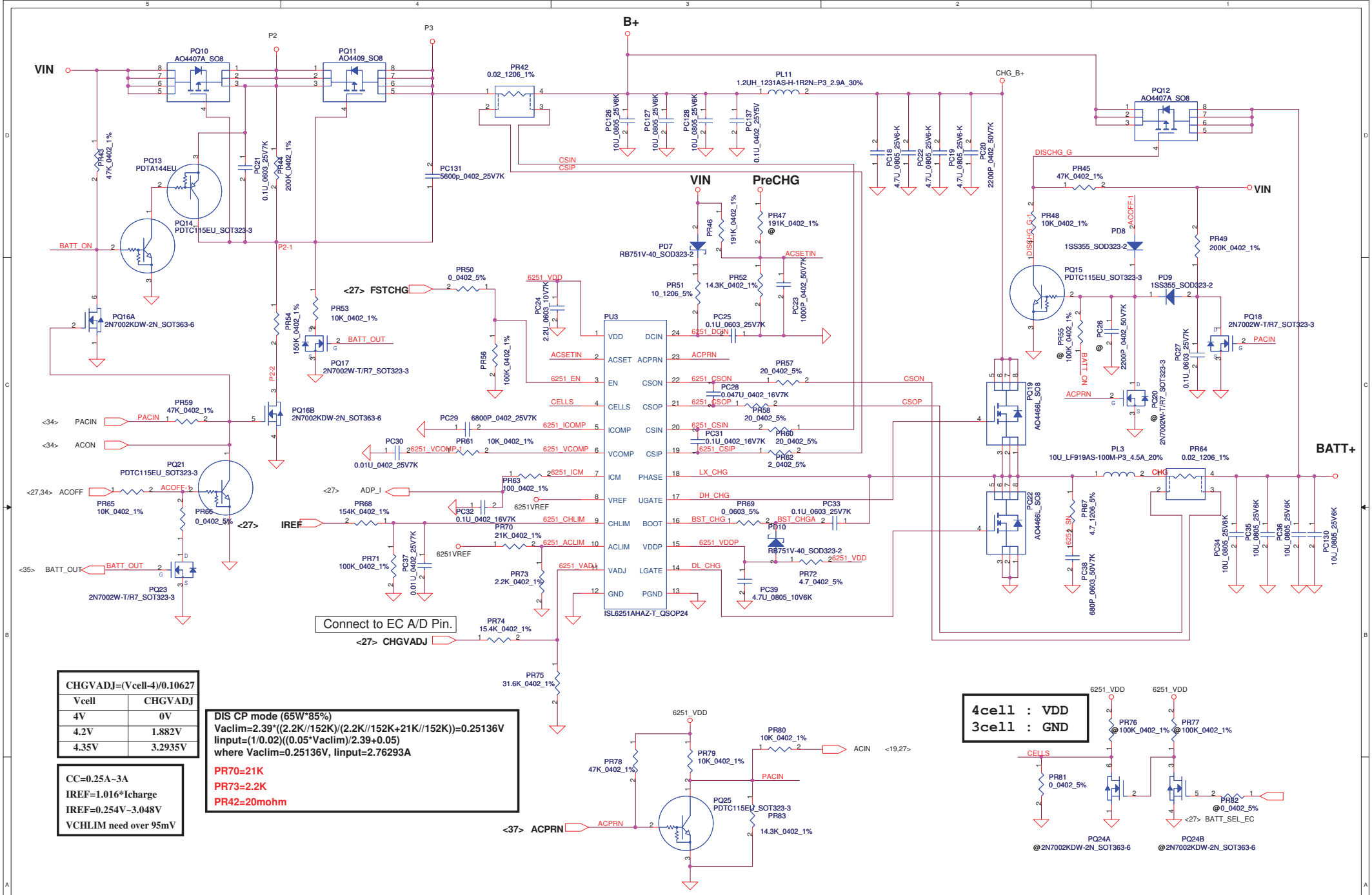
Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.

Title: BATTERY CONN/OTP

Size: Custom | Document Number | Rev: 1.0

Date: Friday, December 24, 2010 | Sheet 35 of 41



Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

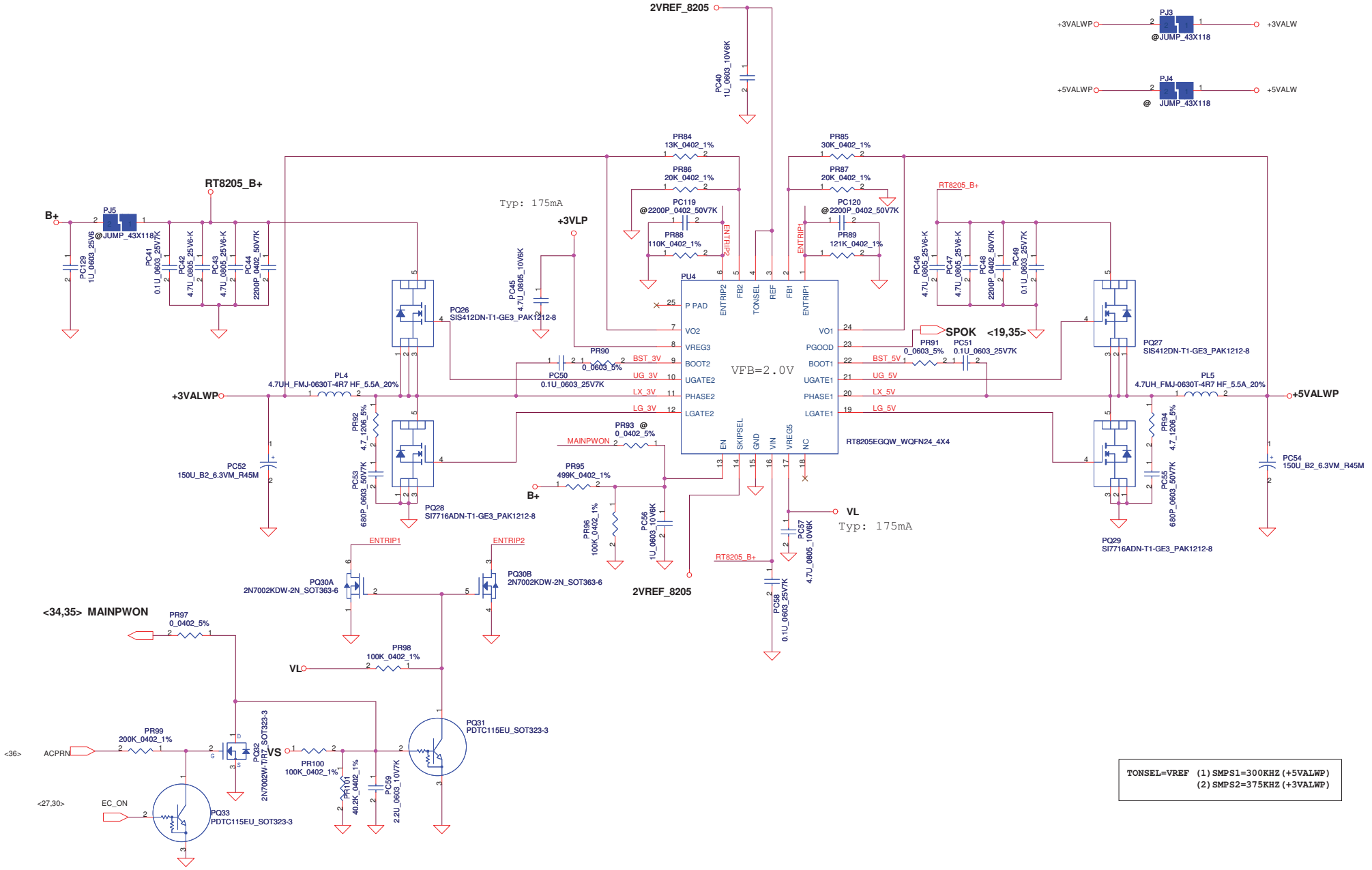
Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
		1.0

Date: Friday, December 24, 2010 Sheet 36 of 41

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
(2) SMPS2=375KHZ (+3VALWP)

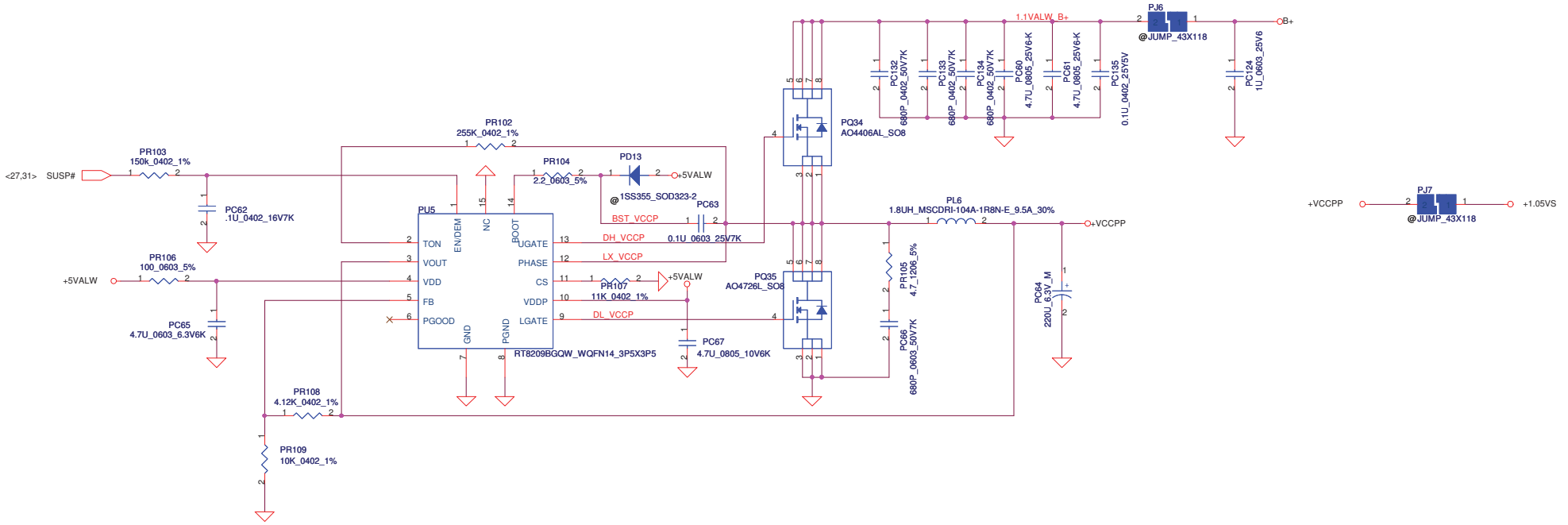
Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number | Rev: 1.0

Date: Friday, December 24, 2010 | Sheet 37 of 41



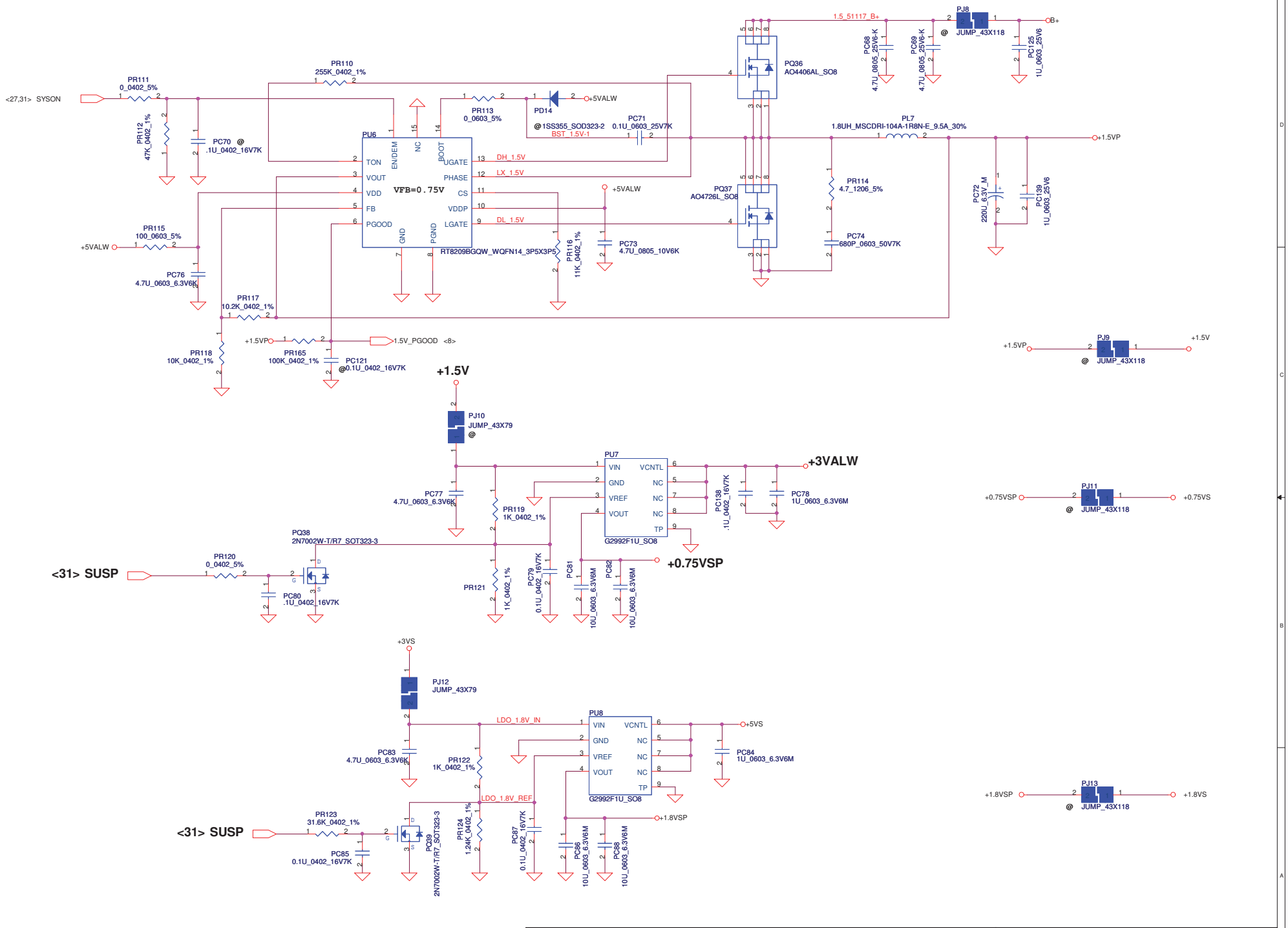
Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.

Title: VCCP

Size	Document Number	Rev
		1.0

Date: Friday, December 24, 2010 Sheet 38 of 41



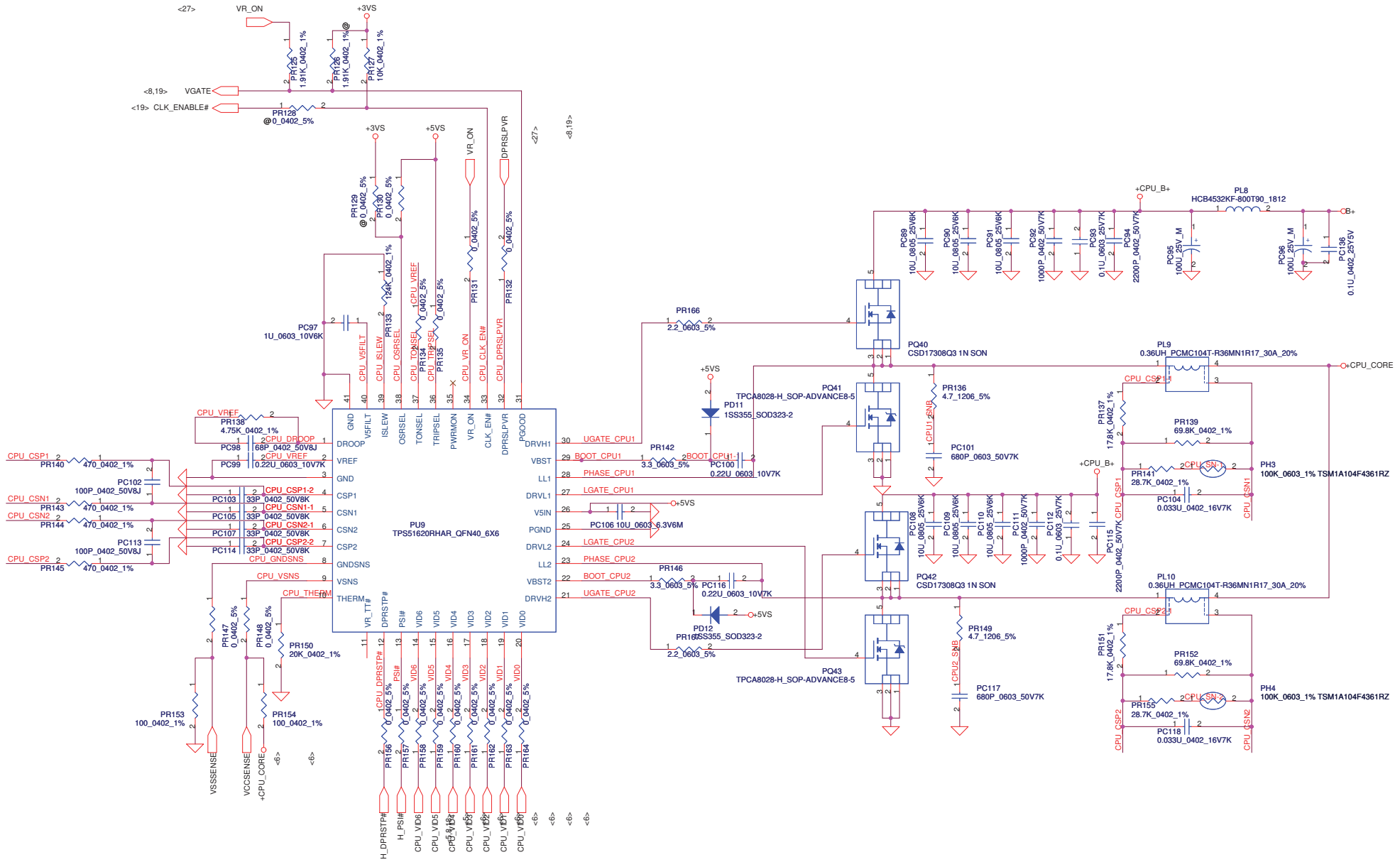
Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.

Title: 1.5VP/1.8VSP/0.75VSP

Size	Document Number	Rev
		1.0

Date: Friday, December 24, 2010 Sheet 39 of 41



Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
Custom		1.0

Date: Friday, December 24, 2010 | Sheet 40 of 41

Version Change List (P. I. R. List) for Power Circuit

Page#	Title	Date	Request Owner	Issue Description	Solution Description
P35,37,39	Add capacities for EMI request	2010.11.12	EMI	EMI test fail	Add PC132,PC133,PC134,PC135,PC136,PC137
P37	Change resistance for EMI request	2010.11.12	EMI	EMI test fail	Change PR104 from 0 ohm to 2.2ohm
P35	Add one capacitor for prevent inrush current too large	2010.11.12	PWR	If there isn't add capacity, the MOS of PQ11 have damged risk.	Add PC131 which value is 5600PF
P34	Add one transistor for improve design margin	2010.11.12	PWR	If there isn't add transitor, the design margin of PQ11 is not enough.	Add PQ44
P39	Change resistance for CPU loadline fine tuning	2010.11.12	PWR	For meet the load line of intel spec	Change PR138 from 4.3k to 4.75k
P35	Add one capacitor for improve ripple current	2010.11.12	PWR	For meet the ripple current spec of Compal	Add PC130

Compal Electronics, Inc.

Title: Power PIR

Size: Custom | Document Number: LA7011P | Rev: 1.0

Date: Friday, December 24, 2010 | Sheet 41 of 41