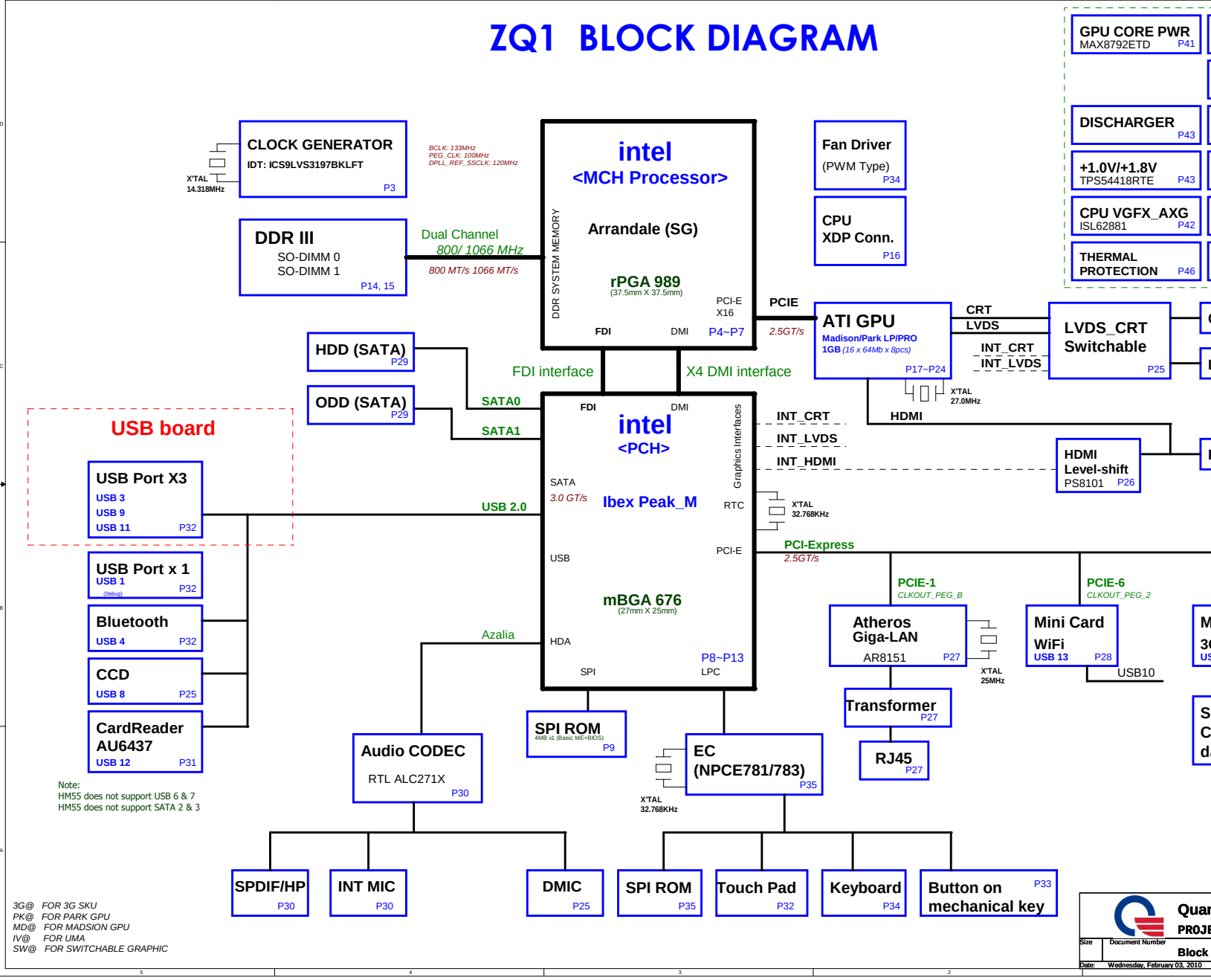
ZQ1 BLOCK DIAGRAM



Note:
HM55 does not support USB 6 & 7
HM55 does not support SATA 2 & 3

3G@ FOR 3G SKU
PK@ FOR PARK GPU
MD@ FOR MADSION GPU
IV@ FOR UMA
SW@ FOR SWITCHABLE GRAPHIC

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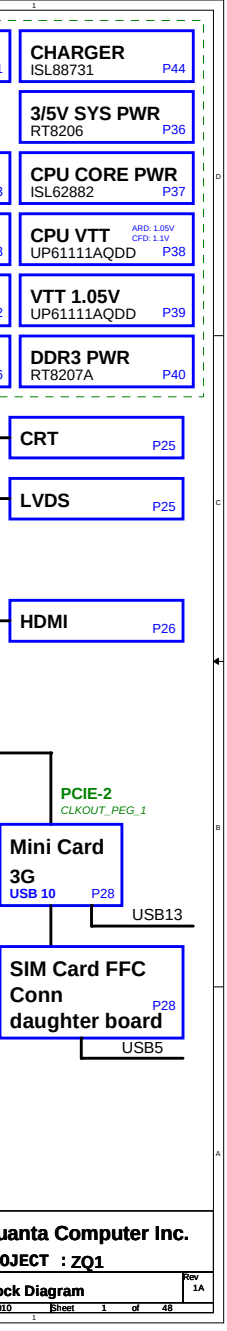
Size | Document Number | Block
Date: Wednesday, February 03, 2010



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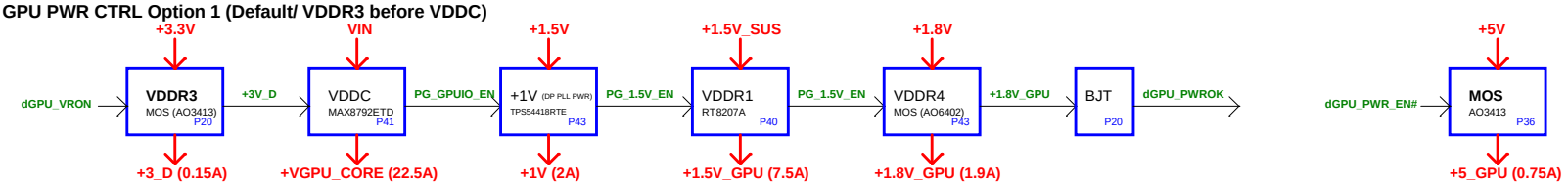
0JECT : ZQ1

ock Diagram

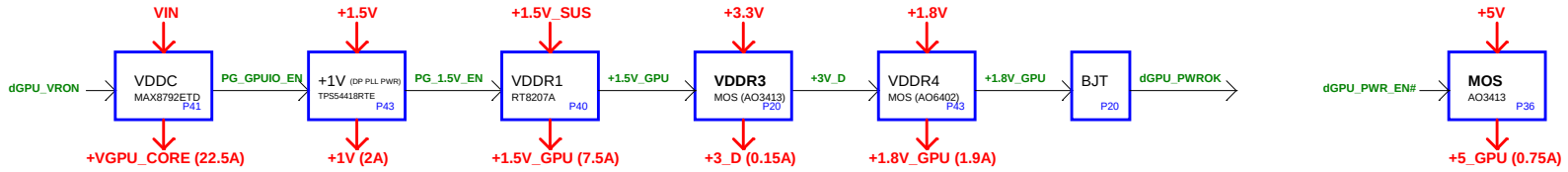
Rev 1A

10 Sheet 1 of 48

GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



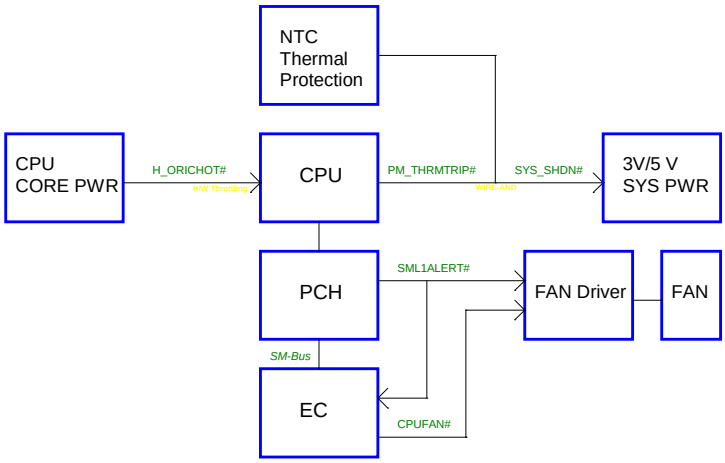
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER		S0~S5
+VCCRTC	+3V~+3.3V	RTC		S0~S5
+3VPCU	+3.3V	8051 POWER	ALWON	S0~S5
+5VPCU	+5V	CHARGE POWER	ALWON	S0~S5
+15V	+15V	LARGE POWER	+15V_ALWP	S0~S5
+5V_S5	+5V		S5D	S0~S5
+3V_S5	+3.3V		S5D	S0~S5
+3VSUS	+3.3V		SUSD	S0, S3
+1.5V_SUS	+1.5V	SODIMM POWER	SUSON	S0, S3
+0.75V_DDR_VTT	+0.9V	SODIMM POWER	MAINON	S0
+5V	+5V		MAIND	S0
+3V	+3.3V		MAIND	S0
+1.8V	+1.8V		MAINON	S0
+1.5V	+1.5V	PCH POWER	MAIND	S0
+1.1V_VTT	+1.05V~+1.1V	CPU POWER	MAINON	S0
+1.05V	+1.05V	PCH POWER	MAINON	S0
+VCC_CORE	0V~+1.5V	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD Power	LVDS_VDDEN	S0
MBAT+	+10V~+17V	MAIN BATTERY		

Thermal Follow Chart



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PWR Status &
Date: Monday, February 01, 20

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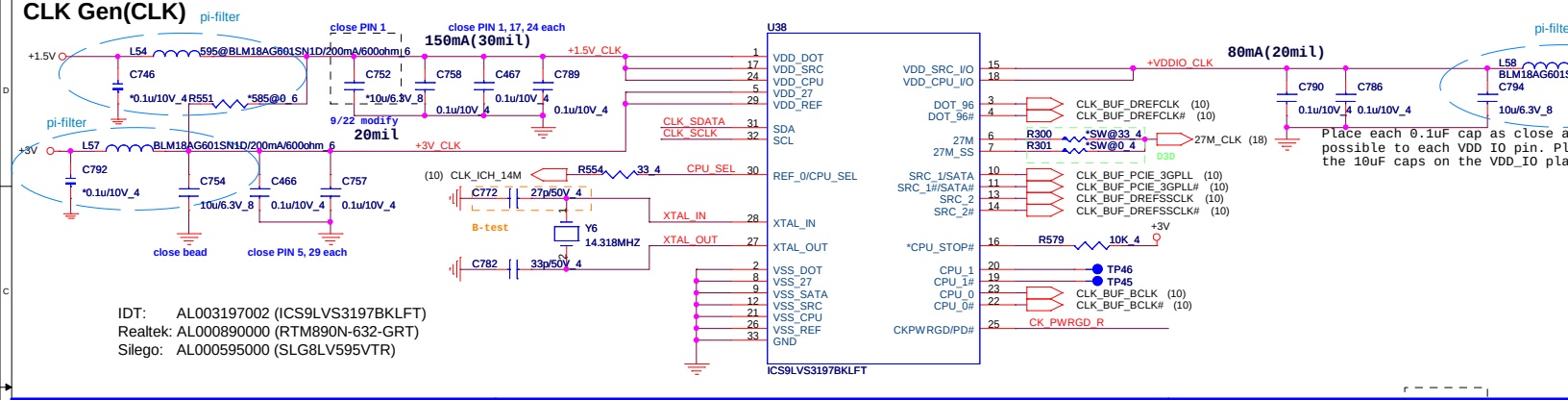
PROJECT : ZQ1

s & GPU PWR CRL & THRM

Rev 1A

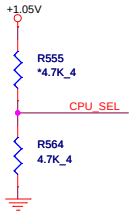
01, 2010 Sheet 2 of 48

CLK Gen(CLK)



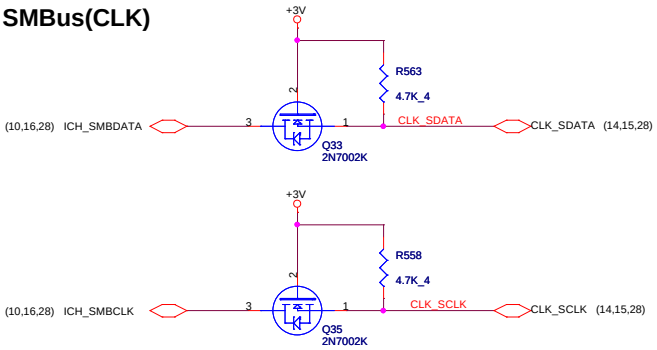
IDT: AL003197002 (ICS9LVS3197BKLFT)
Realtek: AL000890000 (RTM890N-632-GRT)
Silego: AL000595000 (SLG8LV595VTR)

CPU_CLK select(CLK)

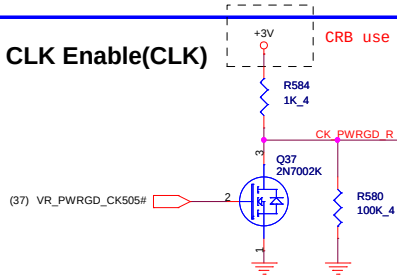


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus(CLK)



CLK Enable(CLK)



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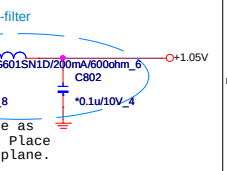
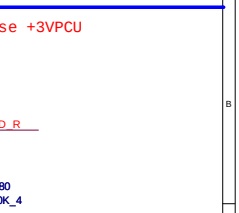
Size	Document Number
	Clock Generator

Date: Tuesday, March 30, 2010





ta Computer Inc.

CT : ZQ1

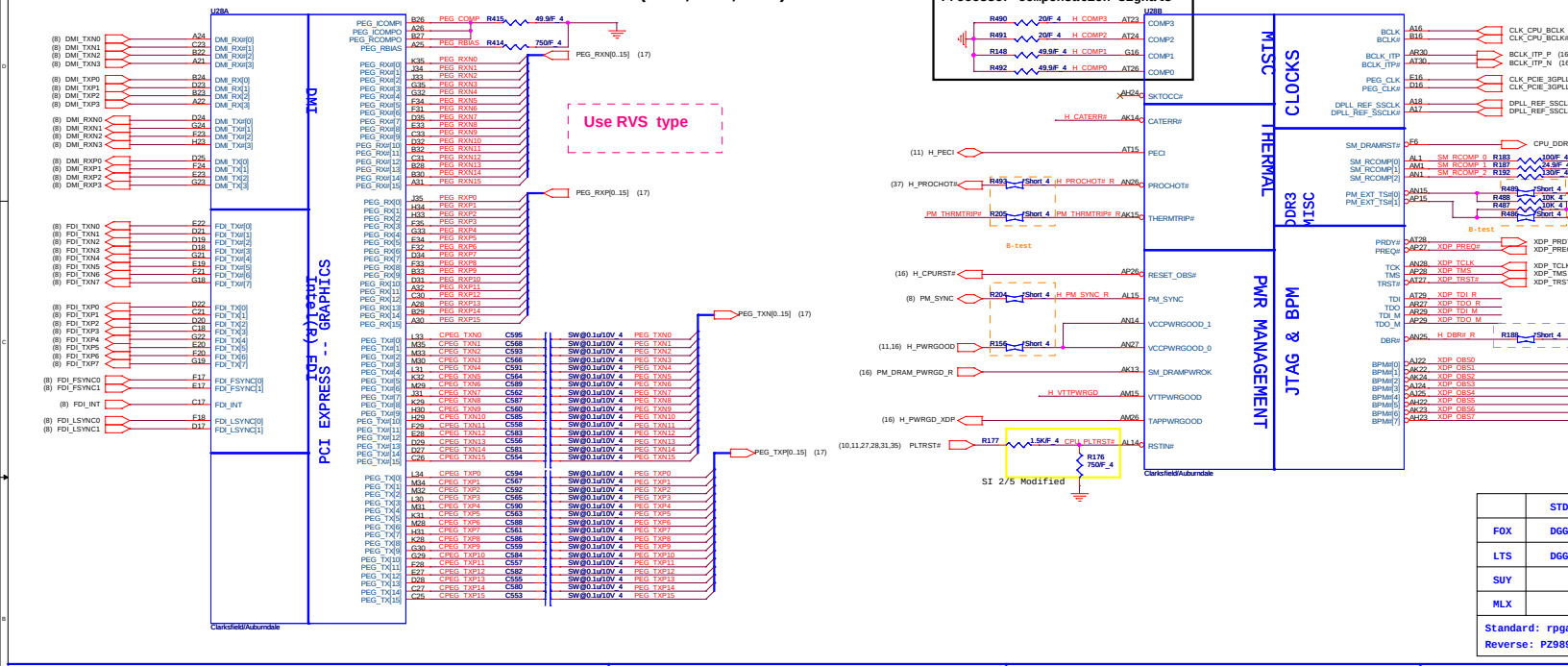
Rev 1A

Sheet 3 of 48

Arrandale_1(CPU)

AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JT

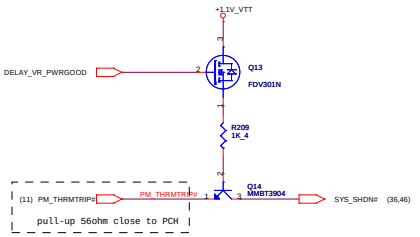
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



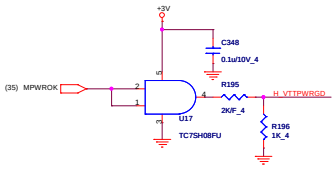
	STD
FOX	DGG
LTS	DGG
SUY	
MLX	

Standard: rpga
Reverse: PZ985

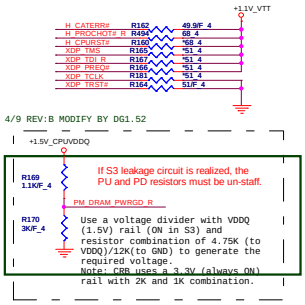
Thermaltrip protect(CPU)



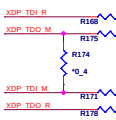
VTT PWR_Good(CPU)



Processor pull-up(CPU)



JTAG MAPPING(CI



Scan Chain (Default)	STUFF NO ST
CPU Only	STUFF NO ST
GMCH Only	STUFF NO ST

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AUBURN
Date: Tuesday, March

JTAG)

BCLK (11)
BCLK# (11)

P (16)
N (16)

3GPLL (10)
3GPLL# (10)

SSCLK (10)
SSCLK# (10)

U_DDR3_DRAMRST# (16)

00/F 4
04 3/F 4
03/F 4

ort 4
0K 4
0K 4
ort 4

PM_EXTTS#0 (14)
+1.1V_VTT
PM_EXTTS#1 (15)

P_PRDY# (16)
P_PREQ# (16)

P_TCLK (16)
P_TMS (16)
P_TRST# (16)

C3C

ort 4

XDP_DBRST# (8,16)
XDP_OBS[0:7] (16)

STD
DGG^9000024
DGG^9000022
rpga989-aca-zif-069-k01-socket
Z98927-364R-01F-SOCKET

(CPU)

XDP_TDI (16)
XDP_TDO (16)

*0_4
*0_4
*0_4
*0_4

STUFF -> R469, R491, R507
NO STUFF -> R489, R490

STUFF -> R490, R491
NO STUFF -> R469, R489, R507

STUFF -> R489, R507
NO STUFF -> R491, R490, R469

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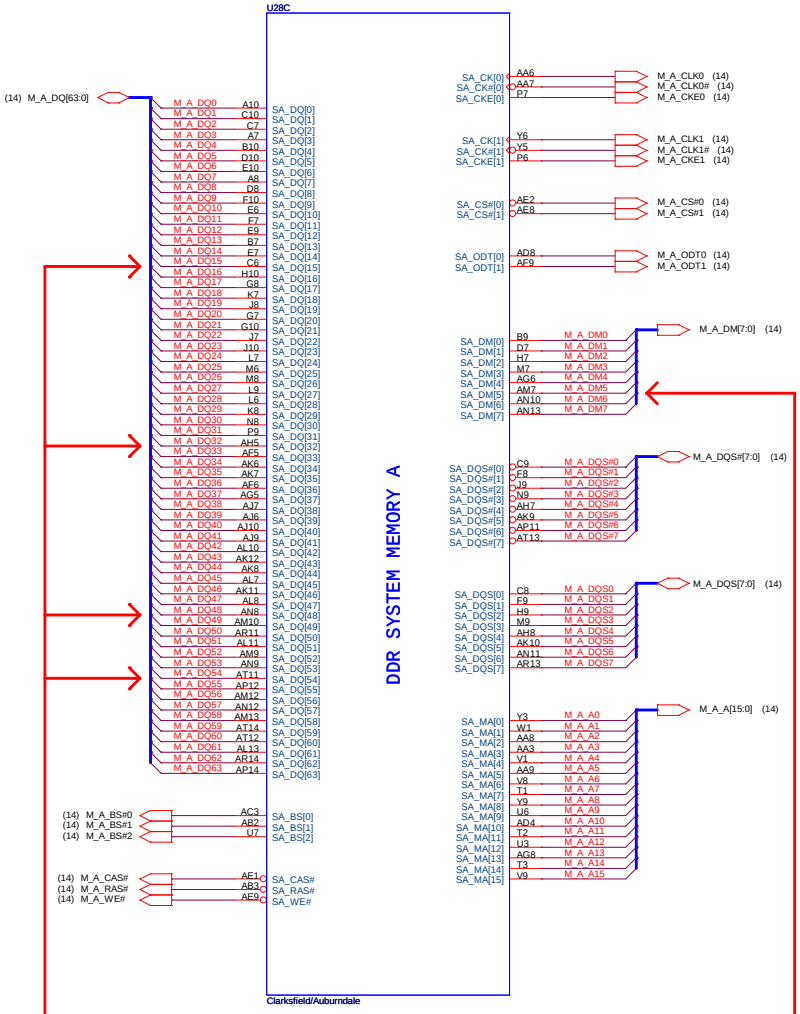
PROJECT : ZQ1

t Number URNDA 1/4	Rev 1A

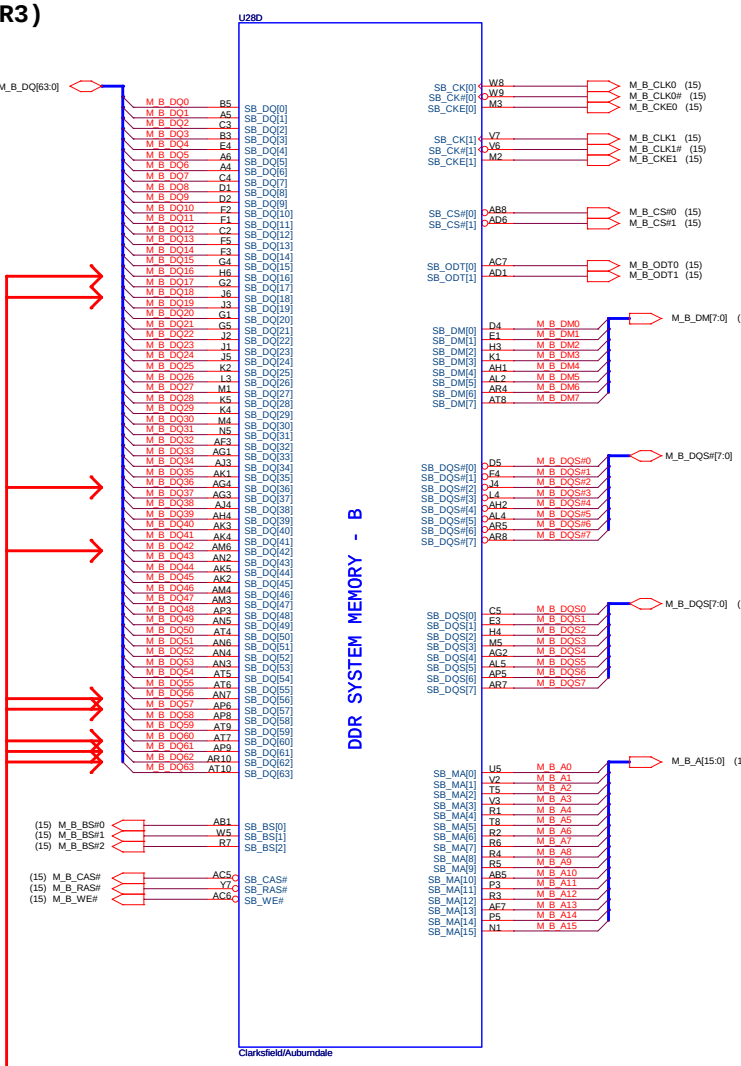
March 30, 2010 Sheet 4 of 48

Arrandale_2(CPU)

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.



Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

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PROJECT : ZQ1

Size	Document Number	
	AUBURNDA 2/4	
Date: Tuesday, March 30, 2010	Sheet 5 of 4	

:0] (15)

7:0] (15)

:0] (15)

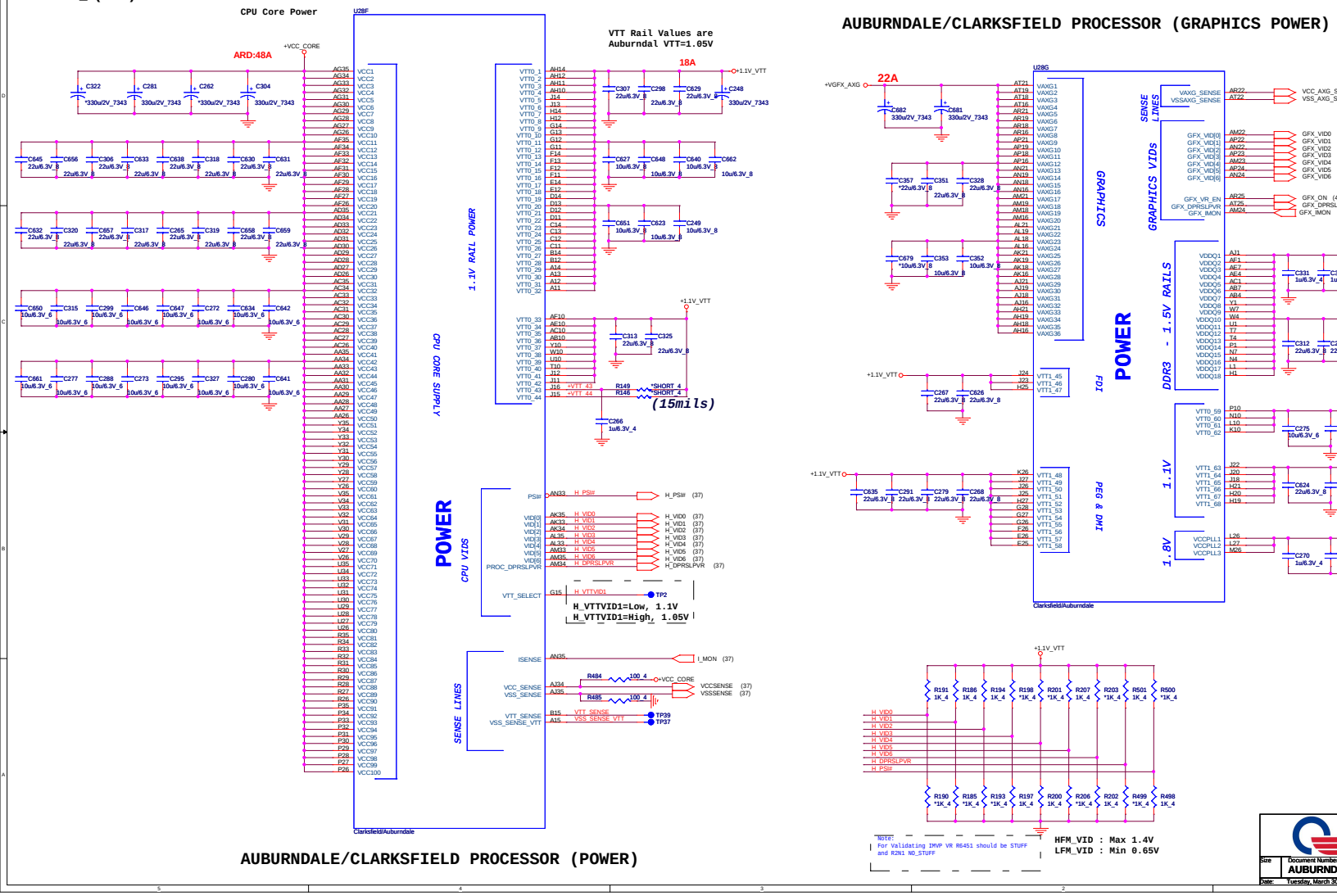
0] (15)

r Inc.

Rev
1A

48

Arrandale_3(CPU)



AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

Size: Document Number: AUBURND

Date: Tuesday, March 3

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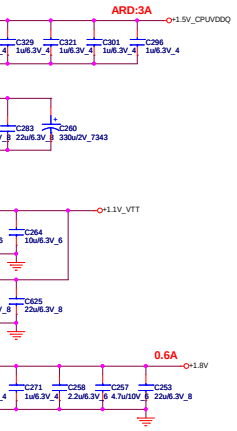
AXG_SENSE (43)
AXG_SENSE (43)

VID0 (43)
VID1 (43)
VID2 (43)
VID3 (43)
VID4 (43)
VID5 (43)
VID6 (43)

ON (43)
DPRSLPVR (43)
MON (43)



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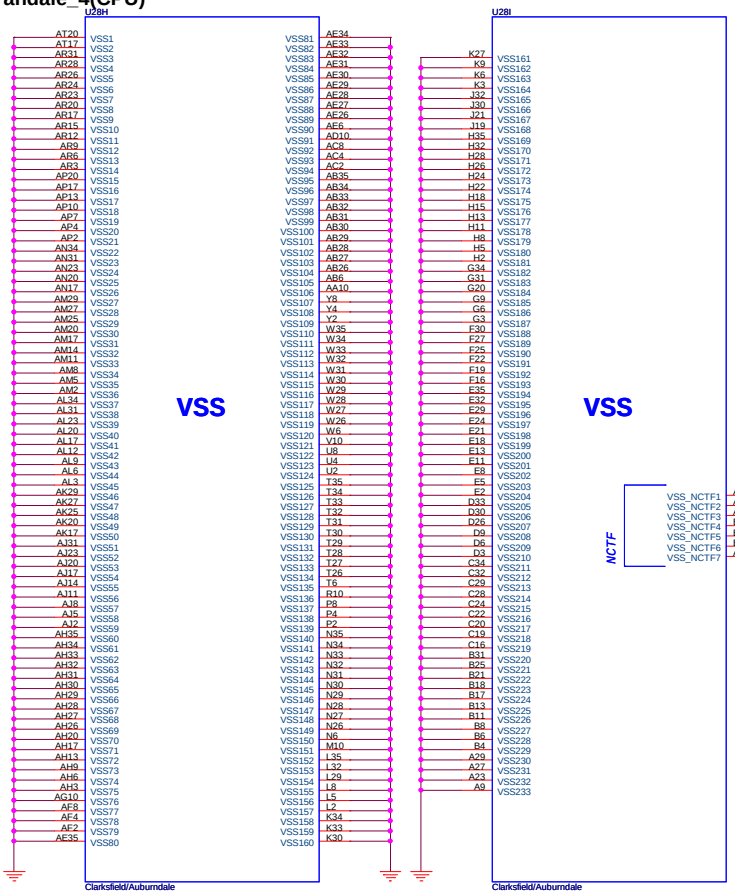
PROJECT : ZQ1

Number	Rev
RNDA 3/4 (PWR)	1A

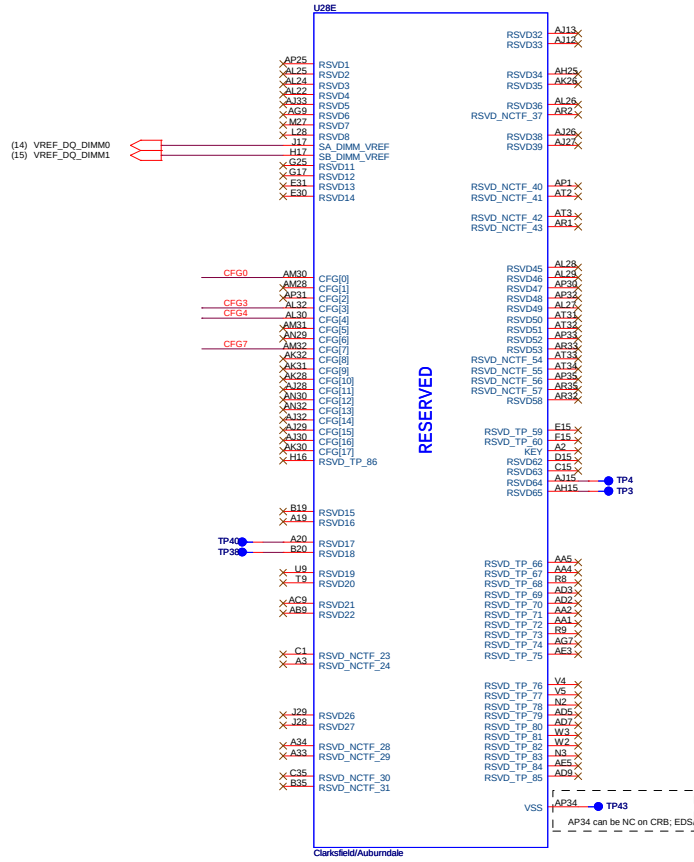
arch 30, 2010 Sheet 6 of 48

Arrandale_4(CPU)

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED,

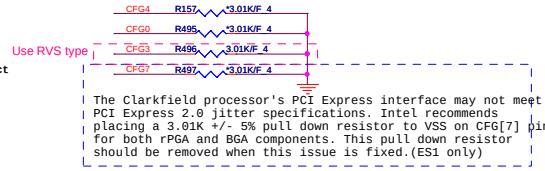


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

```
CFG[ 1:0 ] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG
```



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.(ES1 only)

Size | Document Number
AUBURNDA 4/4
Date: Tuesday, March 30, 2010

, CFG)

EDS/DG suggestion to GND

Quanta Computer Inc.

PROJECT : ZQ1

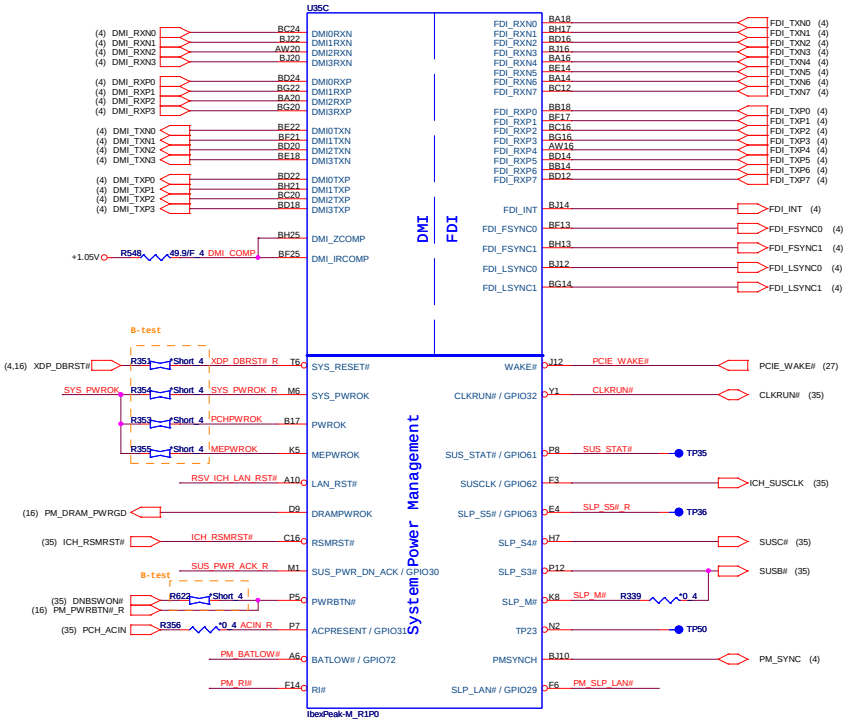
Rev 1A

4/4

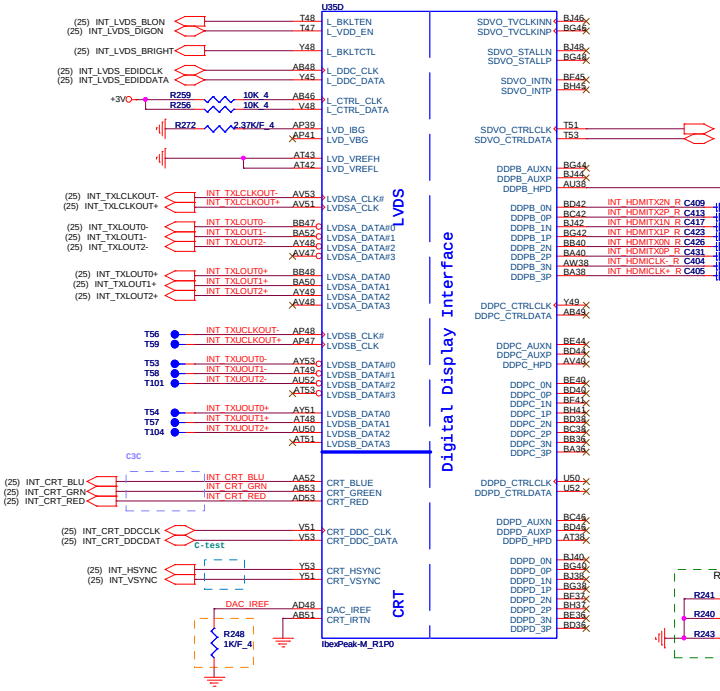
10 Sheet 7 of 48

PCH1(CLG)

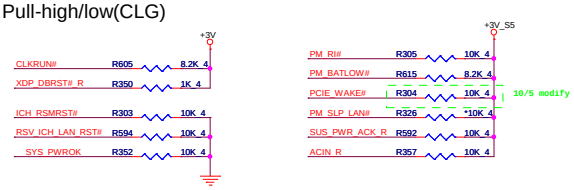
IBEX PEAK-M (DMI,FDI,GPIO)



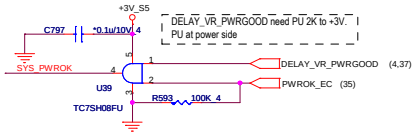
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low(CLG)

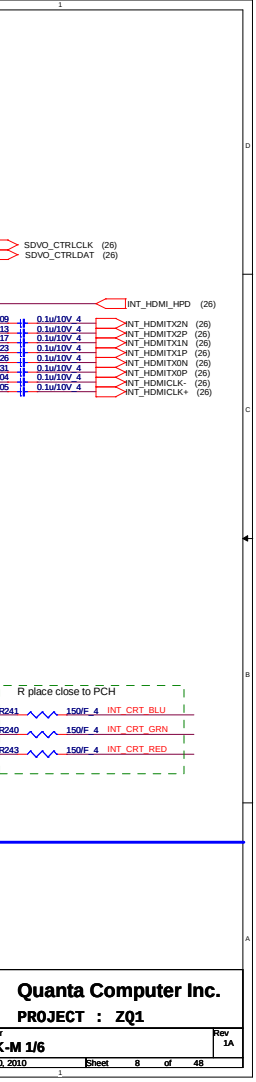


System PWR_OK(CLG)



Size	Document Number
	IBEX PEAK-M

Date: Tuesday, March 30, 2010



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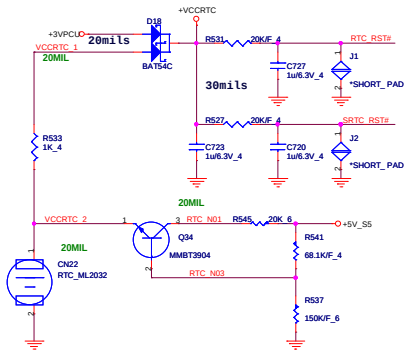
PROJECT : ZQ1

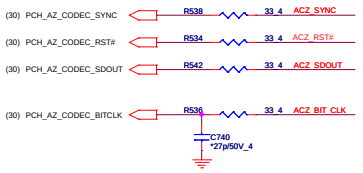
Rev 1A

K-M 1/6

RTC Circuitry(RTC)

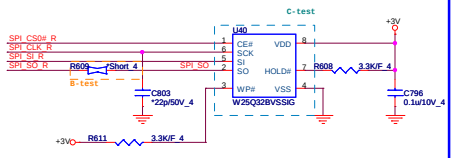


HDA Bus(CLG)

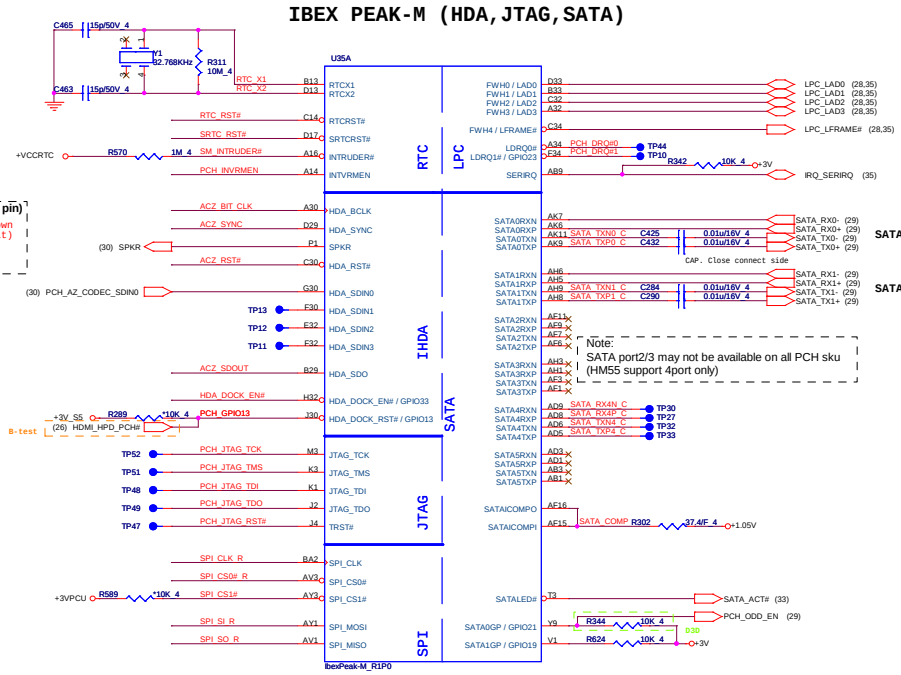


Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

PCH SPI(CLG)



PCH2(CLG)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	ZQ1 note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R601 *10K_4 SPKR
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R517 *10K_4 PCI_GNT3# (10)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**	+VCCRTC R567 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location 1 / 1 / SPI 1 / 0 / PCI 0 / 0 / **LPC**	**Default weak pull-up on GNT0/1#** **[Need external pull-down for LPC BIOS]** +3V R249 1K_4 R245 1K_4 R255 *1K_4 R254 *1K_4 C-test PCI_GNT0# (10) PCI_GNT1# (10)
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)	+1.8V R590 *1K_4 NV_ALE NV_ALE (10)
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm	+1.8V R591 *1K_4 NV_CLE NV_CLE (10)
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V R277 *1K_4 R273 *10K_4 HDA_DOCK_EN#
SPI_MOSI	iTPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R627 *1K_4 SPI_SI_R
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)	
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)	+3V_S5 R340 10K_4 RSV_GPIO8 (11)
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)	
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use defaul (0 = 1.8V supply)
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality	+3V_S5 R349 1K_4 CR_WAKE# (11)

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Size	Document Number	
	IBEX PEAK-M 2/6	
Date:	Tuesday, March 30, 2010	

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SATA HDD

SATA ODD

Quanta Computer Inc.

PROJECT : ZQ1

2/6

Rev 1A

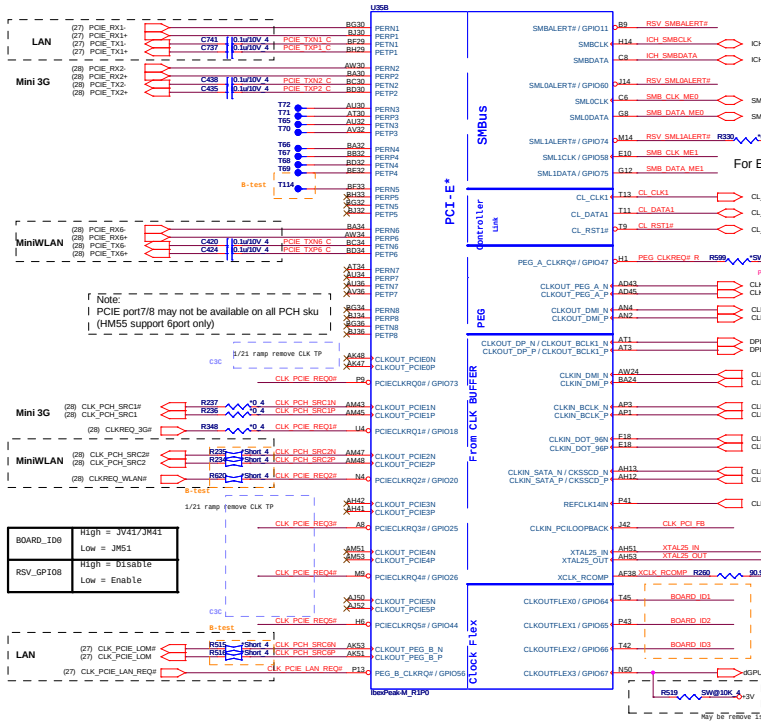
Sheet 9 of 48

PCH3(CLG)

IBEX PEAK-M (PCI,USB,NVRAM)

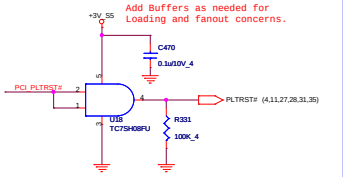
IBEX PEAK-M (PCI-E,SMBUS,CLK)

8/13 Swap Lan and WLAN/ Lan chagne to port 1

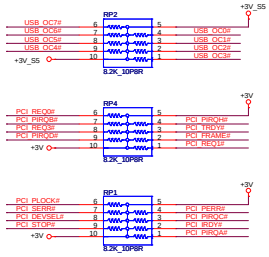


BOARD_ID0	High = JV41/JM41 Low = JM51
RSV_GPIO8	High = Disable Low = Enable

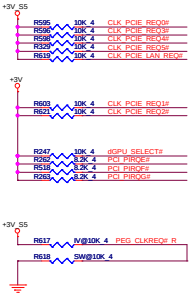
PLTRST#(CLG)



PCI/USBOC# Pull-up(CLG)



CLK_REQ/Strap Pin(CLG)



PEG_A_CLKRQ# PD for FreeRun, due GPU not support.

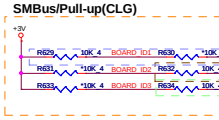
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Boot BIOS Strap		
GNT0#	GNT1#	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

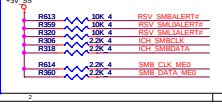
Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

SMBus/Pull-up(CLG)



BOARD_ID1	High = JV41_CP(ZQ1B) Low = JM41_CP(ZQ1B)
BOARD_ID2	High = 80port output to LPC Low = 80port output to PCI
BOARD_ID3	High = Reserved Low = Reserved (Default)



Size	Document Nu
	IBEX PE
Date:	Tuesday, Mar

ICH_SMBCLK (3,16,28)
ICH_SMBDATA (3,16,28)

SMB_CLK_ME0 (27) For LAN
SMB_DATA_ME0 (27)

*0_4 SML1ALERT# (11,34,35)

For EC

CL_CLK1 (28)
CL_DATA1 (28)
CL_RST1# (28)

*SW@0_4 PEG_CLKREQ# (18)
PEG_A_CLKRQ# PD for FreeRun, due GPU not support.

CLK_PCIE_VGA# (17)
CLK_PCIE_VGA (17)

CLK_PCIE_3GPLL# (4)
CLK_PCIE_3GPLL (4)

DPLL_REF_SSCLK# (4)
DPLL_REF_SSCLK (4)

CLK_BUF_PCIE_3GPLL# (3)
CLK_BUF_PCIE_3GPLL (3)

CLK_BUF_BCLK# (3)
CLK_BUF_BCLK (3)

CLK_BUF_DREFCLK# (3)
CLK_BUF_DREFCLK (3)

CLK_BUF_DREFSSCLK# (3)
CLK_BUF_DREFSSCLK (3)

CLK_ICH_14M (3)

C38 C695 10P/50V_4
RS12 1M_4
Y4 25MHz
90.9/F_4 +1.05V C696 10P/50V_4
B-test

No stuff XTAL25_IN and XTAL25_OUT circuitry until integrated CG becomes PCH POR.

INTEL FAE: If having UMA digital display (eDP/DP/DVI/HDMI), then 25MHz is required.

IGPU_EDIDSEL# (25)
+3V
move is OK

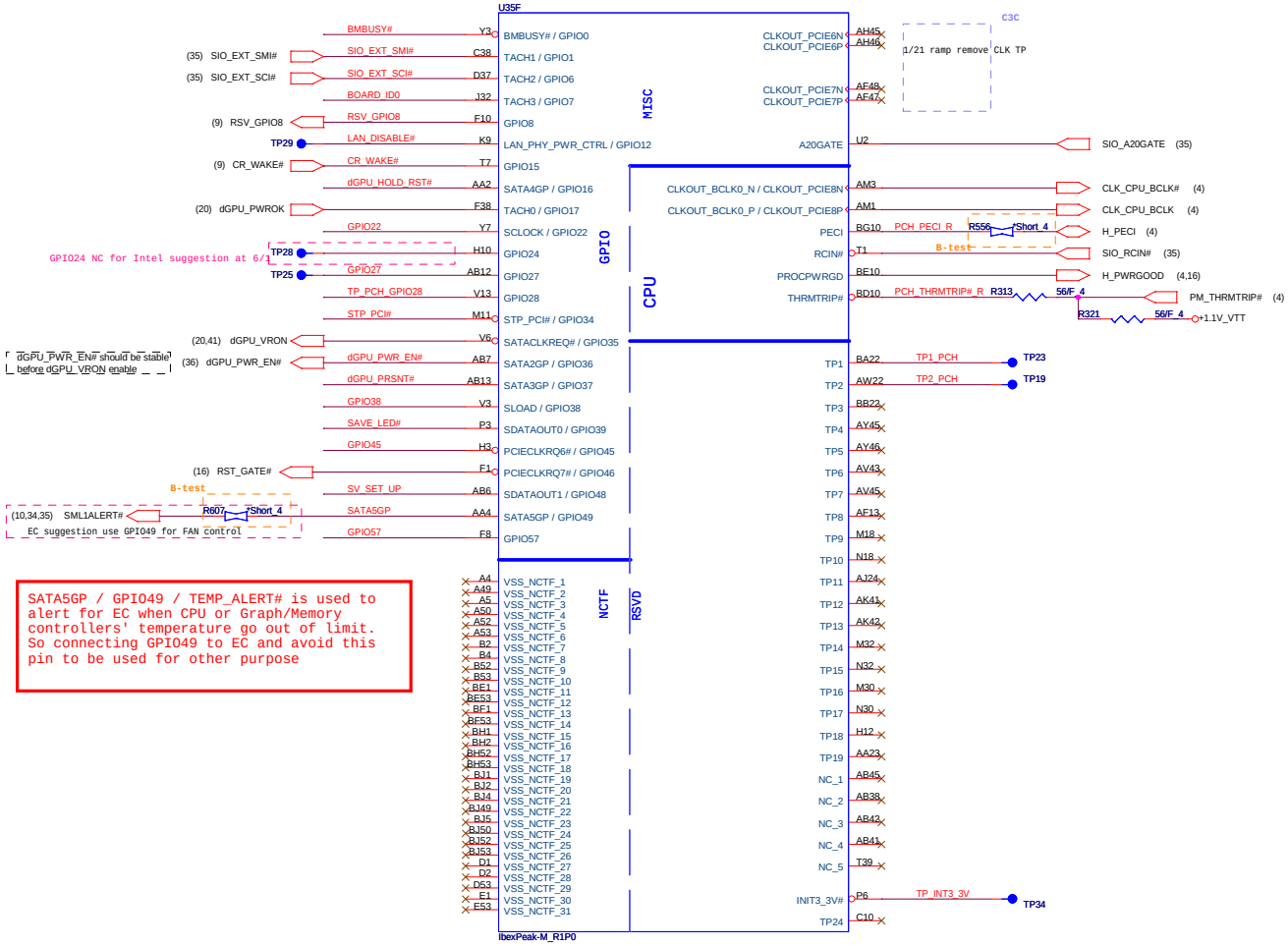
B-test
+3V_S5
R332 2.2K_4
Q18 2N7002K
SMB_CLK_ME1

B-test
+3V_S5
R328 2.2K_4
Q19 2N7002K
SMB_DATA_ME1

Quanta Computer Inc.
PROJECT : ZQ1
Rev 1A
X PEAK-M 3/6
Sheet 10 of 48
y, March 30, 2010

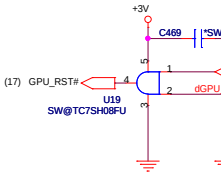
PCH4(CLG)

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

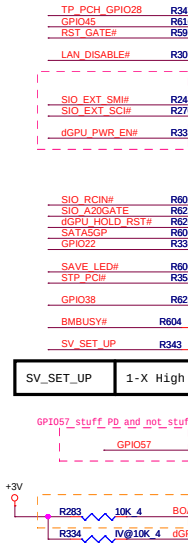


SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

GPU RST#(CLG)



GPIO Pull-up/Pull-down(



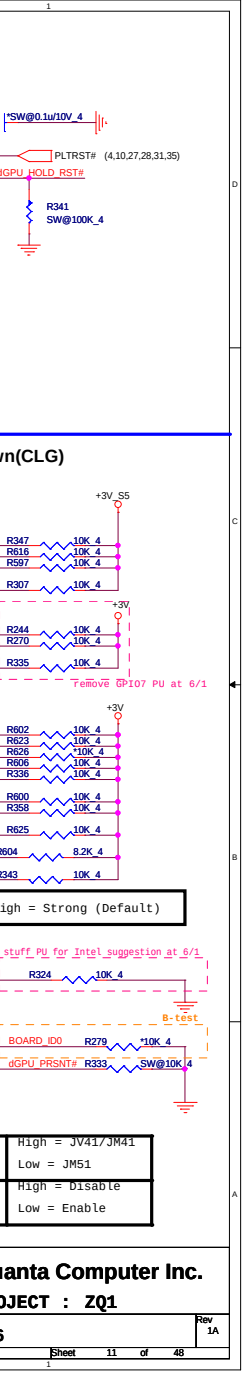
SV_SET_UP	1-X High

BOARD_ID0	H L
RSV_GPIO8	H L

Quar

PROJE

Size	Document Number
	IBEX PEAK-M 4/6
Date:	Tuesday, March 30, 2010



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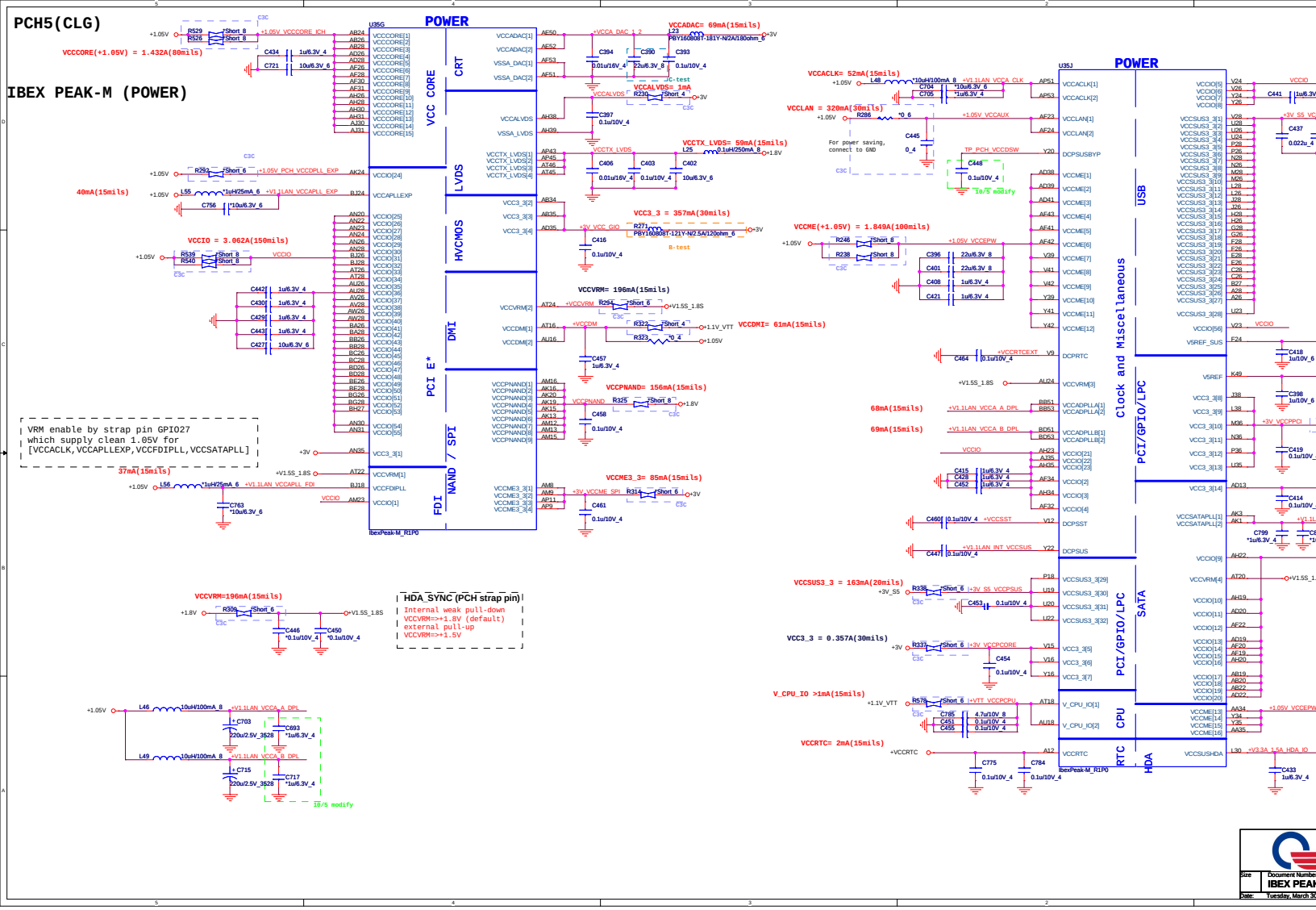
OJECT : ZQ1

6	Rev 1A

Sheet 11 of 48

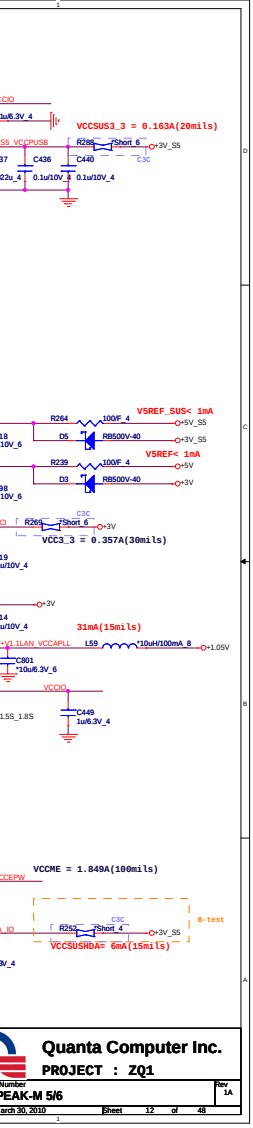
PCH5(CLG)

IBEX PEAK-M (POWER)



Size: Document Number: IBEX PEAK

Date: Tuesday, March 3



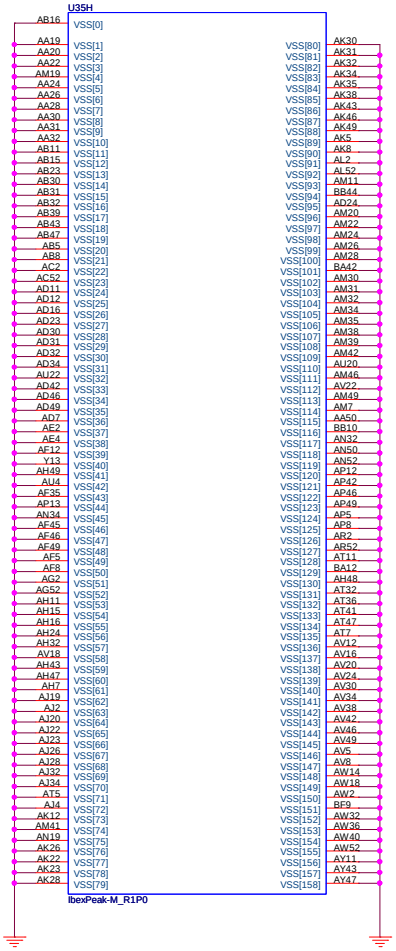
Quanta Computer Inc.

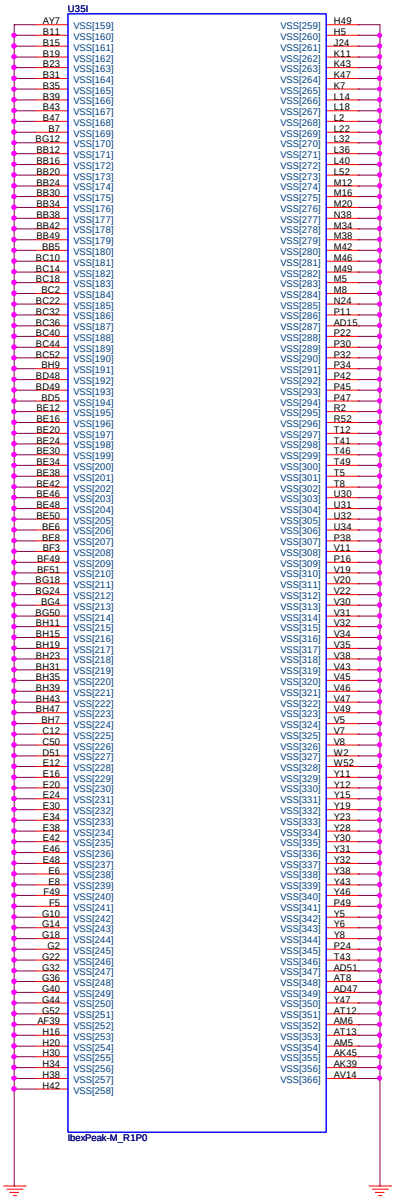
PROJECT : ZQ1

Number	Rev
PEAK-M 5/6	1A

arch 30, 2010 Sheet 12 of 48

IBEX PEAK-M (GND)





Quanta Computer Inc.

PROJECT : ZQ1

Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A

Date: Tuesday, March 30, 2010 Sheet 13 of 48

D

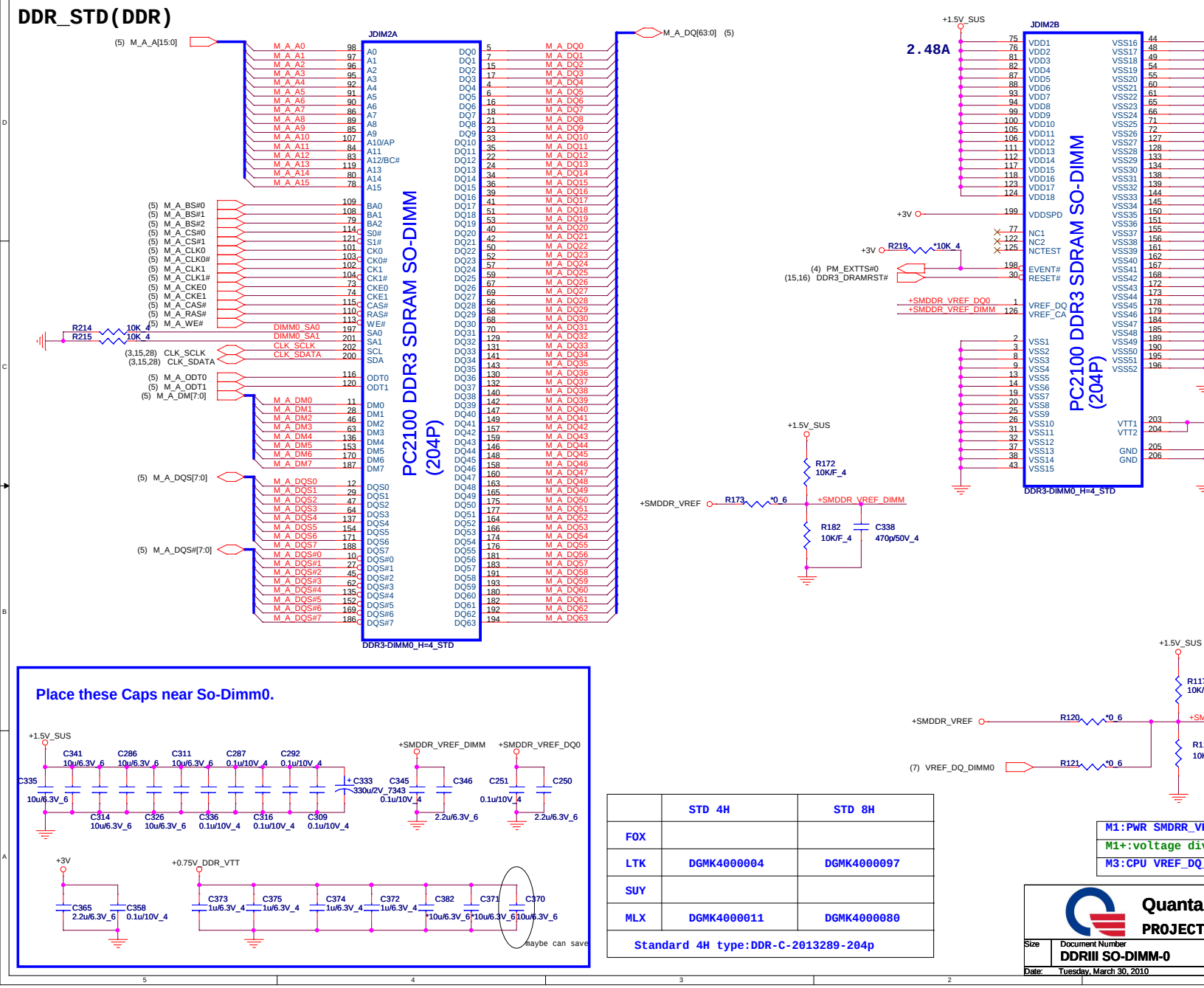
C

B

A

A

DDR_STD(DDR)



Place these Caps near So-Dimm0.

	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 4H type:DDR-C-2013289-204p

M1:PWR SMDRR_V
M1+:voltage di
M3:CPU VREF_DQ

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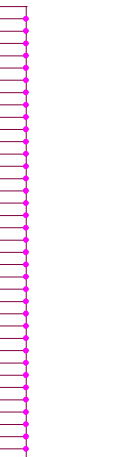
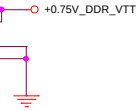
PROJECT

Size	Document Number
	DDRIII SO-DIMM-0

Date: Tuesday, March 30, 2010





+0.75V_DDR_VTT

SUS

R117
10K/F_4

+SMDDR_VREF_DQ0

R118
10K/F_4

_VREF
divider(Default)
DQ_DIMM0

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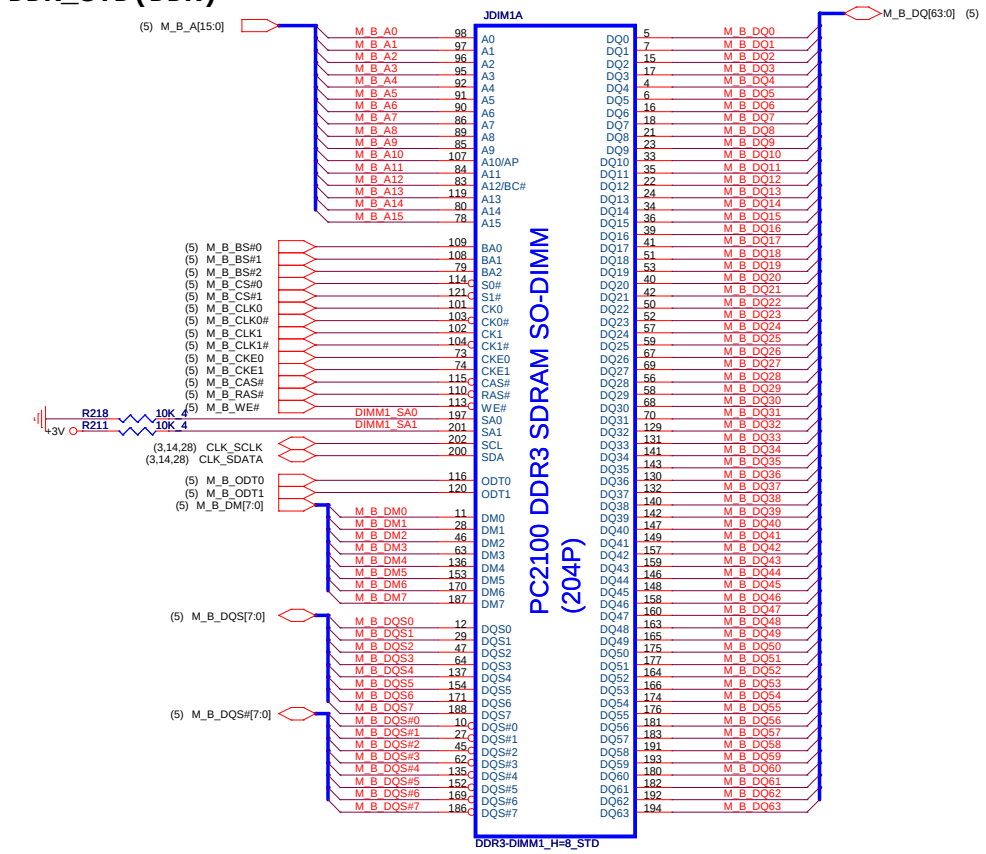
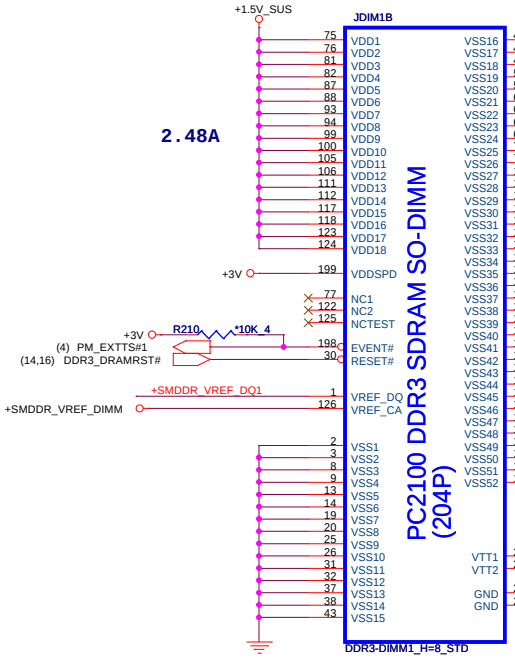
CT : ZQ1

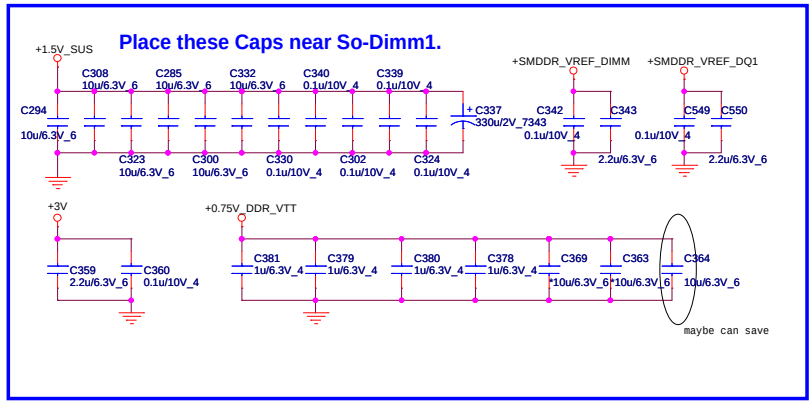
Rev
1A

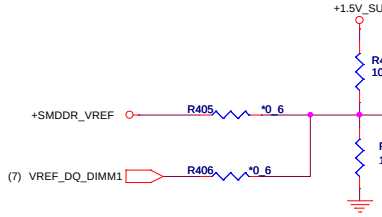
Sheet 14 of 48

DDR_STD(DDR)









	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 8H type:DDR-C-2013310-204p-1		

M1:PWR SMDRR_
M1+:voltage d
M3:CPU VREF_D

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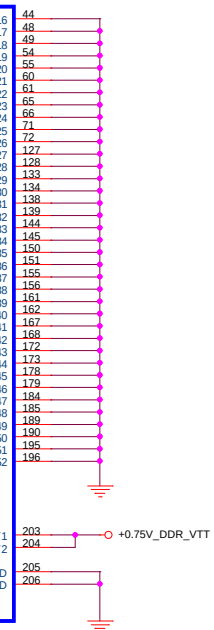
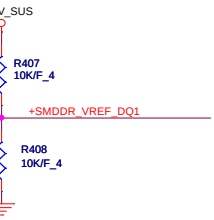
PROJECT

Size	Document Number
	DDRIII SO-DIMM-1
Date:	Tuesday, March 30, 2010





RR_VREF
e divider(Default)
F_DQ_DIMM0

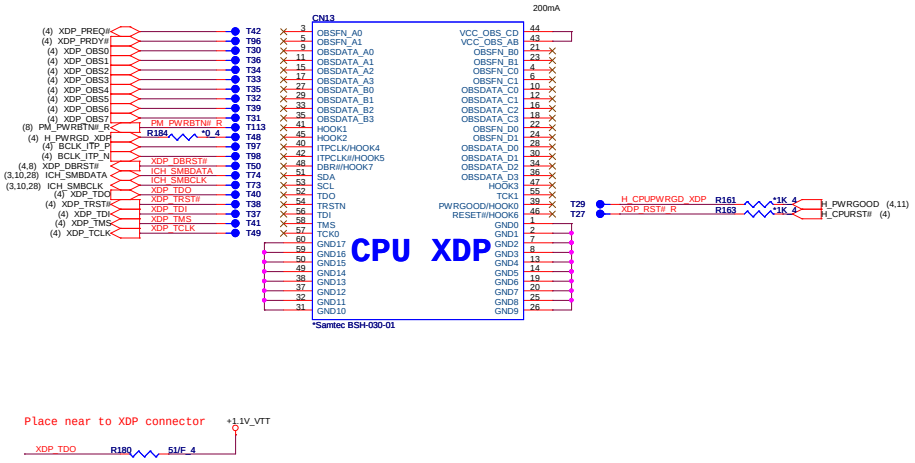
ta Computer Inc.

CT : ZQ1

Rev 1A

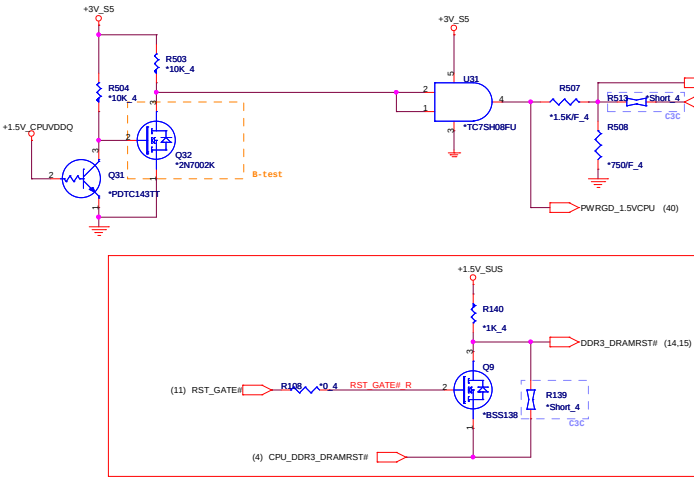
Sheet 15 of 48

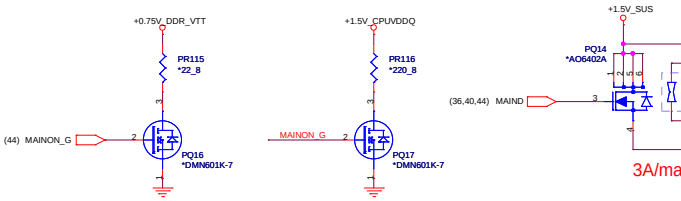
CPU XDP Connector(CPU)



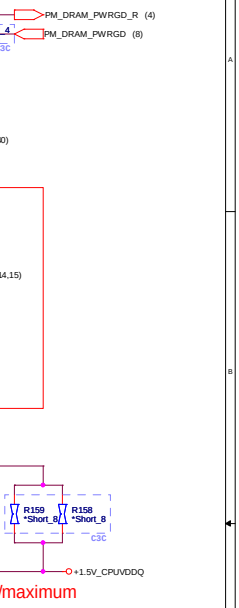
Place near to XDP connector

S3 leakage solution(CLG)





Size	Document Number
	XDP
Date: Tuesday, March 30, 2010	



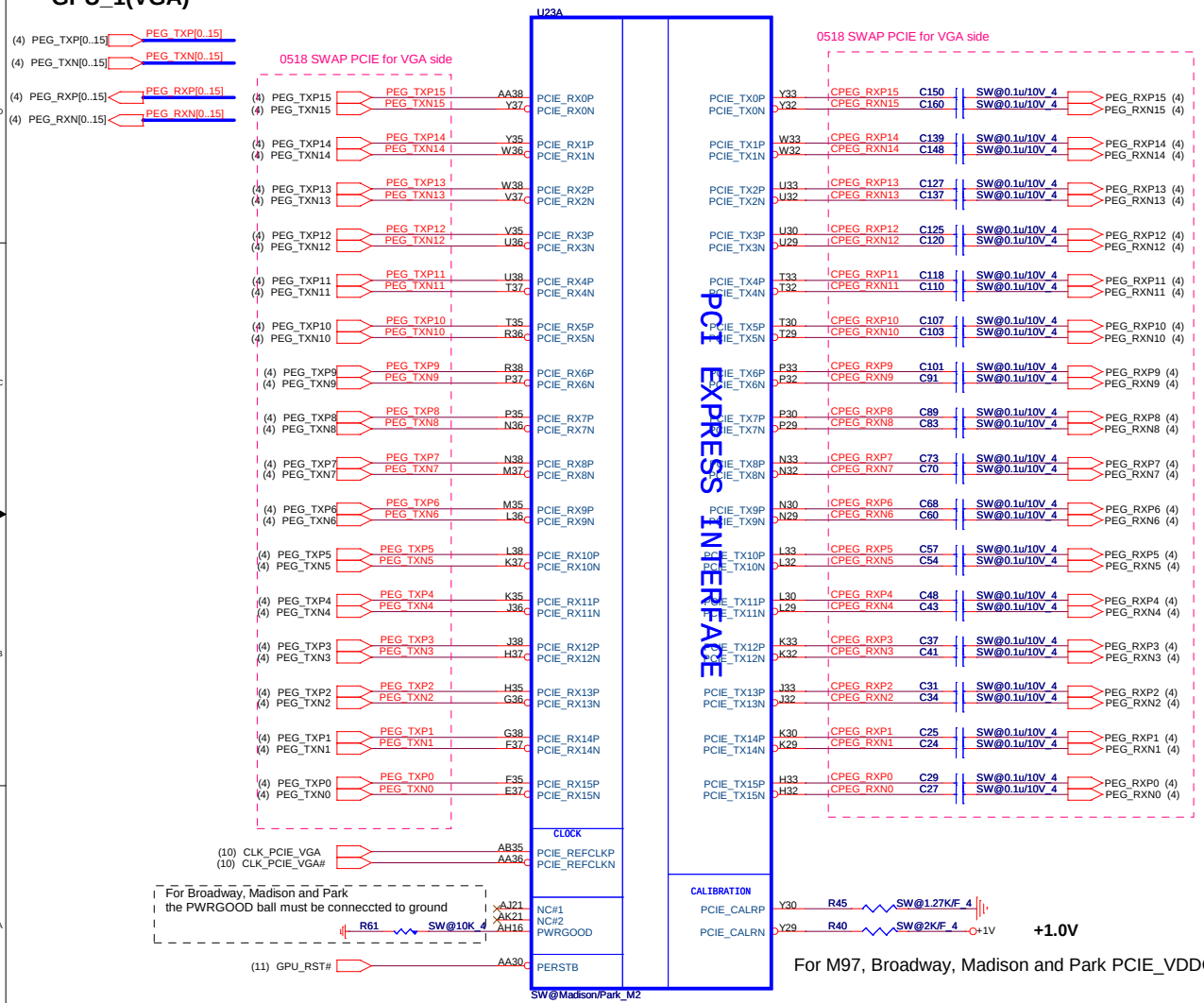
Quanta Computer Inc.

PROJECT : ZQ1

Rev 1A

010 Sheet 16 of 48

GPU_1(VGA)



For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

Madison
Park

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PROJECT

Size	Document Number
	Madison/Park M2-PCIE
Date:	Tuesday, March 30, 2010

n	AJ007720T02
	AJ077400T08

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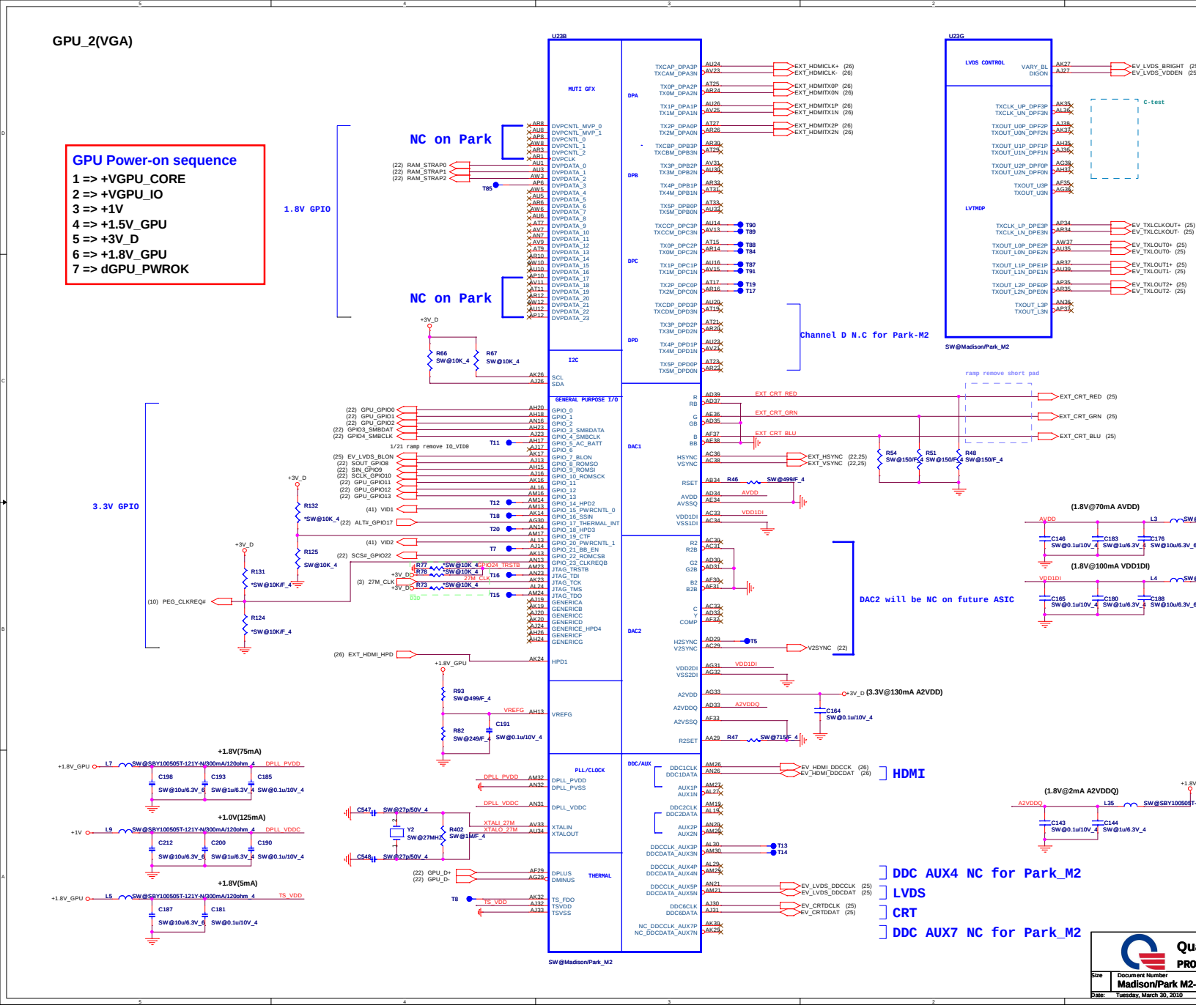
CT : ZQ1

IE I/F

Rev 1A

Sheet 17 of 48

GPU_2(VGA)


GPU Power-on sequence
1 => +VGPU_CORE
2 => +VGPU_IO
3 => +1V
4 => +1.5V_GPU
5 => +3V_D
6 => +1.8V_GPU
7 => dGPU_PWROK
1.8V GPIO
3.3V GPIO
NC on Park
NC on Park
U23B
MUTI GFX
DPA
DPB
DPC
DPD
I2C
GENERAL PURPOSE I/O
DAC1
DAC2
DDC/AUX
PLL/CLOCK
THERMAL
SW@Madison/Park_M2
U23G
LVDS CONTROL
LVTMDP
C-test
SW@Madison/Park_M2
Channel D N.C for Park-M2
ramp remove short pad
DAC2 will be NC on future ASIC
HDMI
DDC AUX4 NC for Park_M2
LVDS
CRT
DDC AUX7 NC for Park_M2
(1.8V@70mA AVDD)
(1.8V@100mA VDD1DI)
(1.8V@2mA A2VDDQ)
(3.3V@130mA A2VDD)
+1.8V(75mA)
+1.0V(125mA)
+1.8V(5mA)
Size
Document Number
Madison/Park M2-
Date:
Tuesday, March 30, 2010

HT (25)
N (25)

(25)
(25)

25)
25)

25)
25)

25)
25)

+1.8V_GPU

SW@SBY100505T-121Y-N/300mA/120ohm_4

6.3V_6

SW@SBY100505T-121Y-N/300mA/120ohm_4

6.3V_6

+1.8V_GPU

0505T-121Y-N/300mA/120ohm_4

Quanta Computer Inc.

PROJECT : ZQ1

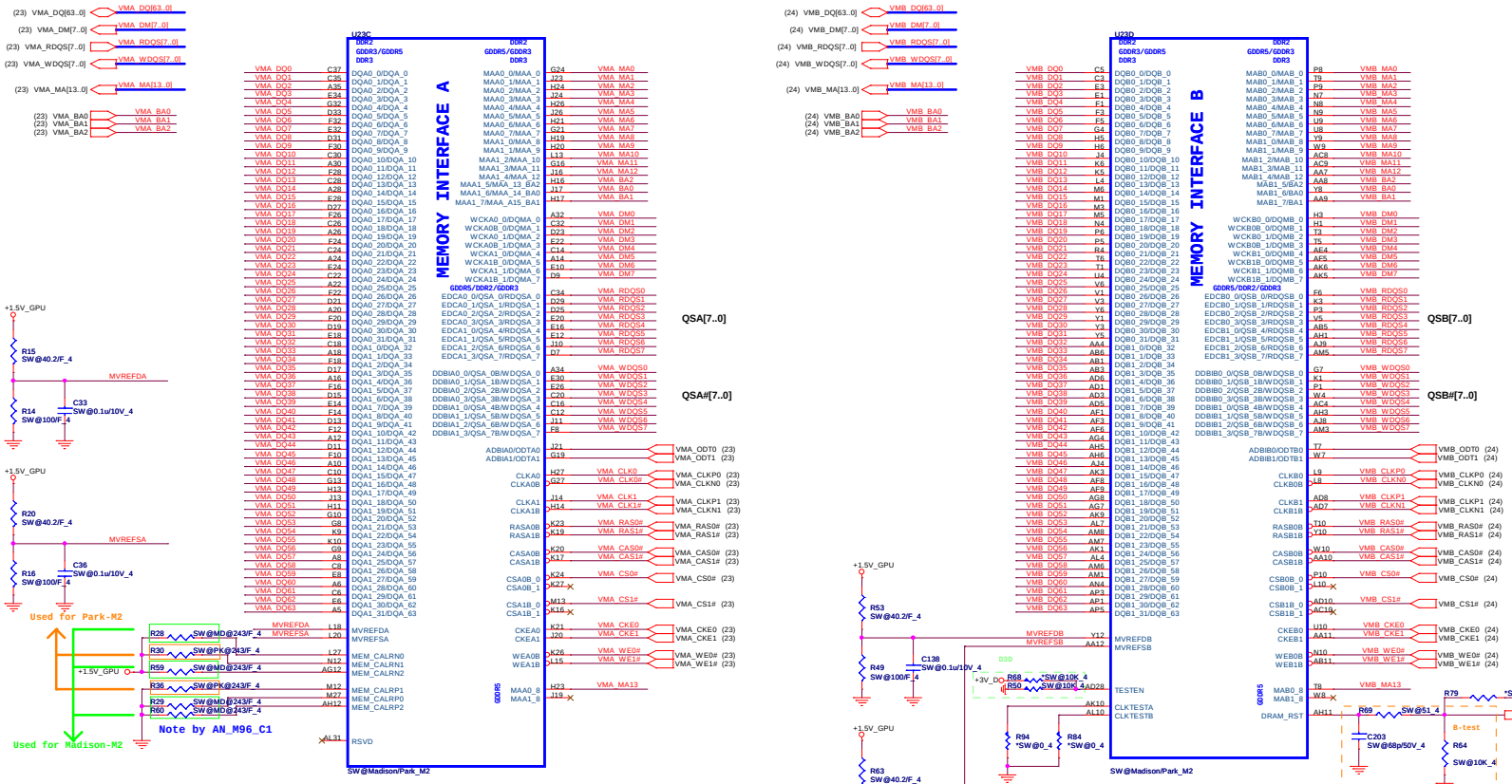
M2-HOST I/F

Rev
1A

D Sheet 18 of 48

GPU_3(VGA)

Park M2-channel B used(S3 package use Channel A



Size	Document Number	Rev
	Madison/Park M2-	
Date:	Tuesday, March 30, 2010	

l A)

24)
24)

(24)
(24)

(24)
(24)

(24)
(24)

(24)
(24)

24)

24)

24)
24)

24)
24)

*SW@4.7K_4 +1.5V_GPU

MEM_RST# (23,24)

4

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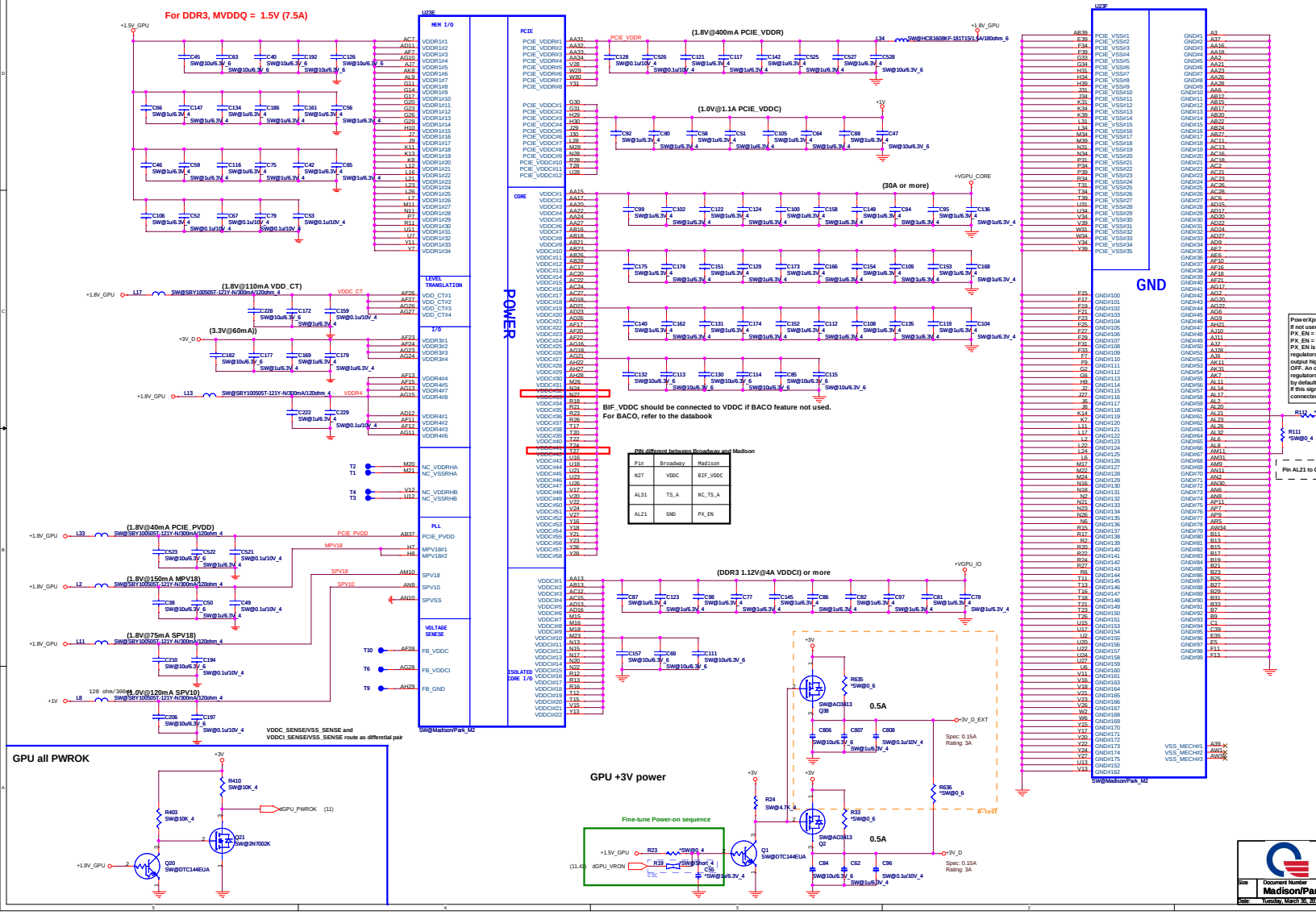
PROJECT : ZQ1

M2-MEM I/F

Rev 1A

D Sheet 19 of 48

GPU_4(VGA)


For DDR3, MVDDQ = 1.5V (7.5A)
U23E
MEM I/O
PCIE
LEVEL TRANSLATION
I/O
POWER
PLL
VOLTAGE SENSE
SW@Madison/Park_M2
(1.8V@400mA PCIE_VDDR)
(1.0V@1.1A PCIE_VDDC)
(30A or more)
(1.8V@110mA VDD_CT)
(3.3V@60mA))
(1.8V@40mA PCIE_PVDD)
(1.8V@150mA MPV18)
(1.8V@75mA SPV18)
(1.0V@120mA SPV10)
(DDR3 1.12V@4A VDDCI) or more
BIF_VDDC should be connected to VDDC if BACO feature not used.
For BACO, refer to the databook
PIN different between Broadway and Madison
Pin | Broadway | Madison
N27 | VDDC | BIF_VDDC
AL31 | TS_A | NC_TS_A
AL21 | GND | PX_EN
VDDC_SENSE/VSS_SENSE and
VDDCI_SENSE/VSS_SENSE route as differetial pair
GND
PowerXpr
If not usin
PX_EN =
PX_EN =
PX_EN is
regulators
output hig
OFF. An o
regulators
by default
If this sign
connection
Pin AL21 to G
GPU all PWROK
GPU +3V power
Fine-tune Power-on sequence
0.5A
Spec: 0.15A
Rating: 3A
Size
Document Number
Madison/Par
Date: Tuesday, March 30, 20

werXpress control signal for Madsion and Park only
not used, can be disconnected.
_EN = LOW, turn on
_EN = HIGH, turn off
_EN is used to turn ON/OFF some
gulators for PowerXpress mode. An
tput high "3.3V" will turn the regulators
FF. An output low "0V" will turn the
gulators ON. PX_EN outputs low (0V)
default.
this signal is unused, it can be NC (not
nnected) or connected to ground.

R12 _SW@0_4 +3V_D

1
W@0_4

L21 to Ground for Broadway

Quanta Computer Inc.

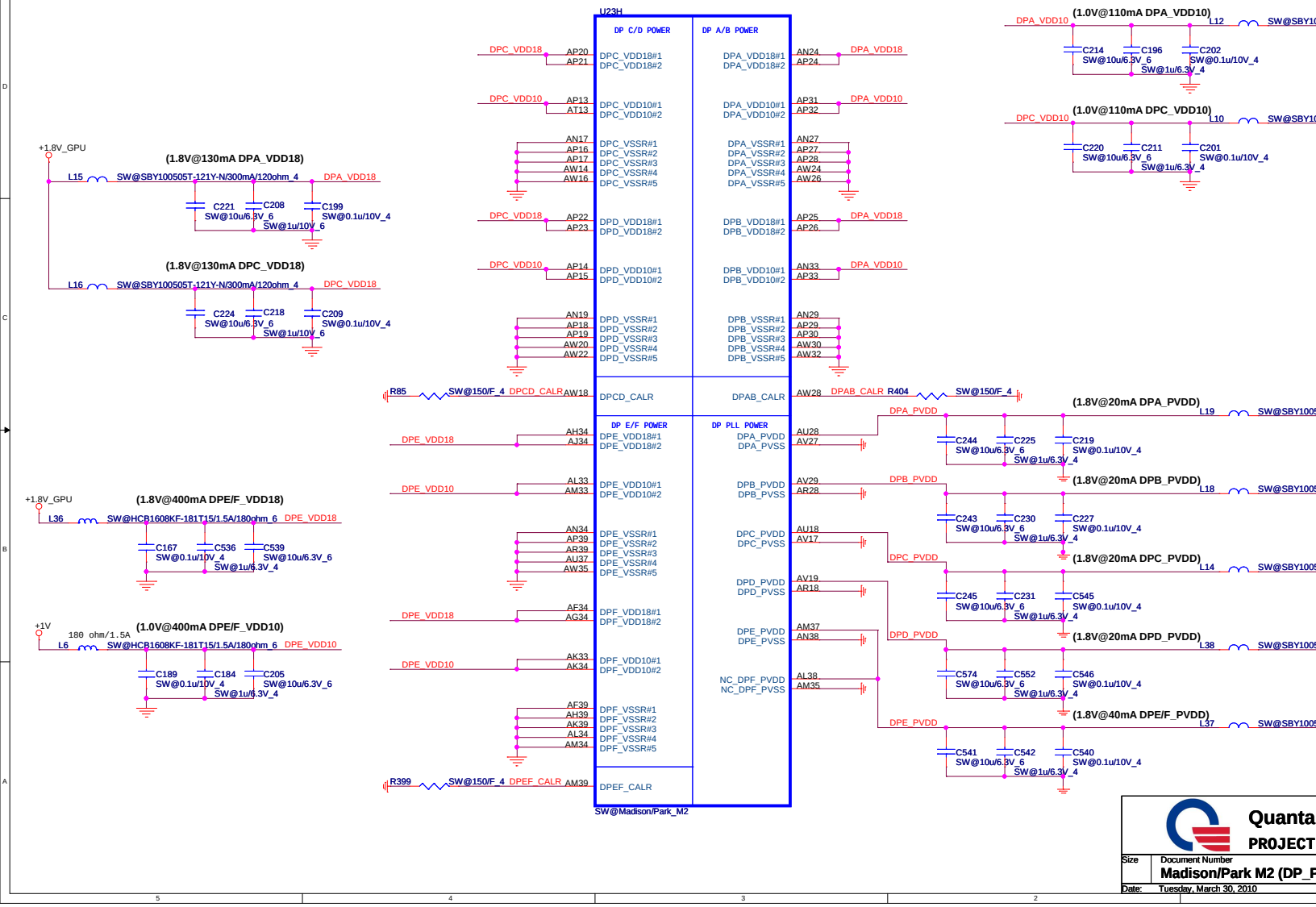
PROJECT : ZQ1

mber
n/Park M2 (PWR/GND)

Rev
1A

s 30, 2030 Sheet 20 of 48

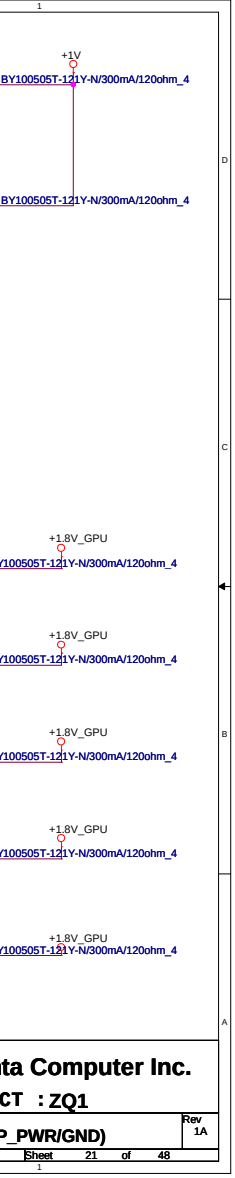
GPU_5(VGA)



Quanta

PROJECT

Size	Document Number
	Madison/Park M2 (DP_F
Date:	Tuesday, March 30, 2010



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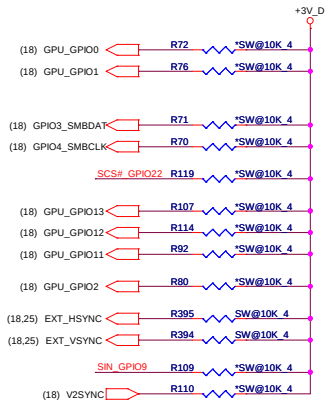
CT : ZQ1

P_PWR/GND)

Rev 1A

Sheet 21 of 48

PIN STRAPS(VGA)



ROM Table		
Manufacturer	Part Number	Code
Numonyx ST Microelectronics	M25P05A	100
	M25P10A	101
	M25P20	101
	M25P40	101
	M25P80	101
Chingis PMC	Pm25LV512A	100
	Pm25LV010A	101

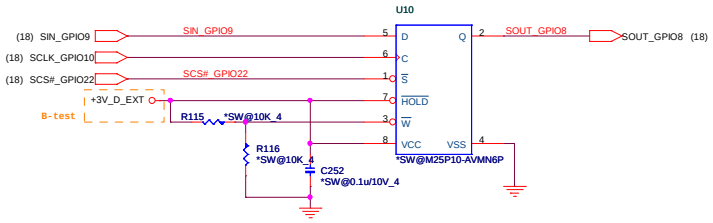
ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.

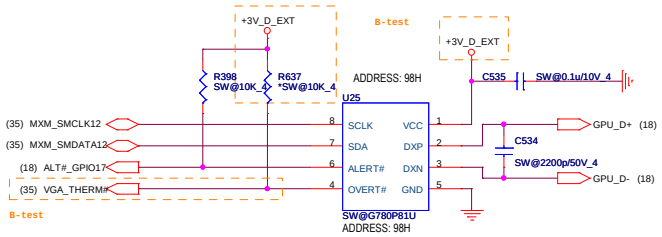
EEPROM(VGA)



Thermal Sensor(VGA)

Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

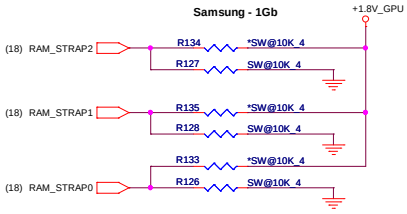
USD0.16



DDR3 Memory Aperture size(GPU)

DDR3 Memory Aperture size					
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_ST DVPDA
Hynix			512Mb	1	1
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1Gb	1	0
			2Gb	1	0
Samsung			512Mb		
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1Gb	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2Gb	0	0
AMD	23EY2387MA12-SZ	AKD5LGGT700	1Gb	0	1

C-test



RAM_STRAP2 SET
RAM_STRAP[1:0]

Qua
PROJ

Size	Document Number
	Strip/Thermal
Date:	Tuesday, March 30, 2010

DEFAULT	REMARK
0	
0	
1	
101	See ROM table
0	
0	
11	See Audio table
0	
0	

D

C

e

M_STRAP1 PDATA_1	RAM_STRAP0 DVPDATA_0
1	0
0	0
0	1
0	0
0	1
1	0

B

A

ET DDR3 Vendor
0] SET SIZE.

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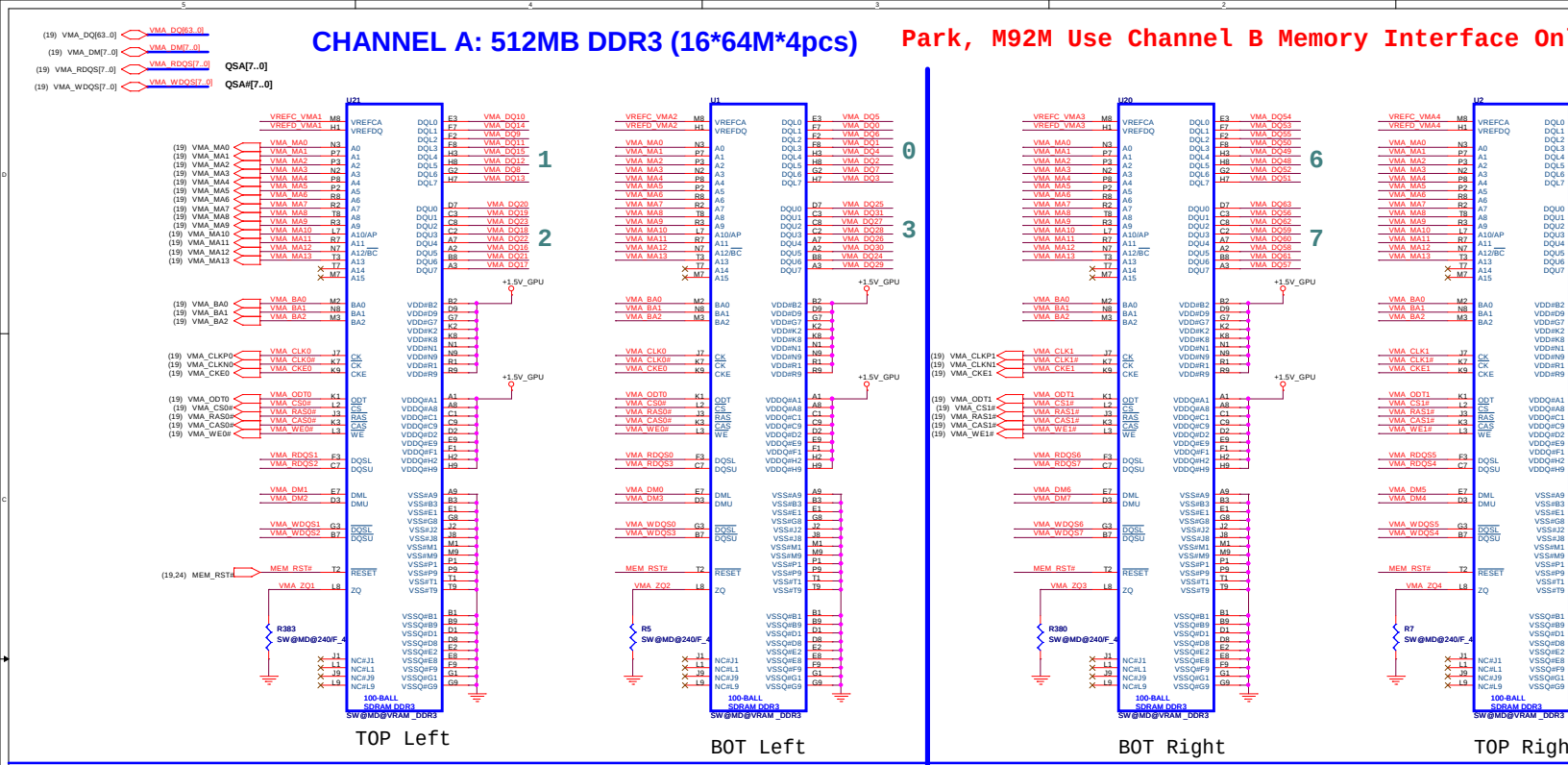
ROJECT : ZQ1

Rev
1A

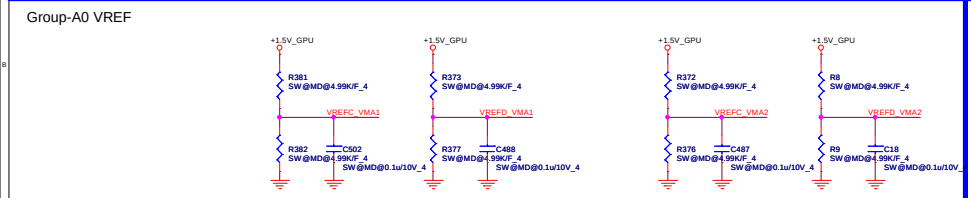
Sheet 22 of 48

CHANNEL A: 512MB DDR3 (16*64M*4pcs)

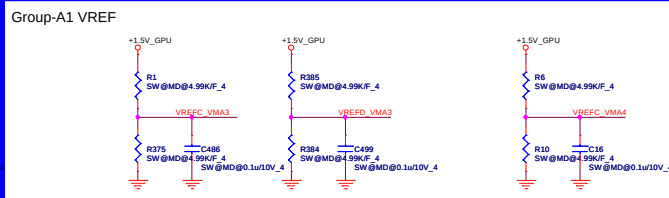
Park, M92M Use Channel B Memory Interface On



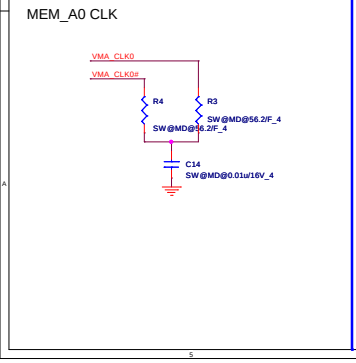
Group-A0 VREF



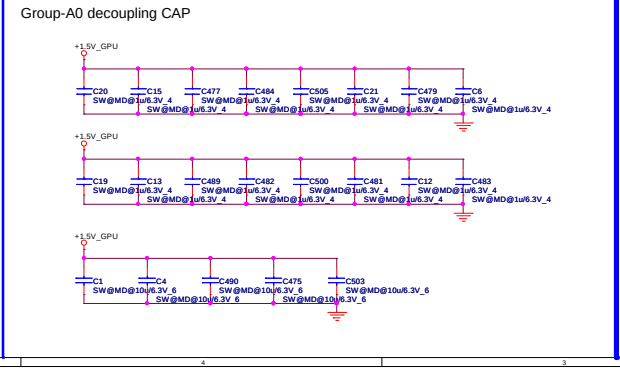
Group-A1 VREF



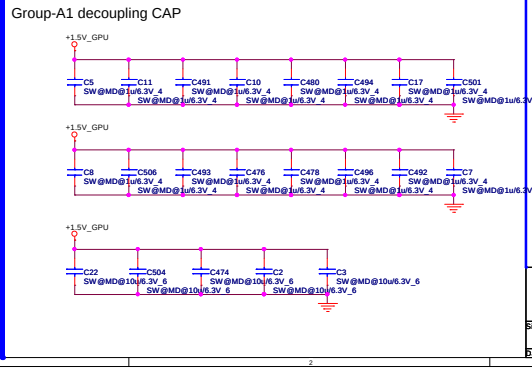
MEM_A0 CLK



Group-A0 decoupling CAP



Group-A1 decoupling CAP

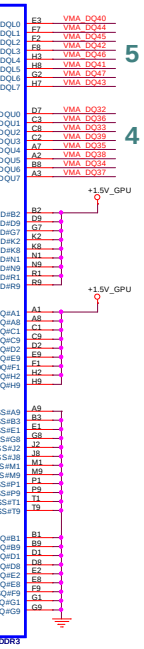


MEM_A1 CLK

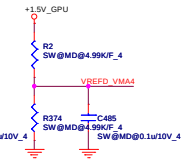
Size	Document Number	
		MEM

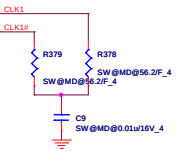
Date: Tuesday, March 30, 2010

Only



ght



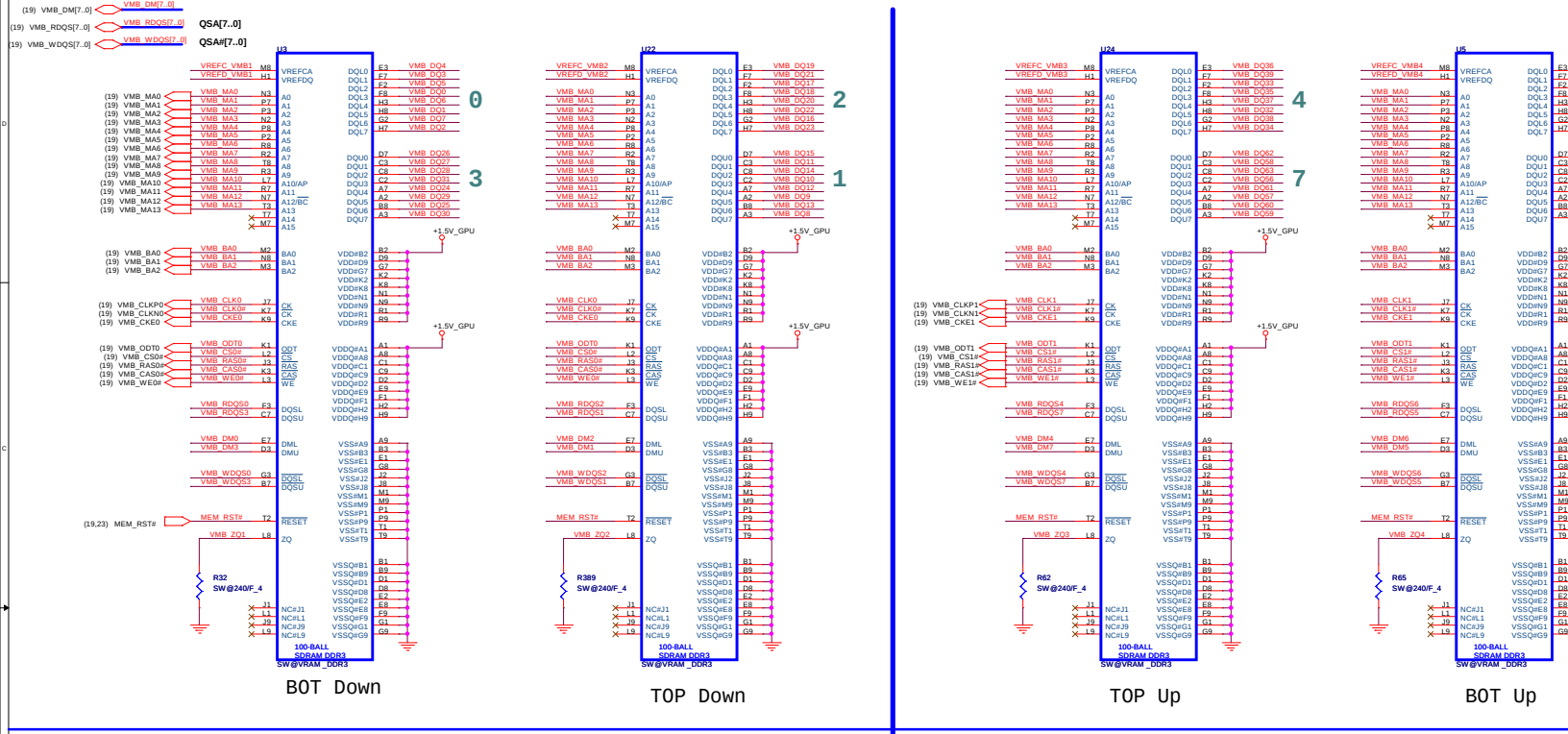


Quanta Computer Inc.

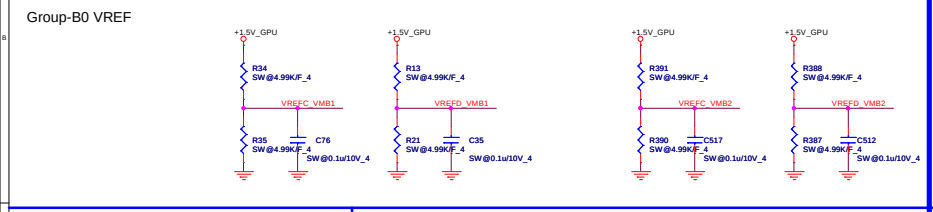
PROJECT : ZQ1

MEMORY 1 channel A	Rev 1A
D	Sheet 23 of 48

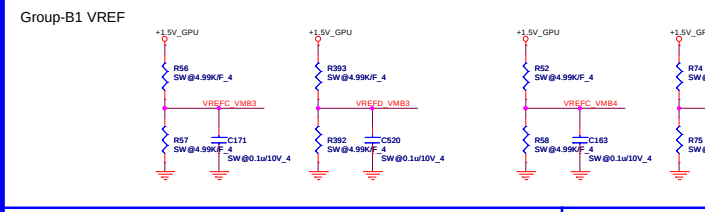
CHANNEL B: 512MB DDR3 (16*64M*4pcs)



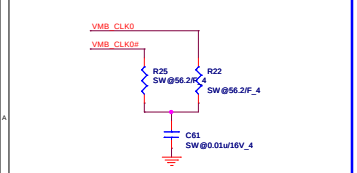
Group-B0 VREF



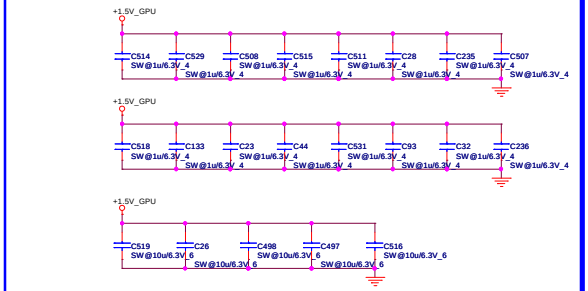
Group-B1 VREF



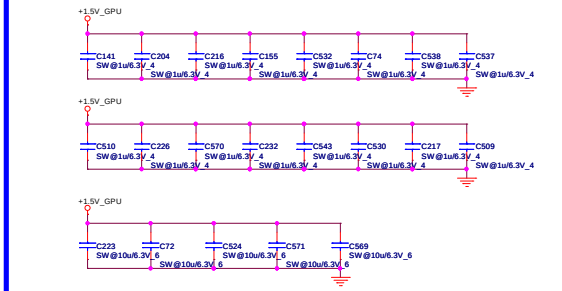
MEM_B0 CLK



Group-B0 decoupling CAP



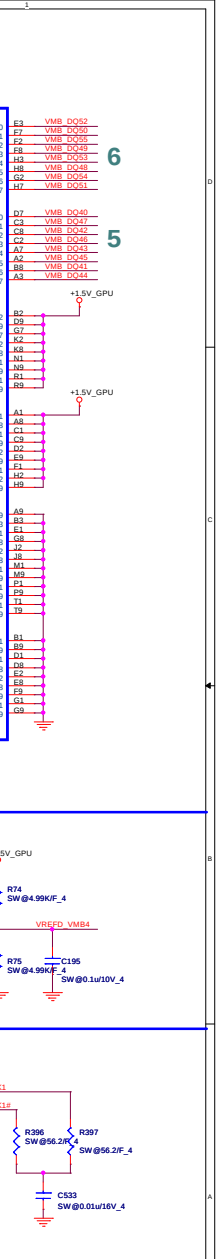
Group-B1 decoupling CAP



MEM_B1 CLK

Size	Document Number	
		MEM

Date: Tuesday, March 30, 2010

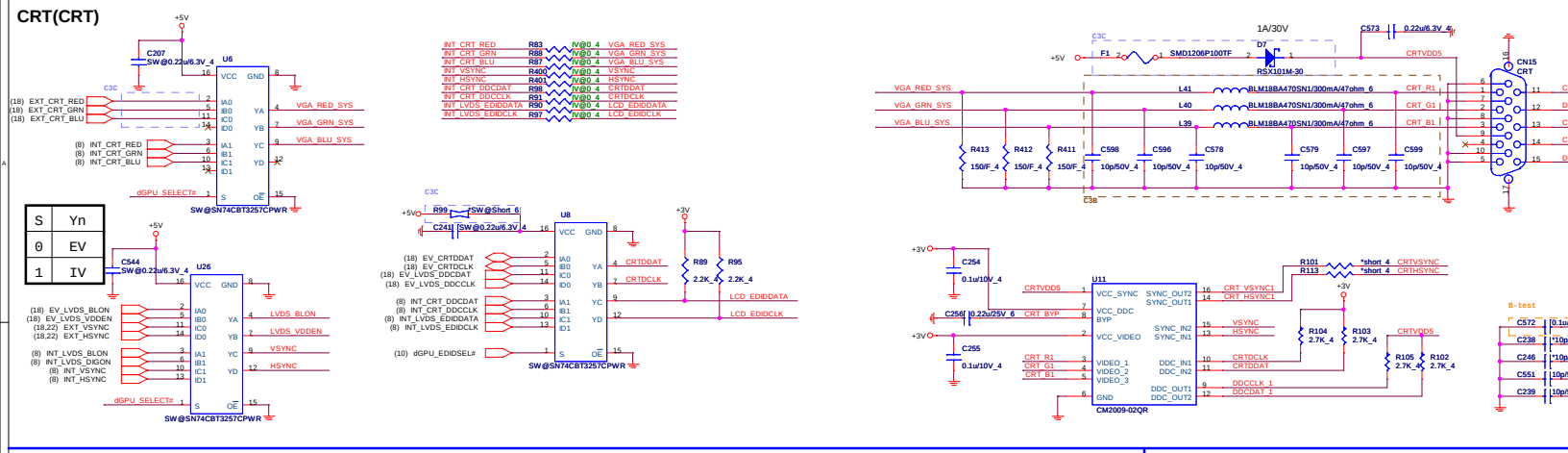


Quanta Computer Inc.

PROJECT : ZQ1

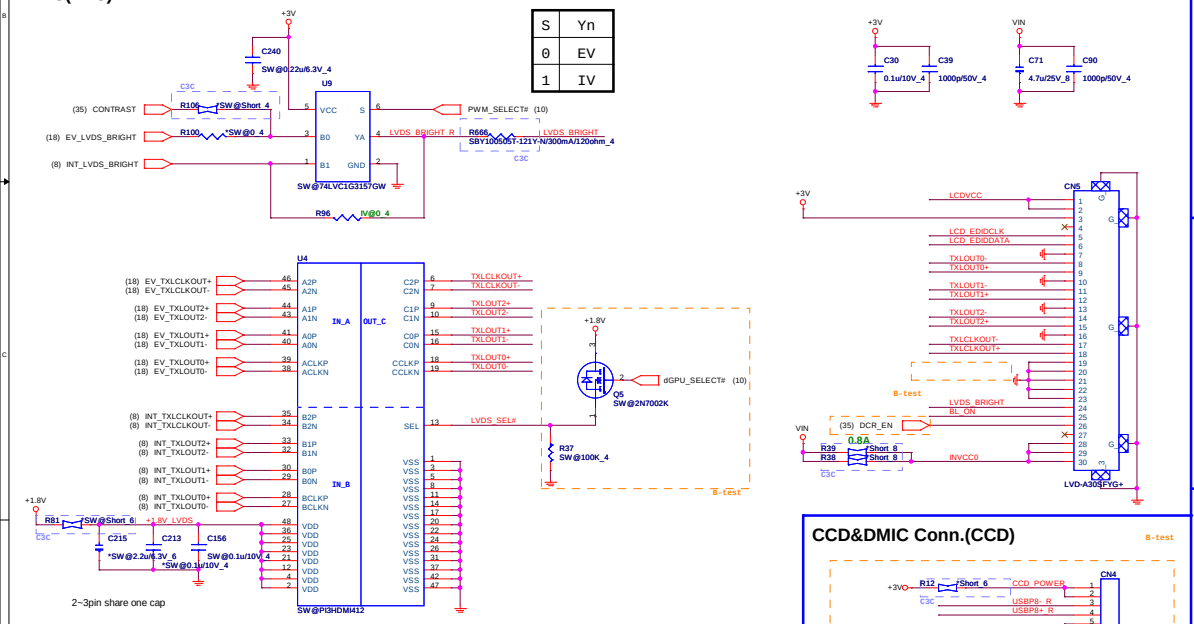
MEMORY 2 channel B | Rev 1A

CRT(CRT)



S	Yn
0	EV
1	IV

LVDS(LDS)

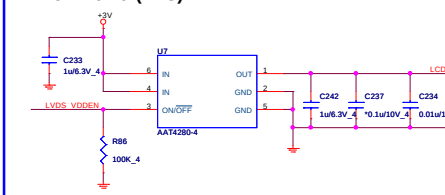


S	Yn
0	EV
1	IV

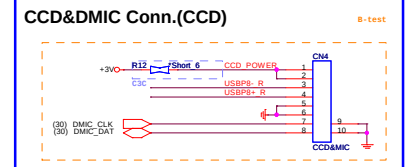
TI	AL3DV421V00
Pericom	AL000412W00

dGPU_SELECT#	Output
L	EV_LVDS
H	INT_LVDS

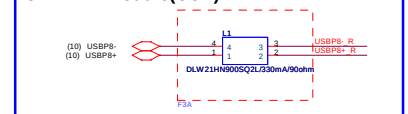
LCD Power(LDS)



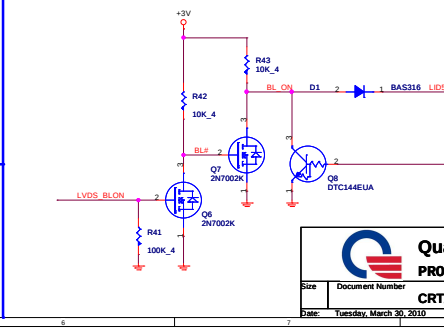
CCD&DMIC Conn.(CCD)



CAMERA Module(CCD)

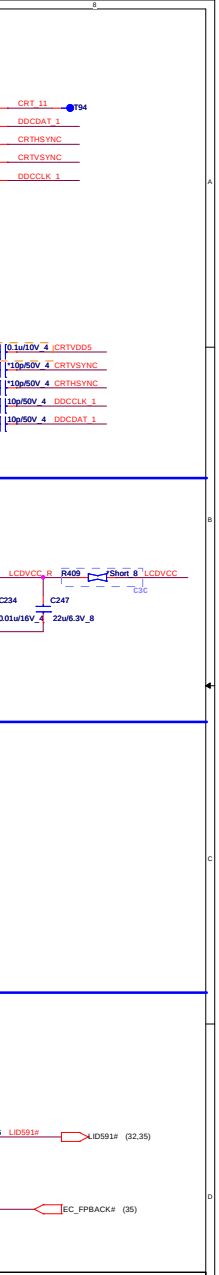


Backlight Control(LDS)



Size	Document Number	
		CRT

Date: Tuesday, March 30, 2010



Quanta Computer Inc.

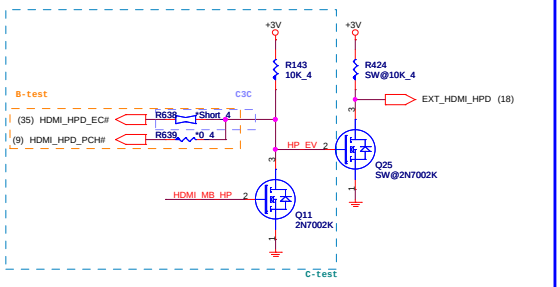
PROJECT : ZQ1

CRT/LVDS

Rev 1A

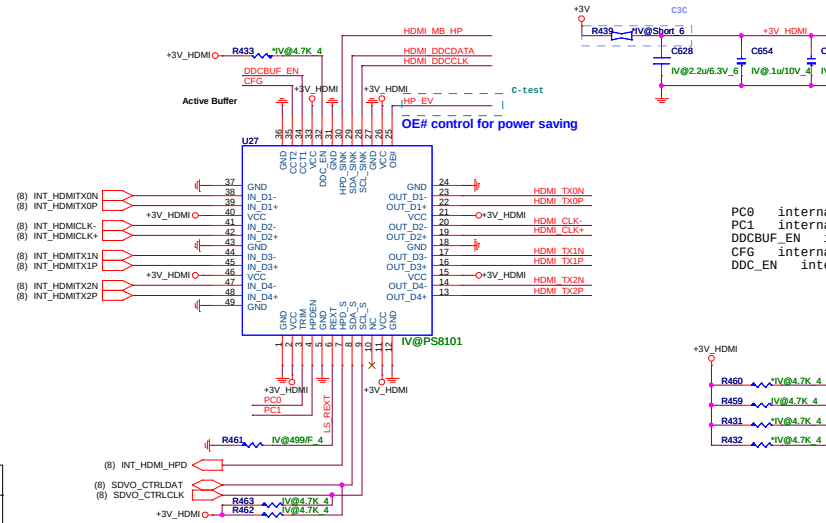
Sheet 25 of 48

HDMI HPD(HDM)



HDMI LEVEL SHIFTER(HDM)

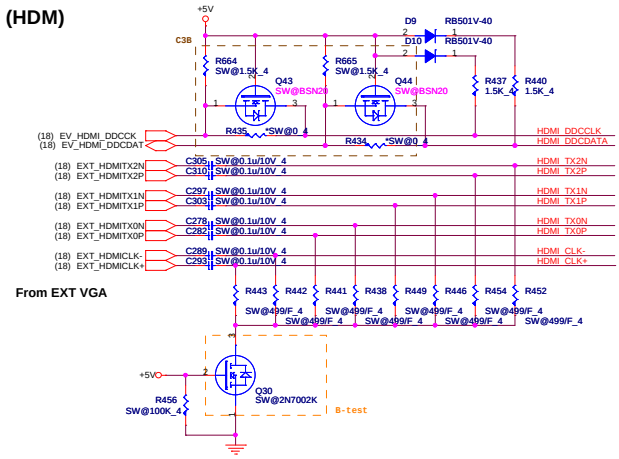
PS8101 :: AL008101000



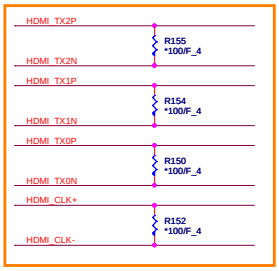
PC0 interna
PC1 interna
DDCBUF_EN
CFG interna
DDC_EN inte

Equalization Control		
PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

(HDM)

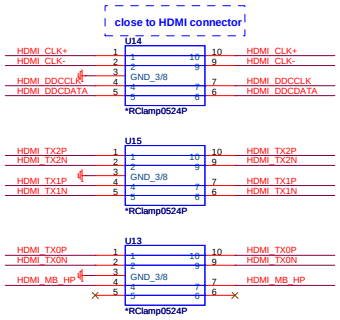


EMI reserve for HDMI(HDM)

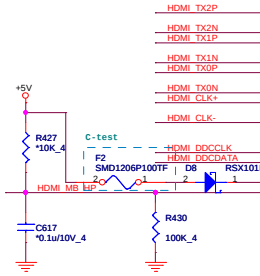


Close connector

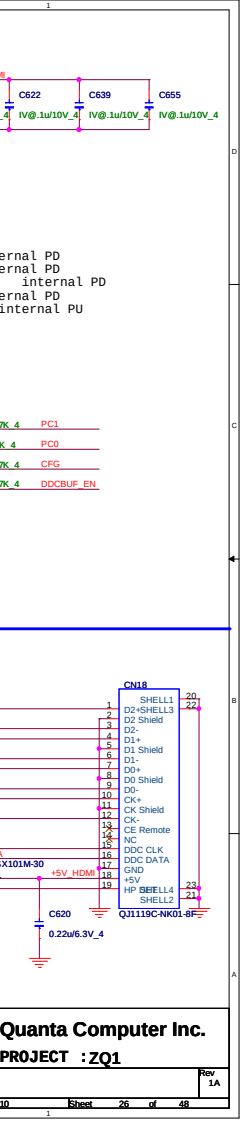
ESD Protect



HDMI connector(HDM)



Size	Document Number
	HDMI
Date:	Tuesday, March 30, 2010



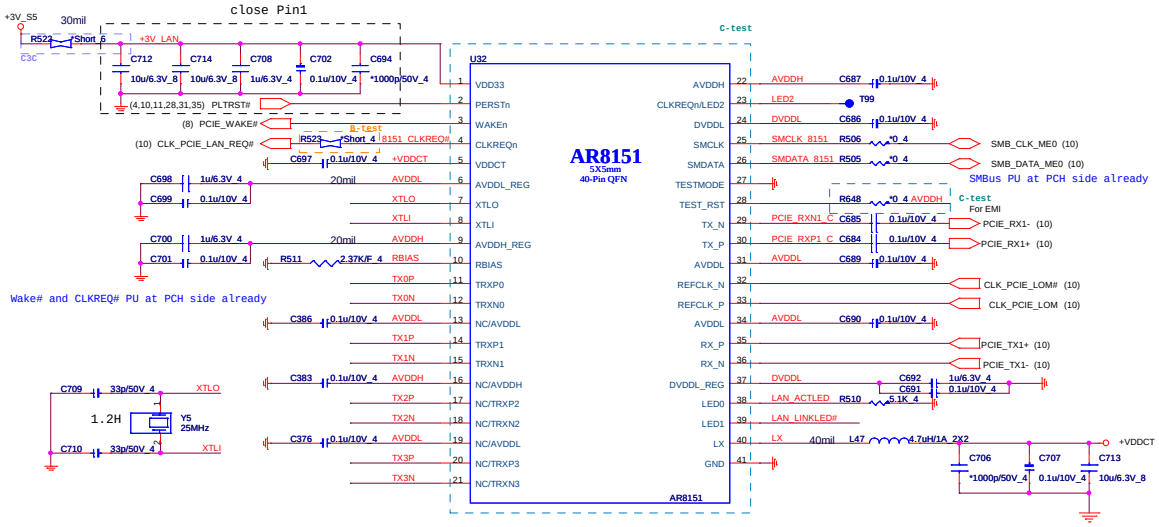
Quanta Computer Inc.

PROJECT : ZQ1

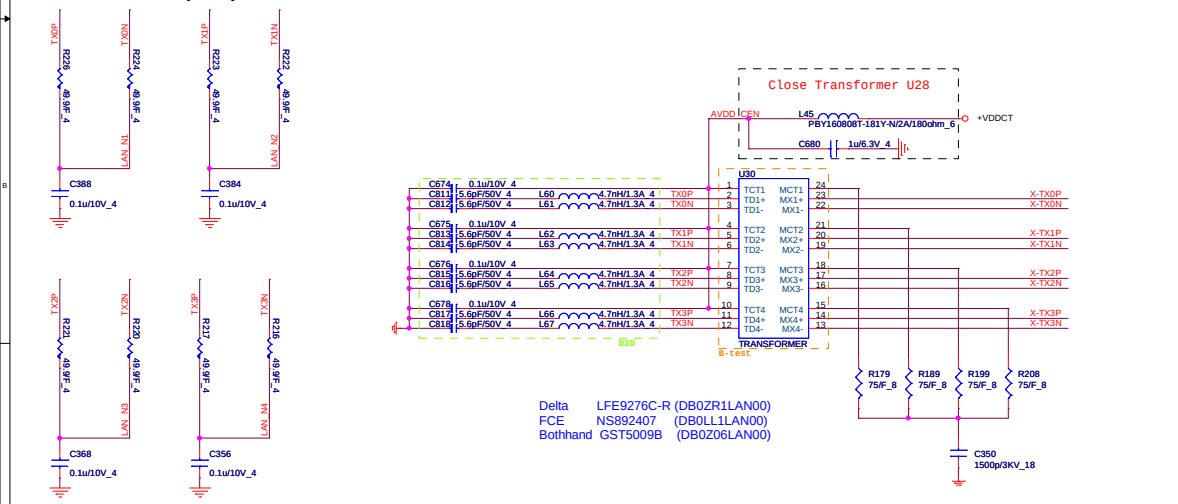
Rev 1A

10 Sheet 26 of 48

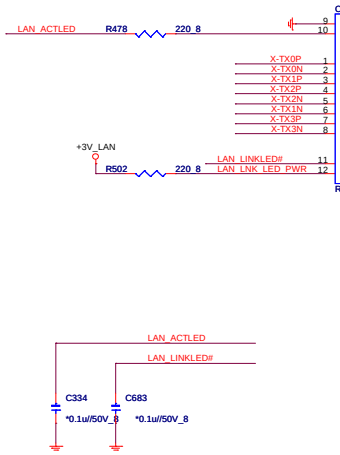
Giga-LAN AR8151(LAN)



TRANSFORMER(LAN)

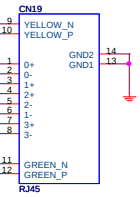


RJ45(LAN)



Size	Document Number	
		Qu PRO LAN

Date: Tuesday, March 30, 2010



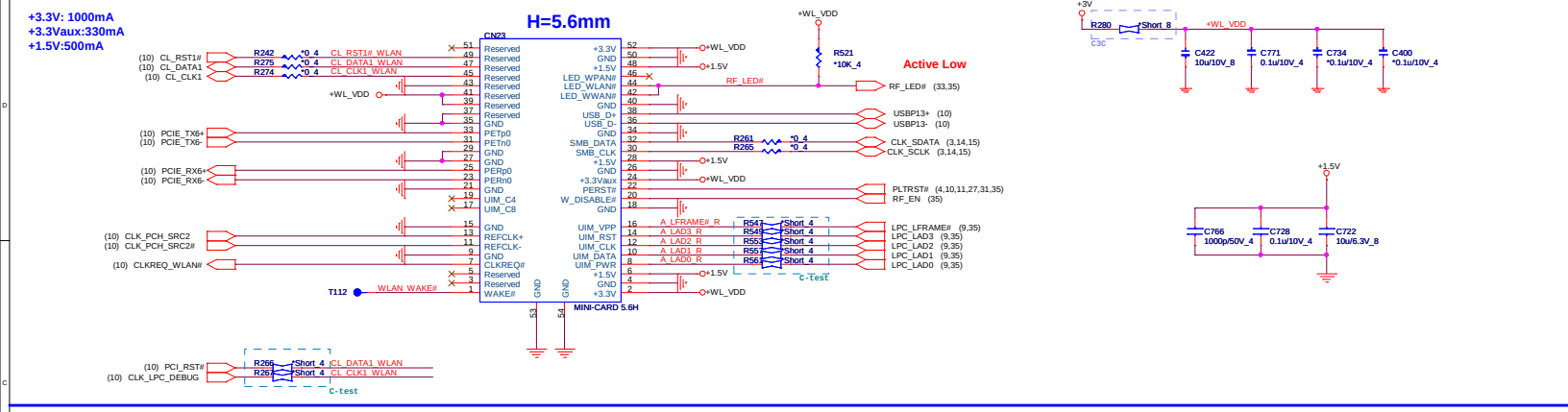
Quanta Computer Inc.

PROJECT : ZQ1

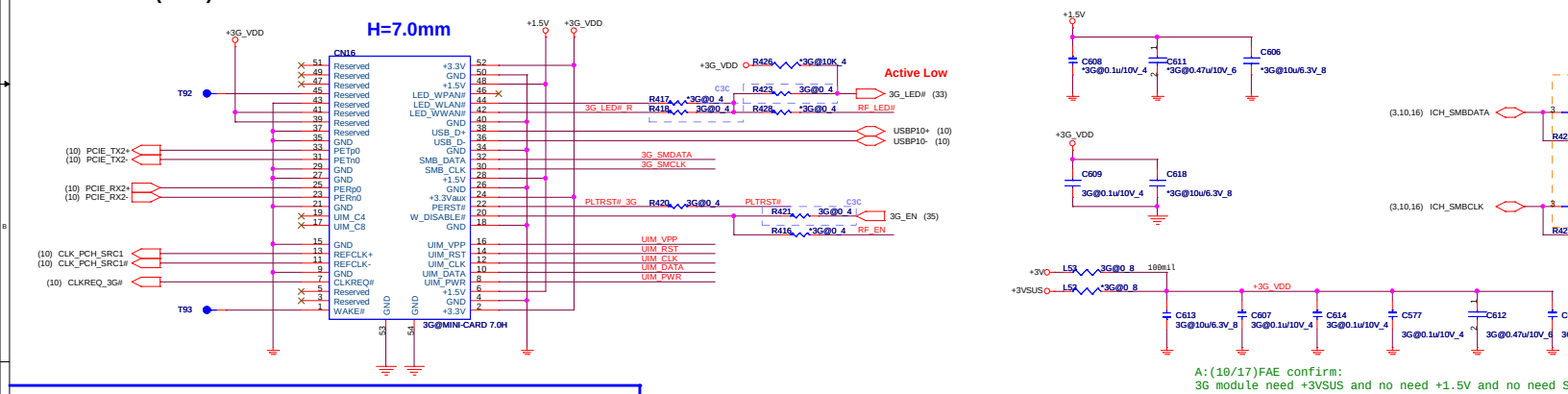
LAN (AR8151) Rev 1A

10 Sheet 27 of 48

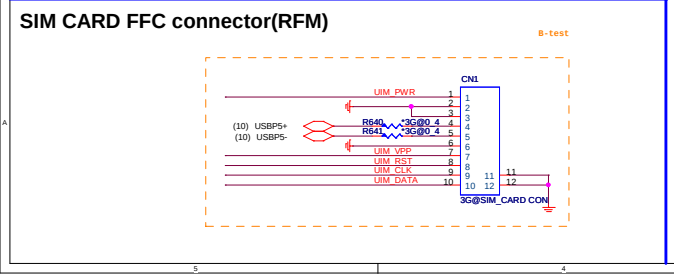
MINI-CARD WLAN(MPC)



MINI-CARD 3G(MNC)Reserve for JV41-CP

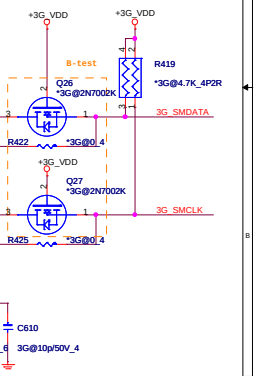


SIM CARD FFC connector(RFM)



A:(10/17)FAE confirm:
3G module need +3VSUS and no need +1.5V and no need S

Size	Document Number
	Mini-Card/WL/
Date:	Tuesday, March 30, 2010

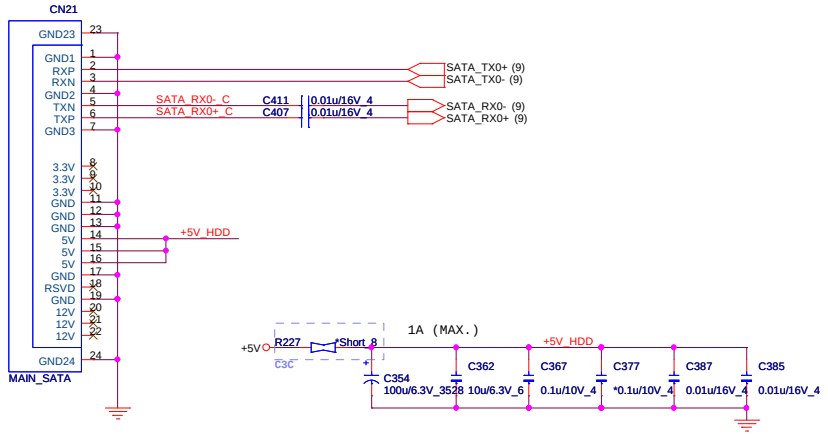


Quanta Computer Inc.

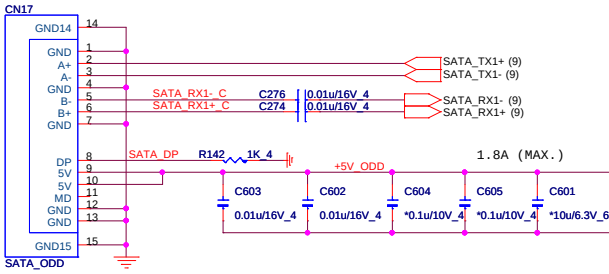
PROJECT : ZQ1

r	WL/3G/SIM	Rev 1A
0, 2010	Sheet 28 of 48	

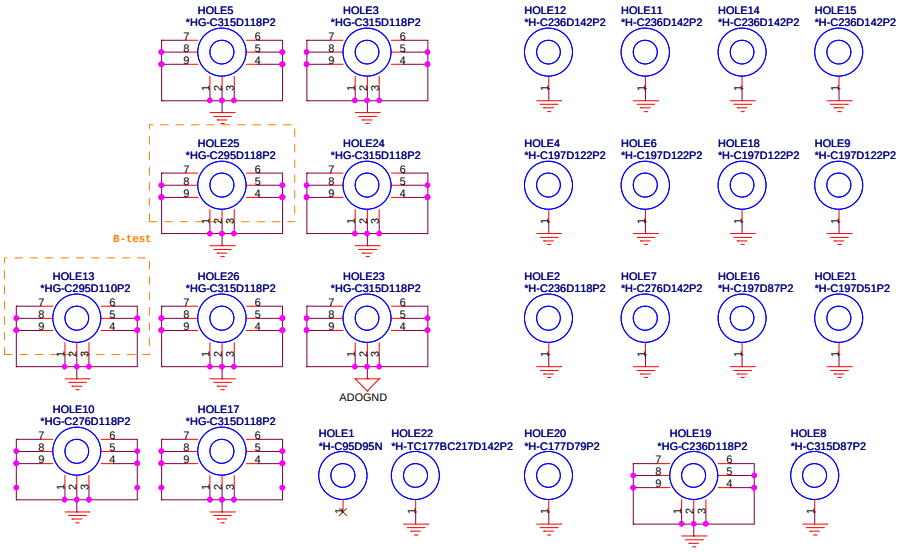
SATA HDD(HDD)



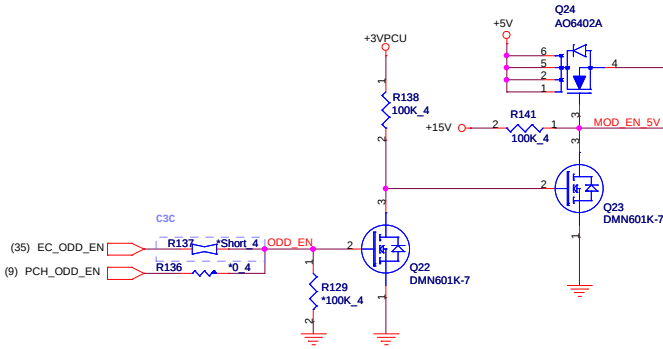
SATA ODD (ODD)



HOLE(OTH)

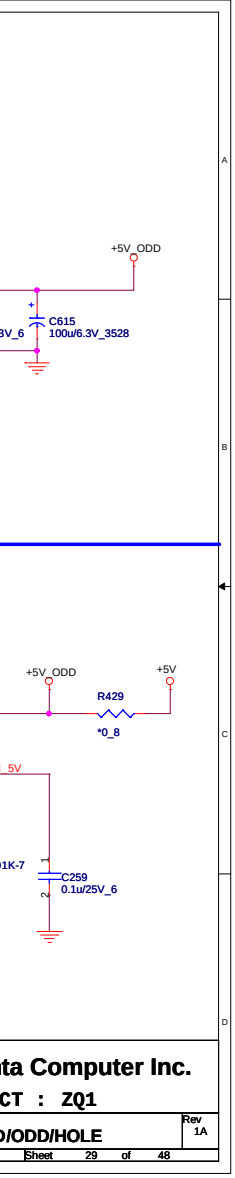


ODD POWER(ODD)



Connect to PCH(GPIO21) pin Y9
and EC pin28(GPIO53)

Quanta		
PROJECT		
Size	Document Number	SATA-HDD/O
Date:	Tuesday, March 30, 2010	



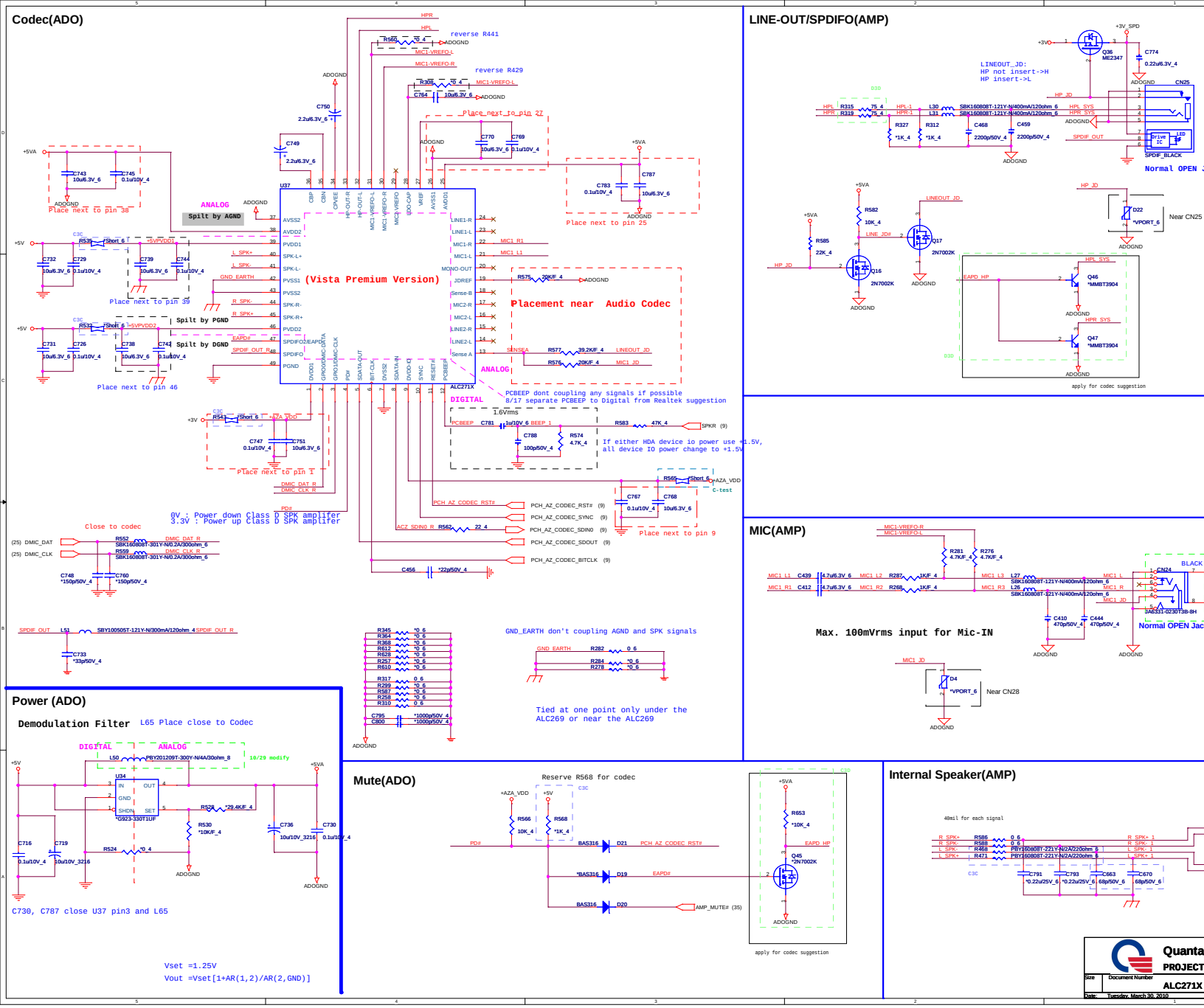
ta Computer Inc.

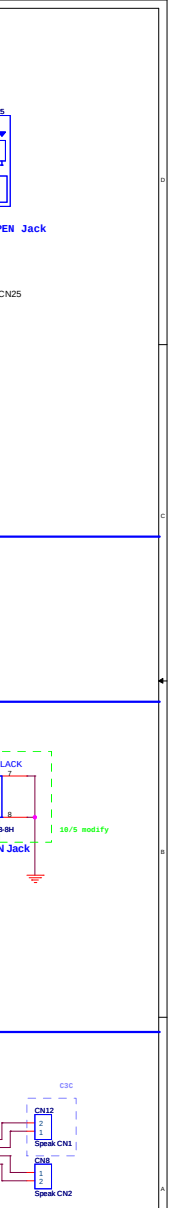
CT : ZQ1

D/ODD/HOLE

Rev 1A

Sheet 29 of 48


Codec(ADO)
U37
ALC271X
(Vista Premium Version)
ANALOG
Spilt by AGND
Spilt by PGND
Spilt by DGND
DIGITAL
Placement near Audio Codec
Place next to pin 38
Place next to pin 39
Place next to pin 46
Place next to pin 1
Place next to pin 25
Place next to pin 9
Place next to pin 27
reverse R441
reverse R429
PCBEEP dont coupling any signals if possible
8/17 separate PCBEEP to Digital from Realtek suggestion
If either HDA device io power use +1.5V,
all device IO power change to +1.5V
0V : Power down Class D SPK amplifier
3.3V : Power up class D SPK amplifier
Close to codec
GND_EARTH don't coupling AGND and SPK signals
Tied at one point only under the
ALC269 or near the ALC269
LINE-OUT/SPDIFO(AMP)
LINEOUT_JD:
HP not insert->H
HP insert->L
Normal OPEN Jack
Near CN25
apply for codec suggestion
MIC(AMP)
Max. 100mVrms input for Mic-IN
Normal OPEN Jack
Near CN28
Power (ADO)
Demodulation Filter
L65 Place close to Codec
C730, C787 close U37 pin3 and L65
Vset =1.25V
Vout =Vset[1+AR(1,2)/AR(2,GND)]
Mute(ADO)
Reserve R568 for codec
apply for codec suggestion
Internal Speaker(AMP)
40mil for each signal
Quanta
PROJECT
ALC271X
Size
Document Number
Date: Tuesday, March 30, 2010



nta Computer Inc.

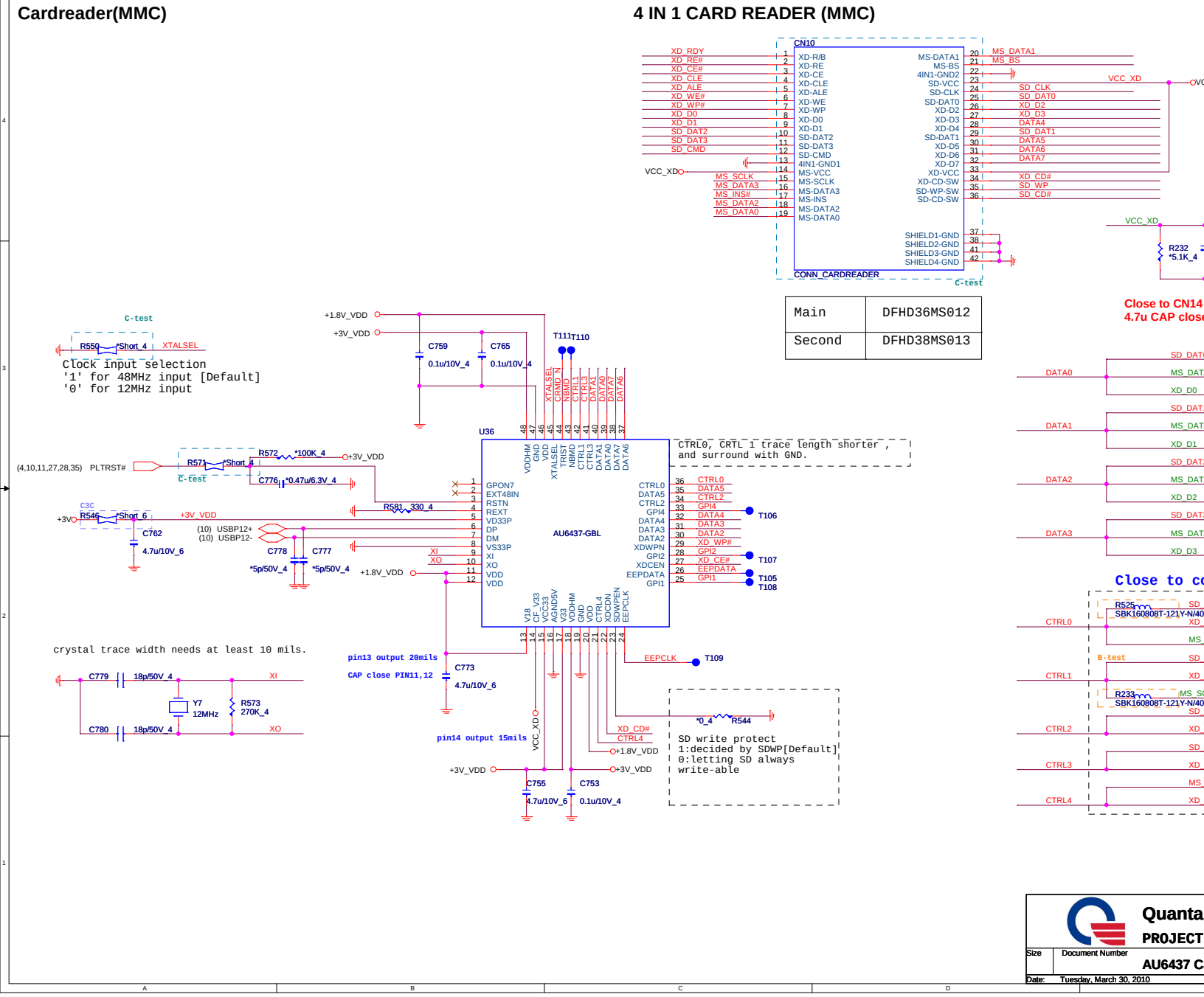
ECT : ZQ1

71X / AMP / SPK Rev 1A

Sheet 30 of 48

Cardreader(MMC)

4 IN 1 CARD READER (MMC)



Main	DFHD36MS012
Second	DFHD38MS013

Quanta

PROJECT

Size | Document Number | AU6437 C

Date: Tuesday, March 30, 2010

VCC_XD

C395
4.7u/10V_6

C392
0.1u/10V_4

N14 pin 14 & pin23
lose to pin23

DAT0
DATA0
D0
DAT1
DATA1
D1
DAT2
DATA2
D2
DAT3
DATA3
D3

connector

SD_CLK
N/400mA/120ohm_6
XD_ALE
MS_BS
SD_WP
XD_CLE
S_SCLK
N/400mA/120ohm_6
SD_CMD
XD_RDY
SD_CD#
XD_WE#
MS_INS#
XD_RE#

C718
*10p/50V_4

C391
*10p/50V_4

ta Computer Inc.

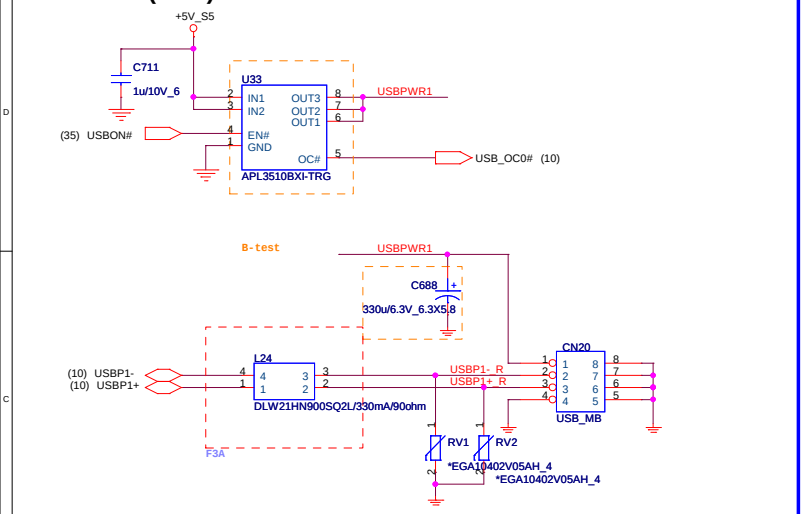
CT : ZQ1

7 CardReader

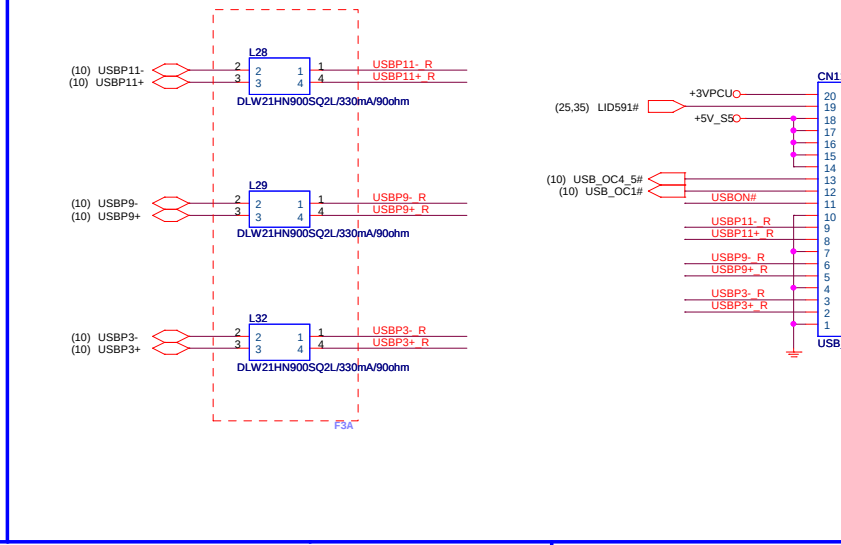
Rev
1A

Sheet 31 of 48

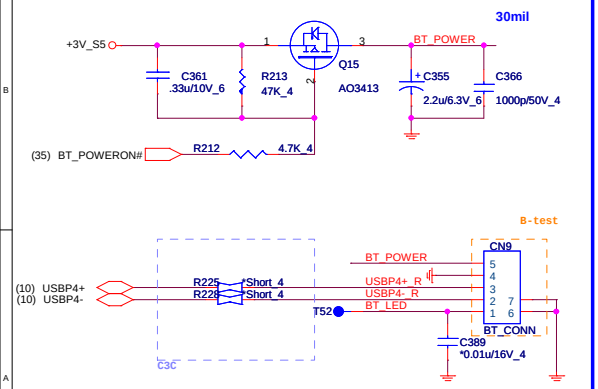
USB PORT(USB)



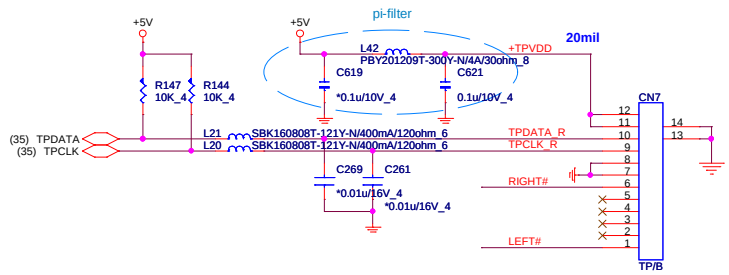
USB BOARD CONN(USB)



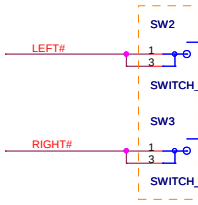
BLUETOOTH CONN(BTM)



TOUCHPAD BOARD CONN(TPD)



TP SWITCH(UIF)



Quanta

PROJECT

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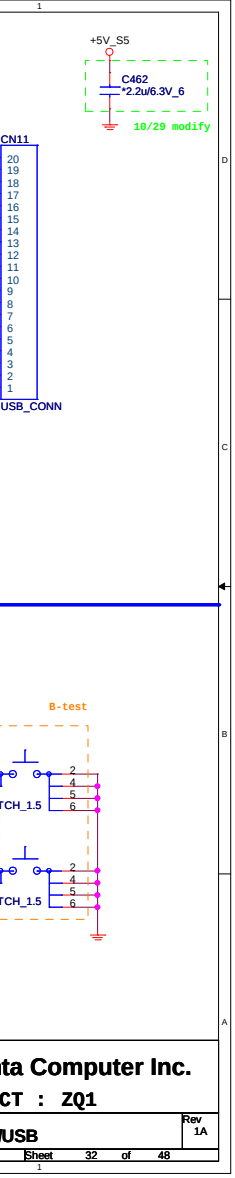
Date:	Tuesday, March 30, 2010	



ta Computer Inc.

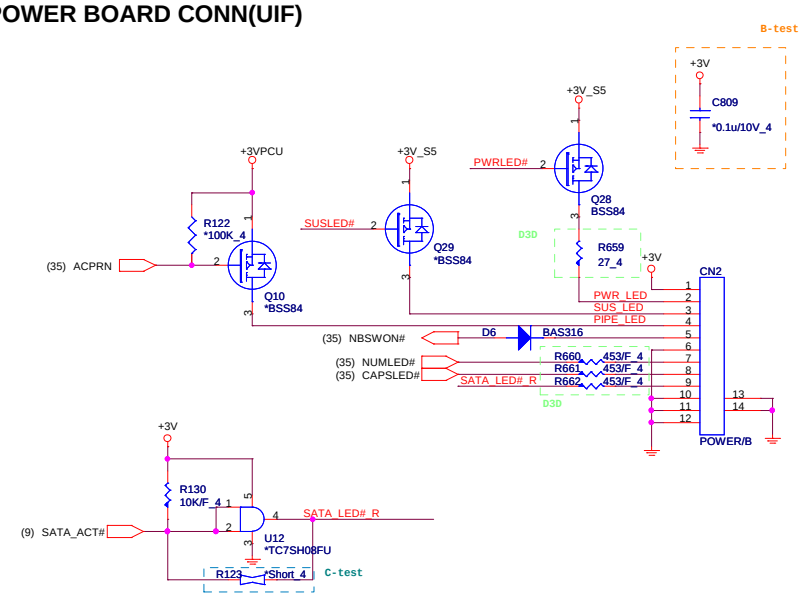
CT : ZQ1

USB

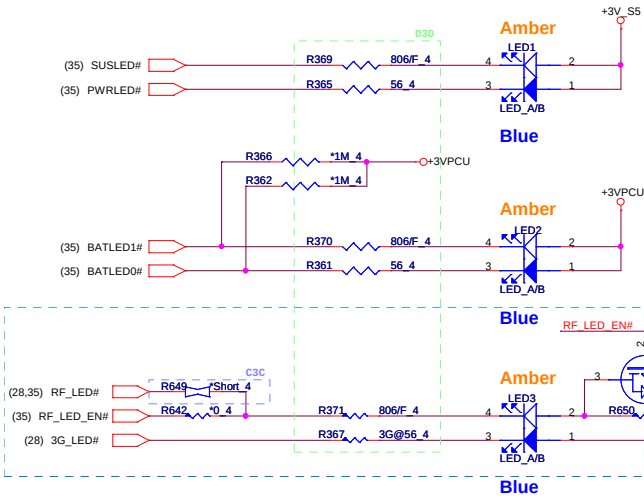
Rev 1A

Sheet 32 of 48

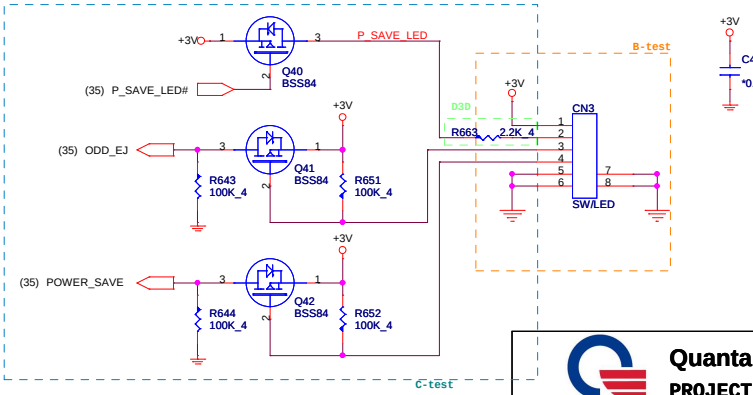
POWER BOARD CONN(UIF)



LED(UIF)



SW BOARD CONNECTOR(UIF)



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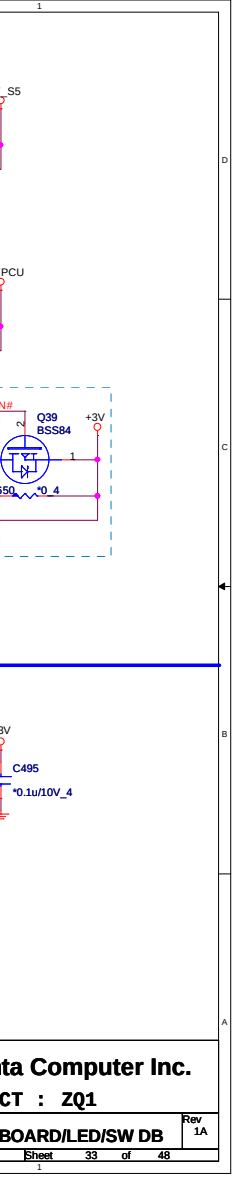
PROJECT

Size	Document Number	POWER BO
Date:	Tuesday, March 30, 2010	



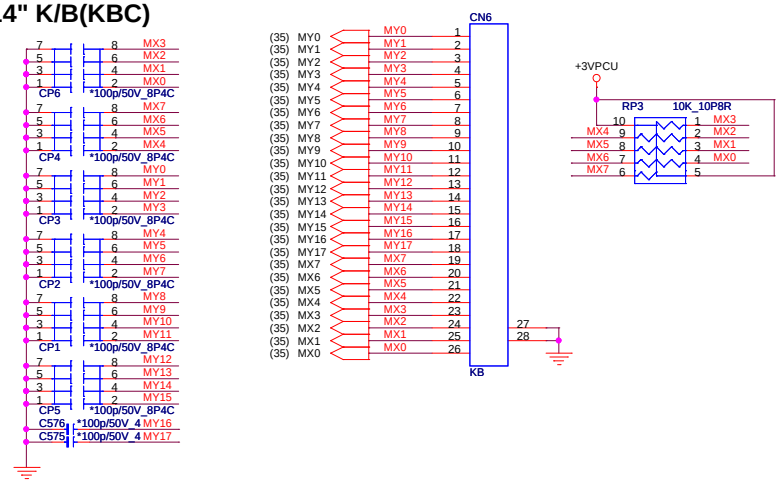
ta Computer Inc.

CT : ZQ1

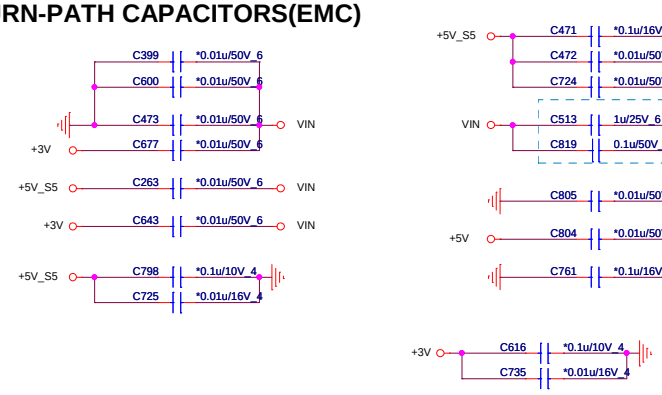
BOARD/LED/SW DB | Rev 1A

Sheet 33 of 48

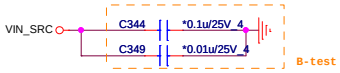
14" K/B(KBC)



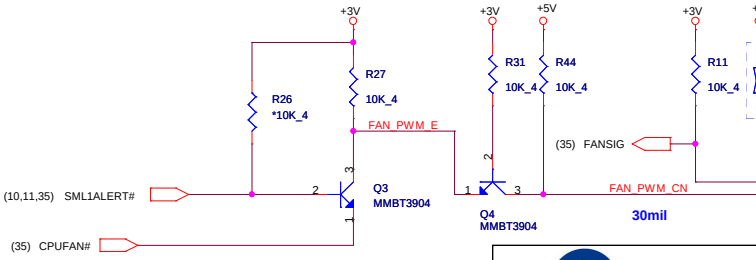
EE RETURN-PATH CAPACITORS(EMC)



STITCHING for LPC



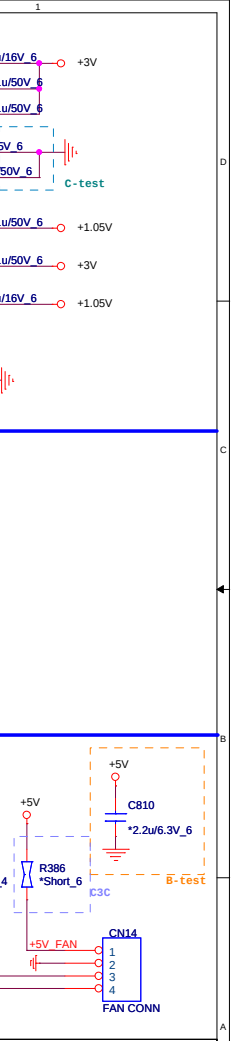
CPU FAN(THM)



Quanta C

PROJECT

Size	Document Number	
	KB/FAN/EE RE	
Date: Tuesday, March 30, 2010		Sh



a Computer Inc.

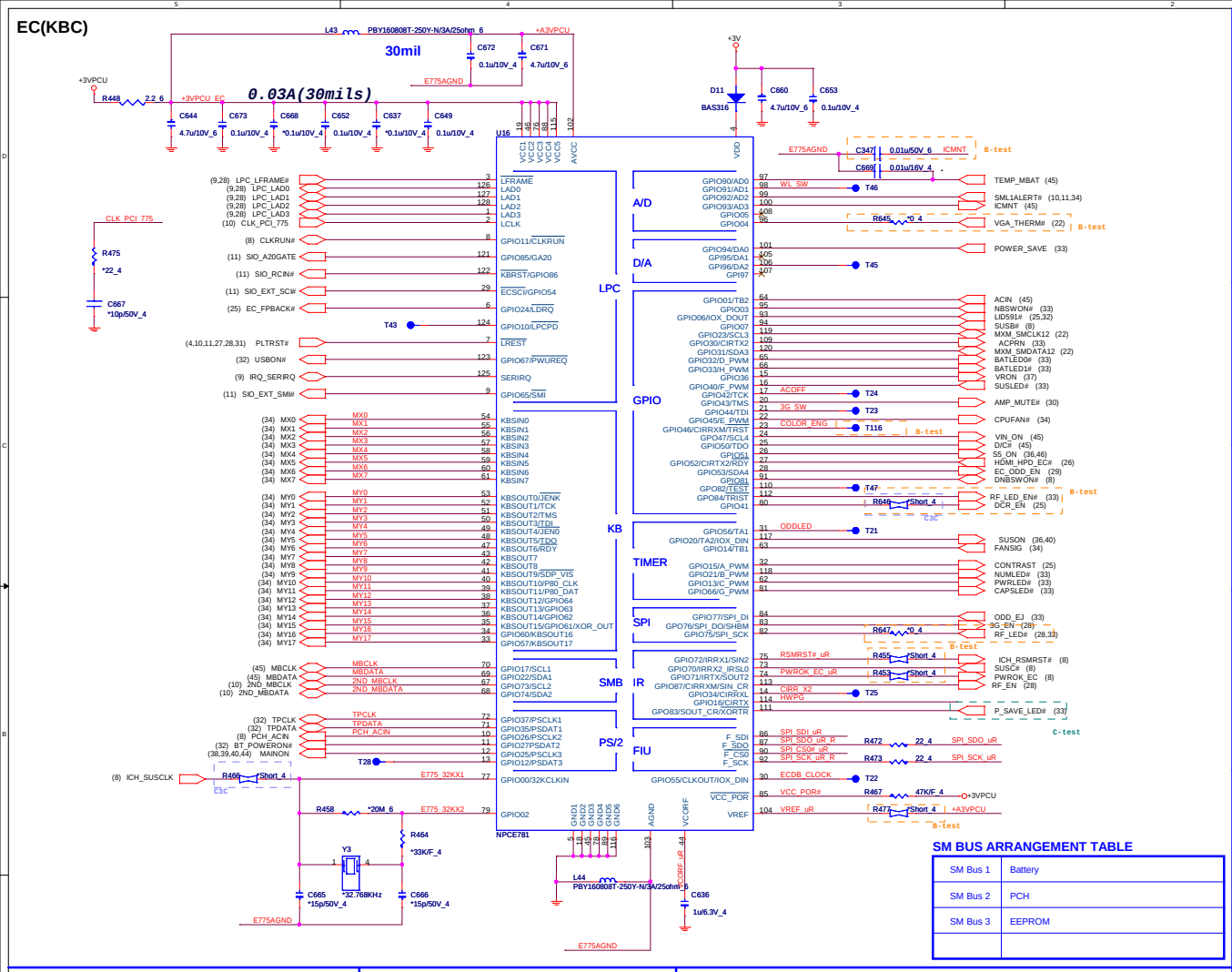
T : ZQ1

RETURN CAP

Rev 1A

Sheet 34 of 48

EC(KBC)



SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	EEPROM

I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared me

SHBM 3G_EN

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH devic
Enabled ('0') if using SPI flash fo

SM BUS PU(KBC)

MBCLK R450
MBDATA R445

MXM_SMCLK12 R447
MXM_SMDATA12 R451

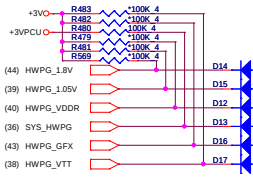
2ND_MBCLK R151
2ND_MBDATA R153
EC_ODD_EN R444

SPI FLASH(KBC)

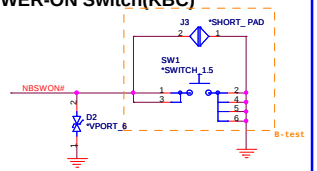
SPI_SDI uR R476 22_4 SPI_SDI uR
R470 100K_4 SPI_SDO uR
SPI_SCK uR
+3VPCU R457 10K_4 SPI_CS0# uR

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by
default, the flash device should be 50MHz (or faster)

HWPG(KBC)



POWER-ON Switch(KBC)



INTERNAL KEYBOARD STRIP

MY0 R14

Size	Document Number	
		Q
		PR
		WI

Date: Tuesday, March 30, 2010

C)

ed memory with host BIOS

R465 10K_4

ail :
device on LPC.
ash for both system BIOS and EC firmware

+3VPCU
50 10K_4
45 10K_4
B-test
+3V_D_EXT
47 10K_4
51 10K_4

+3V
51 10K_4
53 10K_4
44 10K_4

+3VPCU
U29
DI uR_R 2 SO
DO uR 5 SI
CK uR 6 SCK
S0# uR 1 CE
8 VDD
7 HOLD
3 WP
4 VSS
W25X40BVSSIG
C664
0.1u/10V_4
C-test

+3V
R469
10K_4
BAS316
BAS316
BAS316
BAS316
BAS316
BAS316
HWPG
R474
*Short_4
B-test
MPWROK (4)

RIP SET(KBC)

+3VPCU
R145 10K_4

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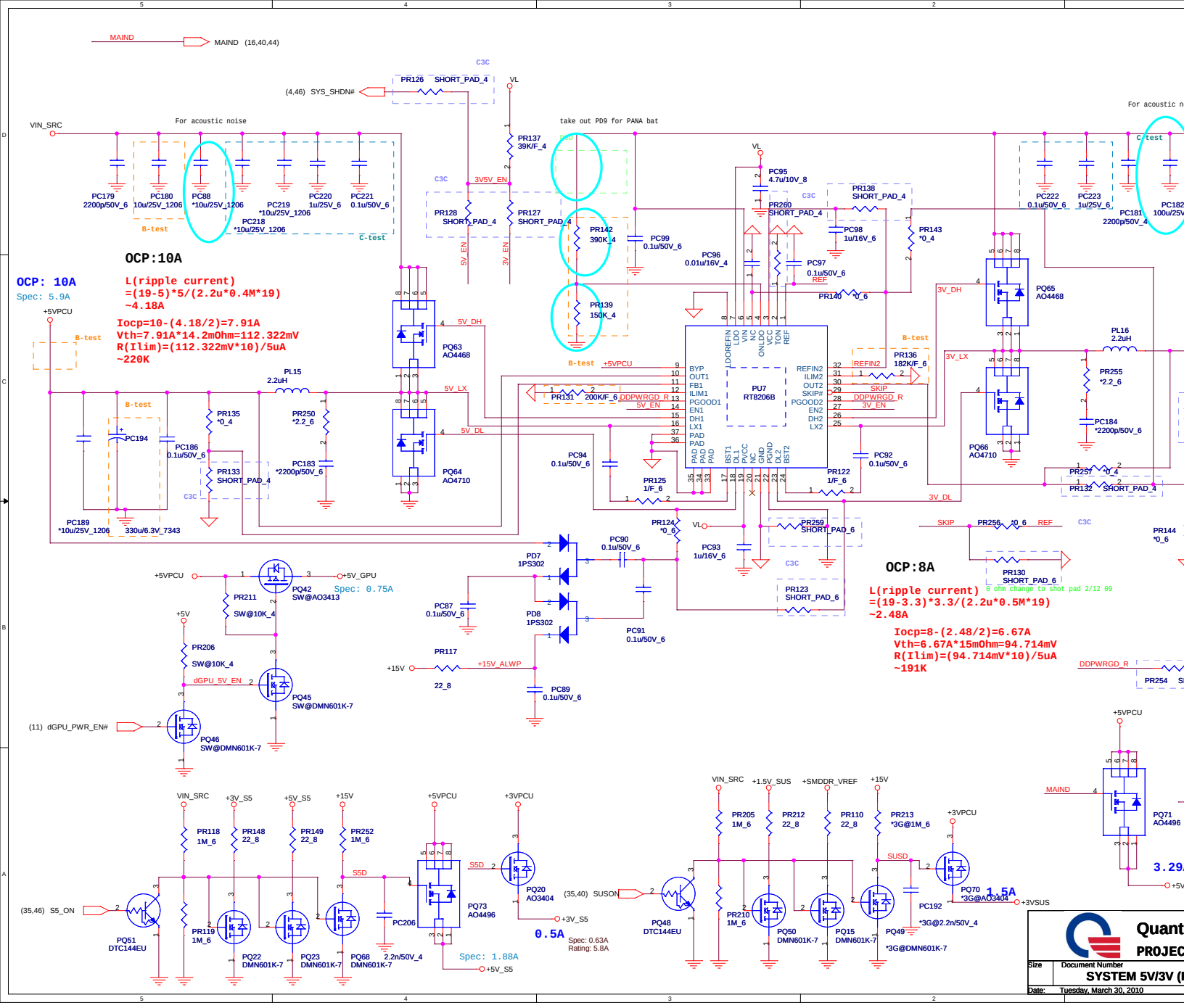
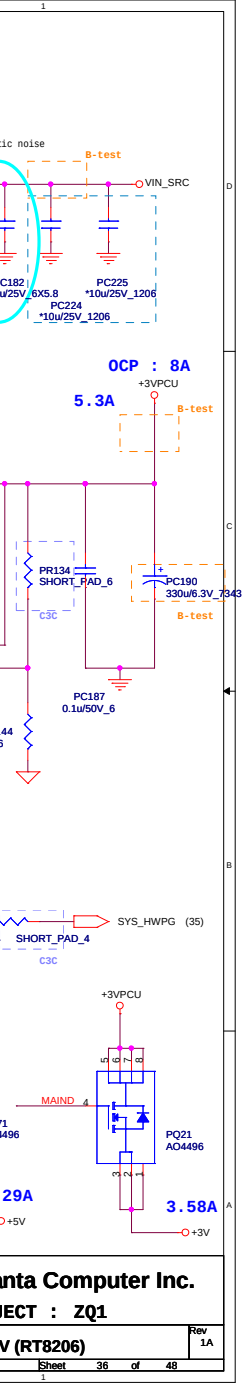
PROJECT : ZQ1

WPCE775C_0DG & FLASH Rev 1A


MAIND
MAIND (16,40,44)
(4,46) SYS_SHDN#
PR126 SHORT_PAD_4
VL
VIN_SRC
For acoustic noise
take out PD9 for PANA bat
For acoustic n
PC179 2200p/50V_6
PC180 10u/25V_1206
PC88 *10u/25V_1206
PC219 *10u/25V_1206
PC220 1u/25V_6
PC221 0.1u/50V_6
PC218 *10u/25V_1206
B-test
C-test
PR137 39K/F_4
PR128 SHORT_PAD_4
PR127 SHORT_PAD_4
3V5V_EN
5V_EN
3V_EN
PR142 390K_4
PR139 150K_4
PC99 0.1u/50V_6
PC96 0.01u/16V_4
PC95 4.7u/10V_8
PR260 SHORT_PAD_4
PR138 SHORT_PAD_4
PC98 1u/16V_6
PR143 *0_4
PC97 0.1u/50V_6
REF
PR140 *0_6
PC222 0.1u/50V_6
PC223 1u/25V_6
PC181 2200p/50V_4
PC182 100u/25V
OCP:10A
OCP: 10A
Spec: 5.9A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=10-(4.18/2)=7.91A
Vth=7.91A*14.2mOhm=112.322mV
R(Ilim)=(112.322mV*10)/5uA
~220K
+5VPCU
PL15 2.2uH
PR135 *0_4
PR250 *2.2_6
PC194
PC186 0.1u/50V_6
PC183 *2200p/50V_6
PR133 SHORT_PAD_4
PC189 *10u/25V_1206
330u/6.3V_7343
PQ63 AO4468
PQ64 AO4710
5V_DH
5V_LX
5V_DL
PR131 200K/F_6
DDPWRGD_R
5V_EN
+5VPCU
PU7 RT8206B
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
LDOREFIN
LDO
VIN
NC
ONLDO
VCC
TON
REF
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
BST1
DL1
PVCC
GND
PGND
DL2
BST2
PR136 182K/F_6
REFIN2
SKIP
DDPWRGD_R
3V_EN
3V_DH
3V_LX
3V_DL
PQ65 AO4468
PQ66 AO4710
PL16 2.2uH
PR255 *2.2_6
PC184 *2200p/50V_6
PR257 *0_4
PR132 SHORT_PAD_4
PC94 0.1u/50V_6
PR125 1/F_6
PC92 0.1u/50V_6
PR122 1/F_6
PR124 *0_6
PC93 1u/16V_6
PR259 SHORT_PAD_6
PR123 SHORT_PAD_6
SKIP
PR256 *0_6
REF
PR130 SHORT_PAD_6
0 ohm change to shot pad 2/12 09
PR144 *0_6
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=94.714mV
R(Ilim)=(94.714mV*10)/5uA
~191K
DDPWRGD_R
PR254
+5VPCU
PQ42 SW@AO3413
Spec: 0.75A
+5V_GPU
PR211 SW@10K_4
+5V
PR206 SW@10K_4
dGPU_5V_EN
PQ45 SW@DMN601K-7
(11) dGPU_PWR_EN#
PQ46 SW@DMN601K-7
PD7 1PS302
PD8 1PS302
PC90 0.1u/50V_6
PC91 0.1u/50V_6
PC87 0.1u/50V_6
PR117 22_8
+15V
+15V_ALWP
PC89 0.1u/50V_6
+5VPCU
MAIND
PQ71 AO4496
3.29
+5V
VIN_SRC
+3V_S5
+5V_S5
+15V
PR118 1M_6
PR148 22_8
PR149 22_8
PR252 1M_6
S5D
(35,46) S5_ON
PQ51 DTC144EU
PR119 1M_6
PQ22 DMN601K-7
PQ23 DMN601K-7
PQ68 DMN601K-7
PC206 2.2n/50V_4
+5VPCU
PQ73 AO4496
Spec: 1.88A
+5V_S5
+3VPCU
PQ20 AO3404
0.5A
+3V_S5
Spec: 0.63A
Rating: 5.8A
(35,40) SUSON
PQ48 DTC144EU
VIN_SRC
+1.5V_SUS
+SMDDR_VREF
+15V
PR205 1M_6
PR212 22_8
PR110 22_8
PR213 *3G@1M_6
PR210 1M_6
PQ50 DMN601K-7
PQ15 DMN601K-7
PQ49 *3G@DMN601K-7
SUSD
PC192 *3G@2.2n/50V_4
+3VPCU
PQ70 *3G@AO3404
1.5A
+3VSUS
Quant
PROJEC
Size
Document Number
SYSTEM 5V/3V (
Date: Tuesday, March 30, 2010

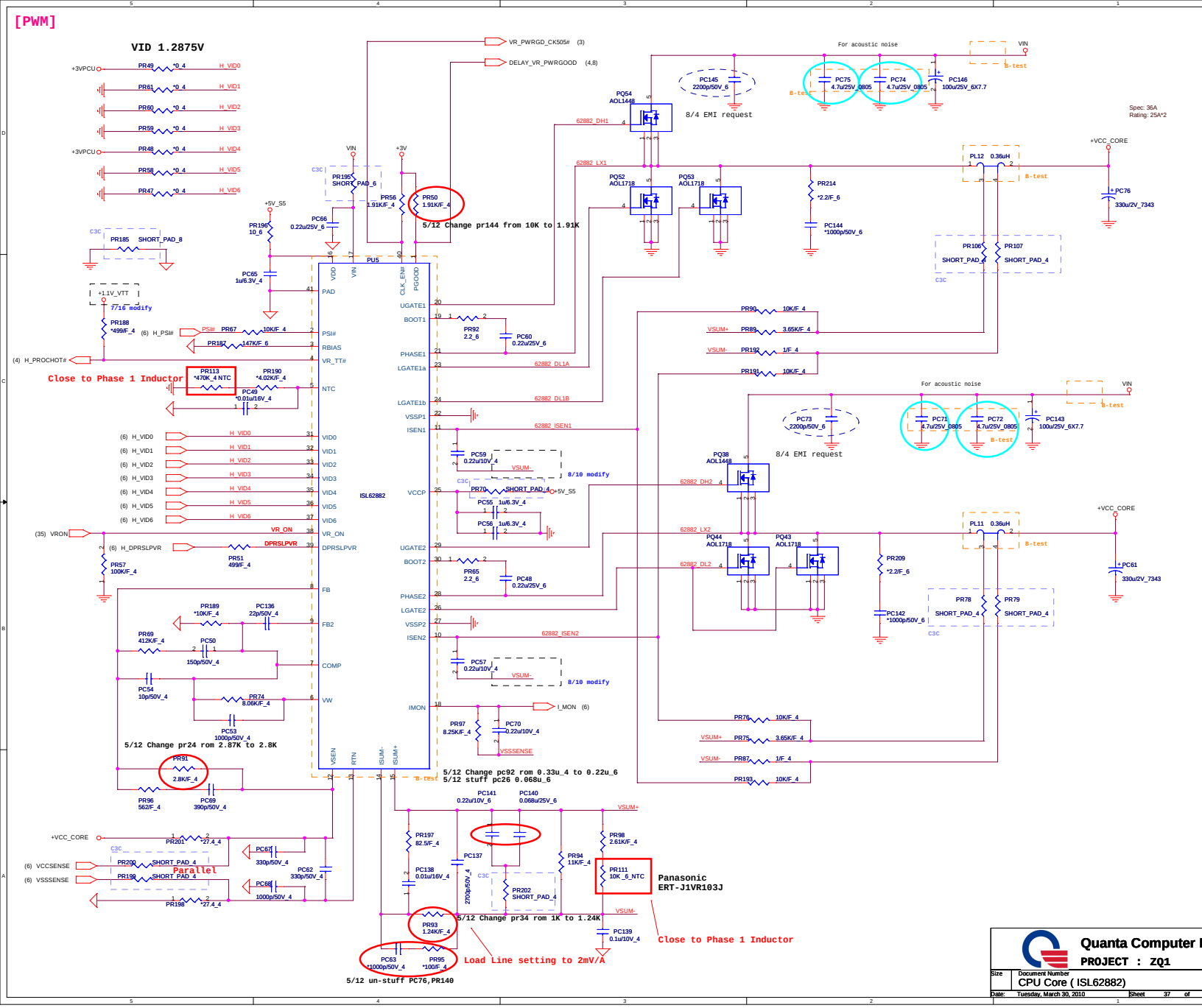


anta Computer Inc.

JECT : ZQ1

V (RT8206)	Rev 1A

Sheet 36 of 48


[PWM]
VID 1.2875V
+3VPCU
PR49 *0_4 H_VID0
PR61 *0_4 H_VID1
PR60 *0_4 H_VID2
PR59 *0_4 H_VID3
PR48 *0_4 H_VID4
PR58 *0_4 H_VID5
PR47 *0_4 H_VID6
VR_PWRGD_CK505# (3)
DELAY_VR_PWRGOOD (4,8)
For acoustic noise
VIN
B-test
PC145 2200p/50V_6
PC75 4.7u/25V_0805
PC74 4.7u/25V_0805
PC146 100u/25V_6X7.7
PQ54 AOL1448
8/4 EMI request
Spec: 36A
Rating: 25A*2
+VCC_CORE
PL12 0.36uH
PC76 330u/2V_7343
62882_DH1
62882_LX1
PQ52 AOL1718
PQ53 AOL1718
PR214 *2.2/F_6
PC144 *1000p/50V_6
PR106 SHORT_PAD_4
PR107 SHORT_PAD_4
C3C
PR195 SHORT_PAD_6
PR56 1.91K/F_4
PR50 1.91K/F_4
5/12 Change pr144 from 10K to 1.91K
PC66 0.22u/25V_6
+5V_S5
PR196 10_6
PR185 SHORT_PAD_8
PC65 1u/6.3V_4
PU5
VDD
VIN
CLK_EN#
PGOOD
PAD
UGATE1
BOOT1
PR92 2.2_6
PC60 0.22u/25V_6
PHASE1
LGATE1a
62882_DL1A
LGATE1b
62882_DL1B
VSSP1
ISEN1
62882_ISEN1
+1.1V_VTT
7/16 modify
PR188 *499/F_4
(6) H_PSI#
PSI#
PR67 10K/F_4
PR187 147K/F_6
RBIAS
VR_TT#
(4) H_PROCHOT#
Close to Phase 1 Inductor
PR113 *470K_4 NTC
PR190 *4.02K/F_4
PC49 *0.01u/16V_4
NTC
PR90 10K/F_4
PR89 3.65K/F_4
PR192 1/F_4
PR191 10K/F_4
VSUM+
VSUM-
For acoustic noise
VIN
B-test
PC73 2200p/50V_6
PC71 4.7u/25V_0805
PC72 4.7u/25V_0805
PC143 100u/25V_6X7.7
8/4 EMI request
PQ38 AOL1448
PC59 0.22u/10V_4
VSUM-
8/10 modify
VCCP
PR70 SHORT_PAD_4
+5V_S5
PC55 1u/6.3V_4
PC56 1u/6.3V_4
(6) H_VID0
(6) H_VID1
(6) H_VID2
(6) H_VID3
(6) H_VID4
(6) H_VID5
(6) H_VID6
VID0
VID1
VID2
VID3
VID4
VID5
VID6
ISL62882
(35) VRON
VR_ON
(6) H_DPRSLPVR
DPRSLPVR
PR51 499/F_4
PR57 100K/F_4
UGATE2
BOOT2
PR65 2.2_6
PC48 0.22u/25V_6
PHASE2
LGATE2
VSSP2
ISEN2
62882_ISEN2
62882_LX2
62882_DL2
PQ44 AOL1718
PQ43 AOL1718
PR209 *2.2/F_6
PC142 *1000p/50V_6
PL11 0.36uH
PC61 330u/2V_7343
PR78 SHORT_PAD_4
PR79 SHORT_PAD_4
FB
PR189 *10K/F_4
PC136 22p/50V_4
PR69 412K/F_4
PC50 150p/50V_4
FB2
COMP
PC54 10p/50V_4
PR74 8.06K/F_4
VW
PC53 1000p/50V_4
5/12 Change pr24 rom 2.87K to 2.8K
PR91 2.8K/F_4
PR96 562/F_4
PC69 390p/50V_4
VSEN
RTN
ISUM-
ISUM+
IMON
I_MON (6)
PR97 8.25K/F_4
PC70 0.22u/10V_4
VSSSENSE
PC57 0.22u/10V_4
PR76 10K/F_4
PR75 3.65K/F_4
PR87 1/F_4
PR193 10K/F_4
5/12 Change pc92 rom 0.33u_4 to 0.22u_6
5/12 stuff pc26 0.068u_6
PC141 0.22u/10V_6
PC140 0.068u/25V_6
PR197 82.5/F_4
PC137 270p/50V_4
PR94 11K/F_4
PR98 2.61K/F_4
PR111 10K_6_NTC
Panasonic
ERT-J1VR103J
PC138 0.01u/16V_4
PR202 SHORT_PAD_4
PR93 1.24K/F_4
5/12 Change pr34 rom 1K to 1.24K
PC139 0.1u/10V_4
Close to Phase 1 Inductor
+VCC_CORE
PR201 *27.4_4
(6) VCCSENSE
(6) VSSSENSE
PR200 SHORT_PAD_4
PR199 SHORT_PAD_4
Parallel
PC67 330p/50V_4
PC62 330p/50V_4
PC68 1000p/50V_4
PR198 *27.4_4
PC63 *1000p/50V_4
PR95 *100/F_4
Load Line setting to 2mV/A
5/12 un-stuff PC76,PR140
Quanta Computer I
PROJECT : ZQ1
Size
Document Number
CPU Core (ISL62882)
Date: Tuesday, March 30, 2010
Sheet 37 of

D

C

B

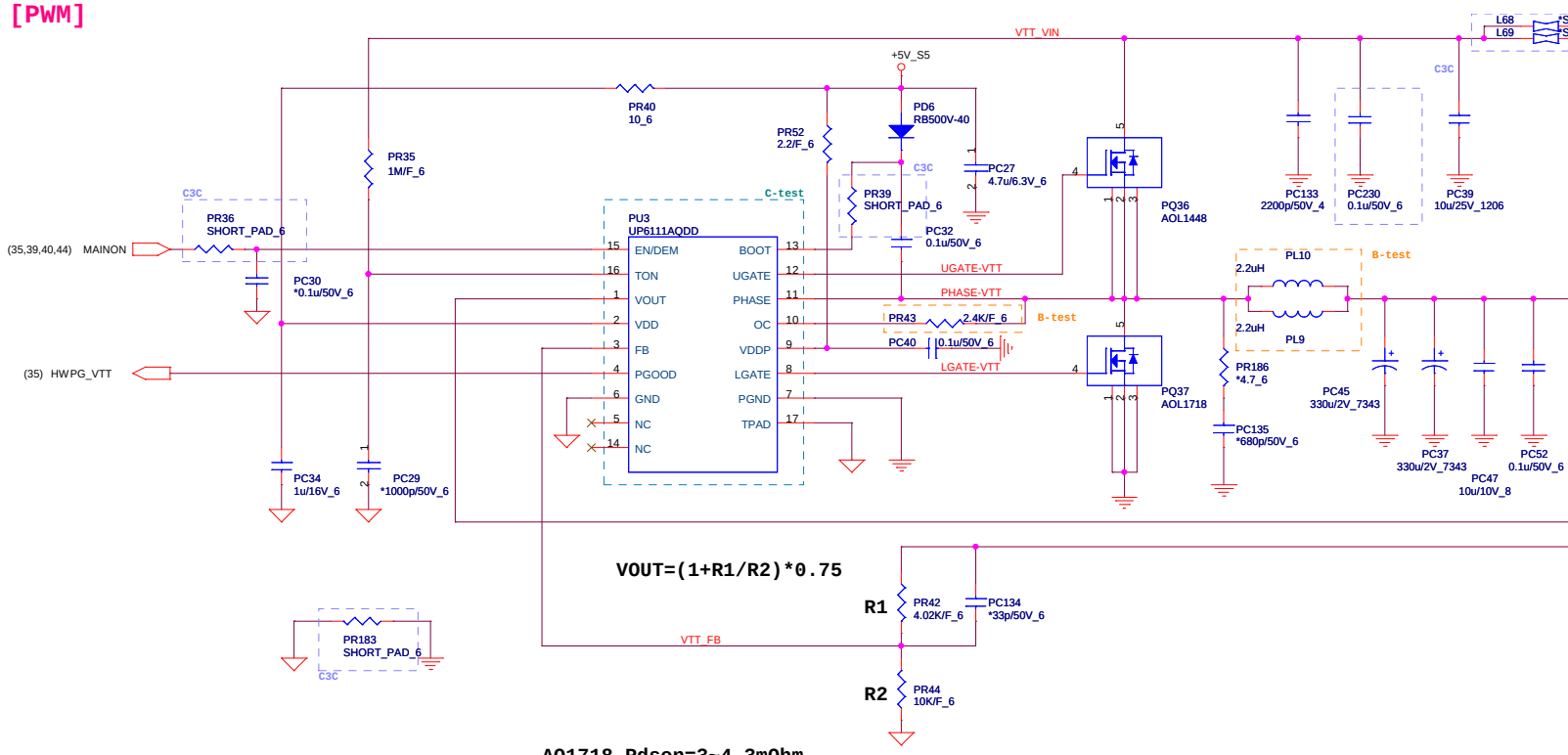
A

er Inc.

Rev
1A

of 48

[PWM]



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO1718 Rdson=3~4.3mOhm

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.64A

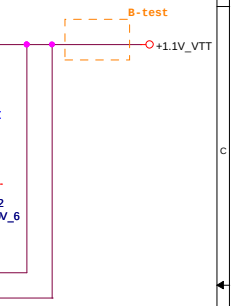
4.3m*18=RILIM*20uA
RILIM=3.87K --- 3.92K

Quanta C

PROJECT

Size	Document Number
	+VTT (UP6111A)
Date: Tuesday, March 30, 2010	Sh

OCP: 18A
1.05V/13.5A

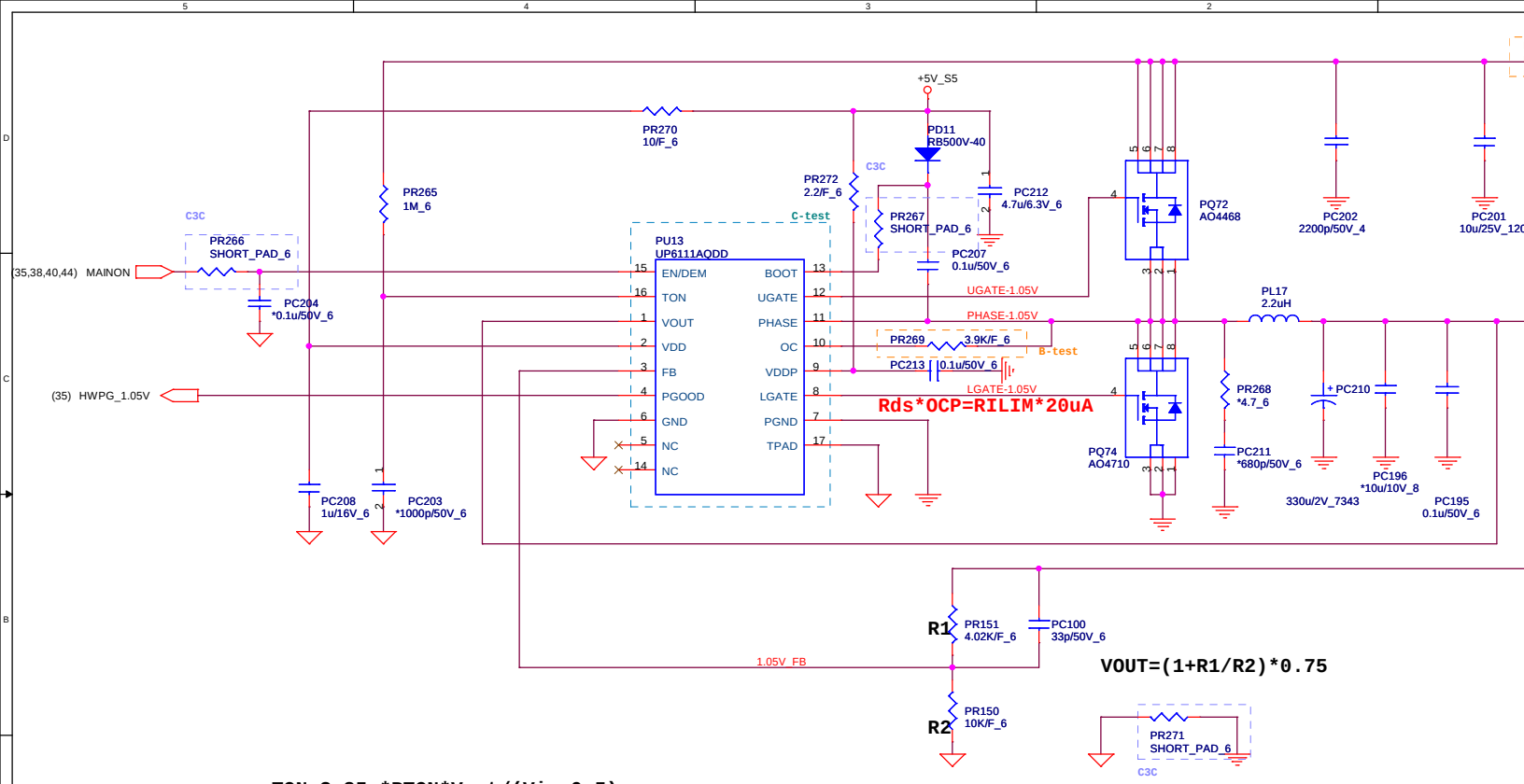


a Computer Inc.

T : ZQ1

Rev
1A

Sheet 38 of 48



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

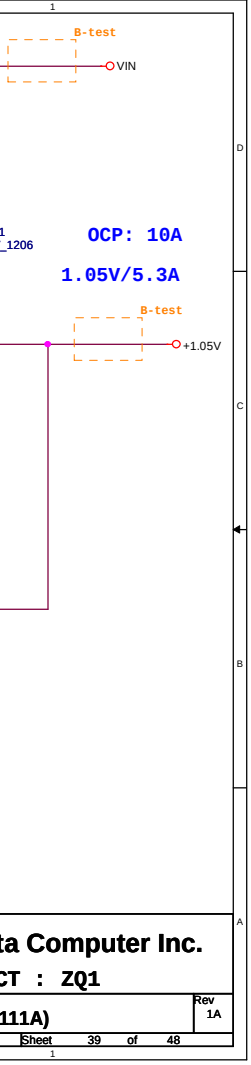
14.2m*10=RILIM*20uA
RILIM=7.1K--- 7.15K

Quanta

PROJECT

Size	Document Number
	VCCP 1.05V(UP6111

Date: Tuesday, March 30, 2010



ta Computer Inc.

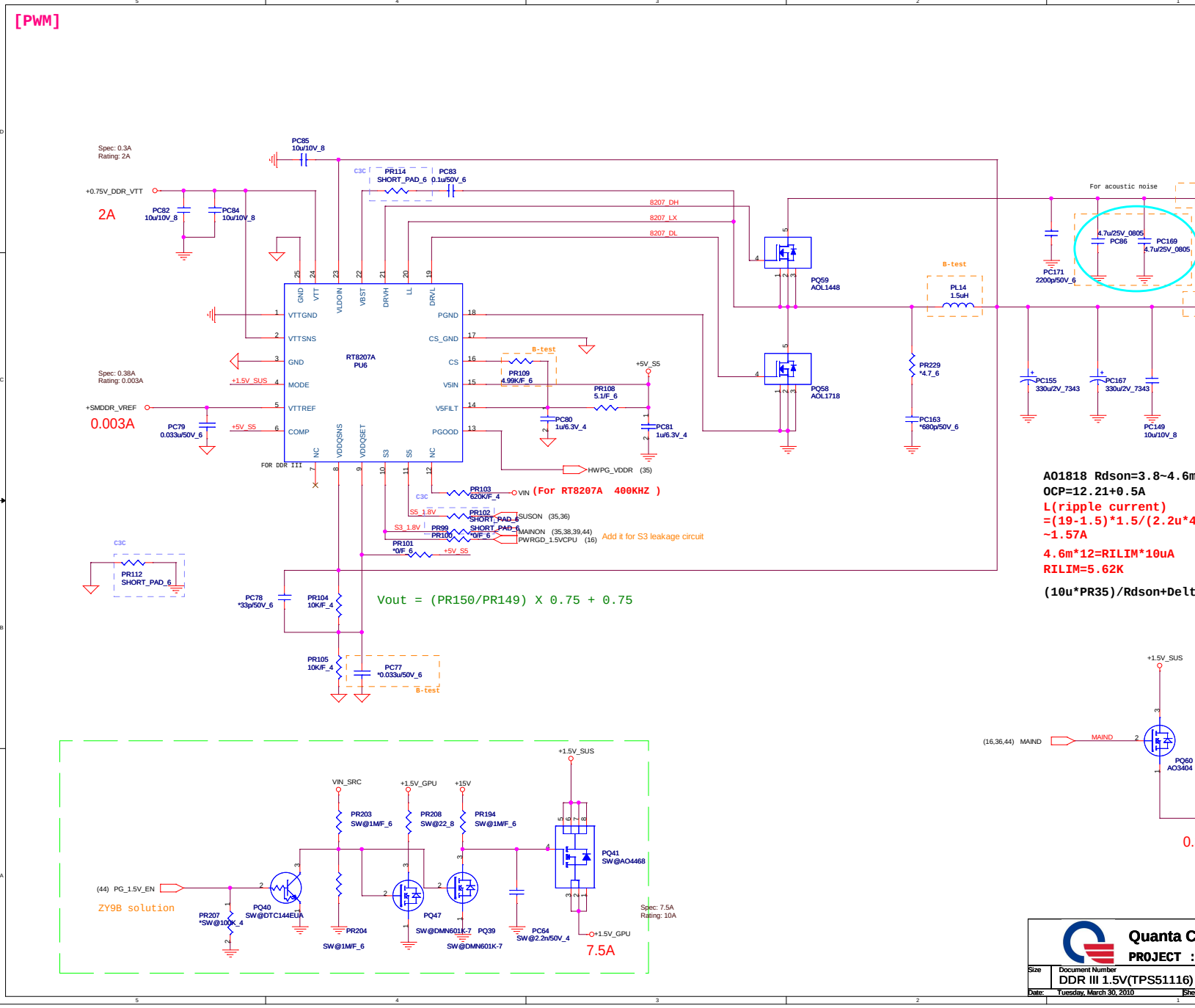
CT : ZQ1

111A)

Rev 1A

Sheet 39 of 48

[PWM]


Spec: 0.3A
Rating: 2A
+0.75V_DDR_VTT
2A
PC85
10u/10V_8
PC82
10u/10V_8
PC84
10u/10V_8
C3C
PR114
SHORT_PAD_6
PC83
0.1u/50V_6
8207_DH
8207_LX
8207_DL
RT8207A
PU6
GND
VTT
VLDOIN
VBST
DRVH
LL
DRVL
VTTGND
VTTSNS
GND
MODE
VTTREF
COMP
PGND
CS_GND
CS
VSIN
VSFILT
PGOOD
NC
VDDQSNS
VDDQSET
S3
S5
NC
FOR DDR III
Spec: 0.38A
Rating: 0.003A
+1.5V_SUS
+SMDDR_VREF
0.003A
PC79
0.033u/50V_6
+5V_S5
B-test
PR109
4.99K/F_6
PR108
5.1/F_6
PC80
1u/6.3V_4
PC81
1u/6.3V_4
HWPG_VDDR (35)
PR103
620K/F_4
VIN
(For RT8207A 400KHZ)
PR102
SHORT_PAD_6
SUSON (35,36)
PR99
SHORT_PAD_6
PR100
*0/F_6
MAINON (35,38,39,44)
PWRGD_1.5VCPU (16)
Add it for S3 leakage circuit
PR101
*0/F_6
PR112
SHORT_PAD_6
PC78
*33p/50V_6
PR104
10K/F_4
Vout = (PR150/PR149) X 0.75 + 0.75
PR105
10K/F_4
PC77
*0.033u/50V_6
PQ59
AOL1448
PQ58
AOL1718
PL14
1.5uH
PR229
*4.7_6
PC163
*680p/50V_6
For acoustic noise
4.7u/25V_0805
PC86
PC169
4.7u/25V_0805
PC171
2200p/50V_6
PC155
330u/2V_7343
PC167
330u/2V_7343
PC149
10u/10V_8
AO1818 Rdson=3.8~4.6m
OCP=12.21+0.5A
L(ripple current)
=(19-1.5)*1.5/(2.2u*4
~1.57A
4.6m*12=RILIM*10uA
RILIM=5.62K
(10u*PR35)/Rdson+Delt
+1.5V_SUS
(16,36,44) MAIND
MAIND
PQ60
AO3404
0.
+1.5V_SUS
VIN_SRC
+1.5V_GPU
+15V
PR203
SW@1M/F_6
PR208
SW@22_8
PR194
SW@1M/F_6
PQ41
SW@AO4468
(44) PG_1.5V_EN
ZY9B solution
PR207
*SW@100K_4
PQ40
SW@DTC144EUA
PR204
SW@1M/F_6
PQ47
SW@DMN601K-7
PQ39
SW@DMN601K-7
PC64
SW@2.2n/50V_4
+1.5V_GPU
7.5A
Spec: 7.5A
Rating: 10A
Quanta C
PROJECT :
Size
Document Number
DDR III 1.5V(TPS51116)
Date:
Tuesday, March 30, 2010

VIN

805 B-test 14.5A

12A

+1.5V_SUS

.6mOhm

u*400k*19)

elta_I/2=Iocp

S

PQ60
3404

+1.5V

0.38A

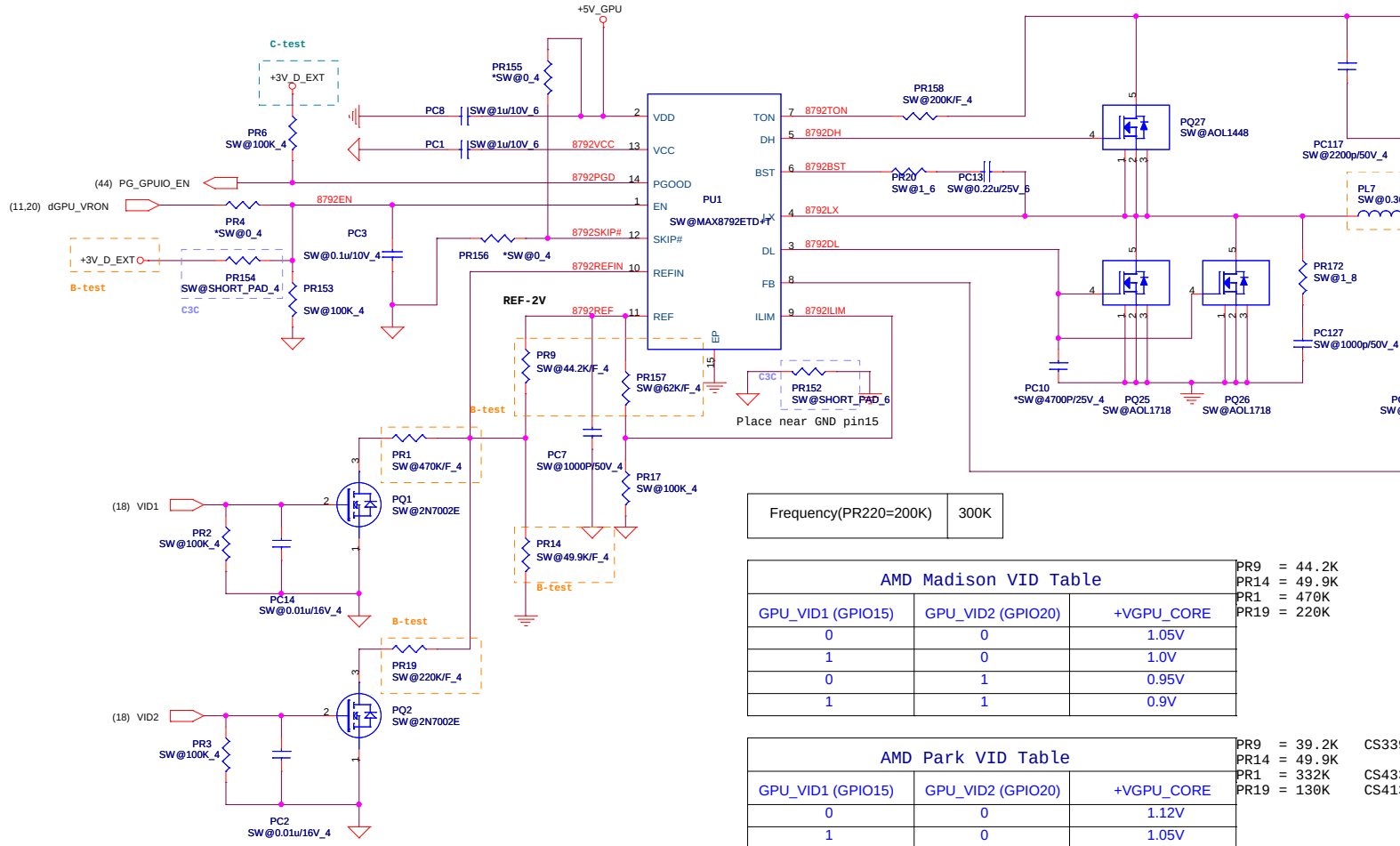
a Computer Inc.

T : ZQ1

16)

Rev
1A

Sheet 40 of 48



Frequency(PR220=200K)	300K

AMD Madison VID Table		
GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.05V
1	0	1.0V
0	1	0.95V
1	1	0.9V

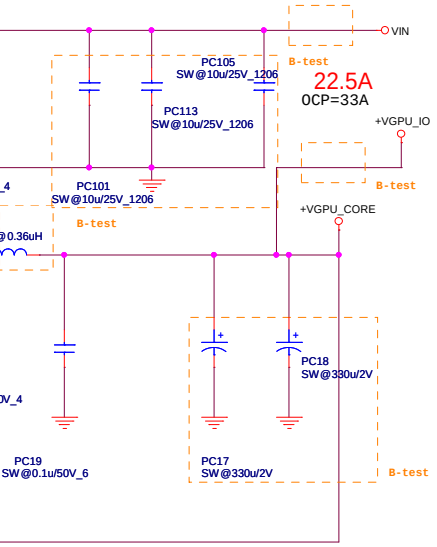
PR9 = 44.2K
PR14 = 49.9K
PR1 = 470K
PR19 = 220K

AMD Park VID Table		
GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.12V
1	0	1.05V
0	1	0.95V
1	1	0.9V

PR9 = 39.2K CS33
PR14 = 49.9K
PR1 = 332K CS43
PR19 = 130K CS41

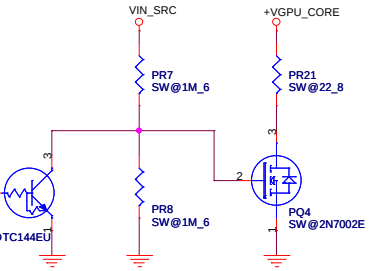
Size

Date:



S33922FB15

S43322FB15
S41302FB00



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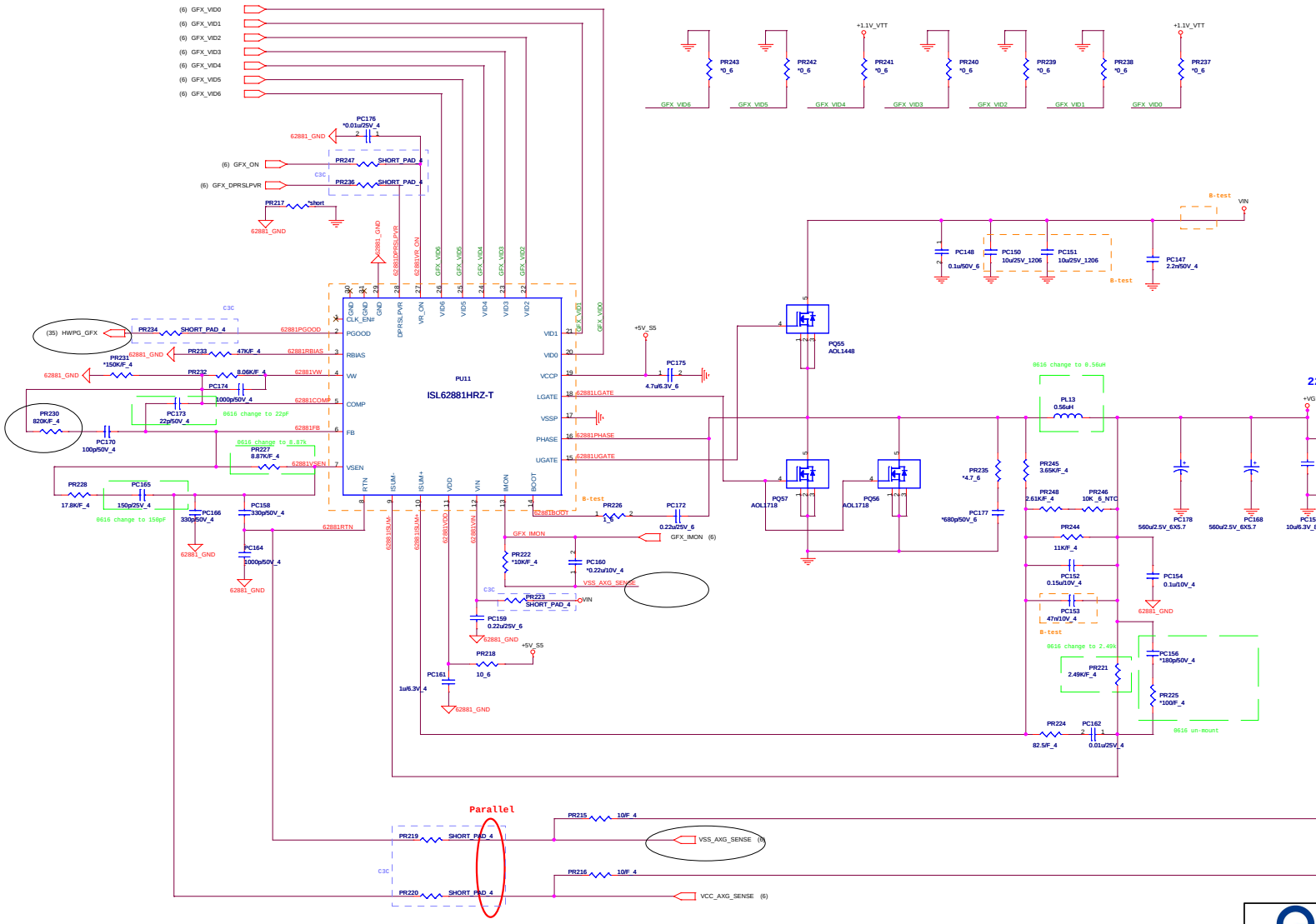
PROJECT : ZQ1

Size	Document Number: GPU CORE(MAX8792)	Rev 1A
Date: Tuesday, March 30, 2010	Sheet 41 of 48	

Int_VGA [PWM]



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Size	Document Numb
	+VGFX_
Date:	Tuesday, March

Spec: 16.5A
Rating: 25A

22A

+VGFX_AXG

DRC=2.7~3mOhm/2

Load Line=7mV/A
3m*6.168=0.925m
0.925m/2.49K=371p
371p*2*8.87K=6.58m
OCP
20u/2*2.42K=24.2m
24.2m/0.6168=36.64m
36.64m/3m=12.21A

PC157
6.3V_8

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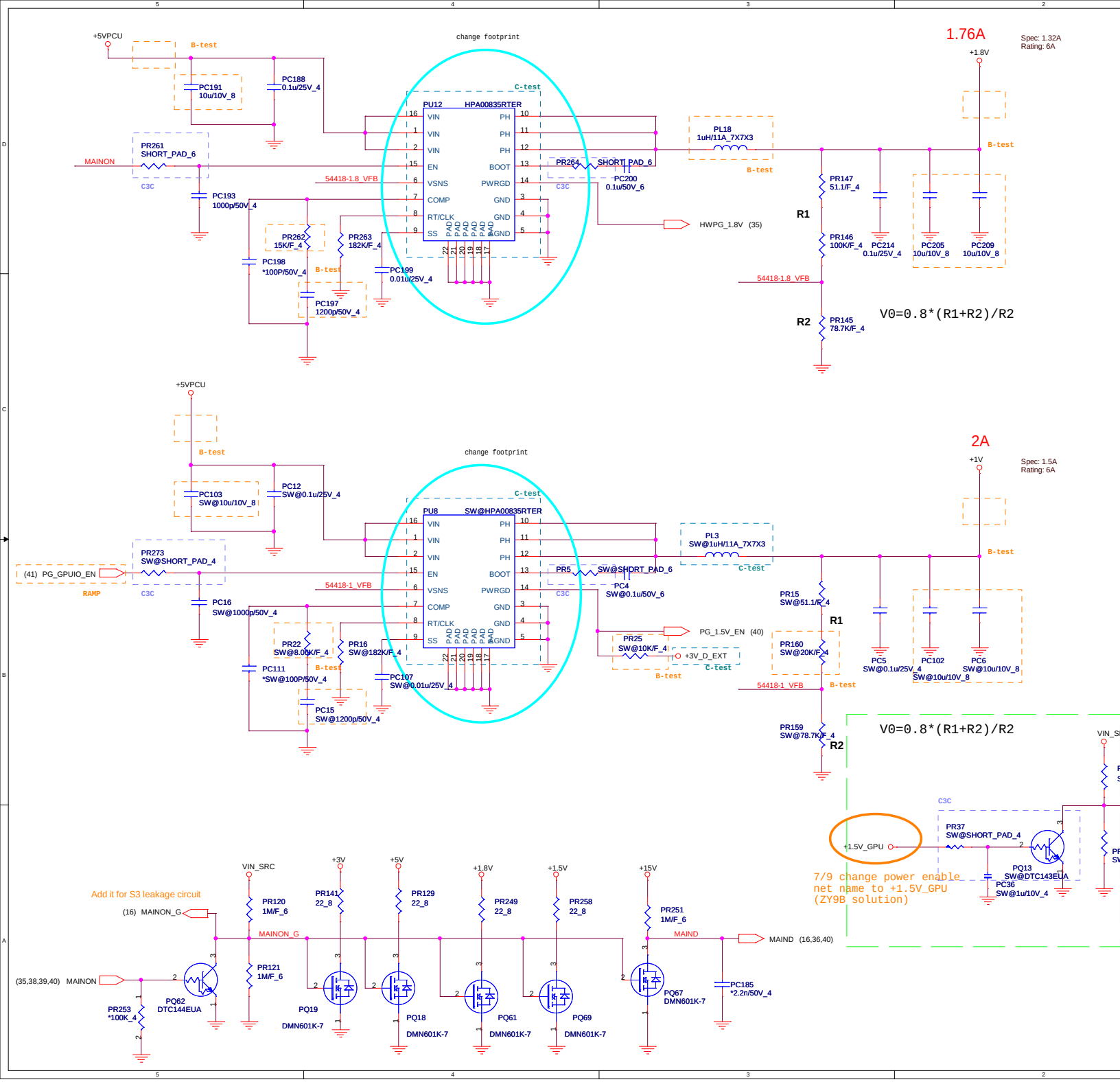
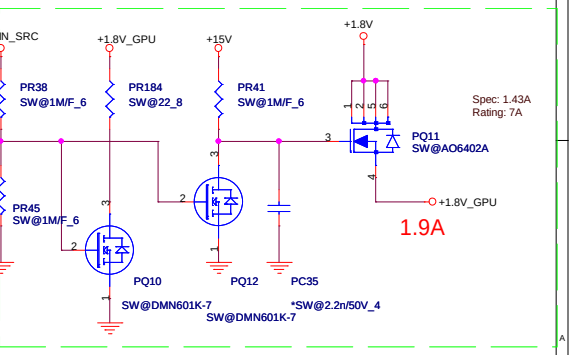
PROJECT : ZQ1

t Number FX_AXG (ISL62881)	Rev 1A

March 30, 2010 | Sheet 43 of 48


1.76A
Spec: 1.32A
Rating: 6A
+5VPCU
B-test
PC191
10u/10V_8
PC188
0.1u/25V_4
change footprint
C-test
PU12
HPA00835RTER
VIN
PH
EN
BOOT
VSNS
PWRGD
COMP
GND
RT/CLK
SS
AGND
PAD
PR261
SHORT_PAD_6
MAINON
C3C
PC193
1000p/50V_4
54418-1.8_VFB
PR262
15K/F_4
PR263
182K/F_4
PC198
*100P/50V_4
PC199
0.01u/25V_4
PC197
1200p/50V_4
PR264
SHORT_PAD_6
PC200
0.1u/50V_6
PL18
1uH/11A_7X7X3
HWPG_1.8V (35)
+1.8V
PR147
51.1/F_4
R1
PR146
100K/F_4
PC214
0.1u/25V_4
PC205
10u/10V_8
PC209
10u/10V_8
PR145
78.7K/F_4
R2
V0=0.8*(R1+R2)/R2
2A
Spec: 1.5A
Rating: 6A
+1V
PC103
SW@10u/10V_8
PC12
SW@0.1u/25V_4
PU8
SW@HPA00835RTER
PR273
SW@SHORT_PAD_4
(41) PG_GPUIO_EN
RAMP
PC16
SW@1000p/50V_4
54418-1_VFB
PR22
SW@8.06K/F_4
PR16
SW@182K/F_4
PC111
*SW@100P/50V_4
PC107
SW@0.01u/25V_4
PC15
SW@1200p/50V_4
PR5
SW@SHORT_PAD_6
PC4
SW@0.1u/50V_6
PL3
SW@1uH/11A_7X7X3
PG_1.5V_EN (40)
PR25
SW@10K/F_4
+3V_D_EXT
PR15
SW@51.1/F_4
PR160
SW@20K/F_4
PR159
SW@78.7K/F_4
PC5
SW@0.1u/25V_4
PC102
SW@10u/10V_8
PC6
SW@10u/10V_8
V0=0.8*(R1+R2)/R2
+1.5V_GPU
PR37
SW@SHORT_PAD_4
PQ13
SW@DTC143EUA
PC36
SW@1u/10V_4
7/9 change power enable
net name to +1.5V_GPU
(ZY9B solution)
Add it for S3 leakage circuit
(16) MAINON_G
VIN_SRC
PR120
1M/F_6
MAINON_G
PR121
1M/F_6
(35,38,39,40) MAINON
PR253
*100K_4
PQ62
DTC144EUA
+3V
PR141
22_8
PQ19
DMN601K-7
+5V
PR129
22_8
PQ18
DMN601K-7
+1.8V
PR249
22_8
PQ61
DMN601K-7
+1.5V
PR258
22_8
PQ69
DMN601K-7
+15V
PR251
1M/F_6
MAIND
PQ67
DMN601K-7
PC185
*2.2n/50V_4
MAIND (16,36,40)

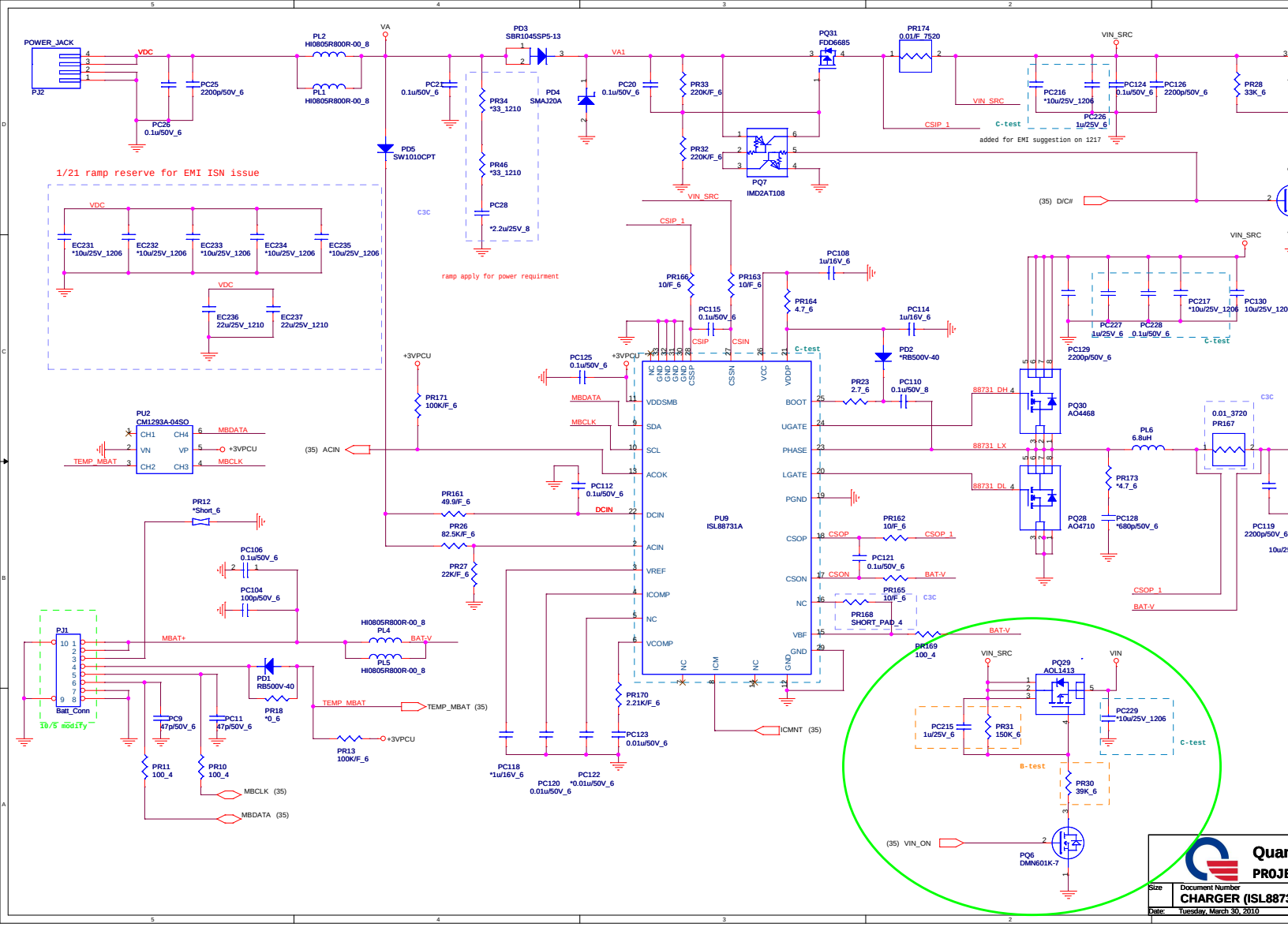


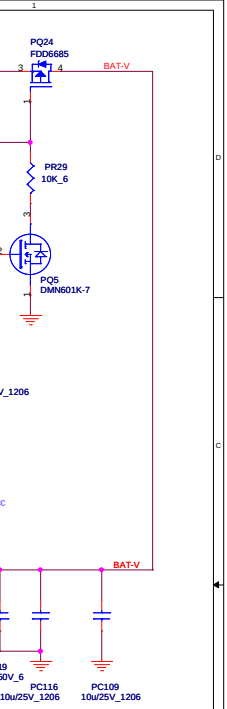
Quanta Computer Inc.

PROJECT : ZQ1

Size	Document Number	Rev
	Discharge/1.8V)	1A

Date: Tuesday, March 30, 2010 Sheet 44 of 48


POWER_JACK
PJ2
VDC
PC25 2200p/50V_6
PC26 0.1u/50V_6
PL2 HI0805R800R-00_8
PL1 HI0805R800R-00_8
VA
PD3 SBR1045SP5-13
VA1
PC21 0.1u/50V_6
PR34 *33_1210
PR46 *33_1210
PC28 *2.2u/25V_8
PD4 SMAJ20A
PD5 SW1010CPT
C3C
PC20 0.1u/50V_6
PR33 220K/F_6
PR32 220K/F_6
PQ31 FDD6685
PQ7 IMD2AT108
PR174 0.01/F_7520
VIN_SRC
CSIP_1
PC216 *10u/25V_1206
PC124 0.1u/50V_6
PC126 2200p/50V_6
PC226 1u/25V_6
C-test
added for EMI suggestion on 1217
PR28 33K_6
(35) D/C#
1/21 ramp reserve for EMI ISN issue
EC231 *10u/25V_1206
EC232 *10u/25V_1206
EC233 *10u/25V_1206
EC234 *10u/25V_1206
EC235 *10u/25V_1206
EC236 22u/25V_1210
EC237 22u/25V_1210
ramp apply for power requirment
PR166 10/F_6
PR163 10/F_6
PC115 0.1u/50V_6
PC108 1u/16V_6
PR164 4.7_6
PC114 1u/16V_6
PD2 *RB500V-40
PC227 1u/25V_6
PC228 0.1u/50V_6
PC217 *10u/25V_1206
PC130 10u/25V_120
PC129 2200p/50V_6
+3VPCU
PC125 0.1u/50V_6
PR171 100K/F_6
PU2 CM1293A-04SO
MBDATA
MBCLK
TEMP_MBAT
(35) ACIN
PC112 0.1u/50V_6
DCIN
PR161 49.9/F_6
PR26 82.5K/F_6
PR27 22K/F_6
PR12 *Short_6
PC106 0.1u/50V_6
PC104 100p/50V_6
PU9 ISL88731A
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
VBF
GND
CSSN
VCC
VDDP
ICM
PR23 2.7_6
PC110 0.1u/50V_8
88731_DH
88731_LX
88731_DL
PQ30 AO4468
PQ28 AO4710
PL6 6.8uH
PR173 *4.7_6
PC128 *680p/50V_6
0.01_3720
PR167
PC119 2200p/50V_6
10u/25
PR162 10/F_6
PC121 0.1u/50V_6
PR165 10/F_6
PR168 SHORT_PAD_4
BAT-V
PR169 100_4
PJ1
Batt_Conn
10/5 modify
MBAT+
HI0805R800R-00_8 PL4
PL5 HI0805R800R-00_8
PD1 RB500V-40
PR18 *0_6
PC9 47p/50V_6
PC11 47p/50V_6
PR11 100_4
PR10 100_4
PR13 100K/F_6
TEMP_MBAT (35)
MBCLK (35)
MBDATA (35)
PR170 2.21K/F_6
PC123 0.01u/50V_6
PC118 *1u/16V_6
PC120 0.01u/50V_6
PC122 *0.01u/50V_6
ICMNT (35)
PQ29 AOL1413
PC215 1u/25V_6
PR31 150K_6
PC229 *10u/25V_1206
B-test
PR30 39K_6
(35) VIN_ON
PQ6 DMN601K-7
Quan
PROJE
Size
Document Number
CHARGER (ISL8873
Date: Tuesday, March 30, 2010



uanta Computer Inc.
OJECT : ZQ1
88731)
Rev 1A
Sheet 45 of 48

PROJECT :ZH3
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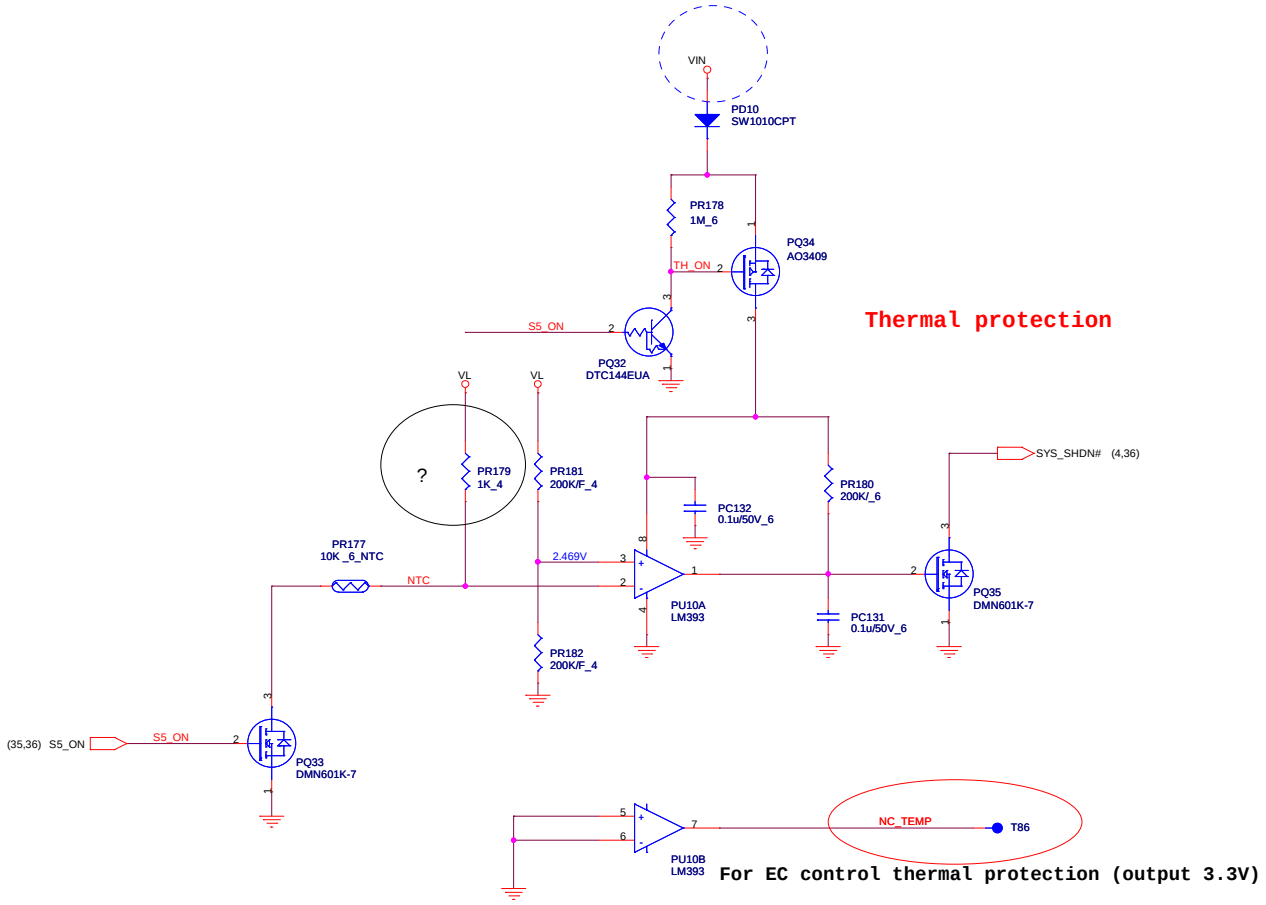

Quanta
PROJECT

Size	Document Number	
	Thermal Protection	
Date:	Tuesday, March 30, 2010	

ta Computer Inc.

CT : ZQ1

ion

Rev 1A

Sheet 46 of 48

Model	REV	CHANGE LIST	MODEL ZQ1 FROM	MODEL ZQ1 To
ZQ1 MB	1A	Schematic first released.	X	1A
	2A	All TP footprint change to "TP3050"	1A	2A
		Delete all power jump besides JP3	1A	2A
		Page03. Change C772 to CH02706JB06	1A	2A
		Page04. Change R493,R205,R204,R156,R489,R486 to shortpad	1A	2A
		Page04. Change U35 to AJSLGZ50T07	1A	2A
		Page08. Change R351,R354,R353,R355,R622,R514,R513 to shortpad	1A	2A
		Page08. Change R248 to CS21002FB24	1A	2A
		Page09. Change R609 to shortpad	1A	2A
		Page09. Change U40 to AKE38ZP0N01	1A	2A
		Page10. Staff Y4,C695,C696,R512 for all sku, and change C695,C696 to CH01006JB08	1A	2A
		Page10. Change R235,R234,R620,R515,R516 to shortpad	1A	2A
		Page10. Add T114,T115	1A	2A
		Page10. Reserved BOARD_ID1~3. Add and reserve R629,R630,R31,R632,R633,R634.	1A	2A
		Page10. Change SMbus PU to +3V_S5	1A	2A
		Page11. Change R607,R556 to shortpad	1A	2A
		Page11. Staff R283 and unstaff R279 for all sku	1A	2A
		Page12. Staff R252 and delete R253	1A	2A
		Page12. Change R271 to CX08T121001	1A	2A
		Page16. Change Q32 to BAM70020002	1A	2A
		Page19. Change R69 to CS05102JB35 and swap C203 and R64	1A	2A
		Page20. Add and staff Q38,C806,C807,C808. Add and reserve R635,R636 for +3V_D_EXT to separate internal and external power domain.	1A	2A
		Page22. Add and reserve R637.	1A	2A
		Page25. Change L39,L40,L41 to CX8LL470000, C598,C596,C578,C579,C597,C599 to CH-6806TB01. Staff C572	1A	2A
		Page25. Change CN4 to DFHS08FR774. Change netname PANEL_ENG to DCR_EN and delete PANEL_COLOR	1A	2A
		Page25. Modify dGPU_SELECT# circuit for leakage and change R37 to CS41002JB20	1A	2A
		Page26. Add HDMI_HPD_PCH# to PCH GPIO13. Add and reserve R639	2A	3A
		Page26. Change Q30 to BAM70020002	2A	3A
		Page27. Change U27 to AL008151003	2A	3A
		Page27. Change R523 to shortpad	2A	3A
		Page27. Add R648 to AVDDH for EMI	2A	3A
		Page28. Change CN1 to DFFC10FR138 and add USB port5. Add and reserve R640,R641	2A	3A
		Page28. Change Q26,Q27 to 2N7002K	2A	3A
		Page29. Change HOLE13,HOLE25 footprint	2A	3A
		Page30. Staff R565 and delete R568	2A	3A
		Page30. Change R315,R319 to CS05602JB17	2A	3A
		Page30. Change U30 footprint to TRF-10-1-24P-smt	2A	3A
		Page31. CN10 change to DFHD39MR001	2A	3A
		Page31. R525,R233 change to CX08T121000	2A	3A
		Page32. Change U33 to AL003510000	2A	3A
		Page32. Unstaff R229,R231,R295,R296,R297,R298,R363,R346 and staff L24,L28,L29,L32 DC09004A014	2A	3A
		Page32. Change CN9 to DFWF05MR042	2A	3A
		Page32. Change SW2,SW3 pin5,6 to GND	2A	3A
		Page32. Change C688 to CC73301MZ00	2A	3A
		Page33. Add and reserve C809	2A	3A
		Page33. Add and reserve R642. Add Q39 for RF_LED function	2A	3A
		Page33. Change CN3 to DFFC06FR255 and add P_SAVE_LED. Add R643,R644 CS41002JB20	2A	3A
		Page34. Add and reserve C810	2A	3A
		Page34. Change C344 to CH4104K9B03, C349 to CH31004KB17	2A	3A
		Page35. Add J3 and unstaff SW1	2A	3A
		Page35. Staff C347 CH31006K919	2A	3A
		Page35. Change R474,R477,R455,R453 to shortpad	2A	3A
		Page35. Add and reserve R645. Add VGA_THERM# to GPU thermal sensor	2A	3A
		Page35. Add RE_LED_EN# and RE_LED# for LED function. Add and reserve R647	2A	3A
		Page35. Delete PANEL_COLOR and add T116,R646	2A	3A
		Page35. Change U29 to AKE38FP0N01	2A	3A
		Page36. Change PC190,PC194 to CH73301M8B9, PC180 to CH61004M291	2A	3A
		Page36. Change PR139 to CS41502FB18, PR131 to CS42003F919, PR136 to CS41823F914, PR142 to CS21002FB24	2A	3A
		Page37. Change PU5 footprint to qfn40-5x5-4-41p-0_75h-smt	3A	3B
		Page37. Change PC75,PC74,PC71,PC72 to CH61004M291, PL11,PL12 to CV+18V0MZ04	3A	3B
		Page38. Change PR43 to CS23923F910, PL9,PL10 to CV-2280MZ05	3A	3B
		Page39. Change PR269 to CS23903F911	3A	3B
		Page40. Unstaff PC77. Change PR109 to CS24993F949, PL14 to CV-15K0MZ05, PC86,PC169 to CH61004M291	3A	3B
		Page41. Change PR1 to CS44702FB13, PR9 to CS34422FB00, PR14 to CS34992FB10, PR19 to CS42202FB10, PR157 to CS36202FB19	3A	3B
		Page41. Change PL7 to CV+18V0MZ04, PC101,PC105,PC113 to CH61004M291, PC17,PC18 toCH733RY8802	3A	3B
		Page42. Change PC33,PC31 to CH61004M291	3A	3B
		Page42. Change PU4 footprint to TQFN20-1_8X3_2-4-SMT	3A	3B
		Page42. Unstaff PQ9,PR62,PR64,PR72,PR80	3A	3B
		Page43. Change PC150,PC151 to CH61004M291, PC153 to CH34702KB10	3A	3B
		Page43. Change PU11 footprint to QFN28-4X4-4-29P-smt	3A	3B
		Page44. Add PU8,PR160 "SW@" and remove PL18 "SW@"	3A	3B
		Page44. Change PC191,PC013 to CH6102K9A19, PC197,PC15 to CH21206KB13, PR262 to CS31502FB08, PR22 to CS28062FB21	3A	3B
		Page44. Change PC102,PC6,PC205,PC209 to CH6102K9A19, PC197,PC15 to CH2126K1B05, PR262 to CS31502FB24, PR22 to CS28062FB21	3A	3B
		Page44. Change PL18 footprint to CHOKE-PCMC063T-3R3MN-NB4	3A	3B
		Page44. Change and staff PR25 to CS21002FB24	3A	3B
		Page44. Add PR273 and unstaff PR24	3A	3B
		Page45. Add PC215 CH5104K9906	3A	3B
		Page45. Change PR30 to CS33903J914, PR31 to CS41503J932	3A	3B
	3A	Page08. Delete R514,R513 and add R653,R654,R655 for EMI	3A	3B
		Page09. Staff R249,R245 and unstaff R255,R254. U40 change to AKE391P0N00	3A	3B
		Page10. Change R290,R316,R285,R291 to shortpad	3A	3B
		Page12. Change C390 to CH6221M9A07 for CRT garbage issue.	3A	3B
		Page18. Delete T75,T76,T78,T79,T77,T80,T82,T83 and add R656,R657,R658 for EMI	3A	3B
		Page22. Update VRAM strapping table	3A	3B
		Page25. Staff L1 DC09004A014 and unstaff R17,R18 for EMI	3A	3B
		Page25. Add F1 DK100TPU028 for safety. Add R666 for EMI	3A	3B
		Page25. Add R667,R668,R669 for CRT garbage		
		Page26. Delete R436,Q12, and R143,Q11 remove SW@		
		Page26. Add and reserve R665,R664,Q43,Q44 for HDMI logo, F2 for safety		

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Quanta Computer Inc.
PROJECT : ZQ1
Size | Document Number: Change list | Rev 1A
Date: Thursday, January 29, 2009 | Sheet 47 of 48

Model	REV	CHANGE LIST	MODEL	ZQ1 FROM	ZQ1 To
ZQ1 MB	3A	Page27. Unstaff R648. Add and reserve L60,L61,L62,L63,L64,L65,L66,L67,C811,C812,C813,C814,C815,C816,C817,C818 for EMI		X	1A
		Page27. Change U32 footprint to qfn40-5x5-4-41p-0_8h		X	1A
		Page28. Change R547,R549,R553,R557,R561,R267,R266,R418,R423,R421 to shortpad		1A	2A
		Page30. Change R565 to shortpad		1A	2A
		Page31. Change R571,R550 to shortpad		1A	2A
		Page31. Change CN10 to DFHD36MS006		1A	2A
		Page32. Change L22 footprint to CHOKE-WCM2012-4P		1A	2A
		Page33. Modfiy W L LED schematic. Add R649. Add and reserve R650		1A	2A
		Page33. Change R369,R370,R371 to CS03902JB21, and R365,R361,R367 to CS-4702JB29		1A	2A
		Page33. Add Q40 and change P_SAVE_LED netname to P_SAVE_LED#		1A	2A
		Page33. Move symbol from D/B to M/B. Add Q41,Q42,R651,R652,R659,R660,R661,R662,R663 and change R663 to CS16802JB27		1A	2A
		Page33. Change R123 to shortpad		1A	2A
		Page34. Staff C513 CH5104K9906 and add C819 for EMI		1A	2A
		Page35. Change U29 to AKE37FN0N01		1A	2A
		Page36. Add PC220,PC221,PC222,PC223. Add and reserve PC218,PC219,PC224,PC225 10uF for EMI		1A	2A
		Page38. Change PU3 footprint to mlpq16-3x3-5-17p-smt		1A	2A
		Page38. Add L68,L69 for CRT noise		1A	2A
		Page39. Change PU13 footprint to mlpq16-3x3-5-17p-smt		1A	2A
		Page41. PR6 PU change to +3V_D_EXT		1A	2A
		Page44. PR25 PU change to +3V_D_EXT		1A	2A
		Page44. Change PU8,PU12 footprint to mlpq16-3x3-5-17p-smt and PL3 to CHOKE-PCMC063T-3R3MN-NB4		1A	2A
		Page45. Change PU9 footprint to QFN28-5X5-5-33P-smt		1A	2A
		Page45. Add PC226,PC227,PC228. Add and reserve PC216,PC217,PC229 10uF for EMI		1A	2A
	3B	Page10. Staff R632		1A	2A
		Page10. Change Y4 to BG625000788		1A	2A
		Page25. Change L39,L40,L41 to CX8BA470003 and C598,C599,C596,C597,C578,C579 to CH01006JB08		1A	2A
		Page26. Staff Q43,Q44,R664,R665 and unstaff R435,R434		2A	3A
		Page38. L68,L69 change to CX09T170000		2A	3A
	3C	Remove +VGPU_IO schematic		2A	3A
		Page04. Change R188 to shortpad		2A	3A
		Page08. Delete R653,R654,R655		2A	3A
		Page10. Update Board_ID table and staff R629 for ZQ1		2A	3A
		Page10. Delete T51,T55,T61,T63,T100,T102,T115		2A	3A
		Page11. Delete TP5,TP6,TP7,TP8		2A	3A
		Page12. Change R529,R526,R292,R539,R540,R309,R230,R294,R322,R325,R314,R246,R238,R338,R337,R578,R288,R269,R252 to shortpad		2A	3A
		Page12. Unstaff R286 and change C445 to CS00002JB38		2A	3A
		Page16. Change R513,R139,R158,R159 to shortpad		2A	3A
		Page18. Delete R656,R657,R658		2A	3A
		Page20. Change R19 to shortpad		2A	3A
		Page25. Swap F1 and D7 location		2A	3A
		Page25. Delete R17,R18,R667,R668,R669		2A	3A
		Page25. Change R106,R81,R99,R38,R39,R12,R409 to shortpad		2A	3A
		Page25. Change R666 to CX05T121000		2A	3A
		Page26. Change R638,R439 to shortpad		2A	3A
		Page27. Change R522 to shortpad		2A	3A
		Page28. Change R423,R418,R421 to 0ohm		2A	3A
		Page28. Change R280 to shortpad		2A	3A
		Page29. Change R227,R137 to shortpad		2A	3A
		Page30. Add Q45,Q46,Q47,R653 for vendor suggestion		2A	3A
		Page30. Change R468,R471 to CX08T221000 and C663,C670 to CH06806J901 for EMI		2A	3A
		Page30. Swap CN12 pin define		2A	3A
		Page30. Change R535,R532,R543 to shortpad		2A	3A
		Page31. Change R546 to shortpad		2A	3A
		Page32. Change R225.R228 to shortpad. Delete R229,R231,R295,R296,R297,R298,R363,R346,L22 co-layout parts.		2A	3A
		Page33. Change R649 to shortpad		2A	3A
		Page34. Change R386 to shortpad		2A	3A
		Page35. Change R466,R646 to shortpad		3A	3B
		Page36. Change PR123,PR126,PR127,PR128,PR130,PR132,PR133,PR134,PR138,PR254,PR259,PR260 to shortpad		3A	3B
		Page37. Change PR70,PR78,PR79,PR106,PR107,PR185,PR195,PR199,PR200,PR202 to shortpad		3A	3B
		Page38. Add PC230 CH41006K911		3A	3B
		Page38. Change L68,L69,PR36,PR39,PR183 to shortpad		3A	3B
		Page39. Change PR266,PR267,PR271 to shortpad		3A	3B
		Page40. Change PR99,PR102,PR112,PR114 to shortpad		3A	3B
		Page41. Change PR152,PR154 to shortpad		3A	3B
		Page42. Change PR219,PR220,PR223,PR234,PR236,PR247 to shortpad		3A	3B
		Page43. Change PR5,PR37,PR261,PR264,PR273 to shortpad		3A	3B
		Page43. Change PQ13 to BA001430Z49		3A	3B
		Page43. Delete PR24		3A	3B
		Page44. Change PR168 to shortpad		3A	3B
		Page44. Add and reserve PR34,PR46,PC28 for power requirement		3A	3B
		Page44. Add EC236,EC237. Add and reserve EC231,EC232,EC233,EC234,EC235 for EMI		3A	3B
		Page44. Change PR167 footprint to RC3720-SMT		3A	3B
	3D	Update Block Diagram, PWR Status & Flow Chart		3A	3B
		Page03. Unstaff R300		3A	3B
		Page09. Staff R344		3A	3B
		Page10. Staff R634		3A	3B
		Page18. Unstaff R77,R73		3A	3B
		Page19. Unstaff R68 and staff R50 CS31002JB28		3A	3B
		Page27. Staff L60,L61,L62,L63,L64,L65,L66,L67 CVB4713TN09 and C811,C812,C813,C814,C815,C816,C817,C818 CH-5606TB01		3A	3B
		Page30. Change R315,R319 to CS07502JB27. Unstaff R653,Q45,Q46,Q47		3A	3B
		Page33. Change R660,R661,R662 to CS14532FB14, R663 to CS22202JB18, R369,R370,R371 to CS18062FB29, and R361,R365,R367 to CS05602JB17		3A	3B
		Page36. Change PD9 to BDDZS36BZ00		3A	3B
				3A	3B
				3A	3B
				3A	3B

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Quanta Computer Inc.
PROJECT : ZQ1
Size | Document Number | Rev 1A
Change list
Date: Monday, February 08, 2010 | Sheet 48 of 48