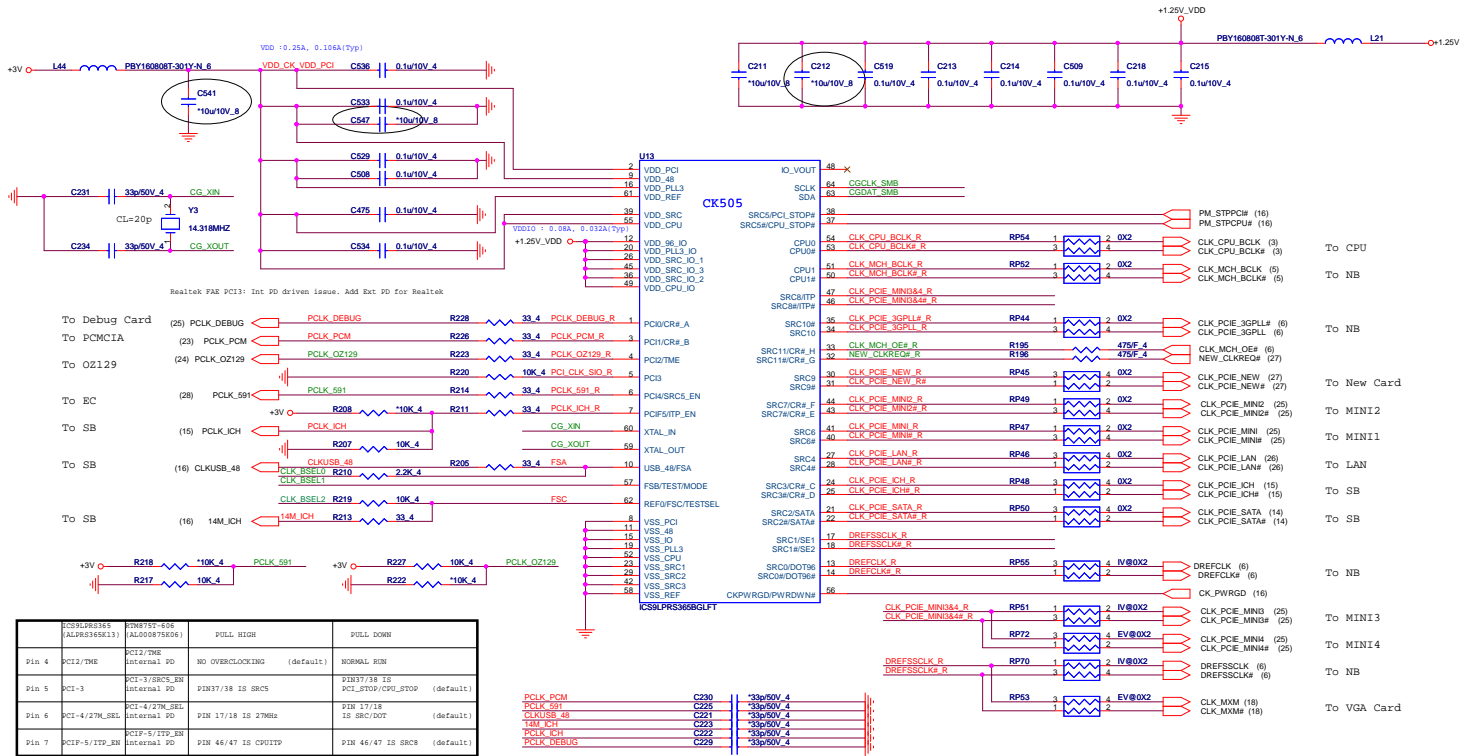
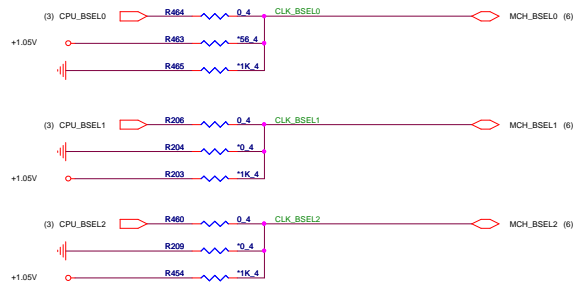


Clock Generator

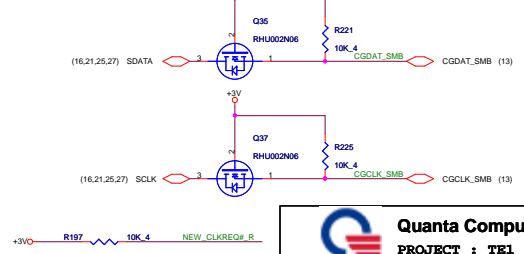


BSEL Frequency Select Table

FSC	F5B	F5A	Frequency
0	0	0	266MHz
0	0	1	133MHz
0	1	1	166MHz
0	1	0	200MHz
1	1	0	400MHz
1	1	1	Reserved
1	0	1	100MHz
1	0	0	333MHz



Clock Gen I2C



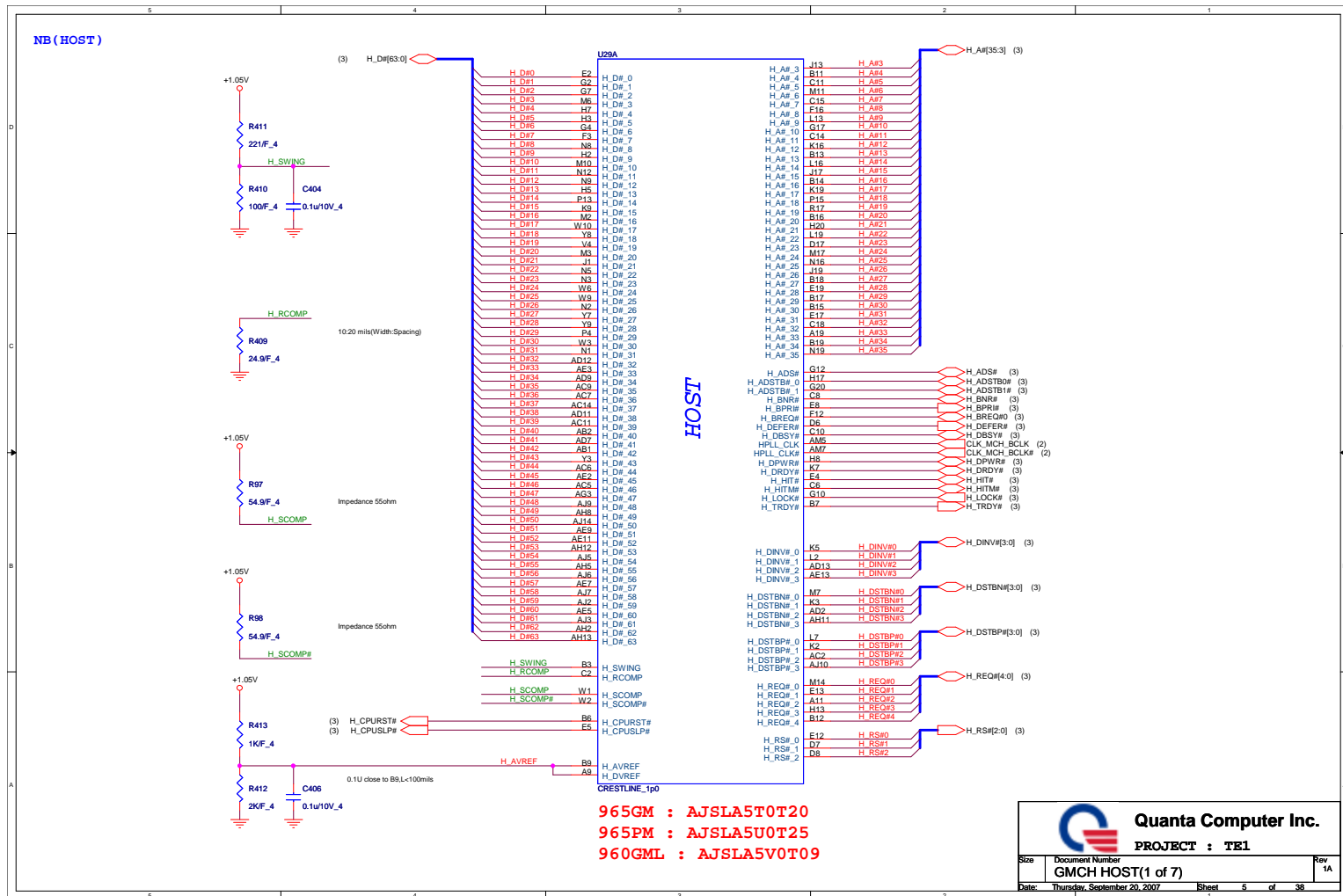
Quanta Computer Inc.

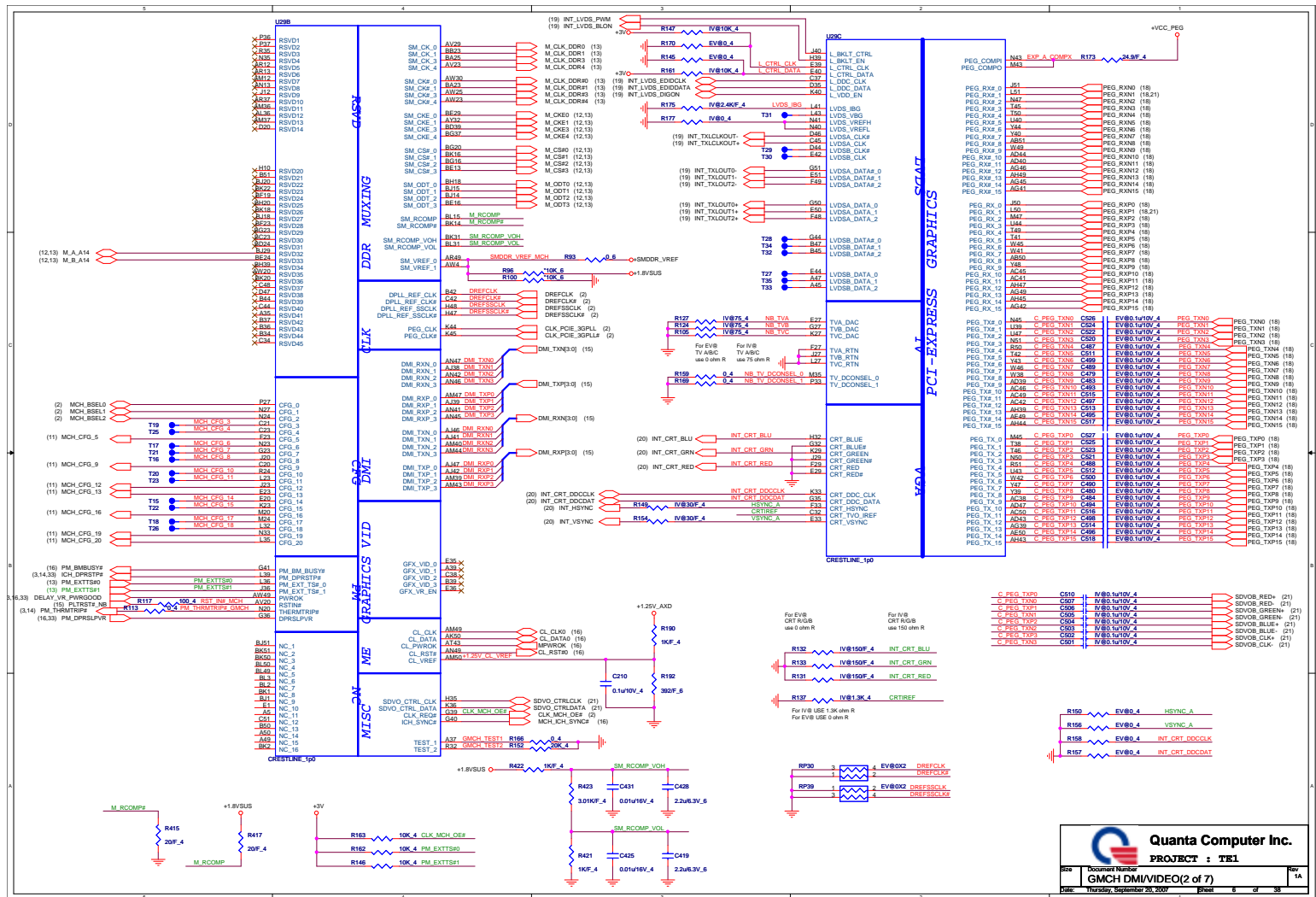
PROJECT : TB1

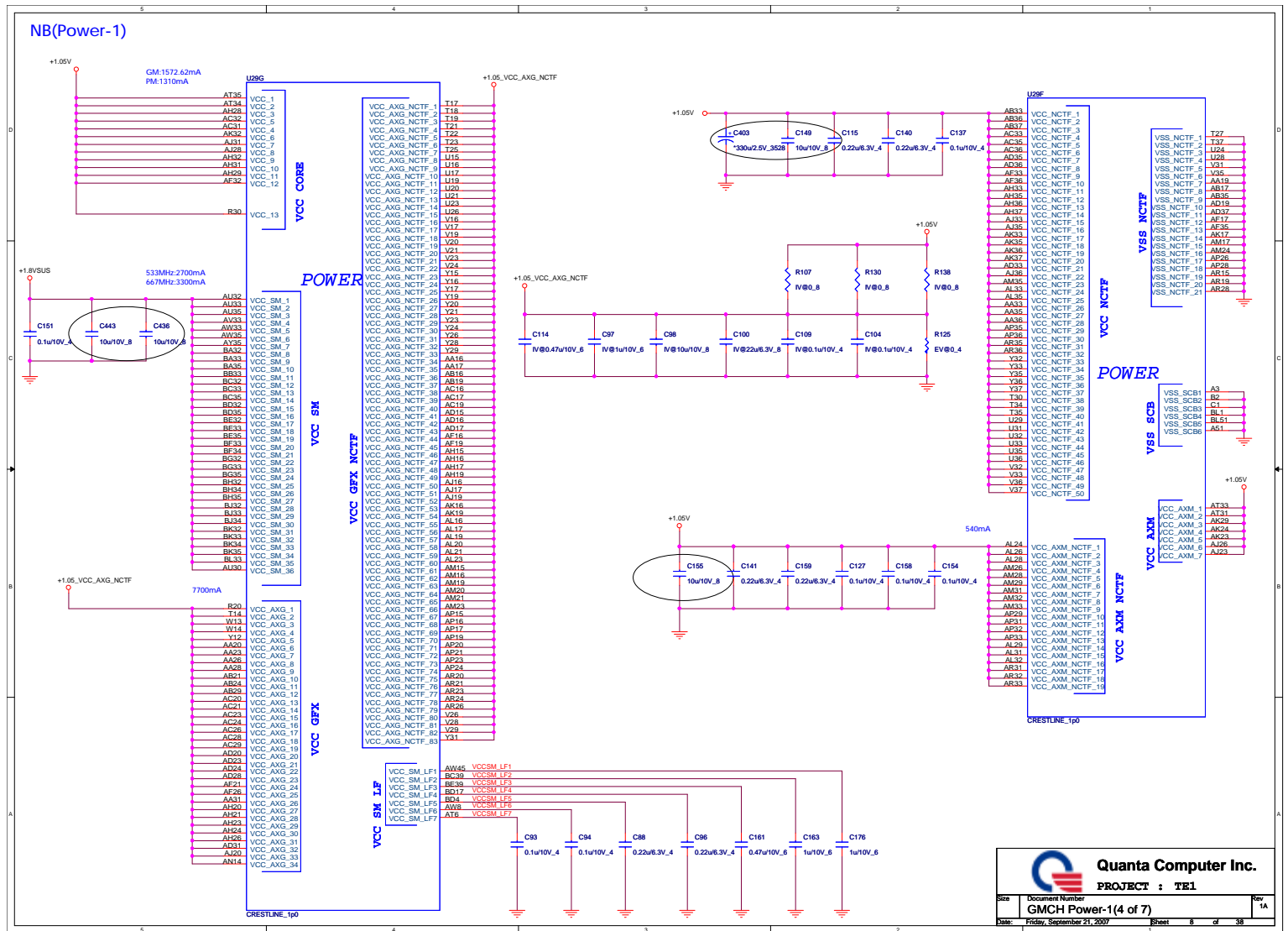
CLK_GEN / CK505

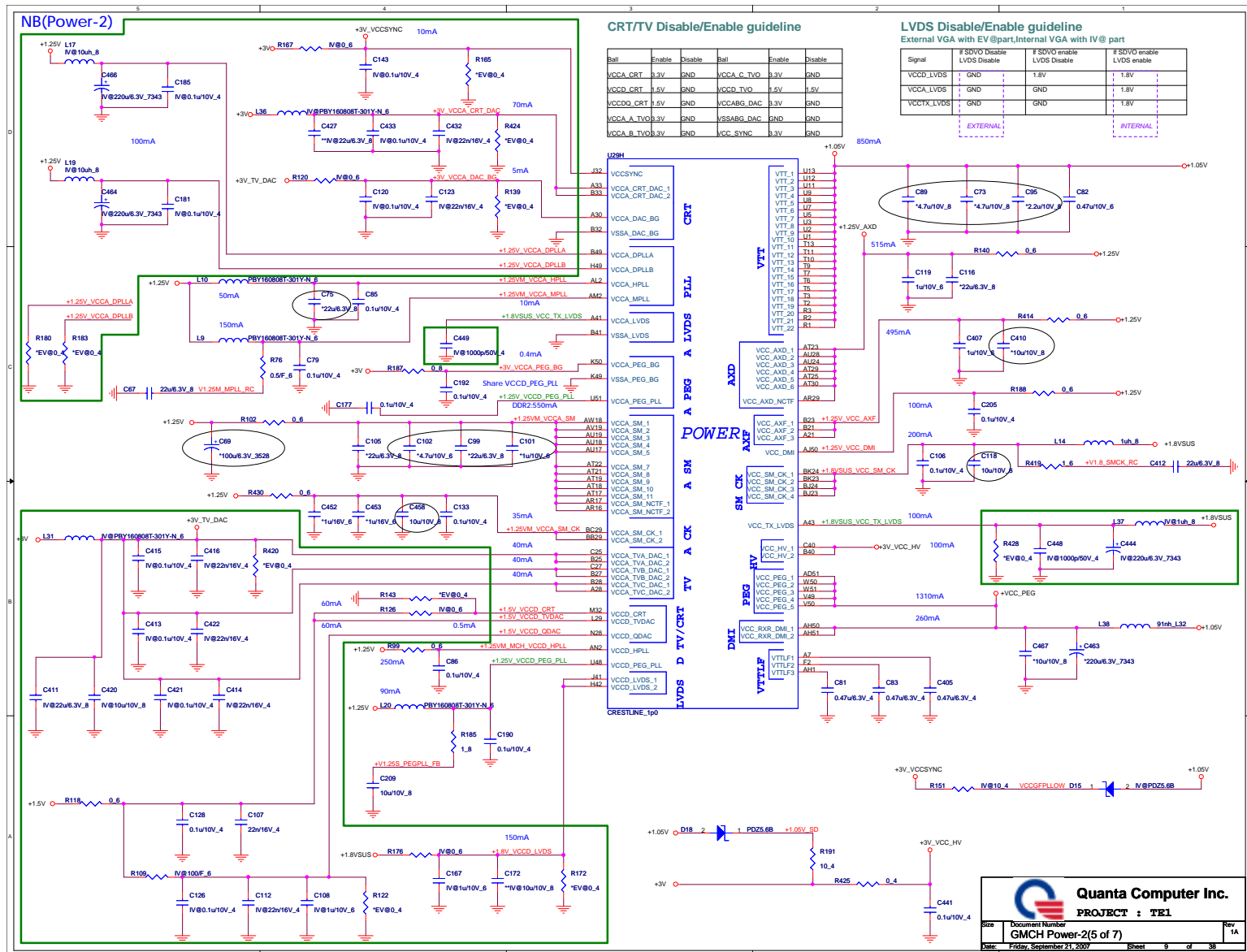
Site: _____ Document Number: _____ Rev: 1A

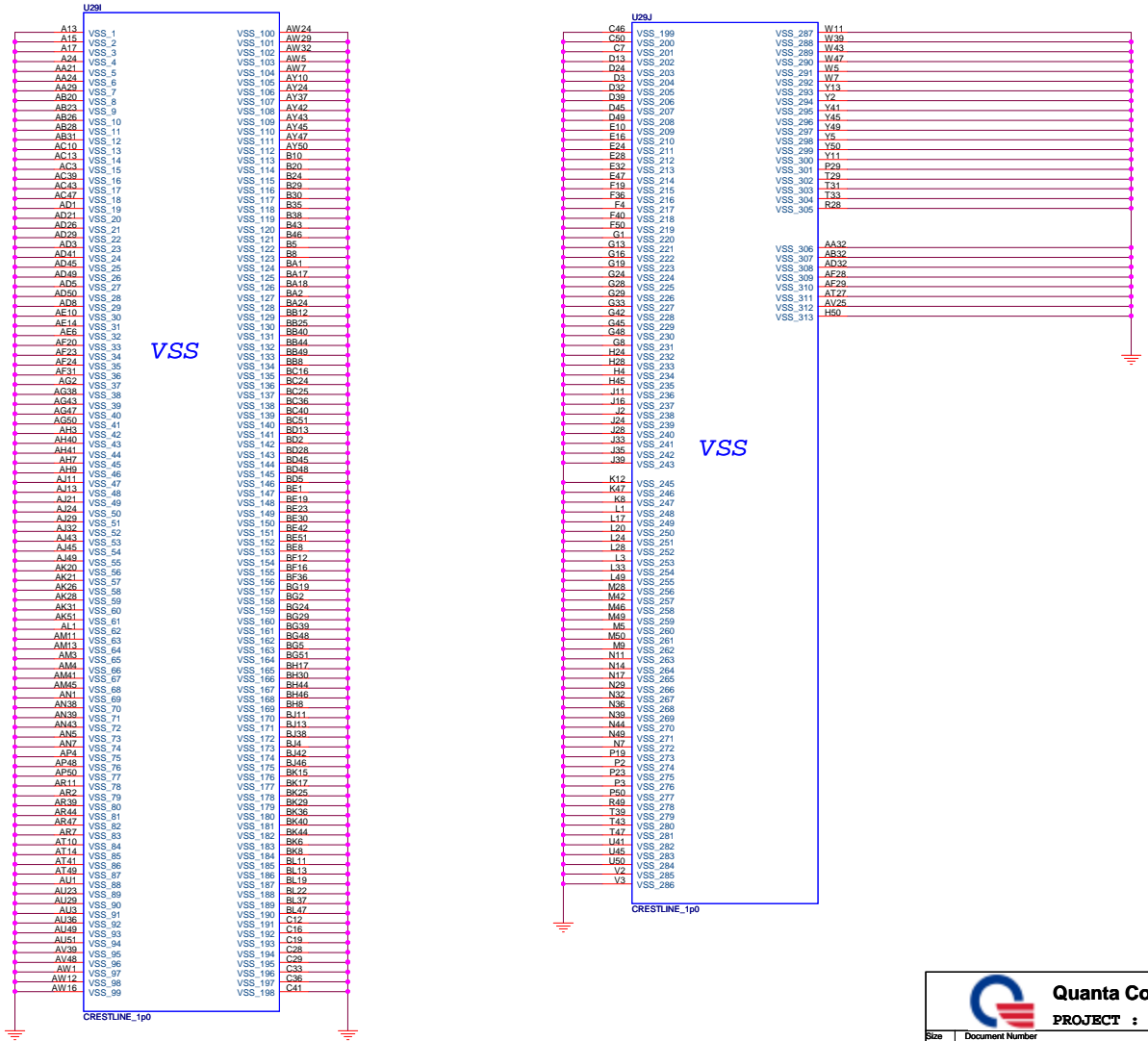
Date: Thursday, September 20, 2007 Sheet 2 of 38














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PROJECT : TE1

Size	Document Number	Rev
	GMCH Power-3(6 of 7)	1A
Date:	Thursday, September 20, 2007	Sheet 10 of 38

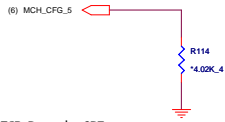
Strap table(base on checklist Ver1.6)

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) signal
 CFG[17:3] Have internal Pull-up
 CFG[18:19] Have internal Pull-down
 Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	Intel? Management Engine Crypto strap	0 = Intel? Management Engine Crypto Transport Layer.Security (TLS) cipher suite with no confidentiality 1= Intel Management Engine Crypto TLS Cipher Suite with confidentiality (default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE is operation(Default) 1 = SDVO and PCIE are operating simultaneously via the PEG port

DMI X2 Select

MCH_CFG_5	Low = DMI X2 High = DMI X4(Default)
-----------	----------------------------------------



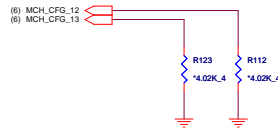
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane
------------	--------------------------------------------------------



XOR /ALLz /Clock Un-gating

MCH_CFG_2	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)
-----------	--------------------------------------------------------



SDVO Present

Strap define at External
HDMI control page

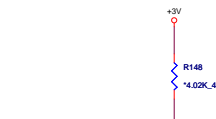
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)
------------	-------------------------------------------------



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE is operational(Default) High = SDVO and PCIE are operating simultaneously via the PEG port
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PROJECT : TE1

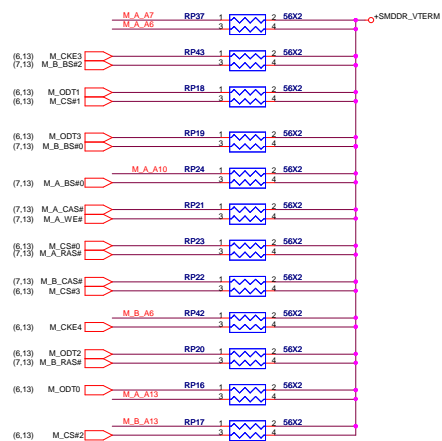
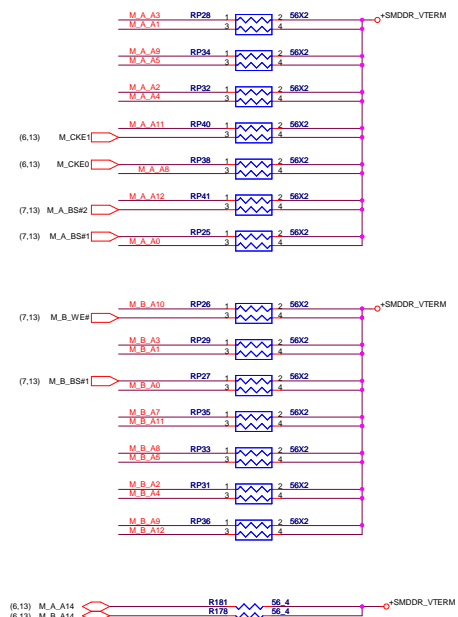
Site	Document Number	Rev	1A
GMCH Strap(7 of 7)			
Date	Thursday, September 20, 2007	Sheet	11 of 38

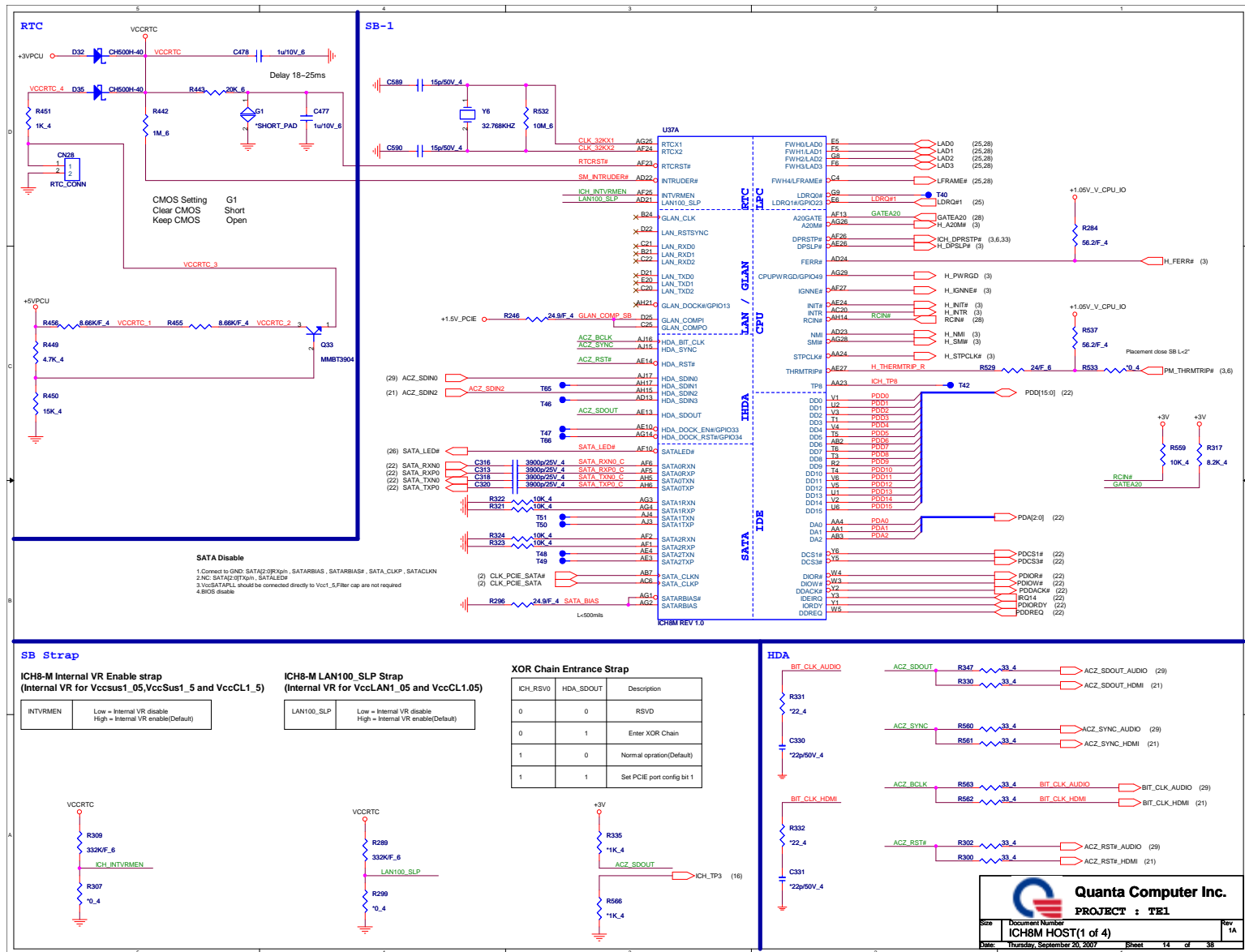
DDRII A CHANNEL

DDRII B CHANNEL



Place one cap close to every 2 pull-up resistor terminated to SMDOR_VTERM





[illegible][illegible]

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#	OZ129T
REQ1# / GNT1#	AD20	INTC#	CB1410

Low = A16 swap override enabled
High = Default

PCI_GNT#3

GNT3s R469 1K 4

ICH8 Boot BIOS select

PCI_GNT#0	SPL_CS#1	Boot BIOS Location
0	1	SPi(Default)
1	0	PCI
1	1	LPC

+3V
O

8.2KX8 +3V

USBOC#5	7		4	USBOC#3
USBOC#7	8		3	USBOC#8
USBOC#9	9		2	USBOC#2

8.2KX8

The circuit diagram shows a +3V DC voltage source connected to a network of resistors and a dependent current source. The network consists of a 10Ω resistor in series with a parallel combination of a 20Ω resistor and a branch containing a dependent current source (labeled $2i_x$) in series with a 10Ω resistor. The current i_x is defined as the current flowing through the 10Ω resistor in the top branch.

DEVSZ#	7		4	INTG#
FRAMES#	8		3	TRDY#
STOR#	9		0	BELOW

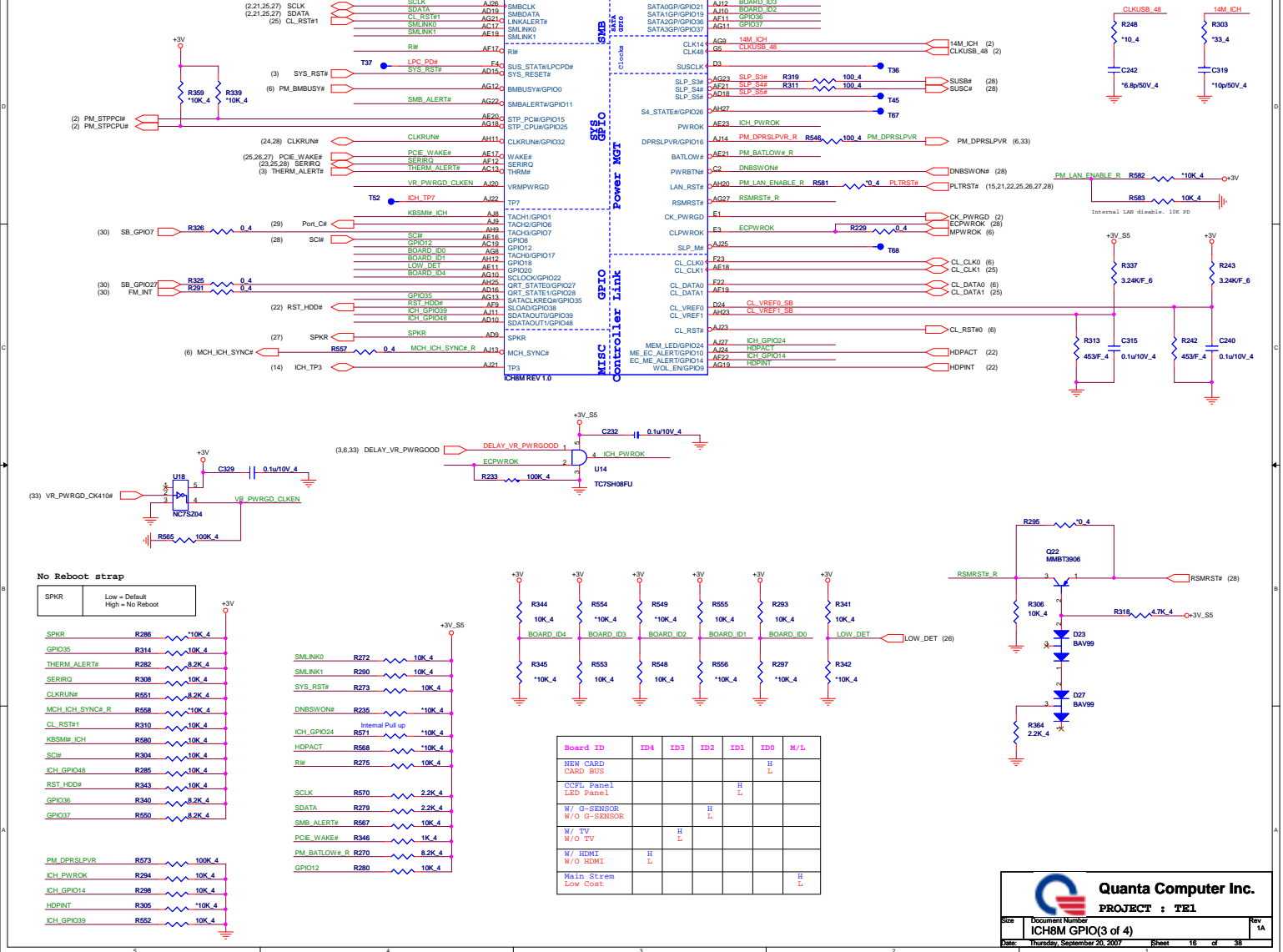
8.2KX8 +3V
RP74

IRDY#	8		3	INTC#
INTD#	9		2	INTA#
	10		4	PE/CY#

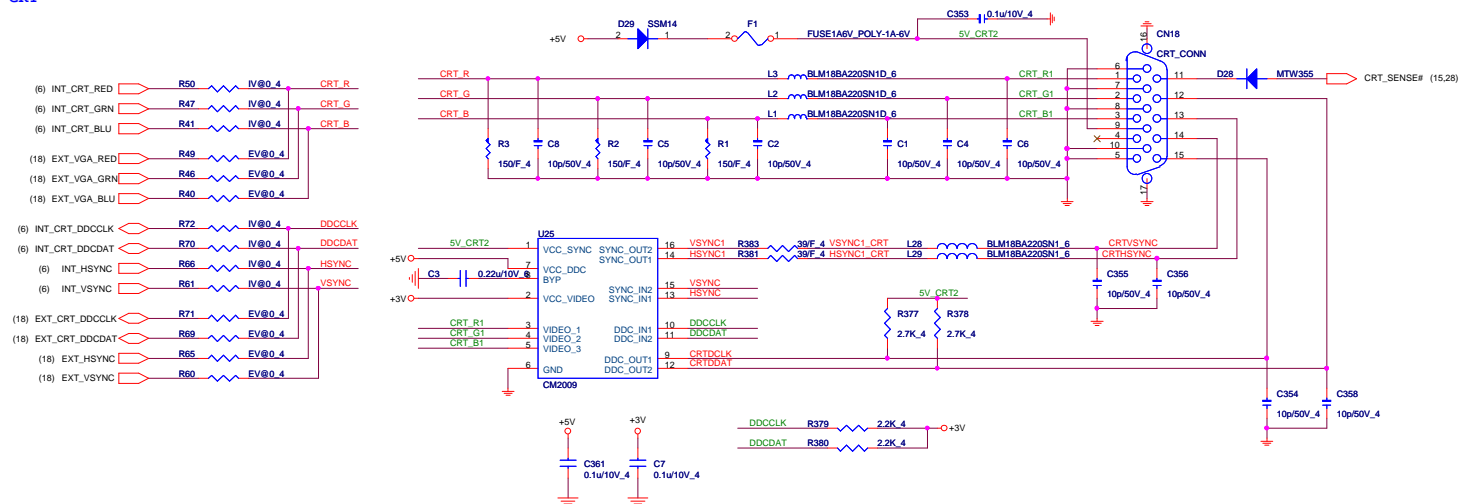
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Document Number
ICH8M PCIE(2 of 4)/ BIOS

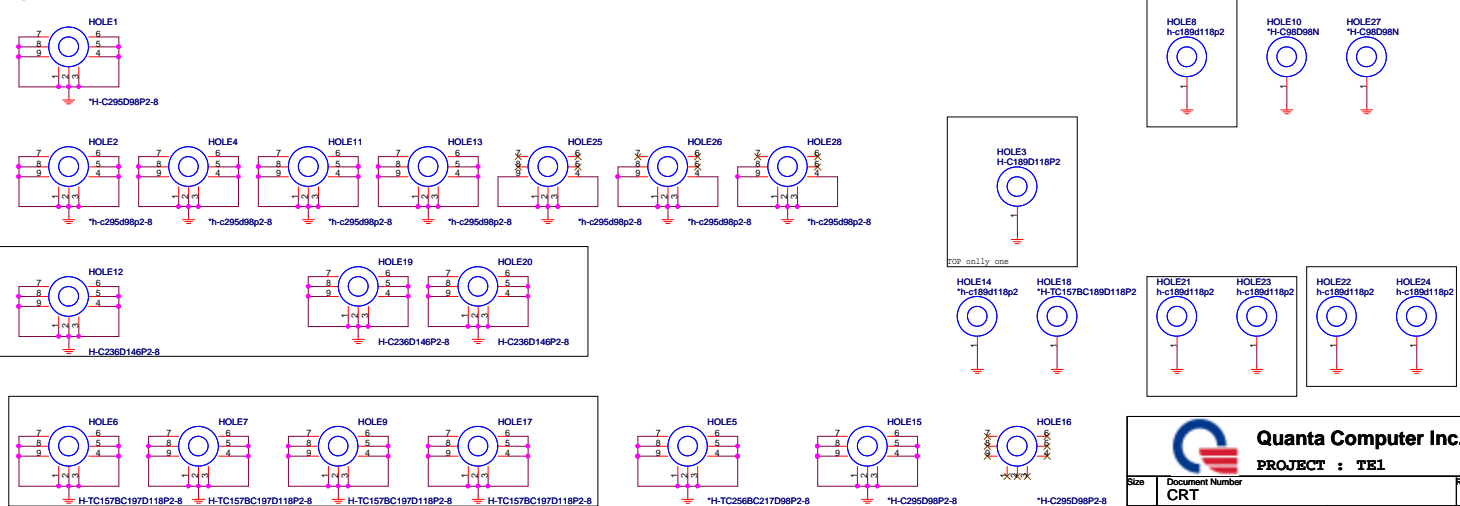
SB-GPIO

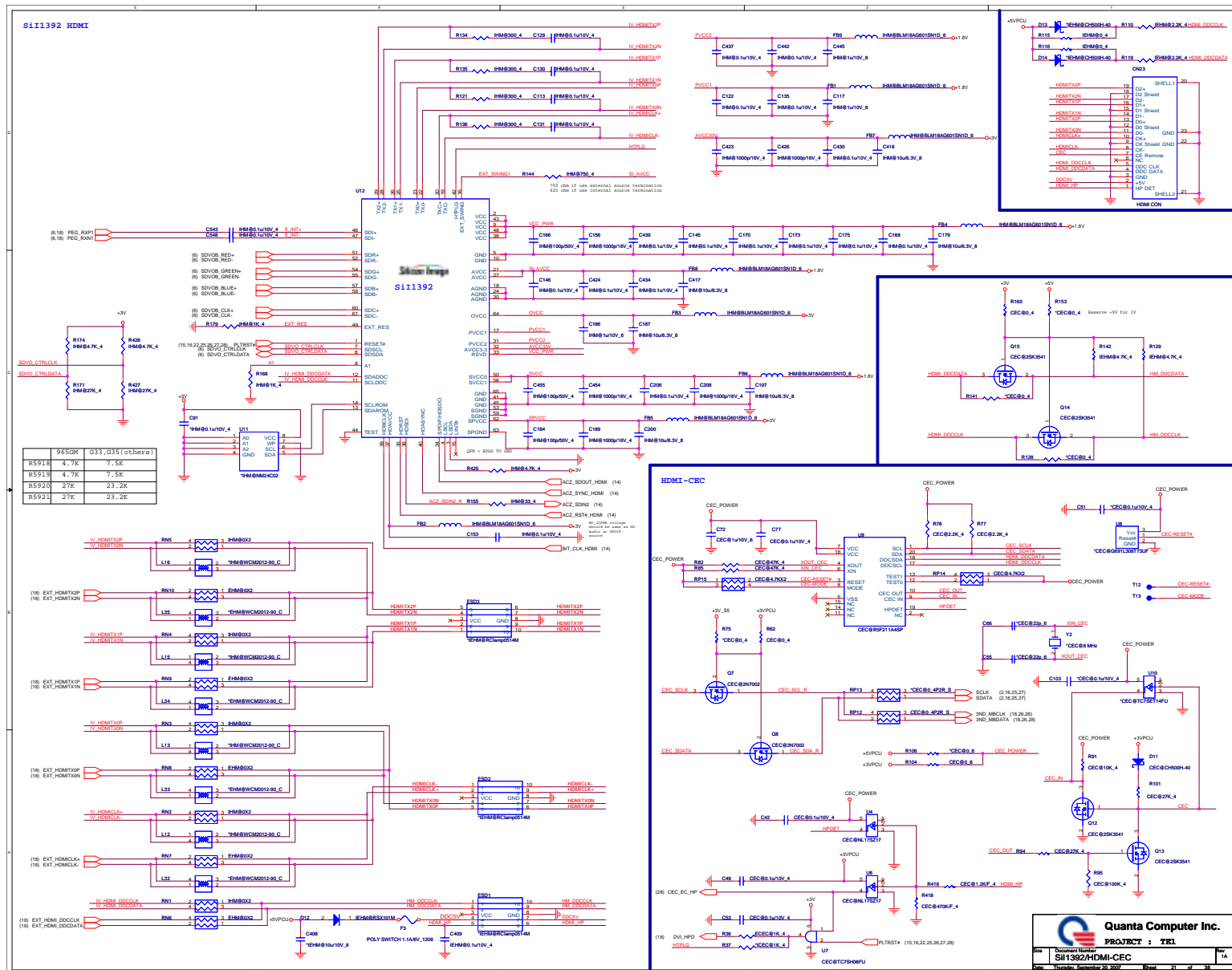


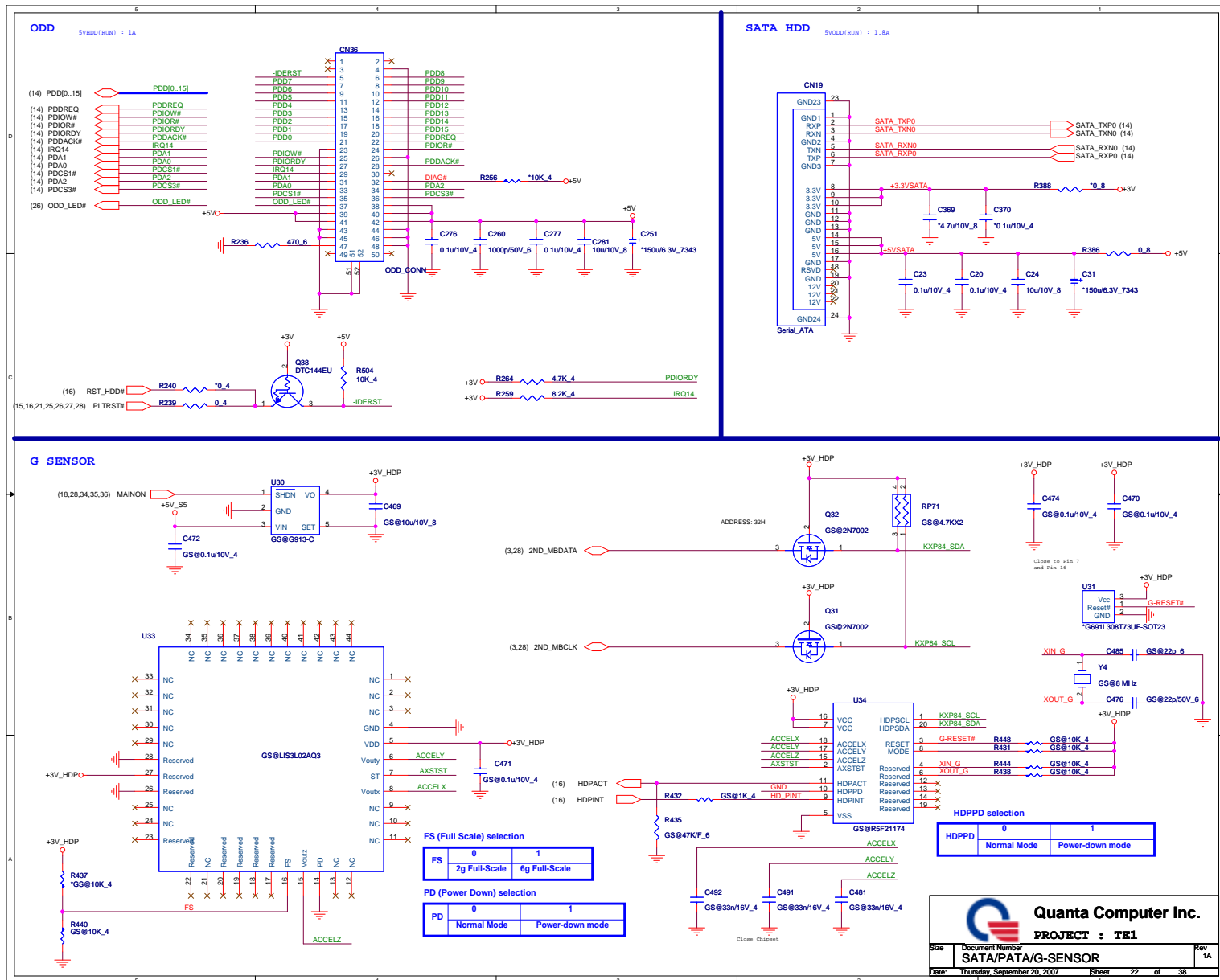
CRT



HOLE

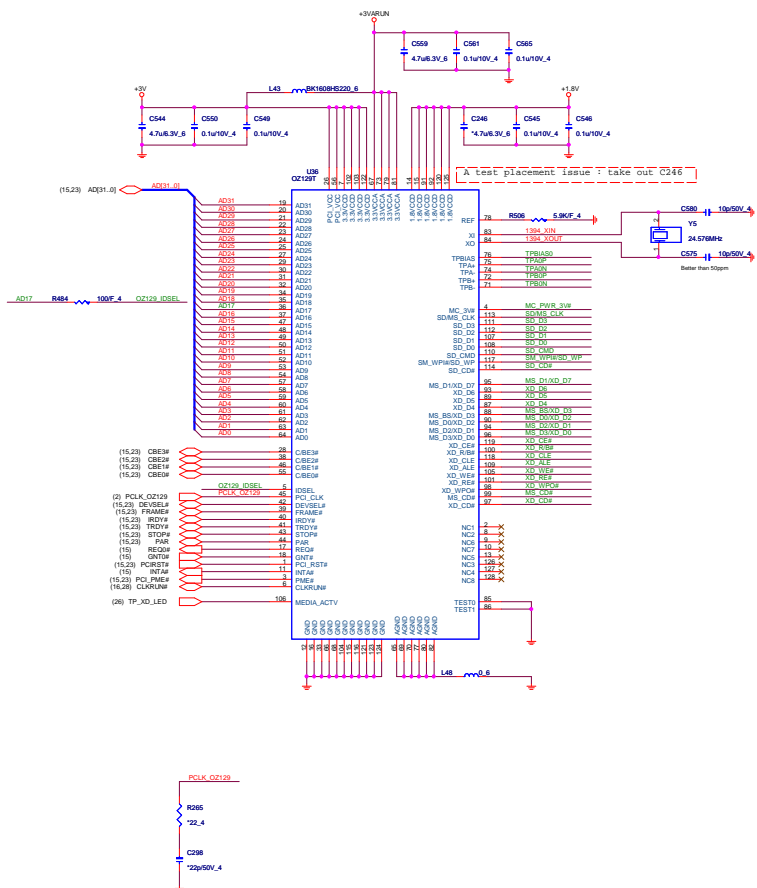




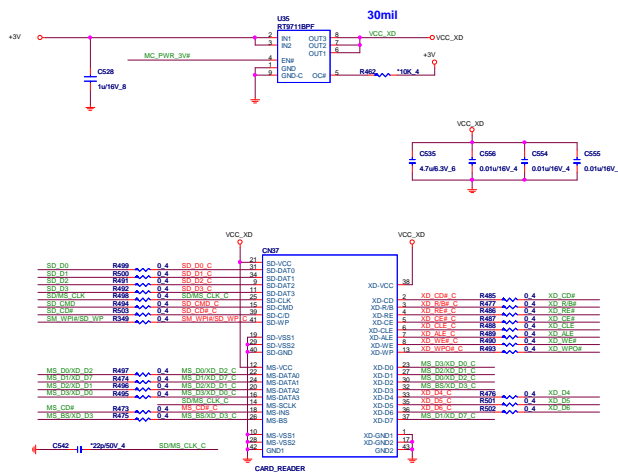


OZ129 for Cardreader+1394

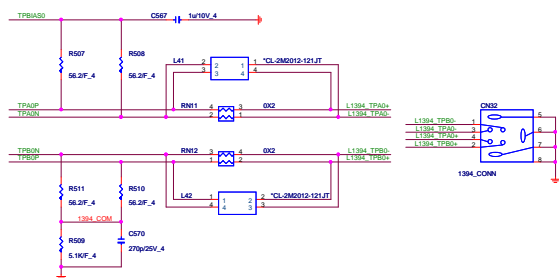
ID Select : AD17
Interrupt Pin : INTA#
Request Indicate : REQ#
Grant Indicate : GNT0#



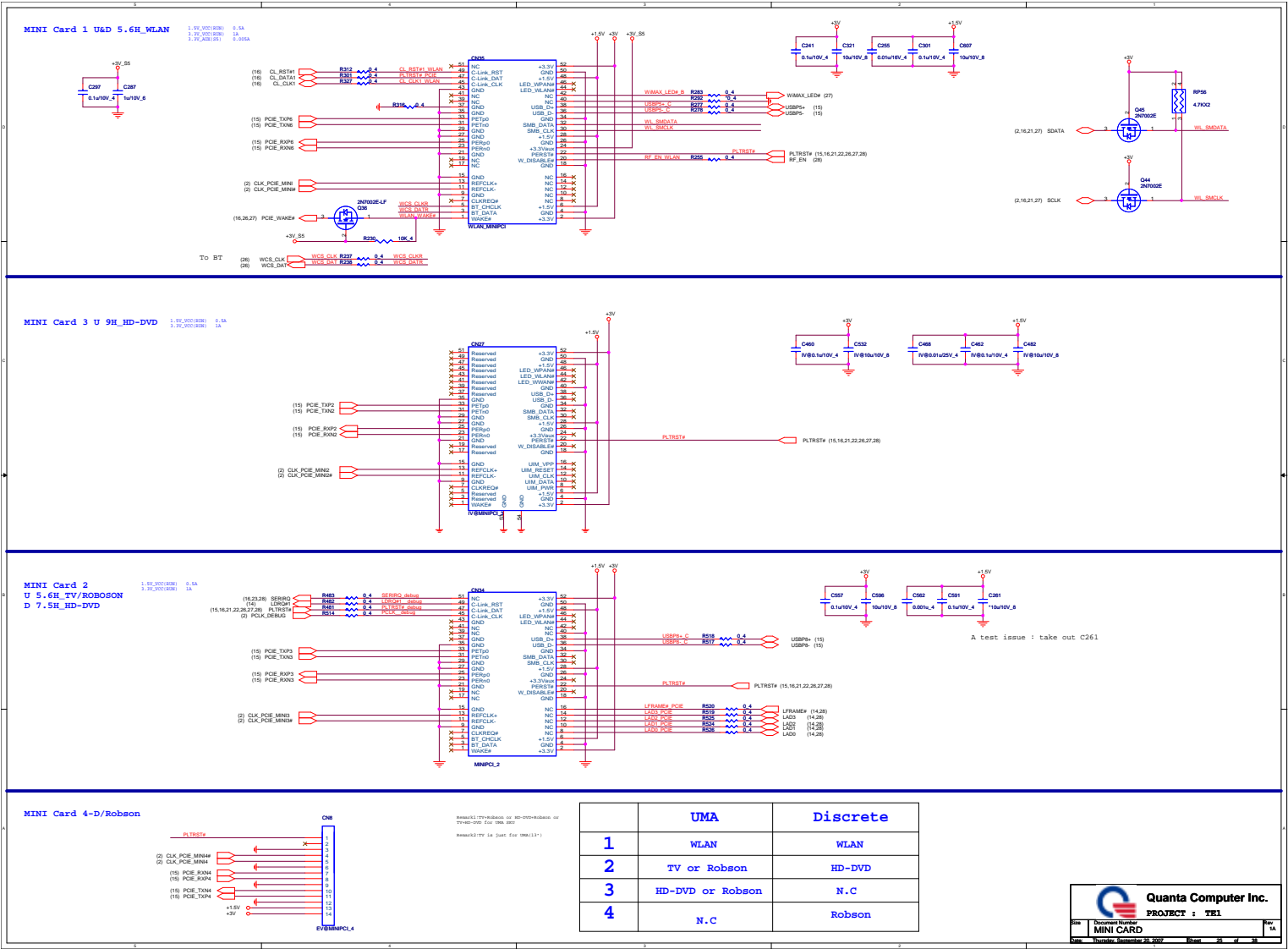
5 IN 1 Card reader

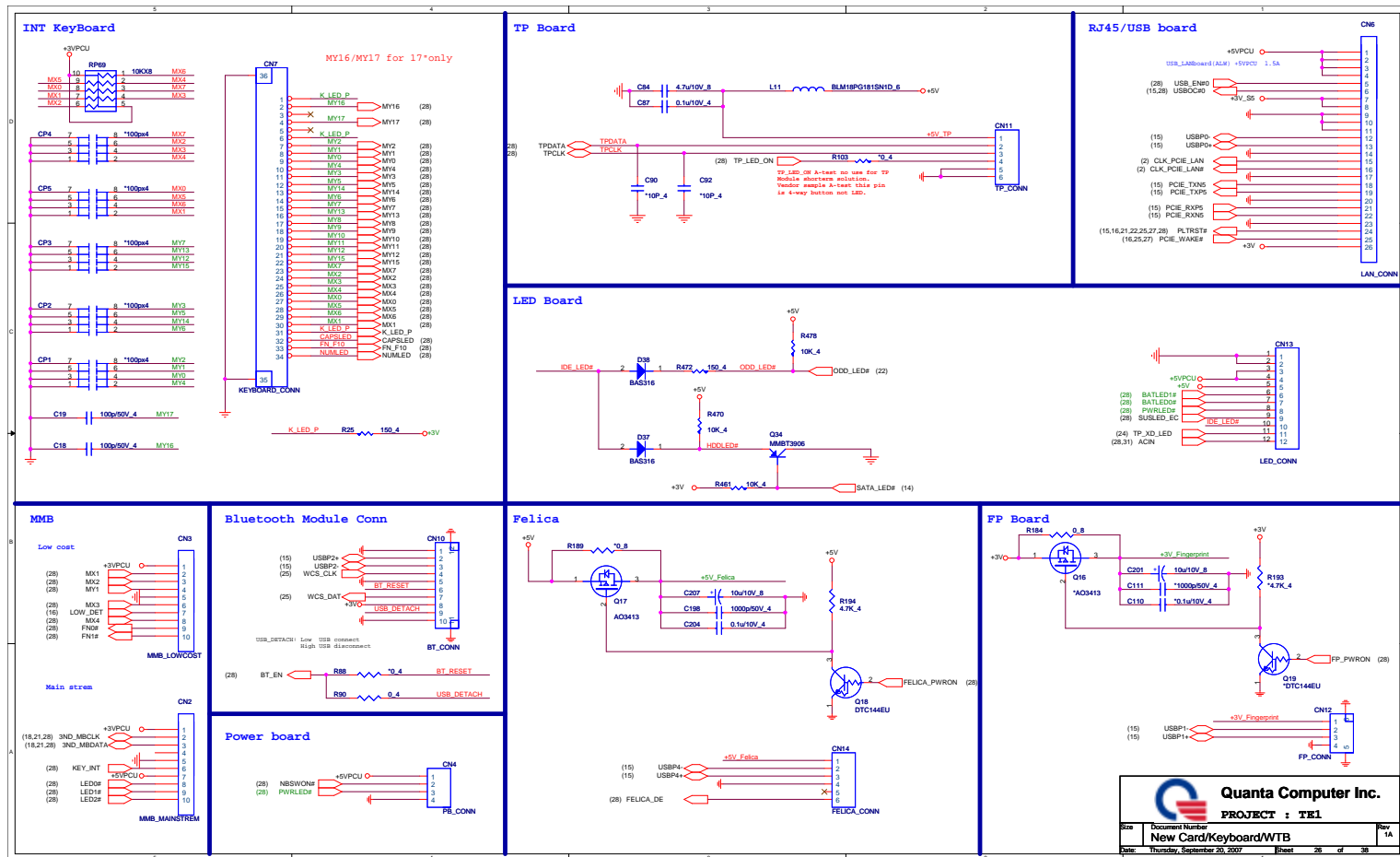


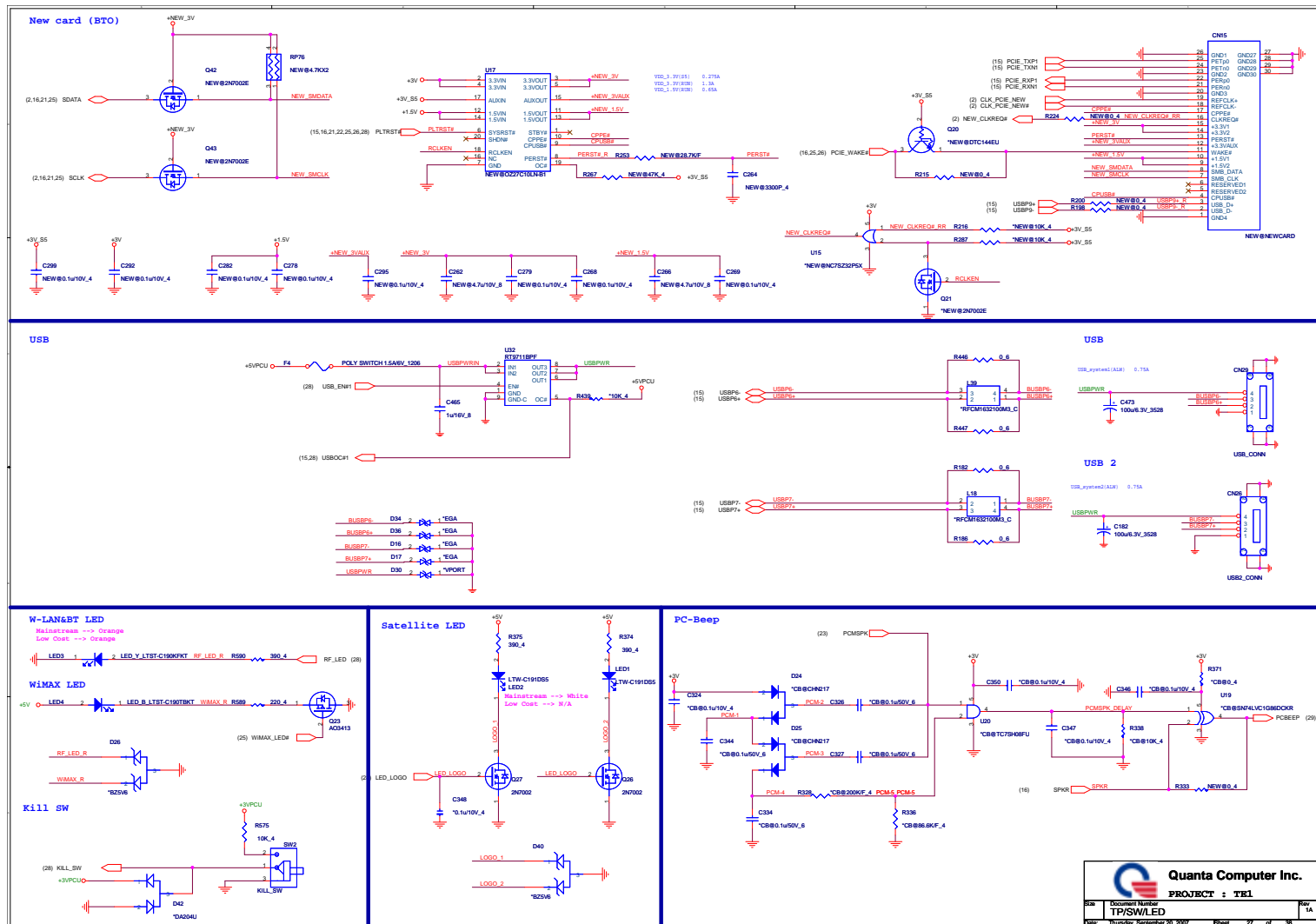
1394

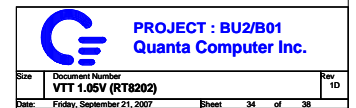


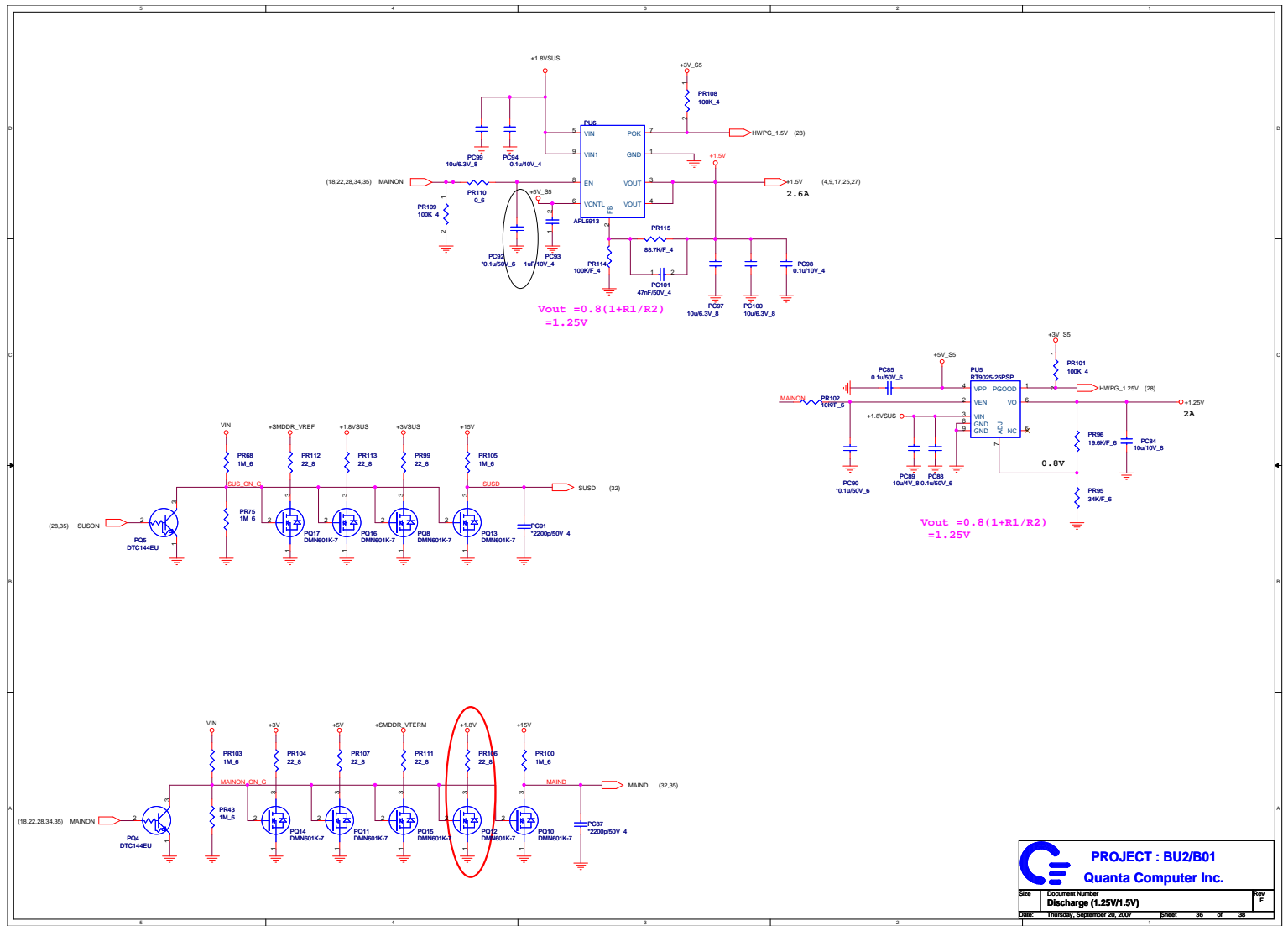
Quanta Computer Inc.
PROJECT : TE1
OZ129T(sm1/1394)
Date: Thursday, September 30, 2007 Page: 24 of 38












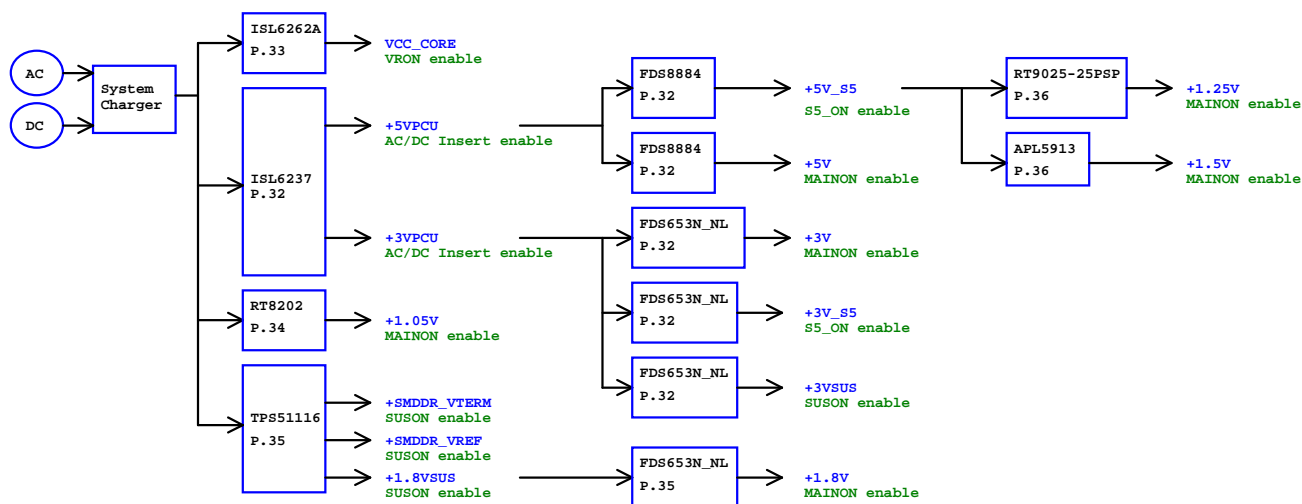
PROJECT : BU2/B01
Quanta Computer Inc.

Size	Document Number	Rev
	Discharge (1.25V/1.5V)	
Date	Thursday, September 26, 2007	Sheet 35 of 38

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Quanta Computer Inc.
PROJECT : TEL
 Size Document Number
 Change list
 Date: Monday, September 10, 2007 10:07 AM
 User: 10 10 10

Power Tree Table



Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/esATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+1.8VSUS	GMCH, DDR
+SMDDR_VREF	GMCH, DDR
+SMDDR_VTERM	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/esATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T)
+3V_S5	Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC
+3VSUS	ICH8M, Mini Card, RJ45/USB /B, New Card
+1.8V	HDMI, Cardreader (OZ129T)
+1.25V	CLK, GMCH, ICH8M