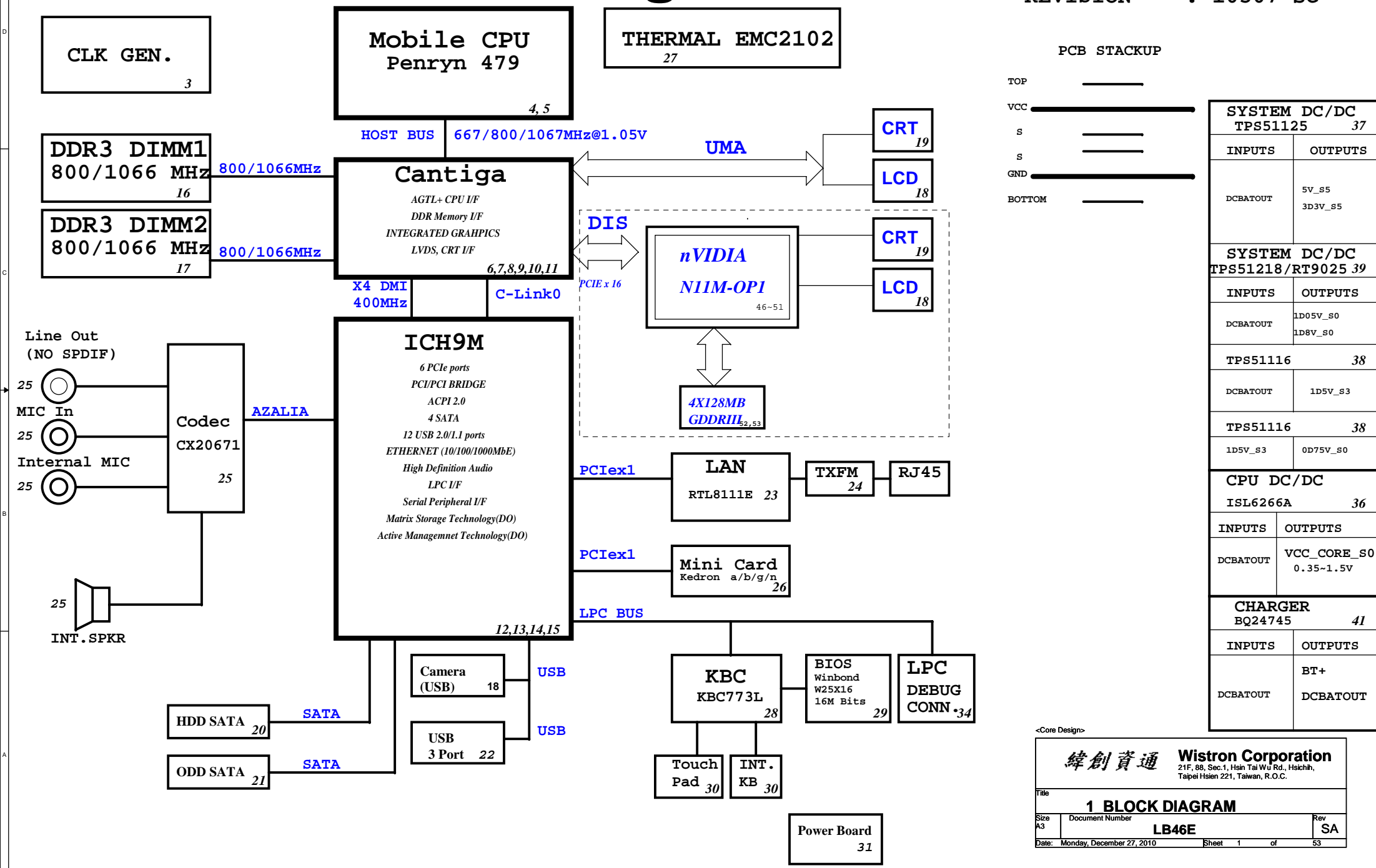


LB46E Block Diagram

Project code: 91.4HK01.A01

PCB P/N :

REVISION : 10307-sc



<Core Design>

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Title

1 BLOCK DIAGRAM

Size

A3

Document Number

LB46E

Rev

SA

Date: Monday, December 27, 2010

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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH [3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCie are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

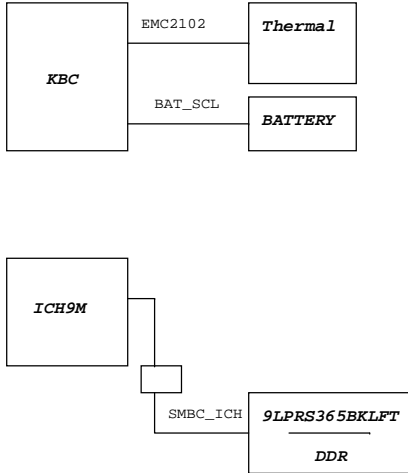
USB Table

USB	
Pair	Device
0	USB1
1	USB3
2	NC
3	MINIC1
4	WEBCAM
5	NC
6	NC
7	NC
8	NC
9	USB2
10	NC
11	NC

PCIE Routing

LANE1	RTL8111E
LANE2	MiniCard WLAN
LANE3	NC
LANE4	NC
LANE5	NC
LANE6	NC

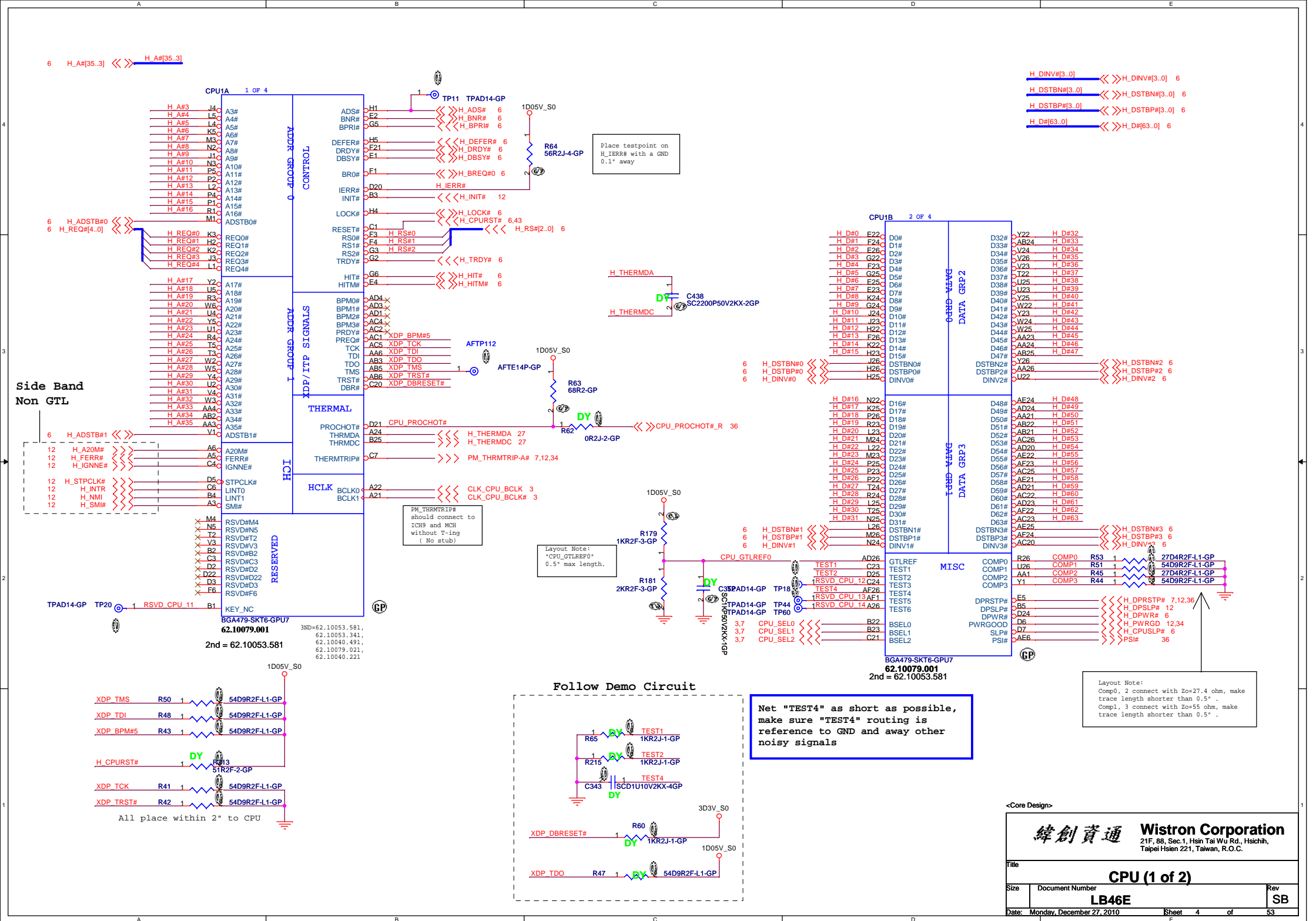
SMBus

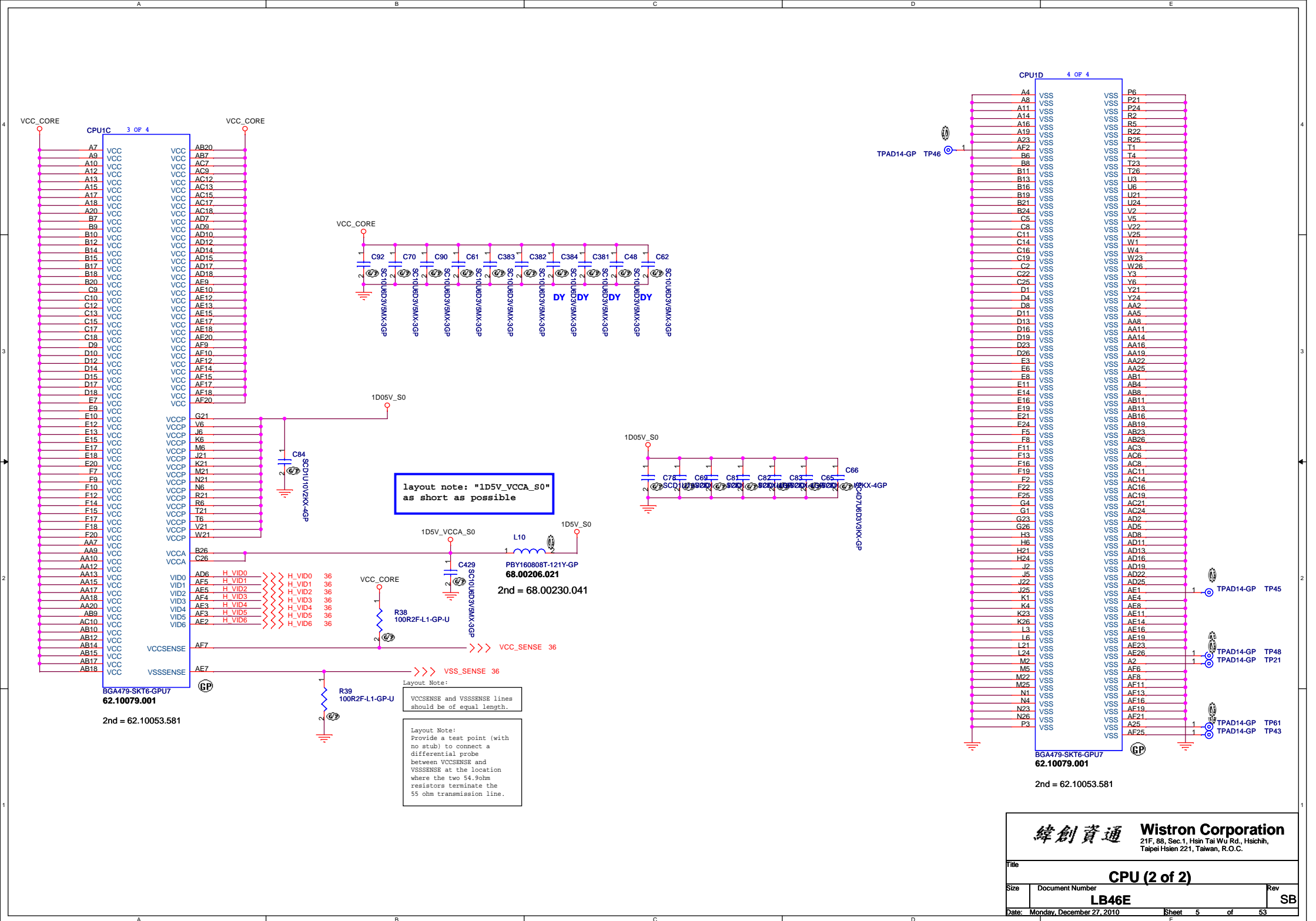


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Reference	
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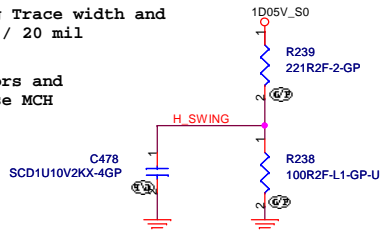
SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M





H_SWING routing Trace width and Spacing use 10 / 20 mil

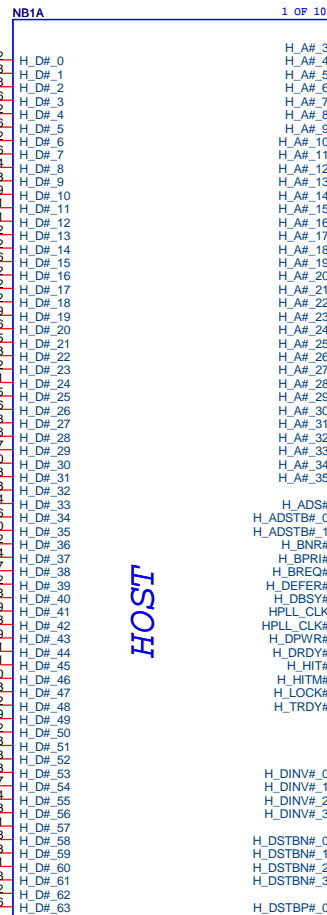
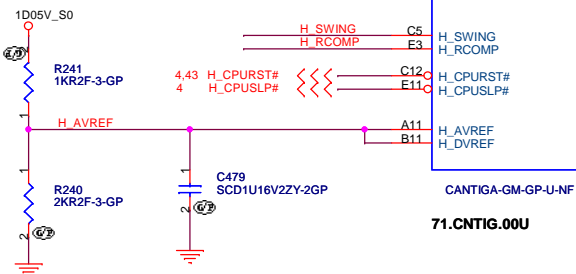
H_SWING Resistors and Capacitors close MCH
500 mil (MAX)



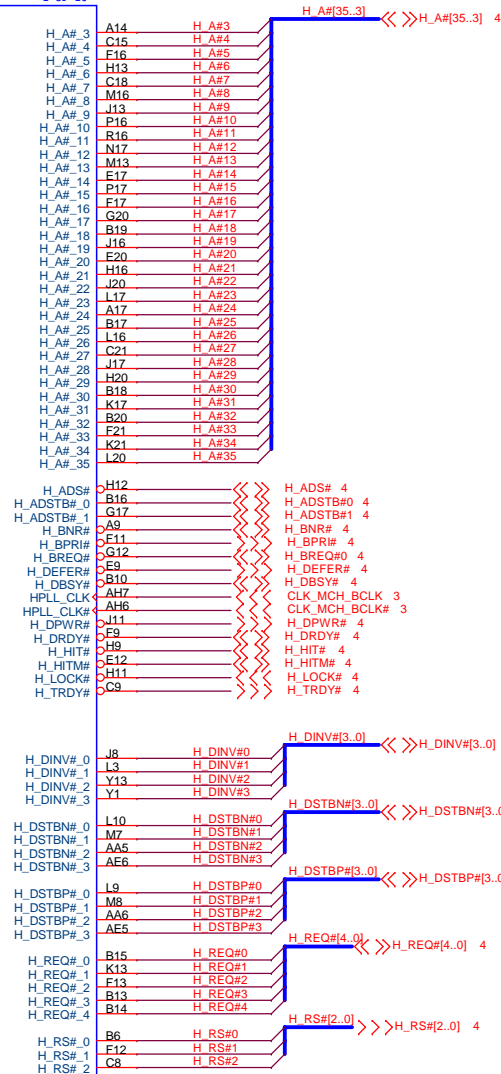
H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



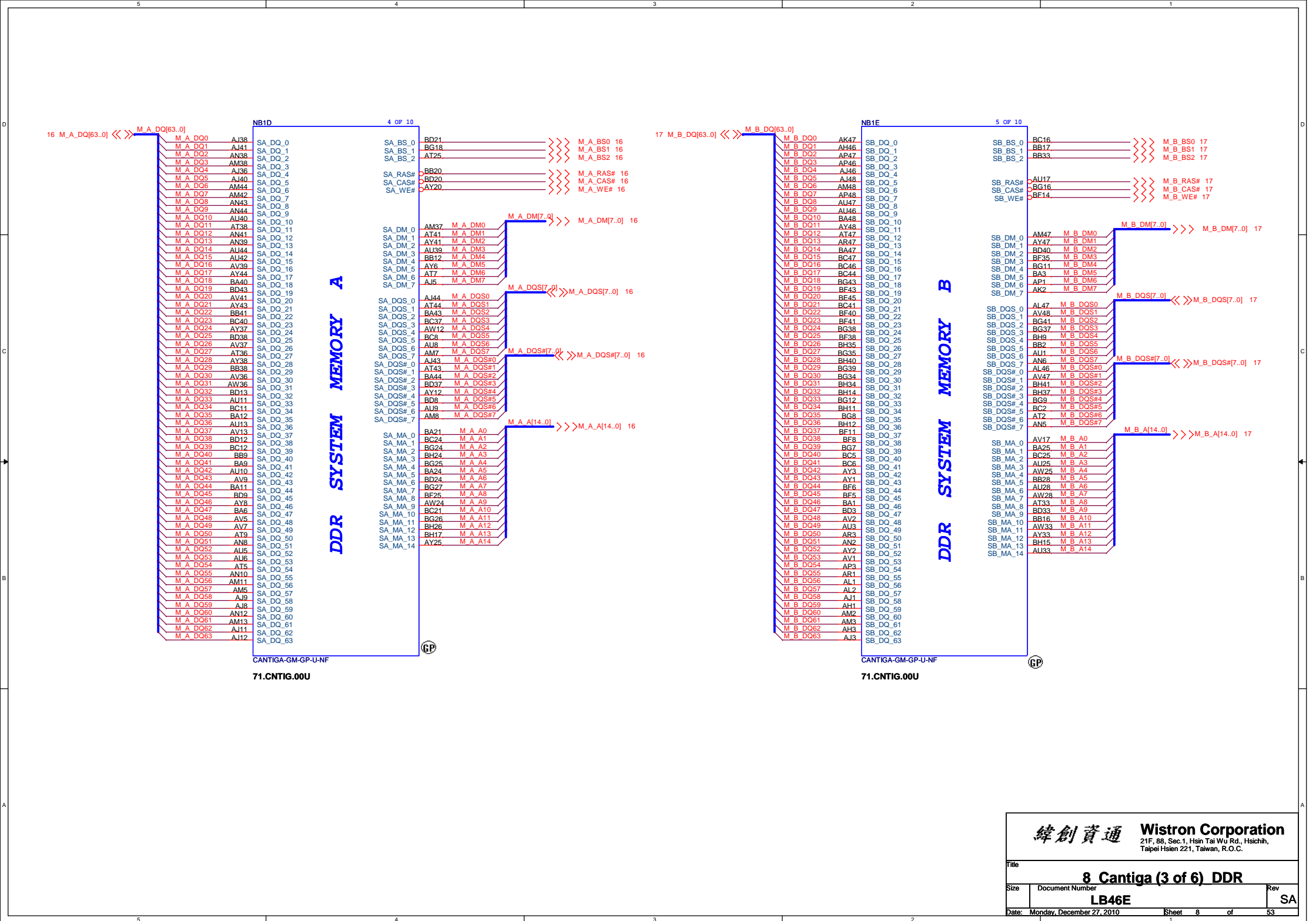
HOST

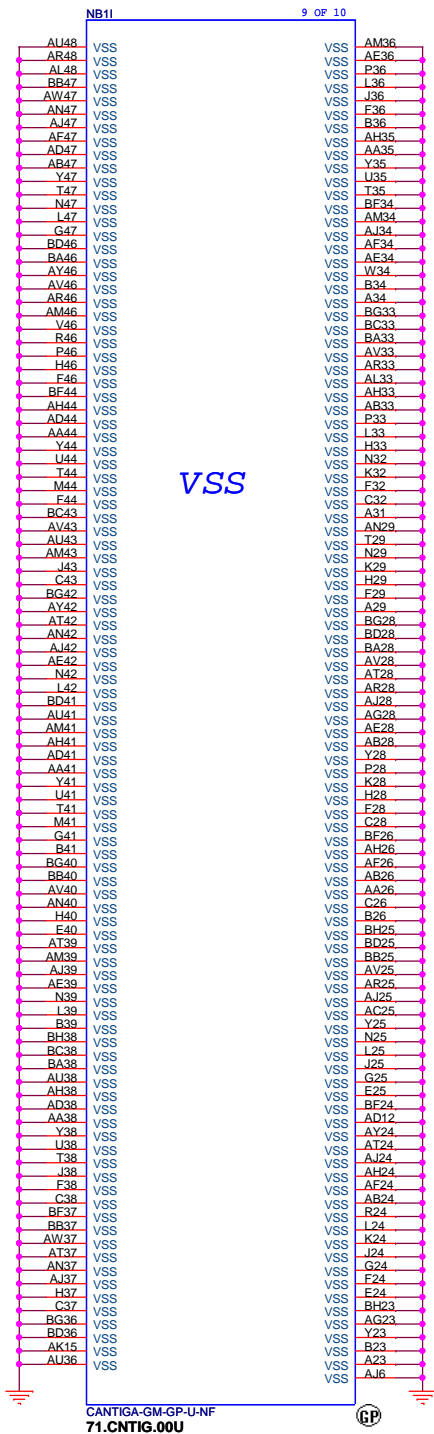


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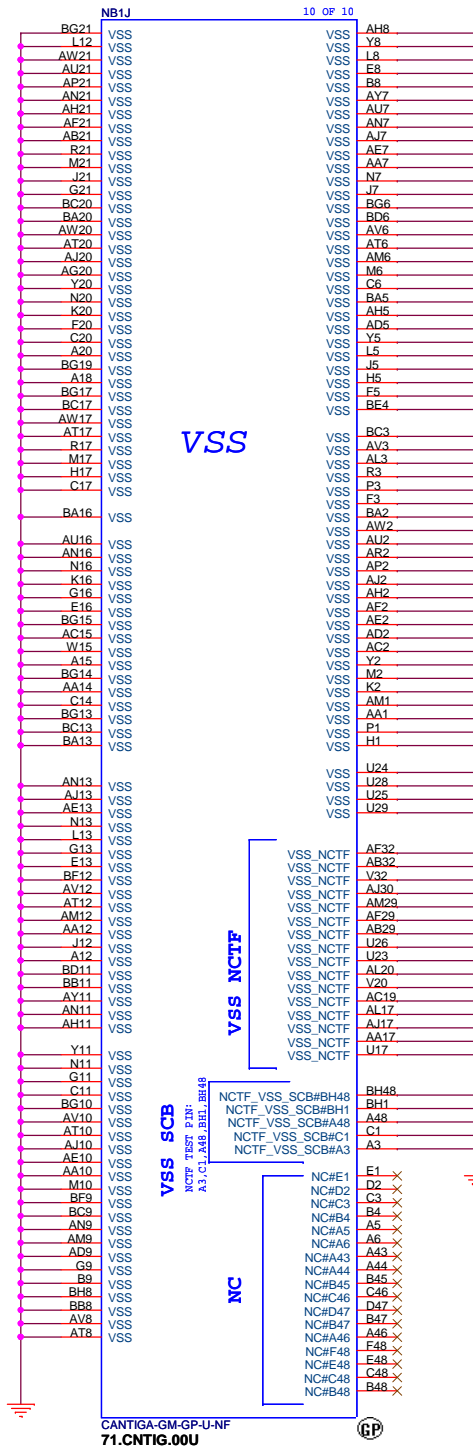
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CANTIGA-GM-GP-U-NF
71.CNTIG.000



CANTIGA-GM-GP-U-NF
71.CNTIG.000



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Cantiga (6 of 6)

Size

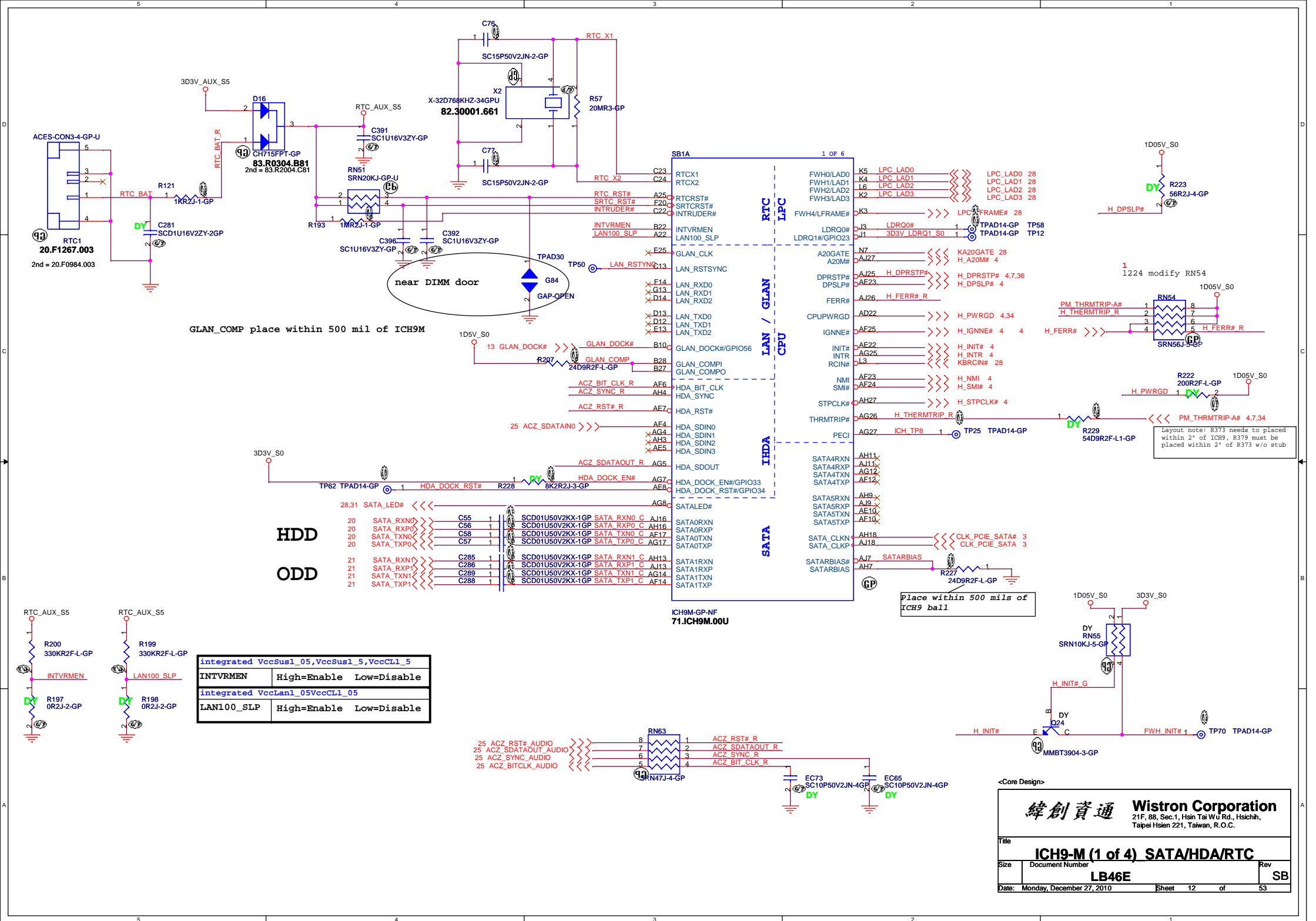
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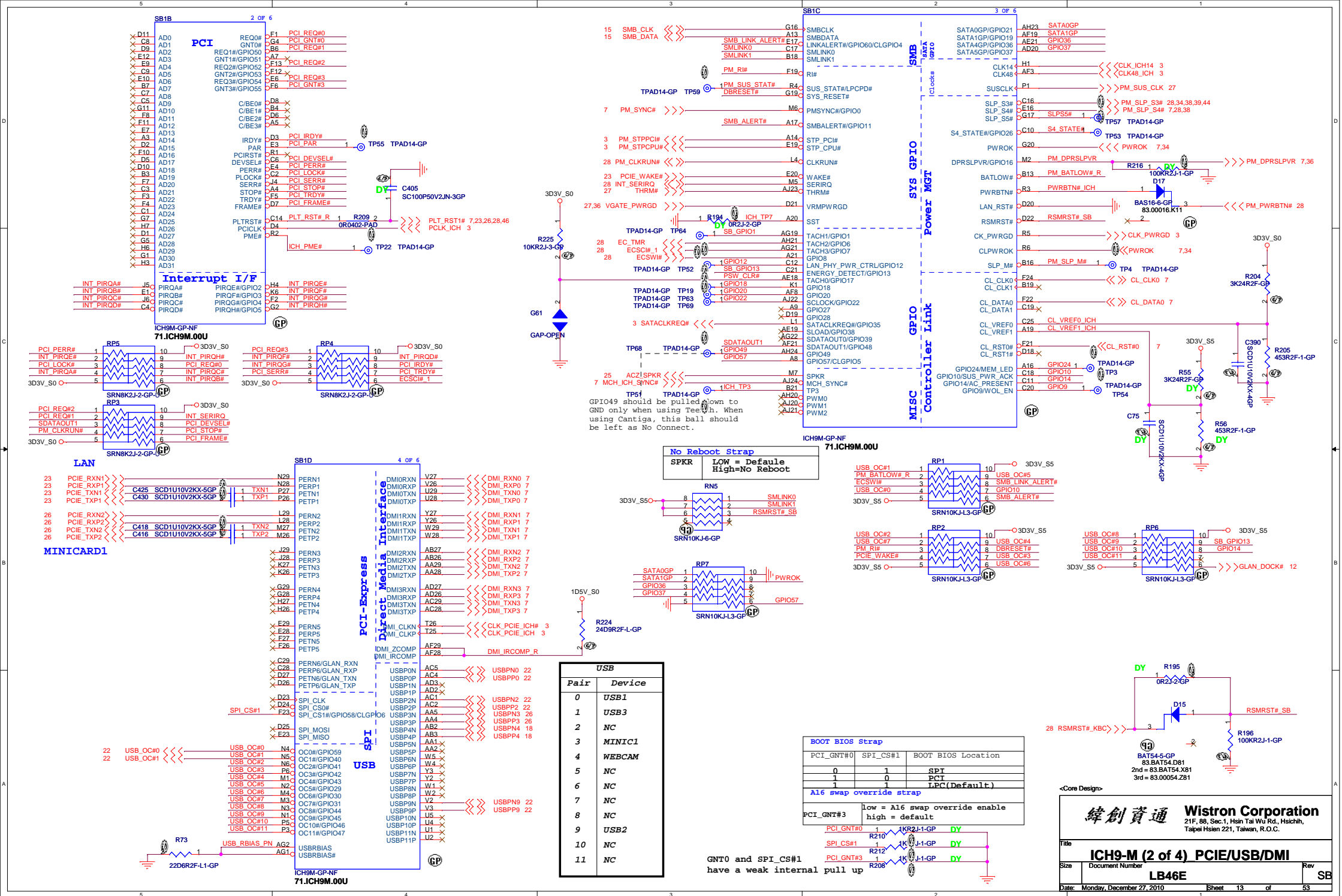
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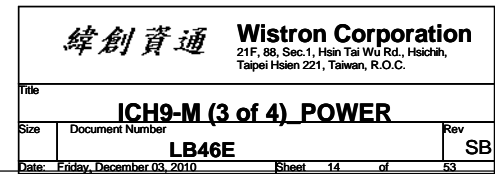
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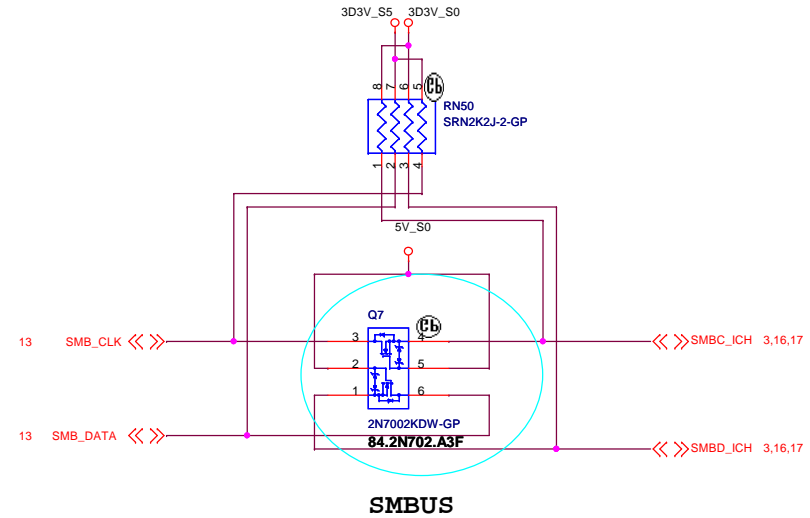
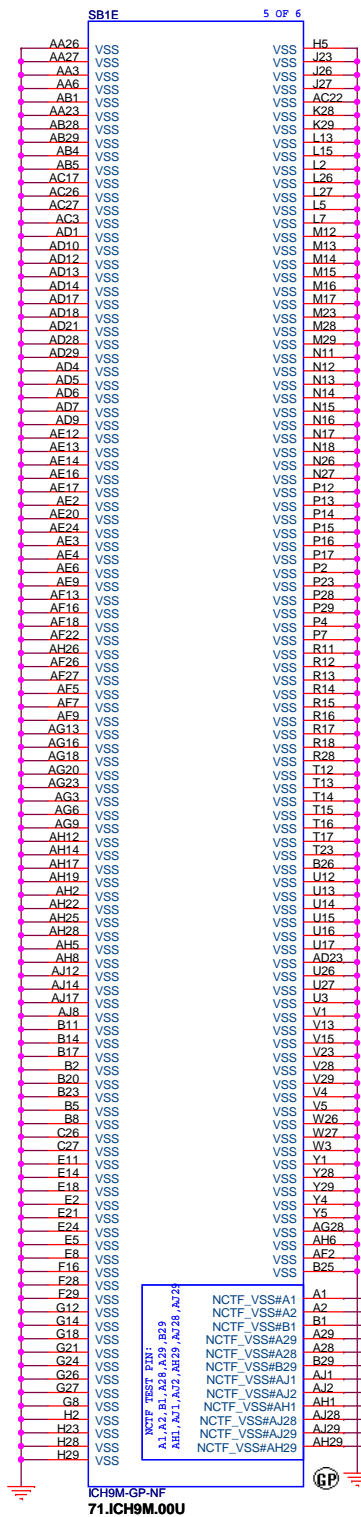
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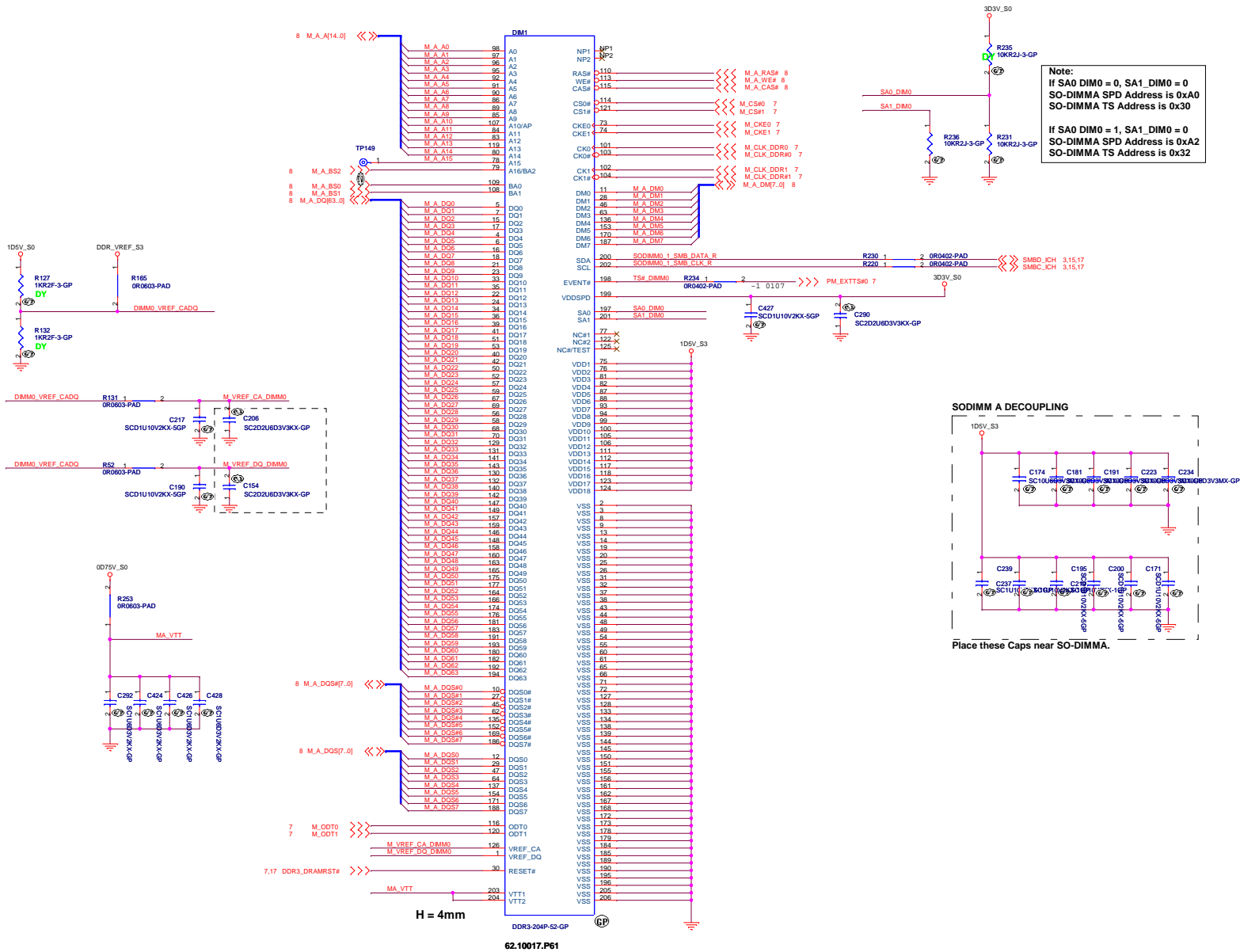
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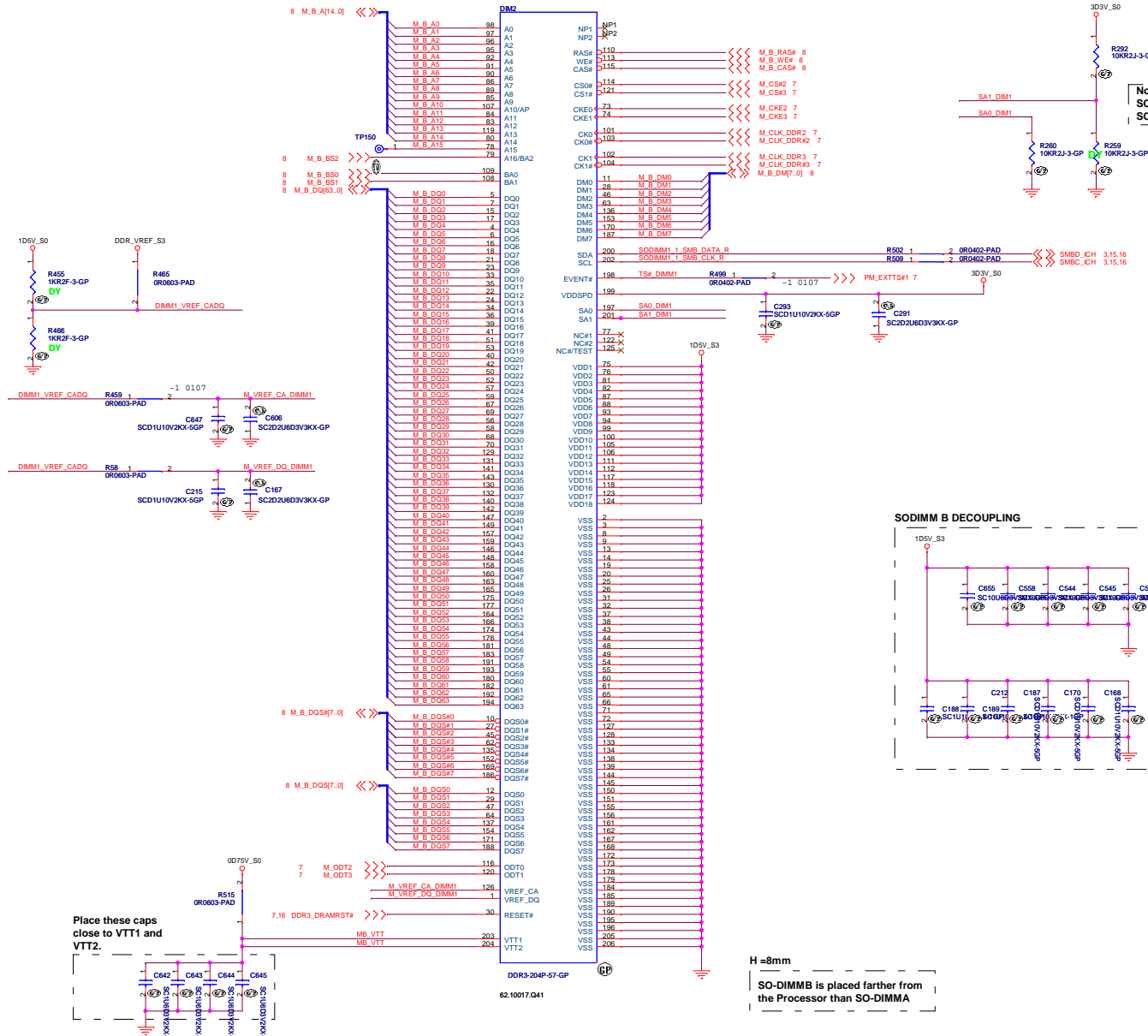


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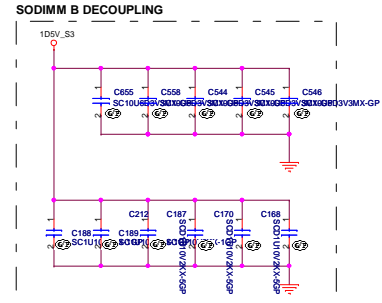
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2010/9/27 Changed

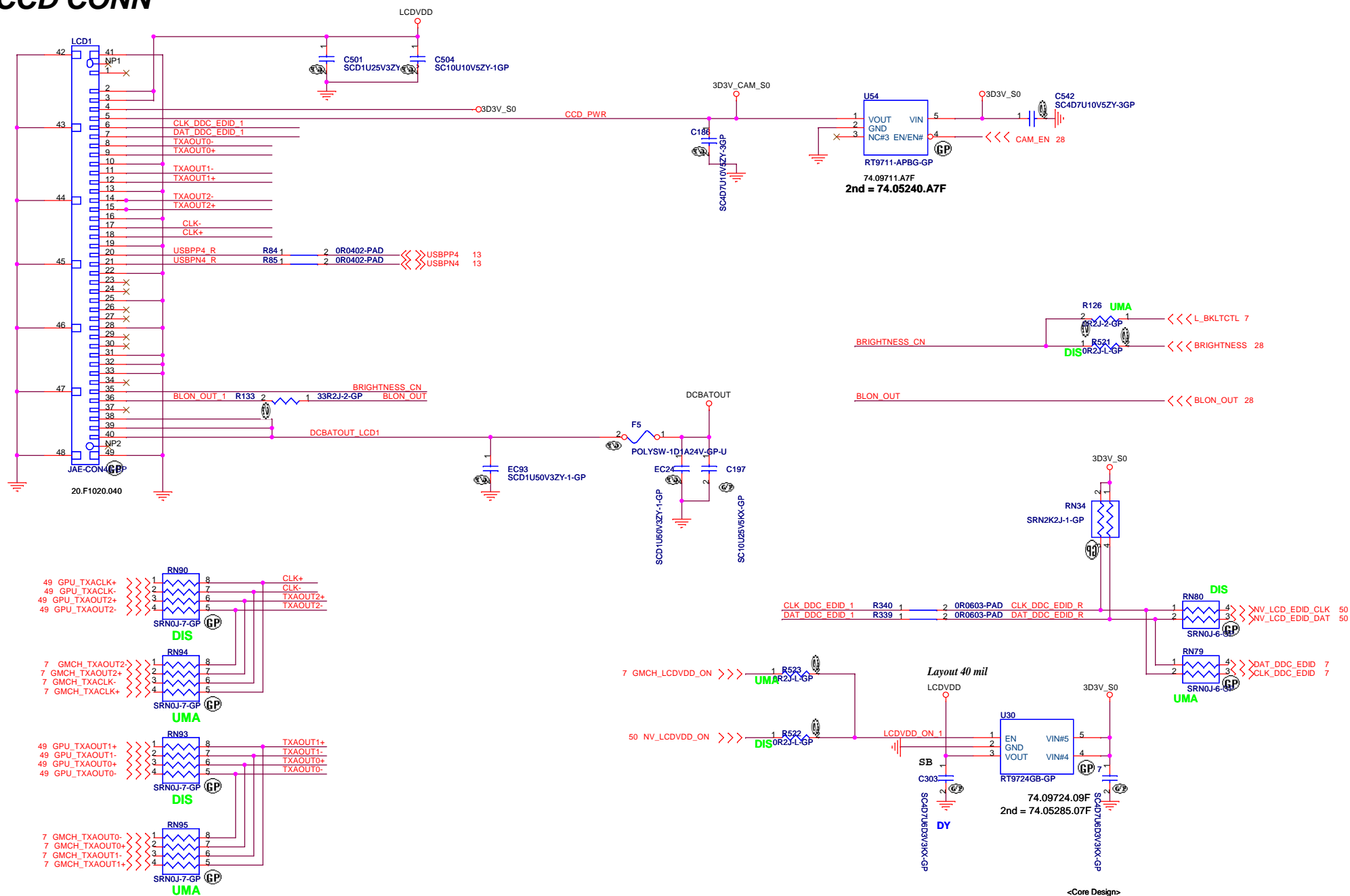


Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34



H = 8mm
SO-DIMMB is placed farther from
the Processor than SO-DIMMA

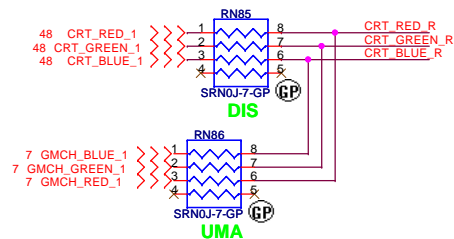
LCD/CCD CONN



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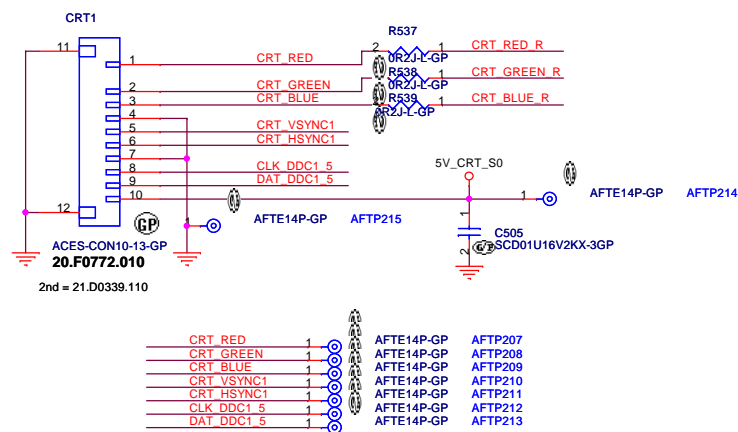


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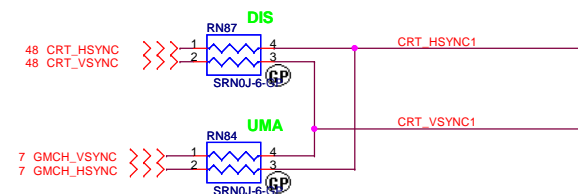
* Must be a ground return path between this ground and the ground on the VGA connector.

Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

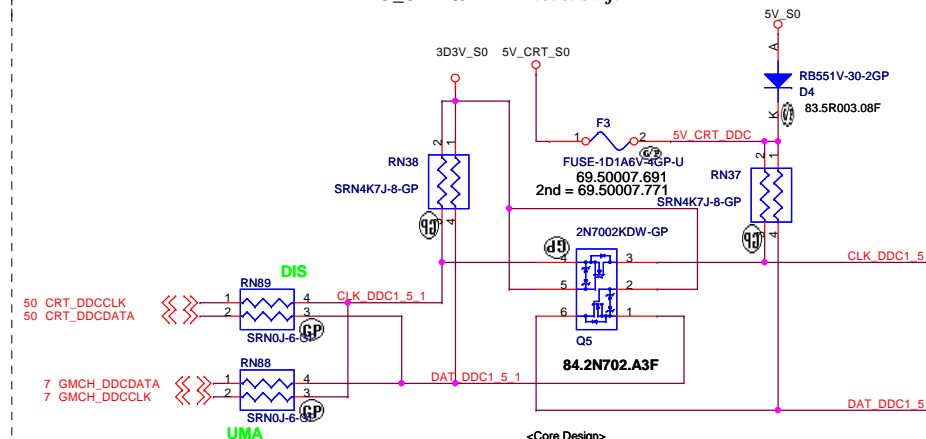
CRT I/F & CONNECTOR



Hsync & Vsync level shift



DDC_CLK & DATA level shift

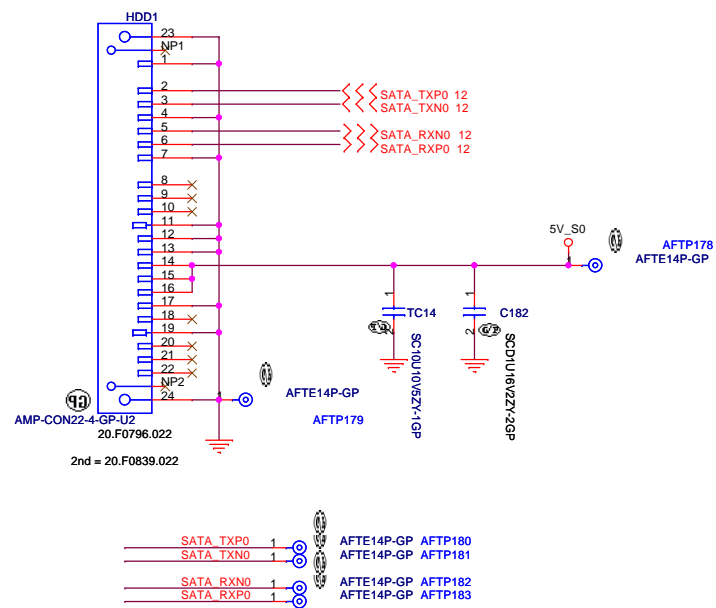


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SATA Connector



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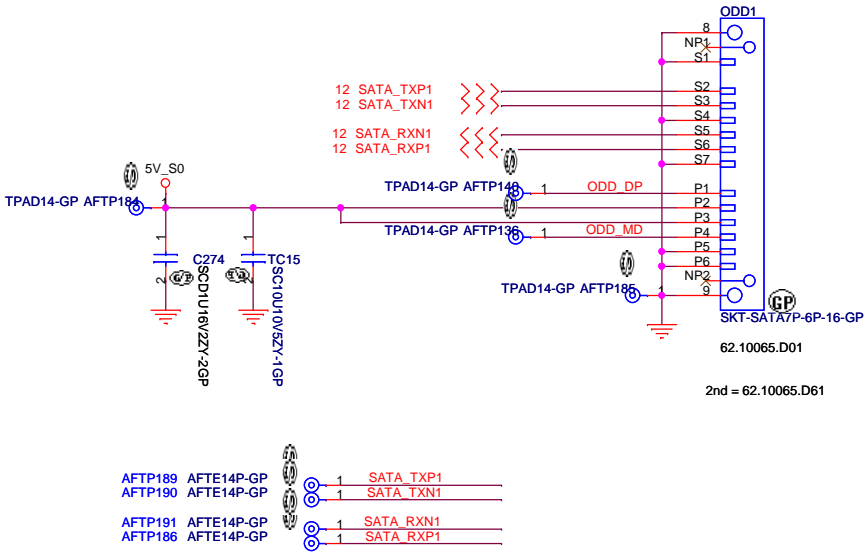
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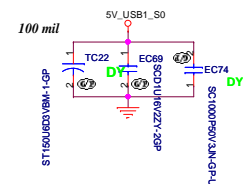
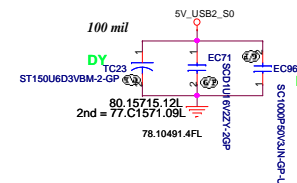
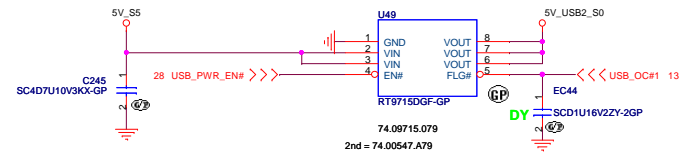
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SATA ODD Connector



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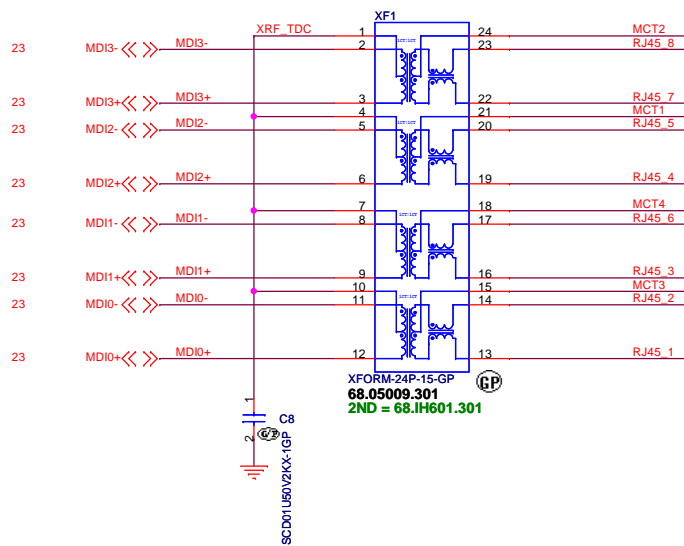
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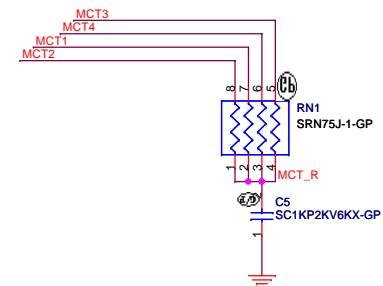
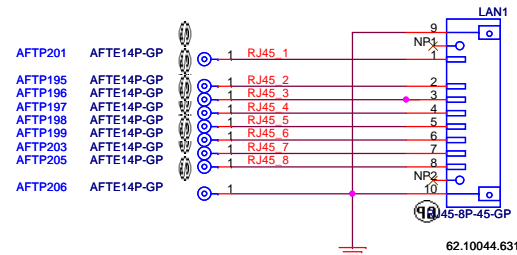
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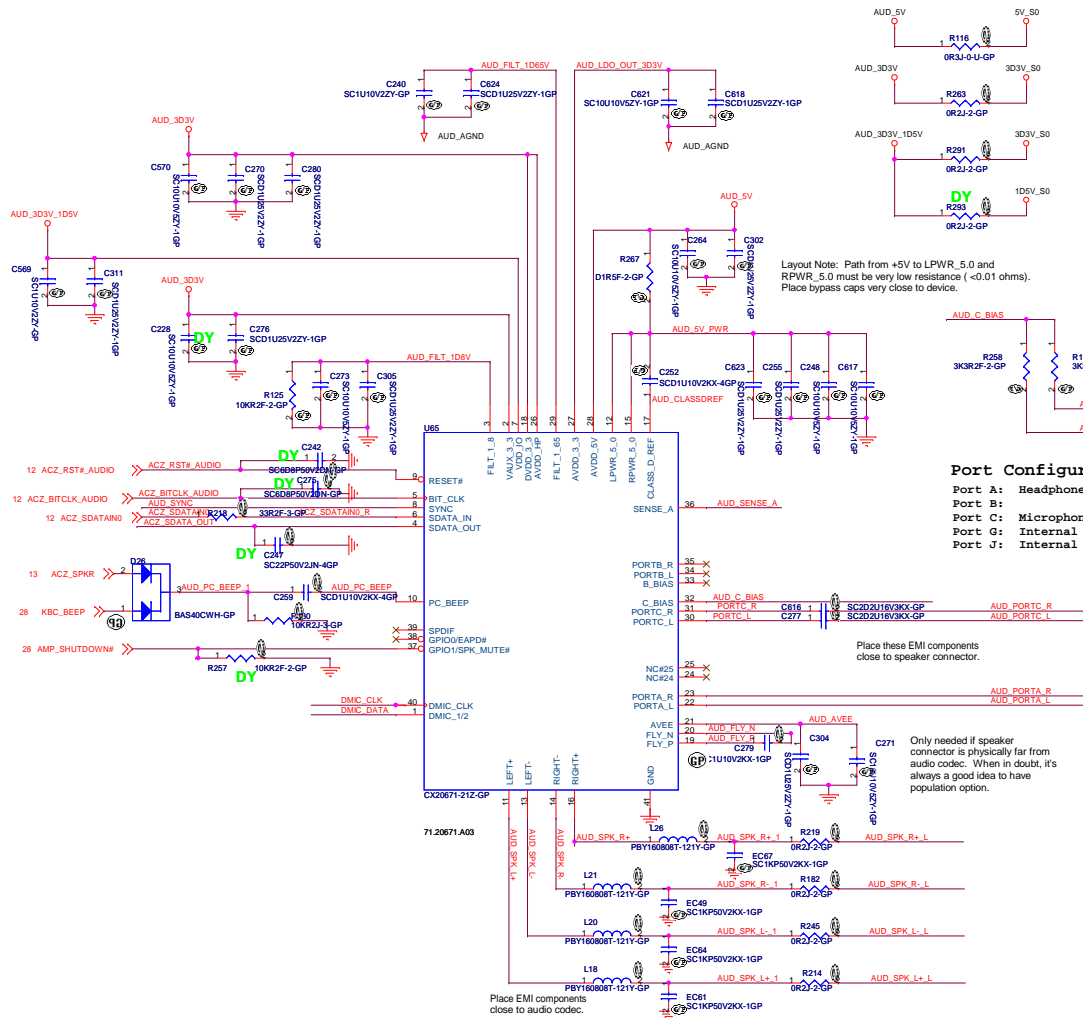
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- 1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width, 12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

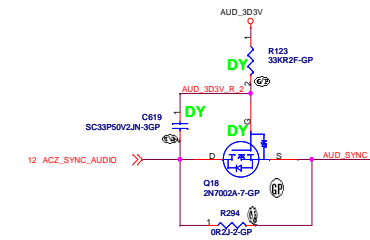
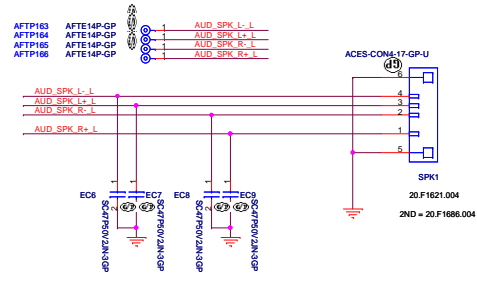


LAN Connector

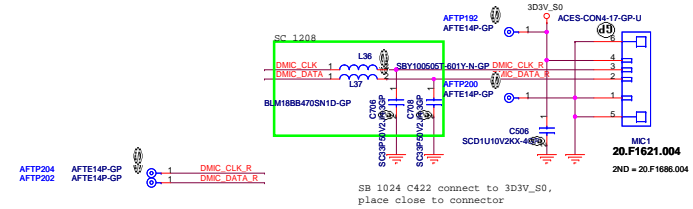




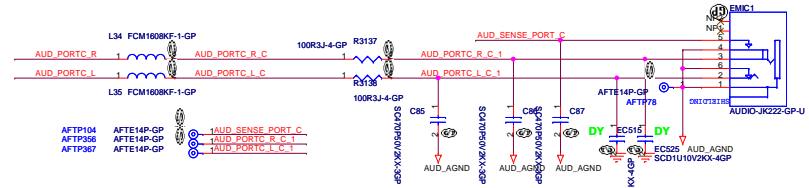
Internal Speaker



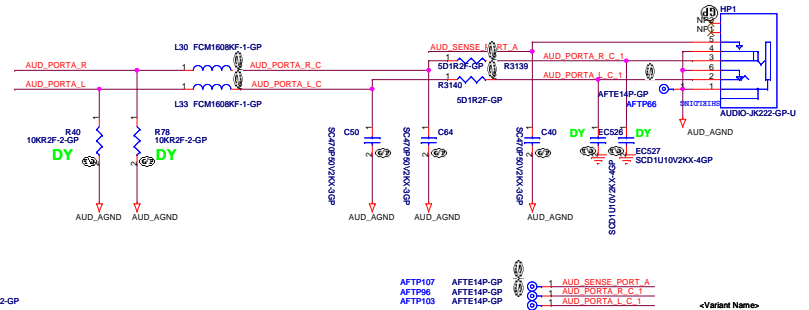
DMIC IN



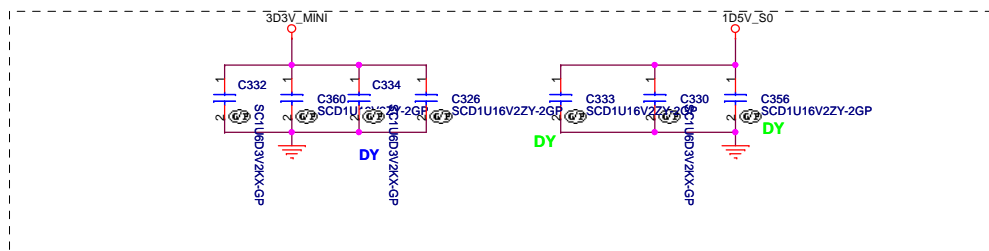
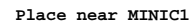
MIC CONN.



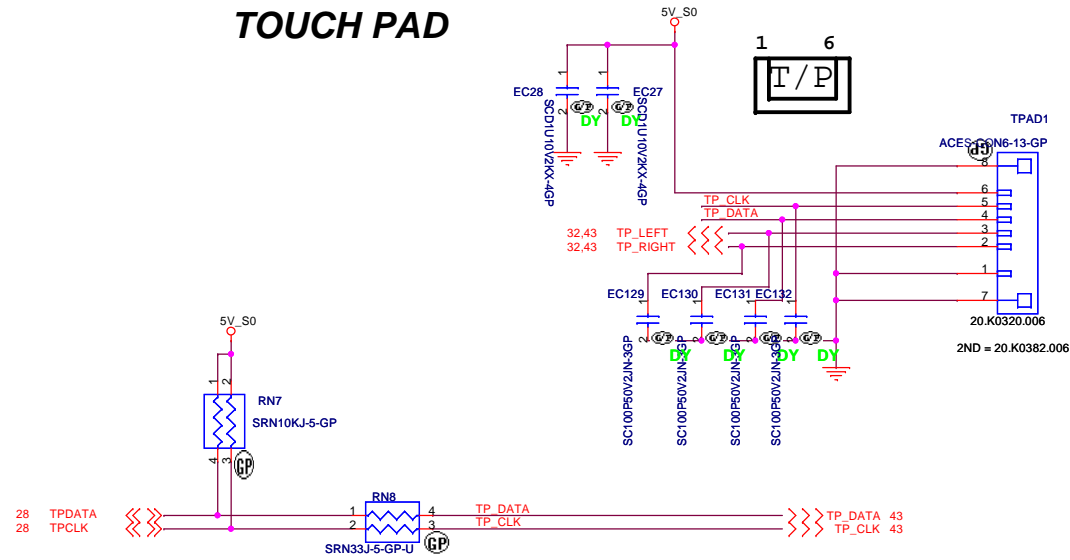
HEADPHONE CONN.



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TOUCH PAD



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Touch pad

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Document Number

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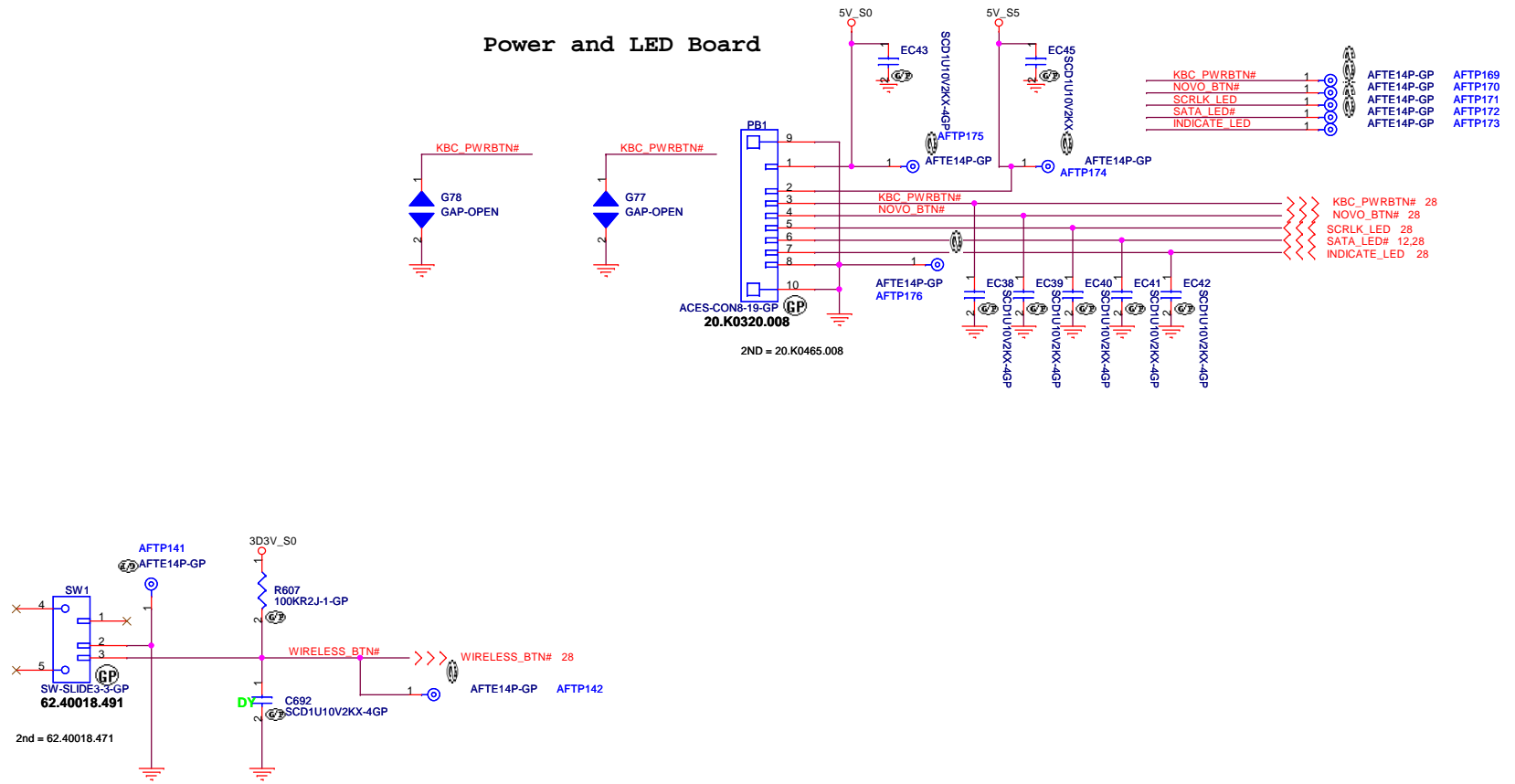
Rev

SB

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Power and LED Board

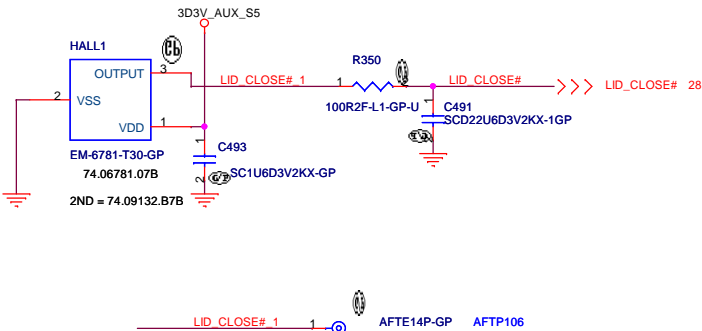
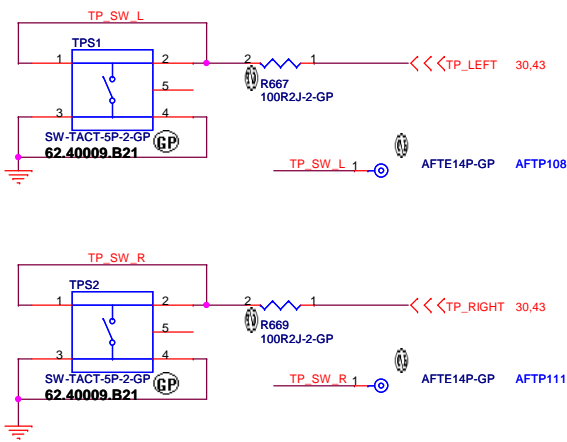


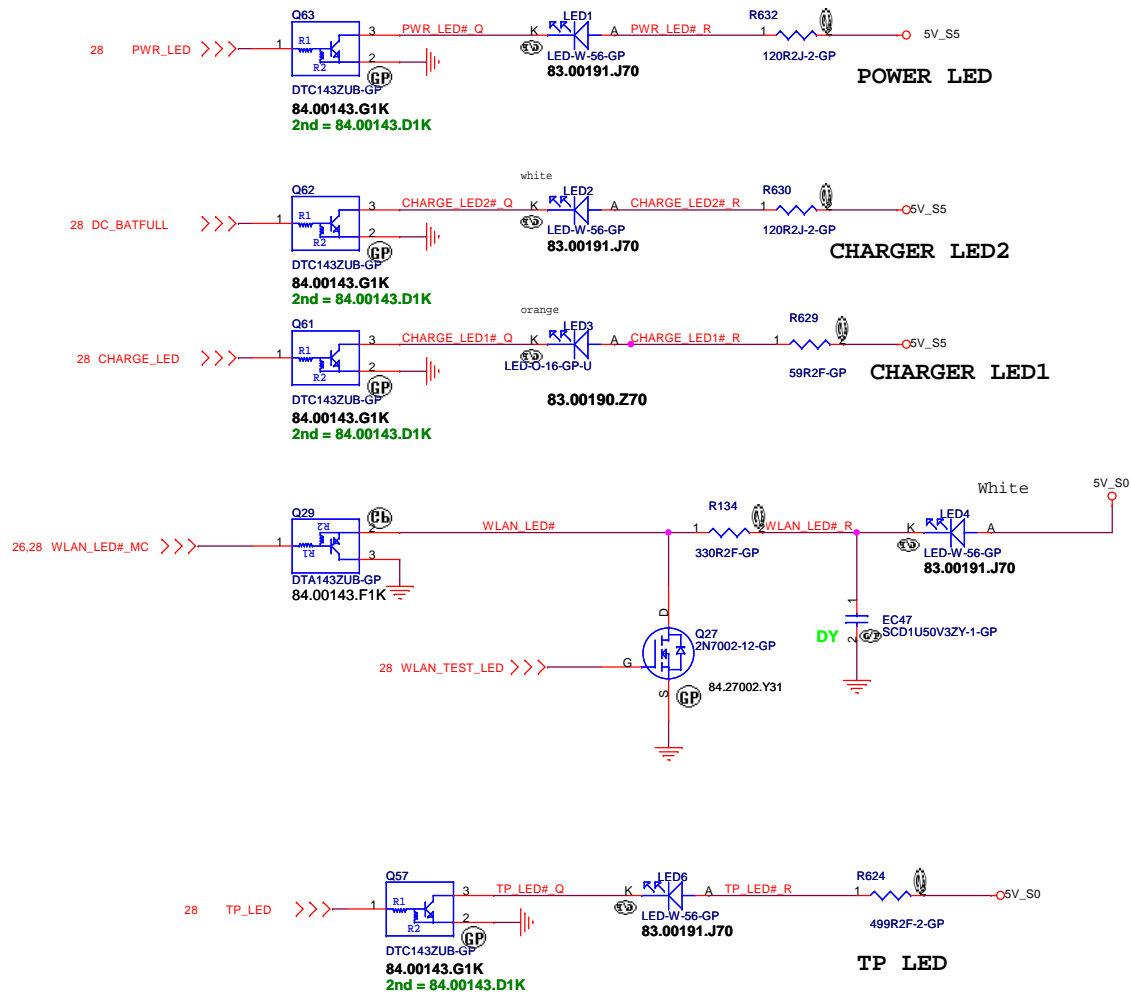
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Cover Up Switch

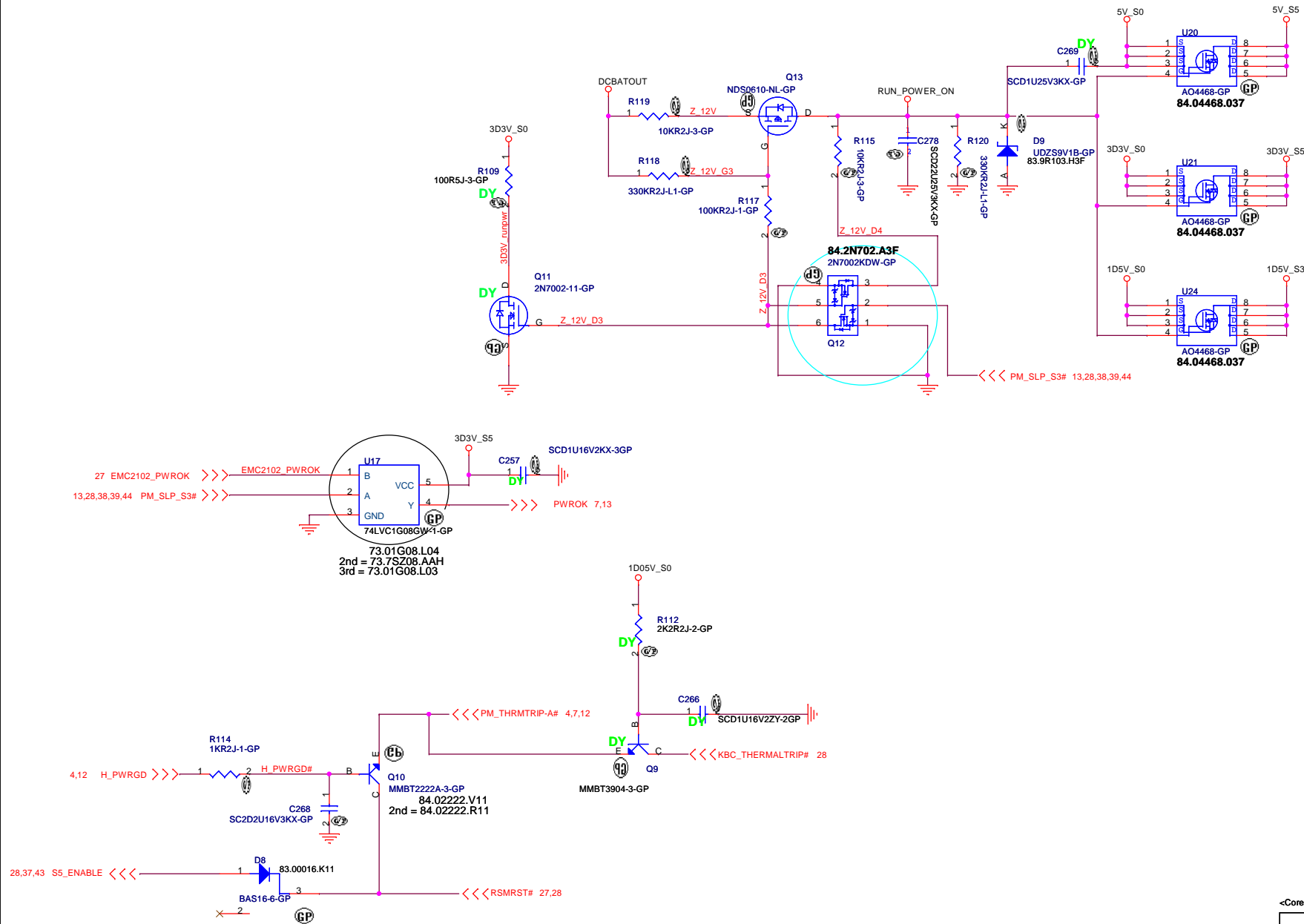




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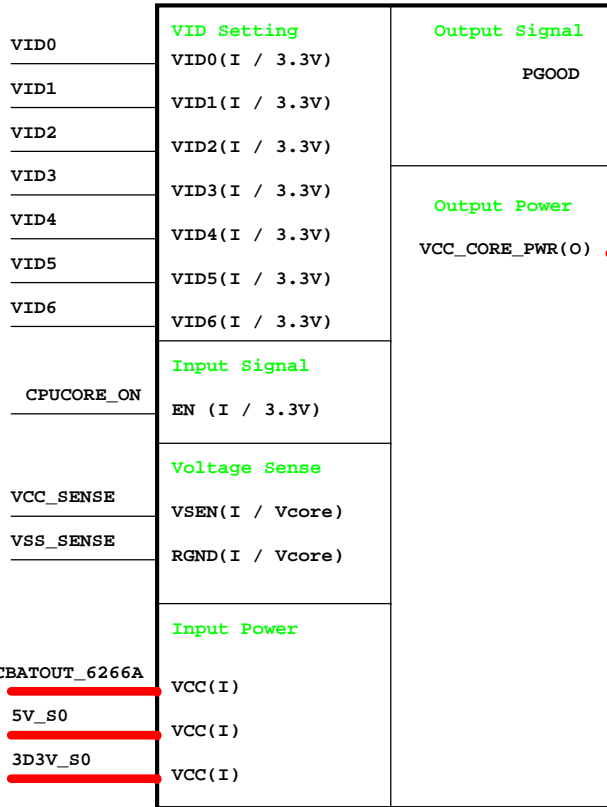
Run Power



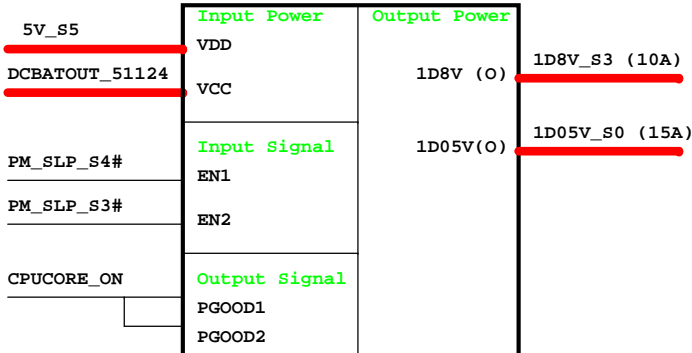
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Title	RUN POWER and 3D3V_AUX_S5
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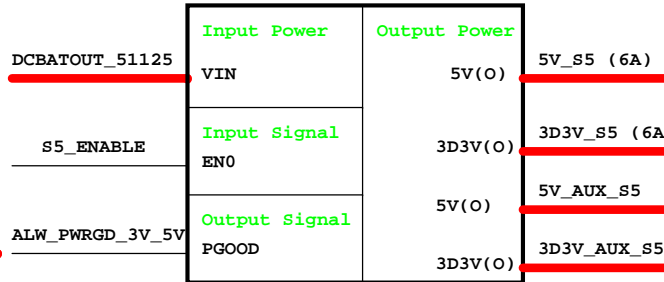
CPU_CORE
ISL6266A



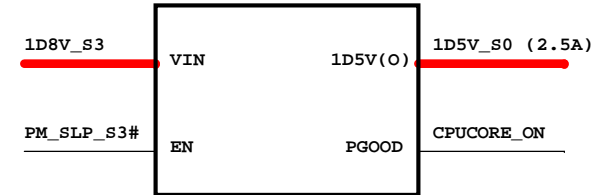
TPS51124
1D8V/1D05V



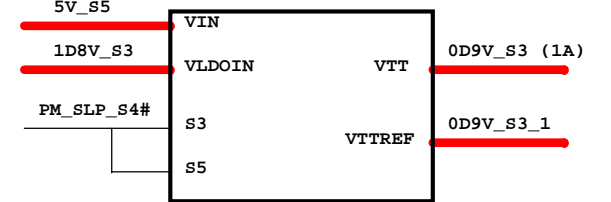
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5V/3D3V



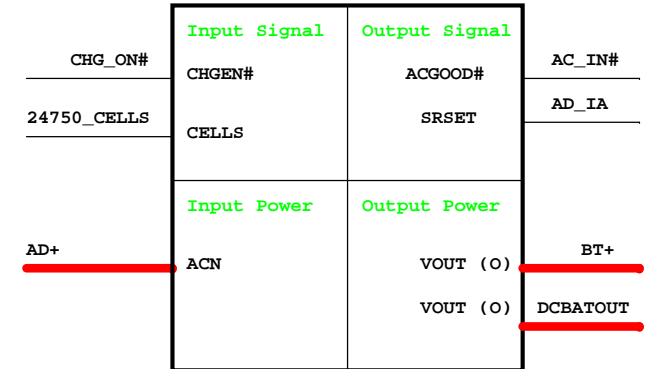
RT9018A
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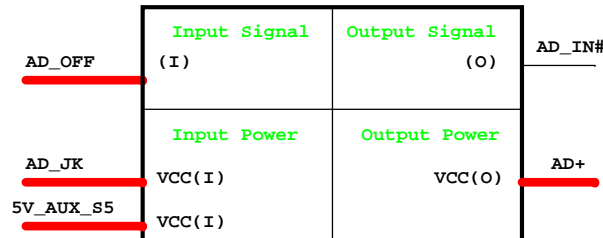
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Charger BQ24745



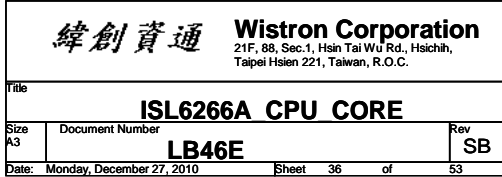
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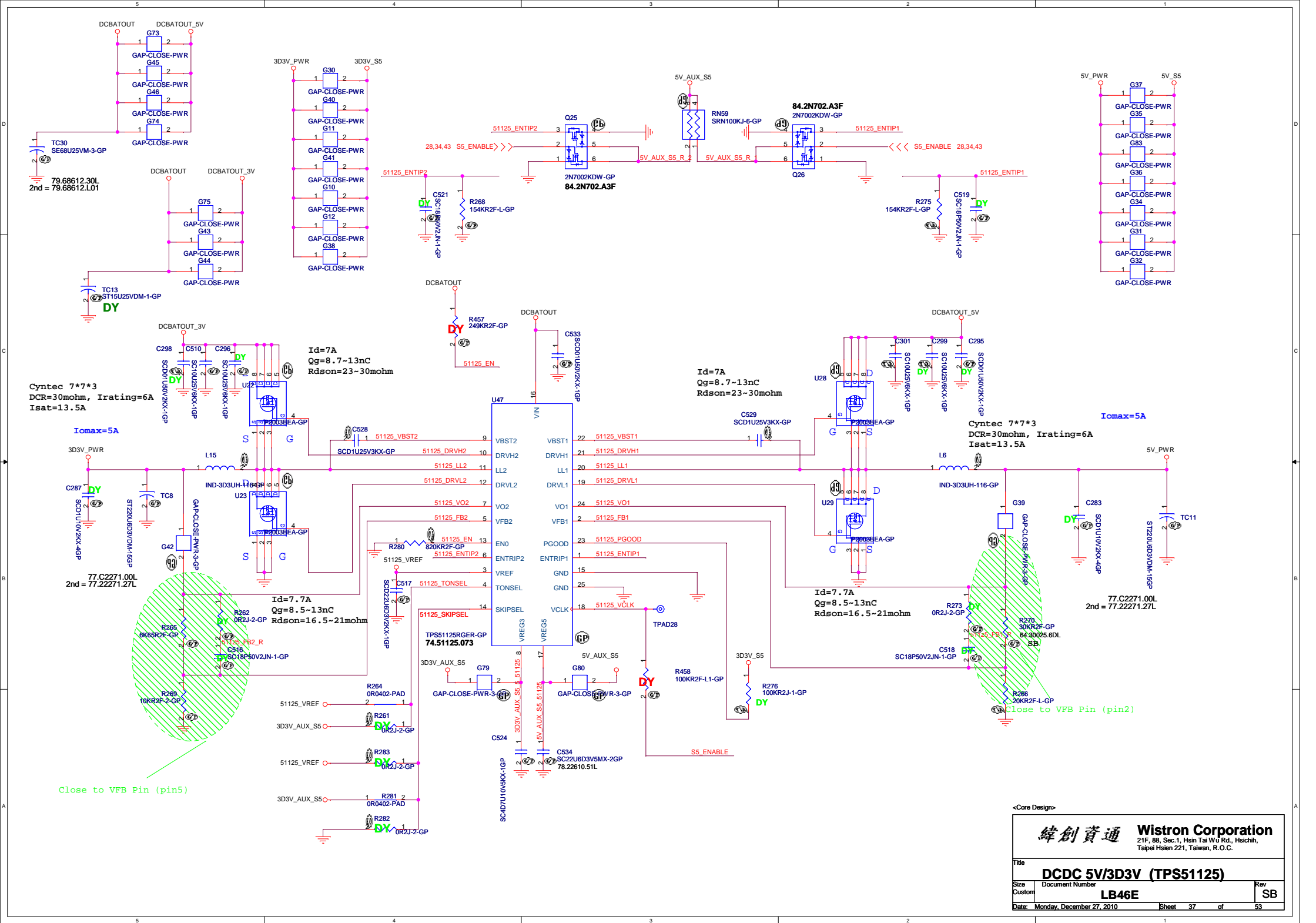


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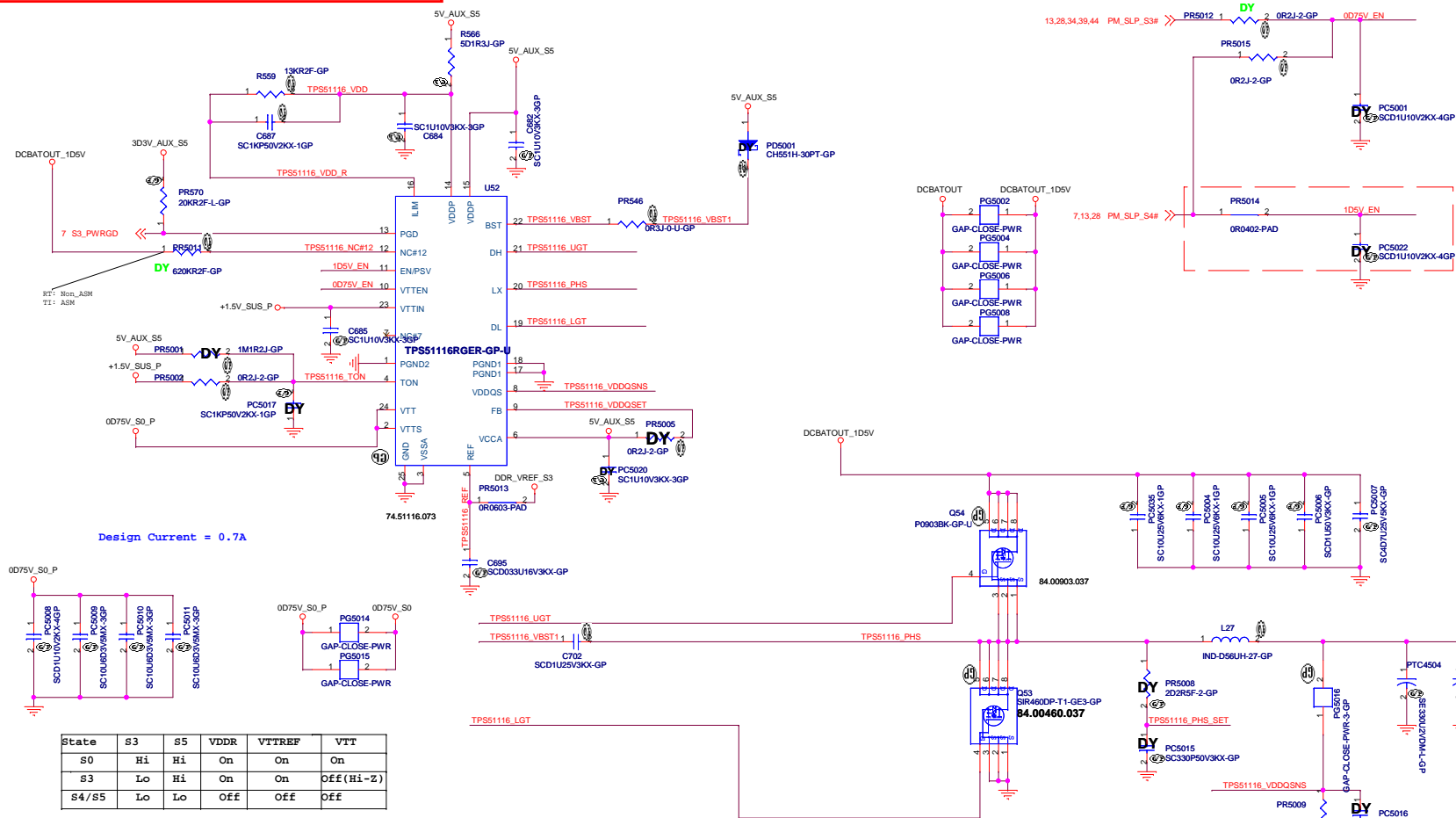
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Taipei Hsien 221, Taiwan, R.O.C.

Title			Power Sequence Logic	
Size B	Document Number	LB46E		Rev SB
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SSID = PWR.Plane.Regulator_1p5v0p75v
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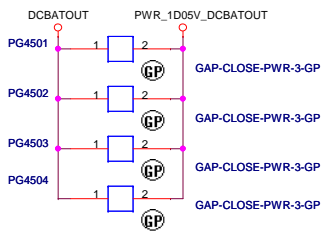


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

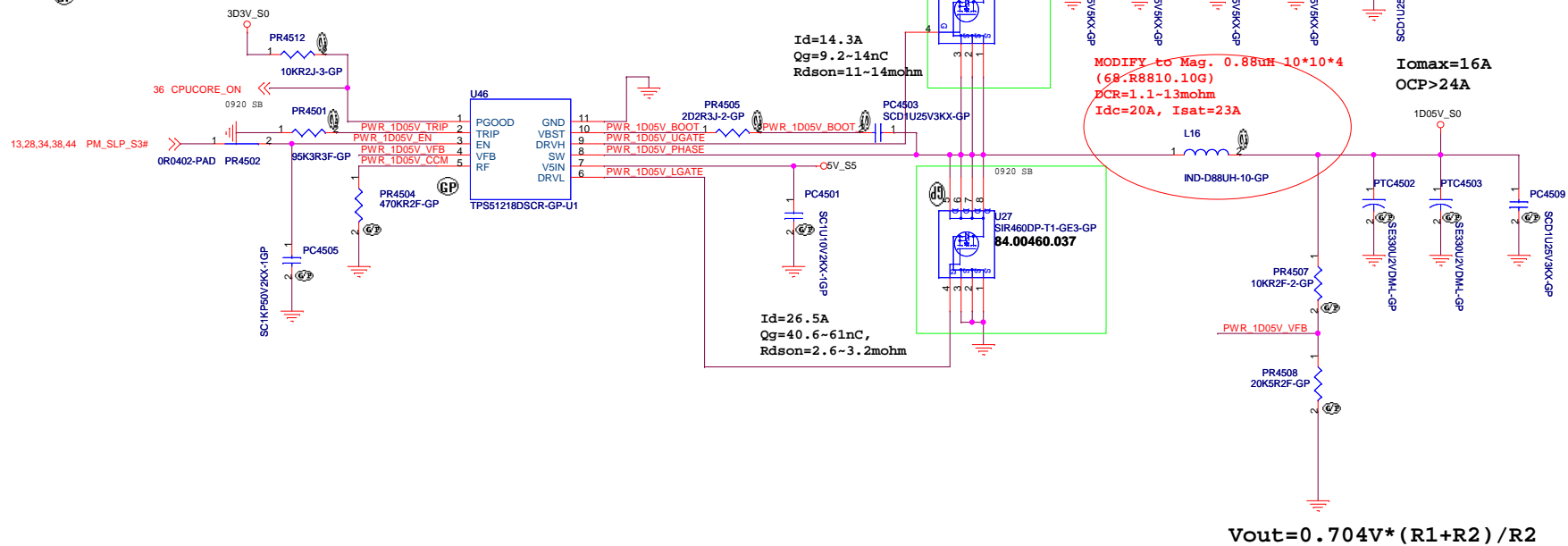
VDDQSET	VDDQ (V)	VTTREF and VIT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V KCM046 X5R/ 78.10622.52L
Inductor: 0.56uH POCM0104T-R56mN Cyntron DCR: 1.1mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEF3S040D331ER 9mohm 3Arms PANASONIC/ 79.03719.L0
H/S: S1S406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm/ 4.5Vgs/ 84.00403.037
L/S: S1S402DN/ POWERPAK-8/ 6.4mOhm/8mohm/4.5Vgs/ 84.00402.037
Switching freq-->400KHz

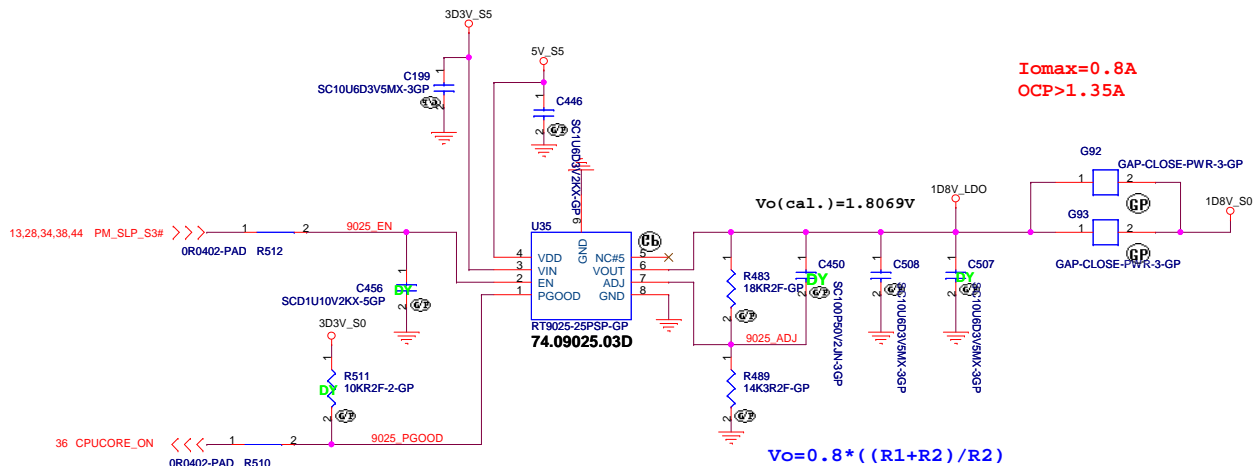




TPS51218 for 1D05V



RT9025 for 1D8V_S0



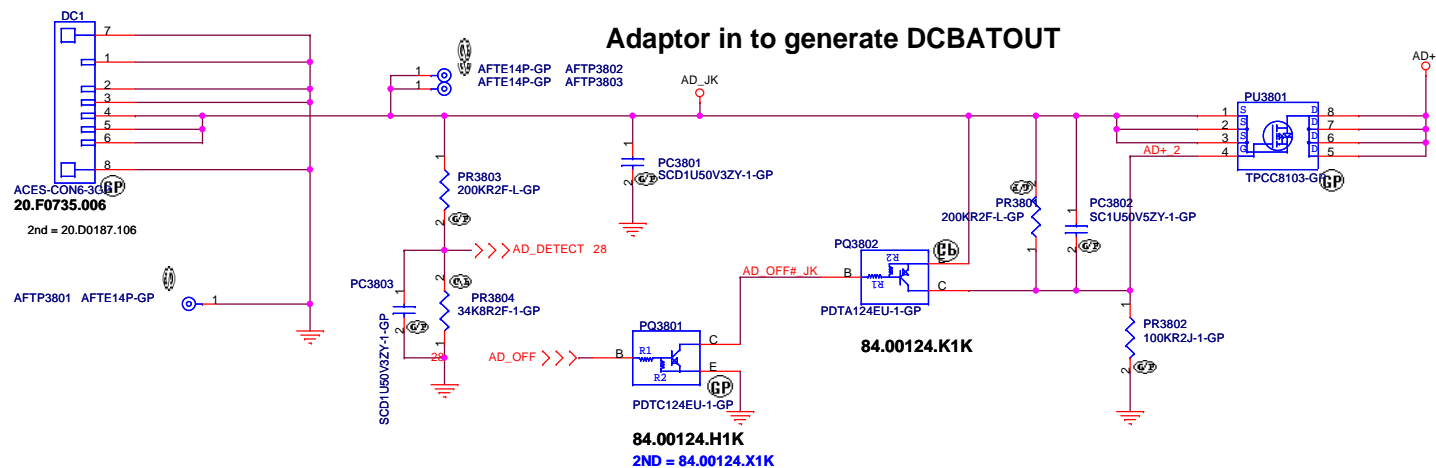
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緯創資通

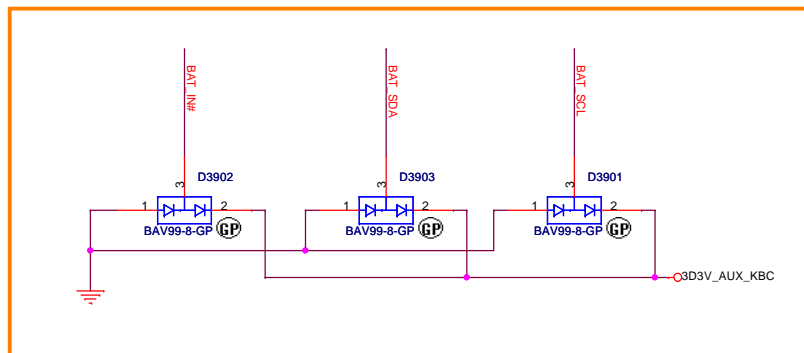
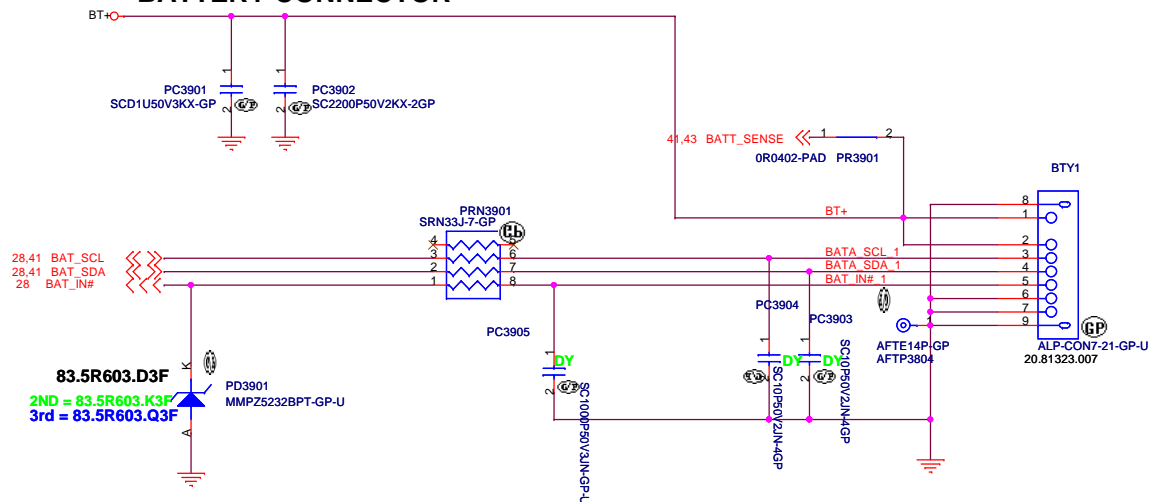
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Title			
DC/DC_1D05V_TPS51218			
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Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Title

AD/BATT CONN

Size

Document Number

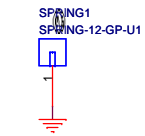
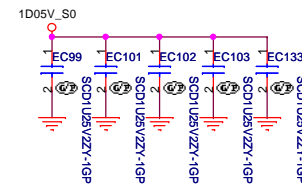
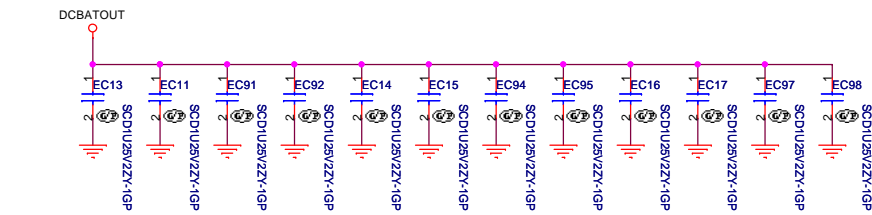
LB46E

Rev

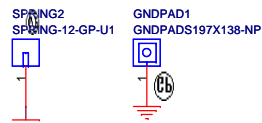
SB

Date: Monday, December 27, 2010

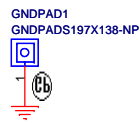
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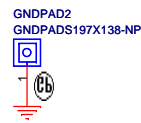
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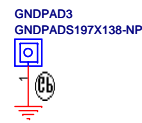
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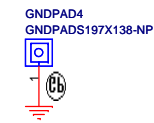
ZZ.00PAD.ZZZ



ZZ.00PAD.ZZZ



ZZ.00PAD.ZZZ



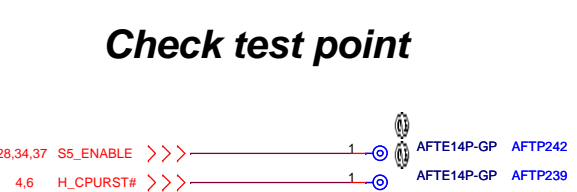
ZZ.00PAD.ZZZ



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

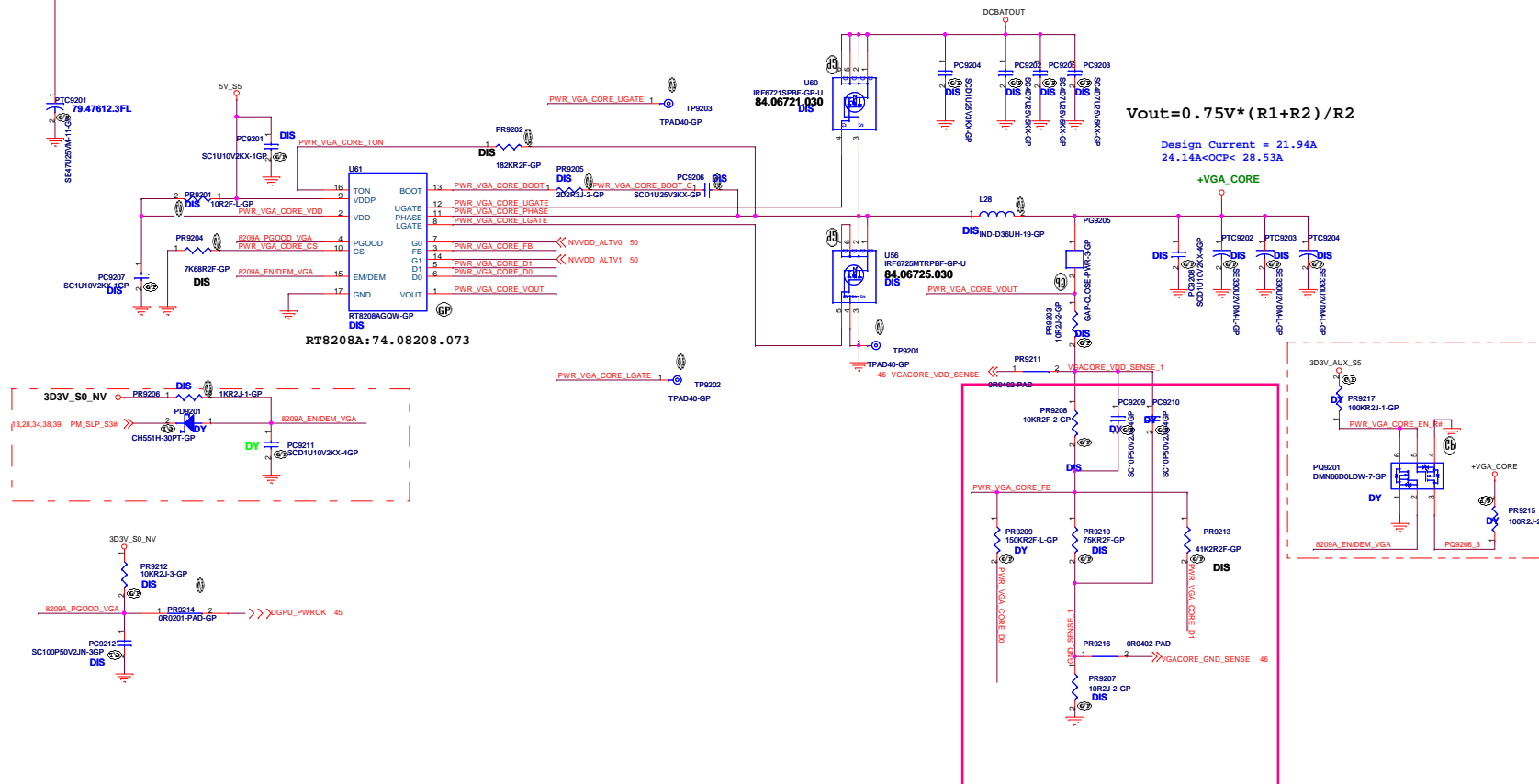
Title		EMI/Spring/Boss	
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Test Point locate near DIMM Door where can be tested

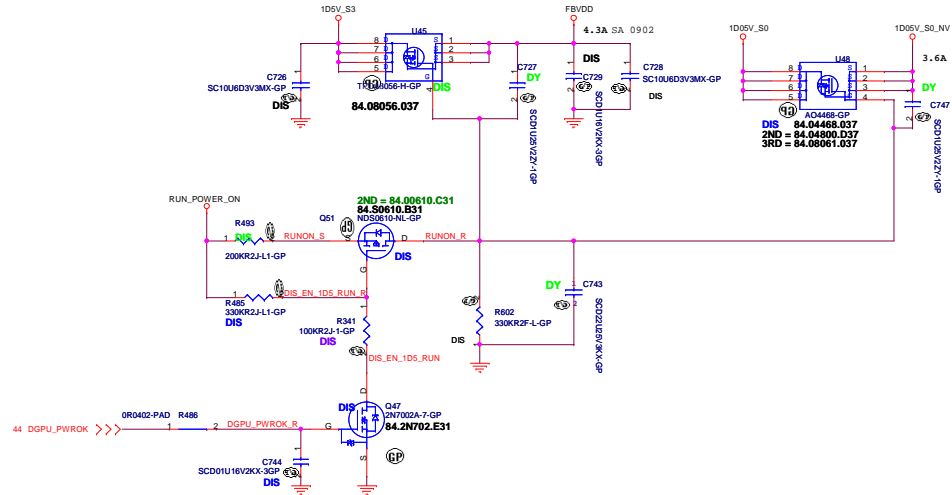


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SSID = PWR.Plane.Regulator_GFX
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[illegible]

+1.05V to +1.05V_NV Transfer



3.3v (580mA)

Title			
N11M(1/6) PEG			
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