

Compal Confidential

Schematics Document

NIWE1

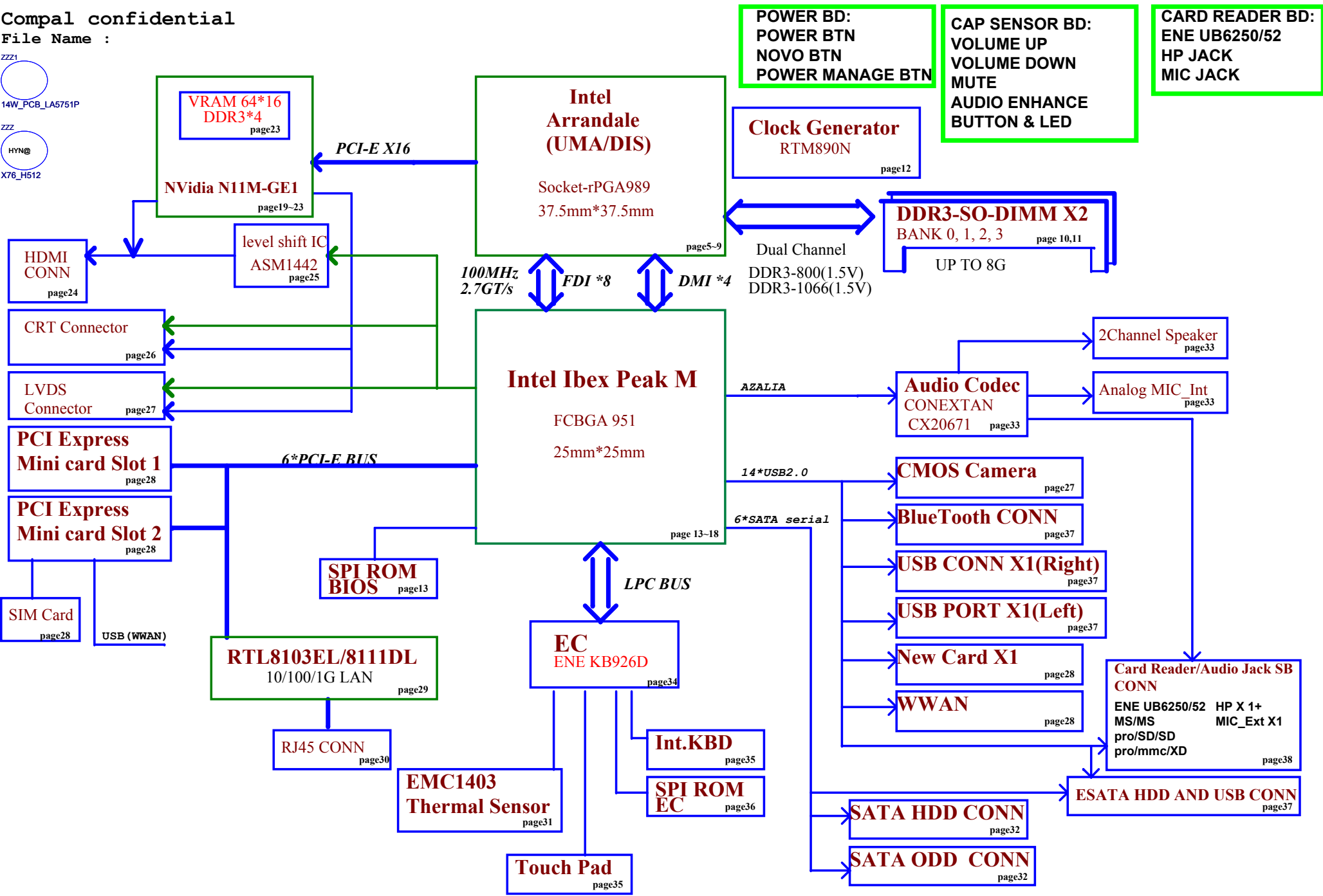
Arrandale

with Intel IBEX PEAK-M core logic

REV : 0 . 3

Security Classification	Compal Secret Data			Compal Electronics,Ltd.		
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	Cover Sheet	
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				Custom	LA-5751	0.3
Date: Thursday, October 29, 2009				Sheet	1	of 51

ZZZ1
14W_PCB_LA5751P
ZZZ
HYN@
X76_H512



Security Classification		Compal Secret Data				Compal Electronics, Inc.									
Issued Date		2008/03/24		Deciphered Date		2008/04/		Title		MB Block Diagram					
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								Custom		LA-5751		0.3			
								Date:		Thursday, October 23, 2009		Sheet		2 of 51	

DDR3 Voltage Rails

power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS
State				
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

SMBUS Control Table

	SOURCE	RAM M2	BATT	KE926	SODIMM	CLK CHIP	WLAN WWAN	N10x Thermal Sensor	N10x	Cap sensor board	NEW CARD	PCH
SMB_EC_CK1	KB926	X	V	X	X	X	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW									
SMB_EC_CK2	KB926	X	X	X	X	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW											+3VALW
SMBCLK	PCH	V	X	X	V	V	X	X	X	X	V	X
SMBDATA	+3VALW	+3VALW			+3VS	+3VS					+3VS	
SML0CLK	PCH	X	X	X	X	X	X	X	X	X	X	X
SML0DATA	+3VALW											
SML1CLK	PCH	X	X	V	X	X	X	V	X	V	X	X
SML1DATA	+3VALW			+3VALW				+3VS		+3VS		

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

@ FUNCTION

Structure	Description	NON-USE
45@	45 BOM	
BT@	Blue Tooth function	
3G@	3G function (WWAN)	
CAP@	CAP Sensor function	
CMOS@	CMOS CAMERA function	
ESATA@	E-SATA function	
HDMI@	HDMI function (UMA or DIS)	
UMA HDMI@	HDMI function (UMA only)	
X76@	X76 BOM	
100@	10/100 LAN function	
GIGA@	GIGA LAN function	
UMA@	UMA only (Arrandale)	
DIS@	DIS only (Arrandale)	

SKU

Arrandale (dGPU) DIS only	DIS@
Arrandale (iGPU) UMA only	UMA@

PCIE PORT LIST	
PORT	DEVICE
1	
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	
7	
8	

USB PORT LIST	
PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	LEFT SIDE
4	RIGHT SIDE
5	CARD READER
6	
7	
8	WIRELESS
9	
10	NEW CARD
11	BT
12	
13	3G

VGA and DDR3 Voltage Rails (N11x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	N/A	
GPIO8	I/O	N/A	
GPIO9	OUT	N/A	
GPIO10	OUT	N/A	
GPIO11	I/O	-	Reserve 10K pull low.
GPIO12	IN	N/A	
GPIO13	OUT	N/A	
GPIO14	OUT	-	Reserve 10K pull low.
GPIO15	IN	N/A	
GPIO16	OUT	N/A	
GPIO17	IN	-	PAD
GPIO18	IN	N/A	
GPIO19	IN	N/A	

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

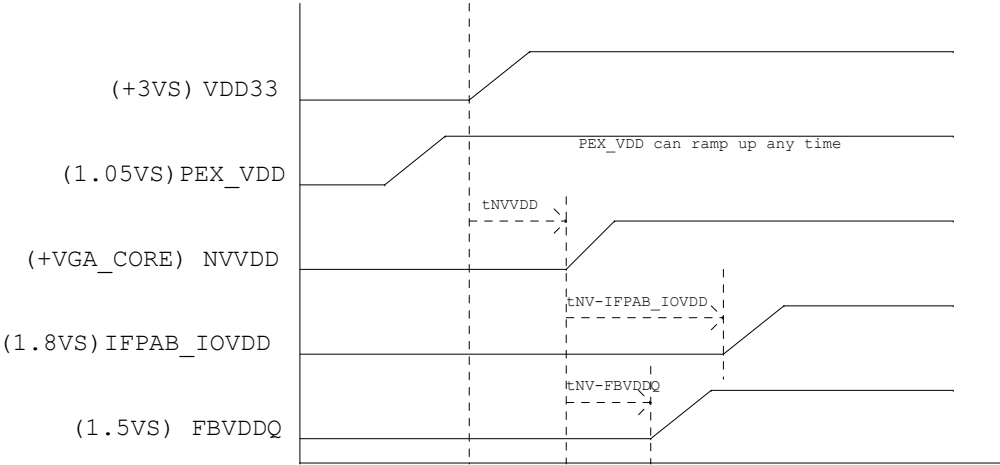
	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.5V)		FBVDDQ (GPU+Mem) (1.5V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N11M-GE1 64bit 512MB DDR3	14.02	2.16	TBD	TBD	12.9	12.26	0.66	0.99	1.3	1.95	530	0.56	84	0.15	140	0.15	38	0.13

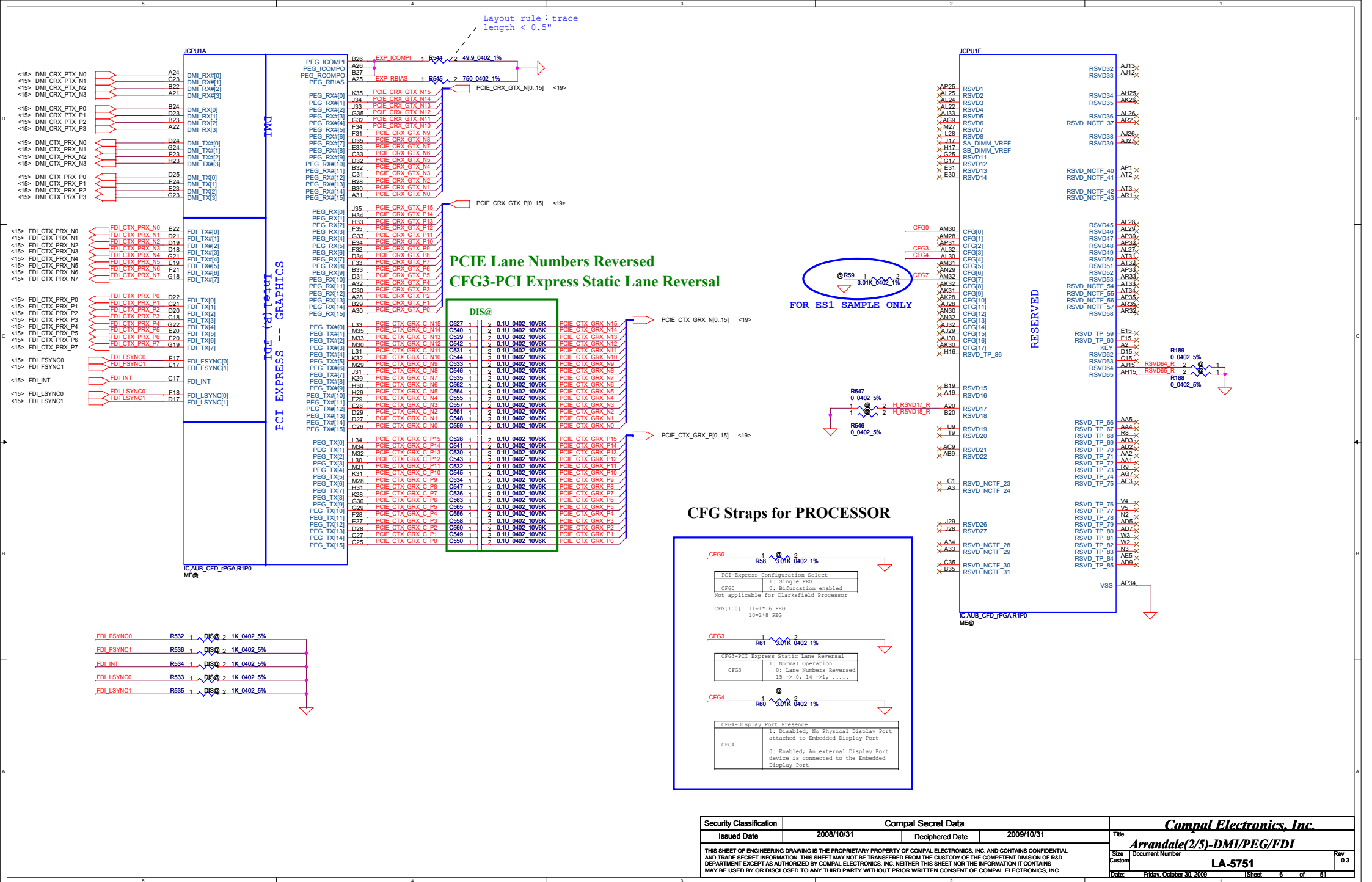
GPIO5 GPIO6

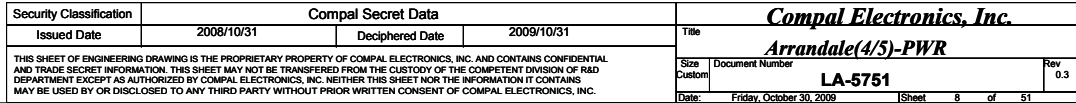
	Device ID	GPU_VID0	GPU_VID1	VGA_CORE	P-State
N11M-GE1/LP1 (40nm)	0x0A7D	0	0	0.8V	Deep P12
		0	1	0.85V	P8
		1	1	1.03V	P0

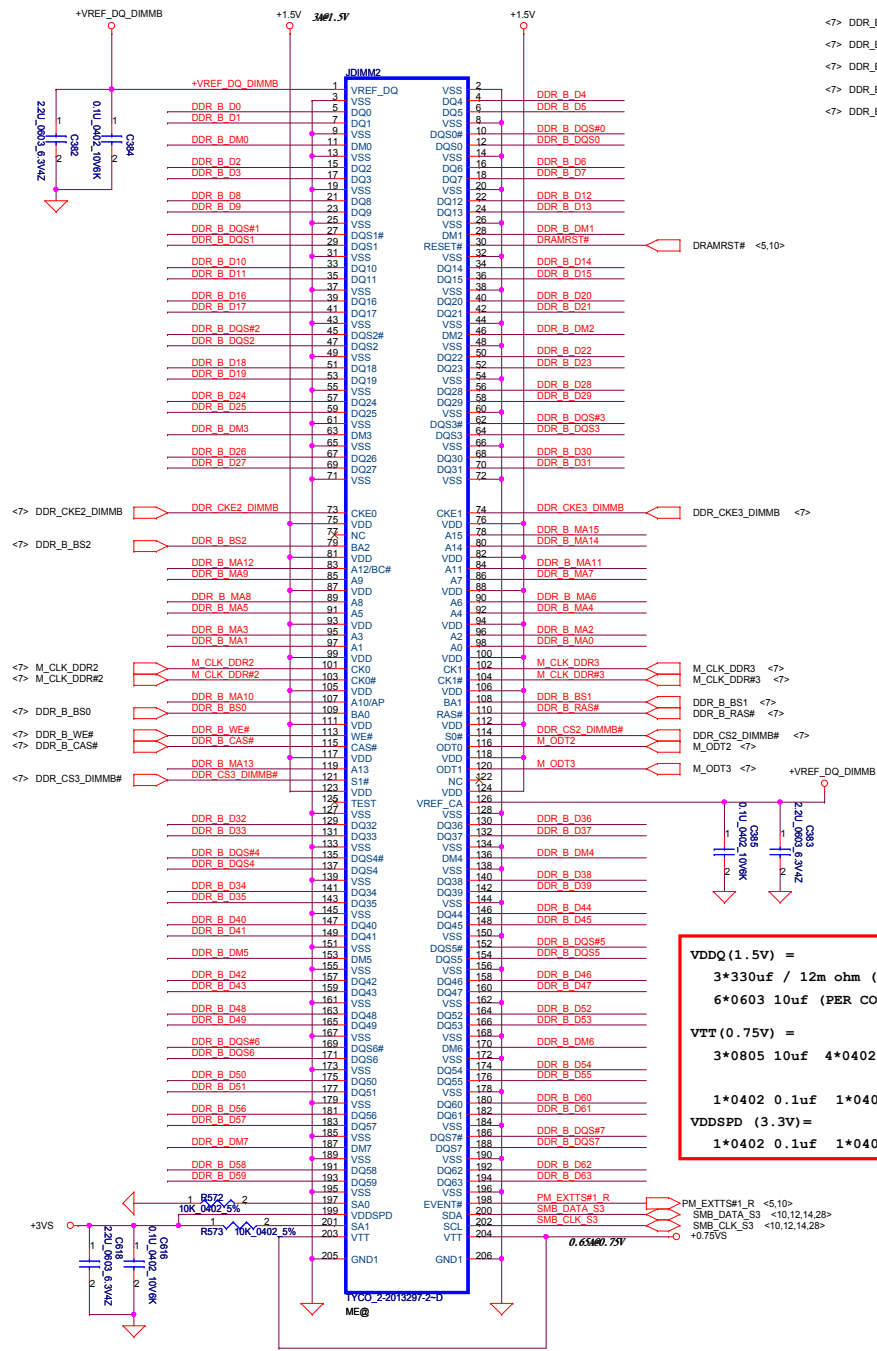
Power Sequence

The ramp time for any rail must be more than 40us

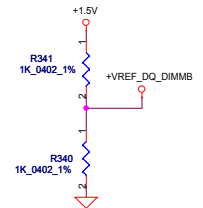






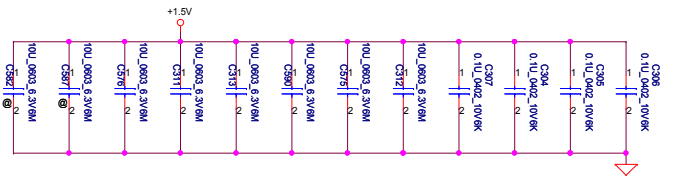


<7> DDR_B_DQS#0..7
<7> DDR_B_DQ[0..63]
<7> DDR_B_DM[0..7]
<7> DDR_B_DQS#0..7
<7> DDR_B_MA[0..15]



For Arranale only +VREF_DQ_DIMMB supply from a external 1.5V voltage divide circuit.
07/17/2009

Layout Note:
Place near DIMM



Layout Note:
Place near DIMM



VDDQ (1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMS)
6*0603 10uf (PER CONNECTOR)
VT (0.75V) =
3*0805 10uf 4*0402 1uf
1*0402 0.1uf 1*0402 2.2uf
VDDSPD (3.3V) =
1*0402 0.1uf 1*0402 2.2uf

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2008/10/31	Deciphered Date	2009/10/31	Title
					DDR3-SODIMM SLOT2
					Size Document Number
					LA-5751
					Rev 0.3
					Date: Friday, October 30, 2009
					Sheet 11 of 51

CLK GEN TO PCH

1. CLK_DMI
2. CLK_BUF_BCLK
3. CLK_BUF_CKSSCD
4. CLK_BUF_DOT96
5. CLK_14M_PCH

CLK GEN TO VGA

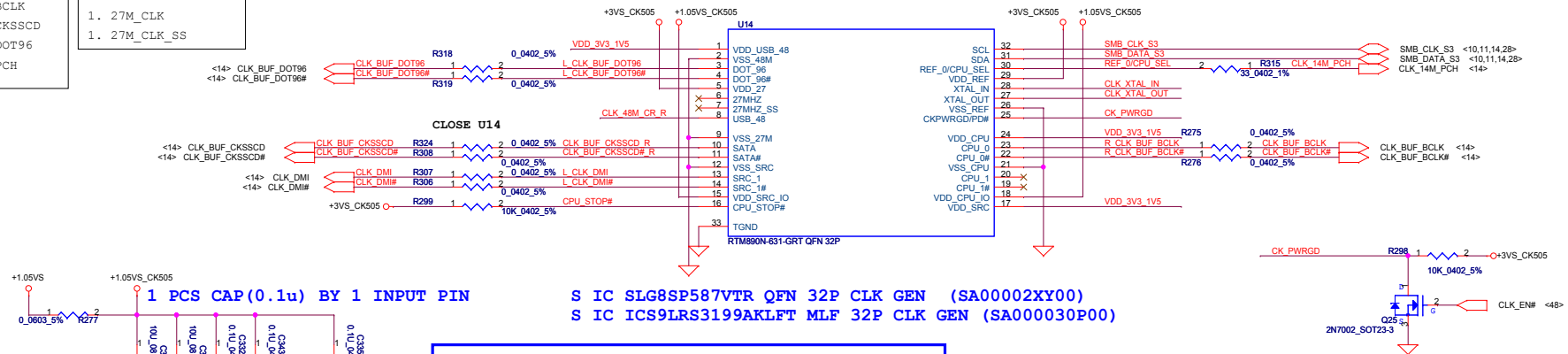
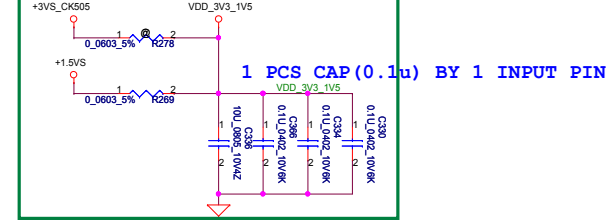
- Unused
1. 27M_CLK
 1. 27M_CLK_SS

Reserve for Low Power CLK GEN.

RTM890N-631 (SA00003HQ00)

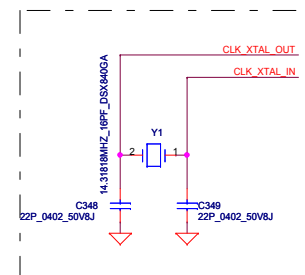
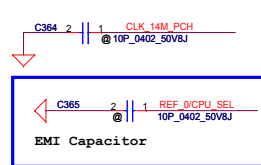
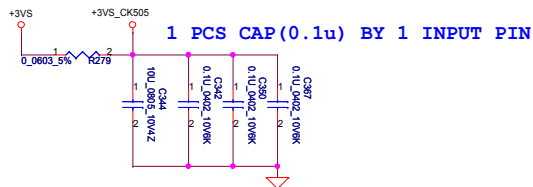
SLG8LV597VTR

9VLS3199 (SA00003HR00)

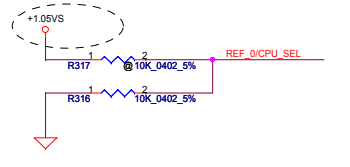


unstuff 09.09.08

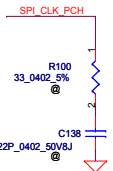
PIN8 IS GND FOR ICS3197
PIN8 IS 48MHz FOR ICS3199



PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

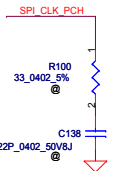


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Issued Date	2008/10/31	Deciphered Date	2009/10/31	Title	CLOCK GENERATOR
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				LA-5751	Rev 0.3
				Date	Friday, October 30, 2009
				Sheet	12 of 51



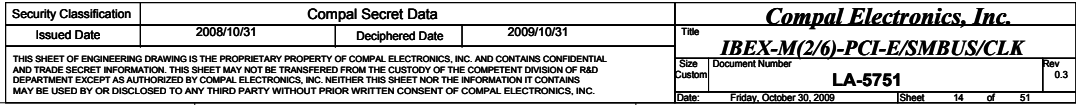
PCH JTAG TCK R114 1 2 51 0402 5% (2009,05,04)

FOR INTEL DPDG REV1.6 (MAY 2009)

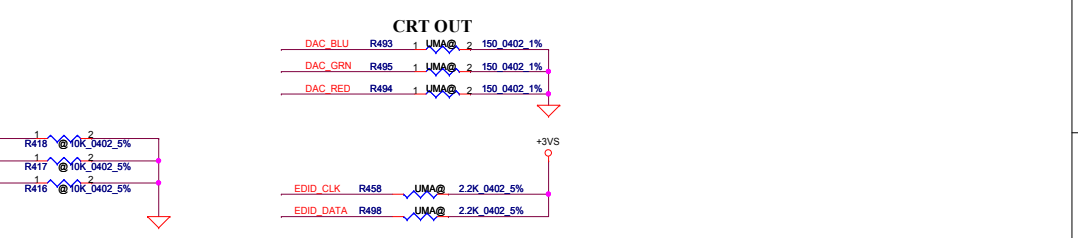
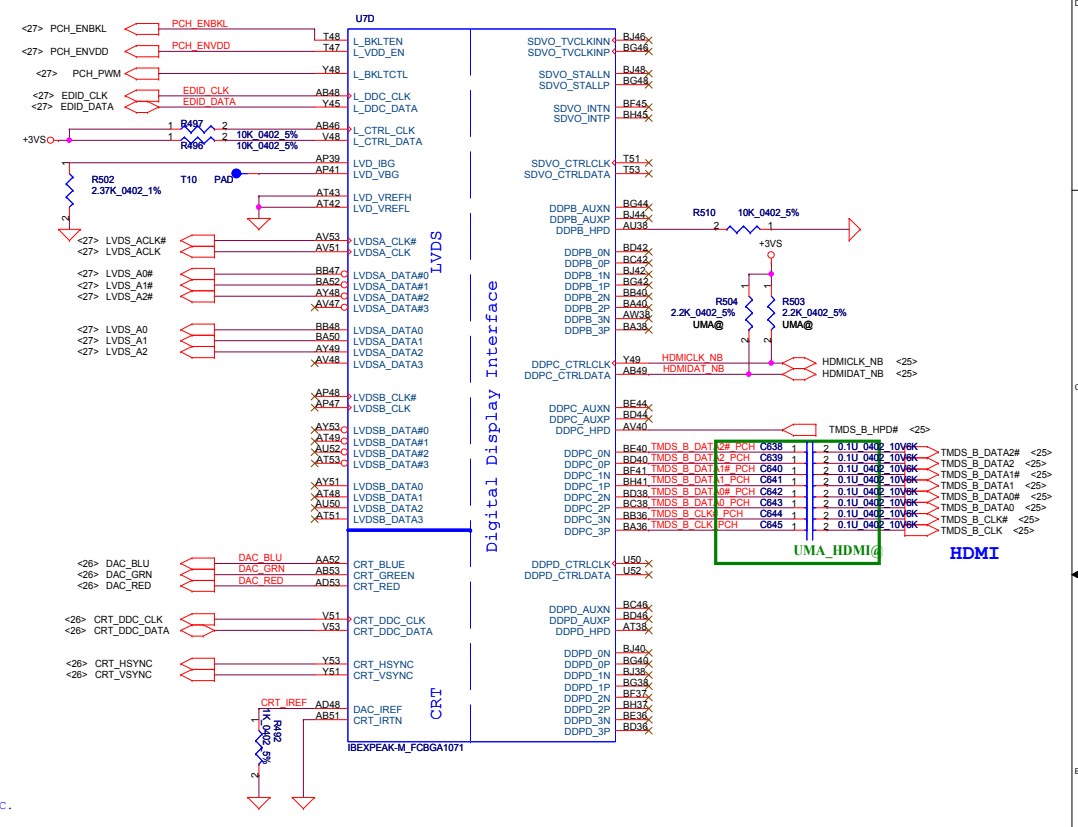
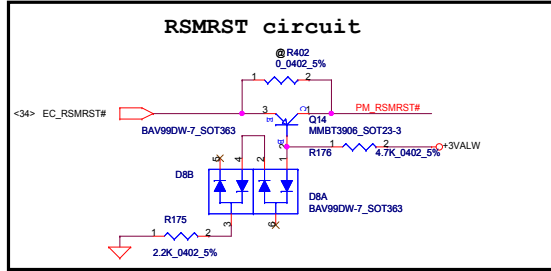
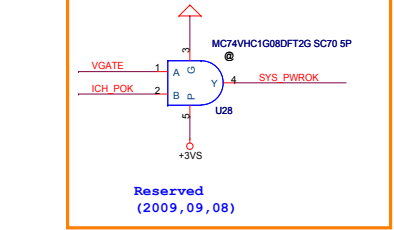
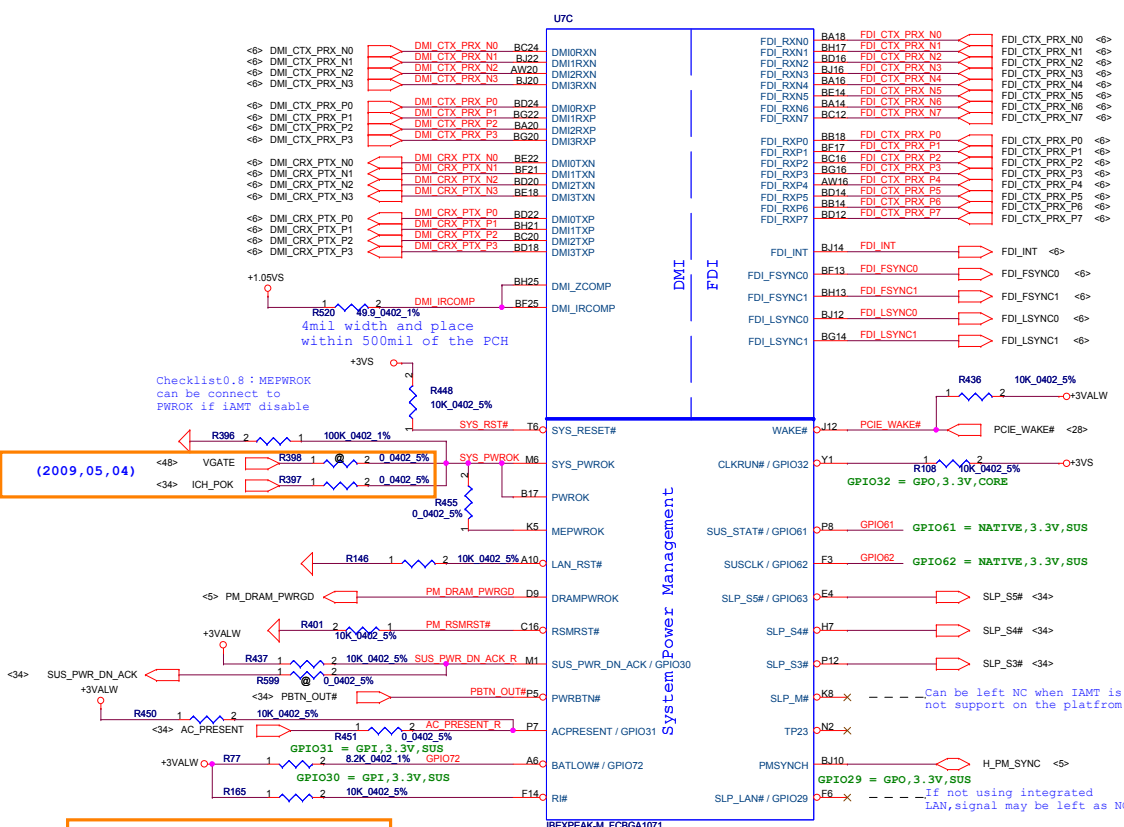


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Issued Date	2008/10/31	Deciphered Date	2009/10/31	Title		
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				Custom	LA-5751	0.3
				Date:	Friday, October 30, 2009	Sheet 13 of 51

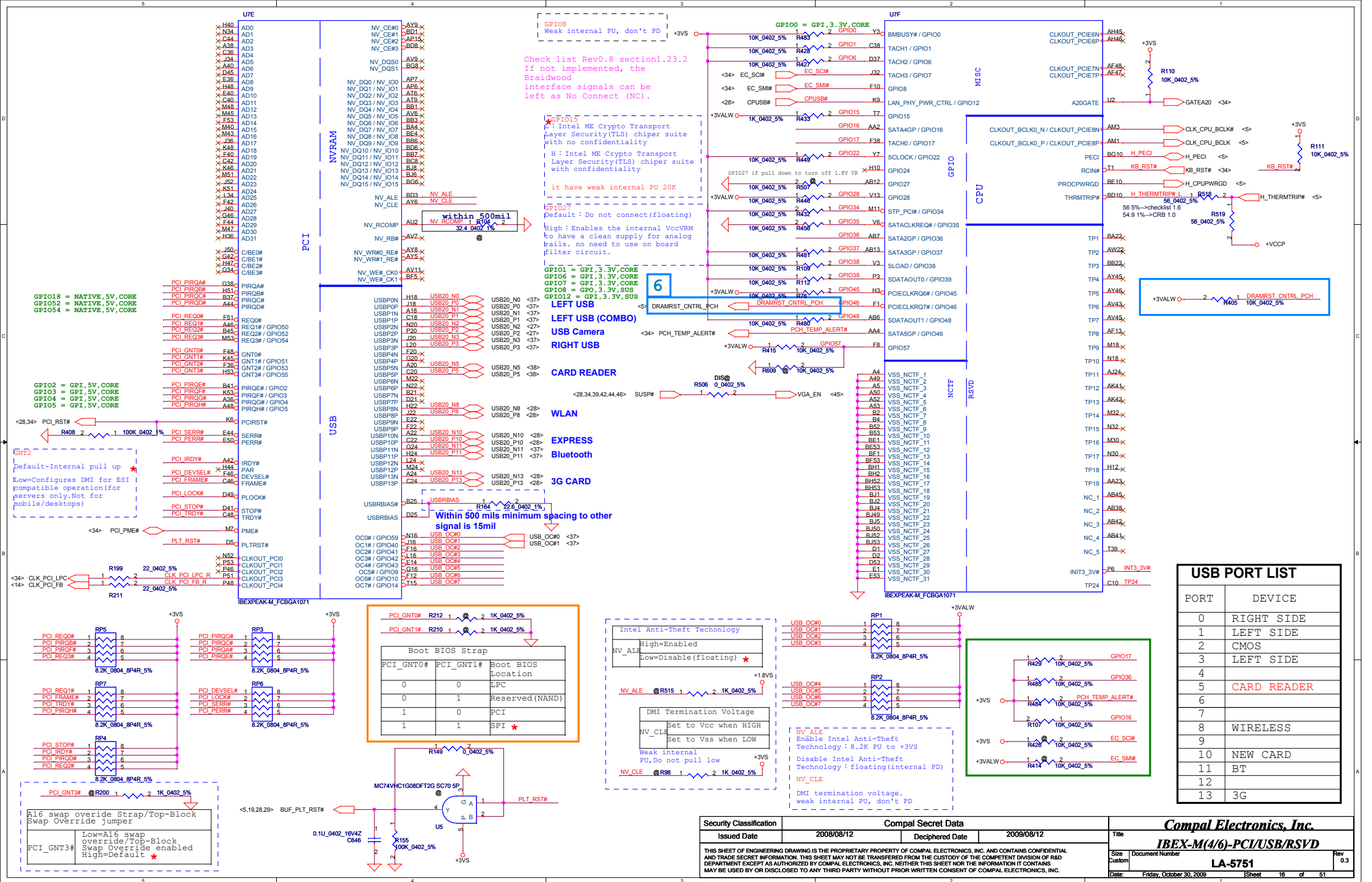
PCIE PORT LIST	
PORT	DEVICE
1	X
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	X
7	X
8	X



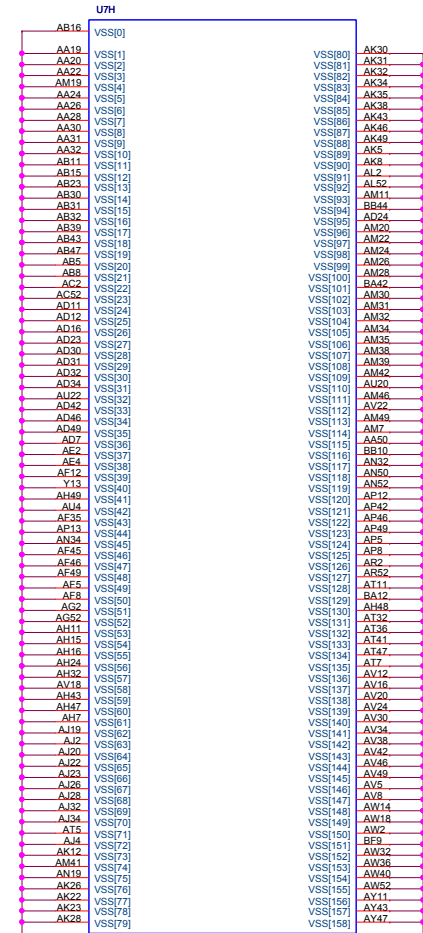
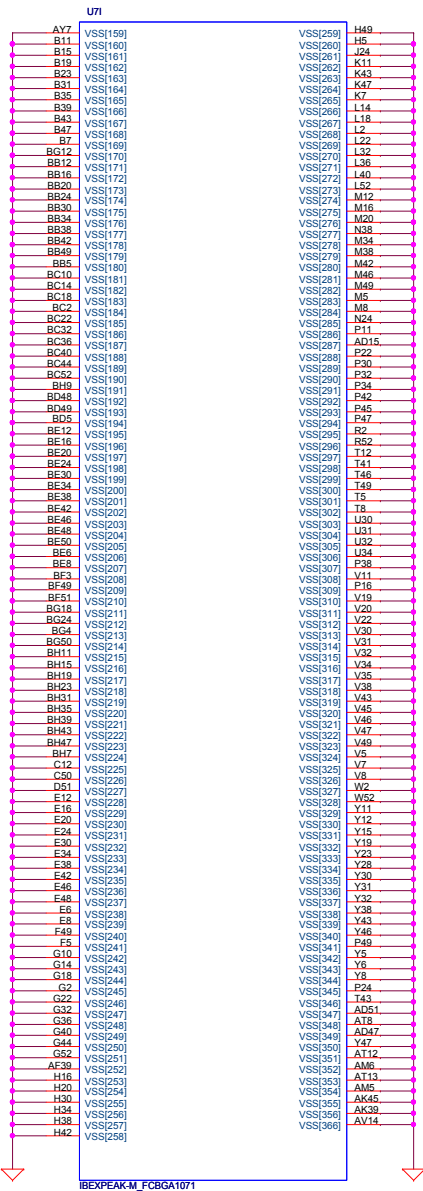
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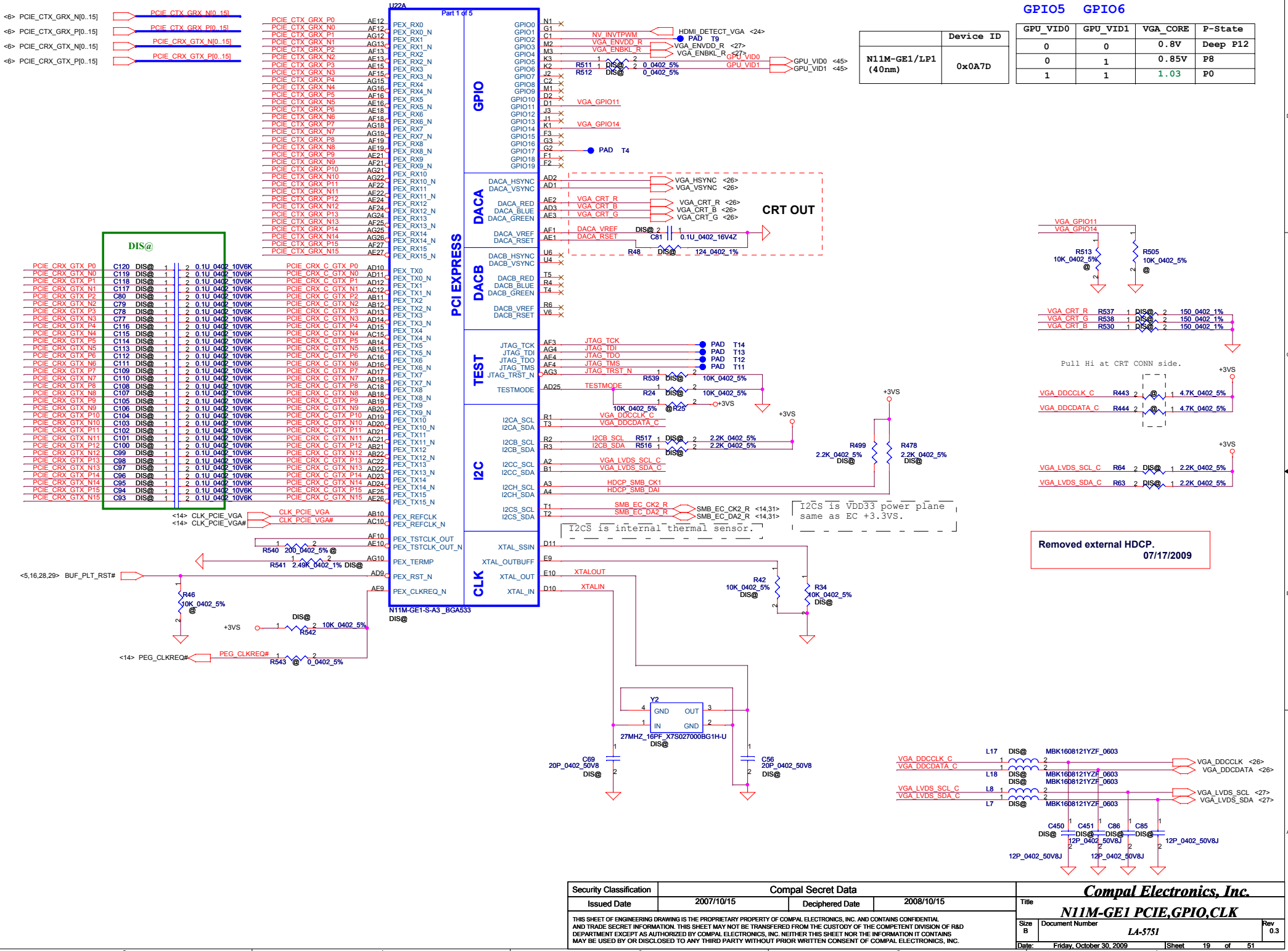
Security Classification		Compal Secret Data		Title	
Issued Date	2008/10/31	Deciphered Date	2009/10/31	IBEX-M(3/6)-DMI/GPIO/LVDS	
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Size	Document Number			Rev	0.3
Custom	LA-5751				
Date:	Friday, October 30, 2009	Sheet	15	of	51



USB PORT LIST	
PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	LEFT SIDE
4	
5	CARD READER
6	
7	
8	WIRELESS
9	
10	NEW CARD
11	BT
12	
13	3G



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Issued Date		2008/10/31	Deciphered Date	2009/10/31	IBEX-M(6/6)-GND
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Size Custom		Document Number		LA-5751	
Date		Thursday, October 29, 2009		Sheet 18 of 51	

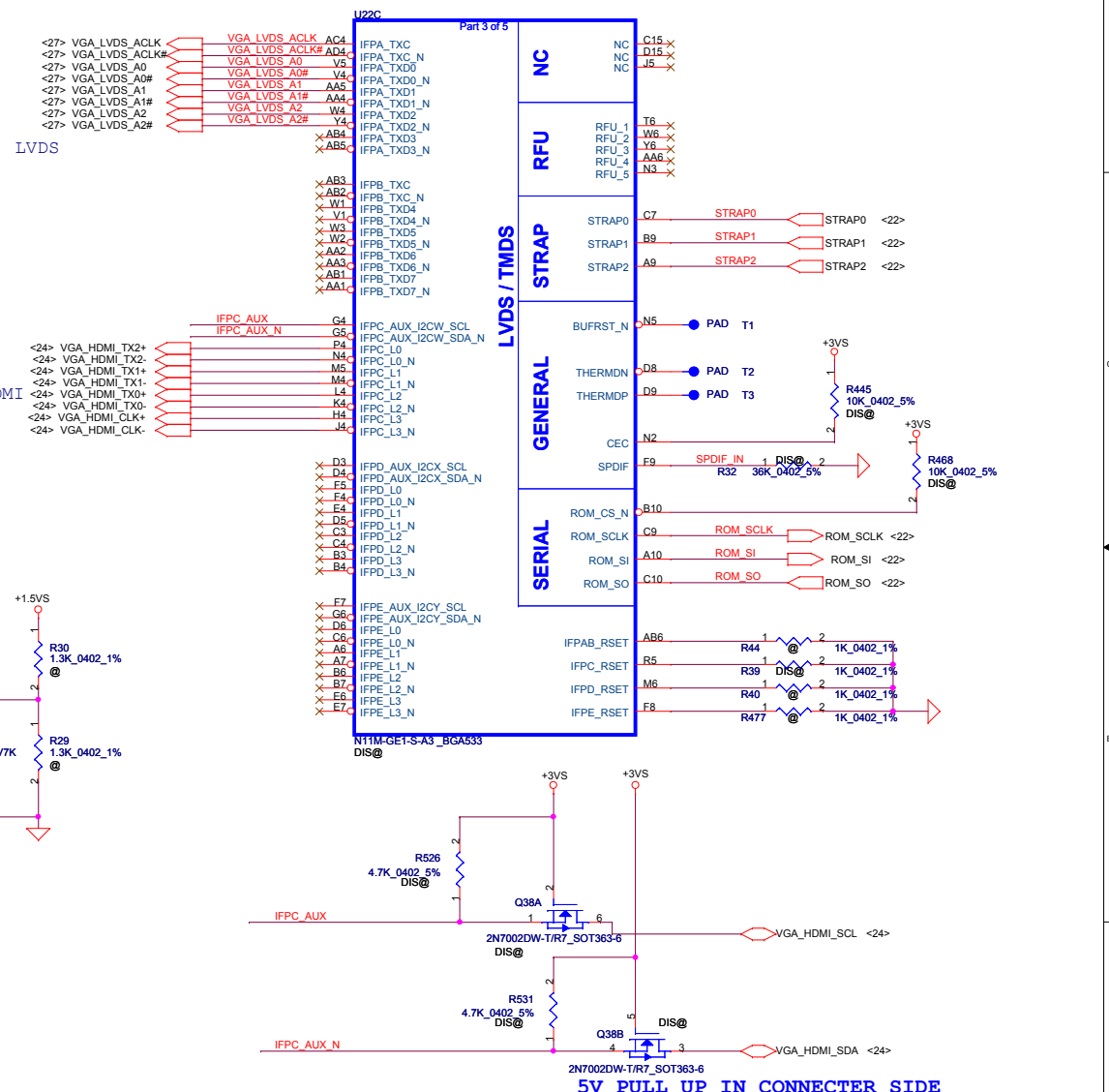
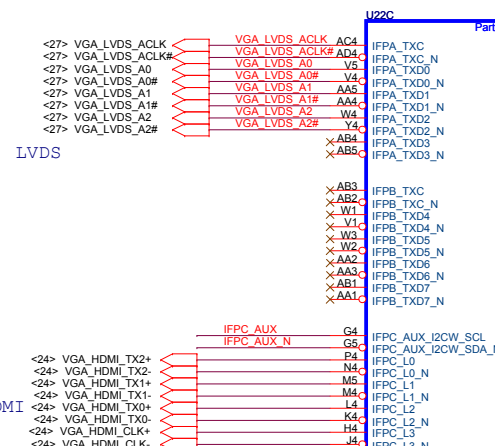
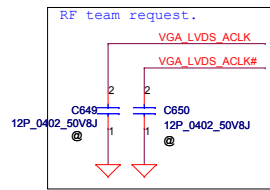


	Device ID
N11M-GE1/LP1 (40nm)	0x0A7D

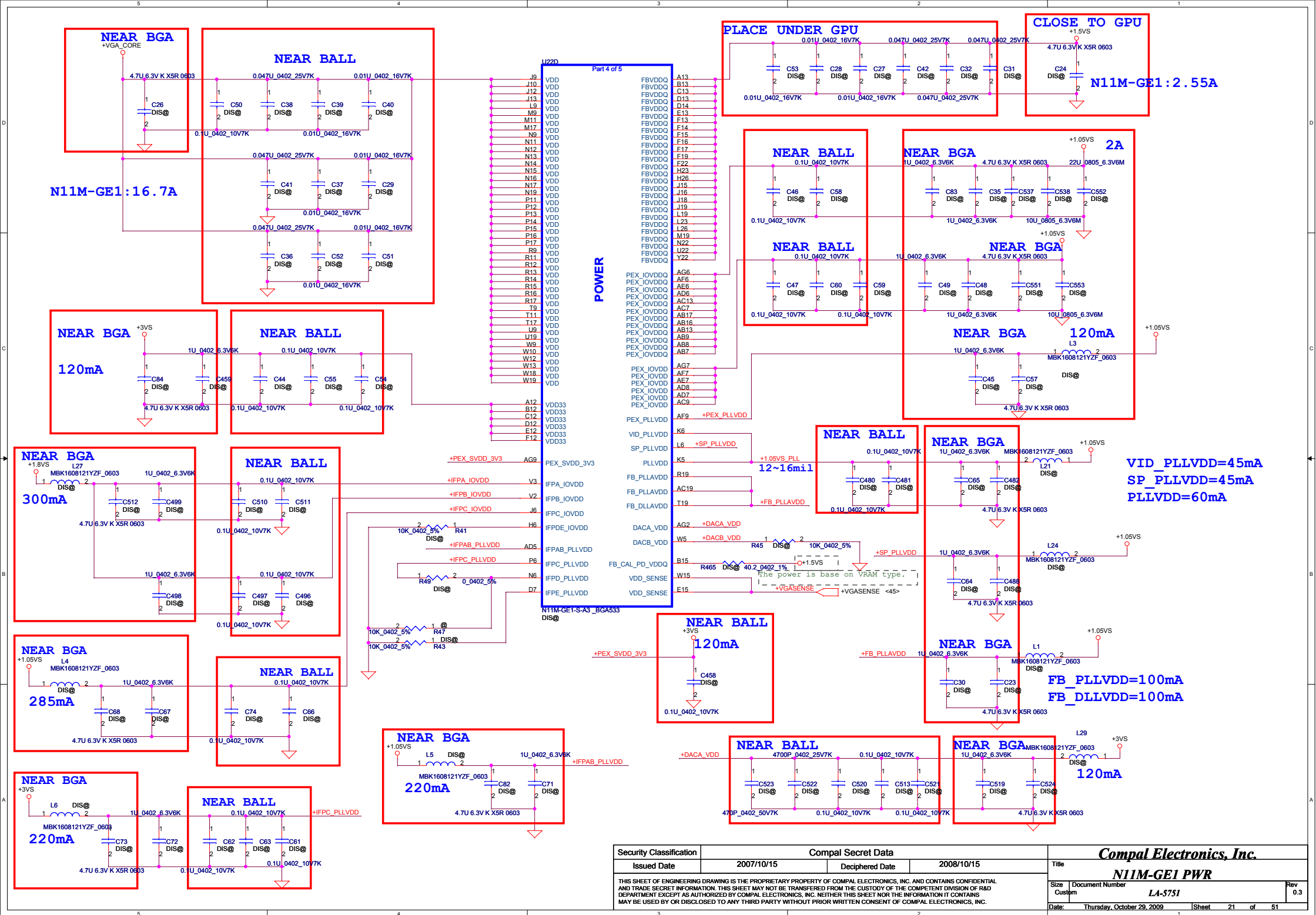
GPIO5	GPIO6	VGA_CORE	P-State
GPU_VID0	GPU_VID1	0.8V	Deep P12
0	0	0.85V	P8
0	1	1.03	P0
1	1		

Security Classification	Compal Secret Data	
Issued Date	2007/10/15	Deciphered Date
		2008/10/15
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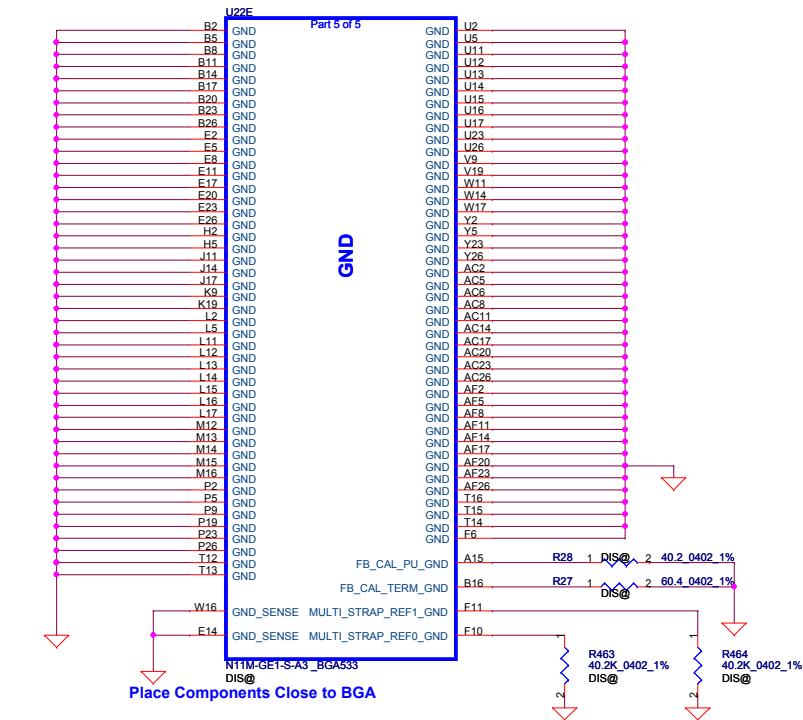
Compal Electronics, Inc.			
N11M-GE1 PCIE,GPIO,CLK			
Size B	Document Number	Rev 0.3	
	LA-3751		
Date:	Friday, October 30, 2009	Sheet	19 of 51



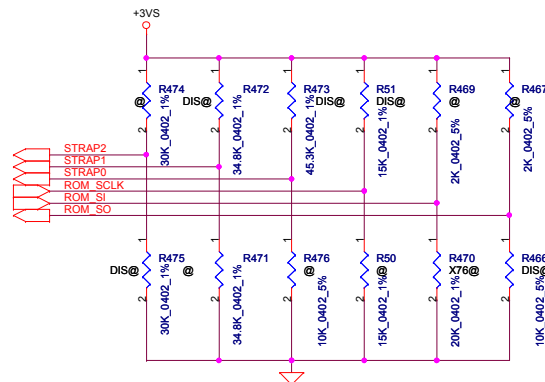
Security Classification		Compal Secret Data		Compal Electronics, Inc. N11M-GE1 LVDS, Memory Bus	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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Date:				Friday, October 30, 2009	Sheet 20 of 51



A total of 8 signals are required for GB1 strapping this includes
2 reference signals
6 physical strapping pins
4 logical strapping bits
A total of 24 logical strapping bits are available



<20> STRAP2
<20> STRAP1
<20> STRAP0
<20> ROM_SCLK
<20> ROM_SI
<20> ROM_SO



STRAP1 use for 3GIO_PADCFG to set 35K pull up.
(PUN-04335-001_V10 HW9 update)

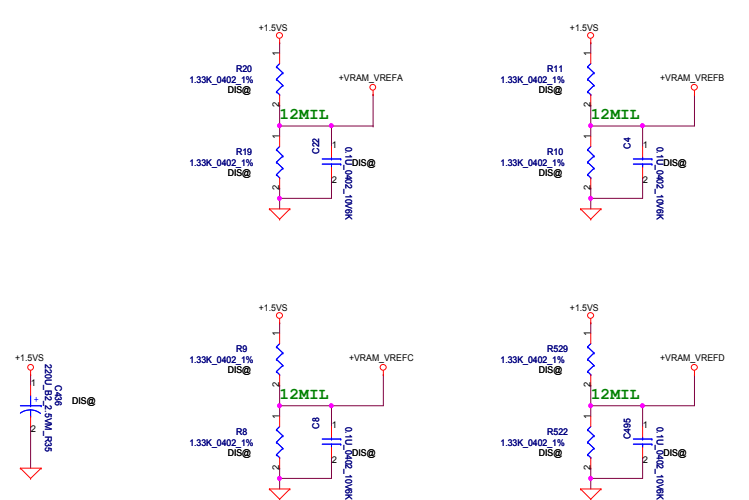
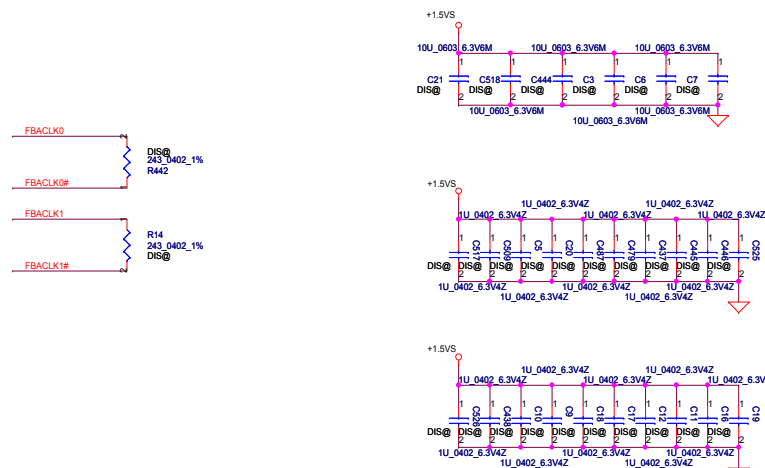
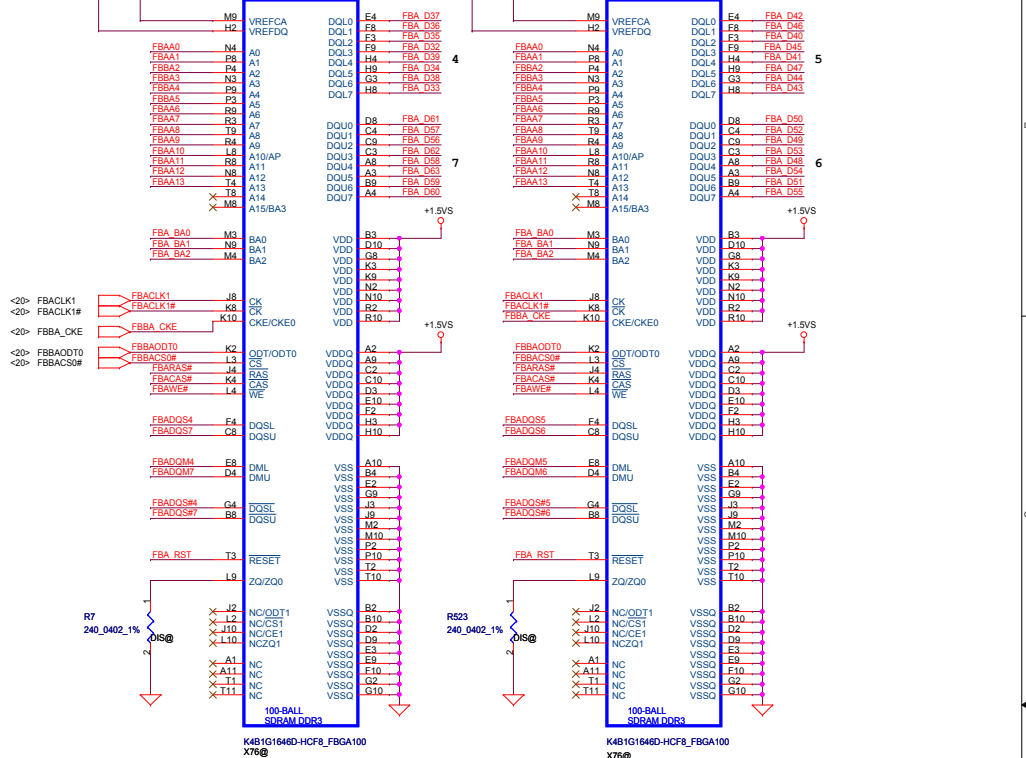
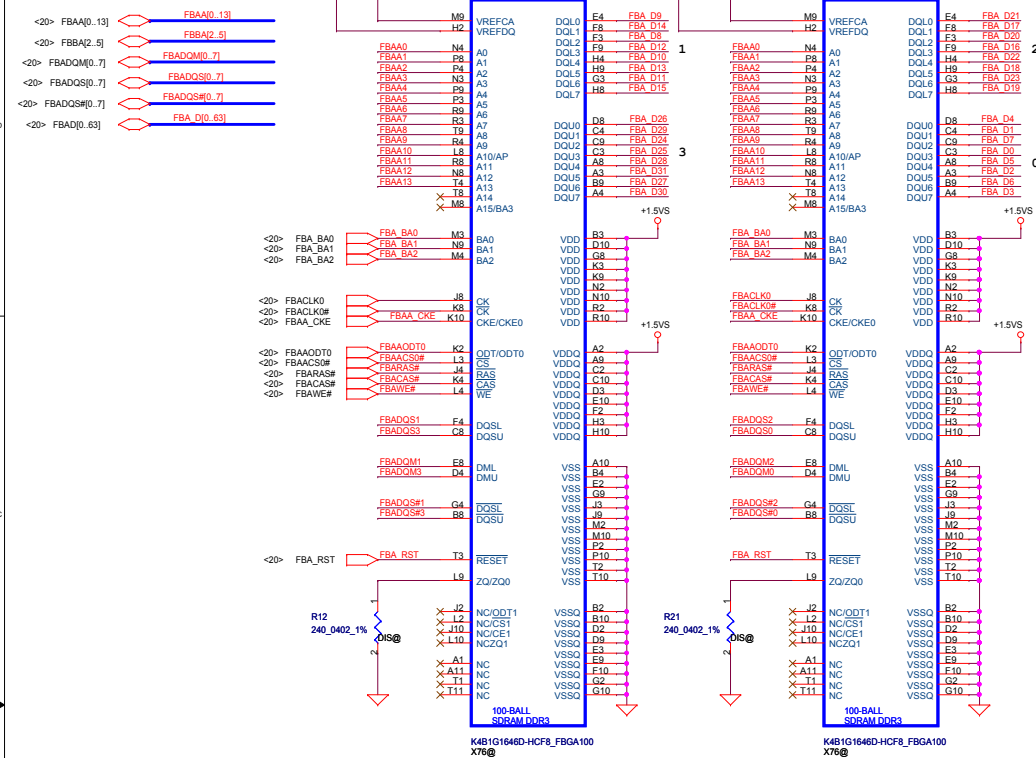
GPU	FB Memory (DDR3)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N11M-GE1 LP1 (0x0A7D) 40nm	Samsung 800MHz (default)	K4W1G1646E-HC12					
		64Mx16	PD 10K	PU 15K	PD 20K	PD 30K	PU 35K PU 45K
	Hynix 800MHz	H5TQ1G63BFR-12C					
		64Mx16	PD 10K	PU 15K	PD 15K	PD 30K	PU 35K PU 45K
X76							

N11M-GE1 LP1	Memory/PKG	FBVDDQ	FB_CAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
	DDR3	+1.5VS	40.2 ohm	40.2 ohm	40.2/60.4 ohm

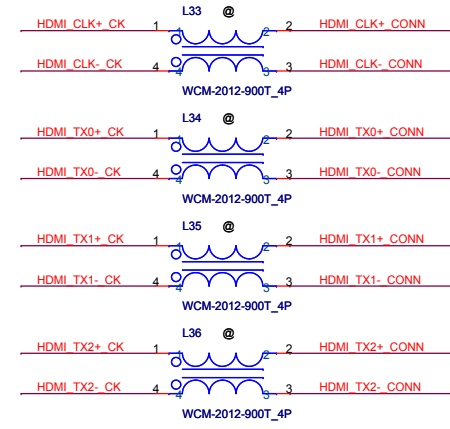
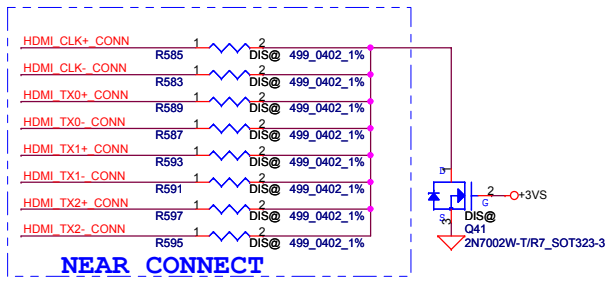
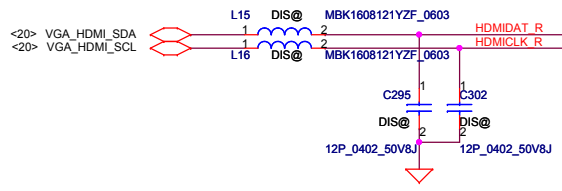
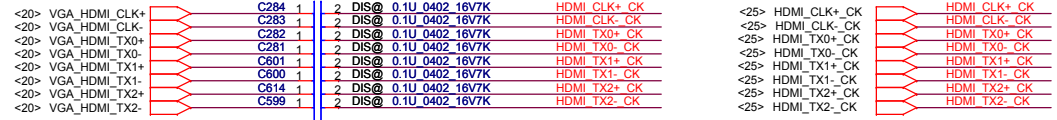
Must be used 1% resistor for driver calibration

DG-04642-001-V01(May 22, 2009)

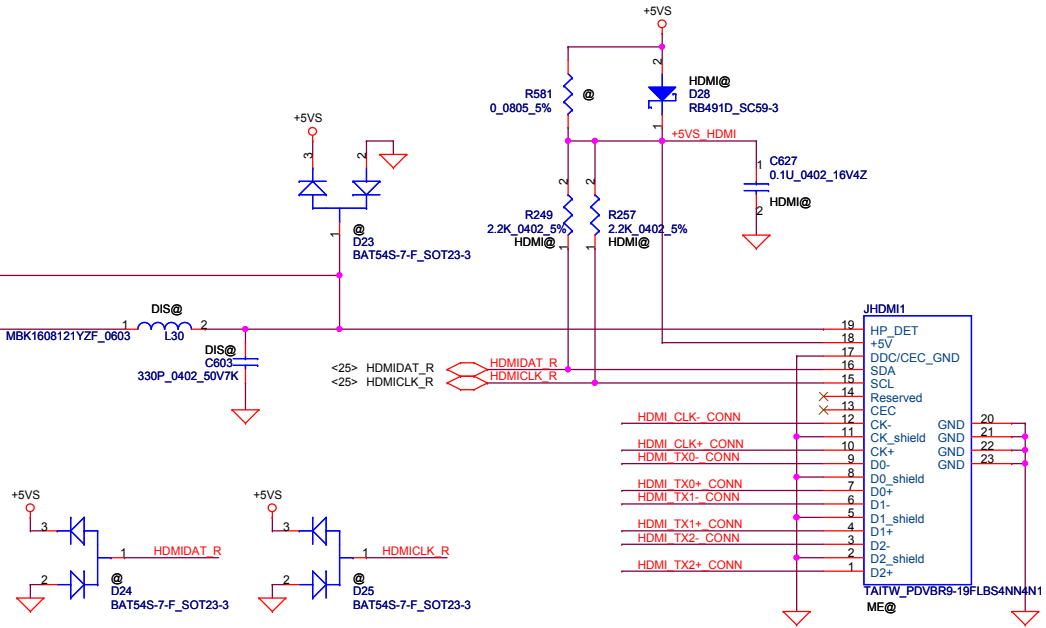
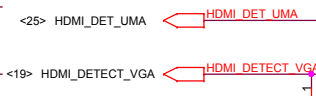
N11x 40nm DDR3 MAPPING
NVIDIA COCUMENT FOR DA-3978-001



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					VRAM DDR3	
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						Size C
				LA-5751	0.3	
Date:		Thursday, October 29, 2009		Sheet	23	of 51



HDMI_CLK+ CK	R584	HDMI@	2	0.0402 5%	HDMI_CLK+ CONN
HDMI_CLK- CK	R582	HDMI@	2	0.0402 5%	HDMI_CLK- CONN
HDMI_TX0+ CK	R588	HDMI@	2	0.0402 5%	HDMI_TX0+ CONN
HDMI_TX0- CK	R586	HDMI@	2	0.0402 5%	HDMI_TX0- CONN
HDMI_TX1+ CK	R592	HDMI@	2	0.0402 5%	HDMI_TX1+ CONN
HDMI_TX1- CK	R590	HDMI@	2	0.0402 5%	HDMI_TX1- CONN
HDMI_TX2+ CK	R596	HDMI@	2	0.0402 5%	HDMI_TX2+ CONN
HDMI_TX2- CK	R594	HDMI@	2	0.0402 5%	HDMI_TX2- CONN

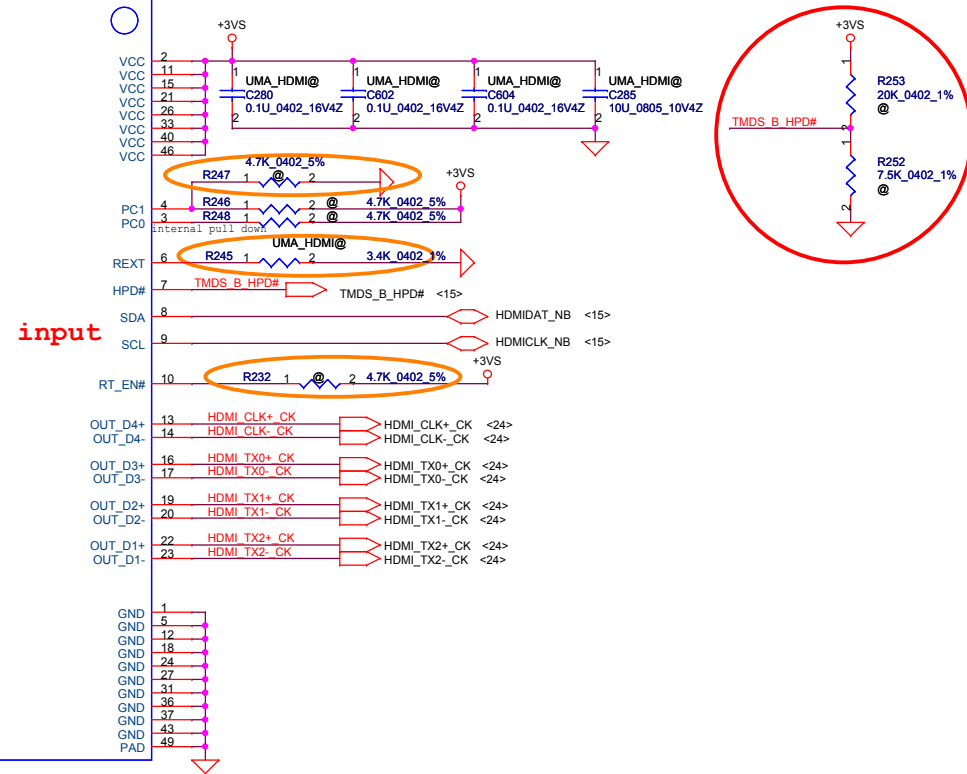


Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
Issued Date		2008/03/25		Title	
		Deciphered Date		HDMI CONN	
		2008/04/		Size	
				Custom	
				Document Number	
				LA-5751	
				Date	
				Friday, October 30, 2009	
				Sheet	
				24 of 51	

P/N:SA00002D700 (8101T)
P/N:SA00001U900 (CH7318A)

PIN6 PULL DOWN 1.2Kohm

PIN7 PULL DOWN 7.5Kohm
PIN7 PULL UP 20Kohm

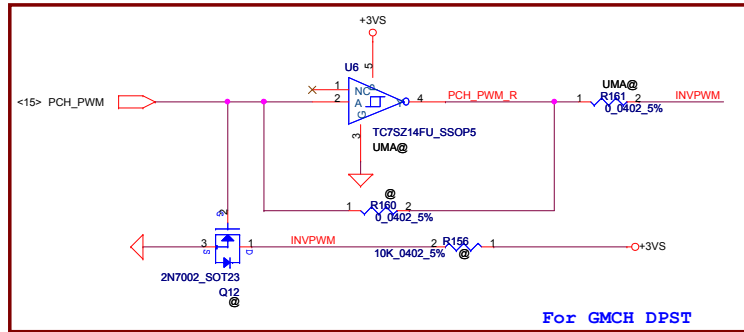
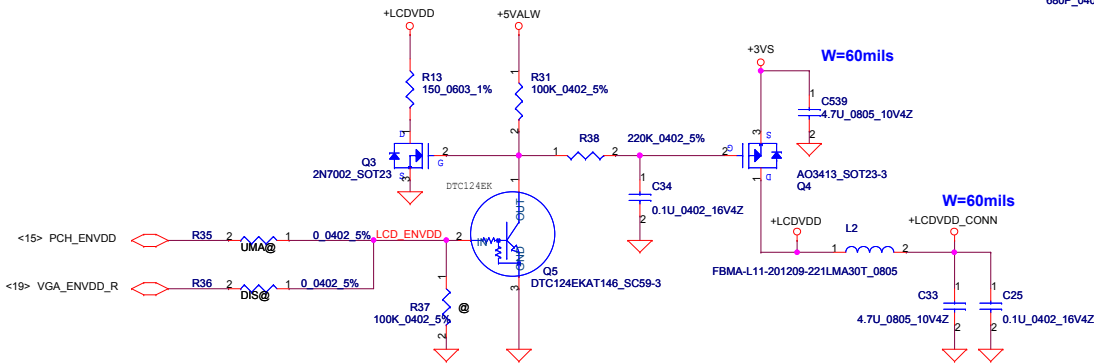


Security Classification		Compal Secret Data		Compal Electronics, Ltd.		
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	Level Shifter _ASM1442	
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				Custom	LA-5751	0.3
Date: Thursday, October 29, 2009				Sheet	25	of 51



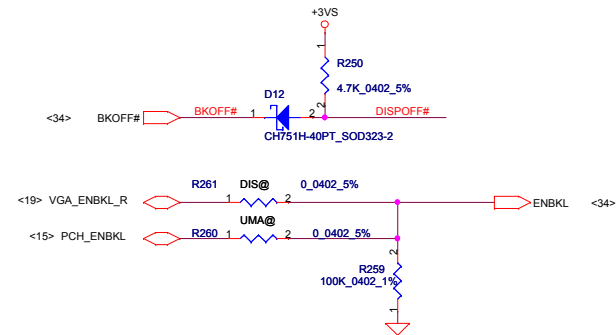
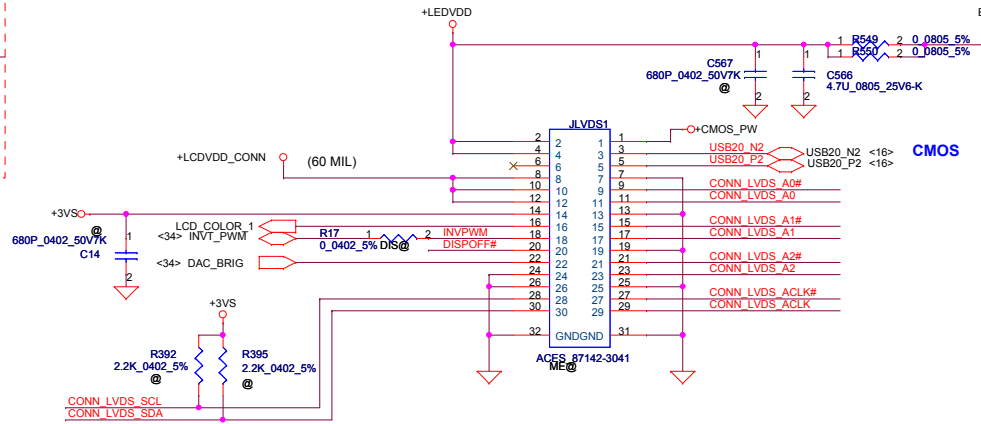
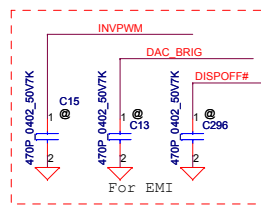
Security Classification		Compal Secret Data		Compal Electronics, Inc. CRT Connector		
Issued Date	2007/10/15	Deciphered Date	2008/10/15			
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				Size	Document Number	Rev
				Custom	LA-5751	0.3
Date:				Thursday, October 29, 2009	Sheet	26 of 51

LCD POWER CIRCUIT

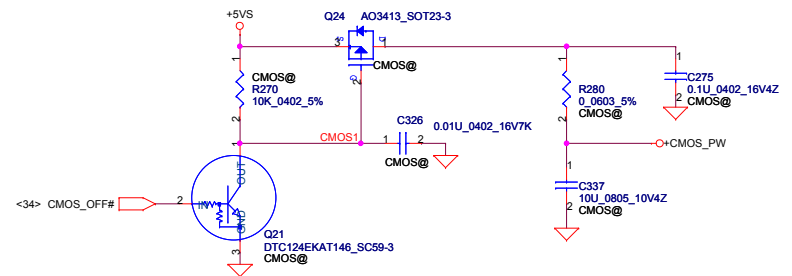


<19> VGA_LVDS_SCL VGA_LVDS_SCL 0.0402_5% 2 DIS@ 1 R390 CONN LVDS_SCL
 <19> VGA_LVDS_SDA VGA_LVDS_SDA 0.0402_5% 2 DIS@ 1 R391 CONN LVDS_SDA
 <20> VGA_LVDS_A0 VGA_LVDS_A0 0.0402_5% 2 DIS@ 1 R86 CONN LVDS_A0
 <20> VGA_LVDS_A0# VGA_LVDS_A0# 0.0402_5% 2 DIS@ 1 R85 CONN LVDS_A0#
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 <20> VGA_LVDS_A1# VGA_LVDS_A1# 0.0402_5% 2 DIS@ 1 R128 CONN LVDS_A1#
 <20> VGA_LVDS_A2 VGA_LVDS_A2 0.0402_5% 2 DIS@ 1 R126 CONN LVDS_A2
 <20> VGA_LVDS_A2# VGA_LVDS_A2# 0.0402_5% 2 DIS@ 1 R127 CONN LVDS_A2#
 <20> VGA_LVDS_ACLK VGA_LVDS_ACLK 0.0402_5% 2 DIS@ 1 R84 CONN LVDS_ACLK
 <20> VGA_LVDS_ACLK# VGA_LVDS_ACLK# 0.0402_5% 2 DIS@ 1 R125 CONN LVDS_ACLK#

<15> EDID_CLK EDID_CLK 0.0402_5% 2 UMA@ 1 R393 CONN LVDS_SCL
 <15> EDID_DATA EDID_DATA 0.0402_5% 2 UMA@ 1 R394 CONN LVDS_SDA
 <15> LVDS_A0 LVDS_A0 0.0402_5% 2 UMA@ 1 R383 CONN LVDS_A0
 <15> LVDS_A0# LVDS_A0# 0.0402_5% 2 UMA@ 1 R382 CONN LVDS_A0#
 <15> LVDS_A1 LVDS_A1 0.0402_5% 2 UMA@ 1 R389 CONN LVDS_A1
 <15> LVDS_A1# LVDS_A1# 0.0402_5% 2 UMA@ 1 R388 CONN LVDS_A1#
 <15> LVDS_A2 LVDS_A2 0.0402_5% 2 UMA@ 1 R386 CONN LVDS_A2
 <15> LVDS_A2# LVDS_A2# 0.0402_5% 2 UMA@ 1 R387 CONN LVDS_A2#
 <15> LVDS_ACLK LVDS_ACLK 0.0402_5% 2 UMA@ 1 R384 CONN LVDS_ACLK
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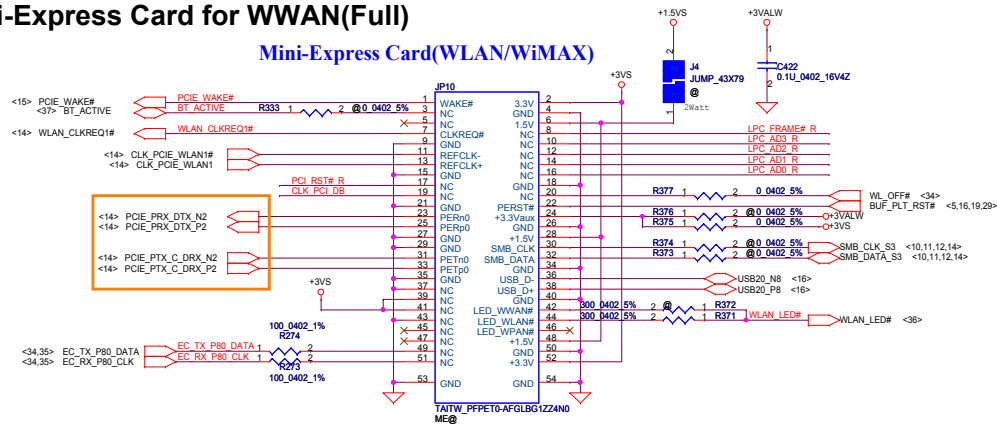
CMOS Camera



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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
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				Size B	Document Number
				LA-5751	
				Date: Friday, October 30, 2009	Rev 0.3
				Sheet 27 of 51	

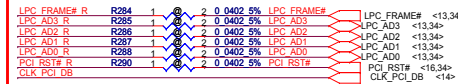
Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for WWAN(Full)

Mini-Express Card(WLAN/WiMAX)

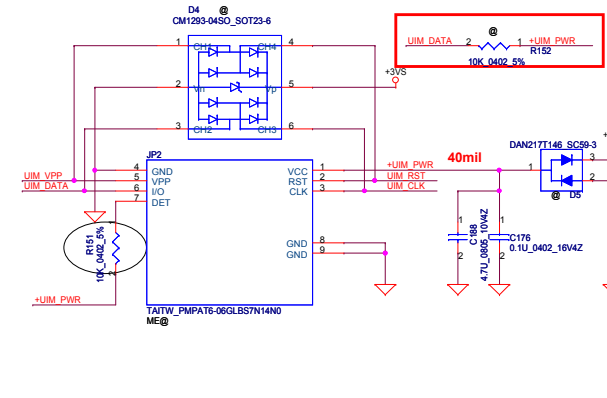
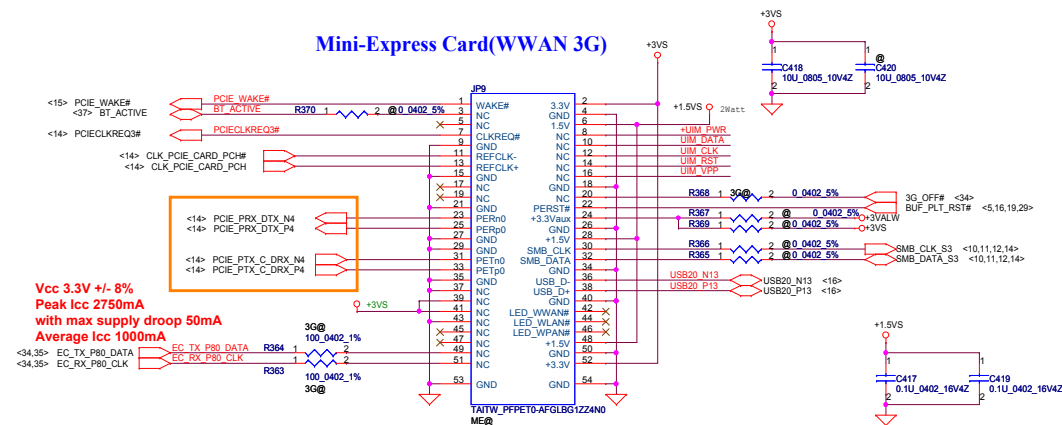


Reserve for SW mini-pcie debug card.

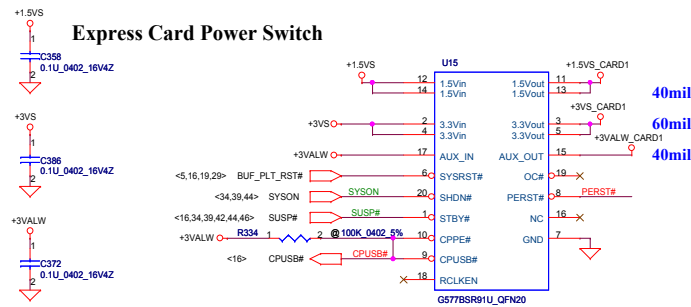
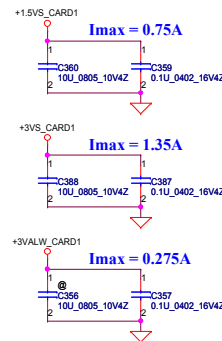
Series resistors closed to KBC side.



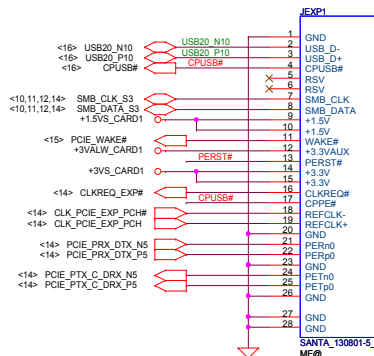
Mini-Express Card(WWAN 3G)



Express Card Power Switch

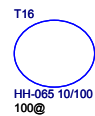
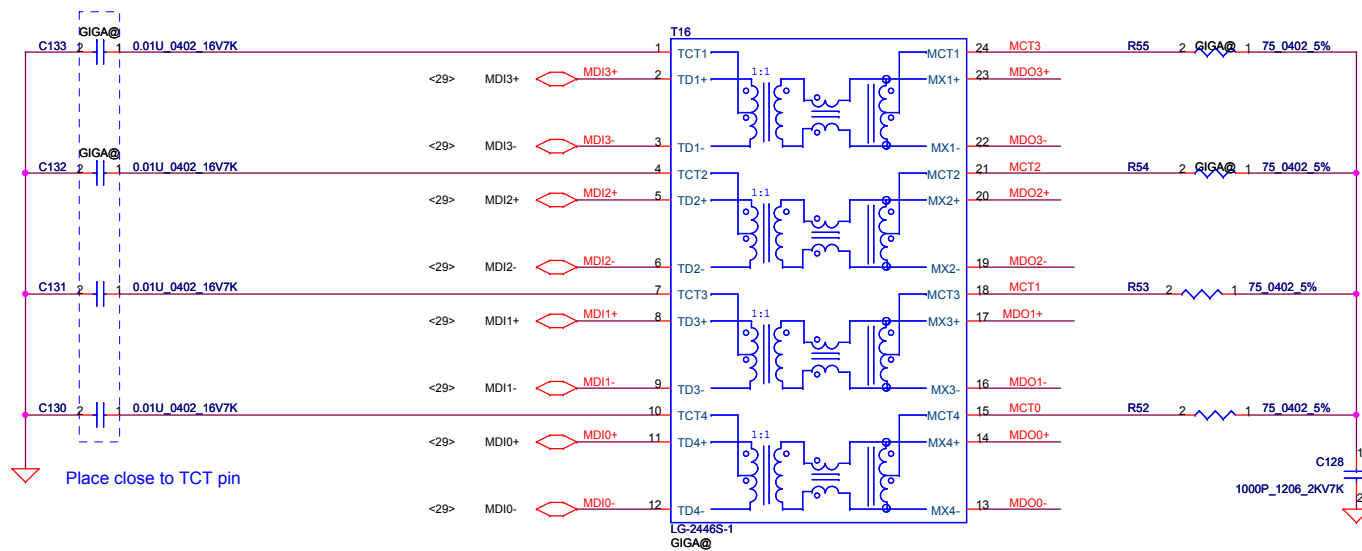

$$I_{\max} = 0.75\text{A}$$

$$I_{\max} = 1.35 \text{ A}$$
$$I_{\max} = 0.275 \text{ A}$$

New Card 34mm Socket (Left/TOP)



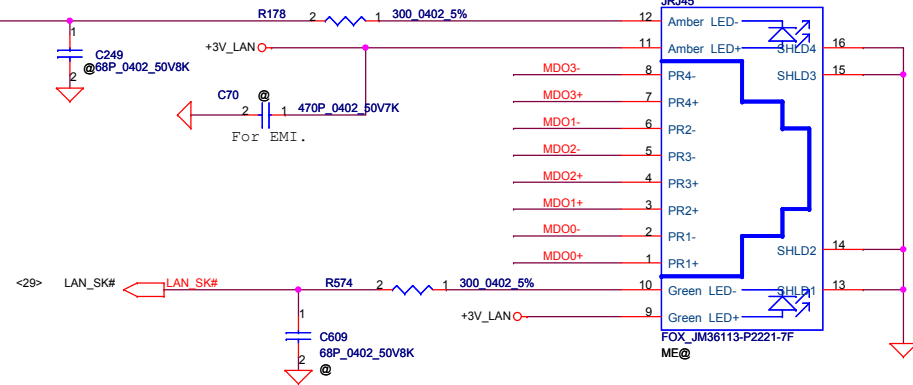
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title Mini-Card/Nwe Card/SIM
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Date:	Friday, October 30, 2009	Sheet	28 of 51	Rev 0.3

Close to T14

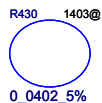


<29> ACTIVITY#

ACTIVITY#

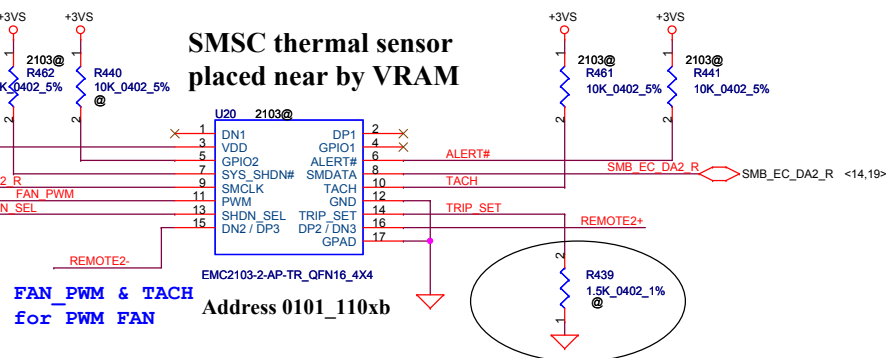


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								Size		Document Number			Rev		
								Custom		LA-5751			0.3		
								Date:		Friday, October 30, 2009			Sheet 30 of 51		

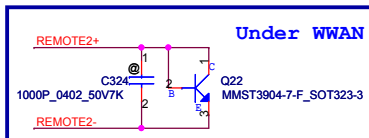
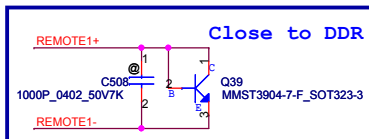


1403:
@C508/@C324=100p

SMSC thermal sensor placed near by VRAM

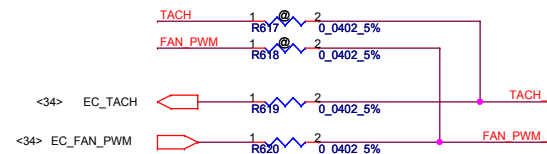
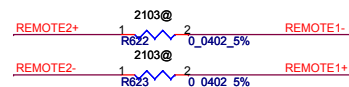
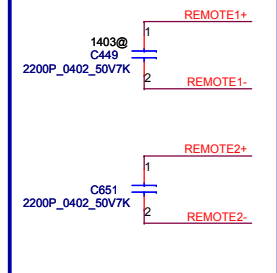


internal pull up 1.2K to 1.5V
R for initial thermal
shutdown temp

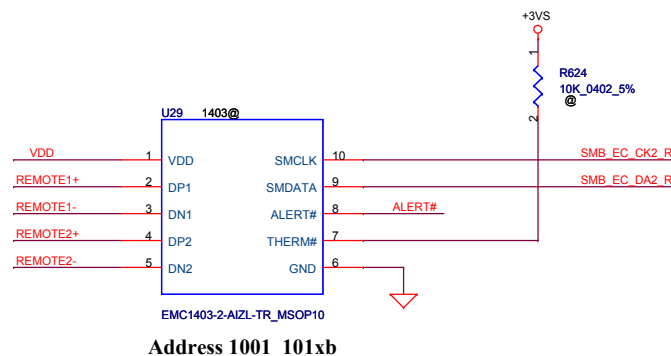


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

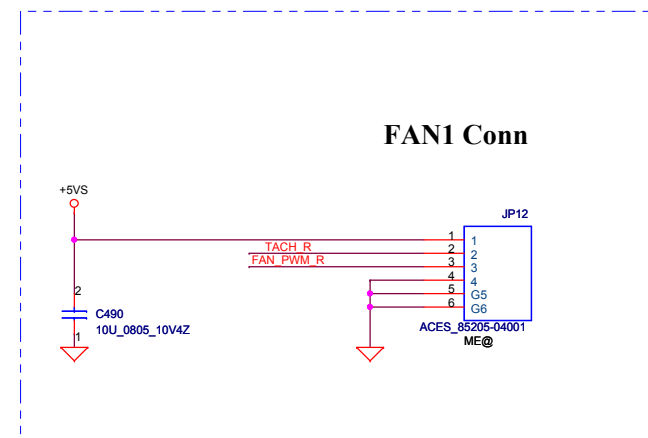
Close U20



Shutdown Temp	TRIP_SET R439 (1%)
93	953ohm
94	1020ohm
95	1100ohm
96	1150ohm
97	1240ohm
98	1330ohm
99	1400ohm
100	1500ohm
101	1580ohm
102	1690ohm
103	1820ohm
104	1960ohm
105	2050ohm

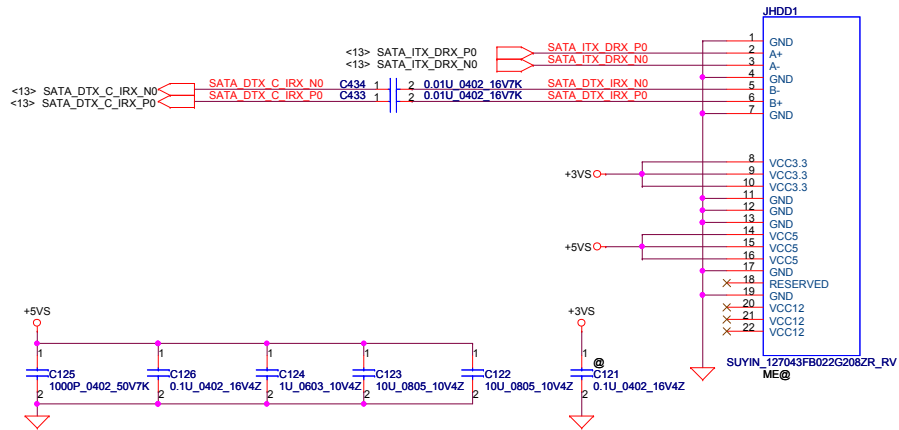


FAN1 Conn

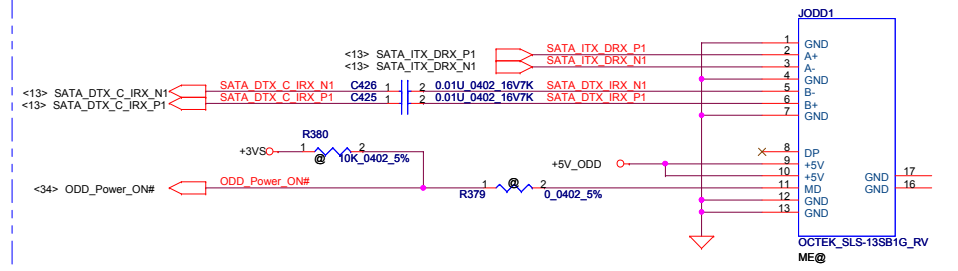


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				Date: Friday, October 30, 2009	Sheet 31 of 51

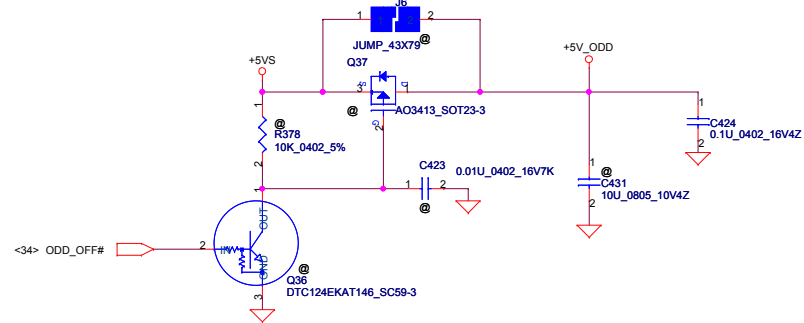
SATA HDD Conn.



SATA ODD Conn.



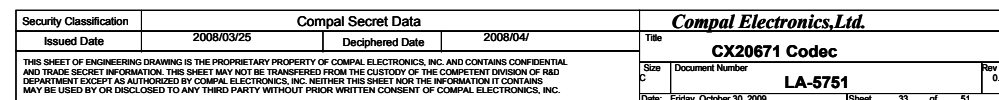
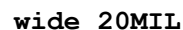
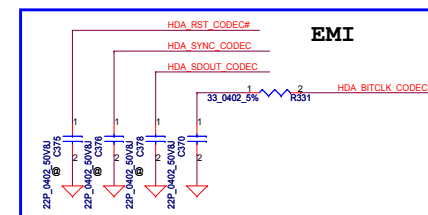
ODD Power Control

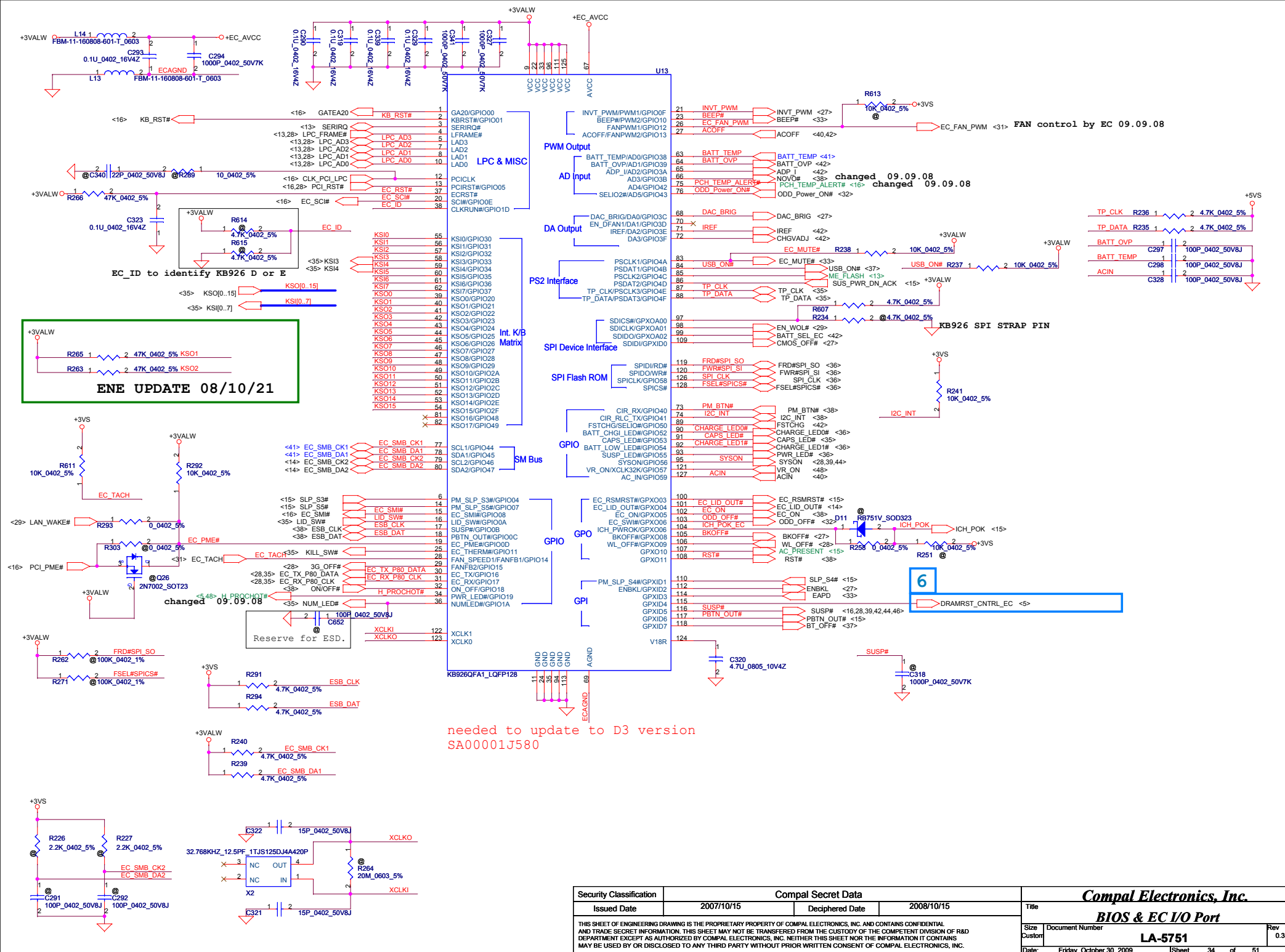


Security Classification	Compal Secret Data			Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	HDD/ODD Connector	
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				LA-5751	
				Date:	Friday, October 30, 2009
				Sheet	32 of 51

An integrated 5 V to 3.3 V Low-dropout voltage regulator (LDO).

An integrated 3.3 V to 1.8V Low-dropout voltage regulator (LDO).



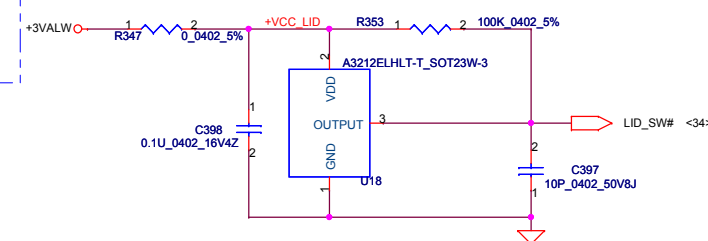


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						Size	Document Number				Rev
						Custom	LA-5751				0.3
Date:		Printed		October 30, 2009	Sheet	34 of 51					



CONN PIN define need double check

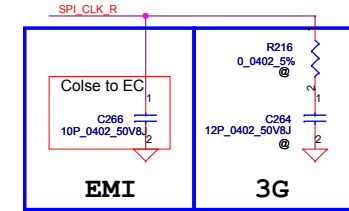
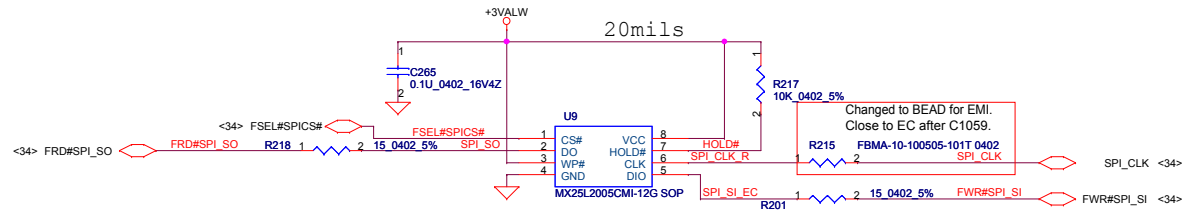
CONN PIN define need double check



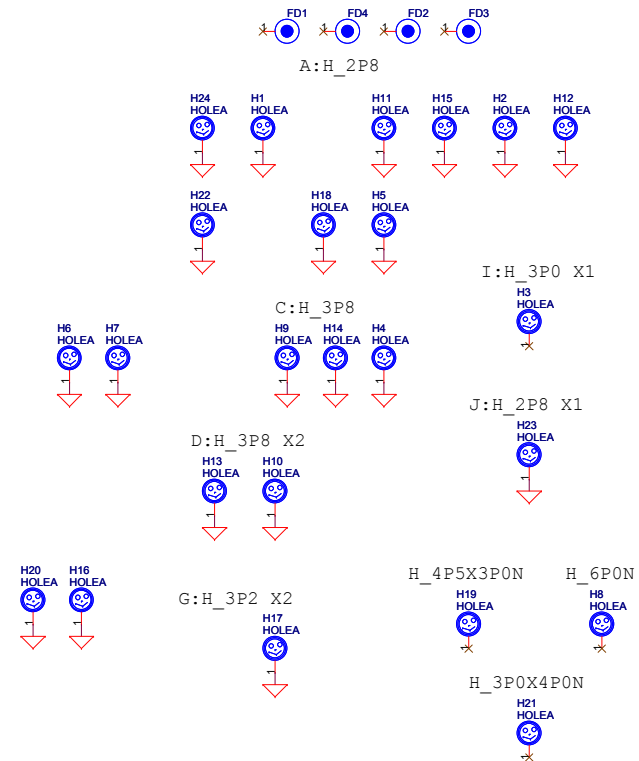
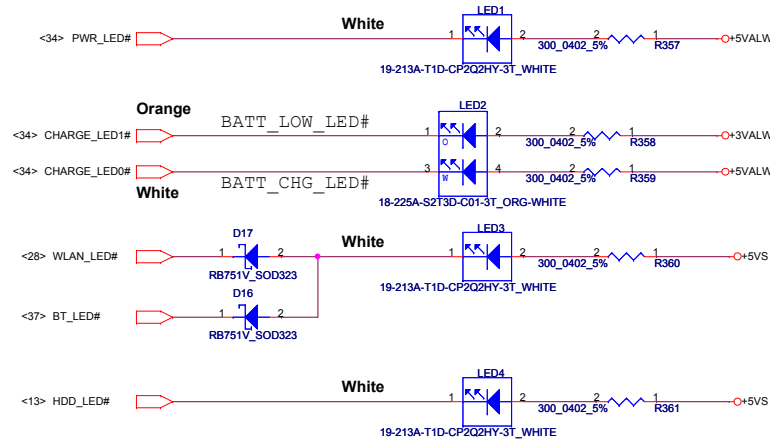
STATUS	
1, 2 (LOW)	OFF
2, 3 (HI)	ON

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title KB /SW /LPC Debug Conn.		
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				LA-5751		0.3
				Date: Friday, October 30, 2009		Sheet 35 of 51

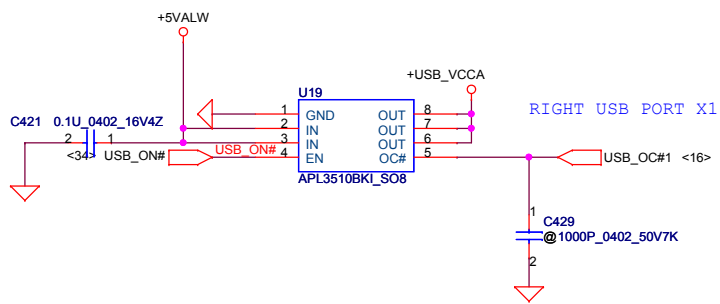
FOR EC 256KB SPI ROM (150mil PACKAGE)



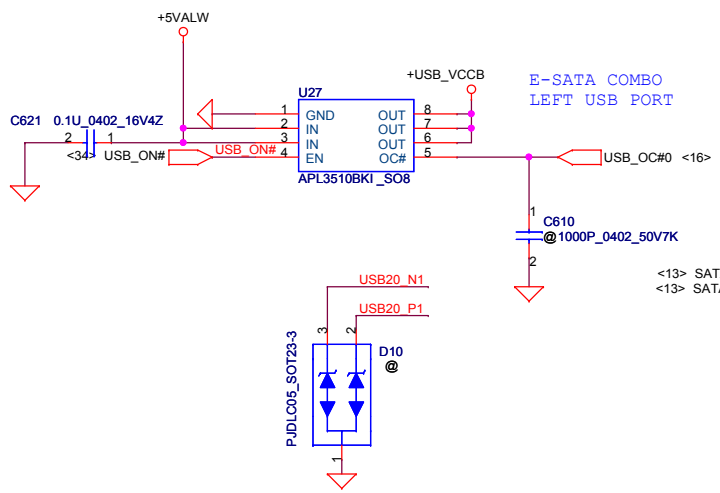
LED



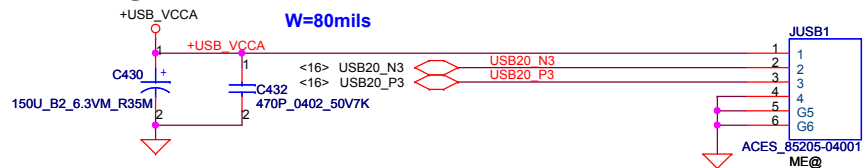
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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Size B	Document Number			LA-5751	Rev 0.3
Date:	Friday, October 30, 2009			Sheet	36 of 51



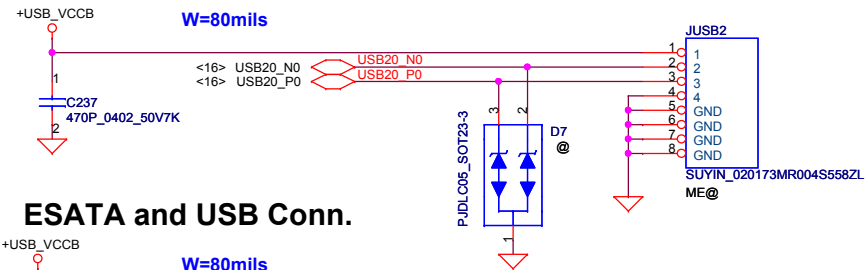
U19/U27 USB power switch need update symbol to SA000039E00 (Low enable)



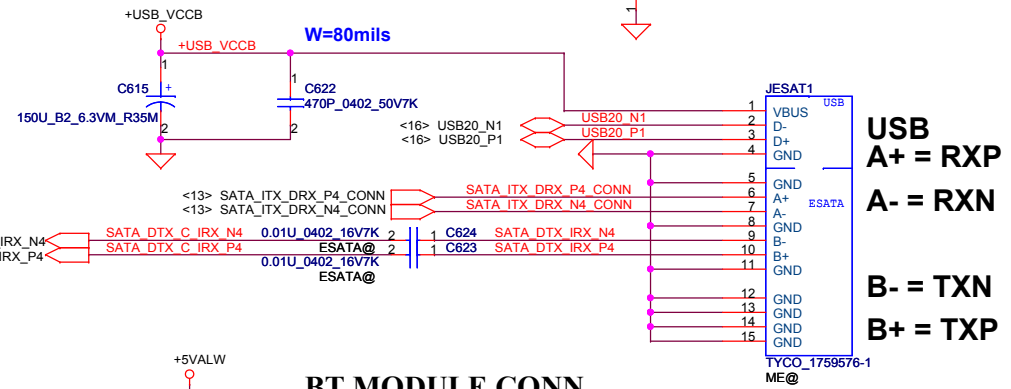
Right USB Conn.



Left USB Conn.

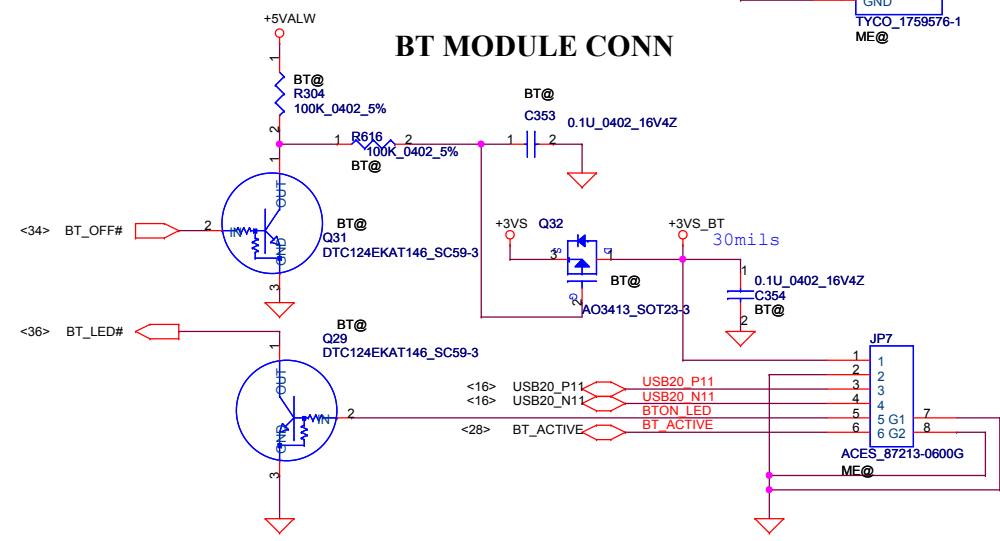


ESATA and USB Conn.



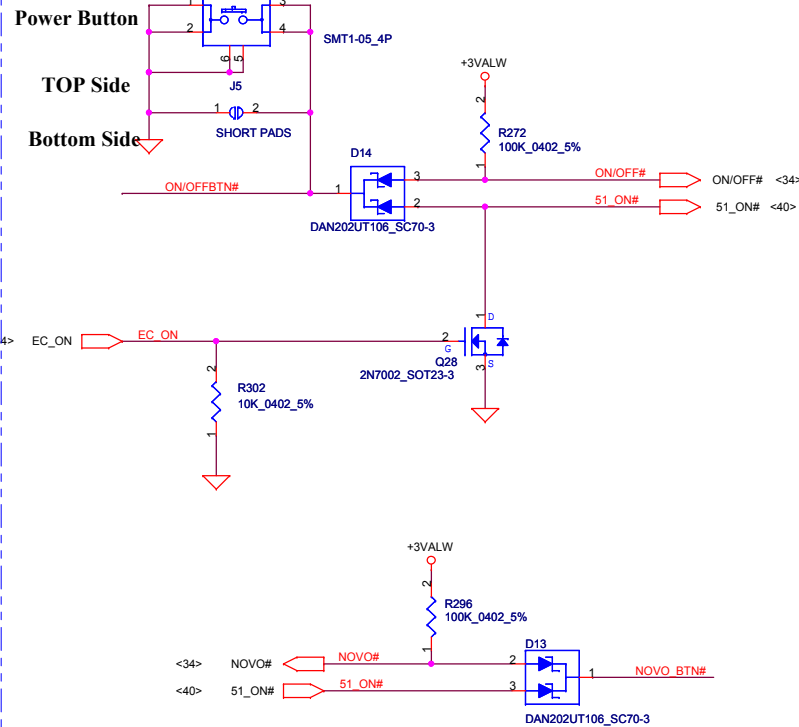
USB
A+ = RXP
A- = RXN
B- = TXN
B+ = TXP

BT MODULE CONN

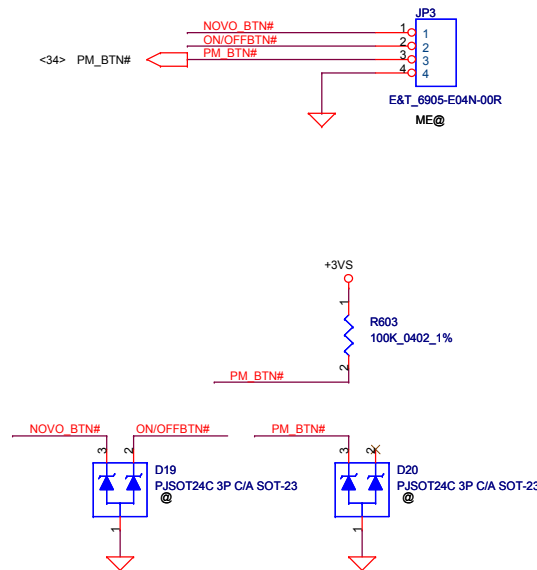


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				Custom	LA-5751
				Rev	0.3
				Date:	Thursday, October 29, 2009
				Sheet	37 of 51

ON/OFF switch

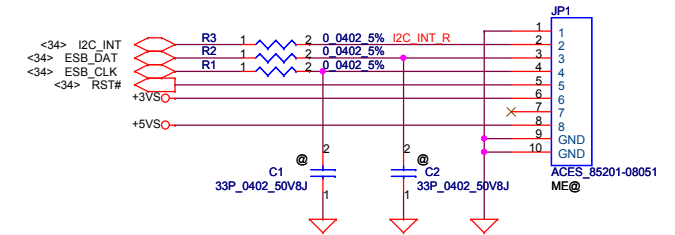


Power Bottom Board Conn. 4pin

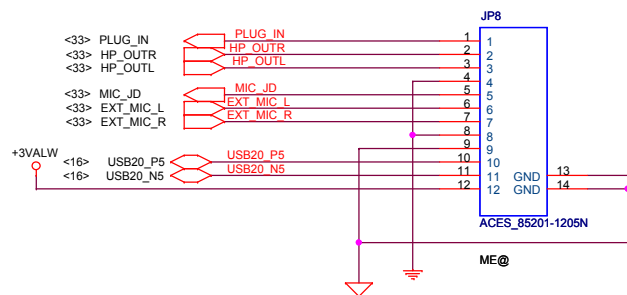


Cap Sensor Board Conn. 6pin

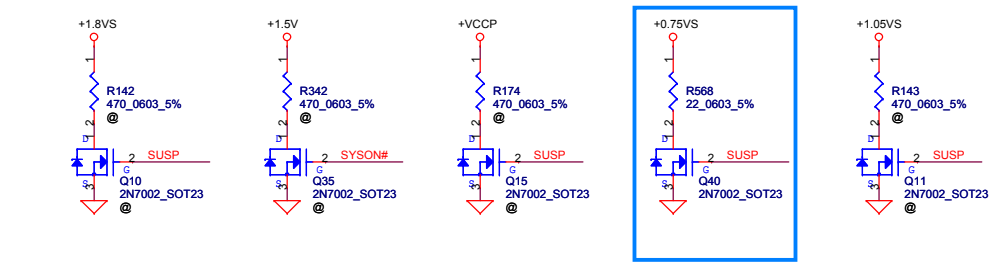
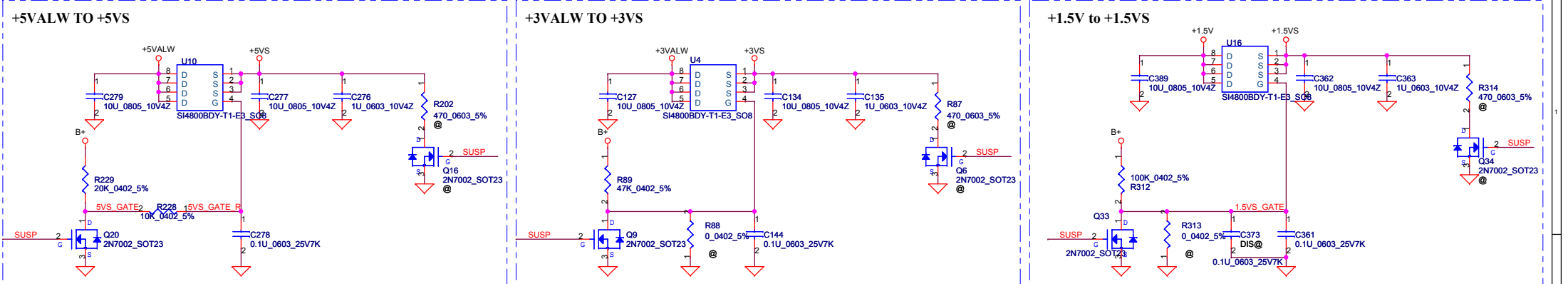
ENE SB3534



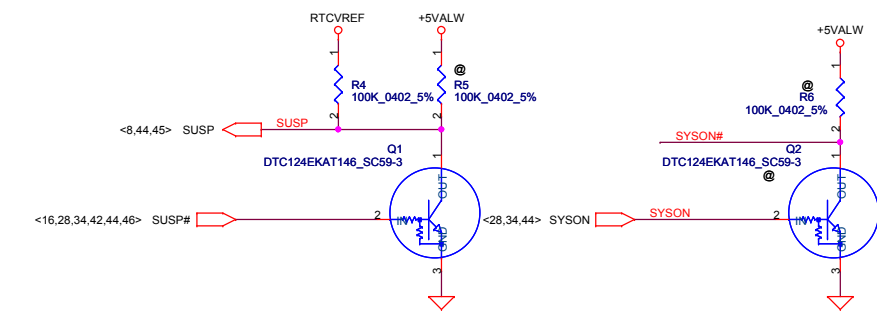
Card Reader/Audio Jack SB CONN



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Size Custom		Document Number		Rev 0.3
Date: Friday, October 30, 2009		Sheet 38 of 51		LA-5751

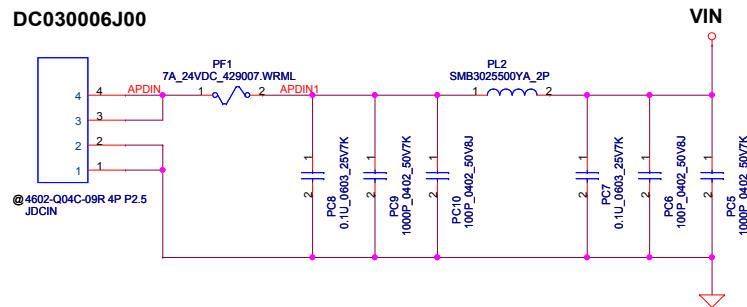


For Intel S3 Power Reduction.



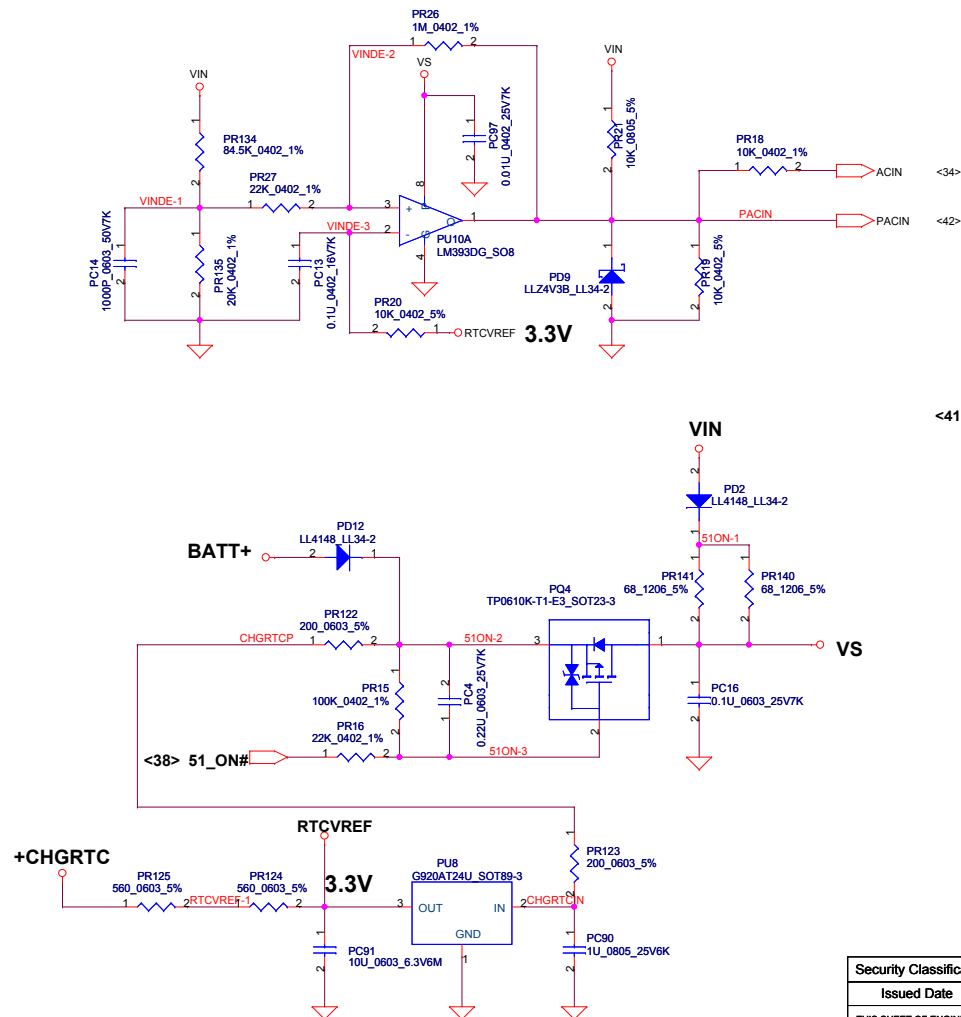
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2007/8/18		Title		DC Interface	
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		LA-5751		Rev	
Date		Thursday, October 29, 2009		Sheet	
		39		of	
		51			

DC030006J00



Vin Detector

	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V



ACIN

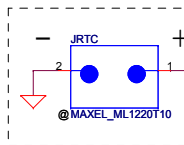
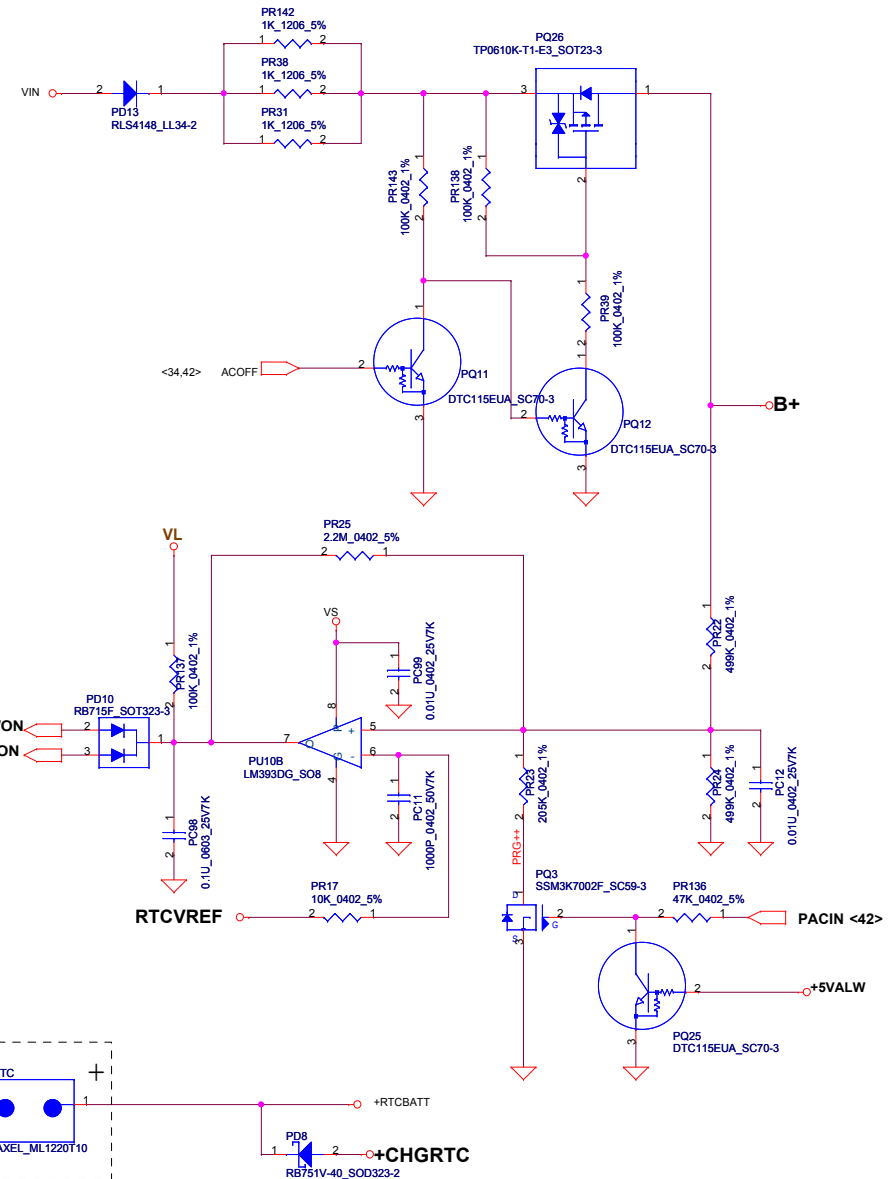
Precharge detector

	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector

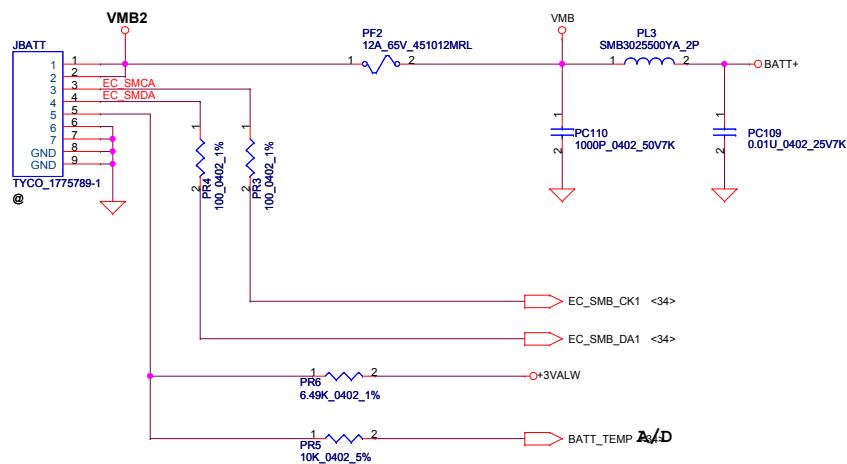
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V



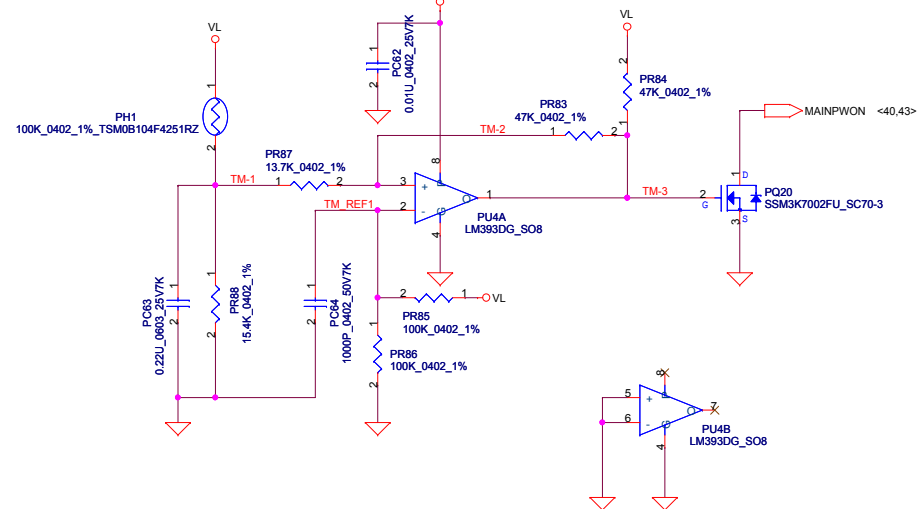
RTC Battery

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						Custom				0.1	
Date:						Friday, October 30, 2009		Sheet 40 of 51			

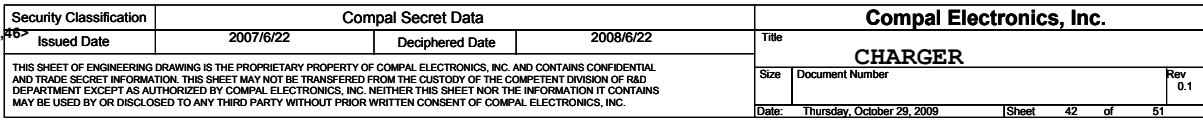
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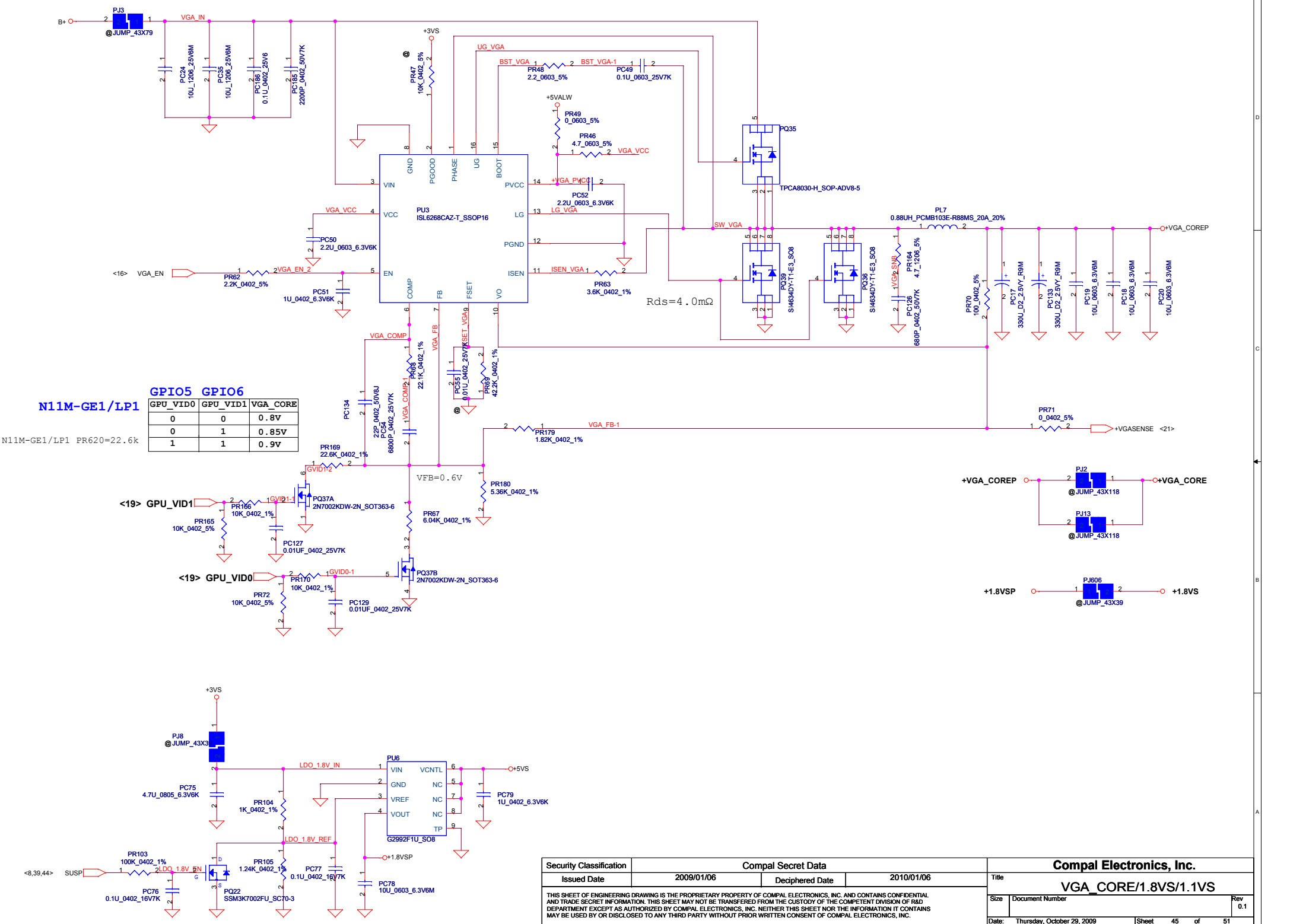


PH1 under CPU bottom side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



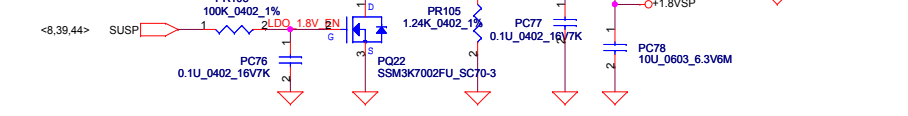
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Size	Document Number	Rev		0.1	
Date:	Thursday, October 29, 2009	Sheet	41	of	51



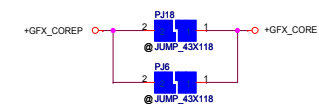


GPIO5 GPIO6			
GPU_VID0	GPU_VID1	VGA_CORE	
0	0	0.8V	
0	1	0.85V	
1	1	0.9V	

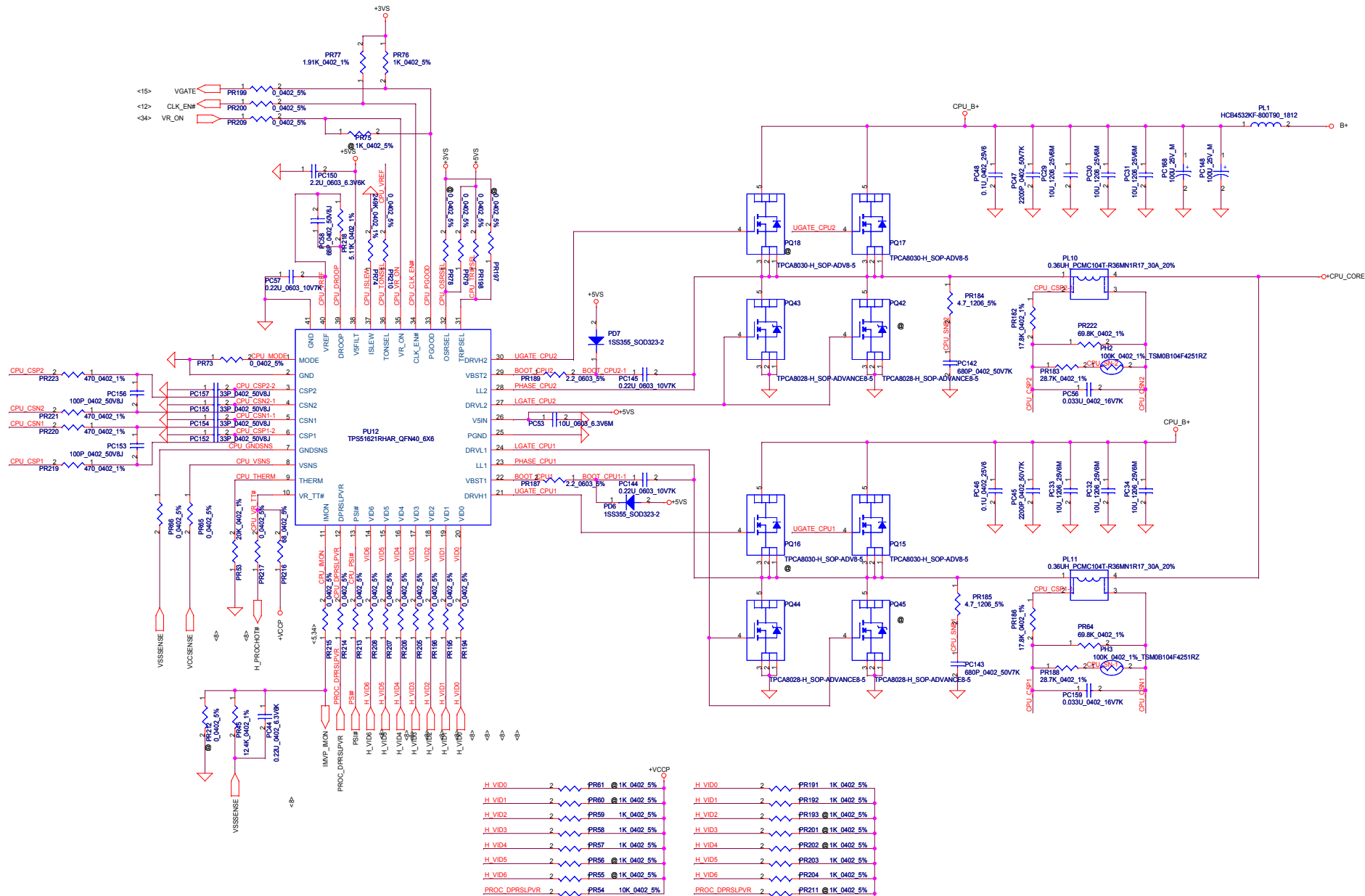
N11M-GE1/LP1 PR620=22.6k



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2009/01/06				2010/01/06				Title			
2010/01/06				2010/01/06				VGA_CORE/1.8VS/1.1VS			
Size				Document Number				Rev			
0.1				0.1				Date			
Thursday, October 29, 2009				Sheet				45 of 51			



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					Rev 0.1
Date:				Friday, October 30, 2009	Sheet 47 of 51



Clarkfield: VID(0-5):001101
 Auburndale: VID(0-5):001110

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Date: Thursday, October 26, 2009				Sheet 48 of 51

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17				20081022	

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE	EVT TO DVT
1		P15	Add C638~C645	For UMA HDMI	
2		P05	Add test point for BCLK_ITP, BCLK_ITP#, PRDY#	For XDP connector	
3		P32, P28	Change J6 size & unstuff ODD power control components Change J4 size	Disable ODD power control circuit	
4		P17	Stuff C262	For UMA CRT	
5		P34	Change R291, R294 from +3VALW to +3VS		
6		P38	Add R603 pull high to +3VS	For PM_BTN#	
7		P38	Change JP1 from 6 pin to 8 pin , Change JP8 from 14 pin to 12 pin , unstuff R322	For LED color changed Remove CLK_48M_CR	
8		P29, P34	Change EN_WOL to EN_WOL#	For identify clearly	
9		P34	EC pin26-> EC_FAN_PWM , pin75->PCH_TEMP_ALERT , pin34->PROCHOT# , pin66->NOVO#	EC GPIO arrangement	
10		P31	Change JP12 pin define	For EC FAN control	
11		P16	Change U5 pin3, pin5	POWER , GND reversed	
12		P15	Add U28 for ICH_POK & VGATE	Reserved	
13		P12	Unstuff R278, stuff R269 and change U14 to SA00003HQ00	For low power CLK GEN	
14		P13	Change U3 from 2MBytes to 4MBytes	For 4MBytes SPI ROM for PCH	
15		P29	Correct Q17 to P/N:SB000007600	For +3V_LAN power	
16		P16	Add C646 for BUF_PLT_RST#	Reserved for BUF_PLT_RST# overshoot problem	
17		P36	Change U9 from 2MBytes to 256KBytes	For 256KBytes SPI ROM for EC	
18		P03	UMA_HDMI@ , HDMI@ , BT@ , 3G@ , ESATA@ , CMOS@	New BOM structure	
19		P08	Add R608	For PSI# pull down	
20		P37	Delete D18		
21		P16	Unstuff R210, R212	Set Boot BIOS Strap to SPI	
22		P22	Change & stuff R475 to 30K, R51 to 15K Unstuff R474, R50	For N11M-GE1 QS sample	
23		P25	Unstuff R246	Level shift default setting	
24		P39	Change C373 to DIS@	for DIS power sequence	
25		P15, P16, P17	Change R436 from 1K to 10K Change C447 from 0.1u to 1u Delete R514 Unstuff C493, C494 Reserve R609	Check list Rev2.0 update	
27		P34	Add R607	Reserved for KB926 SPI STRAP PIN	
28		P36	Change LED1, LED3, LED4 to white color LED2 to orang\white color and orange connect to +3VALW		
29		P14	Change exp-card from PCIE port 1 to port 5	SW BIOS request	
30		P38	Unstuff SW1		
31		P13, P34	Change X1, X2 footprint		
32		P12	Change C348 to 22p, C349 to 22p	For Crystal matching	
33		P13, P20	Add C647~C650 12p, stuff C370->22p, R331->33	Reserved for RF team	
34		P36	Delete JP6	SPI ROM socket	
35		P37	Change C430, C615 footprint to B2 type		
36		P27, P32, P37	Change Q4, Q24, Q32, Q37 footprint to A03413		

Compal Electronics, Inc.		
Title		
HW PIR		
Size B	Document Number LA-5751	Rev 0.3
Date:	Thursday, October 29, 2009	Sheet 50 of 51

5		4		3		2		1	
NO DATE		PAGE		MODIFICATION LIST		PURPOSE		EVT TO DVT	
37		P34		Change C320 to 0805 type					
38		P08		Unstuff C268		For CPU VDDQ (DDR3 1.5V rails)			
				Change C252,C258 from 10u to 22u					
39		P34		Change ODD_power_on# from U13 pin28 to pin 76		EC GPIO arrangement			
				Add EC_TACH on U13 pin28 to JP12					
40		P31		Change U20 to EMC1403, add C651		Change thermal sensor solution to EMC1403			
41		P05		Add Q42,R610		Reserve for +0.75V enable option			
42		P34, P35		Add C652,C653,C654		Reserve for NUM_LED#,CAPS_LED# ESD request			
43		P34		Add R611,R612,R613		For EC_FAN_PWM, EC_TACH			
NO DATE		PAGE		MODIFICATION LIST		PURPOSE		DVT TO PVT	
1		P34		Reseve R614,R615.		EC_ID to identify KB926 D or E			
2		P34		Stuff R607		KB926 SPI STRAP PIN			
3		P33		Stuff C632~C635		EMI request			
4		P16		Stuff C646		For PLT_RST# singnal quality			
5		P37		Add R616 100K, change R304 to 100K, C353 to 0.1u		For +3VS_BT power on rising time			
6		P37		Changed R304 pin1 from +5VS to +5VALW		For +3VS_BT power on leakage			
7		P5		Stuff R283, C338 0.01u		For S3 power reduction			
8		P31		Add U29		Colay EMC2103/EMC1403 thermal sensor			
5		4		3		2		1	