

COMPAL CONFIDENTIAL

MODEL NAME : *HAL31(Discrete) & HAL30(UMA)*

PCB NO : *LA-3001P*

COMPAL P/N : *45140031L11 (For Discrete)*
45140031L01 (For UMA)



Bali (DIS&UMA) Schematics Document

uFCPGA Mobile Yonah
Intel Calistoga + ICH7M

2006-04-14

REV : 0.5 (DELL: X03)

@ : Nopop Component
1@ : UMA Used Only
2@ : Bali with discrete Used Only

MB PCB	
Part Number	Description
DA800004W0L	PCB LA-3001P REV0.4 MB

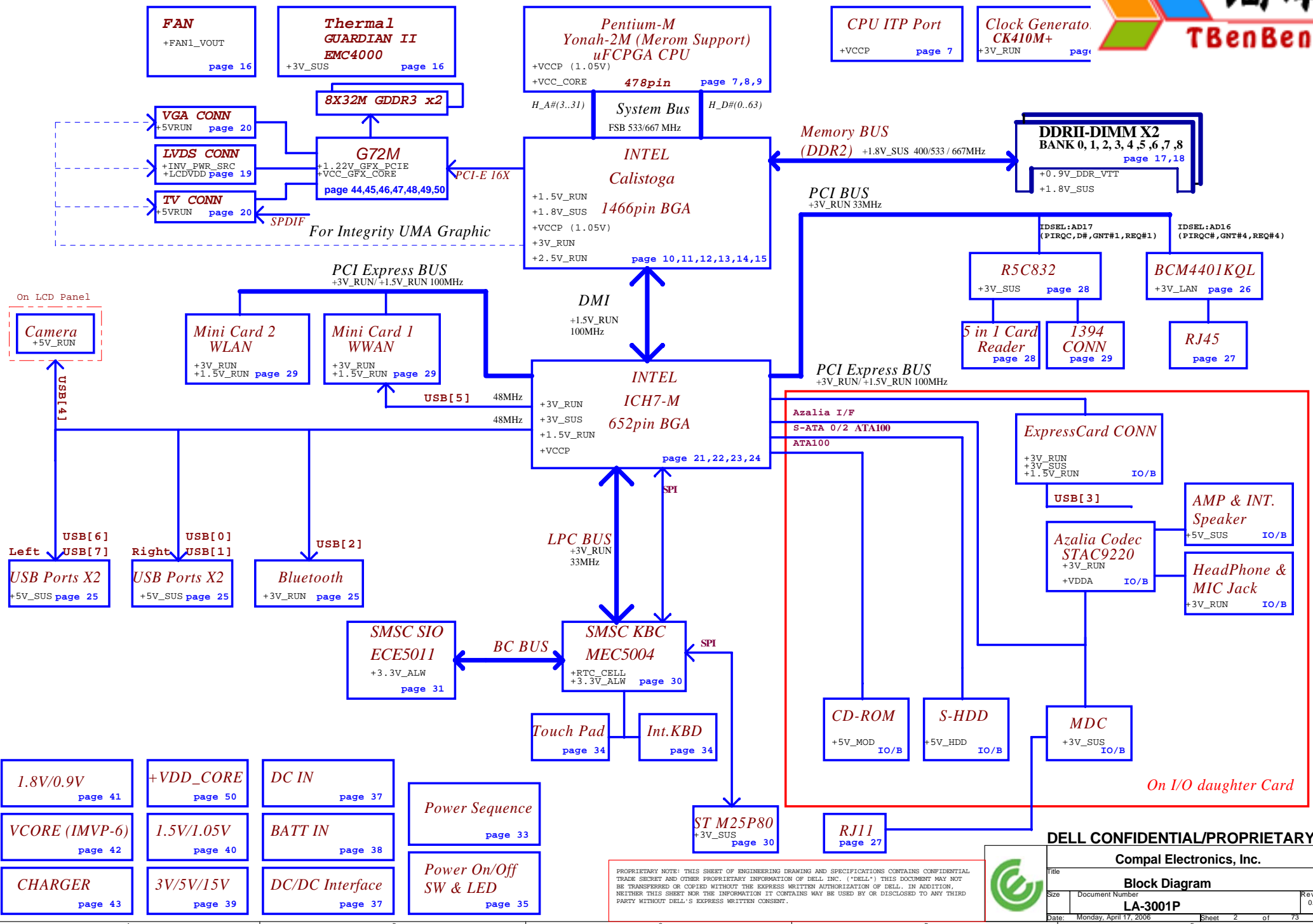
BOM NO: *45140031L11 (For Discrete)*
45140031L01 (For UMA)

PCB P/N: *DA800004W0L*

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Title	Cover Sheet	
Size	Document Number	Rev
	LA-3001P	0.4
Date: Monday, April 17, 2006	Sheet 1 of 73	



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Block Diagram			
Size	Document Number	Rev	
	LA-3001P	0.4	
Date:	Monday, April 17, 2006	Sheet	2 of 73

PM TABLE

power plane State	+5V_ALW +3.3V_ALW	+15V_SUS +5V_SUS +3.3V_SRC +3.3V_SUS +1.8V_SUS	+5V_RUN +3.3V_RUN +2.5V_RUN +1.8V_RUN +1.5V_RUN +1.22V_GFX_PCIE +0.9V_DDR_VTT +VCC_GFX_CORE +VCC_CORE +1.05V_VCCP
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
LAN	AD16	REQ#3/GNT#3	IRQB
R5C832	AD17	REQ#2/GNT#2	IRQC IRQD

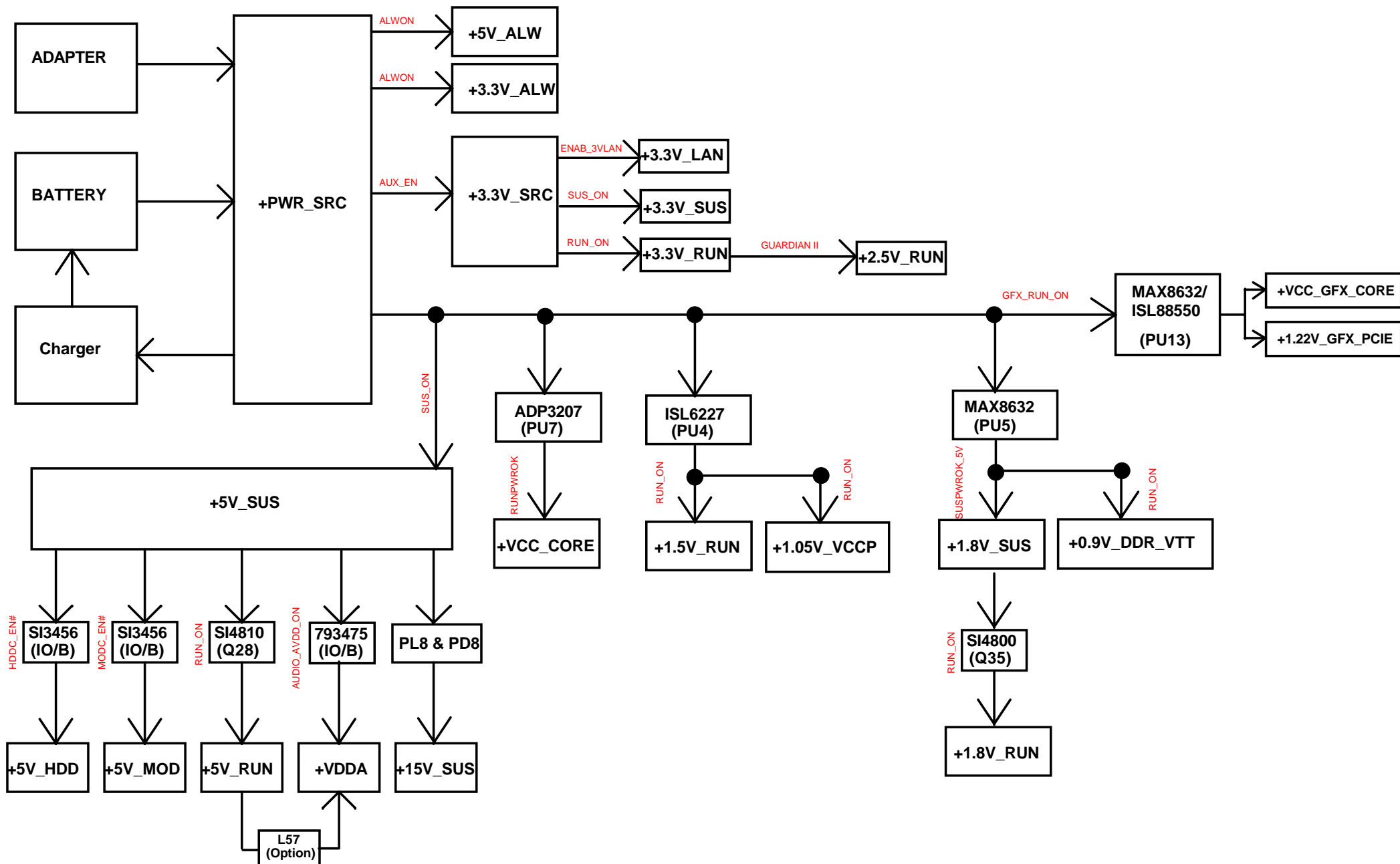
	USB PORT#	DE
ICH7-M	0	JUSB1 (Ext Left Side)
	1	JUSB1 (Ext Back Right Side)
	2	Blue Tooth
	3	EXPRESS CARD
	4	CCD Camera
	5	WWAN
	6	JUSB2 (Ext Back Left Side)
	7	JUSB2 (Ext Back Left Side)
SIO ECE5011	0	None
	1	None
	2	None
	3	None
	4	None

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	None
Lane 4	EXPRESS CARD

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Title	Index and Config.		
Size	Document Number	Rev	
	LA-3001P	0.4	
Date:	Monday, April 17, 2006	Sheet	3 of 73



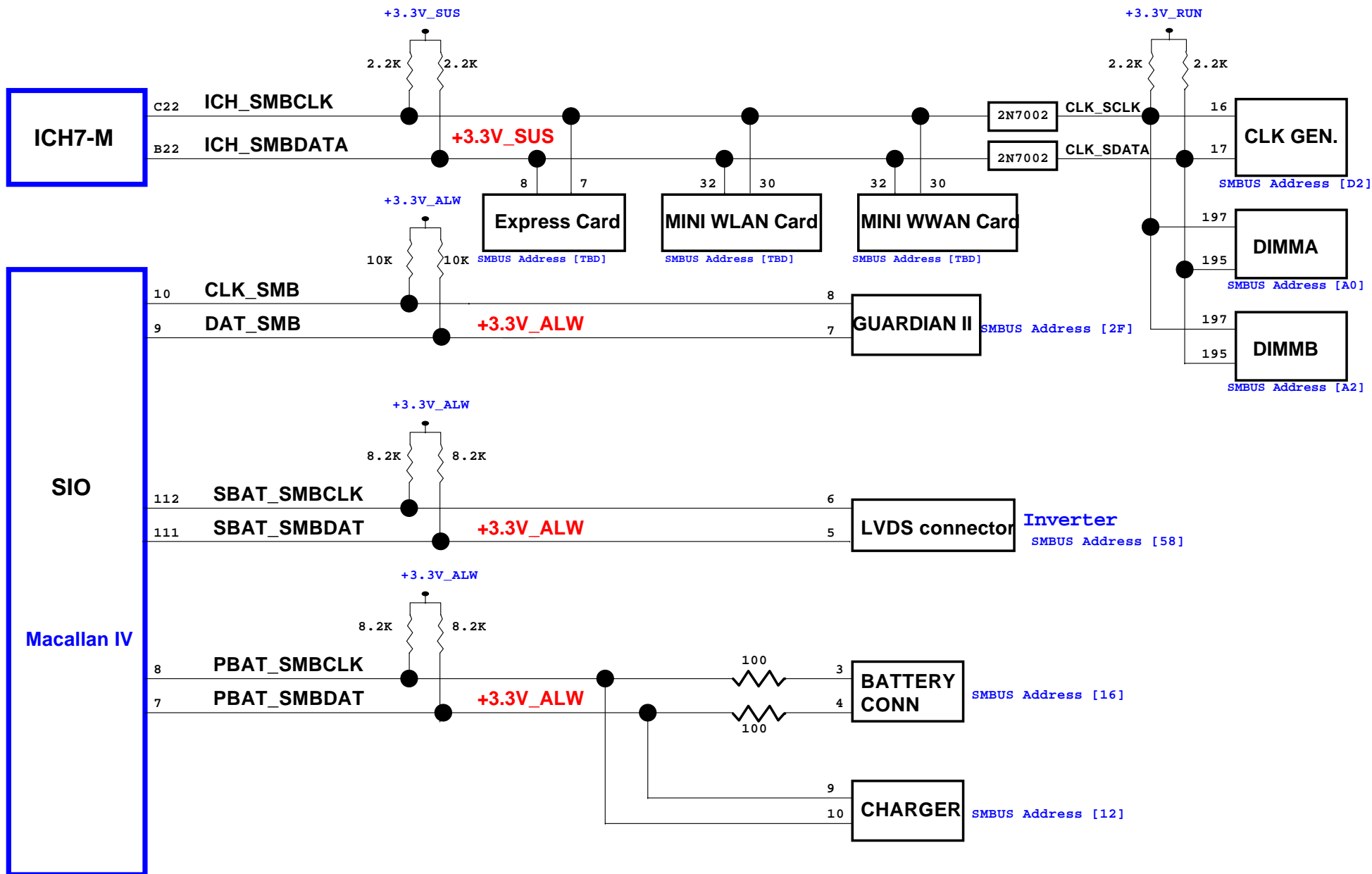
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Size	Document Number	Rev	
	LA-3001P	0.4	
Date:	Monday, April 17, 2006	Sheet	4 of 73



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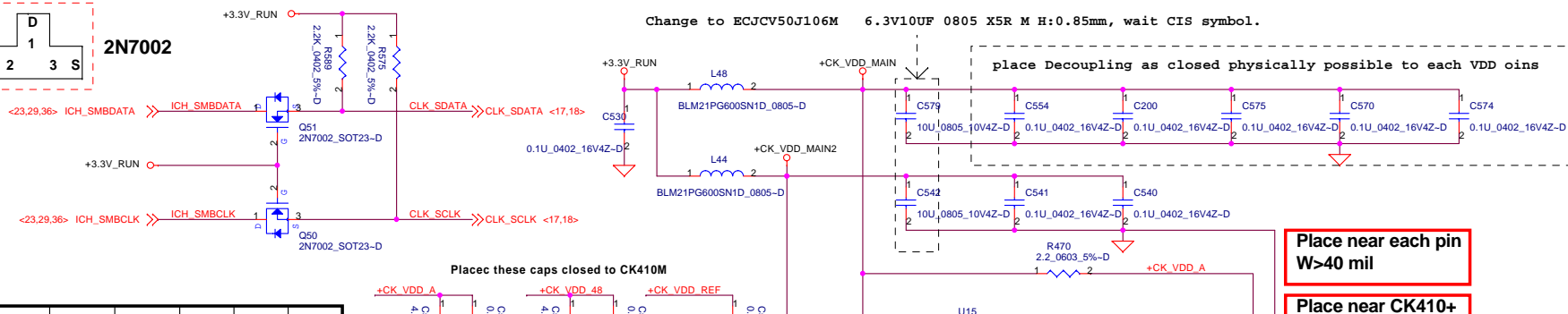


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Title		
SMBUS TOPOLOGY		
Size	Document Number	Rev
	LA-3001P	0.4
Date:	Monday, April 17, 2006	Sheet 5 of 73

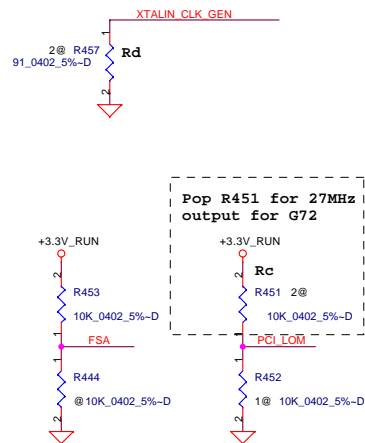
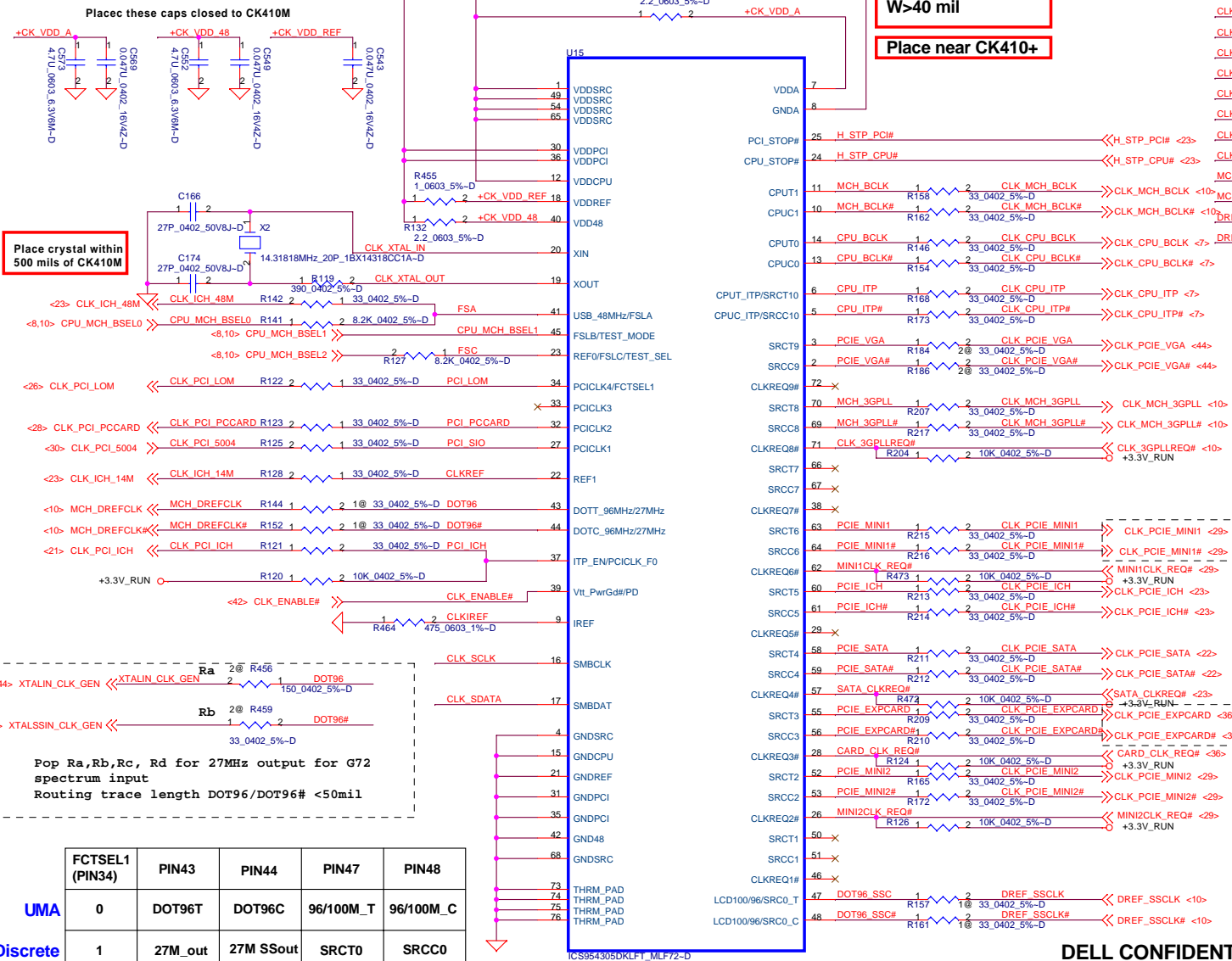
2N7002



	FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
*	0	0	0	266	100	33.3
	0	0	1	133	100	33.3
	0	1	0	200	100	33.3
	0	1	1	166	100	33.3
	1	0	0	333	100	33.3
	1	0	1	100	100	33.3
	1	1	0	400	100	33.3
	1	1	1	Reserve		

Table : ICS954305AK

CPU_BSEL	CPU_BSEL2 (FSC)	CPU_BSEL1 (FSB)
133	0	0
166	0	1



UMA

Discrete

FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0	DOT96T	DOT96C	96/100M_T	96/100M_C
1	27M_out	27M SSout	SRCT0	SRCC0

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Clock Generator

Size	Document Number LA-3001P	Rev 0.4
Date:	Monday, April 17, 2006	Sheet 6 of 73

<10> H_A# [3..31] <<<

JCPU1A

YONAH

>>> H_D# [0..63] <10>

H_A#3 J4 A3#
H_A#4 L4 A4#
H_A#5 M3 A5#
H_A#6 M3 A6#
H_A#7 M3 A7#
H_A#8 J1 A8#
H_A#9 J1 A9#
H_A#10 N3 A10#
H_A#11 P3 A11#
H_A#12 P3 A12#
H_A#13 L1 A13#
H_A#14 P1 A14#
H_A#15 P1 A15#
H_A#16 R1 A16#
H_A#17 Y2 A17#
H_A#18 U3 A18#
H_A#19 W3 A19#
H_A#20 W3 A20#
H_A#21 U4 A21#
H_A#22 Y3 A22#
H_A#23 U2 A23#
H_A#24 R4 A24#
H_A#25 T5 A25#
H_A#26 T3 A26#
H_A#27 W3 A27#
H_A#28 W3 A28#
H_A#29 Y4 A29#
H_A#30 W2 A30#
H_A#31 Y1 A31#

ADDR GROUP

DATA GROUP

<10> H_REQ#0 H_REQ#0 K3 REQ#0
<10> H_REQ#1 H_REQ#1 H2 REQ#1
<10> H_REQ#2 H_REQ#2 K2 REQ#2
<10> H_REQ#3 H_REQ#3 J2 REQ#3
<10> H_REQ#4 H_REQ#4 L3 REQ#4

<10> H_ADSTB#0 H_ADSTB#0 L2 ADSTB#0
<10> H_ADSTB#1 H_ADSTB#1 V4 ADSTB#1

HOST CLK

<6> CLK_CPU_BCLK CLK_CPU_BCLK A22 BCLK0
<6> CLK_CPU_BCLK# CLK_CPU_BCLK# A21 BCLK1

CONTROL

<10> H_ADS# H_ADS# H1 ADS#
<10> H_BNR# H_BNR# E2 BNR#
<10> H_BPR# H_BPR# F1 BPR#
<10> H_BR0# H_BR0# F1 BR0#
<10> H_DEFER# H_DEFER# H8 DEFER#
<10> H_DRDY# H_DRDY# F2 DRDY#
<10> H_HIT# H_HIT# G4 HIT#
<10> H_HITM# H_HITM# D20 HITM#
<10> H_LOCK# H_LOCK# H4 LOCK#
<10> H_RESET# H_RESET# B1 RESET#

<10> H_RS#0 H_RS#0 F3 RS0#
<10> H_RS#1 H_RS#1 F2 RS1#
<10> H_RS#2 H_RS#2 G2 RS2#
<10> H_TRDY# H_TRDY# G3 TRDY#

ITP_BPM#0 AD4 BPM#0
ITP_BPM#1 AD3 BPM#1
ITP_BPM#2 AD1 BPM#2
ITP_BPM#3 AC4 BPM#3

<23,30> ITP_DBRESET# C20 DBR#
<10> H_DBSY# H_DBSY# E1 DBSY#
<22> H_DPSLP# H_DPSLP# E5 DPSLP#
<22,42> H_DPRSTP# H_DPRSTP# D24 DPRSTP#
<10> H_DPWR# H_DPWR# AC2 PRDY#
<31> CPU_PROCHOT# CPU_PROCHOT# D21 PROCHOT#

DSTBN#0 H23 DSTBN#0
DSTBN#1 M24 DSTBN#1
DSTBN#2 W24 DSTBN#2
DSTBN#3 AD24 DSTBN#3
DSTBP#0 G22 DSTBP#0
DSTBP#1 N25 DSTBP#1
DSTBP#2 Y25 DSTBP#2
DSTBP#3 AE24 DSTBP#3

A20M# A6 H_A20M#
FERR# A5 H_FERR#
IGNNE# C4 H_IGNNE#
INIT# C2 H_INIT#
LINT0 C6 H_INTR#
LINT1 B4 H_NMI#

STPCLK# D5 H_STPCLK#
SMI# A3 H_SMI#

THERMAL

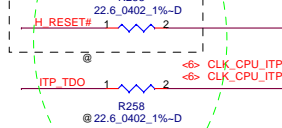
DIODE

<16> H_THERMDA H_THERMDA A24 THERMDA
<16> H_THERMDC H_THERMDC A25 THERMDC
<16> H_THERMTRIP# H_THERMTRIP# C7 THERMTRIP#

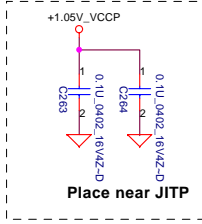
H_THERMDA, H_THERMDC routing together with guard trace,
Trace width / Spacing = 10 / 10 mil



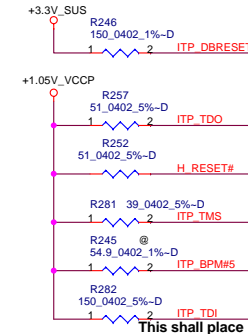
Notes: Can be nopop on X00 board.



No-stuff R253 & R258 for bits issue list: W152082



Place near J1TP



This shall place near CPU

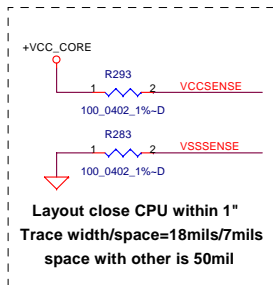
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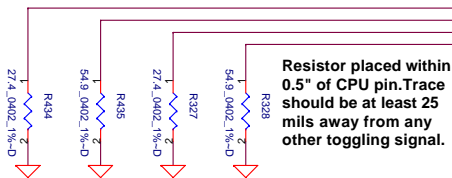


Yonah Processor(1/2)			
File	Document Number	Rev	
	LA-3001P	0.4	
Date	Monday, April 17, 2006	Sheet	7 of 73

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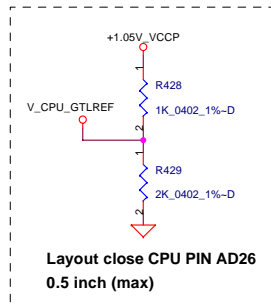


CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1



Layout Note:

COMP0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
COMP1,3 connect with Z0=55.5 ohm, make trace length shorter than 0.5".



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YONAH

POWER, GROUND, RESERVED SIGNALS AND NC

YONAH

POWER, GROUND

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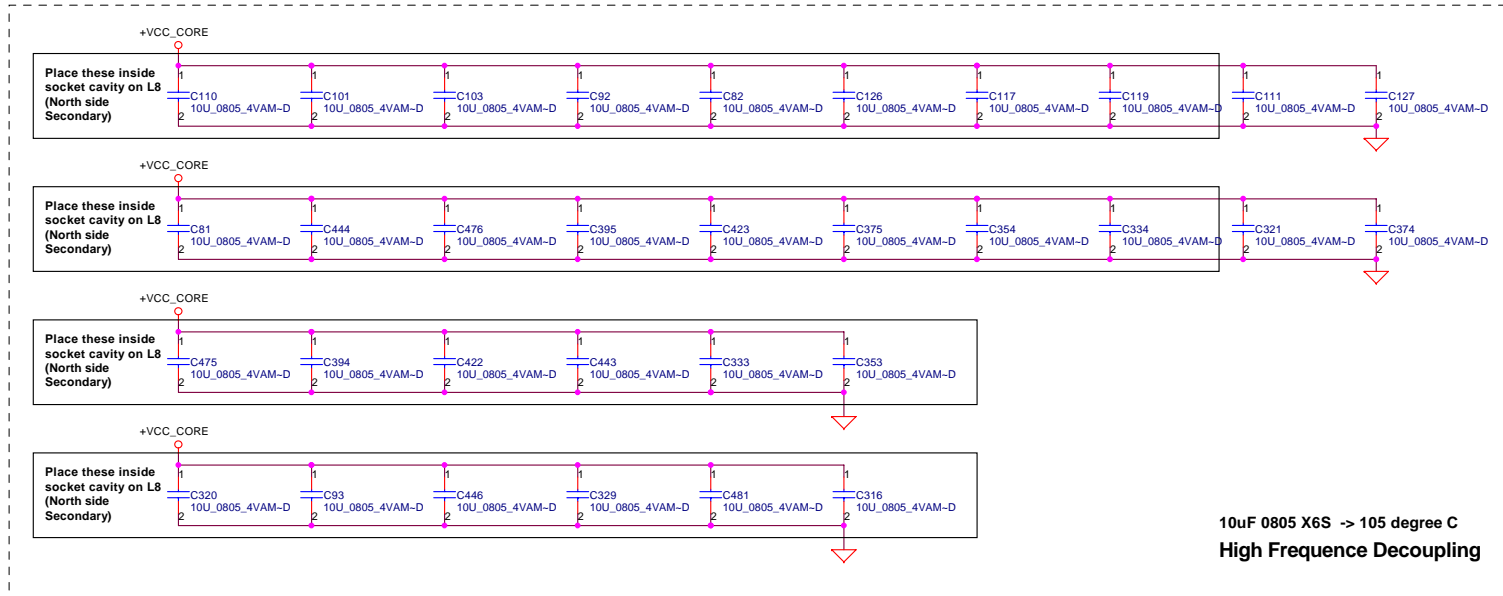
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Yonah Processor(2/2)

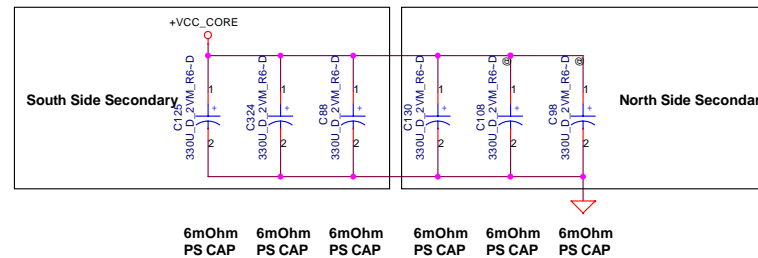


File	Document Number	Rev
LA-3001P		0.4
Date: Monday, April 17, 2006	Sheet 8 of 73	

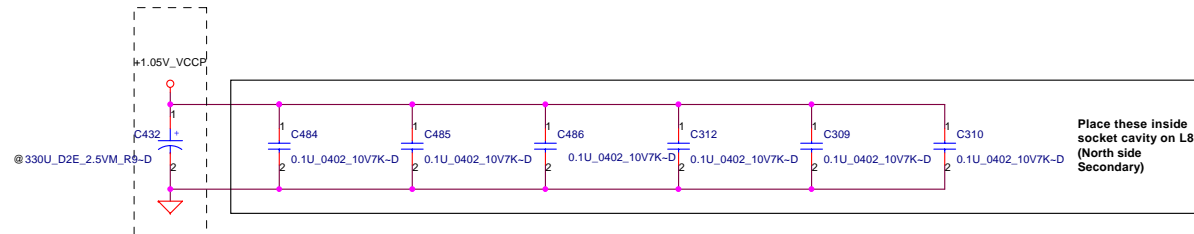
Intel CRB schematic suggest to use X5R or better



Near VCORE regulator



ESR <= 1.5m ohm
Capacitor > 1980uF



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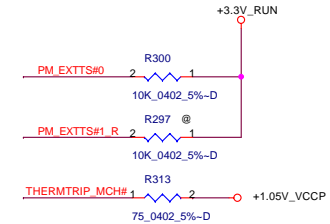
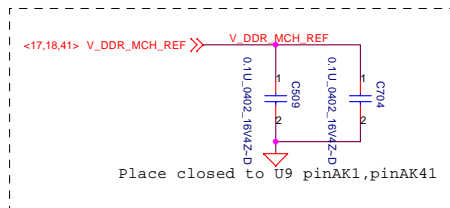
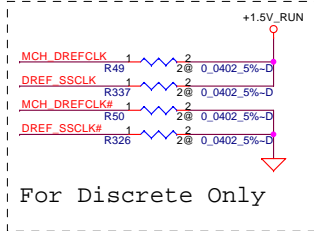
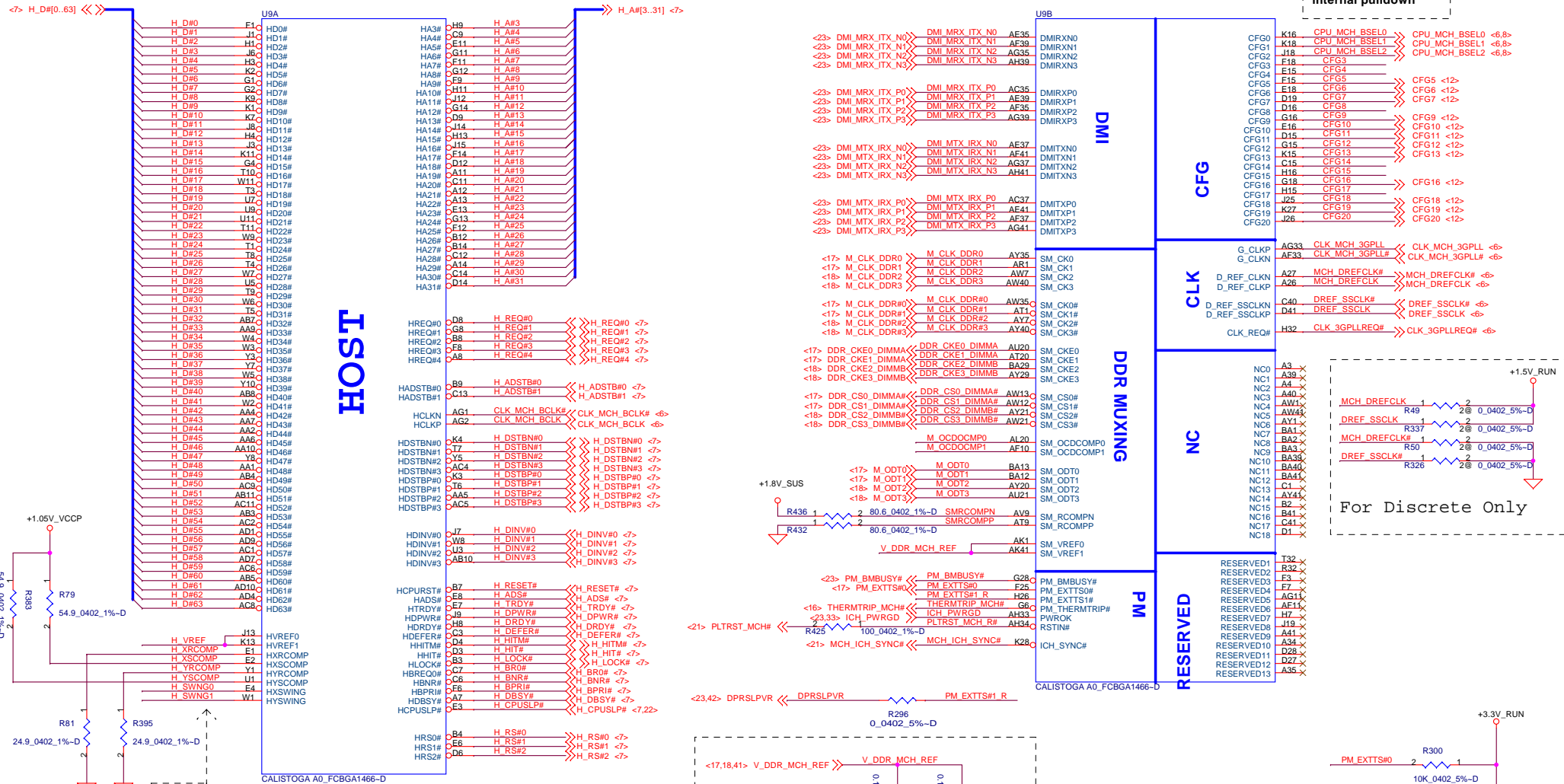


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Title			CPU Bypass
Size	Document Number	Rev	
	LA-3001P	0.4	
Date:	Monday, April 17, 2006	Sheet	9 of 73

Note :
CFG3:17 has
internal pullup,
CFG18:19 has
internal pulldown



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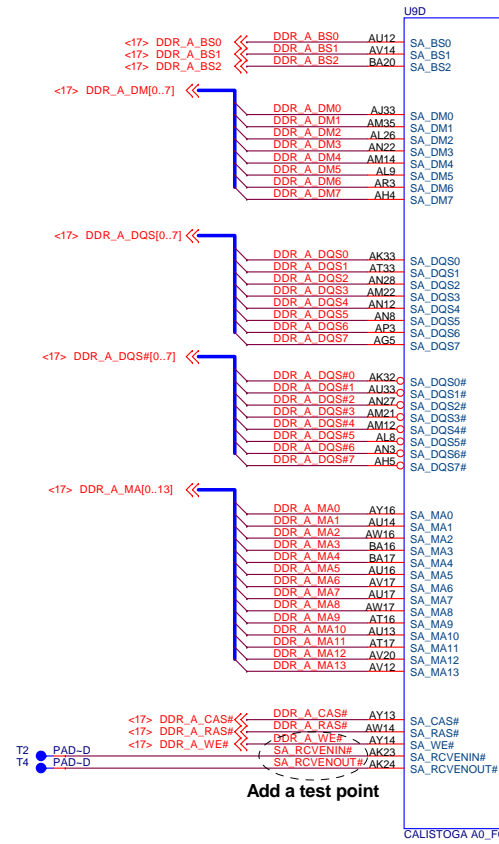
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Calistoga(1 of 6)

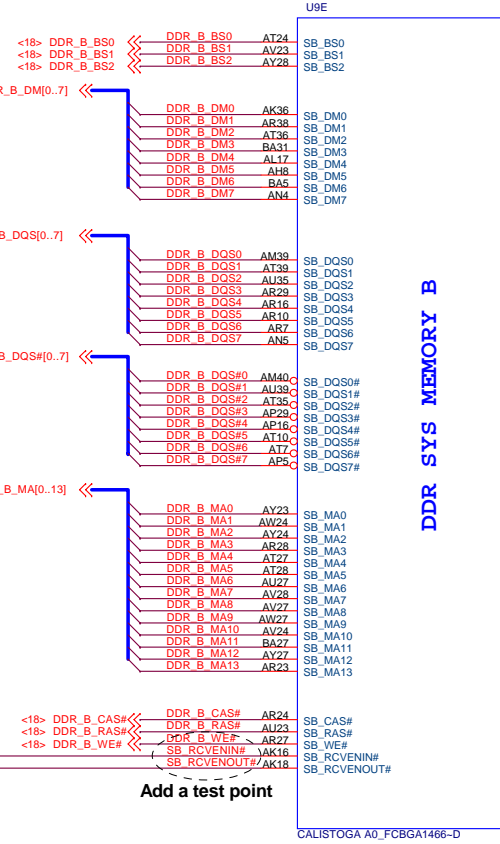
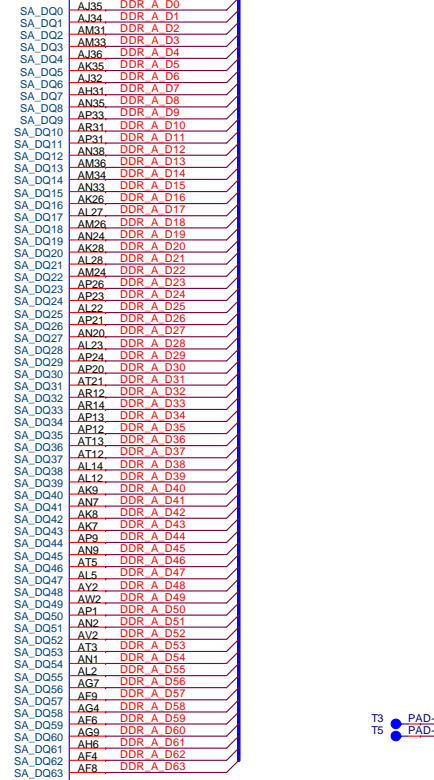


File	Document Number	Rev
LA-3001P	LA-3001P	0.4
Date: Monday, April 17, 2006	Sheet 10 of 73	

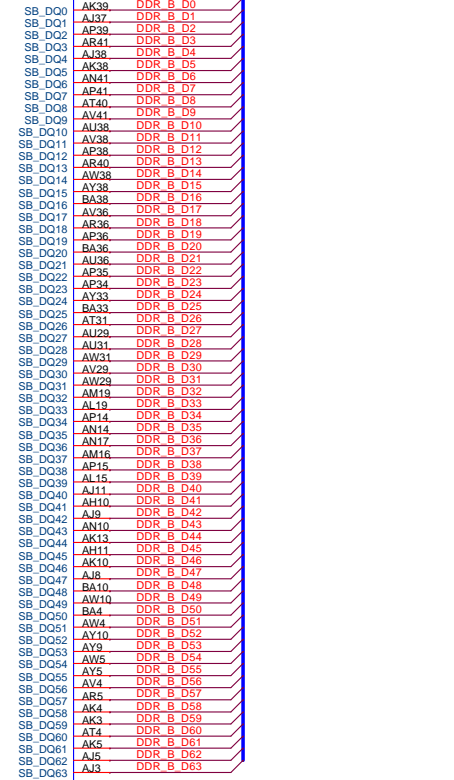
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DDR SYS MEMORY A



DDR SYS MEMORY B



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Calistogo(2 of 6)

Title	Document Number	Rev
LA-3001P	0.4	
Date: Monday, April 17, 2006	Sheet 11 of 73	

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SDVO_CTRLDATA have internal pull down

U9C

SDVOCTRL_DATA
SDVOCTRL_CLK

<19> LCD_A0+_NB
<19> LCD_A1+_NB
<19> LCD_A2+_NB
<19> LCD_A0-_NB
<19> LCD_A1-_NB
<19> LCD_A2-_NB

<19> LCD_A0+_NB
<19> LCD_A1+_NB
<19> LCD_A2+_NB
<19> LCD_A0-_NB
<19> LCD_A1-_NB
<19> LCD_A2-_NB

<19> LCD_A0+_NB
<19> LCD_A1+_NB
<19> LCD_A2+_NB
<19> LCD_A0-_NB
<19> LCD_A1-_NB
<19> LCD_A2-_NB

<19> LCD_A0+_NB
<19> LCD_A1+_NB
<19> LCD_A2+_NB
<19> LCD_A0-_NB
<19> LCD_A1-_NB
<19> LCD_A2-_NB

<19> LCD_A0+_NB
<19> LCD_A1+_NB
<19> LCD_A2+_NB
<19> LCD_A0-_NB
<19> LCD_A1-_NB
<19> LCD_A2-_NB

<19> LCD_A0+_NB
<19> LCD_A1+_NB
<19> LCD_A2+_NB
<19> LCD_A0-_NB
<19> LCD_A1-_NB
<19> LCD_A2-_NB

<19> LCD_A0+_NB
<19> LCD_A1+_NB
<19> LCD_A2+_NB
<19> LCD_A0-_NB
<19> LCD_A1-_NB
<19> LCD_A2-_NB

<19> LCD_A0+_NB
<19> LCD_A1+_NB
<19> LCD_A2+_NB
<19> LCD_A0-_NB
<19> LCD_A1-_NB
<19> LCD_A2-_NB

<19> LCD_A0+_NB
<19> LCD_A1+_NB
<19> LCD_A2+_NB
<19> LCD_A0-_NB
<19> LCD_A1-_NB
<19> LCD_A2-_NB

<19> LCD_A0+_NB
<19> LCD_A1+_NB
<19> LCD_A2+_NB
<19> LCD_A0-_NB
<19> LCD_A1-_NB
<19> LCD_A2-_NB

<19> LCD_A0+_NB
<19> LCD_A1+_NB
<19> LCD_A2+_NB
<19> LCD_A0-_NB
<19> LCD_A1-_NB
<19> LCD_A2-_NB

<19> LCD_A0+_NB
<19> LCD_A1+_NB
<19> LCD_A2+_NB
<19> LCD_A0-_NB
<19> LCD_A1-_NB
<19> LCD_A2-_NB

<19> LCD_A0+_NB
<19> LCD_A1+_NB
<19> LCD_A2+_NB
<19> LCD_A0-_NB
<19> LCD_A1-_NB
<19> LCD_A2-_NB

<19> LCD_A0+_NB
<19> LCD_A1+_NB
<19> LCD_A2+_NB
<19> LCD_A0-_NB
<19> LCD_A1-_NB
<19> LCD_A2-_NB

<19> LCD_A0+_NB
<19> LCD_A1+_NB
<19> LCD_A2+_NB
<19> LCD_A0-_NB
<19> LCD_A1-_NB
<19> LCD_A2-_NB

LVDS

TV

CRT

CRT_IREF

CALISTOGA A0_FCBGA1466-D

CRT_IREF

CRT_IREF

CRT_IREF

CRT_IREF

CRT_IREF

CRT_IREF

CRT_IREF

CRT_IREF

CRT_IREF

CRT_IREF

CRT_IREF

CRT_IREF

CRT_IREF

CRT_IREF

PCI-EXPRESS GRAPHICS

EXP_COMP1
EXP_COMP0
EXP_RXN0
EXP_RXN1
EXP_RXN2
EXP_RXN3
EXP_RXN4
EXP_RXN5
EXP_RXN6
EXP_RXN7
EXP_RXN8
EXP_RXN9
EXP_RXN10
EXP_RXN11
EXP_RXN12
EXP_RXN13
EXP_RXN14
EXP_RXN15

EXP_RXP0
EXP_RXP1
EXP_RXP2
EXP_RXP3
EXP_RXP4
EXP_RXP5
EXP_RXP6
EXP_RXP7
EXP_RXP8
EXP_RXP9
EXP_RXP10
EXP_RXP11
EXP_RXP12
EXP_RXP13
EXP_RXP14
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EXP_TXN0
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EXP_TXN4
EXP_TXN5
EXP_TXN6
EXP_TXN7
EXP_TXN8
EXP_TXN9
EXP_TXN10
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EXP_TXN15

EXP_TXP0
EXP_TXP1
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EXP_TXP7
EXP_TXP8
EXP_TXP9
EXP_TXP10
EXP_TXP11
EXP_TXP12
EXP_TXP13
EXP_TXP14
EXP_TXP15

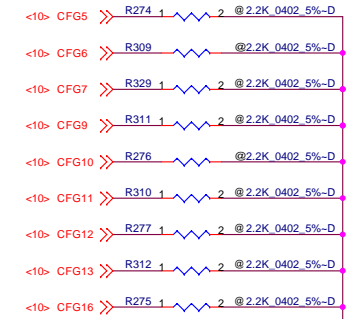
Stuff AC Caps For Discrete

PEG_MTX_GRPX_C_P0	C58	1	2	0.1U_0402_16V4Z-D 2@	PEG_MTX_GRPX_P0
PEG_MTX_GRPX_C_N0	C61	1	2	0.1U_0402_16V4Z-D	PEG_MTX_GRPX_N0
PEG_MTX_GRPX_C_P1	C63	1	2	0.1U_0402_16V4Z-D 2@	PEG_MTX_GRPX_P1
PEG_MTX_GRPX_C_N1	C65	1	2	0.1U_0402_16V4Z-D	PEG_MTX_GRPX_N1
PEG_MTX_GRPX_C_P2	C68	1	2	0.1U_0402_16V4Z-D 2@	PEG_MTX_GRPX_P2
PEG_MTX_GRPX_C_N2	C71	1	2	0.1U_0402_16V4Z-D	PEG_MTX_GRPX_N2
PEG_MTX_GRPX_C_P3	C74	1	2	0.1U_0402_16V4Z-D 2@	PEG_MTX_GRPX_P3
PEG_MTX_GRPX_C_N3	C79	1	2	0.1U_0402_16V4Z-D	PEG_MTX_GRPX_N3
PEG_MTX_GRPX_C_P4	C80	1	2	0.1U_0402_16V4Z-D 2@	PEG_MTX_GRPX_P4
PEG_MTX_GRPX_C_N4	C84	1	2	0.1U_0402_16V4Z-D	PEG_MTX_GRPX_N4
PEG_MTX_GRPX_C_P5	C87	1	2	0.1U_0402_16V4Z-D 2@	PEG_MTX_GRPX_P5
PEG_MTX_GRPX_C_N5	C90	1	2	0.1U_0402_16V4Z-D	PEG_MTX_GRPX_N5
PEG_MTX_GRPX_C_P6	C91	1	2	0.1U_0402_16V4Z-D 2@	PEG_MTX_GRPX_P6
PEG_MTX_GRPX_C_N6	C94	1	2	0.1U_0402_16V4Z-D	PEG_MTX_GRPX_N6
PEG_MTX_GRPX_C_P7	C96	1	2	0.1U_0402_16V4Z-D 2@	PEG_MTX_GRPX_P7
PEG_MTX_GRPX_C_N7	C105	1	2	0.1U_0402_16V4Z-D	PEG_MTX_GRPX_N7
PEG_MTX_GRPX_C_P8	C106	1	2	0.1U_0402_16V4Z-D 2@	PEG_MTX_GRPX_P8
PEG_MTX_GRPX_C_N8	C107	1	2	0.1U_0402_16V4Z-D	PEG_MTX_GRPX_N8
PEG_MTX_GRPX_C_P9	C109	1	2	0.1U_0402_16V4Z-D 2@	PEG_MTX_GRPX_P9
PEG_MTX_GRPX_C_N9	C113	1	2	0.1U_0402_16V4Z-D	PEG_MTX_GRPX_N9
PEG_MTX_GRPX_C_P10	C112	1	2	0.1U_0402_16V4Z-D 2@	PEG_MTX_GRPX_P10
PEG_MTX_GRPX_C_N10	C116	1	2	0.1U_0402_16V4Z-D	PEG_MTX_GRPX_N10
PEG_MTX_GRPX_C_P11	C120	1	2	0.1U_0402_16V4Z-D 2@	PEG_MTX_GRPX_P11
PEG_MTX_GRPX_C_N11	C124	1	2	0.1U_0402_16V4Z-D	PEG_MTX_GRPX_N11
PEG_MTX_GRPX_C_P12	C123	1	2	0.1U_0402_16V4Z-D 2@	PEG_MTX_GRPX_P12
PEG_MTX_GRPX_C_N12	C129	1	2	0.1U_0402_16V4Z-D	PEG_MTX_GRPX_N12
PEG_MTX_GRPX_C_P13	C134	1	2	0.1U_0402_16V4Z-D 2@	PEG_MTX_GRPX_P13
PEG_MTX_GRPX_C_N13	C137	1	2	0.1U_0402_16V4Z-D	PEG_MTX_GRPX_N13
PEG_MTX_GRPX_C_P14	C136	1	2	0.1U_0402_16V4Z-D 2@	PEG_MTX_GRPX_P14
PEG_MTX_GRPX_C_N14	C140	1	2	0.1U_0402_16V4Z-D	PEG_MTX_GRPX_N14
PEG_MTX_GRPX_C_P15	C142	1	2	0.1U_0402_16V4Z-D 2@	PEG_MTX_GRPX_P15
PEG_MTX_GRPX_C_N15	C147	1	2	0.1U_0402_16V4Z-D	PEG_MTX_GRPX_N15

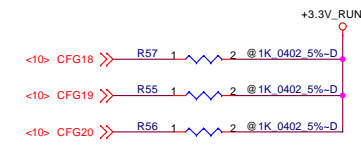
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Strap Pin Table

CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = Moby Dick High = Calistoga *
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG10	Low = Reserved High = Mobility *
CFG11	Low = Calistoga * High = Reserved
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (DMI Lane Reversal)	Low = Normal Operation (Default): * Lane number in Order High = Reverse Lane
SDVO_CTRLDATA	Low = No SDVO Device Present (Default) * High = SDVO Device Present
CFG20 (PCIE/SDVO select)	Low = Only PCIE or SDVO is operational. (Default) * High = PCIE/SDVO are operating simu.



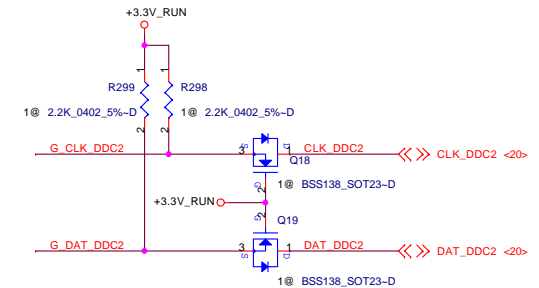
CFG[3:17] have internal pullup



CFG[18:19] have internal pulldown

Resistors Stuff Table

UMA	R290,R305,R307,R308,R360 R366,R301,R302,R303,R294 R295,R292,R306,R304,R38 R39,298,R299,
Discrete	R271,R272,R273,R270,R53, R358,R345,R266,R267,R268, R371,R269

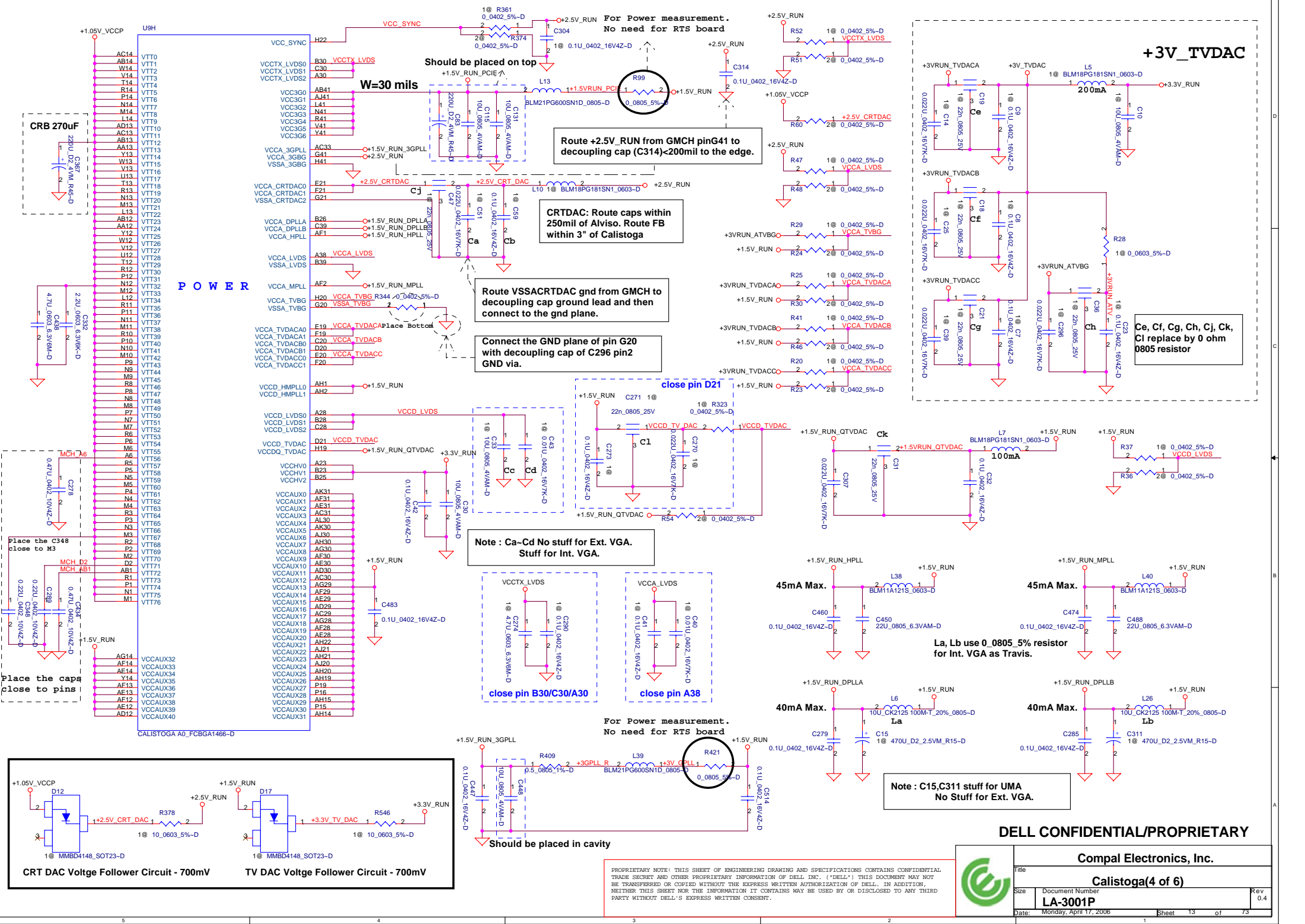


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Calistoga(3 of 6)

File	Document Number	Rev
LA-3001P		0.4
Date: Monday, April 17, 2006	Sheet 12 of 73	



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U9I		
AC41	VSS0	VSS100
AA41	VSS1	AC34
W41	VSS2	C34
T41	VSS3	AW33
P41	VSS4	AV33
M41	VSS5	AR33
J41	VSS6	AE33
F41	VSS7	AB33
AV40	VSS8	Y33
AP40	VSS9	V33
AN40	VSS10	T33
AK40	VSS11	R33
A40	VSS12	M33
AH40	VSS13	H33
AG40	VSS14	G33
AF40	VSS15	J21
AE40	VSS16	D33
B40	VSS17	B33
AY39	VSS18	AH32
AW39	VSS19	AG32
AV39	VSS20	AR20
AP39	VSS21	AM20
AN39	VSS22	AA20
AJ39	VSS23	K20
AC39	VSS24	B20
AB39	VSS25	A20
AA39	VSS26	AN19
Y39	VSS27	R32
W39	VSS28	AC19
V39	VSS29	AY31
T39	VSS30	AV31
R39	VSS31	AN31
P39	VSS32	AJ31
N39	VSS33	AG31
M39	VSS34	AB31
L39	VSS35	Y31
J39	VSS36	D18
H39	VSS37	A18
G39	VSS38	AY17
F39	VSS39	AR17
D39	VSS40	AP17
AT38	VSS41	AM17
AM38	VSS42	AK17
AH38	VSS43	AV16
AG38	VSS44	AN16
AF38	VSS45	C29
AE38	VSS46	F29
C38	VSS47	A29
AK37	VSS48	VSS145
AH37	VSS49	BA28
AB37	VSS50	AM15
AA37	VSS51	AW28
Y37	VSS52	AL15
W37	VSS53	AK15
V37	VSS54	N15
T37	VSS55	M15
R37	VSS56	L15
P37	VSS57	B15
N37	VSS58	W28
M37	VSS59	J28
L37	VSS60	E28
J37	VSS61	AT14
H37	VSS62	AP27
G37	VSS63	AM27
F37	VSS64	AK27
D37	VSS65	I27
AY36	VSS66	G27
AW36	VSS67	F27
AN36	VSS68	C27
AH36	VSS69	AV13
AG36	VSS70	AR13
AF36	VSS71	M26
AE36	VSS72	K26
AC36	VSS73	F26
C36	VSS74	AL13
B36	VSS75	D26
BA35	VSS76	AK25
AV35	VSS77	P25
AR35	VSS78	H25
AK35	VSS79	E25
AB35	VSS80	D25
AA35	VSS81	A25
Y35	VSS82	BA24
W35	VSS83	AU24
V35	VSS84	AL24
T35	VSS85	AW23
R35	VSS86	AT23
P35	VSS87	AN23
N35	VSS88	AM23
M35	VSS89	AH23
L35	VSS90	AC23
J35	VSS91	W23
H35	VSS92	K23
G35	VSS93	J23
F35	VSS94	F23
D35	VSS95	C23
AK34	VSS96	AA22
AG34	VSS97	K22
AF34	VSS98	G22
	VSS99	F22
		E22
		D22
		A22
		BA21
		AV21
		AR21

POWER

U9J		
AN21	VSS200	VSS280
AL21	VSS201	AG10
AB21	VSS202	AC10
Y21	VSS203	W10
M21	VSS204	U10
J21	VSS205	BA9
H21	VSS206	AW9
C21	VSS207	AR9
AW20	VSS208	AH9
AR20	VSS209	AB9
AM20	VSS210	Y9
AA20	VSS211	R9
K20	VSS212	E9
B20	VSS213	G9
A20	VSS214	A9
AN19	VSS215	VSS292
R32	VSS216	VSS291
AC19	VSS217	VSS290
AY31	VSS218	VSS289
AV31	VSS219	VSS288
AN31	VSS220	VSS287
AJ31	VSS221	VSS286
AG31	VSS222	VSS285
AB31	VSS223	VSS284
Y31	VSS224	VSS283
D18	VSS225	VSS282
A18	VSS226	VSS281
AY17	VSS227	VSS280
AR17	VSS228	VSS279
AP17	VSS229	VSS278
AM17	VSS230	VSS277
AK17	VSS231	VSS276
AV16	VSS232	VSS275
AN16	VSS233	VSS274
C29	VSS234	VSS273
F29	VSS235	VSS272
A29	VSS236	VSS271
VSS145	VSS237	VSS270
BA28	VSS238	VSS269
AM15	VSS239	VSS268
AW28	VSS240	VSS267
AL15	VSS241	VSS266
AK15	VSS242	VSS265
N15	VSS243	VSS264
M15	VSS244	VSS263
L15	VSS245	VSS262
B15	VSS246	VSS261
W28	VSS247	VSS260
J28	VSS248	VSS259
E28	VSS249	VSS258
AT14	VSS250	VSS257
AP27	VSS251	VSS256
AM27	VSS252	VSS255
AK27	VSS253	VSS254
I27	VSS254	VSS253
G27	VSS255	VSS252
F27	VSS256	VSS251
C27	VSS257	VSS250
AV13	VSS258	VSS249
AR13	VSS259	VSS248
M26	VSS260	VSS247
K26	VSS261	VSS246
F26	VSS262	VSS245
AL13	VSS263	VSS244
D26	VSS264	VSS243
AK25	VSS265	VSS242
P25	VSS266	VSS241
H25	VSS267	VSS240
E25	VSS268	VSS239
D25	VSS269	VSS238
A25	VSS270	VSS237
BA24	VSS271	VSS236
AU24	VSS272	VSS235
AL24	VSS273	VSS234
AW23	VSS274	VSS233
AT23	VSS275	VSS232
AN23	VSS276	VSS231
AM23	VSS277	VSS230
AH23	VSS278	VSS229
AC23	VSS279	VSS228
W23	VSS280	VSS227
K23	VSS281	VSS226
J23	VSS282	VSS225
F23	VSS283	VSS224
C23	VSS284	VSS223
AA22	VSS285	VSS222
K22	VSS286	VSS221
G22	VSS287	VSS220
F22	VSS288	VSS219
E22	VSS289	VSS218
D22	VSS290	VSS217
A22	VSS291	VSS216
BA21	VSS292	VSS215
AV21	VSS293	VSS214
AR21	VSS294	VSS213

POWER

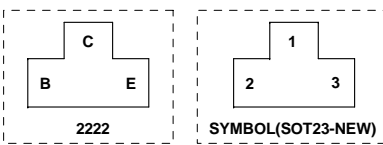
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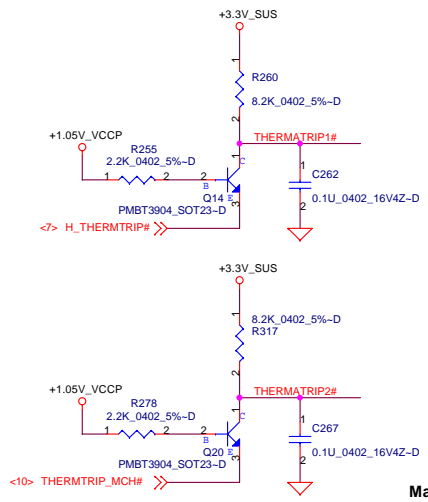
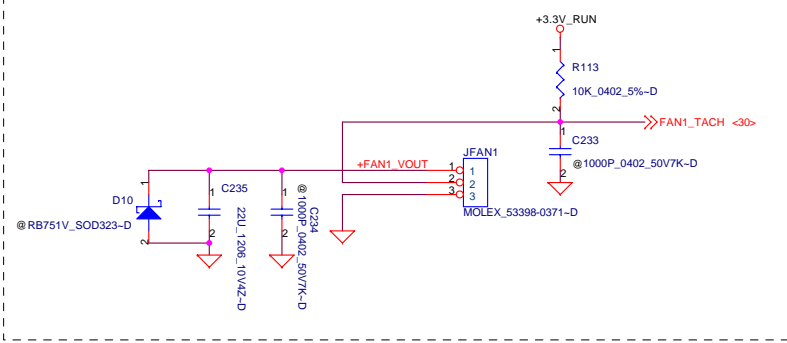
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Title		
Calistoga(6 of 6)		
Size	Document Number	Rev
	LA-3001	0.4
Date:	Monday, April 17, 2006	Sheet 15 of 73

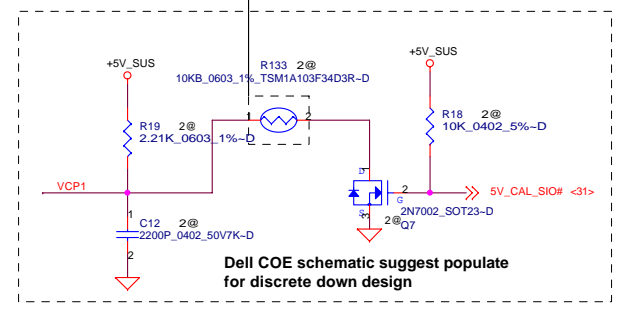
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FAN1 Control and Tachometer



Place thermal resistor near the SODIMM For discrete design

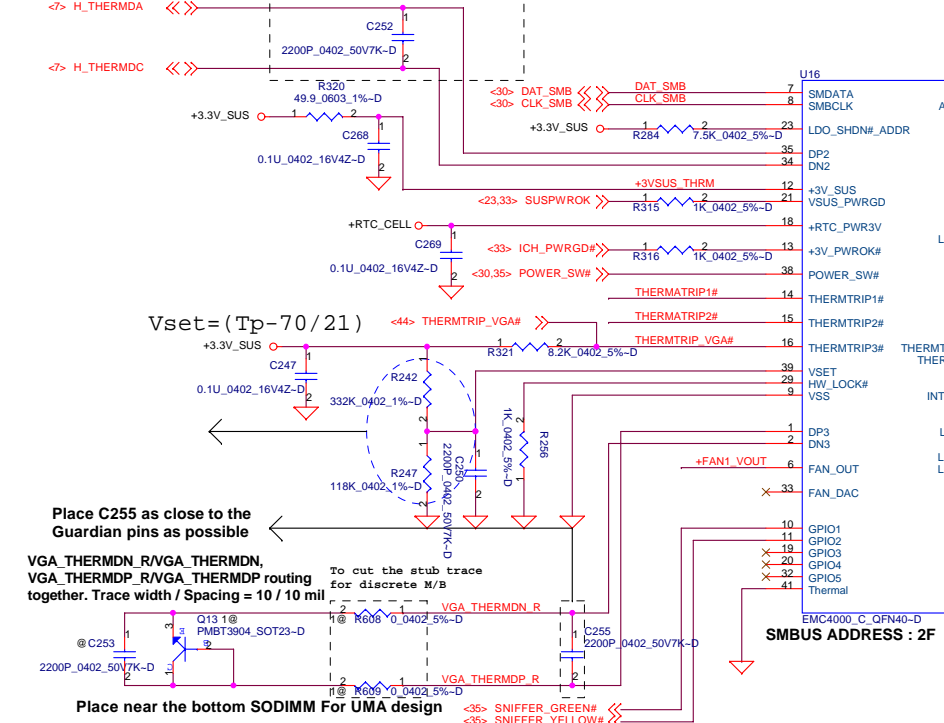


Dell COE schematic suggest populate for discrete down design

May need to place thermal resistor underneath WWAN Mini Card stuff this thermistor circuit for additional sensor in Discrete Down Designs

H_THERMDA/H_THERMDC routing together. Trace width / Spacing = 10 / 10 mil

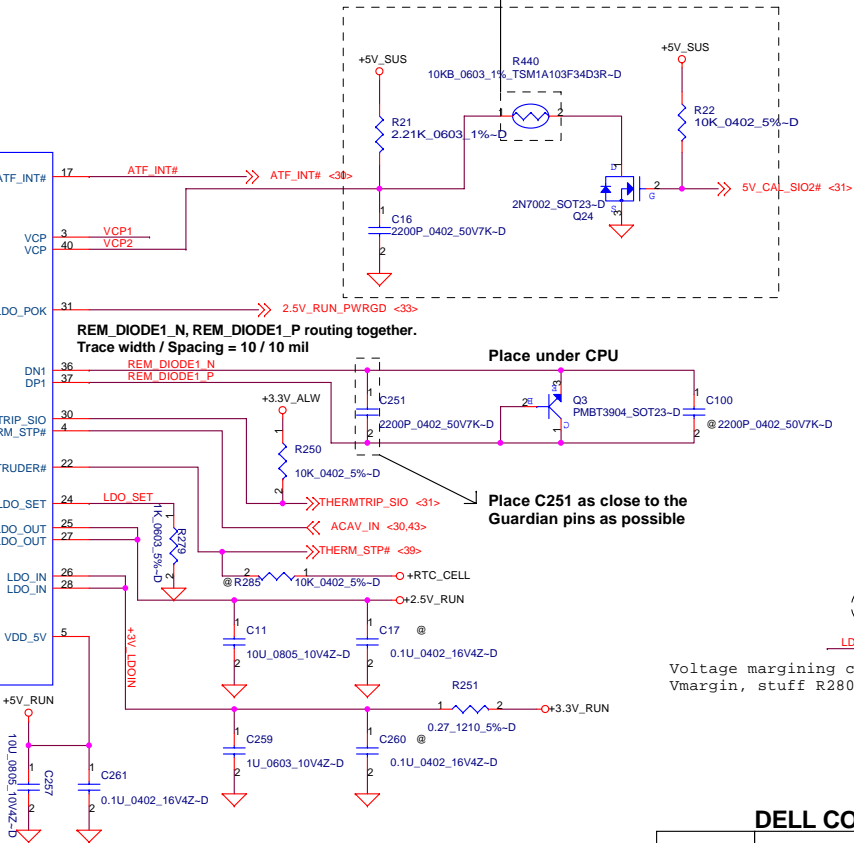
Place C252 as close to the Guardian pins as possible



REM_DIODE1_N, REM_DIODE1_P routing together. Trace width / Spacing = 10 / 10 mil

Place under CPU

Place C251 as close to the Guardian pins as possible



Voltage margining circuit for LDO output. For Vmargin, stuff R280=31.6K and R279=1K for production

For Discrete: Stuff R259, R249 and no stuff Q13, C253
For UMA: Stuff Q13 and no stuff R259, R249



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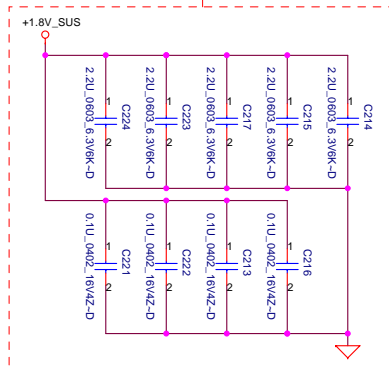
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Thermal sensor and Fan

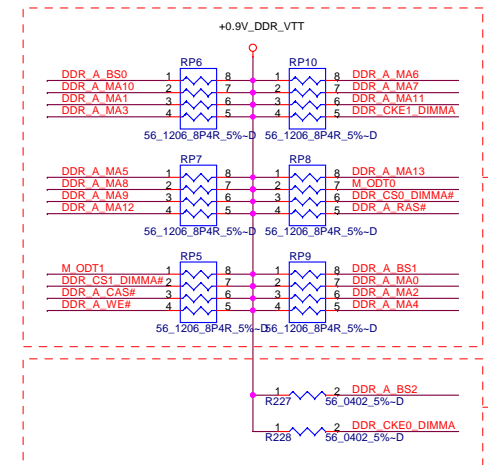
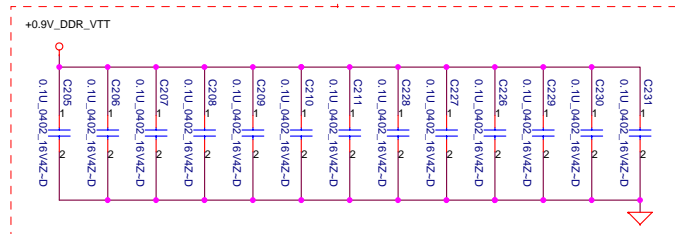
LA-3001P
Date: Monday, April 17, 2006 Sheet 16 of 73

<1> DDR_A_DQS#[0..7] <<>>
 <1> DDR_A_D[0..63] <<>>
 <1> DDR_A_DM[0..7] <<>>
 <1> DDR_A_DQS#[0..7] <<>>
 <1> DDR_A_MA[0..13] <<>>

Layout Note:
Place near JDIMA1

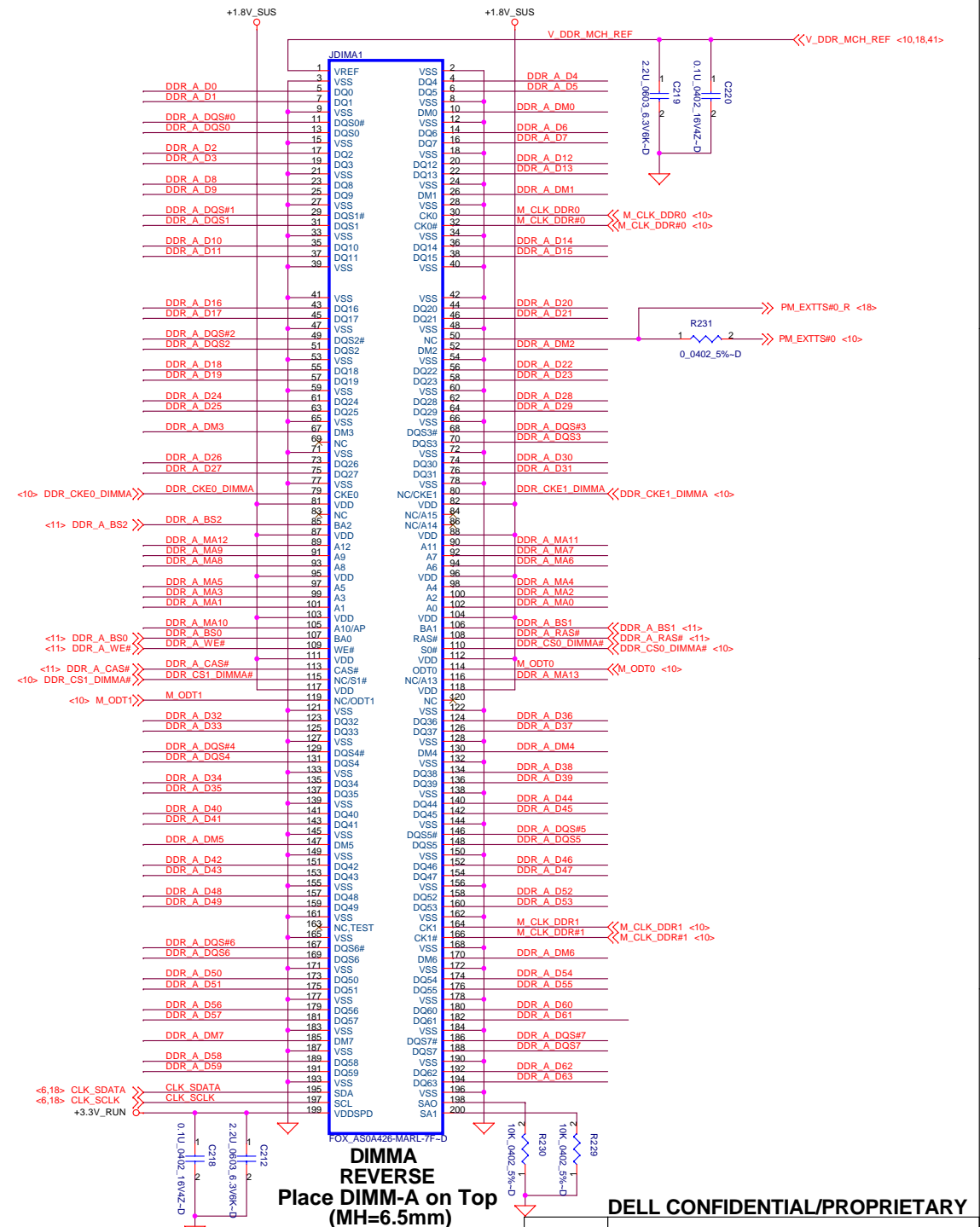


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



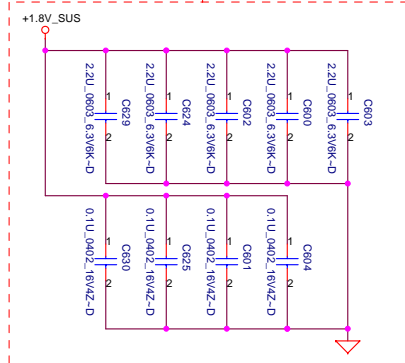
Layout Note:
Place this resistor closely JDIMA1, all trace length < 750 mil

Layout Note:
Place these resistor closely JDIMA1, all trace length Max=1.3"

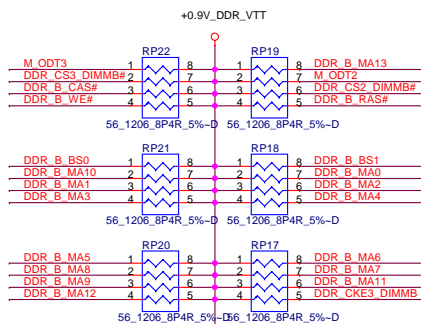
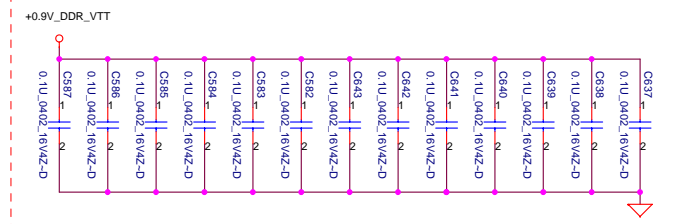


<1> DDR_B_DQS#[0..7] <<>>
 <1> DDR_B_D[0..63] <<>>
 <1> DDR_B_DM[0..7] <<>>
 <1> DDR_B_DQS#[0..7] <<>>
 <1> DDR_B_MA[0..13] <<>>

Layout Note:
Place near JDIMB1

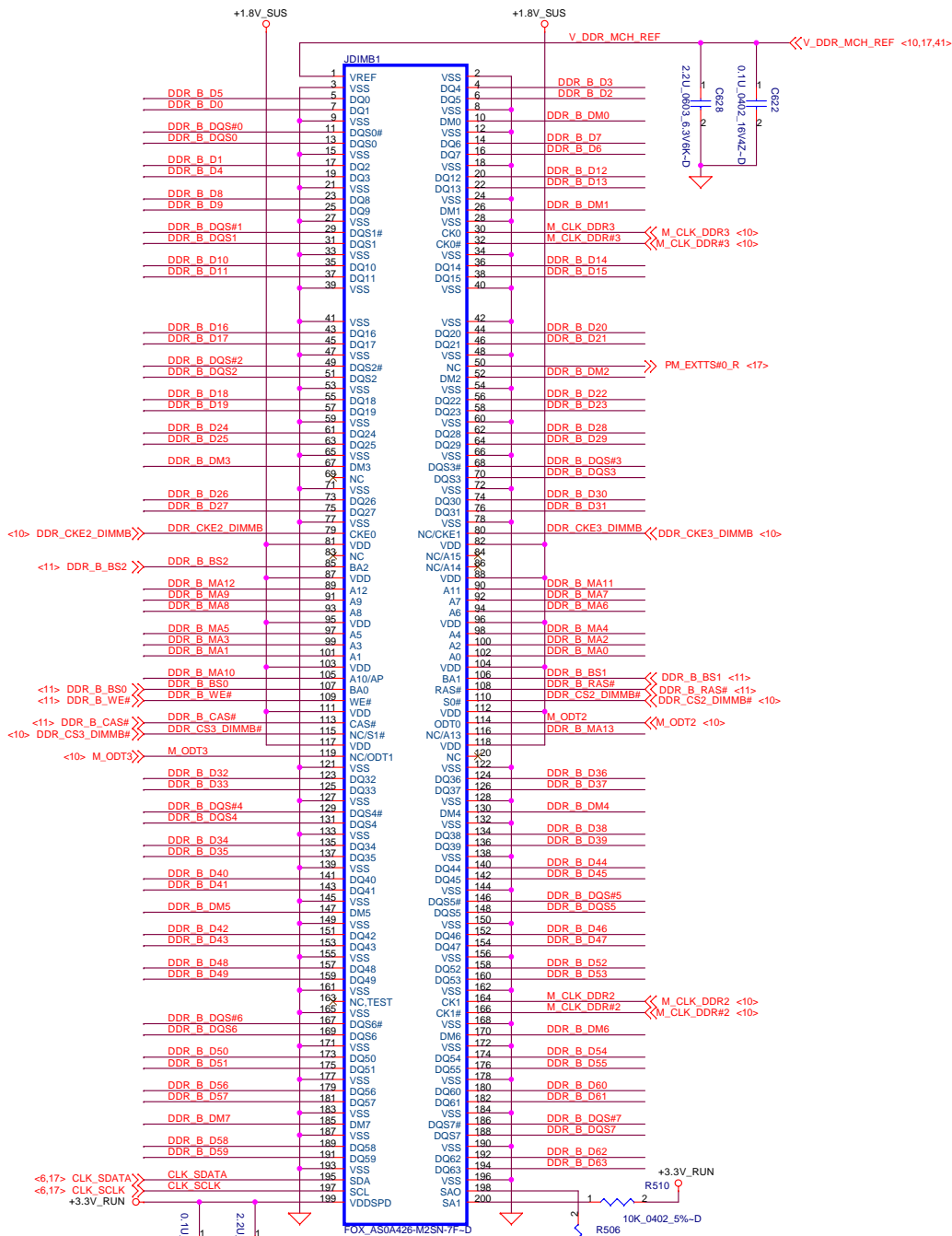


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



Layout Note:
Place these resistor closely JDIMB1,all trace length<750 mil

Layout Note:
Place these resistor closely JDIMB1,all trace length Max=1.3"



DIMMB STANDARD
Place DIMM-B on Bottom (5.2mm)

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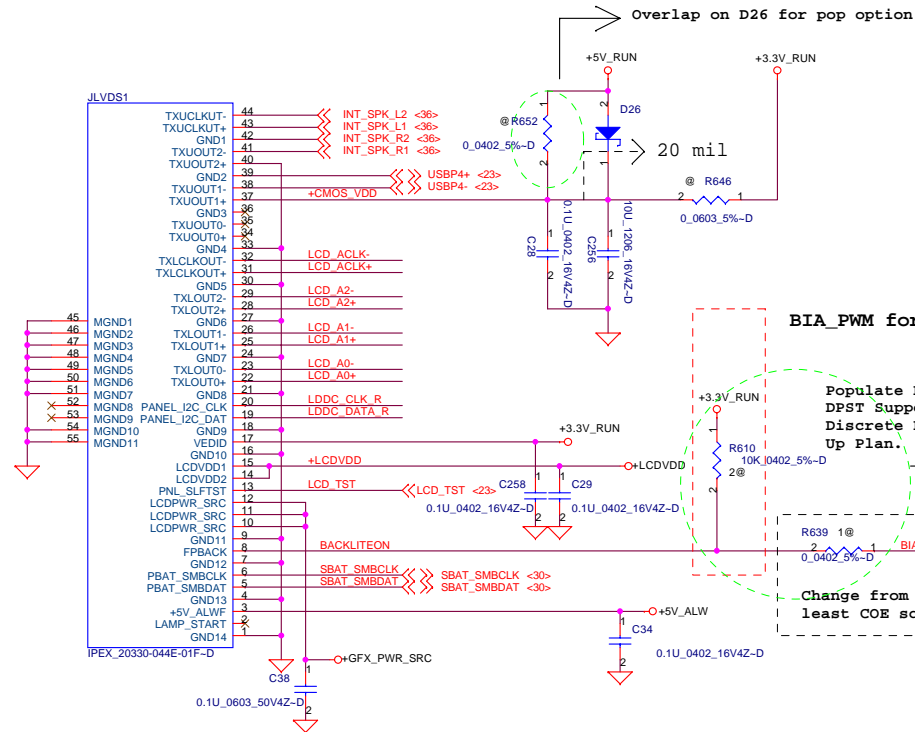
DDRII-SODIMM SLOT-B



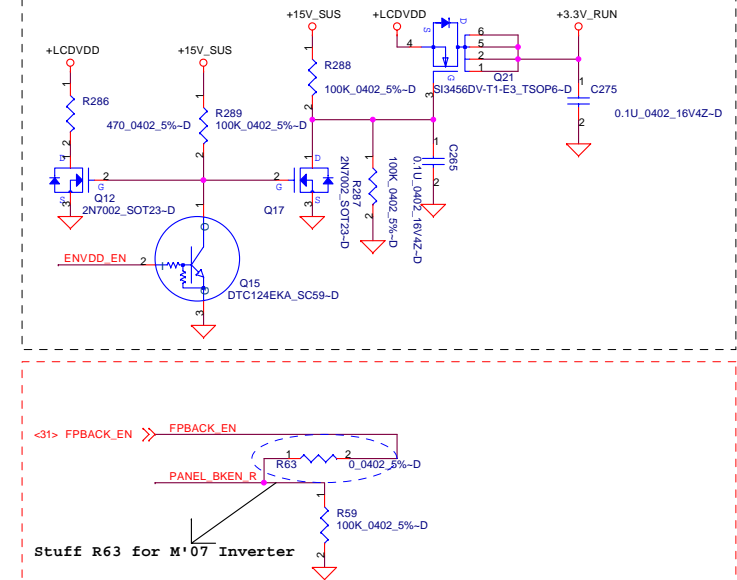
File		Rev	
Size		Document Number	
Date		Sheet	
Monday, April 17, 2006		18 of 73	

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Overlap on D26 for pop option

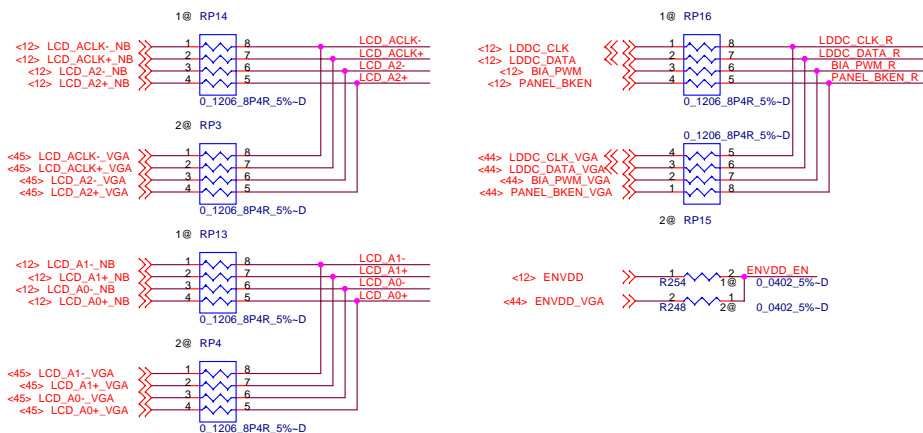


LCD Power



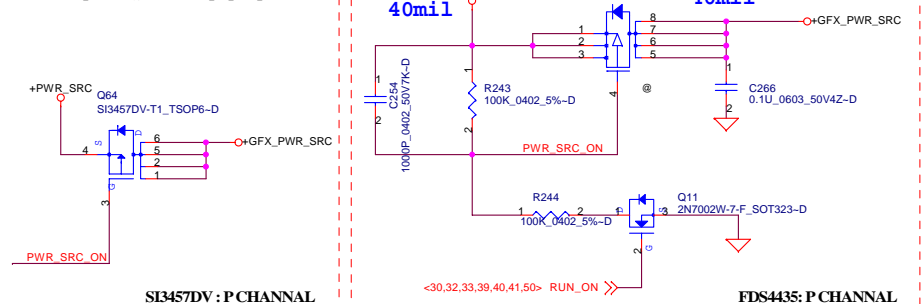
Please put the resistors close to connector side

For Discrete: Populating RP3,RP4,RP15,R248
For UMA: Populating RP14,RP13,RP16,R254



Dual layout for Q16

Overlap on Q16 for pop option

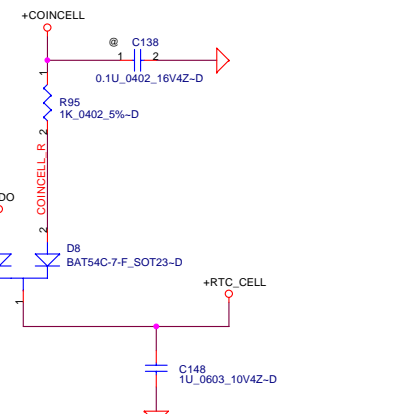
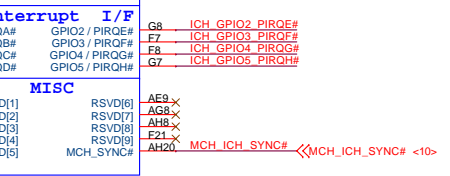
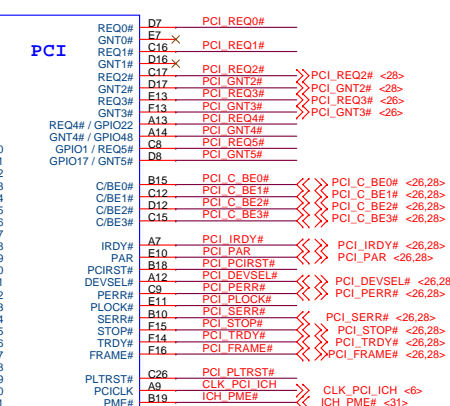
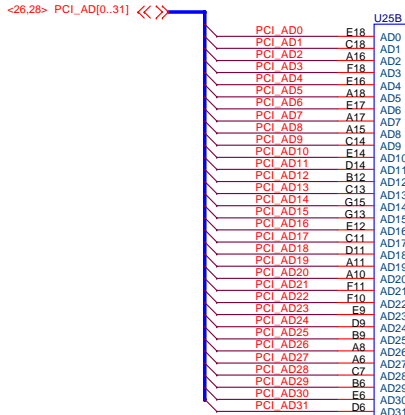
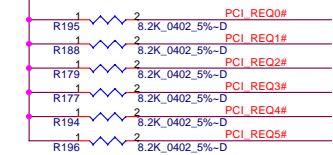
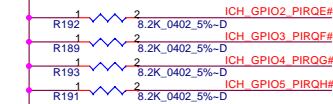
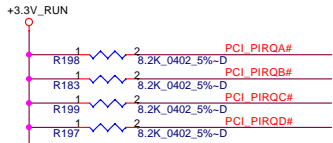
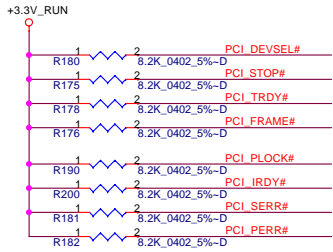


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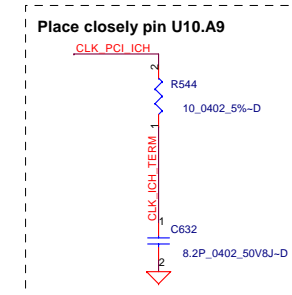
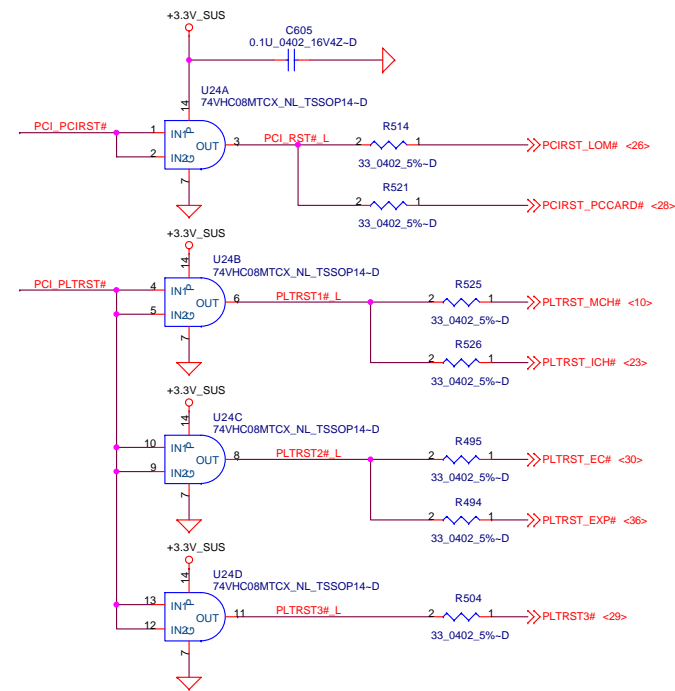
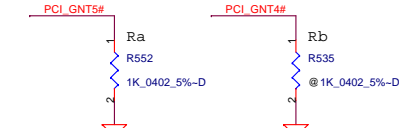
File			
LVDS Conn			
Size	Document Number	Rev	
	LA-3001P	0.4	
Date:	Monday, April 17, 2006	Sheet	19 of 73

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ICH Boot BIOS select

		GNT5# Ra	GNT4# Rb
LPC	11	unstuff	unstuff
PCI	10	unstuff	stuff
SPI	01	stuff	unstuff

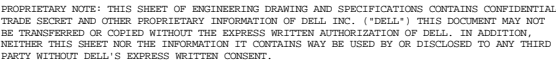


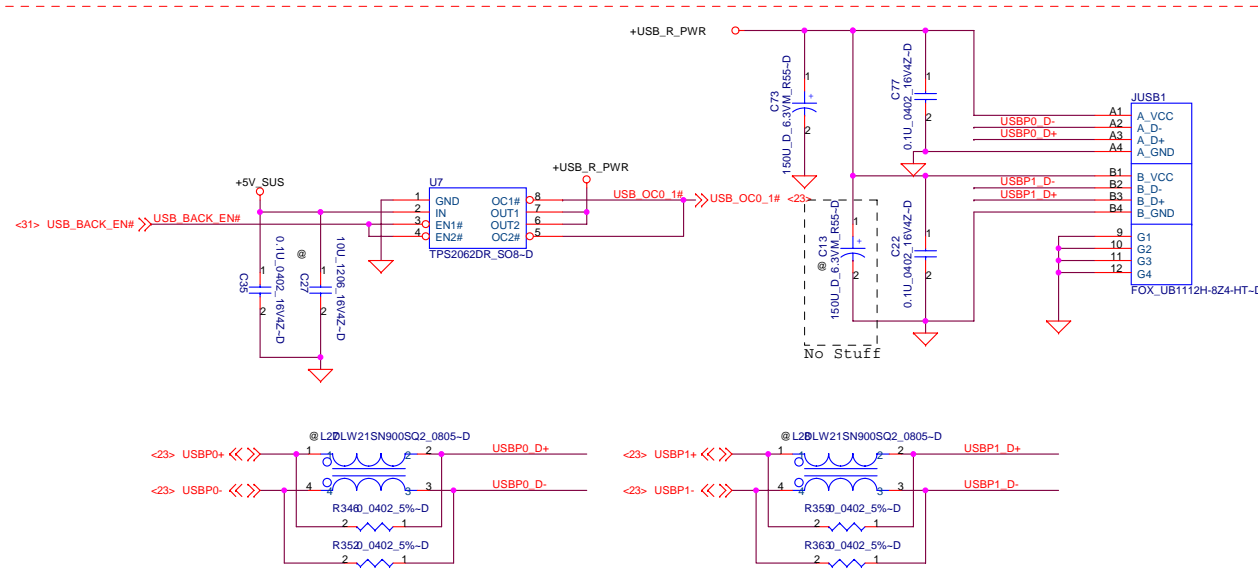
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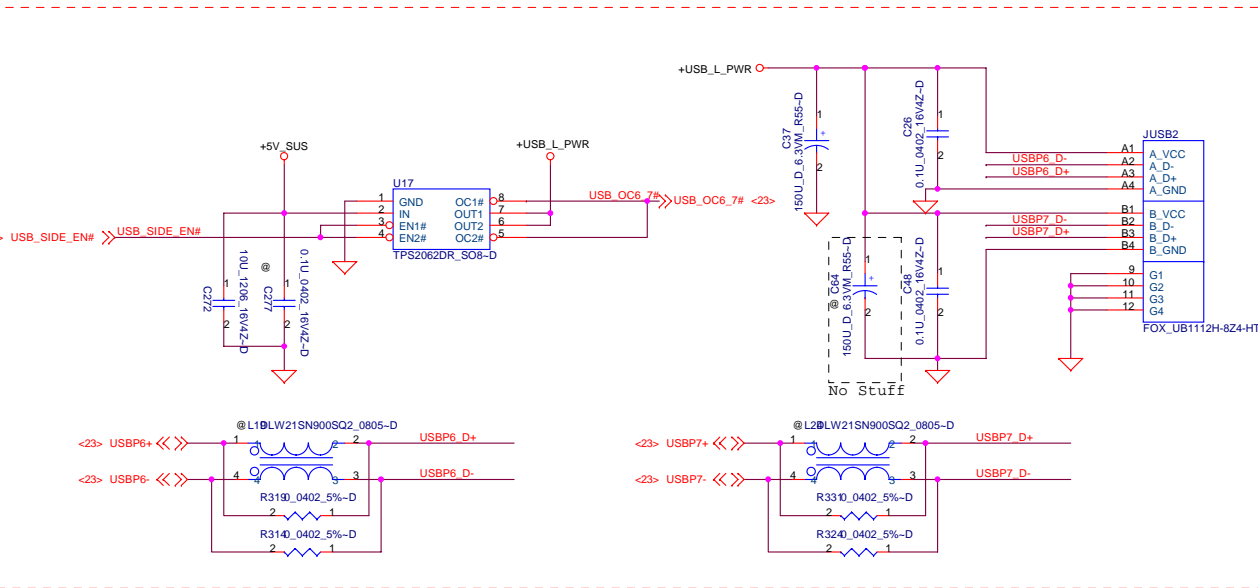
Compal Electronics, Inc.	
File	ICH7(1/4)
Size	Document Number
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Sheet	21 of 73

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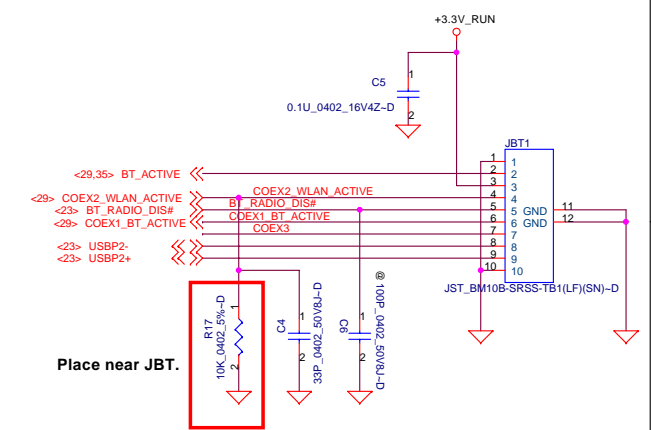
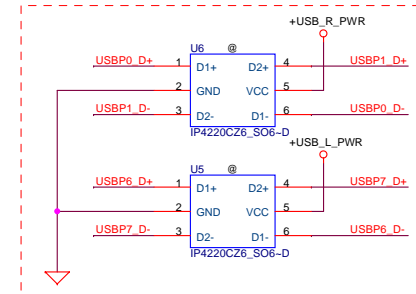




USB PORT#	DESTINATION
0	JUSB1 (Ext Back Right Side)
1	JUSB1 (Ext Back Right Side)
2	Blue Tooth
3	EXPRESS CARD
4	CCD Camera
5	ECE5011 HUB
6	JUSB2 (Ext Back Left Side)
7	JUSB2 (Ext Back Left Side)



Place U5, U6 as close as USB connector.



Place near JBT.

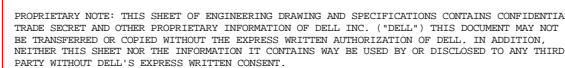
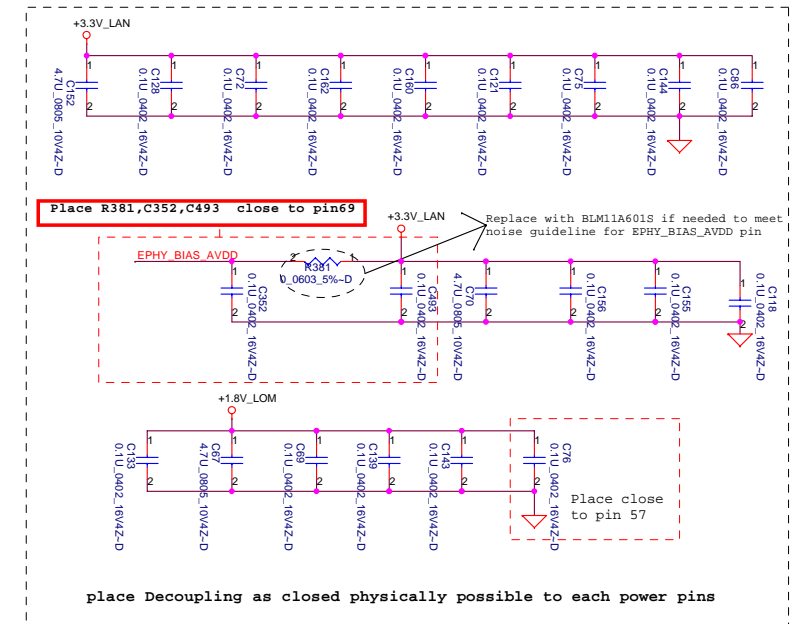
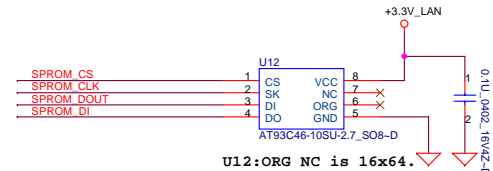
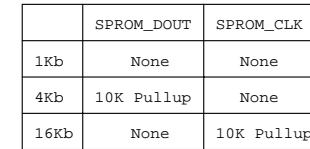
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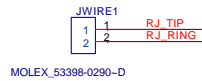


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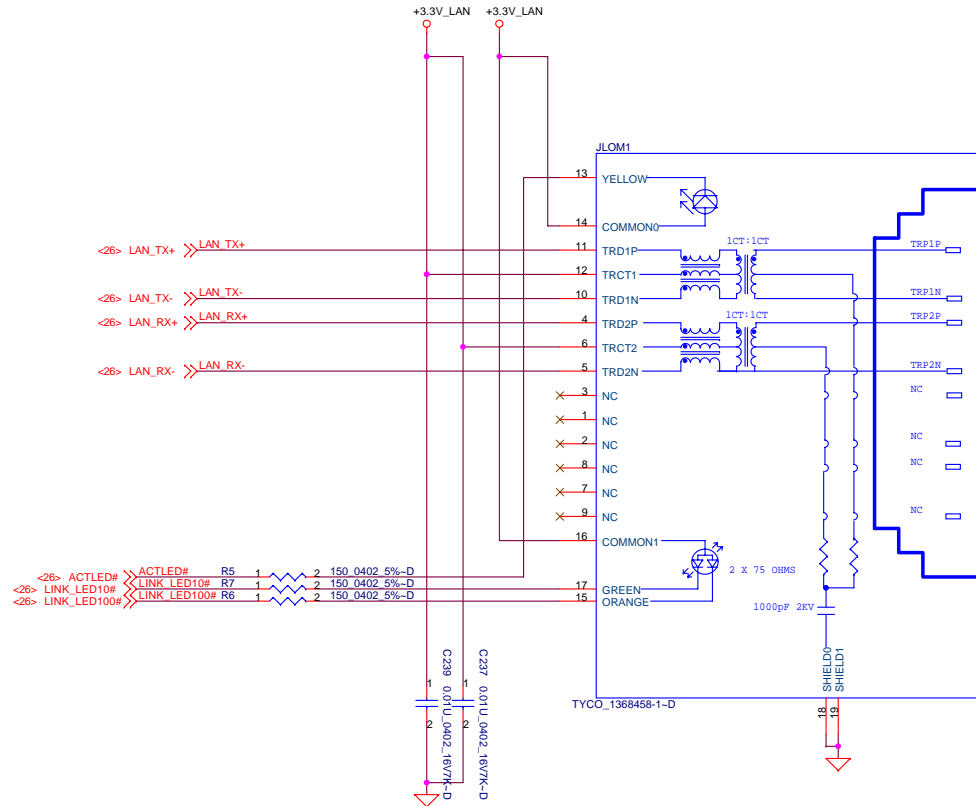
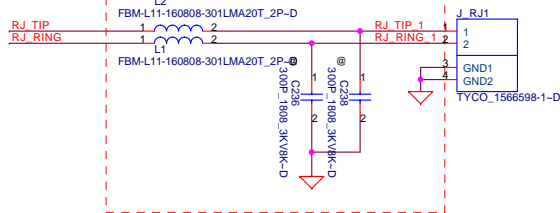
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USB 2.0 PORT		
File	Document Number	Rev
	LA-3001P	0.4
Date: Monday, April 17, 2006	Sheet 25 of 73	





Layout Note: Place close to the J_RJ1



<26> ACTLED# >> ACTLED# R5 1 2 150 0402 5%-D
 <26> LINK_LED10# >> LINK_LED10# R7 1 2 150 0402 5%-D
 <26> LINK_LED100# >> LINK_LED100# R6 1 2 150 0402 5%-D

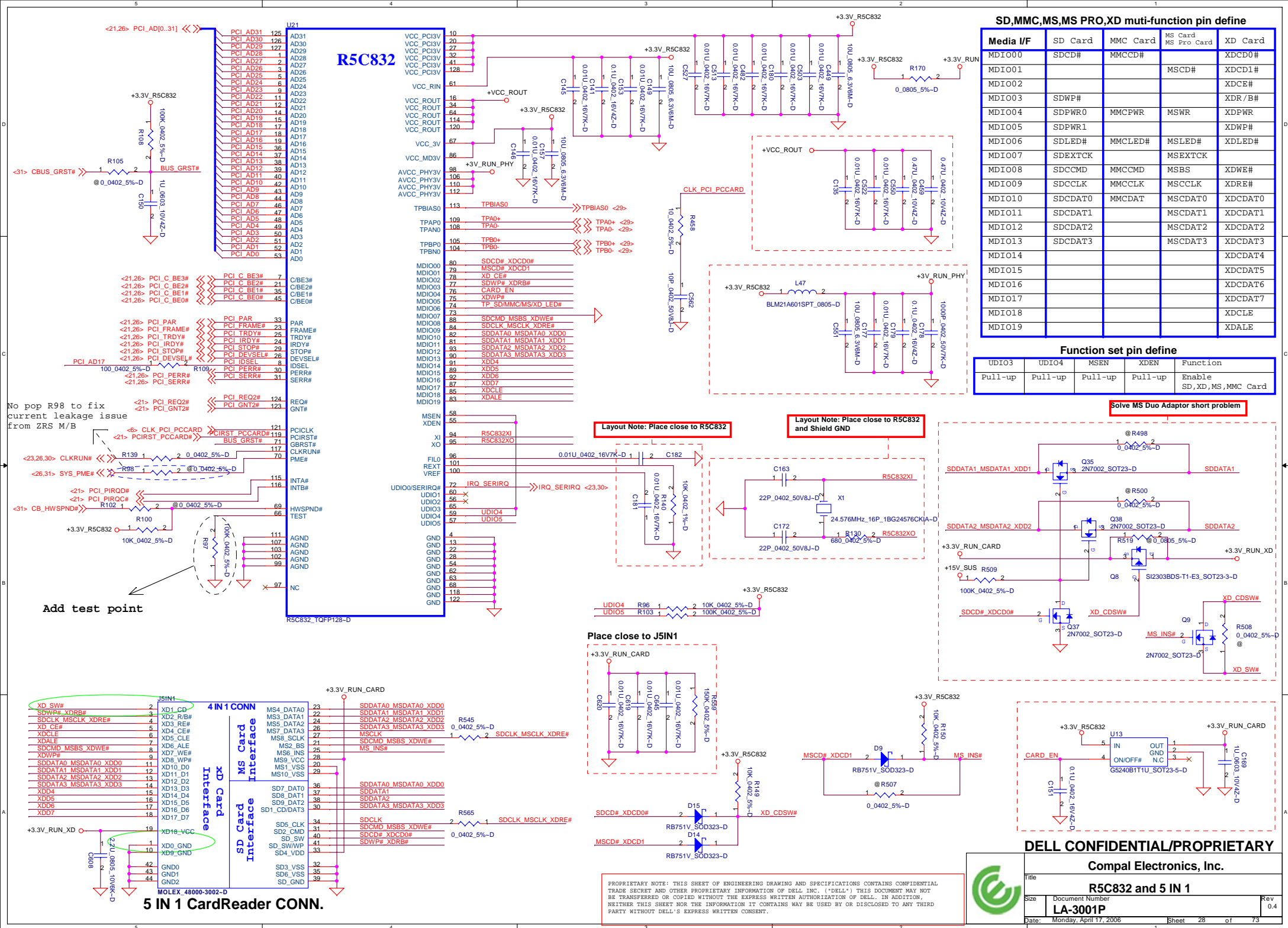
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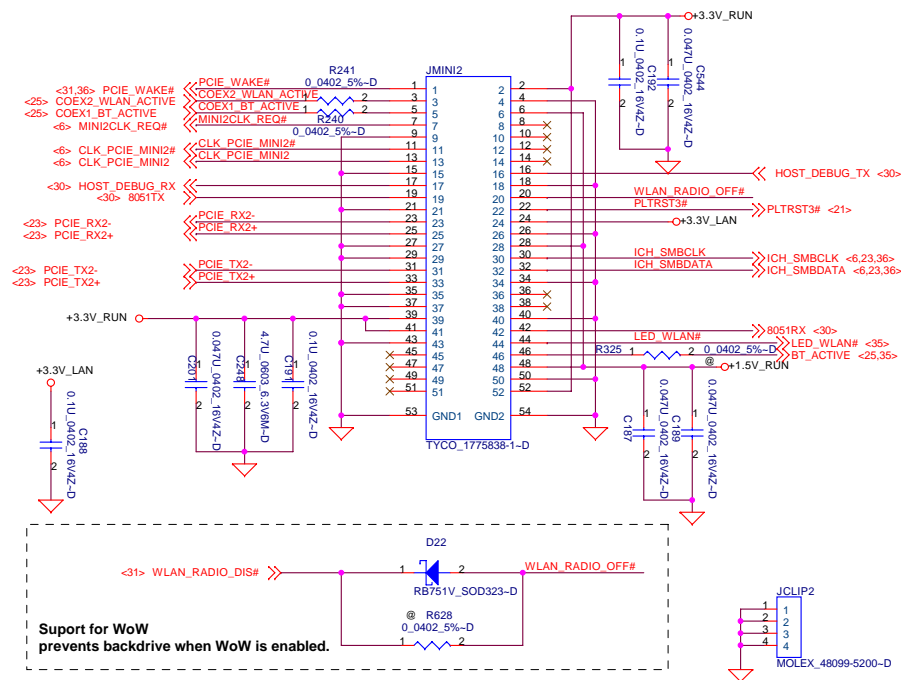


Title		
Magnetic & RJ45		
Size	Document Number	Rev
	LA-3001	0.4
Date:	Monday, April 17, 2006	Sheet 27 of 73

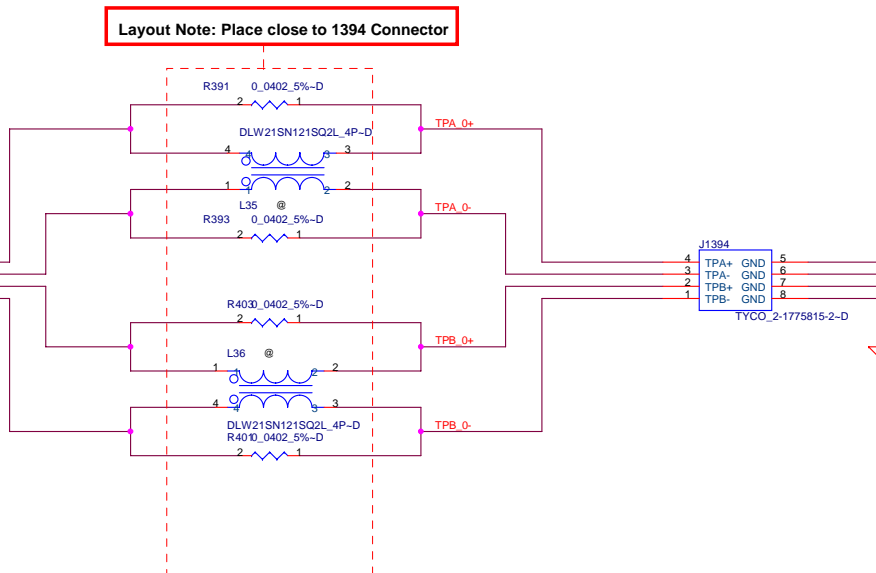
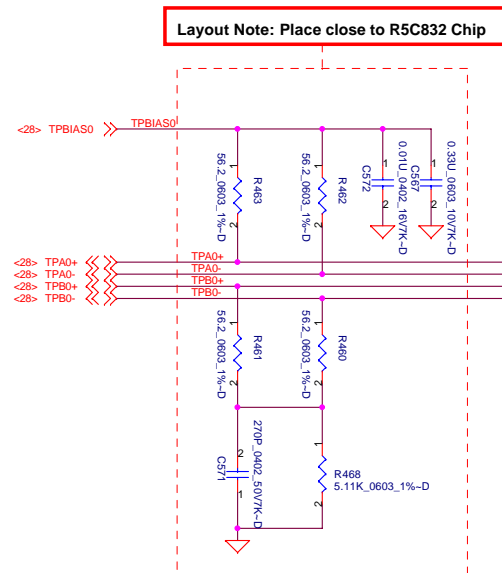
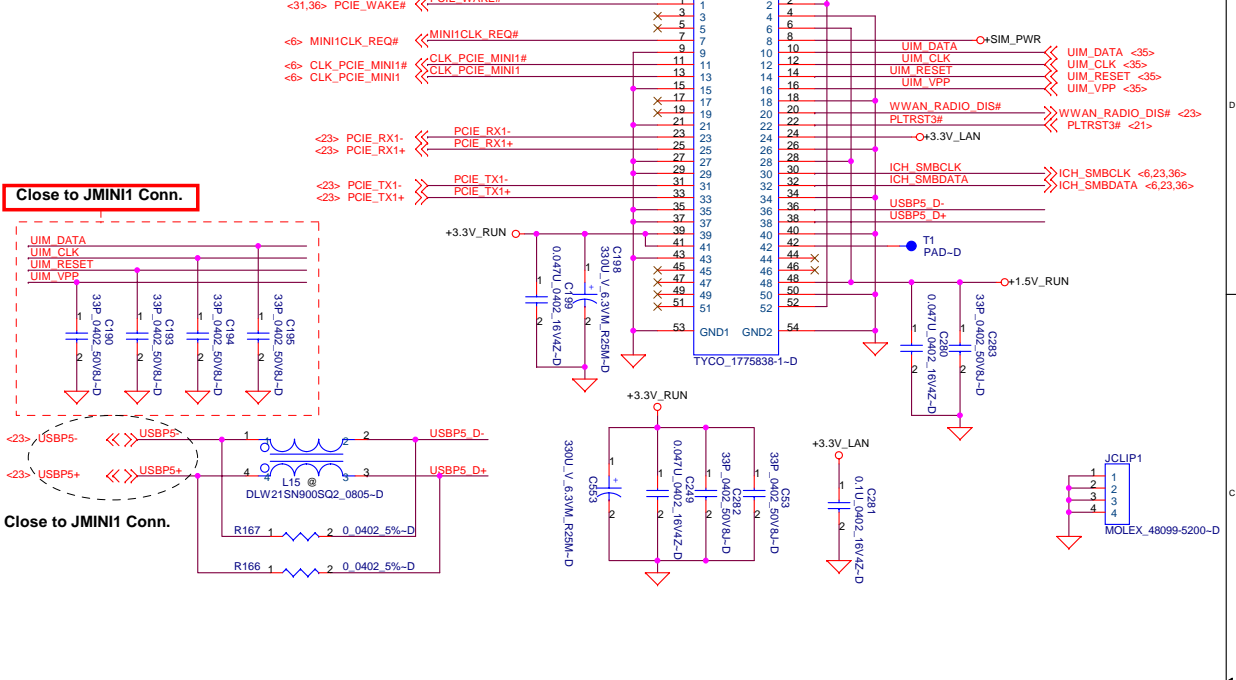
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Mini Wireless LAN Card



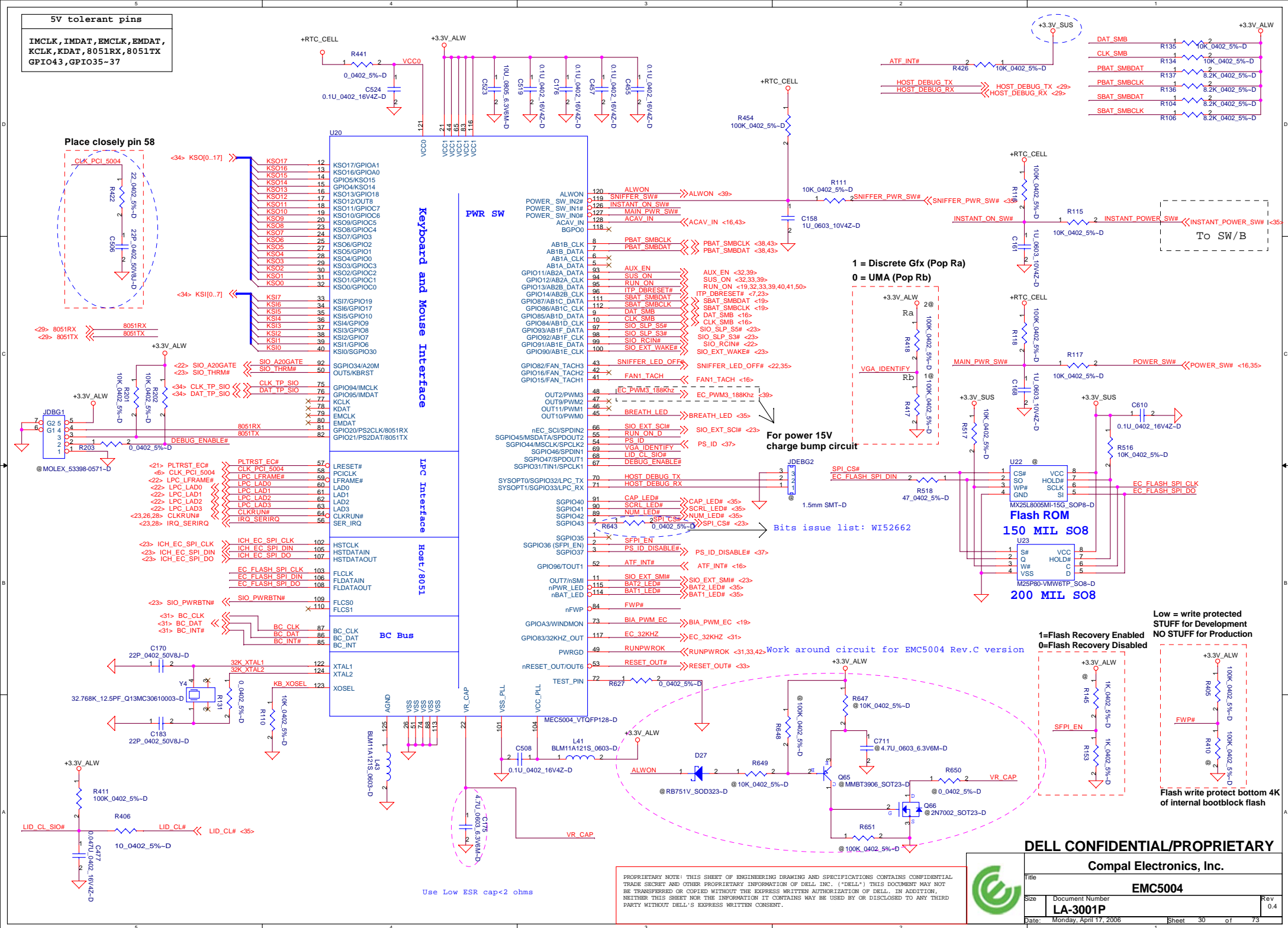
Mini Wireless WAN Card

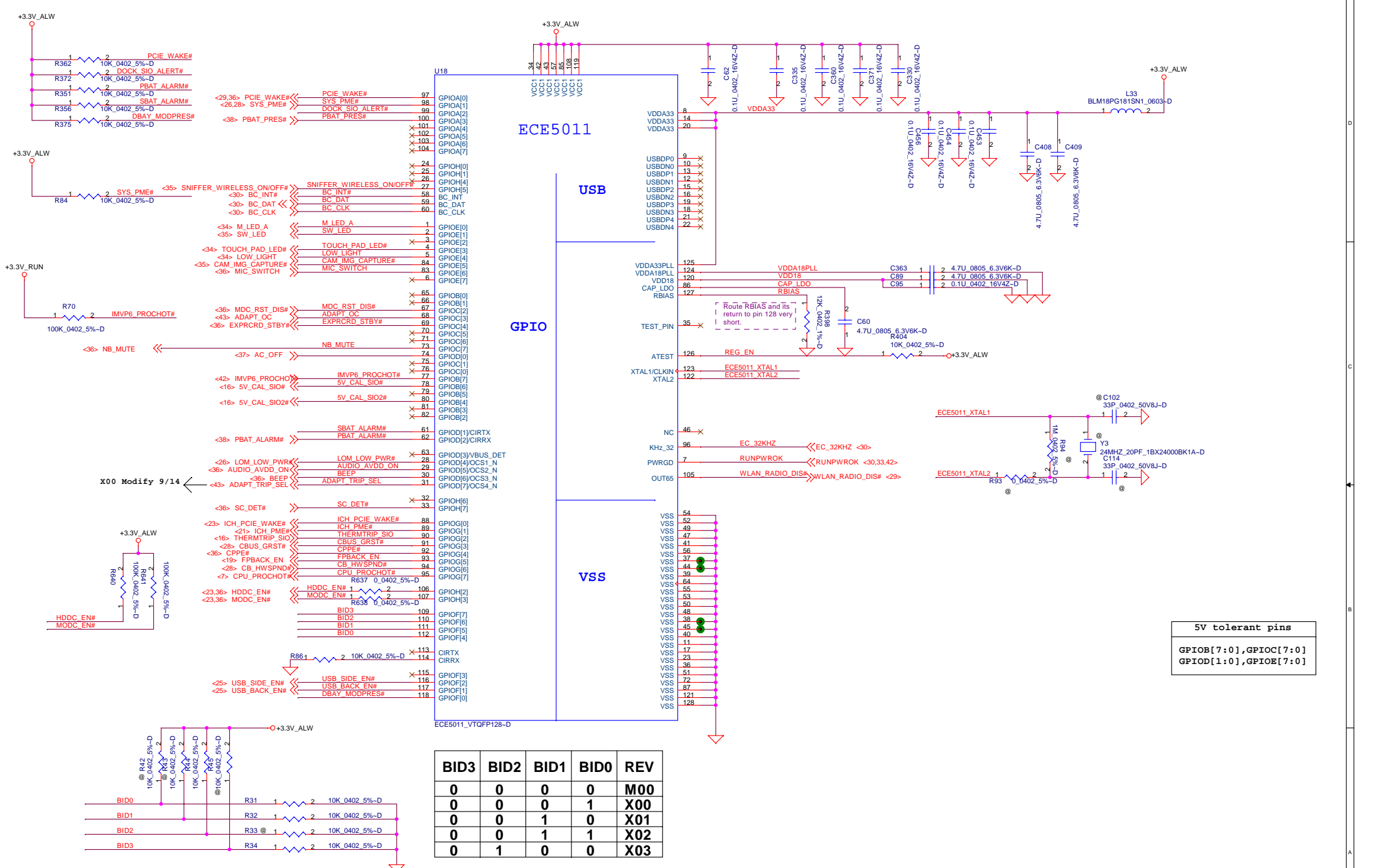


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	MINI CARD & 1394 Connector		
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	Date: Monday, April 17, 2006	Sheet 29 of 73	

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5V tolerant pins

GPIOB[7:0], GPIOC[7:0]
GPIOD[1:0], GPIOE[7:0]

BID3	BID2	BID1	BID0	REV
0	0	0	0	M00
0	0	0	1	X00
0	0	1	0	X01
0	0	1	1	X02
0	1	0	0	X03



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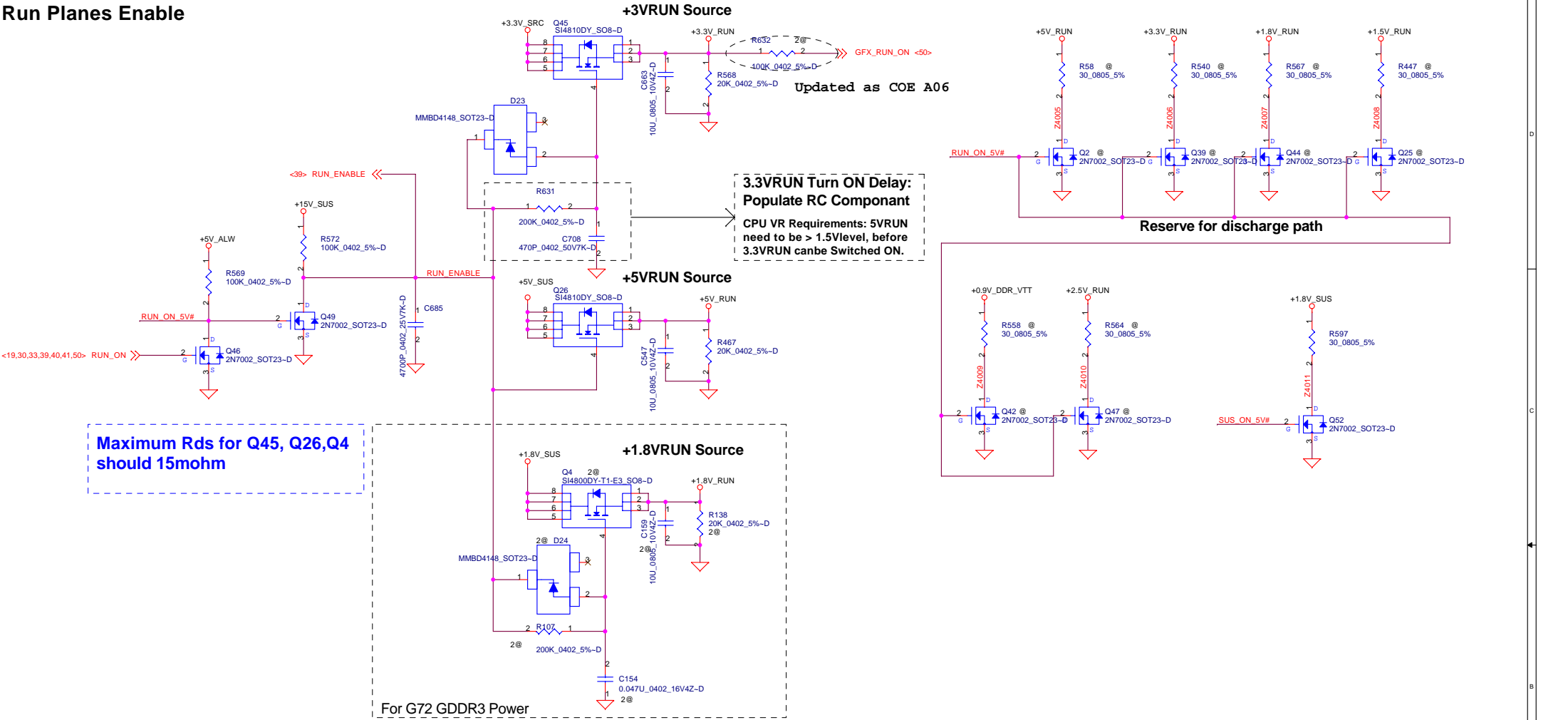
HUB/ECE5011

Size Document Number Rev
LA-3001P 0.4

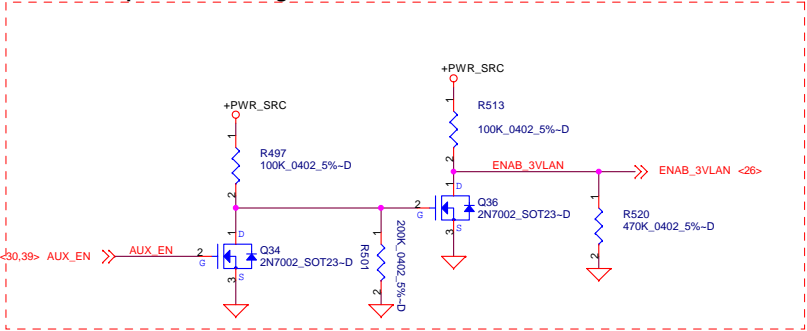
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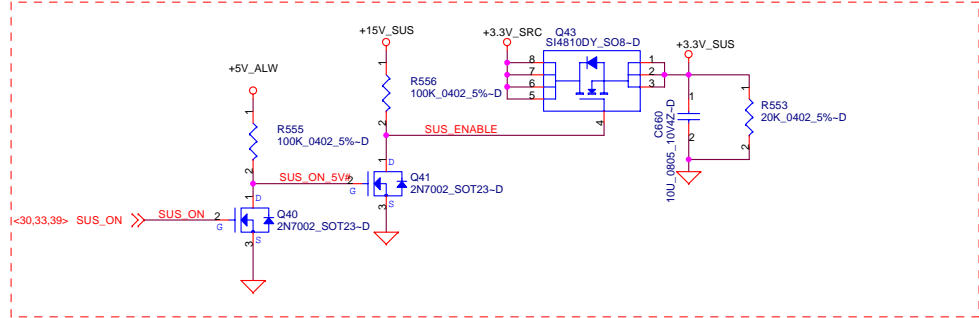
Run Planes Enable



+3.3V_LAN power enable signal



+3.3V_SUS Source



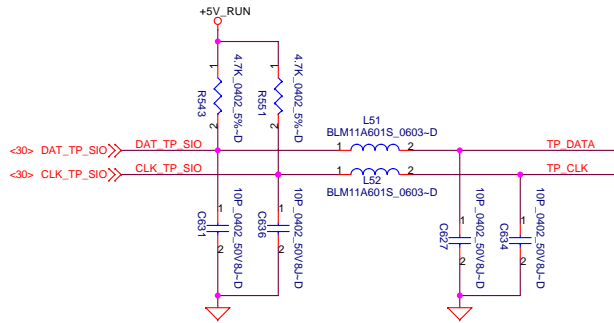
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Compal Electronics, Inc.

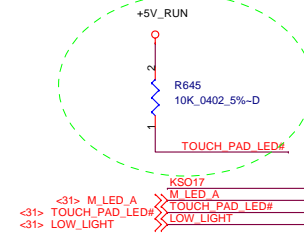


POWER CONTROL		
File	Document Number	Rev
Size	LA-3001P	0.4
Date	Monday, April 17, 2006	Sheet 32 of 73

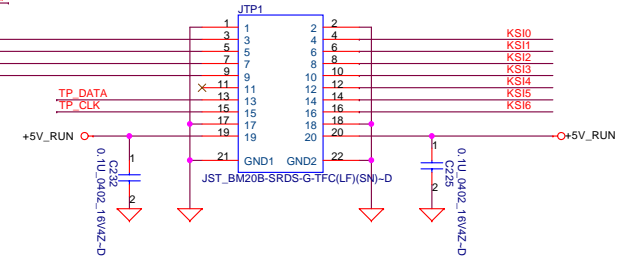
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Add a 10K pull-up to +5V_RUN from bits issue list: W152078

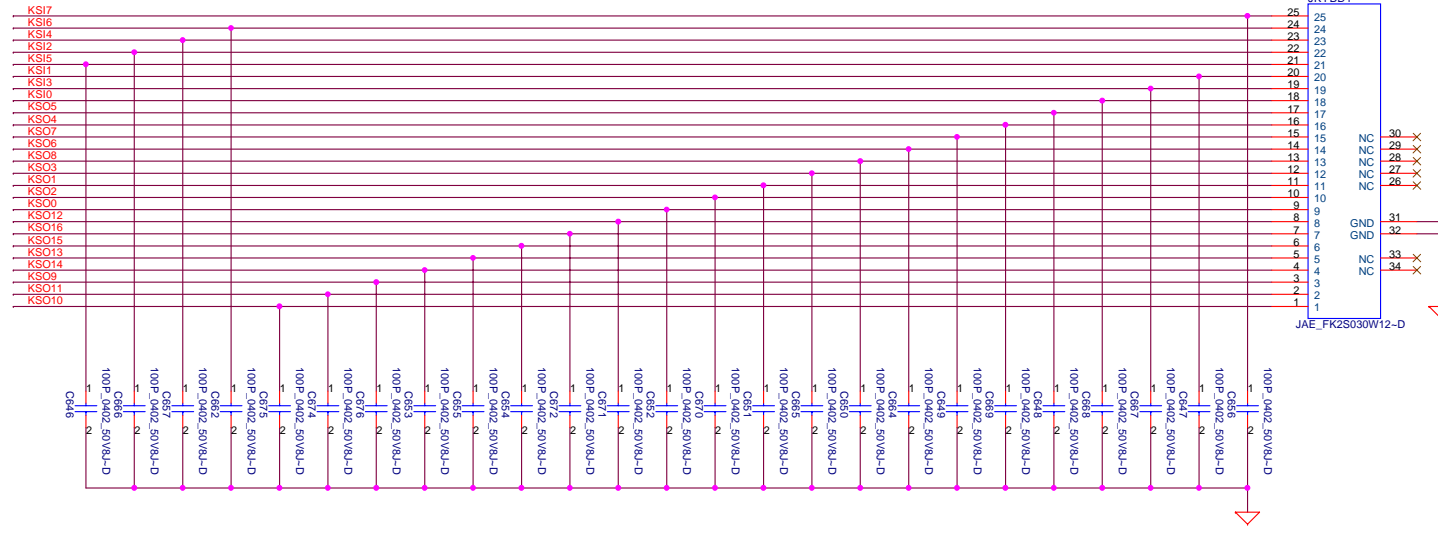
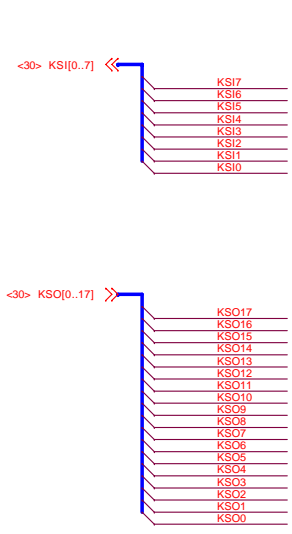


T/P & Media CONN.



LED Control		
Status	LOW_LIGHT	TOUCH_PAD_LED#
OFF	L	L
LOW	L	H
HIGH	H	H

Signals	Description
M_LED_A	High bright for Media LED
	High bright for Touch PAD LED
	Low bright for Media LED/Touch PAD LED



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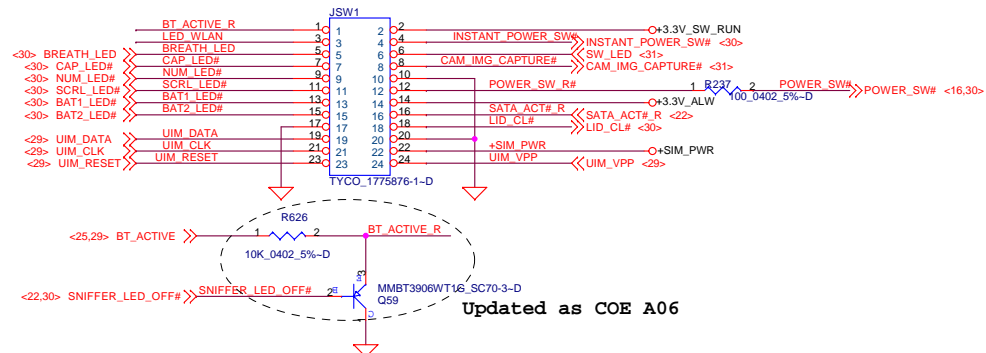
Compal Electronics, Inc.



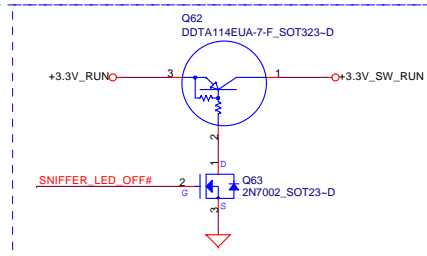
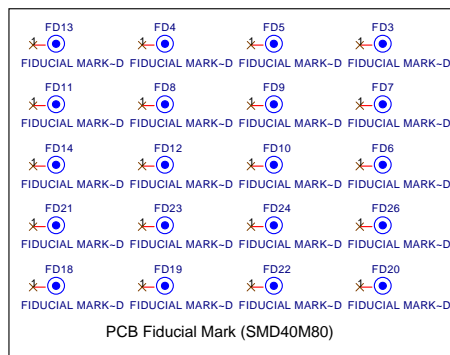
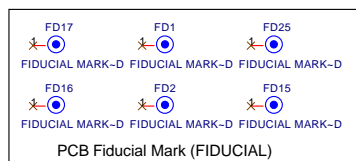
Title		
INT KB/Touch Pad/Media CONN		
Size	Document Number	Rev
	LA-3001P	0.4

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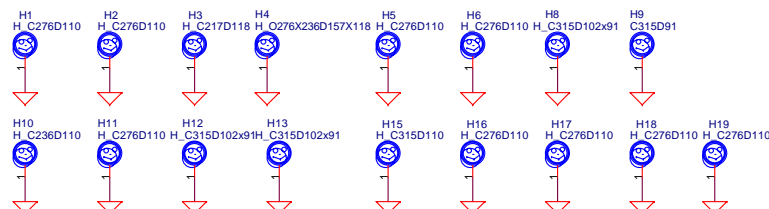
POWER Button CONN.



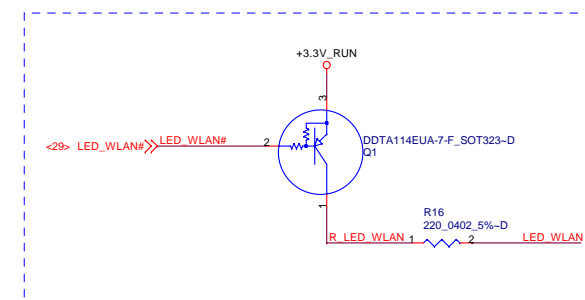
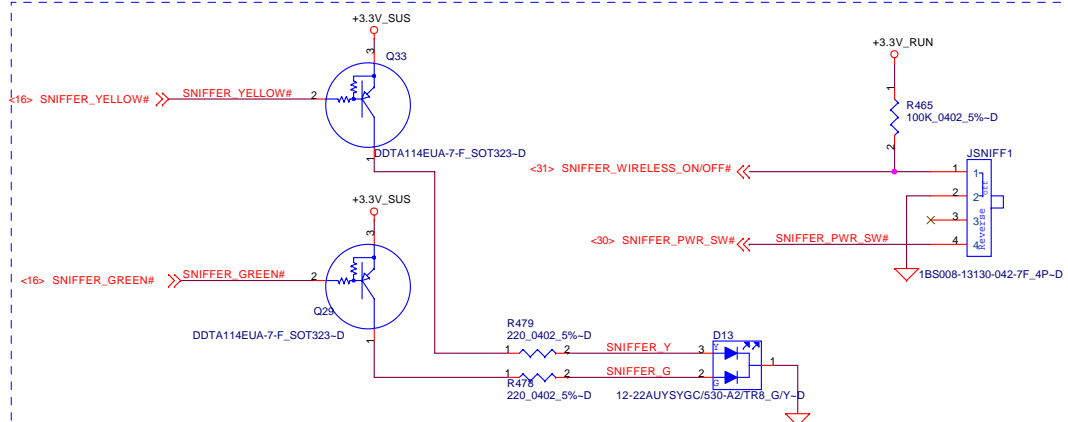
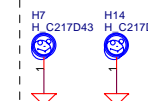
Fiducial Mark



Screw



VGA stand-Off



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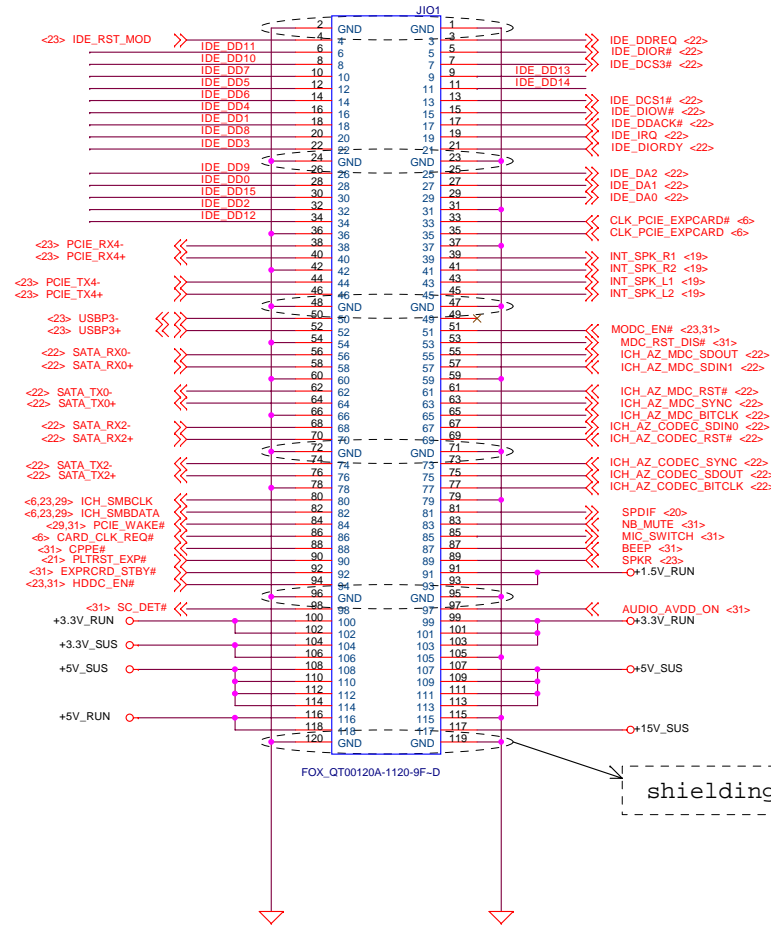
Title			
SW LED/B & ME & spare parts			
Size	Document Number		Rev
	LA-3001P		0.0
Date:	Monday, April 17, 2006	Sheet	35 of 73

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CD-ROM IDE BUS

EXPRESS CARD

SATA HDD



SPEAKER

MDC

AC 97

IDE_DD[0..15] <<>> IDE_DD[0..15] <22>

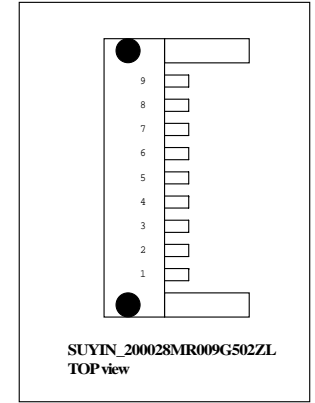
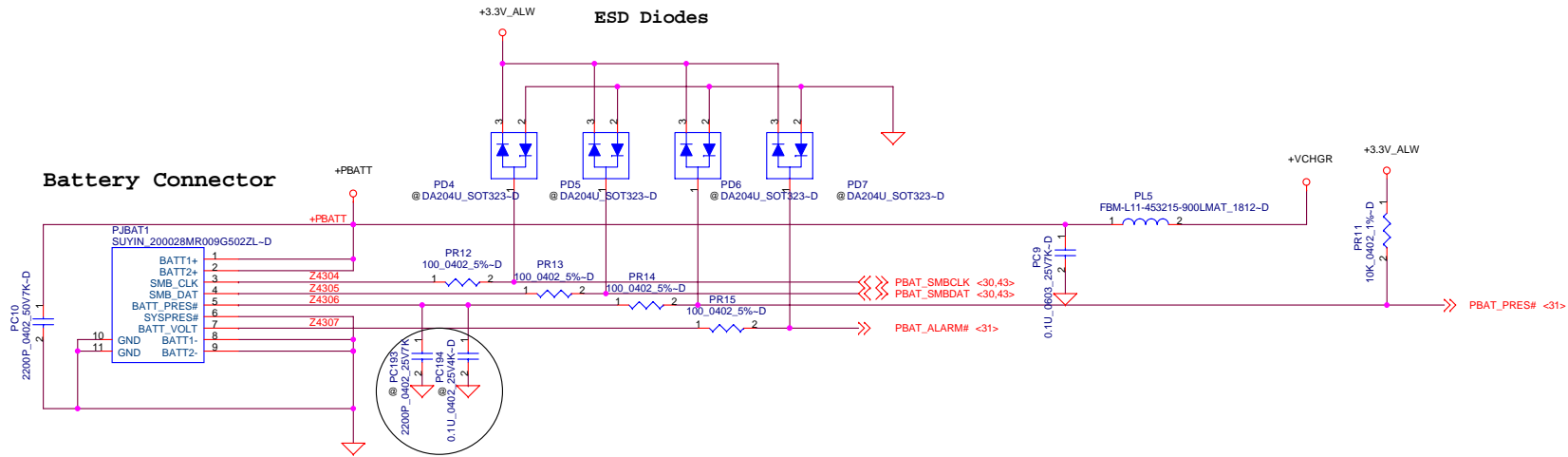
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Date:	Monday, April 17, 2006	Sheet	36 of 73



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Battery Conn

Bali

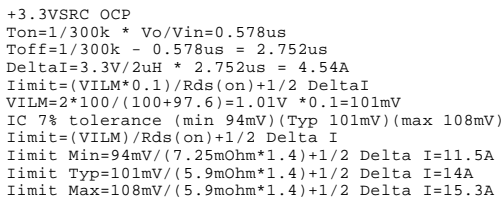
Rev X02

Date: Monday, April 17, 2006 Sheet 38 of 73


MAX8734 Current Limit Characteristics				
	min	typ	max	Tolerance
VLIM=0.5V	40mV	50mV	60mV	20%
VLIM=1.0V	93mV	100m	107mV	7%

5 Volt +/-5%
design current: 4.1A
peak current: 5.8A
Min OCP: 5.9A

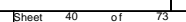
3.3 Volt +/-5%
design current: 7A
Max current: 9.9A
Min OCP: 11.5A

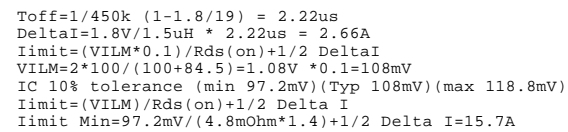
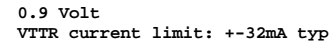


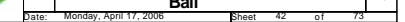
```
+5VSUSP OCP
Ton=1/200k * Vo/Vin=1.316us
Toff=1/200k - 1.316us = 3.684us
DeltaI=5V/4.7uH * 3.684us = 3.92A
Iimit=(VILM*0.1)/Rds(on)+1/2 DeltaI
VILM=2*102/(102+84.5)=1.094V *0.1=109.4mV
IC 7% tolerance (min 101.7mV)(Typ 109.4mV)(max 117mV)
Iimit=(VILM)/Rds(on)+1/2 Delta I
Iimit Min=101.7mV/(20mOhm*1.4)+1/2 Delta I=5.86A
Iimit Typ=109.4mV/(16mOhm*1.4)+1/2 Delta I=6.8A
Iimit Max=117mV/(16mOhm*1.4)+1/2 Delta I=7.2A
```

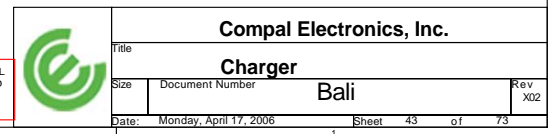
	Compal Electronics, Inc.			
	Title			
	+3.3V/+5V			
	Size	Document Number		Rev
		Bali		X02
	Date	Monday, April 17, 2006		Sheet 34 of 75

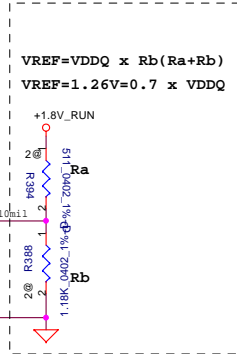
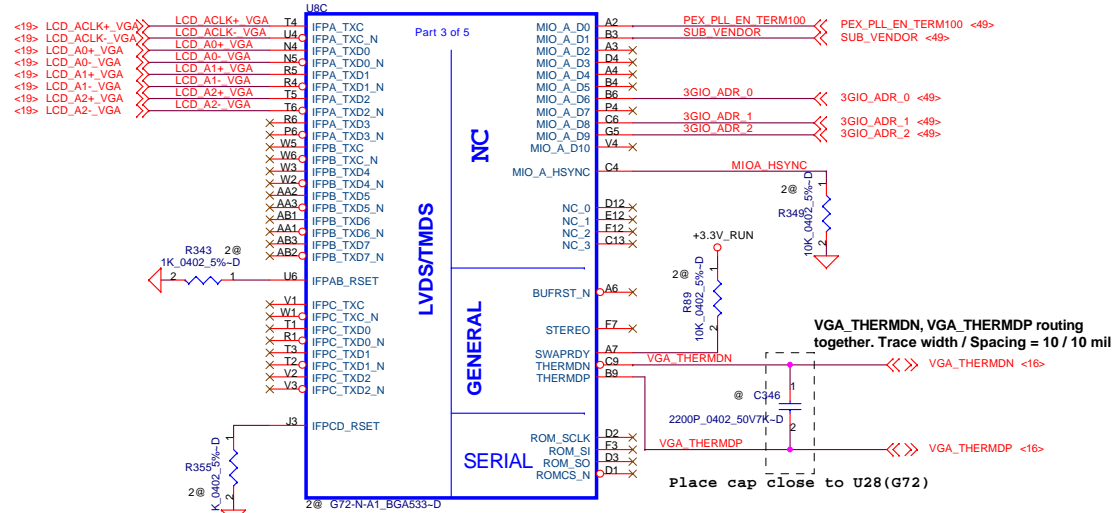
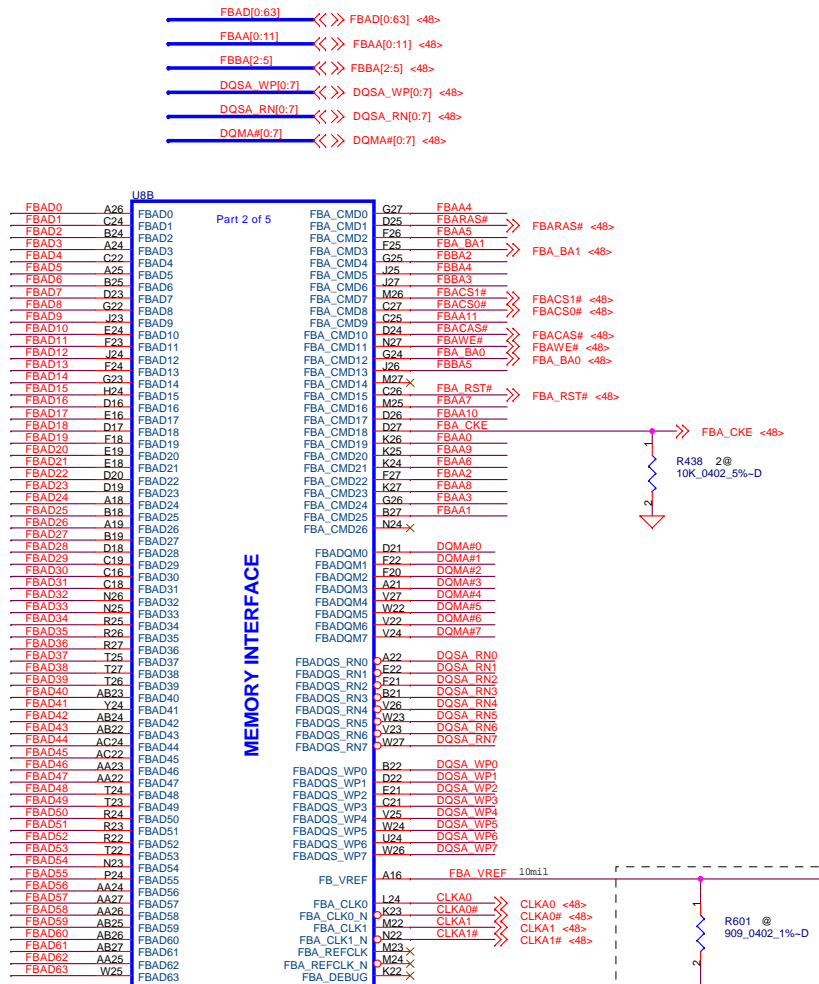
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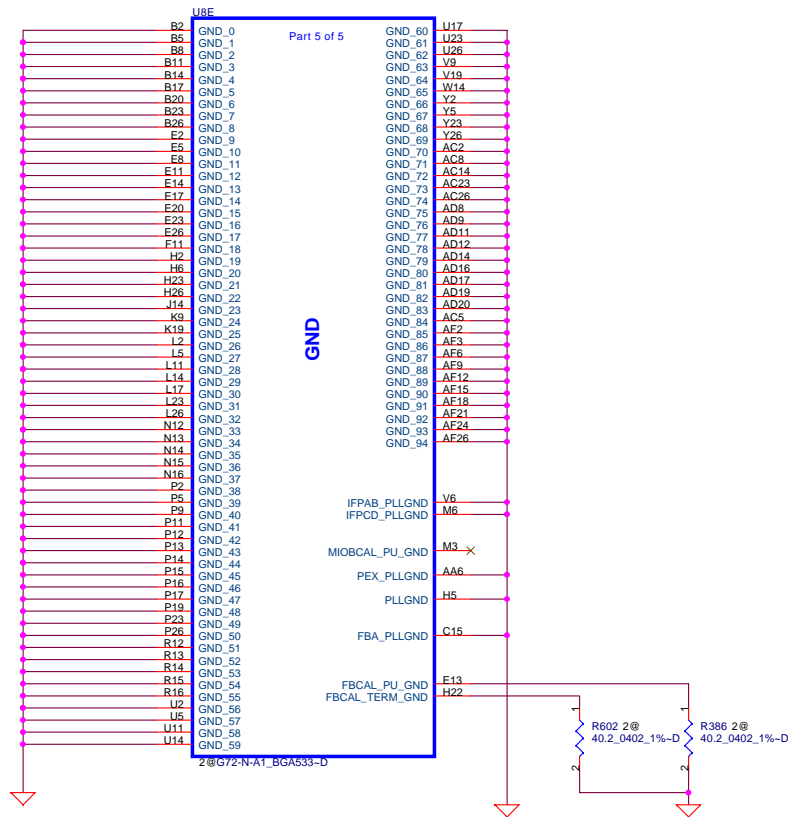
Calibration	GDDR3
FB_CALx_PD_VDDQ	60
FB_CALx_PU_GND	40
FB_CALx_TERM_GND	60
VREF RATIO	0.7xFBVDDQ

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Compal Electronics, Inc.			
Title NVG72 Memory Interface, LVDS			
Size	Document Number	Rev 0.4	
Date		Sheet 45 of 73	

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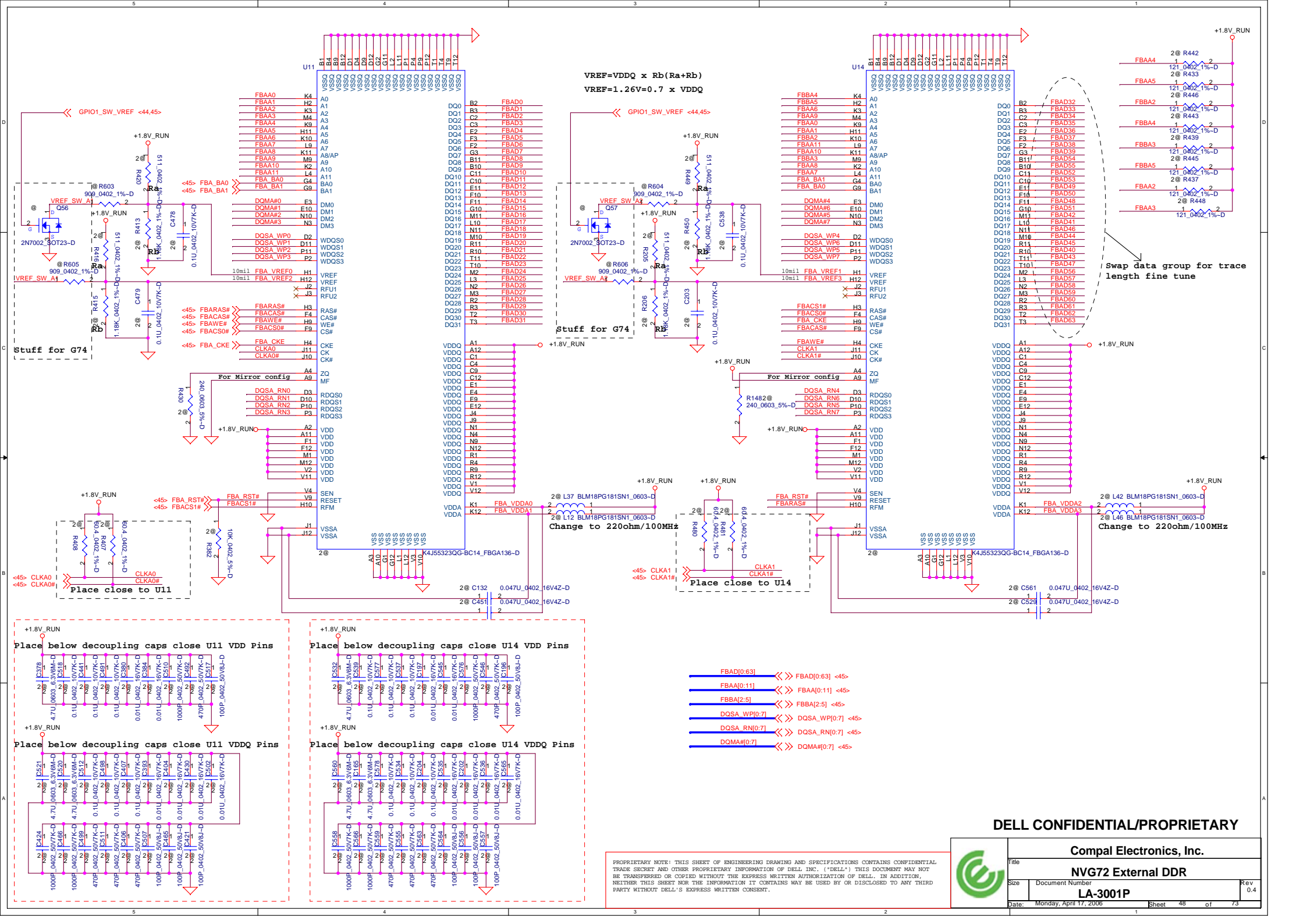
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Compal Electronics, Inc.

Title			NVG72 GND	
Size	Document Number		Rev	
	LA-3001P		0.4	
Date:	Monday, April 17, 2006		Sheet	47 of 73

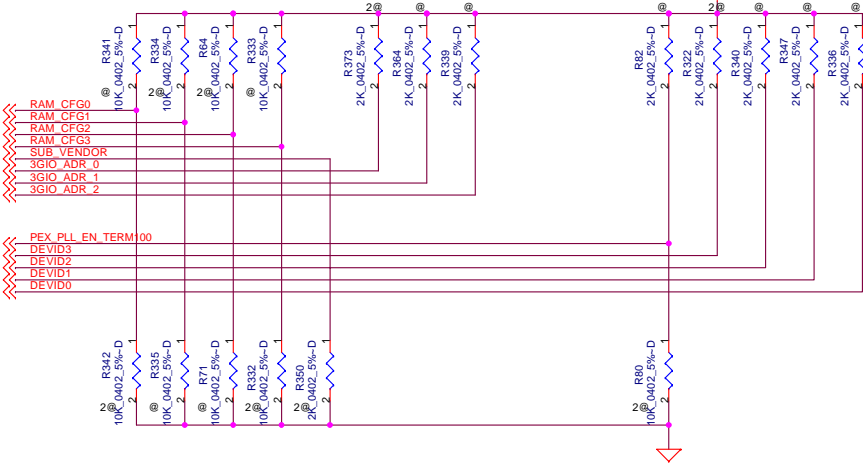


G72MV STRAPS

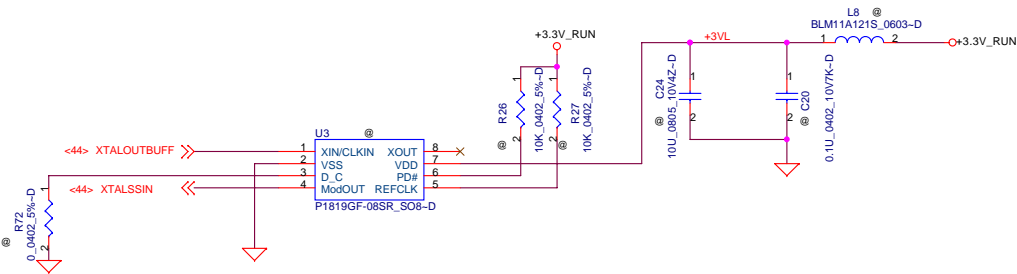
STRAPS	PIN	DESCRIPTION	Value
ROM_TYPE[1:0]	MIOBD10 MIOB_VSYNC	Parallel=00, SERIAL AT25F=01 DEFAULT, Serial SST45VF=10, LpC=11	01
SUB_VENDOR	MIOAD1	VBIOS on card (pull high) VBIOS with system BIOS (pull down)	0
PEX_PLL_TERM	MIOAD0		0
RAM_CFG[3:0]	MIOBD0 MIOBD1 MIOBD8 MIOBD9	8Mx32 DDR monolithic (64bit) 300MHz, 1.8V	0001
		8Mx32 DDR monolithic (32bit) 300MHz, 1.8V	1001
		8Mx32 DDR (Samsung K4D55323QF-GC) 300MHz, 1.8V	0010
		4Mx32 DDR generic (64bit) 1.8V I/O	0100
		4Mx32 DDR generic (32bit) 1.8V I/O	1100
	For GDDR3	Infineon 8Mx32 500MHz, 1.8V	0101
		Hynix 8Mx32 500MHz, 1.8V	0111
		Samsung 8Mx32 500MHz, 1.8V	0110
			*

<44> RAM_CFG0
<44> RAM_CFG1
<44> RAM_CFG2
<44> RAM_CFG3
<45> SUB_VENDOR
<45> 3GIO_ADR_0
<45> 3GIO_ADR_1
<45> 3GIO_ADR_2

<45> PEX_PLL_EN_TERM100
<44> DEVID3
<44> DEVID2
<44> DEVID1
<44> DEVID0



G72xx				
	DEVID3	DEVID2	DEVID1	DEVID0
G72GLM	1	1	0	0
G72M	1	0	0	0
G72MV	0	1	1	1



	U3.Pin3	Internal pull up
-1.75% (DOWN)	0	*
±0.875% (CENTER)	1	

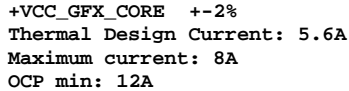
DELL CONFIDENTIAL/PROPRIETARY



Compal Electronics, Inc.		
Title NVG72 Strapping		
Size	Document Number	Rev
	LA-3001P	0.4
Date	Monday, April 17, 2006	Sheet 49 of 73

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Graphics Power for HAL31 Discrete only.



Populated PR159, PR160
if Page 33 R576, R577 are Unpop.

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Title	PWR_NVG72 +VDD_CORE
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Size	Document Number	Rev
	LA-3001P	X02
Date:	Monday, April 17, 2006	Sheet 50 of 73

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request	Owner Issue	Solution Description	Rev.
1	ALL	H/W	9/14	Bill	Revision change to X00(0.2)	Modify Done.	0.2
2	31	H/W	9/14	Bill	Update Board ID to 0001 for X00	Stuff R42 and no-stuff R31	0.2
3	31	H/W	9/14	Bill	CoE update. (EC_A05)	Add GPIO USB_CAM_EN# and ADAPT_TRIP_SEL	0.2
4	19	H/W	9/20	Bill	CoE update. (CRT, LVDS, SVIDEO and DVI Interfaces_A06)	Delete U28, R607. Add R610.	0.2
5	20	H/W	9/20	Bill	CoE update. (CRT, LVDS, SVIDEO and DVI Interfaces_A06)	Update Population Note for the RGB and TV out Filter.	0.2
6	32	H/W	9/23	Reden	CoE update. (M07 SYSTEM POWER SEQUENCE_A03)	Change R58,R540,R567,R447,R558,R564,R597 to 30_0805_5%	0.2
7	23	H/W	9/28	Reden	Update the ICH7 USB bus connection	Add connection of USB4+/- for CCD, USB2+/- for Blue tooth	0.2
8	ALL	H/W	9/28	Reden	Change Connector for ME request	Update J1394, JTP1, JBT1, JLVDS1 connector	0.2
9	14	H/W	9/30	Reden	Update the note for MCH power	Remove the placement note for C489,C525 as COE schematic	0.2
10	22	H/W	9/30	Scott	Pull-up on SATA_ACT# (R530) should be populated	Modify OK	0.2
11	22	H/W	9/30	Scott	Capacitor on THRMTRIP_ICH# (C609) can be de-populated	Modify OK	0.2
12	23	H/W	9/30	Scott	Rename net LCM_SMB_CLK to ICH_SMLINK0	Modify OK	0.2
13	23	H/W	9/30	Scott	Rename net LCM_SMB_DAT to ICH_SMLINK1	Modify OK	0.2
14	29	H/W	9/30	B.McFarland	Can remove R489 and R490. Leave pins 3 and 5 as NC on JMINI1. See A06 Ref Schem.	Modify OK	0.2
15	20	H/W	9/30	John Lerma	Please check the latest reference schematics. Delete 75 ohm resistors on RED, GREEN, & BLUE. Add 39 ohms series resistors to ouputs of U1 & U2. Move L3 & L4 before caps C1 & C2.	Delete R233, R235, R238, Add R611, R612 (39 Ohm). And move L3 & L4 before caps C1 & C2.	0.2
16	20	H/W	9/30	John Lerma	Please check the latest reference schematics. Delete 75 ohm resistors on TV_C, TV_CVBS, & TV_Y. Filter circuit values have been changes and a cap in parallel with each inductor has been added.	Remove R368, R380, R385.	0.2
17	33	H/W	9/30	John Lerma	Add diode for power leakage in power sequence circuit	Change R129,R482,R466 to 100K,and change Q6,Q30,Q27 to 2N3906,and change R471,R474,R469 to 4.7K.	0.2
18	23	H/W	9/30	Reden	No stuff R485 (10k pull high) for M'07 inverter	Modify OK	0.2
19	47	H/W	9/30	Reden	Change pull down resistor value to follow COW schematic	Change R602,R386 to 37.4_0402_1%	0.2
20	20	H/W	10/04	Reden	Change S-video filter bead same as COE schematic	Change L29,L32,L34 to 0.47UH_CIL10NR47KNC_10%_0603	0.2

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			Compal Electronics, Inc.	
			Changed-List History 1	
Size	Document Number		Rev	
	LA-3001P		0.3	
Date:	Monday, April 17, 2006		Sheet	51 of 73

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request	Owner	Issue Description	Solution Description	Rev.
1	29	H/W	10/05	John		Swap CLKREQ signal between WWAN and WLAN	Modify ok.	0.2
2	27	H/W	10/05	John		Change C236,C238 from 1000p to 300p	Modify ok.	0.2
3	29	H/W	10/05	John		Add debug signals to WLAN connector	Connecting JMINI2 pins 16 - HOST_DEBUG_TX, 17 - HOST_DEBUG_RX, 19 - 8051_TX & 42 - 8051_RX.	0.2
4	32	H/W	10/05	John		Remove C682 and replace C685 with 4700pF as COE schematic	Modify ok.	0.2
5	44	H/W	10/05	John		Add signal THERMTRIP_VGA# to G72 pin B13 from Guardian II	Modify ok.	0.2
6	49	H/W	10/05	John		Change R341, R334, R64, & R333 from 2K to 10K	Modify ok.	0.2
7	20	H/W	10/05	John		Change Caps C331,C325,C351,C349,C381,& C379 from 82pF to 47pF and add C705-C707	Modify ok.	0.2
8	44	H/W	10/05	John		Add 10K pull-down resistor to G72 pins C3, C1, & D7	Modify ok.	0.2
9	31	H/W	10/06	Reden		Add signal U18 pin5 (GPIOE4) connect to TP connector for LED.	Modify ok.	0.2
10	44	H/W	11/02	John		Add 150ohm terminal resistor on GFx side.	Add 150ohm of R619~R624	0.3
11	22	H/W	11/02	Reden		Add SNIFFER LED Disable Circuit as COE schematic	Add Q58,R625	0.3
12	30	H/W	11/02	Reden		Added 0 ohm to EC5004 test pin	Modify ok.	0.3
13	29	H/W	11/02	Reden		Added circuit to support WoW from S3/S4. Blocking diode and bypass resistor as COE	Modify ok.	0.3
14	35	H/W	11/02	Reden		Added a circuit (Transistor and Resistors) to keep BT LED off when the SNIFFER is turned on	Modify ok.	0.3
15	44	H/W	11/02	Reden		Change pull up resistor same as COE graphic schematic.	Change R370,R376 from 4.7K to 470K.	0.3
16	20	H/W	11/17	Reden		Change VCC_CRT Diode D11 to RB500 (rate Io=100mA).	Modify ok.	0.3
17	44	H/W	11/17	Reden		Add series resistor on signal of PLTRST_DELAY#.	Modify ok.	0.3
18	44	H/W	11/17	Reden		Add series resistor on signal of THERMTRIP_VGA#.	Modify ok.	0.3
19	33	H/W	11/18	Reden		Change Q6,Q27,Q30 to MMBT3906, and delete D19~D21(RB751V_SOD323~D) same as COE schematic.	Modify ok.	0.3
20								
21	32	H/W	11/18	Reden		Added 3VRUN Delay RC CKT, to fix IMVP_PWRGD Glitch issue and add 1.8 VRUN Delay RC CKT, to meet GFX Power Sequence Requirement	Modify ok.	0.3
22								
23								
24	32	H/W	11/18	Reden		Added Diode Bleed off for 3VRUN and 1.8VRUN for GFX Power Down Sequence adjustment.	Modify ok.	0.3
25	32	H/W	11/21	Reden		Change the GFX_RUN_ON connection to VR turn on pin as COE A06 version schematic.	Modify ok.	0.3
26	20	H/W	11/23	John		Change U19 connection from EC to GND as GG list request.	Modify ok.	0.3

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Compal Electronics, Inc.			
Title Changed-List History 2			
Size	Document Number		Rev
	LA-3001P		0.3
Date	Monday, April 17, 2006		Sheet 52 of 73

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	H/W	11/23	John	Change JTP1 pin 19 from +5V_ALW to +5V_RUN as Dell GG list	Modify ok.	0.3
2	20	H/W	11/23	John	Place a 0 ohm 1206 place holder between D11 pin 1 and JCRT1 pin 9	Modify ok.	0.3
3	29	H/W	11/23	John	Change WWAN USB source from EC to ICH7M/USB5 and remove WWLAN USB signal from EC.	Modify ok.	0.3
4	44	H/W	11/24	John	Add connection for signal of YPRPB_DET# to G72 pin A15 through a series resistor.	Modify ok.	0.3
5	44	H/W	12/01	John	Change R615 to no-pop	Modify ok.	0.3
6	23/31	H/W	12/02	John	Add connection to EC for signal HDDC_EN# and MODC_EN#	Modify ok.	0.3
7	6	H/W	12/06	Reden	Change R456 to 150, R457 to 91 for internal spectrum clock.	Modify ok.	0.3
8	20	H/W	12/07	John	Add a diode for U1,U2 power pin.	Modify ok.	0.3
9	20	H/W	12/07	John	Add a cap 0.1uf for JSVID1 pin5	Modify ok.	0.3
10	28	H/W	12/07	John	Change u13 to G5240B1T1U	Modify ok.	0.3
11	30	H/W	12/07	John	Add connection for pin73 for LVDS BIA_PWM through resistor	Modify ok.	0.3
12	20	H/W	12/08	John	Remove the C104 form dell COE team request.	Modify ok.	0.3
13	6/44/49	H/W	12/12	Reden	Remove external spectrum and swap populated resistor for internal CLK GEN.	Modify ok.	0.3
14	31	H/W	12/12	John	Add pull up resistors to +3.3V_ALW for signals of HDDC_EN#,MDDC_EN#	Modify ok.	0.3
15	23/30	H/W	12/13	John	Add damping series resistors (47ohm) for signal SPI_CS# on EC and ICH7	Modify ok.	0.3
16	33	H/W	12/13	John	Removed 3V/5V power good sequence circuit and change +1.8V_RUN PWRGD circuit.	Modify ok.	0.3
17	35	H/W	12/14	Reden	Swap the Sniffer LED (D13) pin define, Pin3=>Yellow, Pin2=>Green.	Modify ok.	0.3
18	9	H/W	12/14	Reden	Change CPU VCORE area caps , 22uF->10uF and replace 330uF poly with 6m ohm x 4pcs.	Modify ok.	0.3
19	31	H/W	12/15	Reden	Change pull up resistors of HDDC_EN#,MDDC_EN# from 10k to 100K for leakage issue.	Modify ok.	0.3
20	49	H/W	12/15	Reden	Change Device ID from 0111 to 1000 for G72M	Modify ok.	0.3
21	32	H/W	2006/2/07	Reden	Change C154 from 0.01uf to 0.047uf to match G72 VDD_CORE&1.8V power up sequence	Modify ok.	0.4
23	13	H/W	2006/2/07	Reden	Change L6/L26 TDK to 2nd and use Taiyo for main source	Modify ok.	0.4
24	24	H/W	2006/2/07	Reden	Change L53 TDK to 2nd and use Taiyo for main source	Modify ok.	0.4
25	20	H/W	2006/2/08	Reden	Change TV filter caps valus as dell's suggest 1. Change C331,C351,C381,C325,C349,C378 from 47pf to 82pf 2. Change C705,C706,C707 from 22pf to 8.2pf	Modify ok.	0.4

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		Compal Electronics, Inc.	
		Changed-List History 3	
Size	Document Number		Rev
	LA-3001P		0.3
Date	Monday, April 17, 2006		Sheet 53 of 73

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	35	H/W	02/17	Reden	To add logic circuit to control 3.3V_RUN for power switch board.	Modify ok.	0.4
2	35	H/W	02/17	Reden	Add pull down resistor (10K) for signal PLTRST_DELAY# to fix leakage issue	Modify ok.	0.4
3	19	H/W	02/21	Reden	Add SI3457DV P channel mos to dual-stuff for +GFX_PWR_SRC	Modify ok.	0.4
4	31	H/W	02/21	Reden	Change board ID to X02 (0011)	Modify ok.	0.4
5	19	H/W	02/21	Reden	Add voltage drop diode for CMOS power (+5V_RUN), and remove D'05 buffer.	Modify ok.	0.4
6	22, 23, 34	H/W	02/21	Reden	populate the 48MHz/bit_clk/keyboard signal termination for EMI issue	Modify ok.	0.4
7	19	H/W	02/21	Reden	Change population option for BACKLITEON,stuff R610 for DSC and stuff R639 for UMA.	Modify ok.	0.4
8	20	H/W	02/21	Reden	Change R611,R612 resistor to 0 for signal quality.	Modify ok.	0.4
9	23	H/W	02/22	Reden	Stuff R485 for Bits issue WI52653	Modify ok.	0.4
10	16	H/W	02/22	Reden	Change thermal setpoint from 85 degrees to 88 degrees, change R242 from 147K ohm to 322K ohm 1% and R247 from 41.2K ohm to 118K ohm 1%.	Modify ok.	0.4
11							
12	19	H/W	02/28	Reden	Add R652 overlap on D26 for CMOS power pop option	Modify ok.	0.4
13	31	H/W	04/03	Reden	Change board ID to X03 (0100)	Modify ok.	0.5
14	16	H/W	04/11	Reden	Switch Q7,Q24 Pin S,D connection	Modify ok.	0.5
15		H/W				Modify ok.	0.5
16		H/W				Modify ok.	0.5
17		H/W				Modify ok.	0.5
18		H/W				Modify ok.	0.5
19		H/W				Modify ok.	0.5
20		H/W				Modify ok.	0.5
21		H/W				Modify ok.	0.5
23		H/W				Modify ok.	0.5
24		H/W				Modify ok.	0.5
25		H/W				Modify ok.	0.5
26		H/W					

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		Compal Electronics, Inc.	
Title		Changed-List History 4	
Size	Document Number		Rev
	LA-3001P		0.3
Date	Monday, April 17, 2006		Sheet 54 of 73

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Version Change List (P. I. R. List)for Power Circuit



Item	Page#	Title	Date	Request Owner	Issue Description	Solution Descr
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1	P39	+3.3VALW	0926/2005	Dell	Dell request to change PC30 from 4.7U_1206 to 10U_1206	PC30 change to 10U_1206_10V	X00
2	P40	+1.5V / +1.05V OCP	0926/2005	Dell	+1.5V OCP min = 7.4A, +1.05V OCP min = 9.3A	1.) +1.5V OCP: PR56 change to 124K, PR46 change to 1.43K 2.) +1.05V OCP: PR57 change to 124K, PR47 change to 1.87K	X00
3	P41	+1.8V_SUS	0926/2005	Dell	Contact the FB pin of the controller to the AVDD pin via zero ohm resister	Add PR202 0 ohm 0603 between FB pin with AVDD pin of PU5 MAX8632	X00
4	P39	+15V_SUS	0926/2005	Compal	Follows COE +15V reference schematics	Unpop PR179 10K_0805	X00
5	P50	+VCC_GFX	0926/2005	Compal	Improve +1.22V_GFX_PCIEP pin7 STBY# and pin5 POK1 pull high resister of PU13 MAX8632.	Depop PR159, PR160 100K_0402	X00
6	P40	+1.5V / +1.05V	1004/2005	Dell	Improve better phase margin	PC46 change to 330pf/0402/50v	X00
7	P41	+1.8V_SUSP OCP	1004/2005	Dell	Improve 1.8V_SUSP OCP	PR78 change to 84.5K	X00
8	P39	+3.3VALW	1004/2005	Dell	Dell request to populate PC11 at the input to the 3V regulator	Populate PC11 10uf/1206/25V	X00
9	P50	+VCC_GFX	1007/2005	Dell	Dell request to Change PR167 pin 1 contact to +3.3V_RUN	PR167 pin1 contact to +3.3V_RUN	X00
10	P50 P41	+VCC_GFX +1.8V_SUSP	1007/2005	Dell	MAX8632 Just connect pin 24 directly to the exposed pad without using zero ohm resistor .	DEL PR186 and PR79	X00
12	P41	+1.8V_SUSP	1007/2005	Dell	Dell request to populate PR74. (PU5 MAX8632 f from 300K change to 450khz)	Add PR74	X00
13	P43	Charger	1007/2005	Dell	Dell request to change PR174 to 1_0603.	PR174 from 1_0805 change to 1_0603(refer to COE Rev A09)	X00
14							
15	P41	+1.8V_SUSP	1107/2005	Dell	Dell Coe DDR Rev A05 request to del PR70	DEL PR70 Change PR69 from 0 ohm to 1 ohm.	X01
16	P43	Charger	1107/2005	Dell	Dell Coe Cgarger Rev A07 requested	1. Change PR174 from 1_0805 to 1_0603. 2. Add PC175 220P_0402 3. Del PR200, Add PR199 100_0402, PC189 0.01U_0603 PU10 Pin 15 & Pin16 shorted. 4. Add PR144 4.3M 0402. 5. Del PR201. 6. Change PR149 from 59K to 56.2K 0402 7. Change PR150 from 33.2K to 27.4K 0402.	X01

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Power-Changed-List History			
Title	Document Number	Rev	
Bali		X01	
Date:	Monday, April 17, 2006	Sheet	55 of 73


Version Change List (P. I. R. List) for

Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description
17	P50	+VDD_CORE	1108/2005	Dell	Dell COE Graphics Power reference A07 requested	1. Change PR155 to 1 ohm. 2. Change PR161 from 69.8K to 57.6K. 3. Change PR164 from 118K to 178K. 4. Change PR166 from 301 to 0 ohm. 5. Change PR162 from 1.1K to 1.21K 6. All +5V_RUN change to +5V_SUS. 7. All +3V_RUN change to +3V_SUS.
18	P50	+VDD_CORE	1108/2005	Dell	Follow Coe ref De-pop PR203. Del PR204, H/W has same R632 100k on Page 32 between +3.3V_RUN to PU13 Pin_27.	Del PR203 Del PR204
19	P37	+DC_IN	1202/2005	Dell	Add solder jumper pads in parallel with PL2 & PL3.	Add PJP21, PJP22
20	P43	Charger	1120/2005	Dell	Dell COE Charger reference A09 requested	De pop PC189 Add PC191
21	P42	+VCC_CORE	1120/2005	Compal	Improve VCC-CORE OCP to 55A. (original design X00 PR109 191K OCP point 45A only.)	Change PR109 to 160K
22	P37 P38 P39 P40 P41 P42 P43 P50	EMI Bead	1122/2005	Compal	Change Footprint 'L_1812' to 'L-1812-S' for 2nd source	Change PL2, PL5, PL6, PL9, PL12, PL14, PL19, PL21 footprint to L_1812-S for 2nd source
23	P39	3.3VSRRC	1124/2005	Dell	Nopop PQ39 since this will not be needed once the EC HUB is removed.	Unpop PQ39
24	P42	+VCC_CORE	1130/2005	Compal	Tokin inductor 0.45uH/27A rusted on surface after storage test.	change PL15, PL16, PL17 to Panasonic ETQP4LR45XFC (0.45uH 10% Lead Free)
25	P50	+VDD_CORE	1201/2005	Dell	Improve +3.3V_RUN leakage at S3 mode	1. Change PR167 Pin_1 net name from +3.3V_SUS change to +3.3V_RUN 2. Change PR159, PR160 Pin_1 net name from +3.3V_SUS change to +3.3V_RUN
26	P43	Charger	1201/2005	Dell	CoE Charger Ref A10 request: Deeply discharged battery problem.	Add PR208, PD20
27	P50	+VDD_CORE	1202/2005	Dell	Change PR167 to 4.7K to fix stair step issue seen on signal.	Change PR167 to 4.7K
28	P40	+1.5V_RUN	1202/2005	Dell	Add PC192 0.1uF cap to pin 21 of PU4 for power-up sequencing. Also add PD20 diode in parallel with PR59 for power-down sequencing.	Add PC192, PD21
29	P37	DC_IN	1206/2005	Dell	ChangePR9 from 4.7K to 10K. The existing 4.7K exceeds power dissipation rating of 0603 size at 20V.	Change PR9 from 4.7K to 10K
30	P43	Charger	1206/2005	Dell	Unpop PQ27, PR126	Unpop PQ27, PR126
31	P44	+15VP	1206/2005	Dell	Add a PR209 150 ohm between PD19 Pin_3 and PD18 Pin_2 to prevent +15V_SUSP short cause PD18 damage.	Add PR209 150 ohm



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Power-Changed-List History

Date: Monday, April 17, 2006

Sheet 56 of 73

Title	Bali		
Size	Document Number	Rev	X01

Request Owner

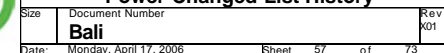
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Issue

~~Description~~

Solution

~~Description~~



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