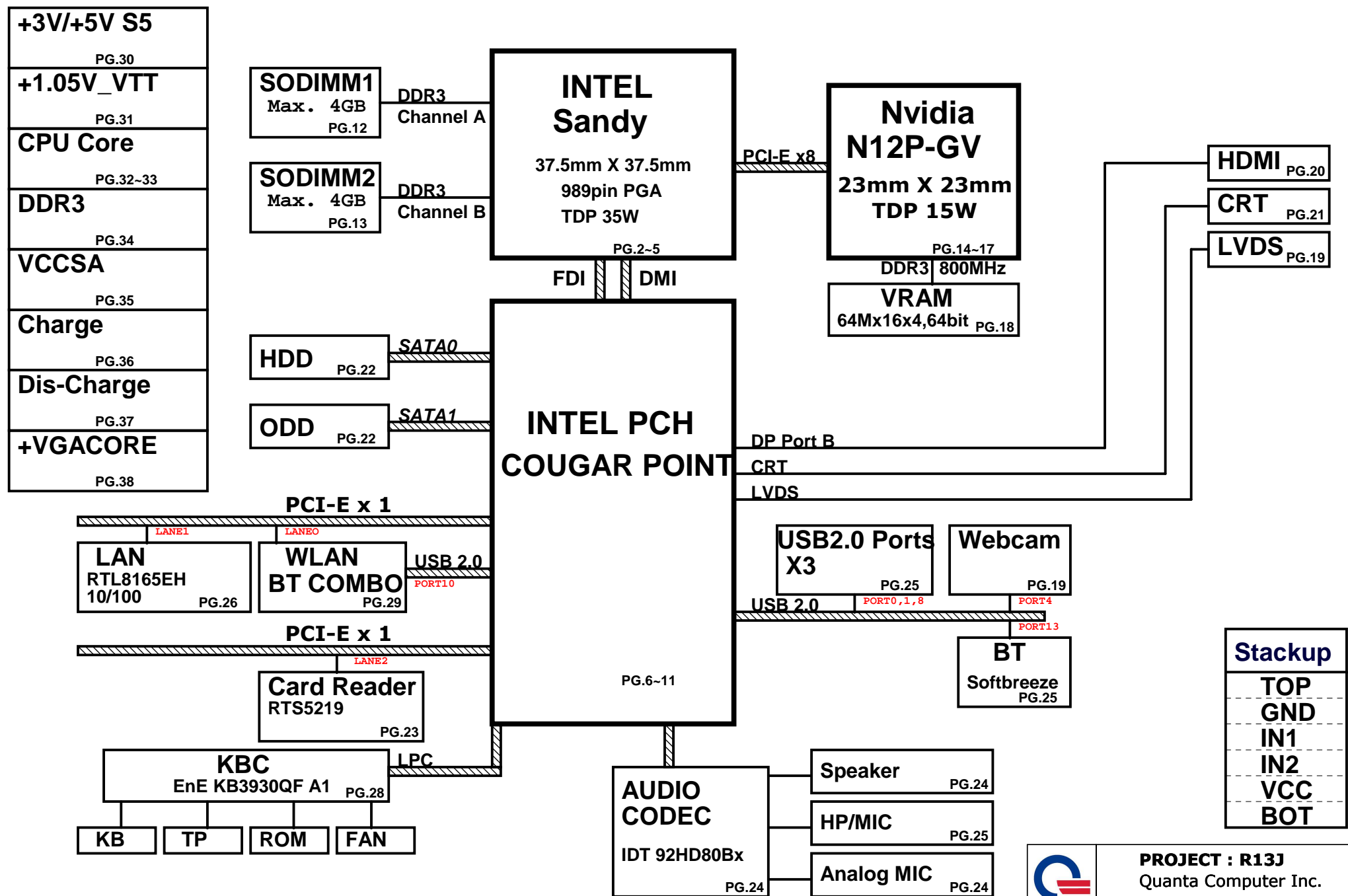


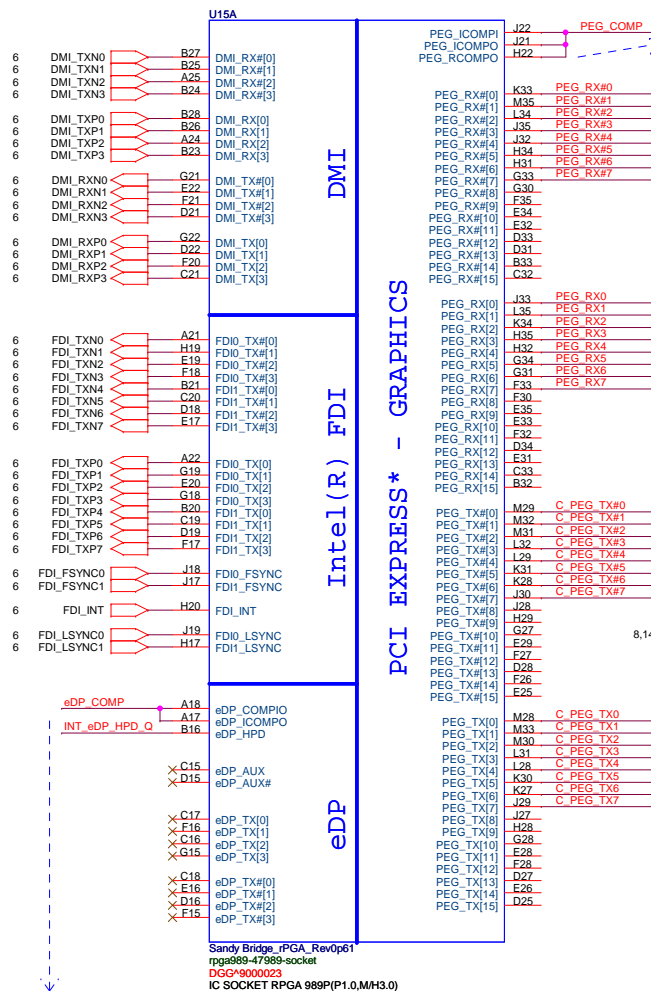
# R13J INTEL UMA/DISCRETE SYSTEM DIAGRAM

01



**PROJECT : R13J**  
Quanta Computer Inc.

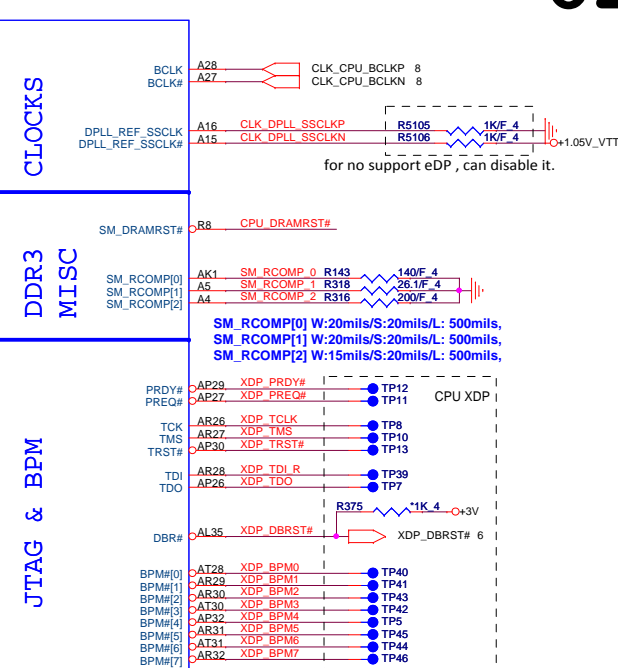
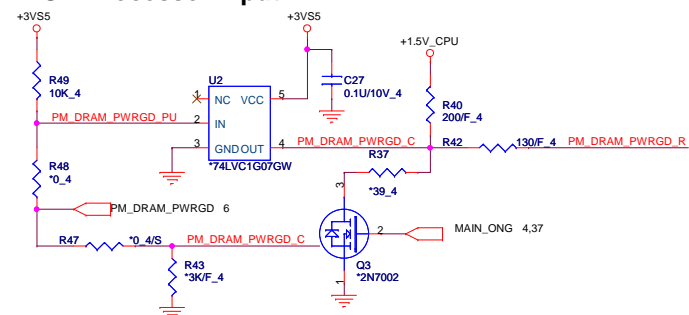
Size Custom Document Number BLOCK DIAGRAM Rev 1A  
Date: Wednesday, September 28, 2011 Sheet 1 of 38



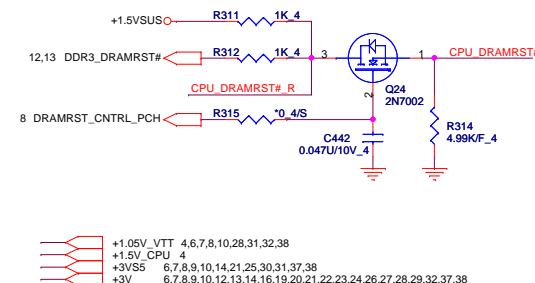
eDP\_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.  
eDP\_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.



**SM DRAMPWROK Processor Input.**



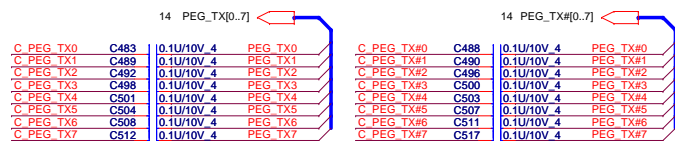
## DDR3 DRAM RESET



**FDI disable  
(DIS only stuff)**

FDI\_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

**PEG x16 disable (UMA only remove)**



0.22uF AC coupling Caps for PCIE GEN1/2/3

0.22uF AC coupling Caps for PCIE GEN1/2/3

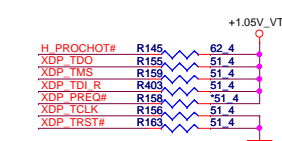
## DP & PEG Compensation

+1.05V\_VTTO R67 10K 4 INT\_eDP\_HPDP Q

eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG\_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms  
PEG\_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

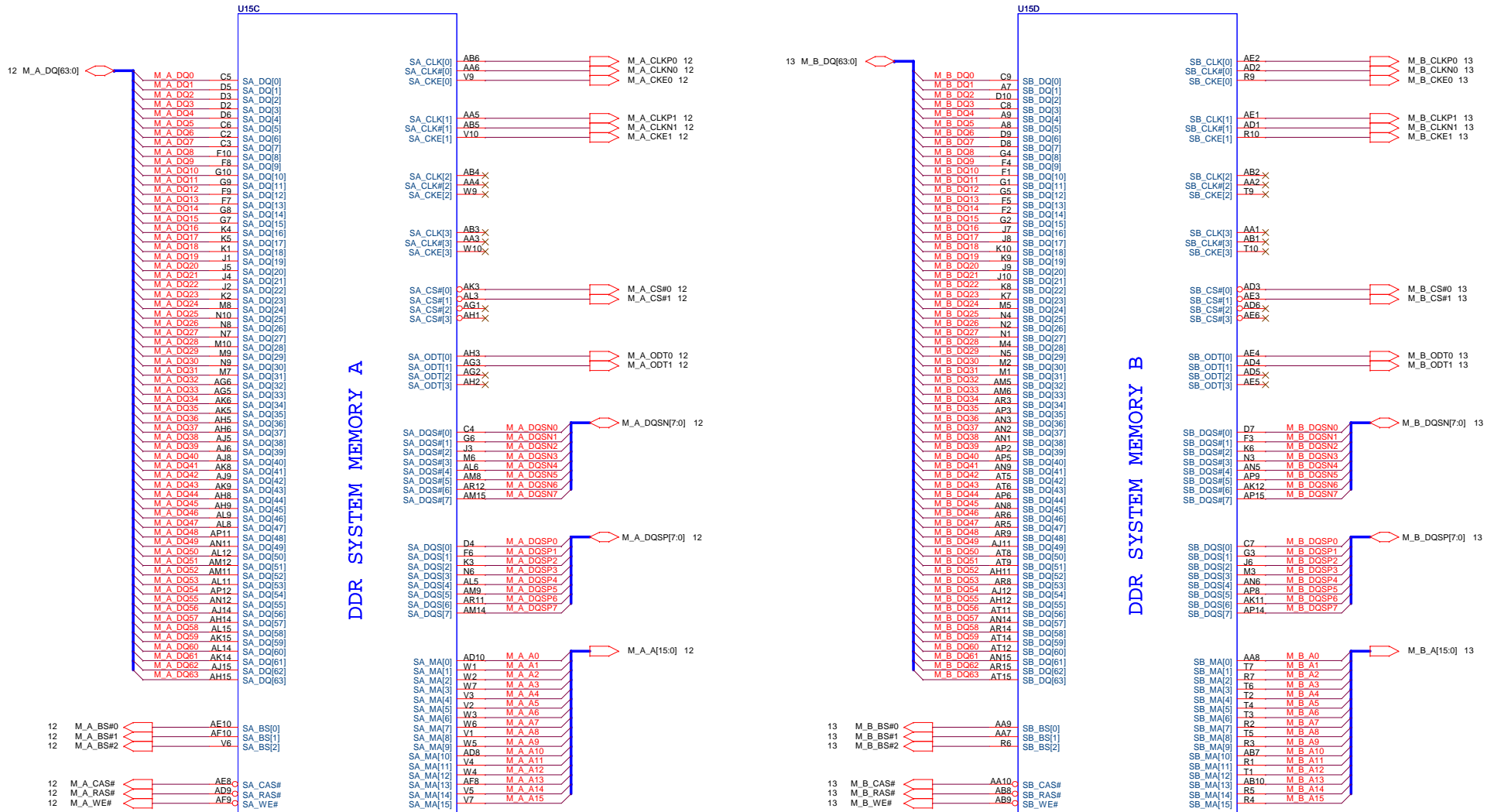
### Processor pull-up (CPU)



**PROJECT : R13J**  
Quanta Computer Inc.

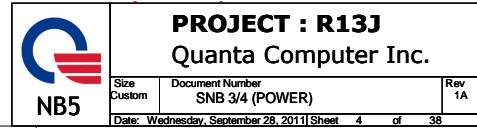
Size Custom	Document Number <b>SNB 1/4 (PCIE&amp;DMI&amp;FDI)</b>	Rev 1A
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## Sandy Bridge Processor (DDR3)



Sandy Bridge\_rPGA\_Rev0p61  
rpg989-47989-socket  
DGG-9000023  
IC SOCKET RPGA 989P(P1.0,M/H3.0)

Sandy Bridge\_rPGA\_Rev0p61  
rpg989-47989-socket  
DGG-9000023  
IC SOCKET RPGA 989P(P1.0,M/H3.0)



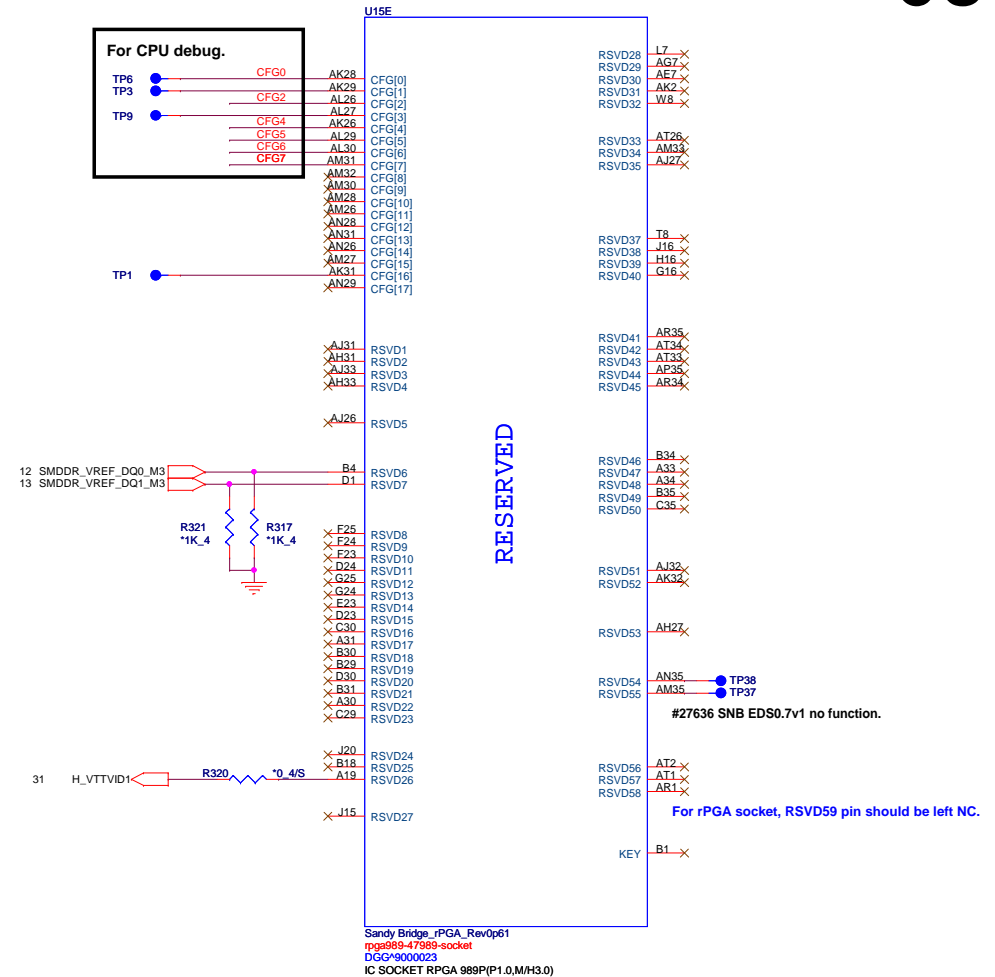
## Sandy Bridge Processor (GND)



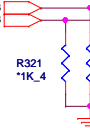
Sandy Bridge\_rPGA\_Rev0p61  
rpg989-47989-socket  
DGG\*9000023  
IC SOCKET RPGA 989P(P1.0,M/H3.0)

Sandy Bridge\_rPGA\_Rev0p61  
rpg989-47989-socket  
DGG\*9000023  
IC SOCKET RPGA 989P(P1.0,M/H3.0)

## Sandy Bridge Processor (RESERVED, CFG)



12 SMDDR\_VREF\_DQ0\_M3  
13 SMDDR\_VREF\_DQ1\_M3



31 H\_VTTVID1



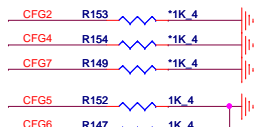
**CFG[6:5] (PCIe Port Bifurcation Straps)**

11: (Default) x16 - Device 1 functions 1 and 2 disabled  
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled  
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)  
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

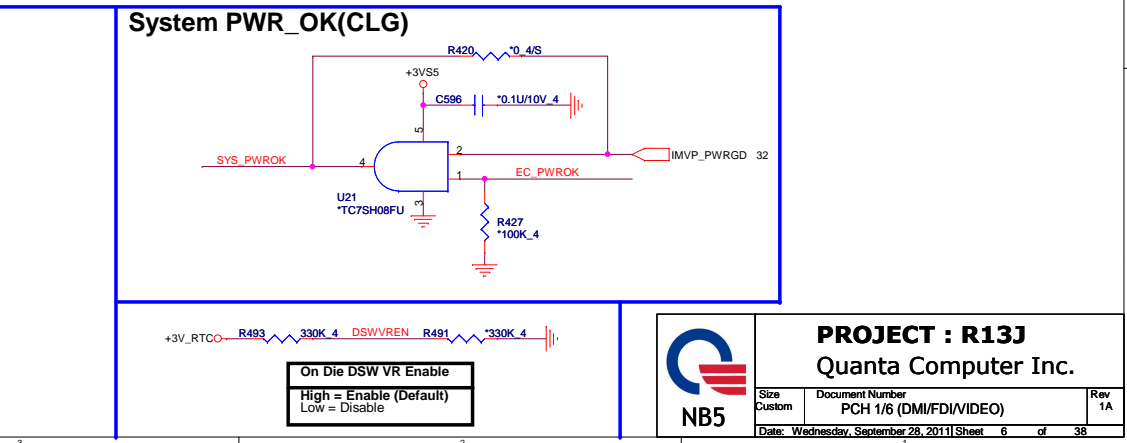
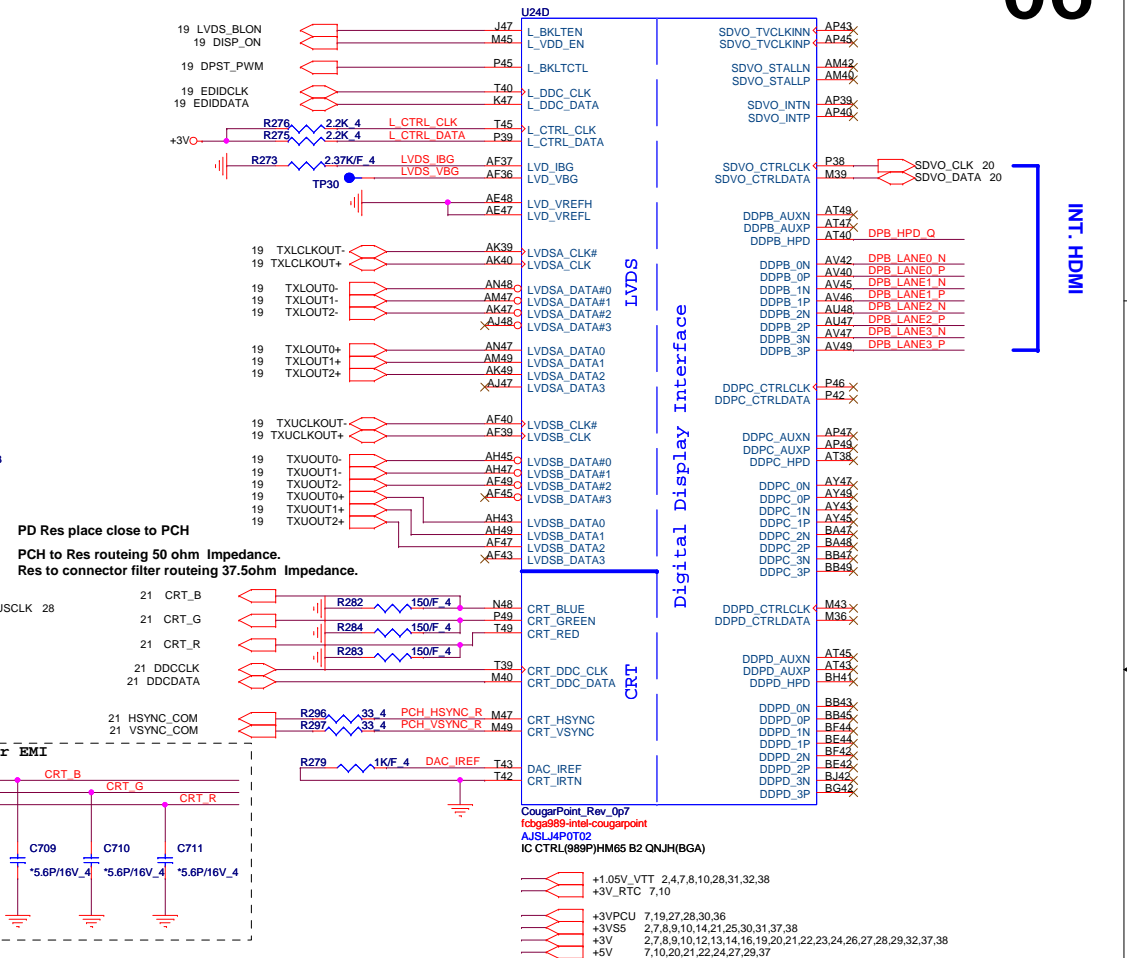
	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

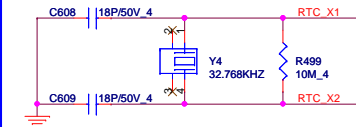


**PROJECT : R13J**  
Quanta Computer Inc.

Size Custom	Document Number SNB 4/4 (GND)	Rev 1A
Date: Wednesday, September 28, 2011 Sheet 5 of 38		



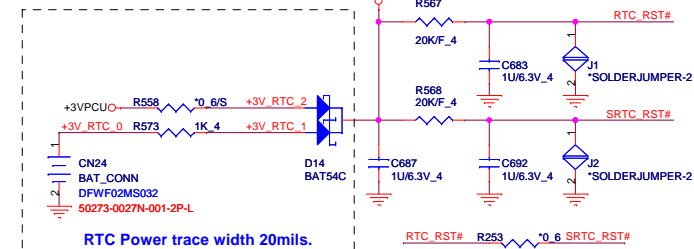




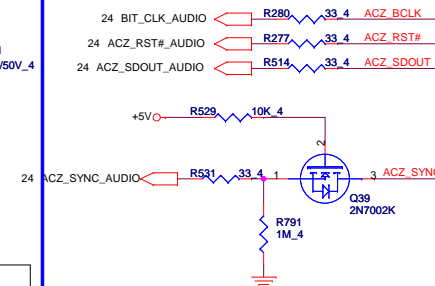
HDD0 (SATA3 6.0Gb/s)

ODD (SATA1 1.5Gb/s)

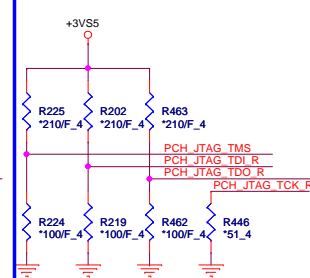
DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.



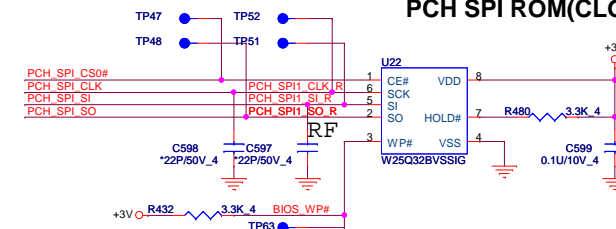
## HDA Bus(CLG)



## PCH JTAG Debug(CLG)



## PCH SPI ROM(CLG)



Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG
Socket		DG008000031

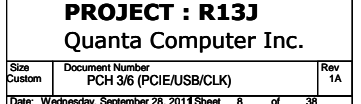


**PROJECT : R13J**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A
Date: Wednesday, September 28, 2011   Sheet 7 of 38		

### PCH Strap Table

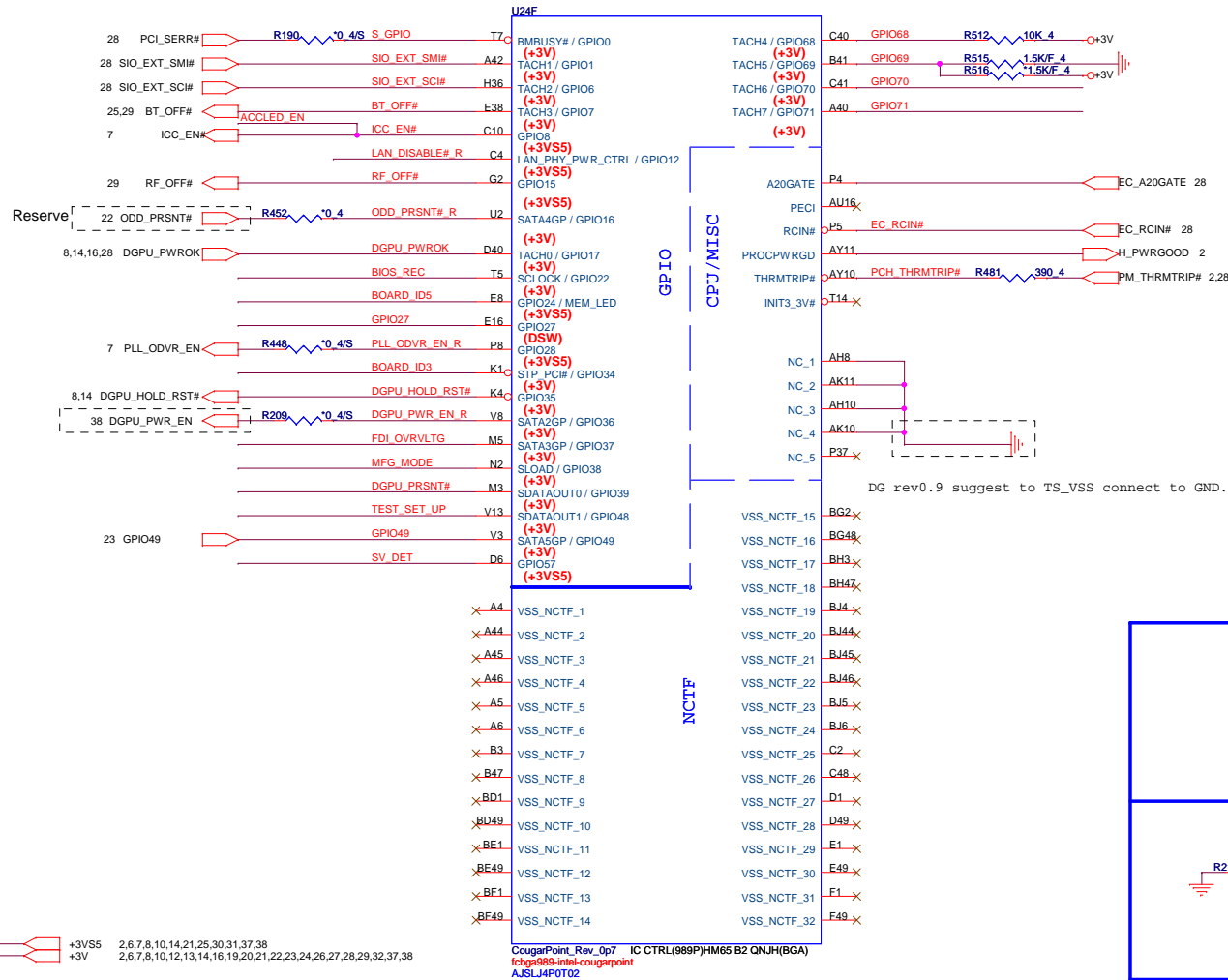
Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR <div>Different from Calpella</div>	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>SPI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table>	GNT1#	GNT0#	Boot Location	1	1	SPI	0	0	LPC	(Need external pull-down for LPC BIOS) Default weak pull-up on GNT0/1#
GNT1#	GNT0#	Boot Location											
1	1	SPI											
0	0	LPC											
GPIO19 <div>Different from Calpella</div>	Boot BIOS Selection 0 [bit-0]	PWROK											
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)										
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
GPIO28 <div>Different from Calpella</div>	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										



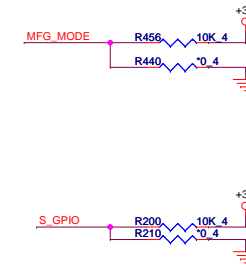


## Cougar Point (GPIO,VSS\_NCTF,RSVD)

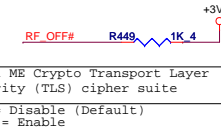
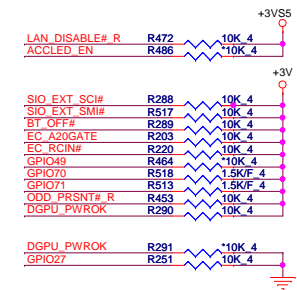
## Clock Gen Power OK (CLG)



## MFG-TEST

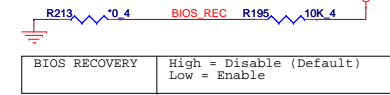


## GPIO Pull-up/Pull-down(CLG)



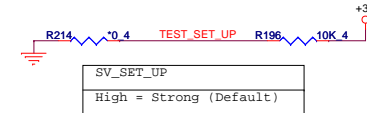
Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)  
High = Enable



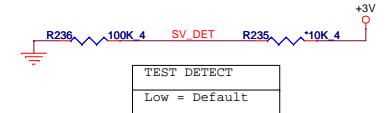
BIOS RECOVERY

High = Disable (Default)  
Low = Enable



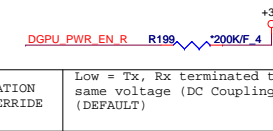
SV\_SET\_UP

High = Strong (Default)



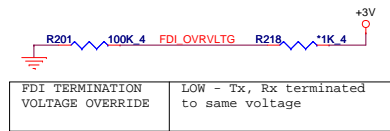
TEST DETECT

Low = Default



DMI TERMINATION VOLTAGE OVERRIDE

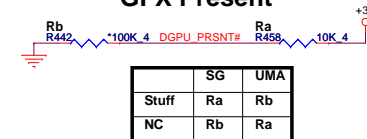
Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)



FDI TERMINATION VOLTAGE OVERRIDE

LOW - Tx, Rx terminated to same voltage

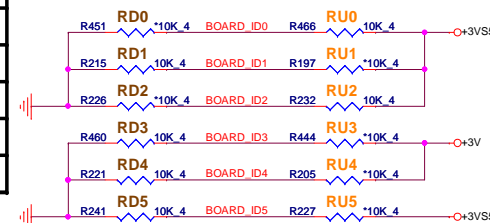
## GFX Present



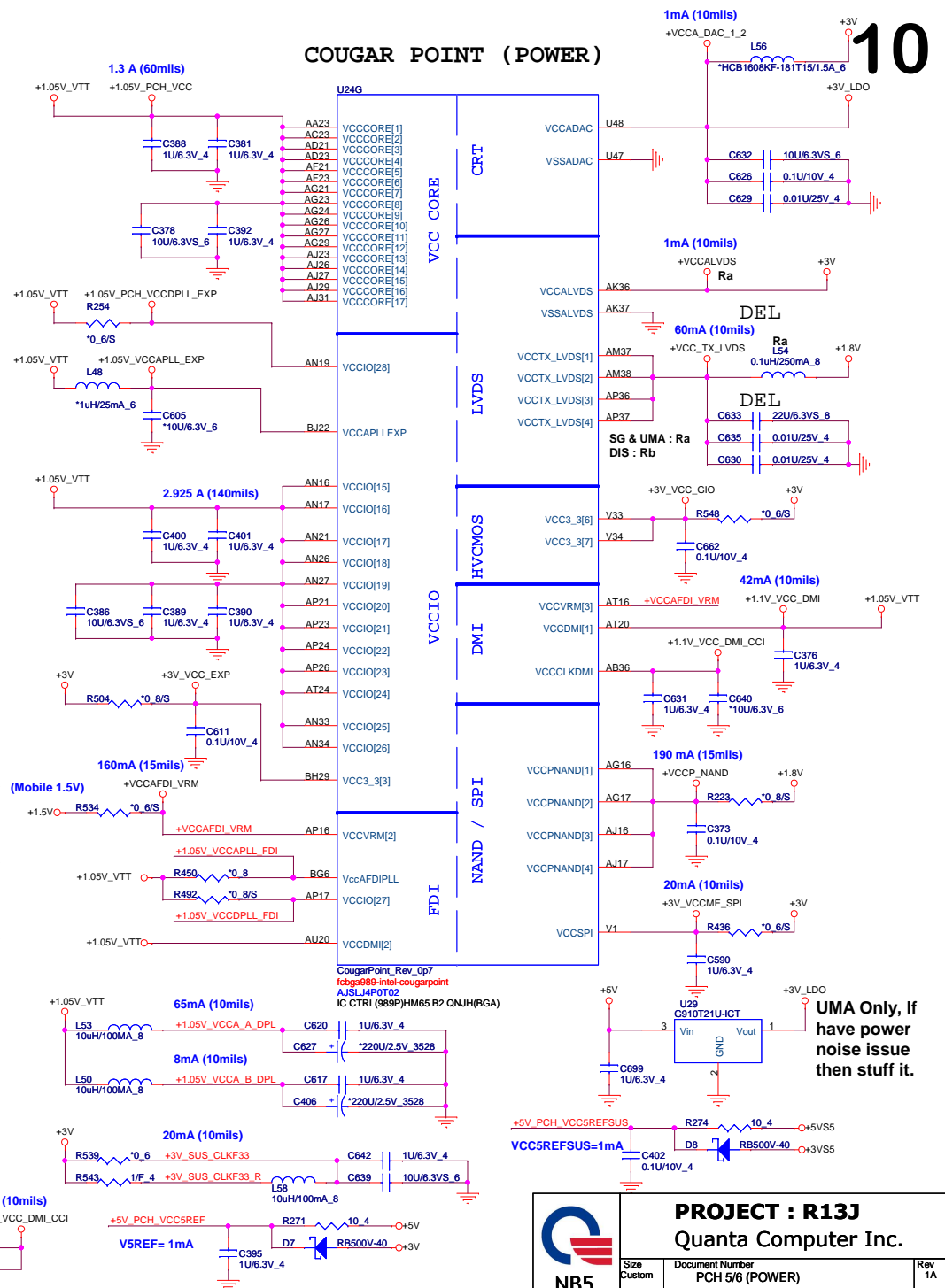
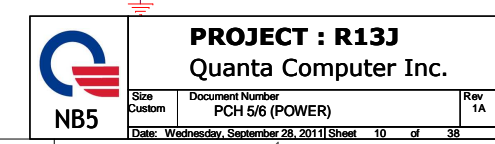
SG	UMA
Stuff	Ra
NC	Rb

## BOARD ID SETTING

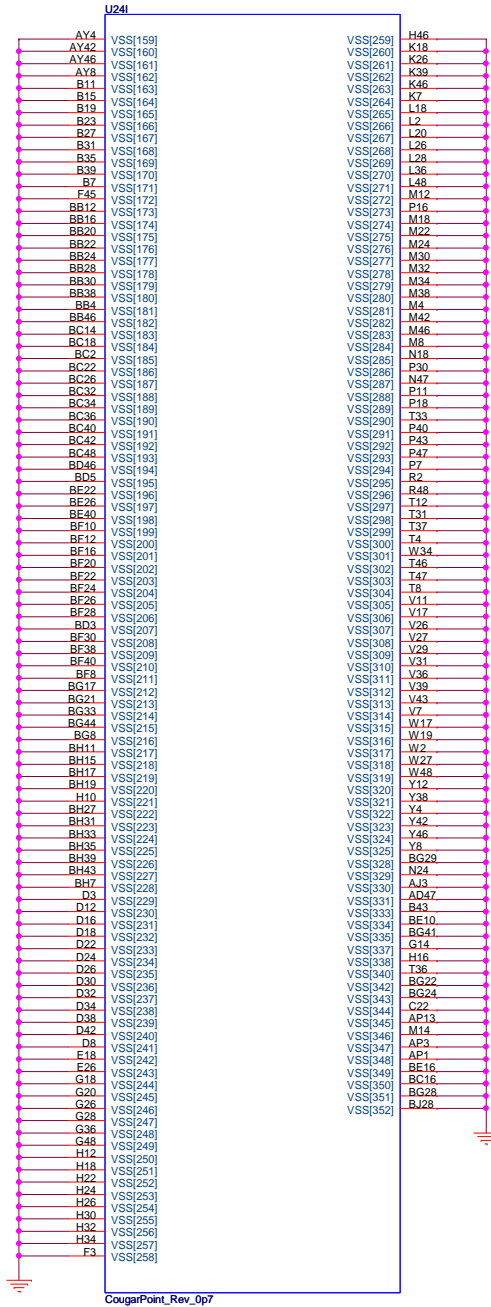
Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
R13 UMA	0	0	0	0	0	0
R13 DIS	0	0	0	0	0	1
R13 (1.1) DIS (AMD)	0	0	0	0	1	1
R13J (1.3) DIS (NVIDIA)	0	0	0	1	0	1
	0	0	0	0	0	0



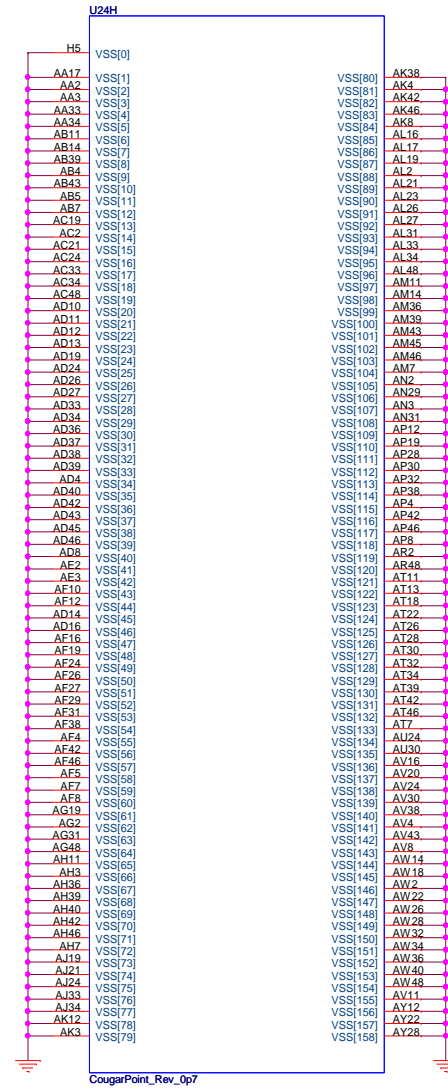
3V 10

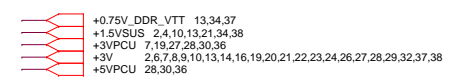


## IBEX PEAK-M (GND)

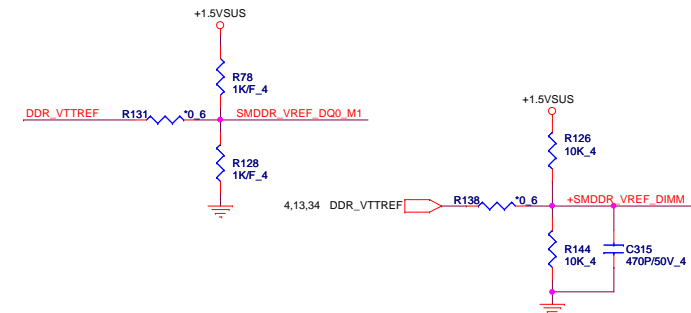


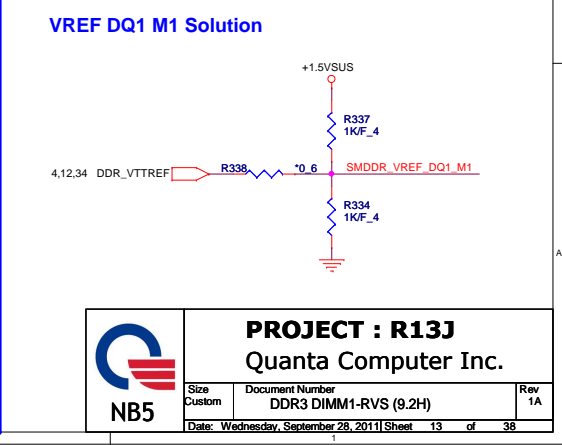
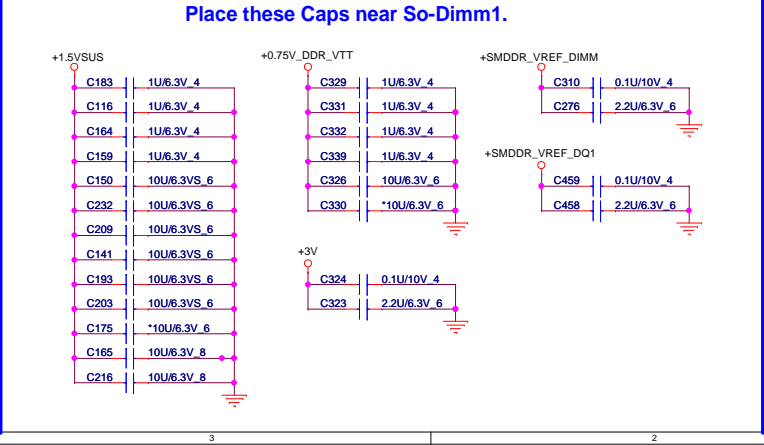
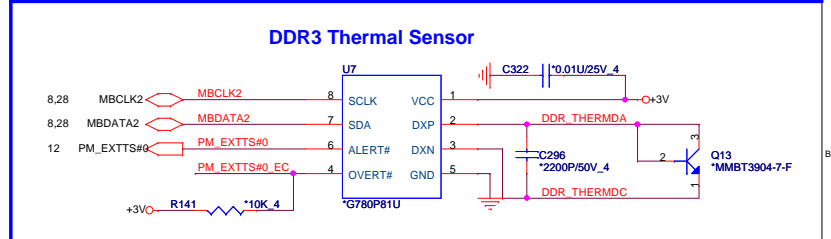
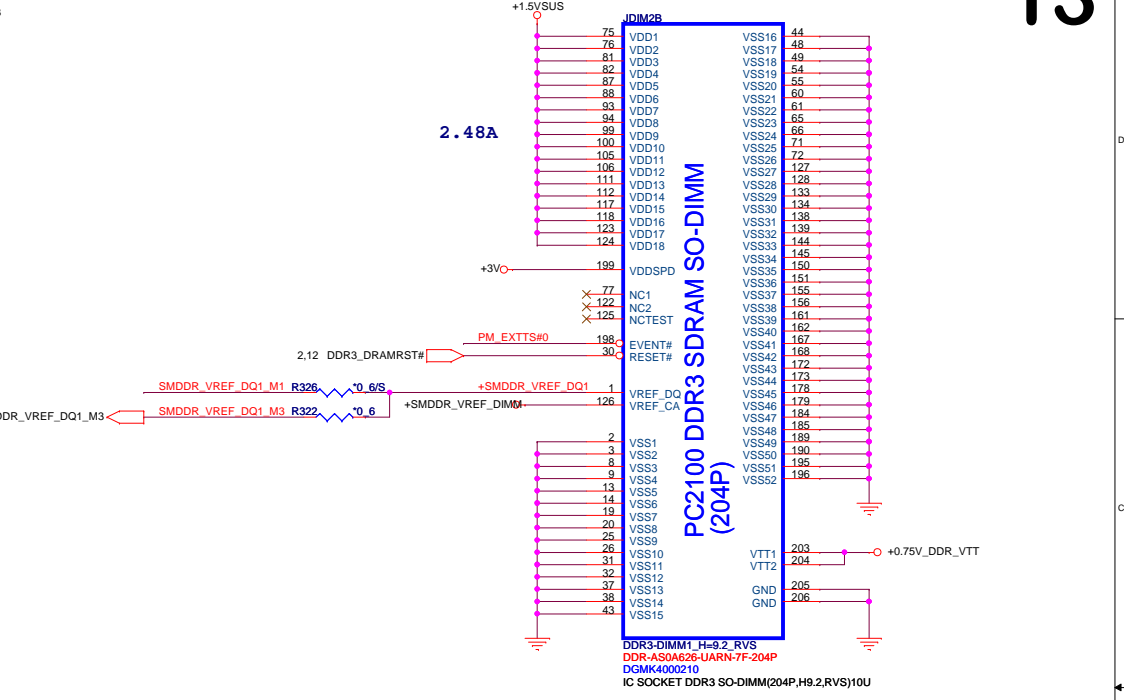
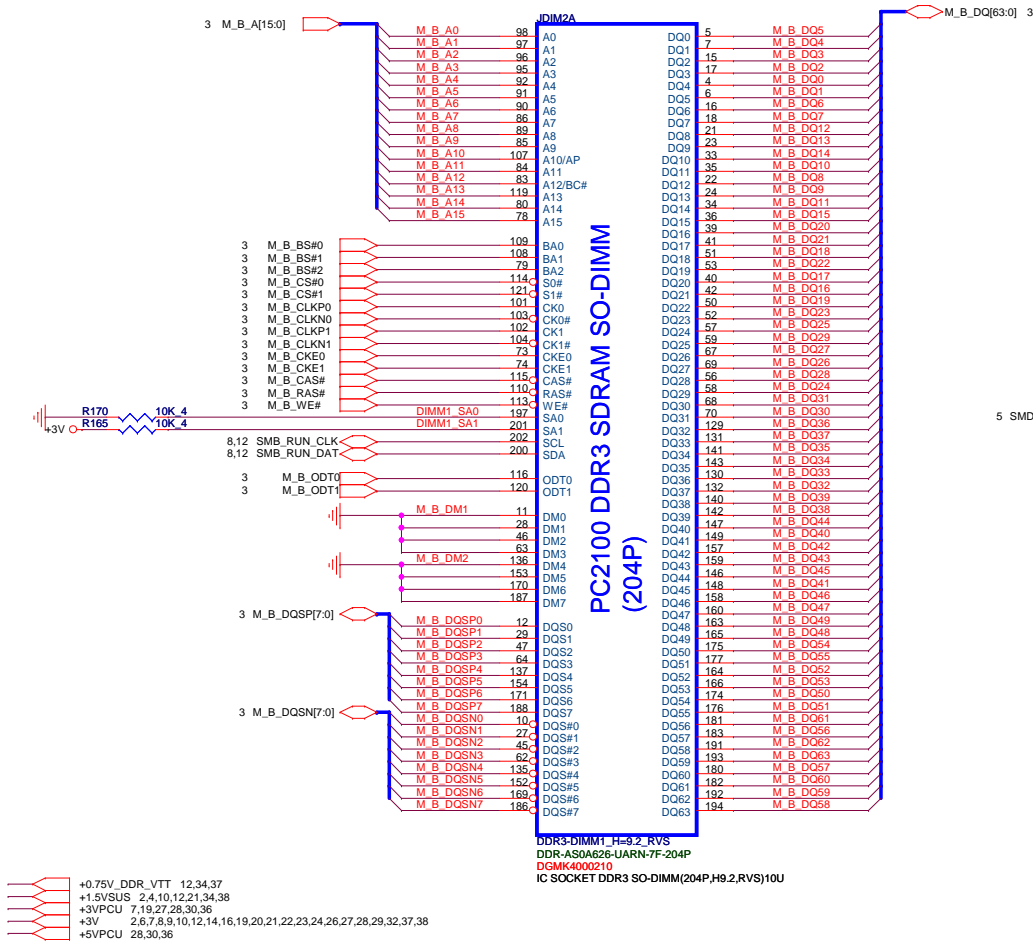
## IBEX PEAK-M (GND)





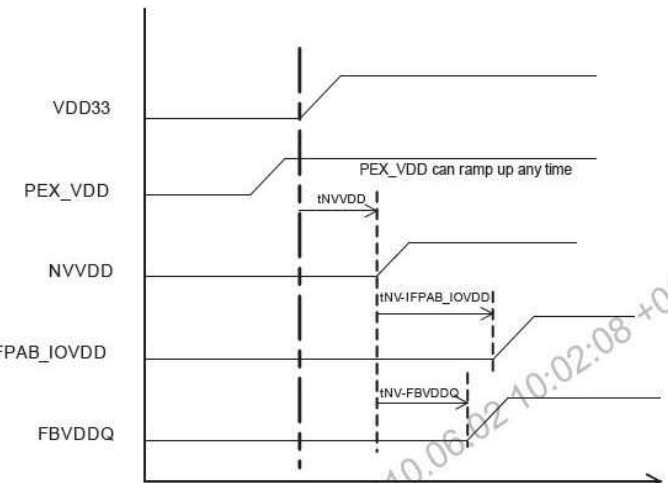
### VREF DQ0 M1 Solution



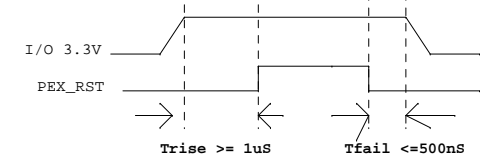




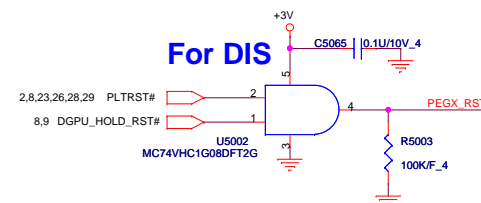
## power up sequence



## PEX\_RST timing

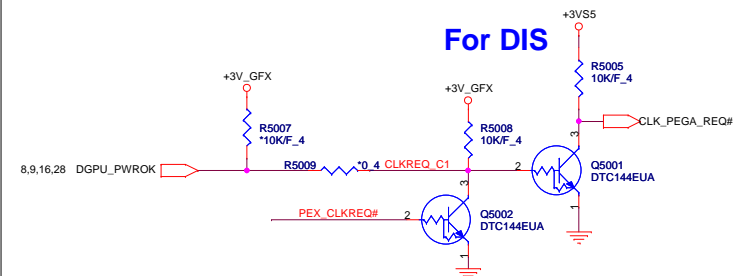


## For DIS



12/28 Nvidia to suggest R5009 not stuff and R5008 and Q5002 stuff.

## For DIS



**PROJECT : R13J**  
Quanta Computer Inc.

Size Custom Document Number N11M-GE2(PCIE/F) Rev 1A  
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2.16A

+1.5V\_GFX

U5001B

PBGA533-NVIDIA-GEFORCE6250  
N10M

2/13 FRAME\_BUFFER

18 VMA\_DQ[3..0]  
18 VMA\_DM[7..0]  
18 VMA\_WDQS[7..0]  
18 VMA\_RDQS[7..0]

U50011

PBGA533-NVIDIA-GEFORCE6250  
N10M

13/13 GND\_NC

nVIDIA comment 8/18

FBA\_CMD0 R5012 10K/F 4  
FBA\_CMD3 R5010 10K/F 4  
FBA\_CMD16 R5013 10K/F 4  
FBA\_CMD19 R5014 10K/F 4  
FBA\_CMD20 R5015 10K/F 4

FBA\_CMD0

FBA\_CMD1

FBA\_CMD2

FBA\_CMD3

FBA\_CMD4

FBA\_CMD5

FBA\_CMD6

FBA\_CMD7

FBA\_CMD8

FBA\_CMD9

FBA\_CMD10

FBA\_CMD11

FBA\_CMD12

FBA\_CMD13

FBA\_CMD14

FBA\_CMD15

FBA\_CMD16

FBA\_CMD17

FBA\_CMD18

FBA\_CMD19

FBA\_CMD20

FBA\_CMD21

FBA\_CMD22

FBA\_CMD23

FBA\_CMD24

FBA\_CMD25

FBA\_CMD26

FBA\_CMD27

FBA\_CMD28

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FBA\_CMD225

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FBA\_CMD227

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FBA\_CMD250

FBA\_CMD251

FBA\_CMD252

FBA\_CMD253

FBA\_CMD254

FBA\_CMD255

FBA\_CMD256

FBA\_CMD257

FBA\_CMD258

FBA\_CMD259

FBA\_CMD260

FBA\_CMD261

FBA\_CMD262

FBA\_CMD263

FBA\_CMD264

FBA\_CMD265

FBA\_CMD266

FBA\_CMD267

FBA\_CMD268

FBA\_CMD269

FBA\_CMD270

FBA\_CMD271

FBA\_CMD272

FBA\_CMD273

FBA\_CMD274

FBA\_CMD275

FBA\_CMD276

FBA\_CMD277

FBA\_CMD278

FBA\_CMD279

FBA\_CMD280

FBA\_CMD281

FBA\_CMD282

FBA\_CMD283

FBA\_CMD284

FBA\_CMD285

FBA\_CMD286

FBA\_CMD287

FBA\_CMD288

FBA\_CMD289

FBA\_CMD290

FBA\_CMD291

FBA\_CMD292

FBA\_CMD293

FBA\_CMD294

FBA\_CMD295

FBA\_CMD296

FBA\_CMD297

FBA\_CMD298

FBA\_CMD299

FBA\_CMD300

FBA\_CMD301

FBA\_CMD302

FBA\_CMD303

FBA\_CMD304

FBA\_CMD305

FBA\_CMD306

FBA\_CMD307

FBA\_CMD308

FBA\_CMD309

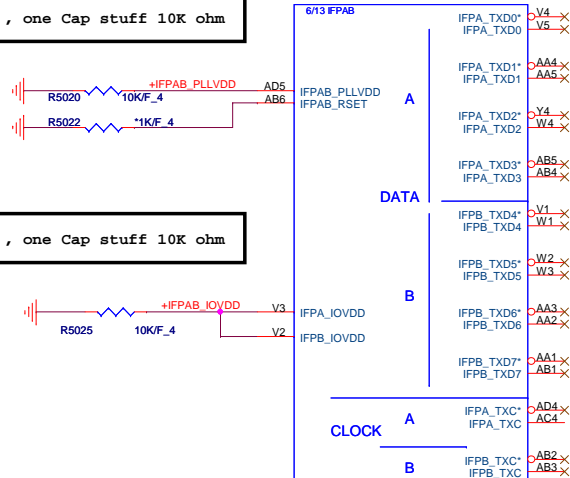
FBA\_CMD310

FBA\_CMD311

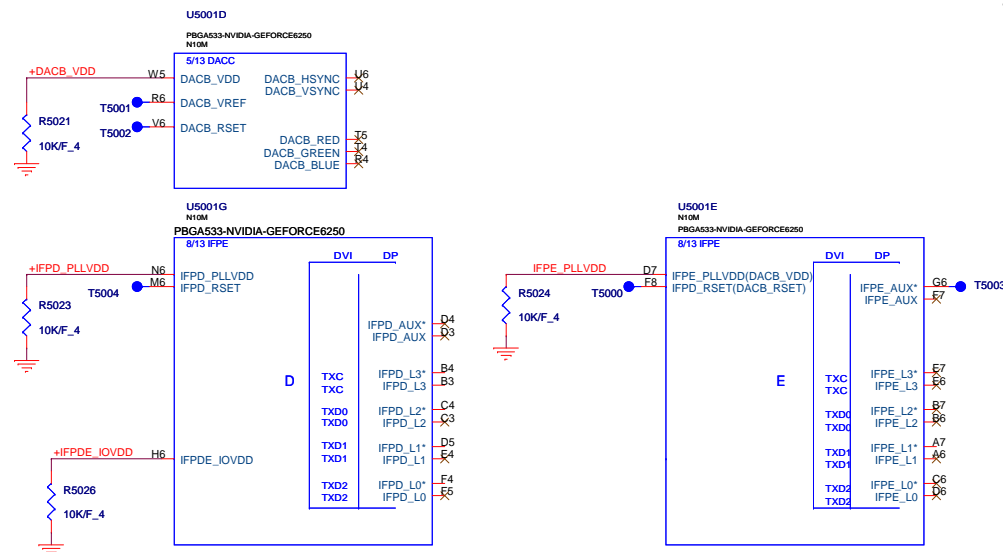
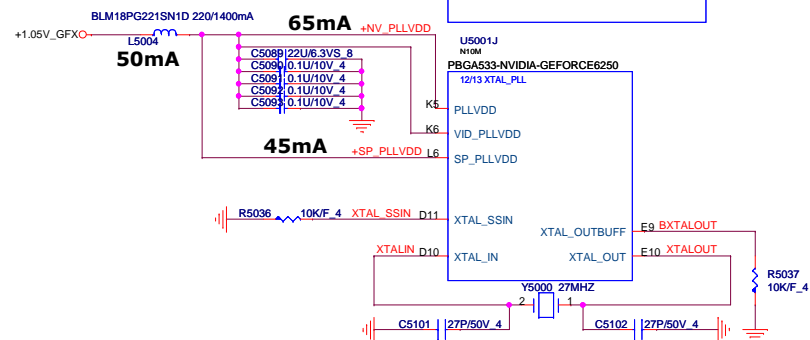
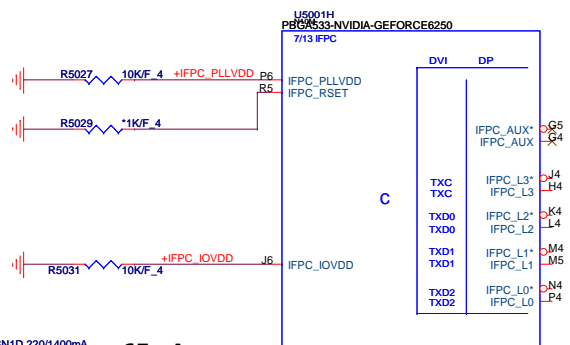
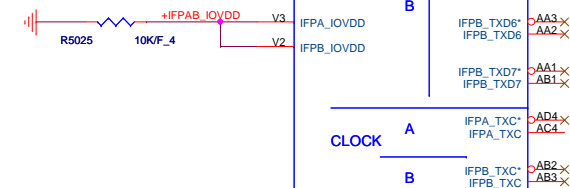
FBA\_CMD312

FBA\_CMD313

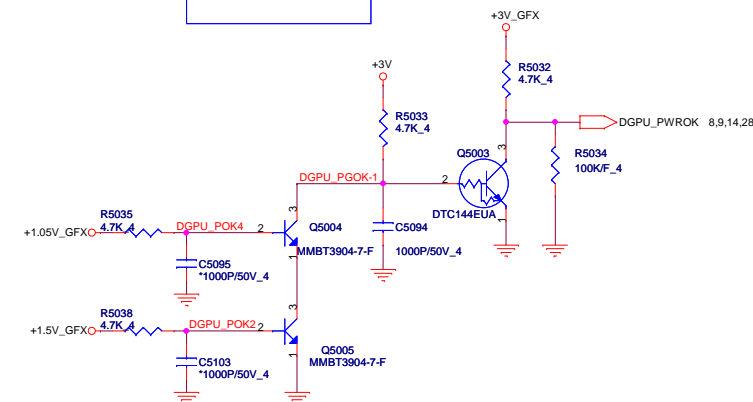
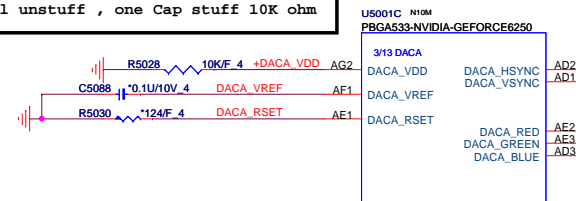
FBA\_CMD314

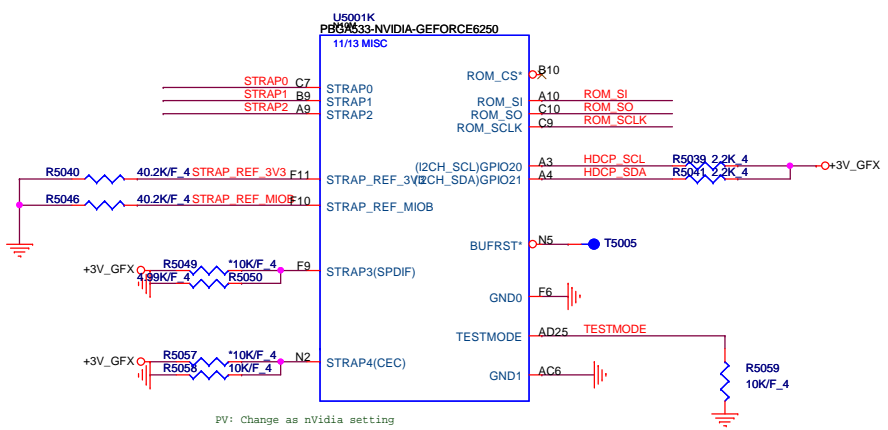


Optimus:  
All unstuff , one Cap stuff 10K ohm

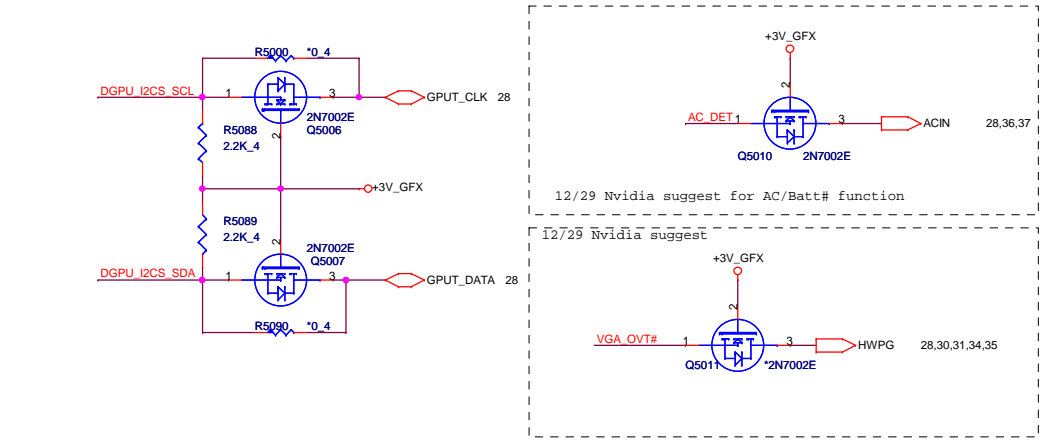
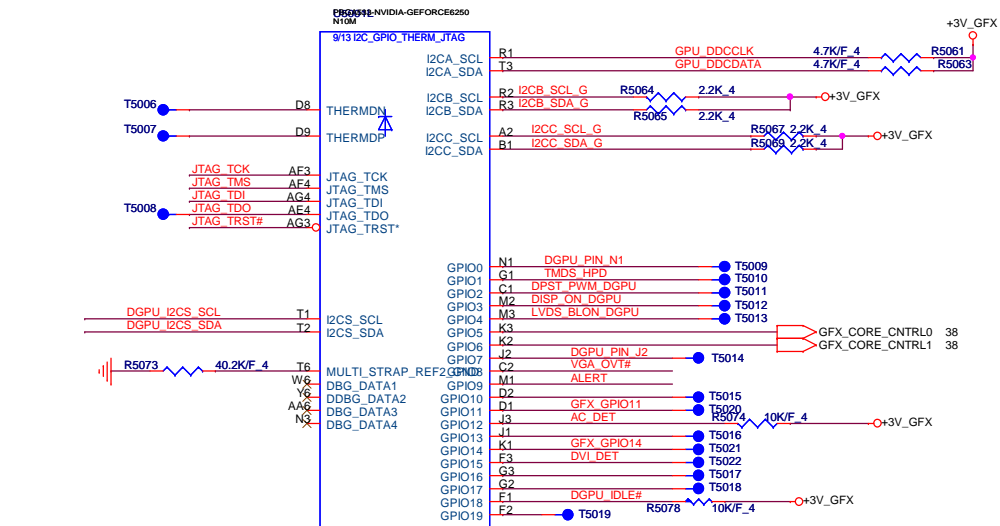


Optimus:  
All unstuff . one Cap stuff 10K ohm



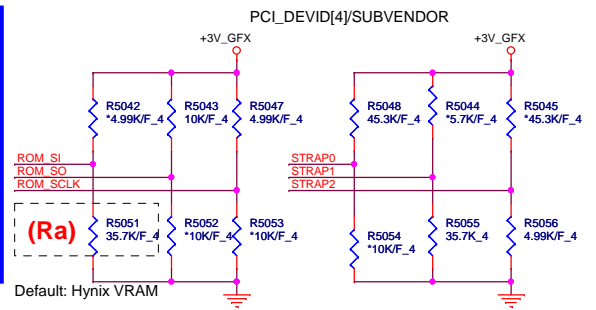


ROM\_SI -> based on VRAM.  
ROM\_SO -> PU 10K  
ROM\_SCLK -> PU 5K  
STRAP0 -> PU 45K  
STRAP1 -> PD 35K  
STRAP2 -> PD 5K  
STRAP3 -> PD 5K  
STRAP 4 -> PD 10K.



N12P-GV -> 0x17F  
N12M-GE -> 0xA7A 1010 -> PU15K

Logical Strap Bit Mapping		
	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVICE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V

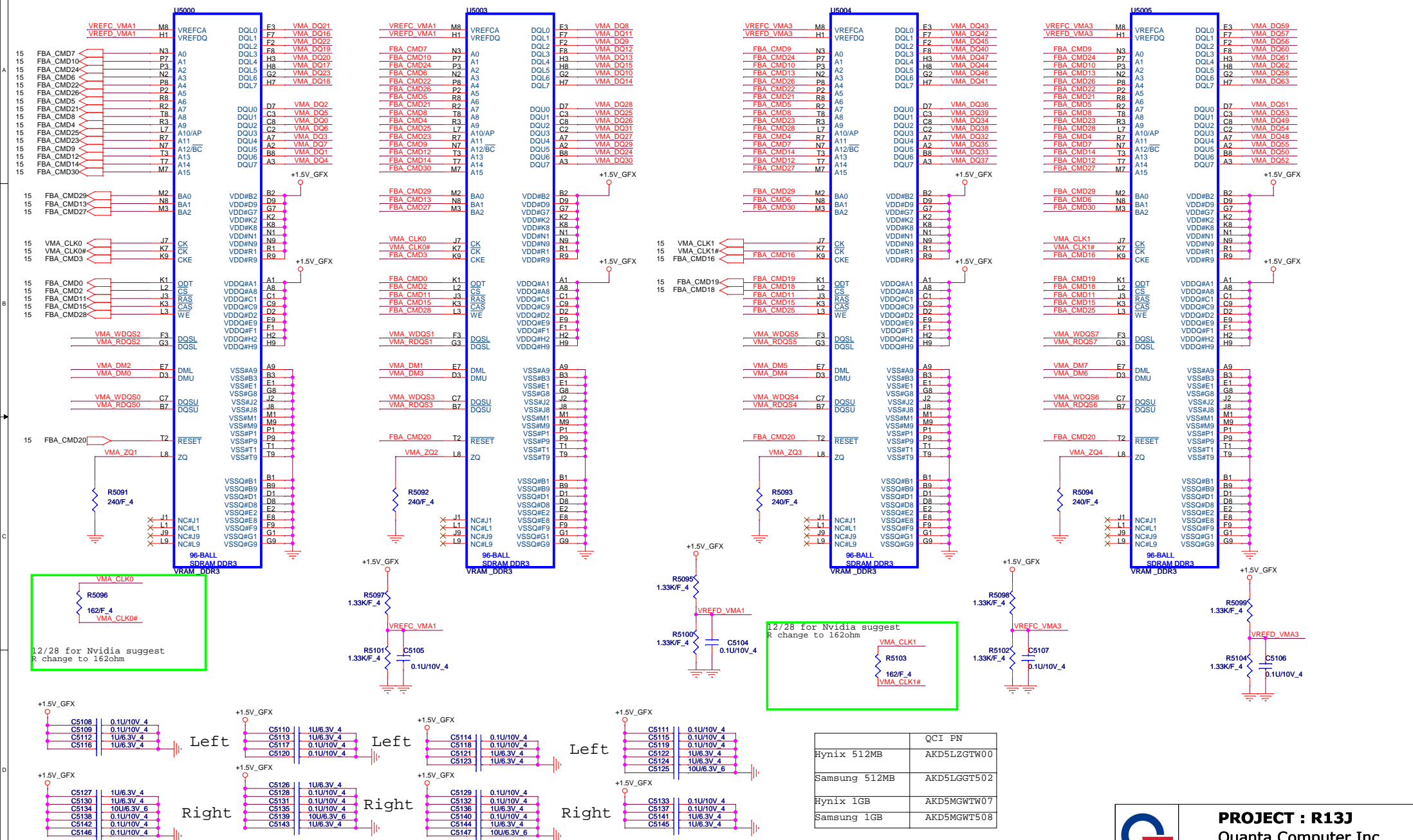
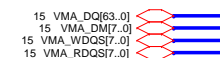
VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	ROM_SI
0000		Reserved			
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix			PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung			PD 20K
0110	DDR3 128Mx16x4, 128bit, 1GB,900MHz	Hynix	H5TQ2G63BFR-11C	AKD5MGWTW07	PD 35K
0111	DDR3 128Mx16x4, 128bit, 1GB,900MHz	Samsung	K4W2G1646C-HC11	AKD5MGWT508	PD 45K
XXXX					

## GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	I-C-T
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVD VDD0
6	OUT	N/A	NVVD VDD1
7	OUT	N/A	NVVD VDD2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	Memory VREF SELECT
11	I/O	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	THERM_LOAD_STEP_DOWN
14	OUT	N/A	THERM_LOAD_STEP_UP

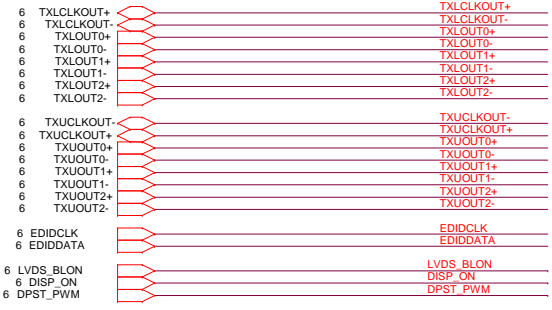
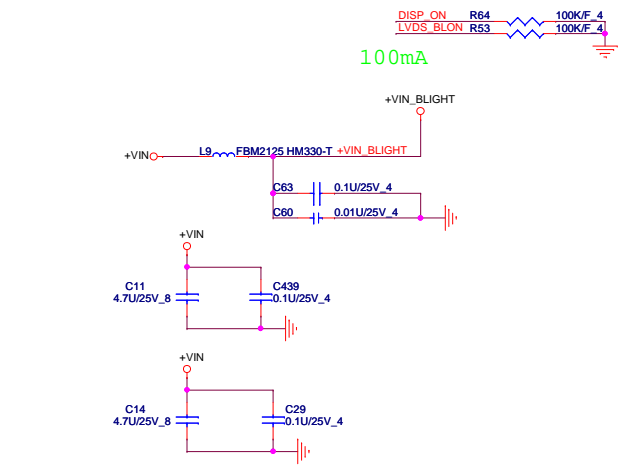
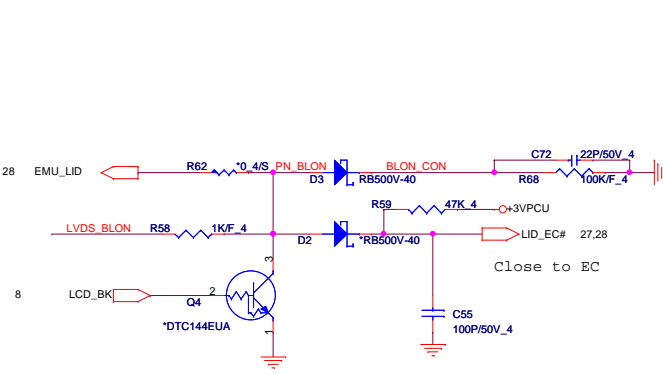
**CHANNEL A: 256MB/512MB DDR3**



	QCI PN
Hynix 512MB	AKD5LZGTW0
Samsung 512MB	AKD5LGGT50
Hynix 1GB	AKD5MGWTW0
Samsung 1GB	AKD5MGWT50



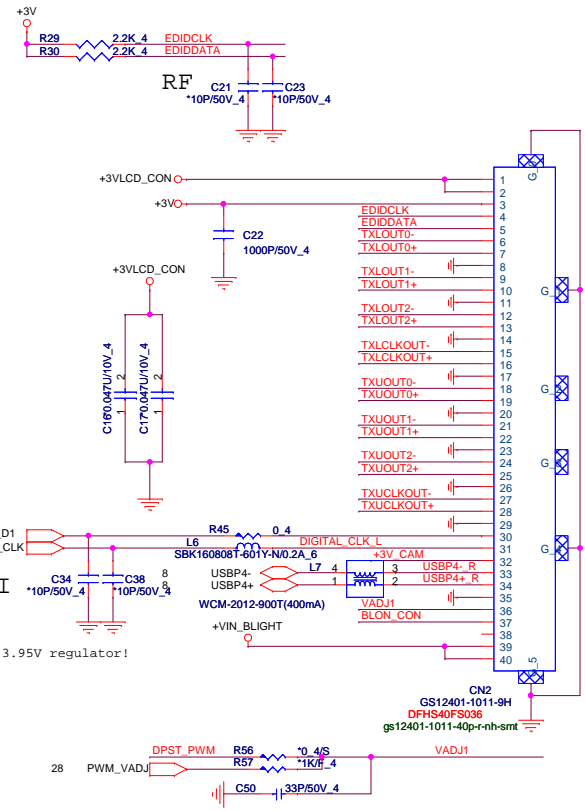
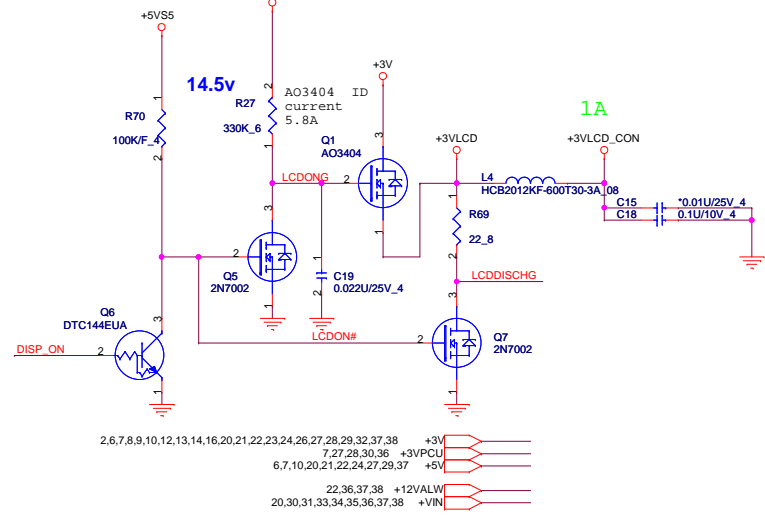
LID Switch

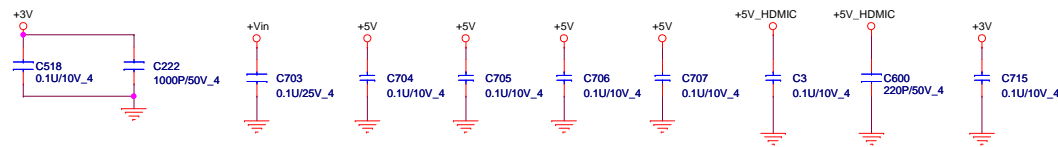


Please note that 2011 camera is +3V a We do not need to use 5V -> 3.95V regulator!

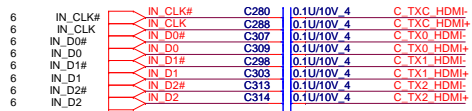
follow L7 location  
DEL reserved Restor

change to +5VS5

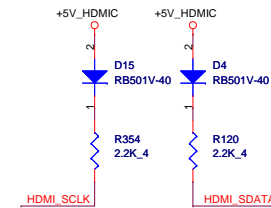
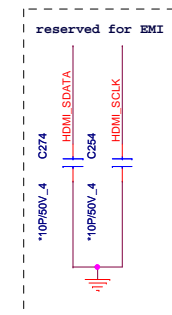
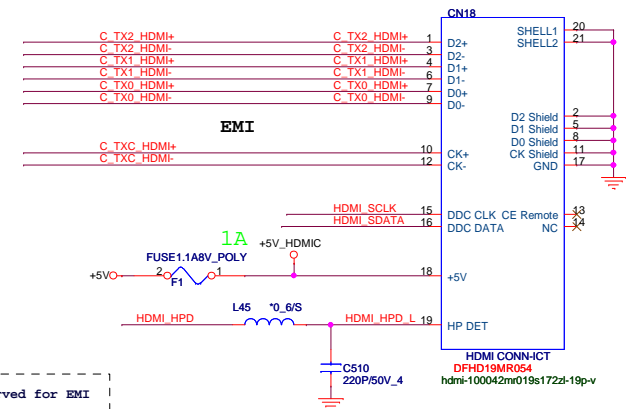
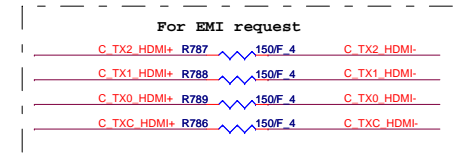
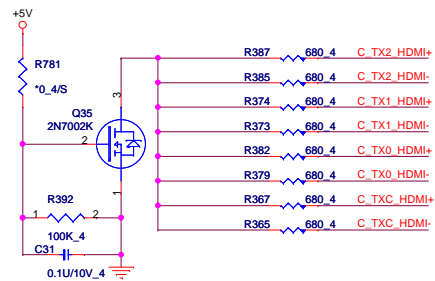
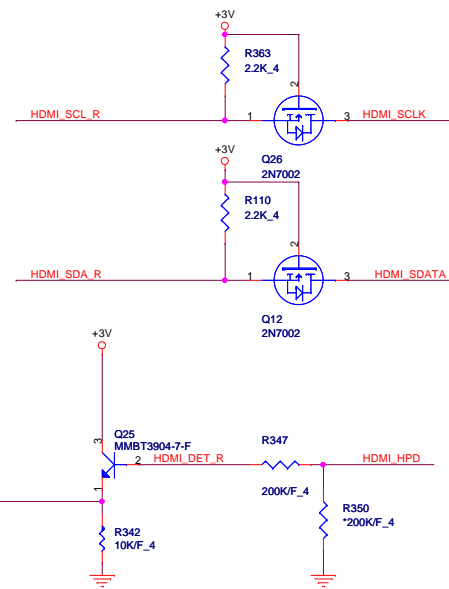


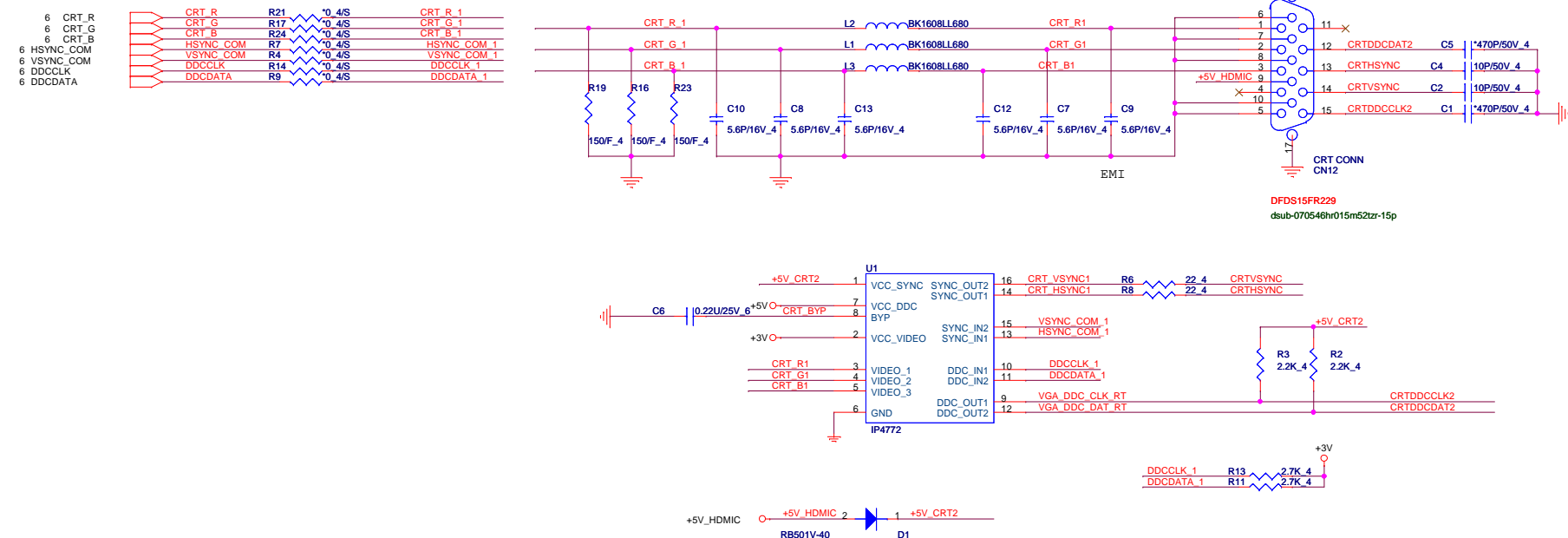


## close to HDMI conn

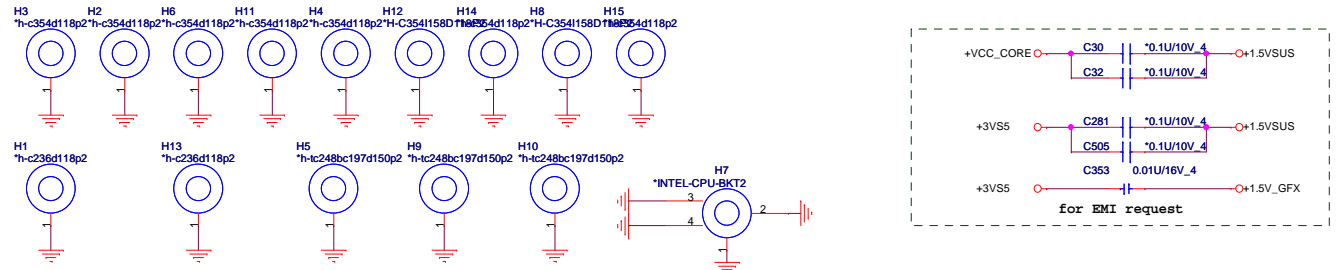


## Close to HDMI Connector

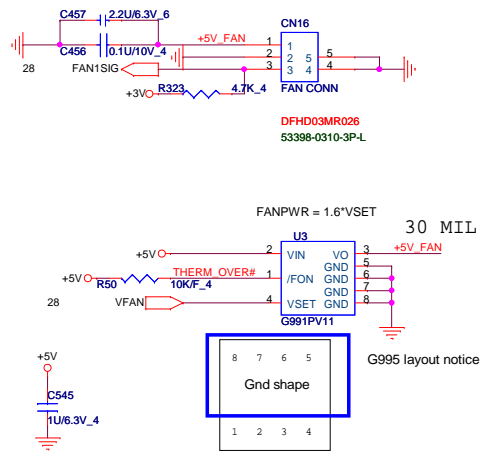




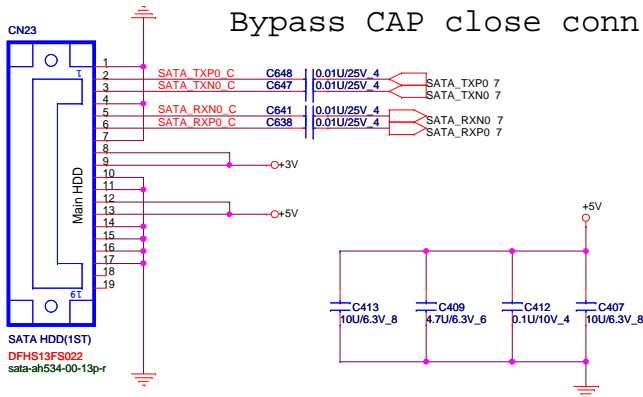
HOLE



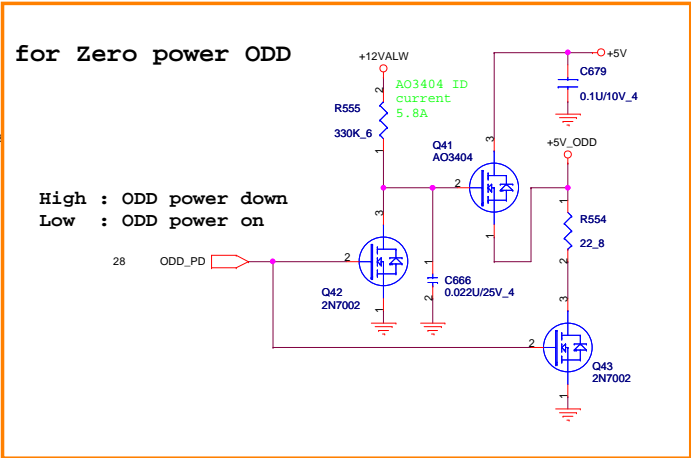
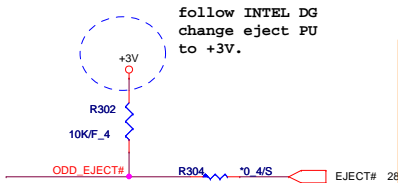
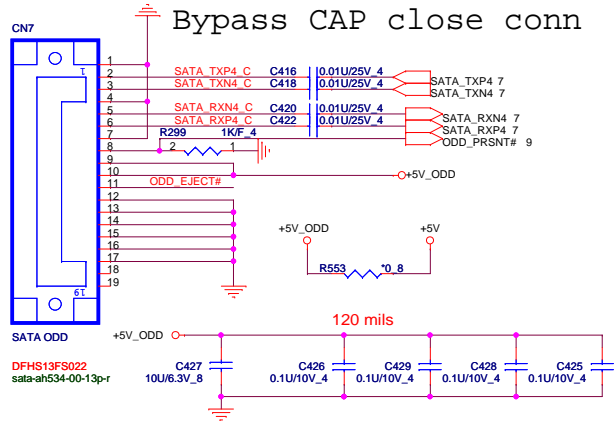
CPU FAN



SATA HDD CONNECTOR



SATA ODD CONNECTOR

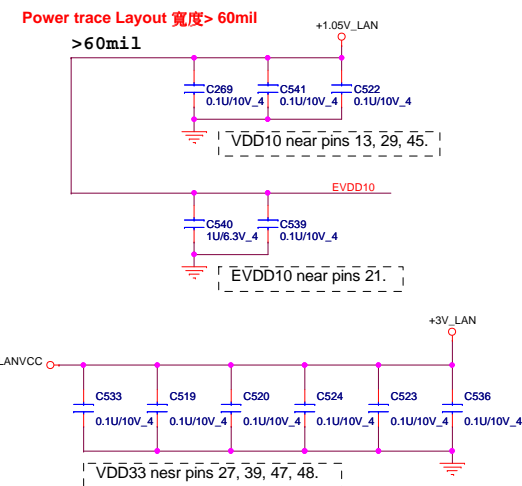




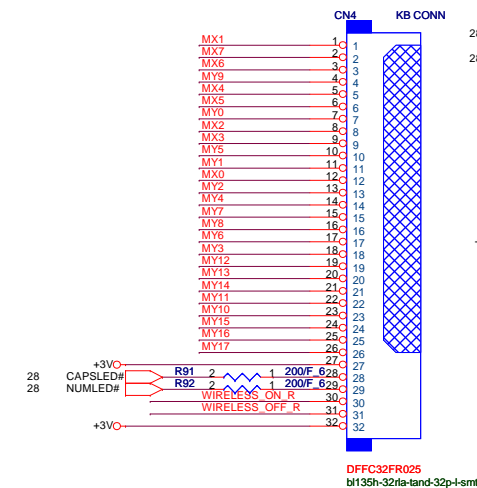






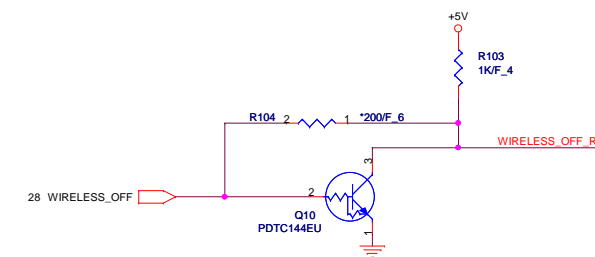
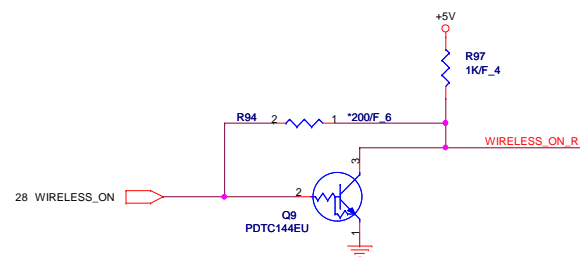
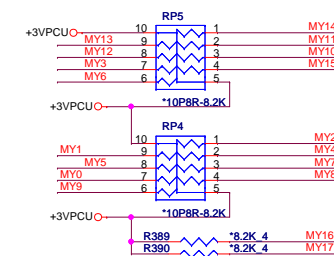


## 27

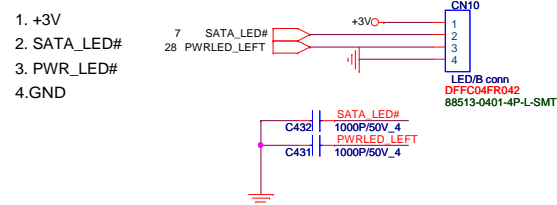


28 MY[0..17]  MY[0..17]

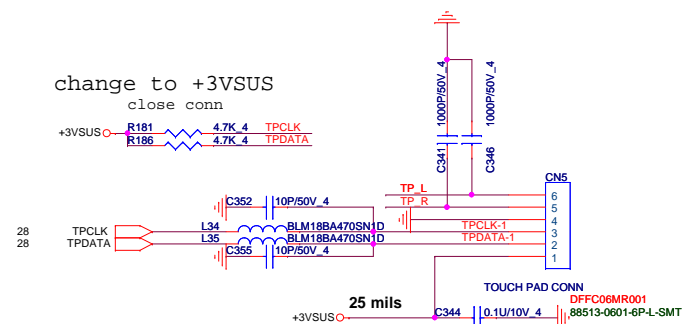
28 MX[0..7]  MX[0..7]



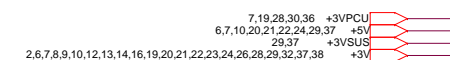
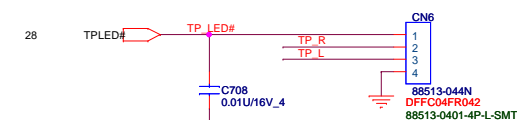
## TOUCH PAD Con.



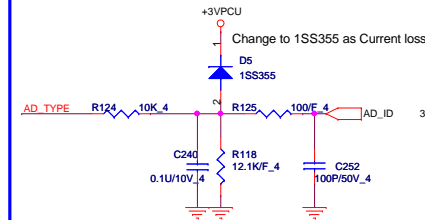
```
change to +3VSUS
close conn
```



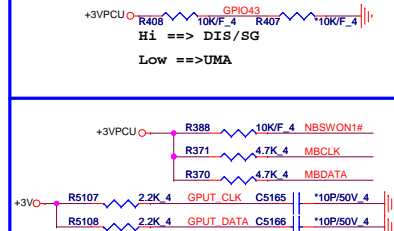
**To TOUCH PAD SW board**



## adapter Type check

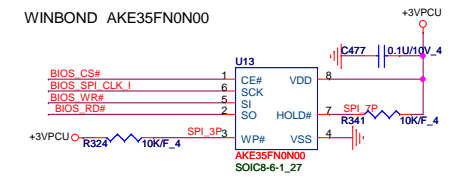


adapter select for EC



128K byte SPI EC ROM

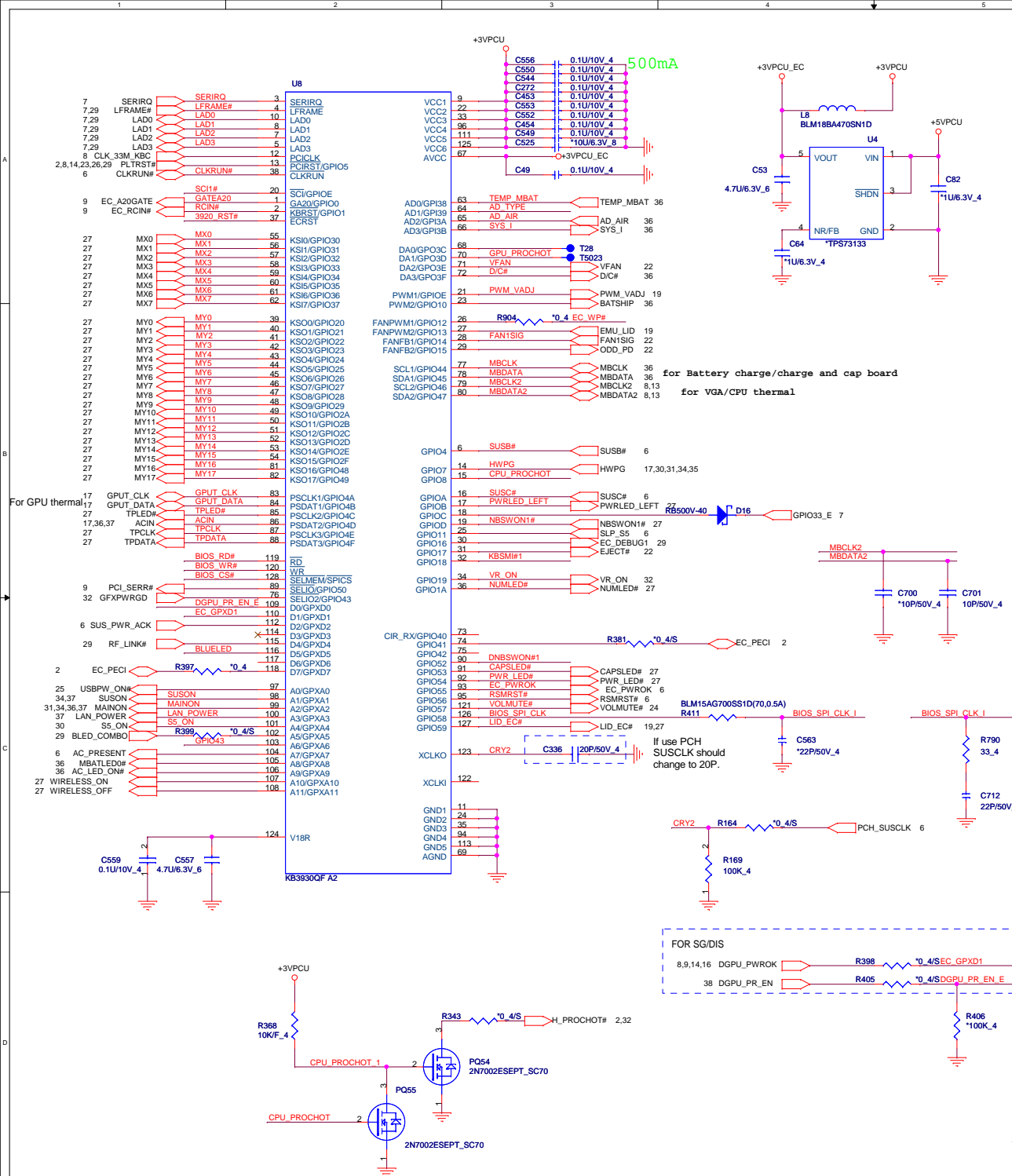
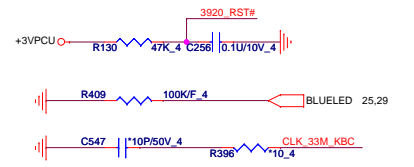
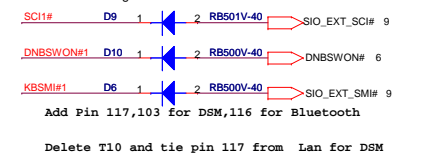
Socket: DG008000031  
EON AKE35FN0Q00  
WINBOND AKE35FN0N00



INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	1
H	L	X	X	L	0
L	L	X	X	H <sub>old</sub>	1
H	H	↑	H	H	1
H	H	↓	L	L	0
H	H	L	X	Q <sub>0</sub>	$\bar{Q}_0$



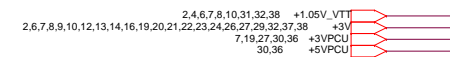
Change to RB500 as Current loss



FOR SG/DIS

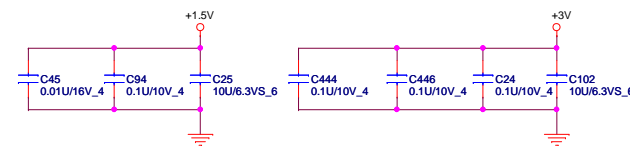
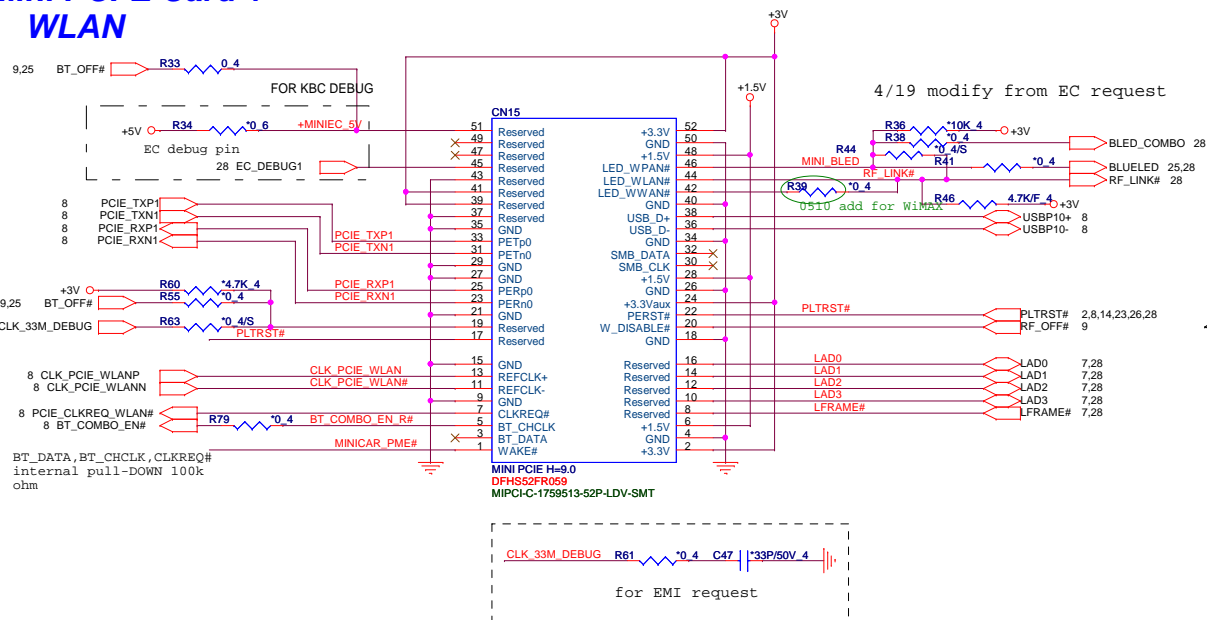
8,9,14,16 DGPU\_PWROK R398 \*0\_4/SEC GPXD1

38 DGPU\_PR\_EN R405 \*0\_4/SDGPU PR\_EN\_E

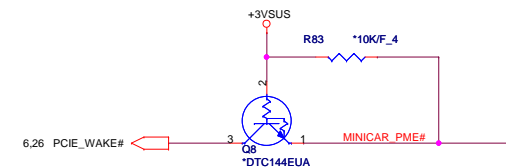


# Mini PCI-E Card 1 WLAN

29



INTEL WLAN  
CARD PIN 20  
W\_DISABLE#  
have  
internal  
pull-up 110k  
ohm



4,10,12 +1.5V

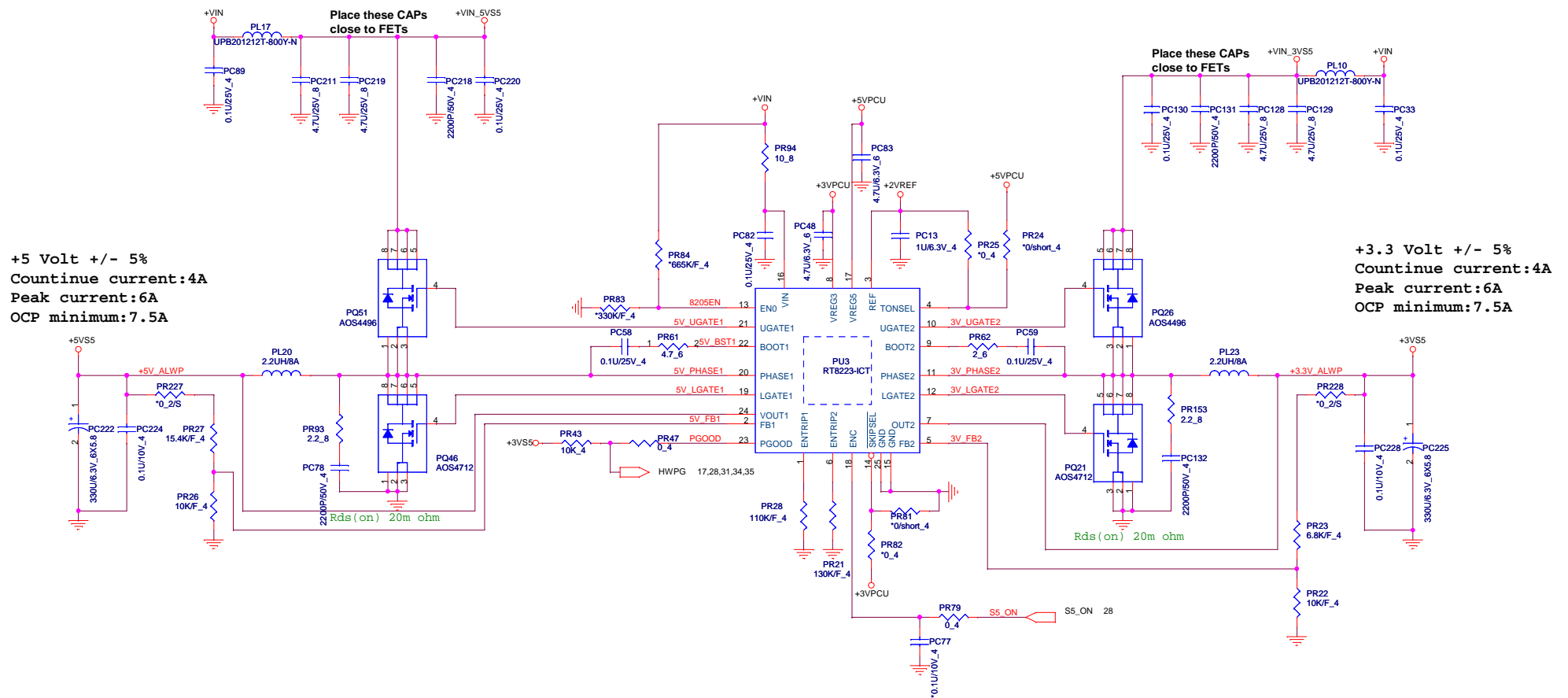
2,6,7,8,9,10,12,13,14,16,19,20,21,22,23,24,26,27,28,32,37,38 +3V

7,19,27,28,30,36 +3VPCU

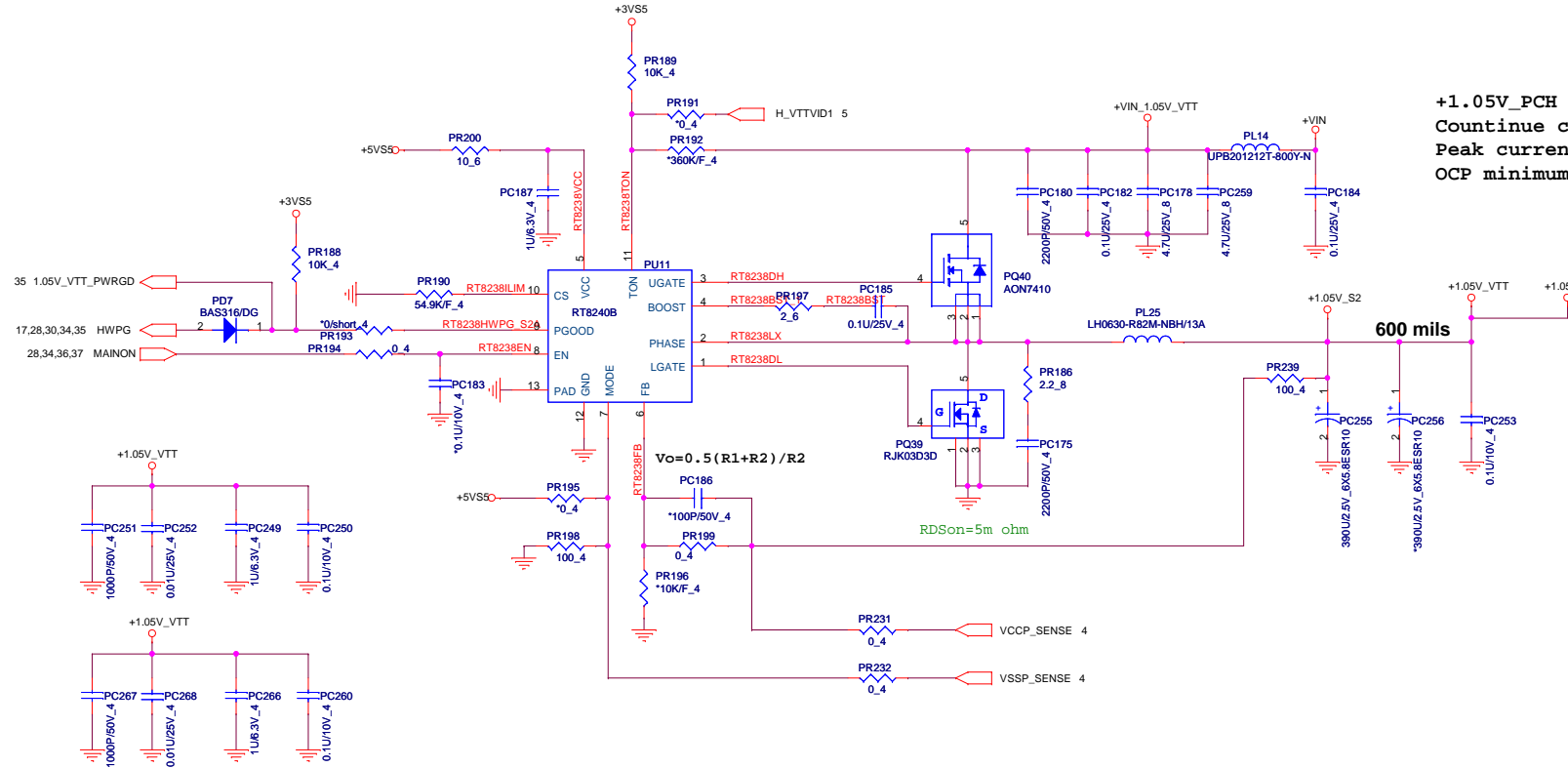
6,7,10,20,21,22,24,27,37 +5V

	<b>PROJECT : R13J</b>		
	Quanta Computer Inc.		
	Size Custom	Document Number <b>MINI PCIE CONN X1</b>	Rev 1A
Date: Wednesday, September 28, 2011   Sheet 29 of 38			

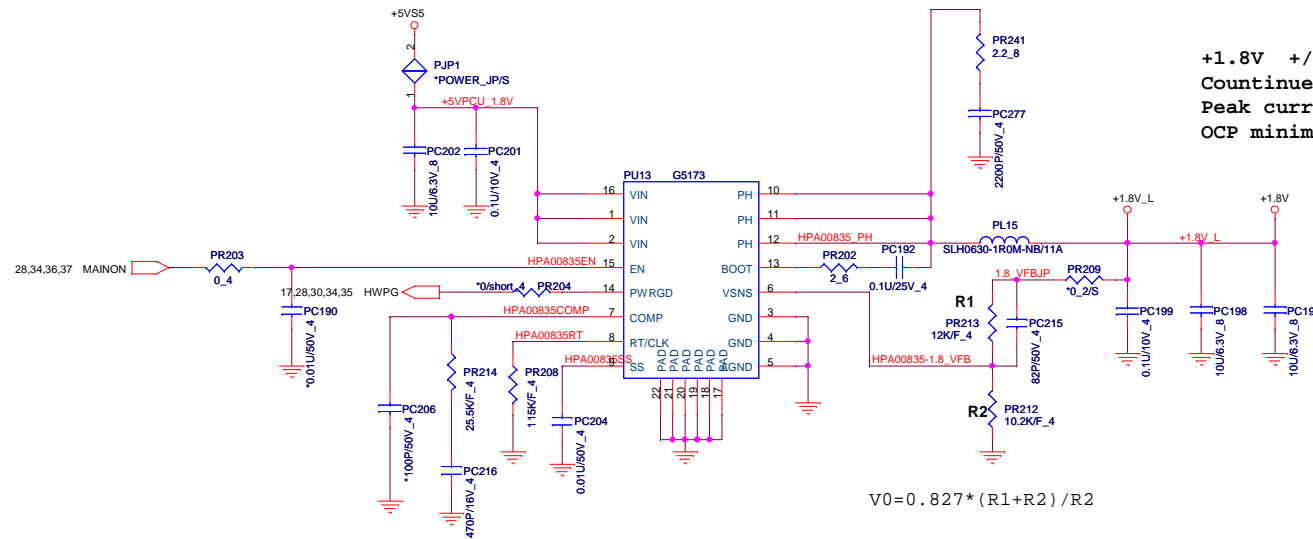




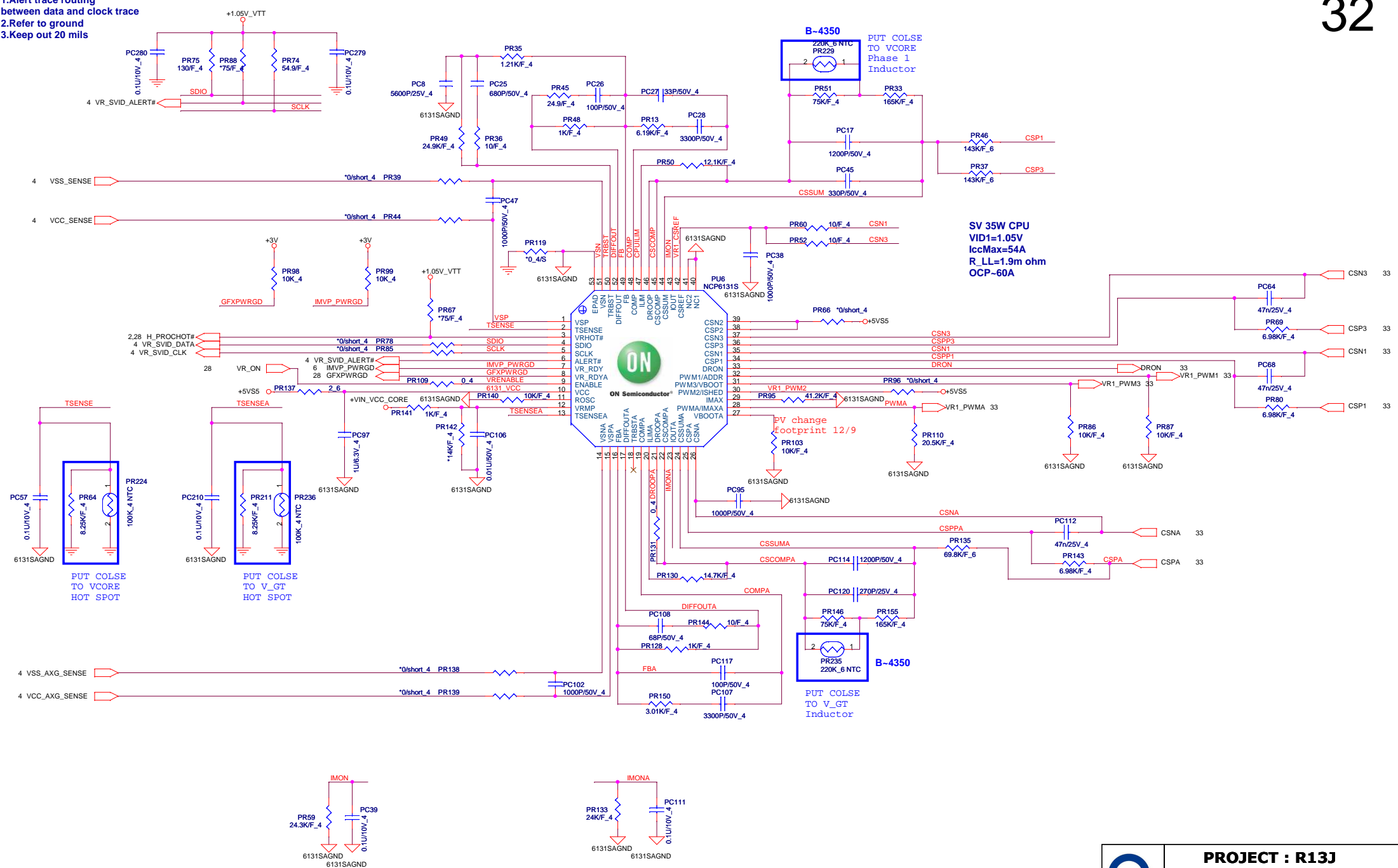
+1.05V\_PCH Volt +/- 5%  
 Countinue current:10A  
 Peak current: 12A  
 OCP minimum: 14.5A

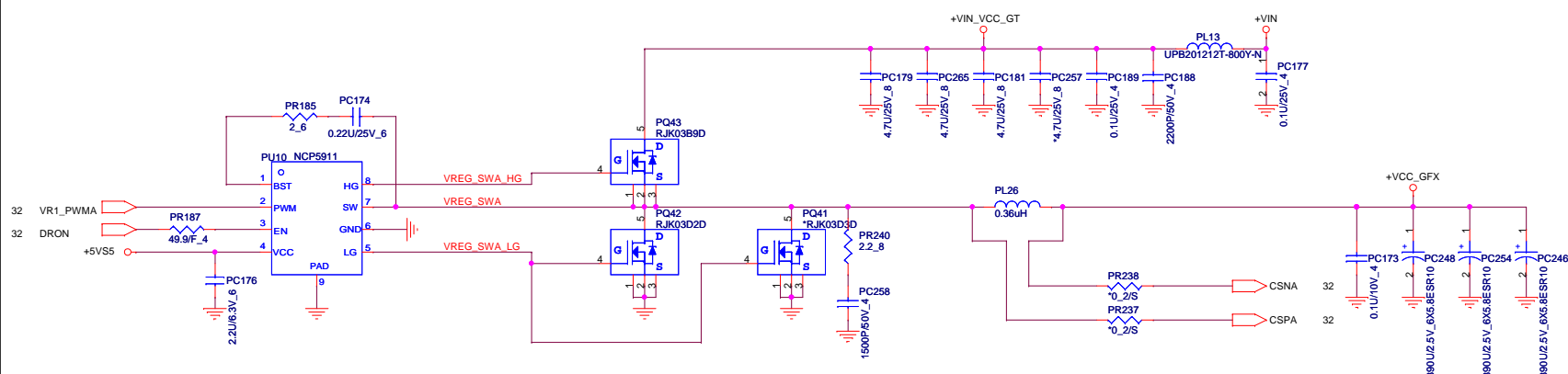
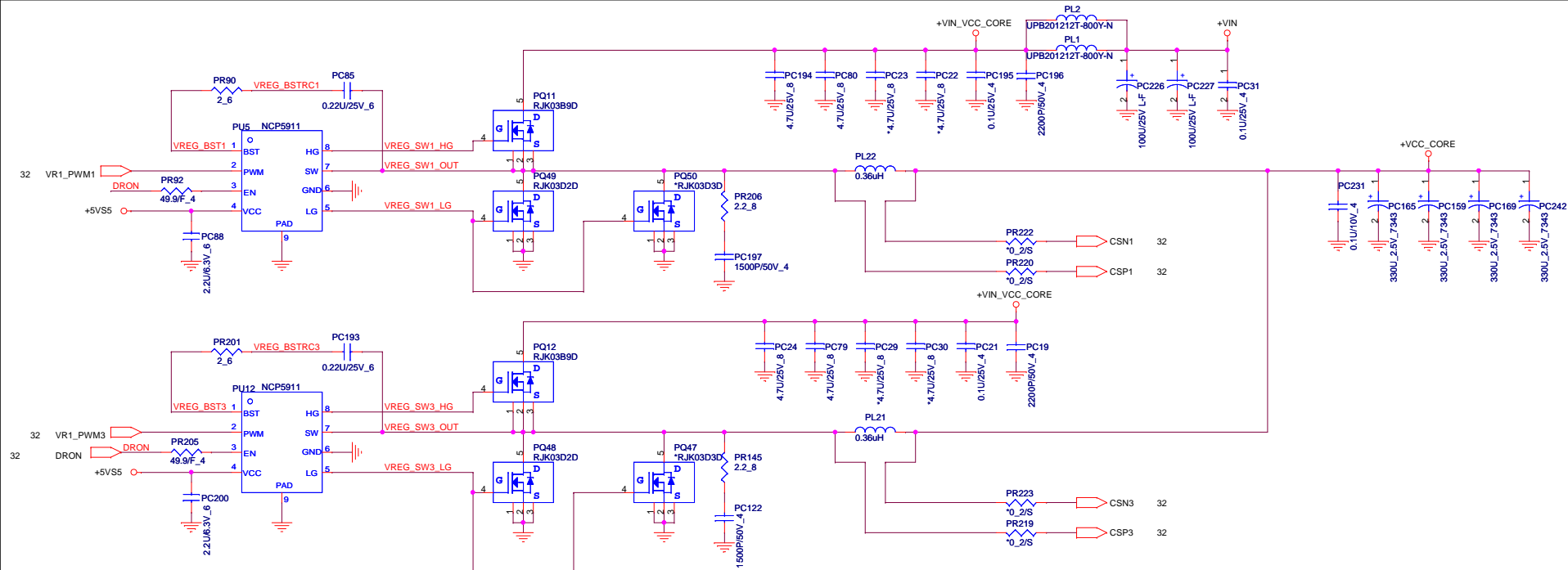


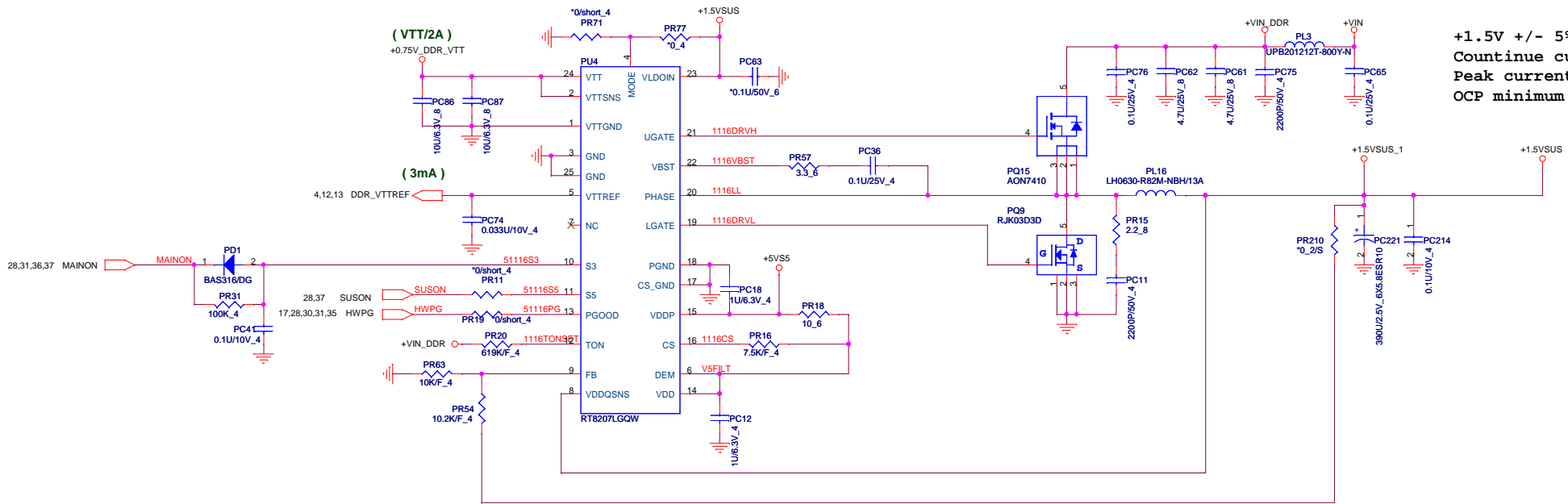
+1.8V +/- 5%  
 Countinue current:1.5A  
 Peak current:2.5A  
 OCP minimum 4A



- 1.Alert trace routing between data and clock trace
- 2.Refer to ground
- 3.Keep out 20 mils





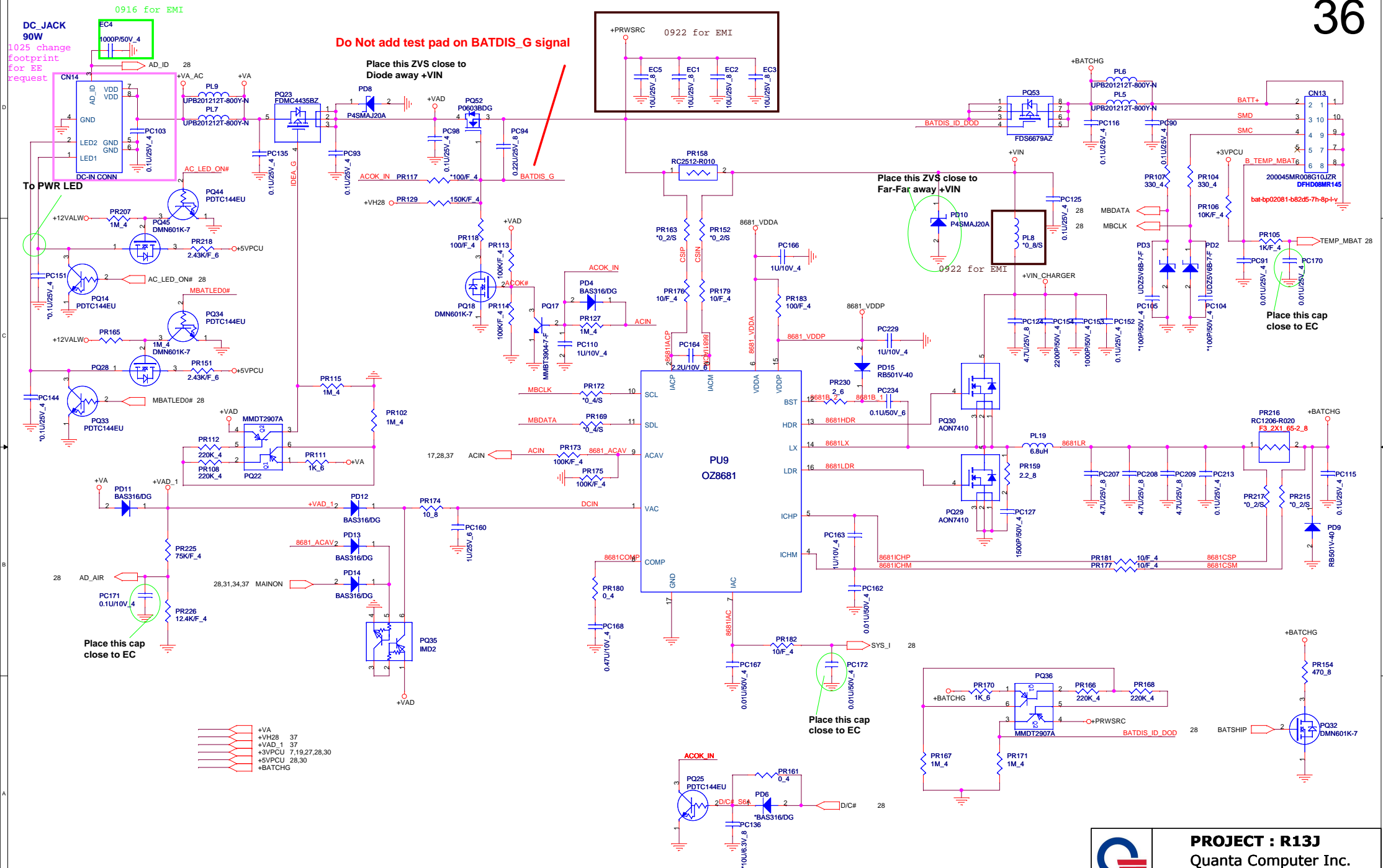


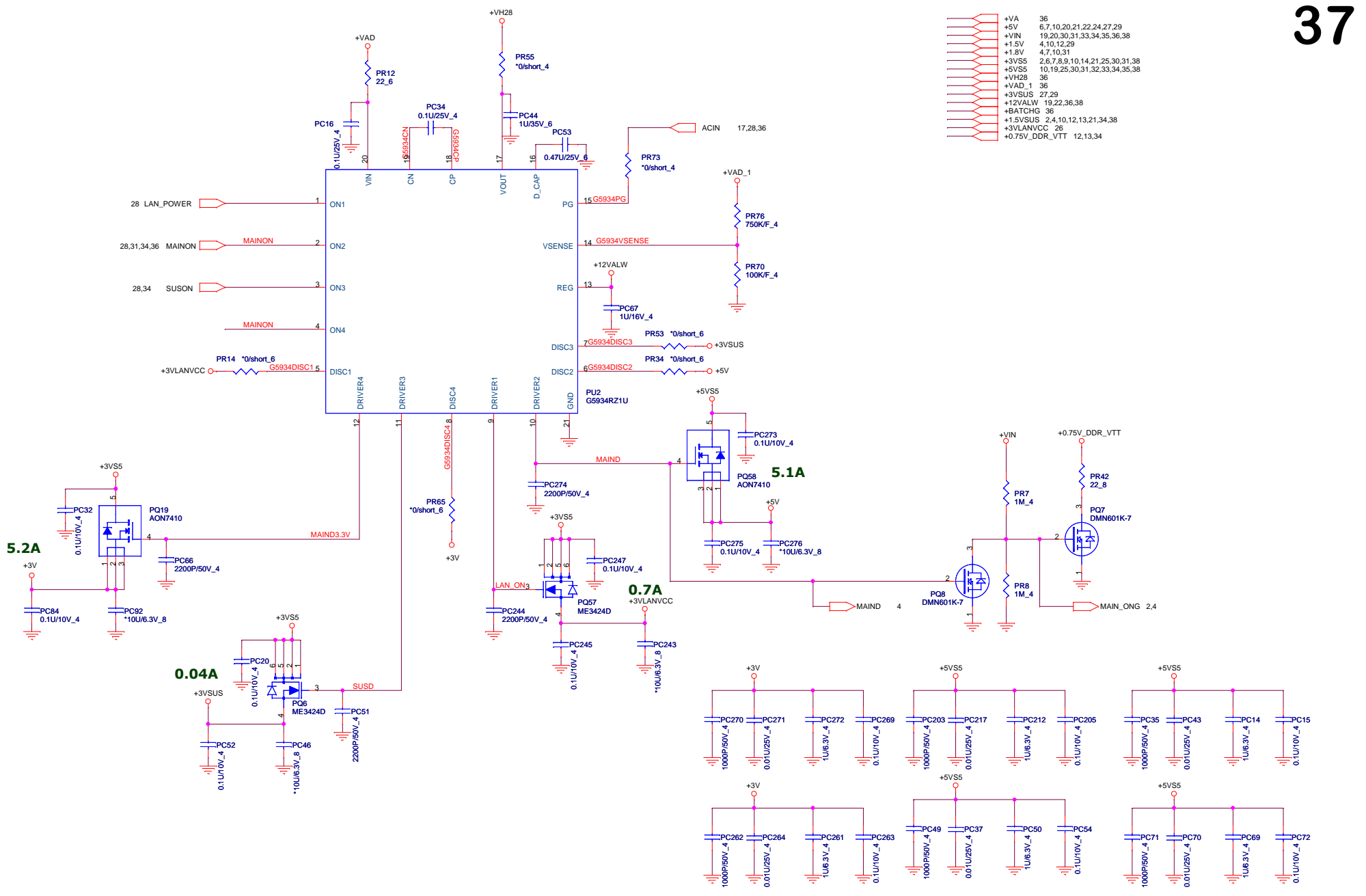
2011\_0217 modify for EE request cancel 1.0V\_VGA











## 38

