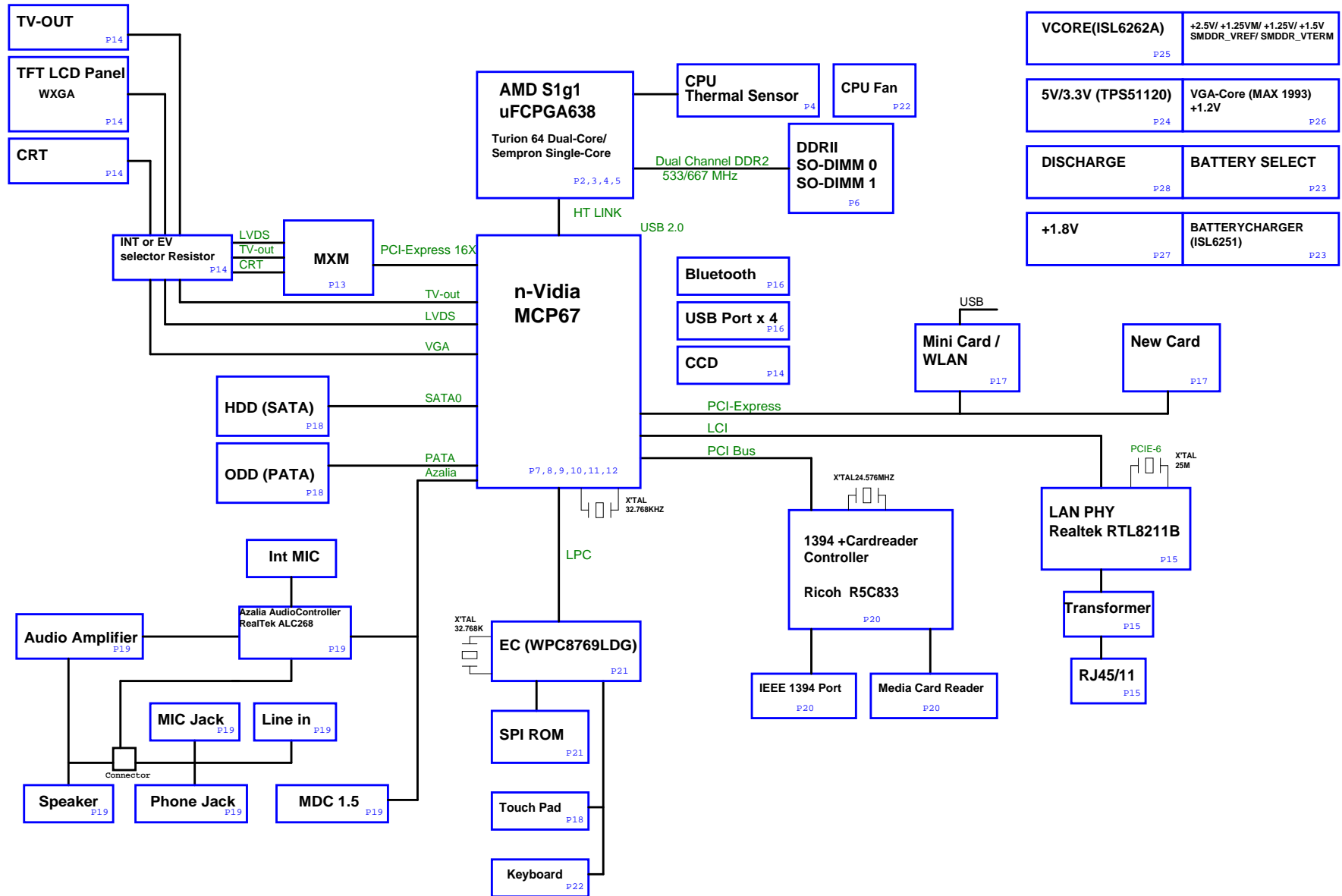


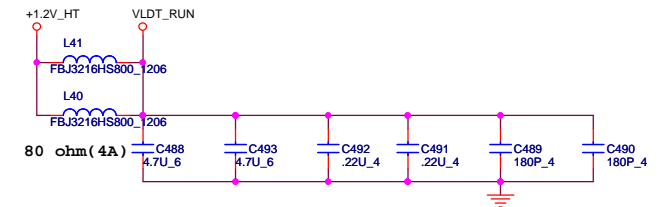
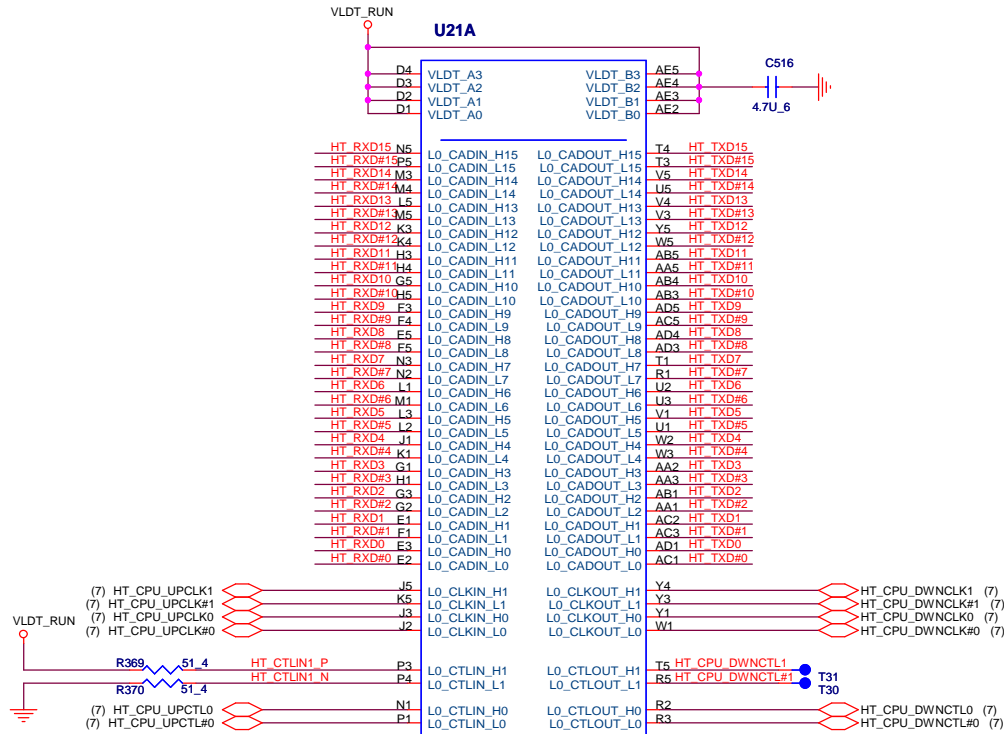
ZO3 SYSTEM BLOCK DIAGRAM





PROCESSOR HYPERTRANSPORT INTERFACE

VLDLT_Ax AND VLDLT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



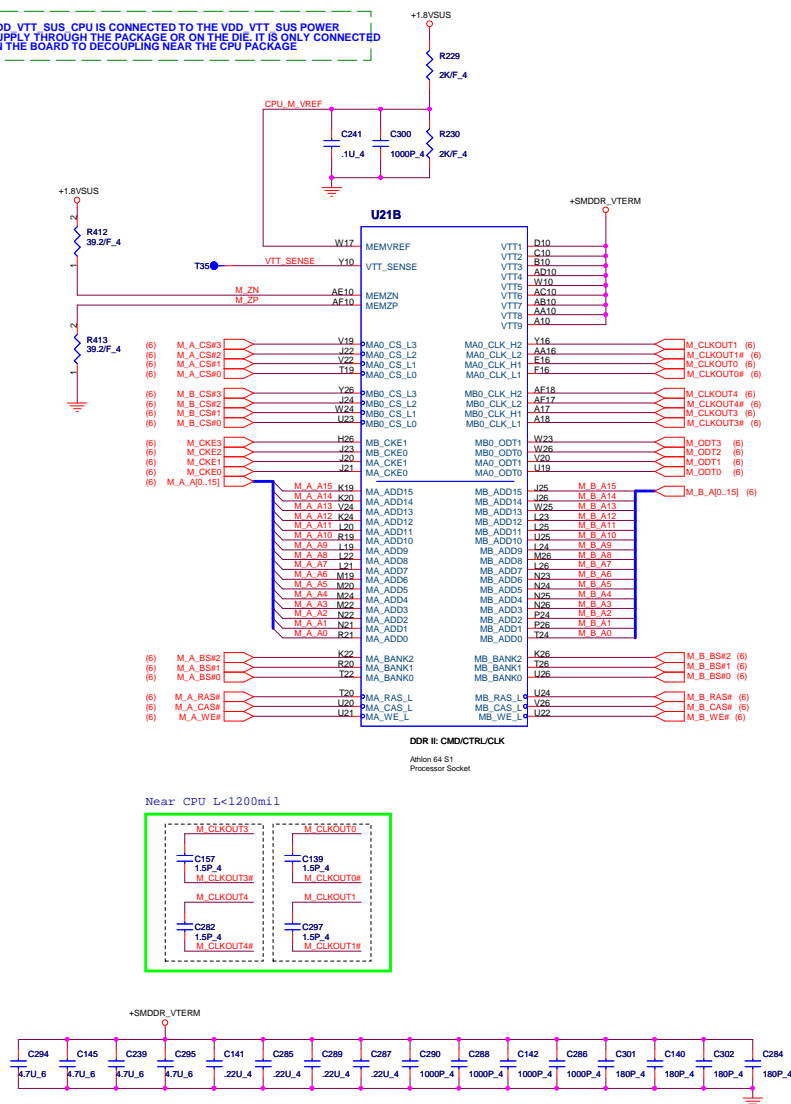
LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDLT0 POWER PINS

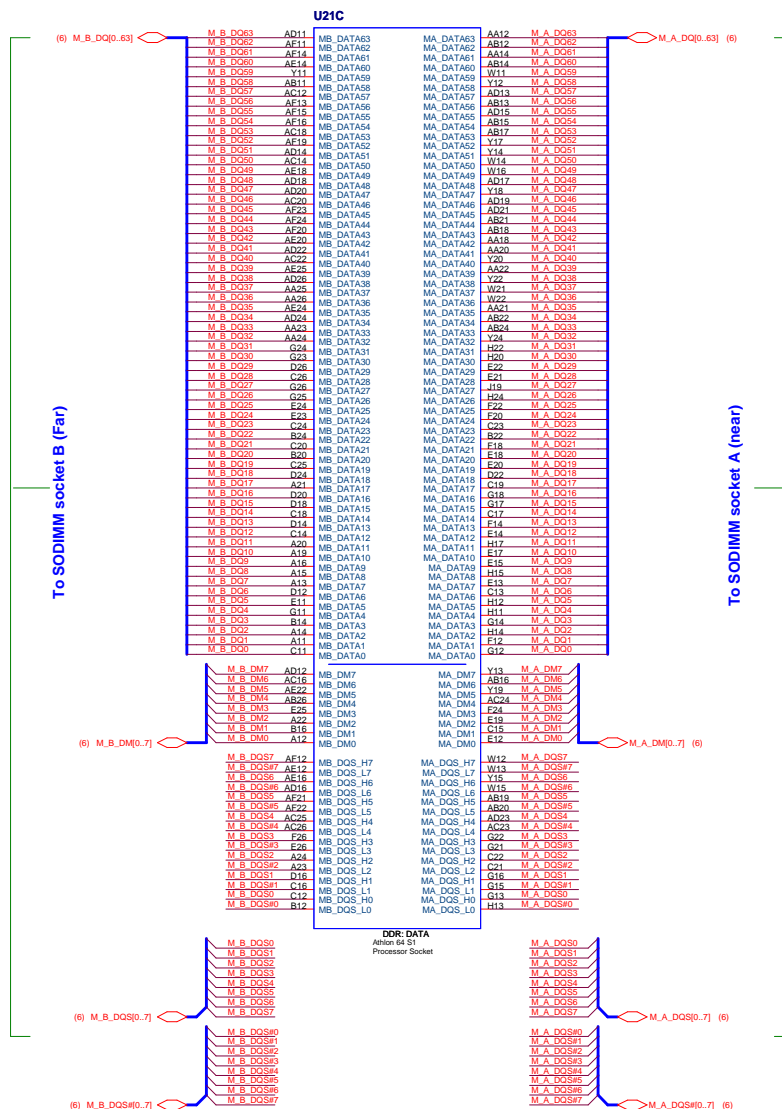


PROJECT : Z03
Quanta Computer Inc.

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	ATHLON64 HT I/F	1A
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Processor DDR2 Memory Interface



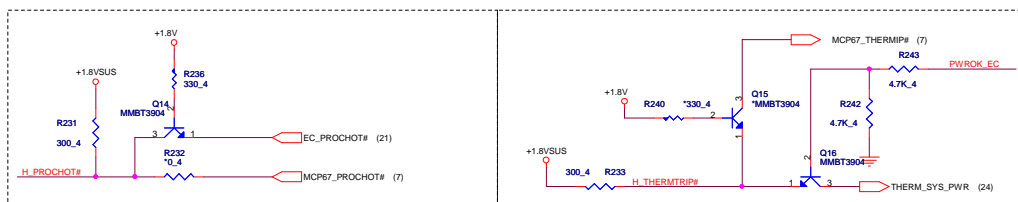
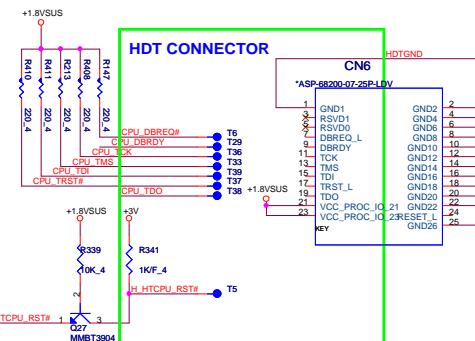
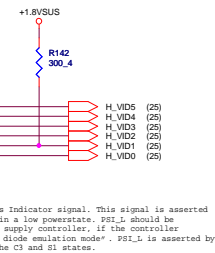
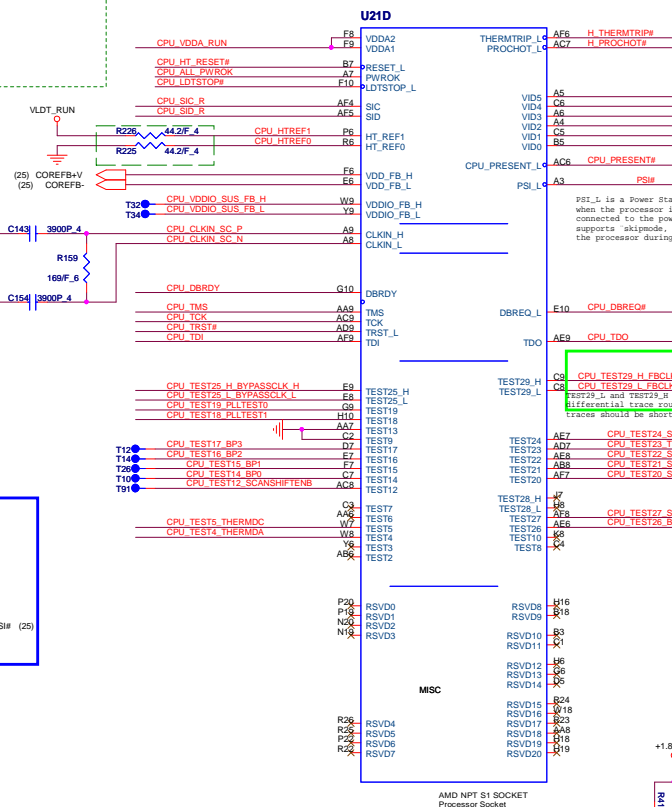
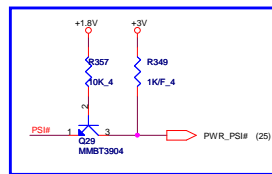
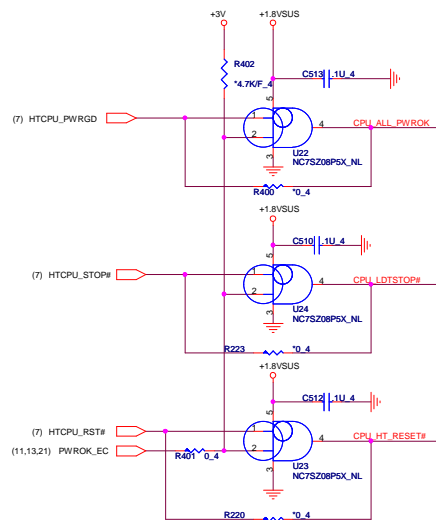
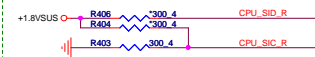
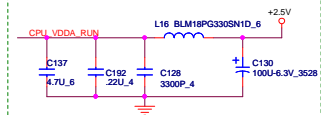
PROJECT : ZO3
Quanta Computer Inc.

Size	Document Number ATHLON64 DDRII MEMORY I/F		
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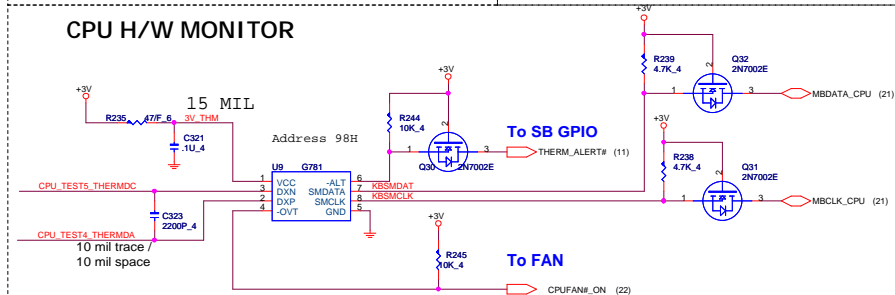


ATHLON Control and Debug

If AMD SI is not used, the SID pin can be left unconnected and SIO should have a 300- (±5%) pulldown to VSS.



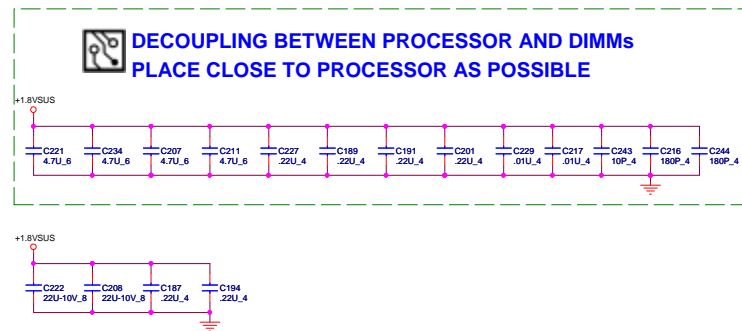
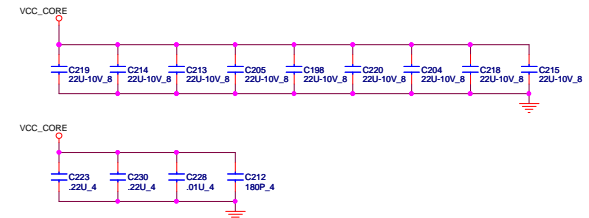
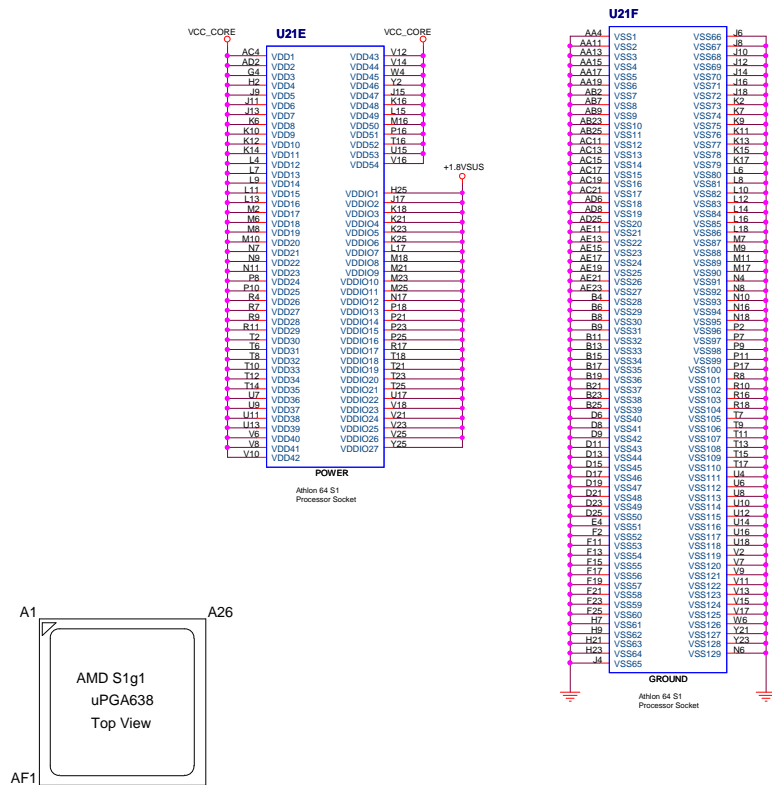
CPU H/W MONITOR

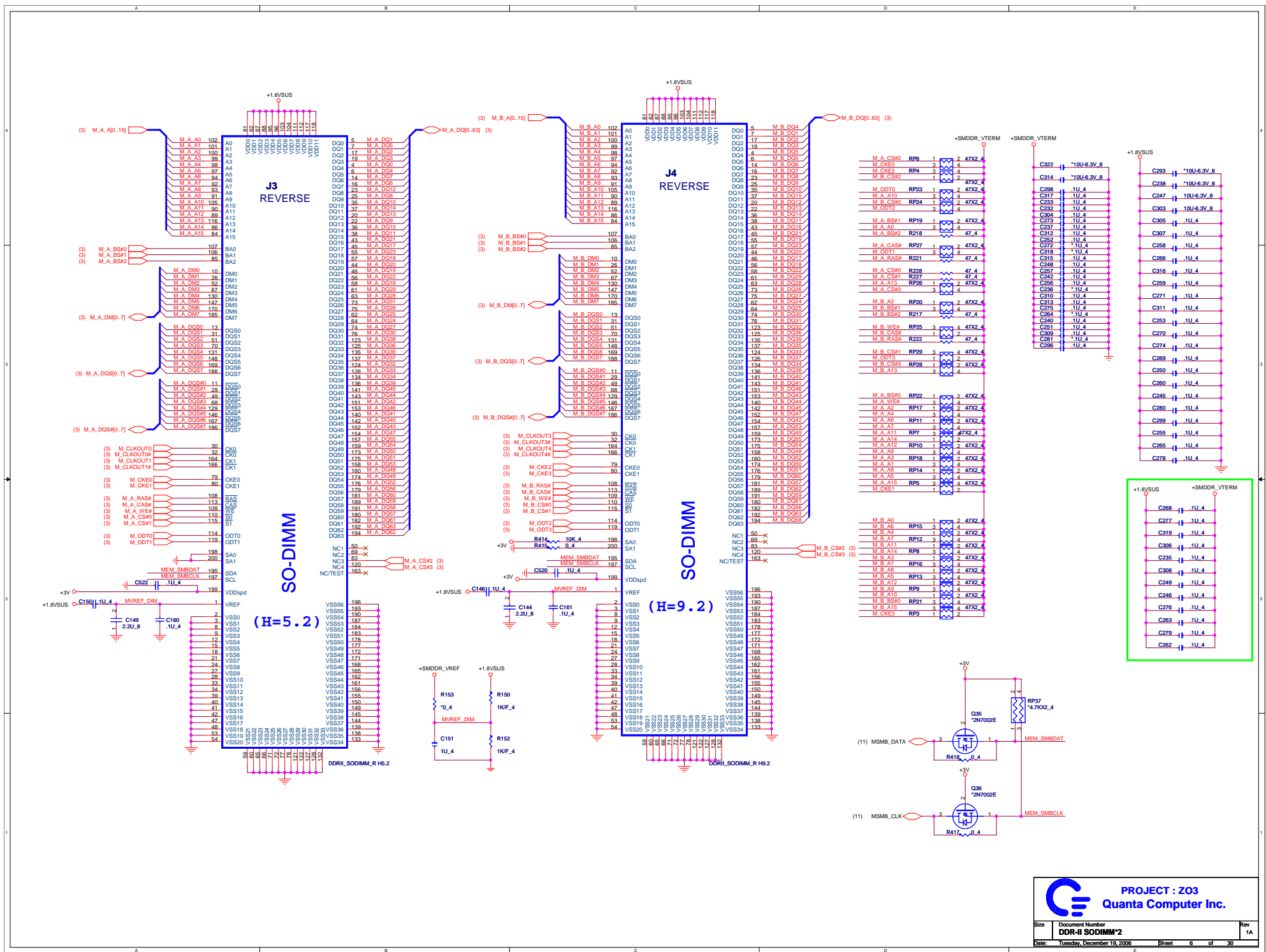


PROJECT : Z03
Quanta Computer Inc.

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	ATHLON64 CTRL & DEBUG		
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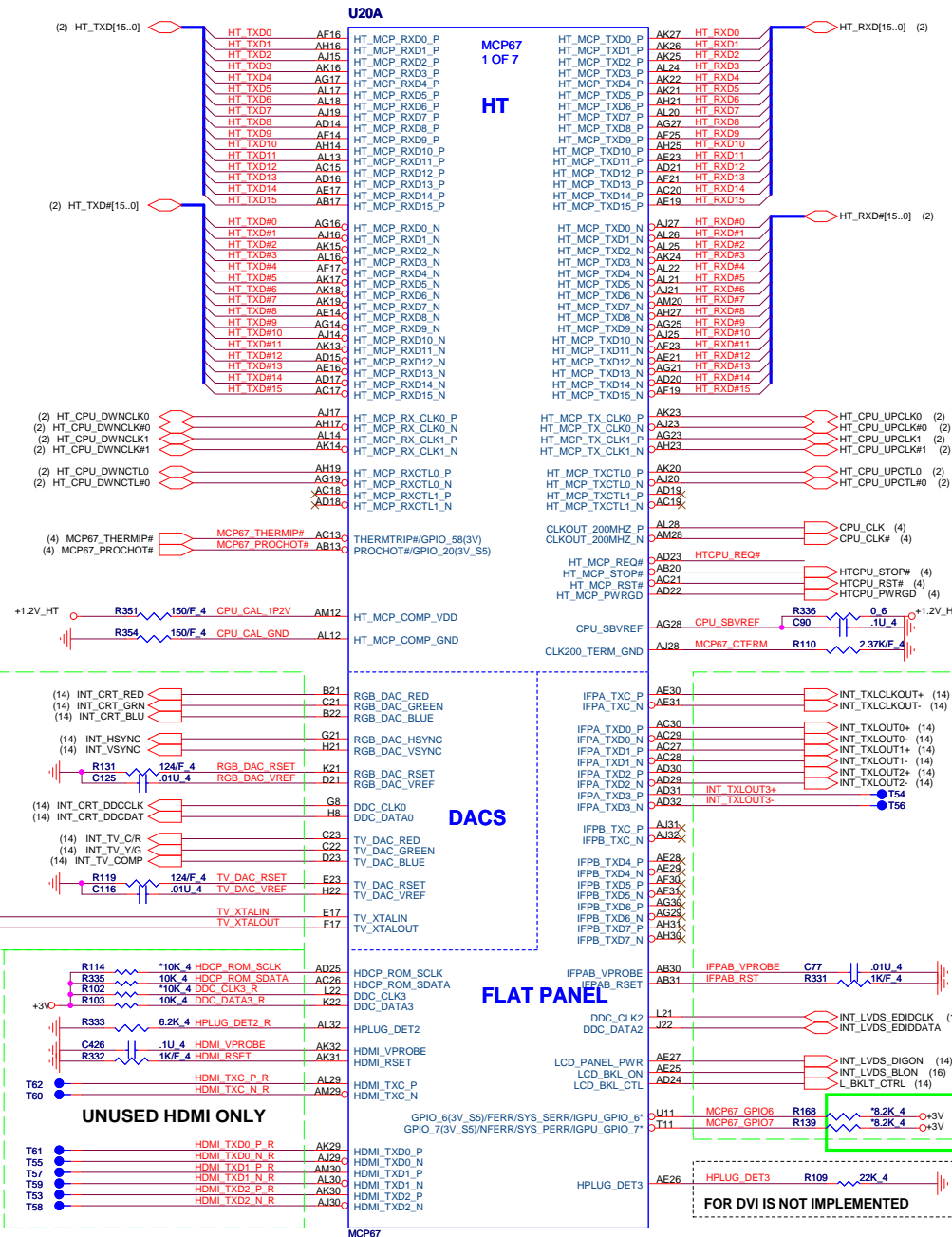
PROCESSOR POWER AND GROUND





MCP67 Unused UMA Only	
MCP67 Signal Name	Component
RGB_DAC_RSET	STUFF
RGB_DAC_VREF	STUFF
DDC_DATA0	10K PULLHIGH
TV_DAC_RSET	STUFF
TV_DAC_VREF	STUFF
IFPAB_RST	STUFF
IFPAB_VROBE	STUFF
DDC_DATA2	10K PULLHIGH
HPLUG_DET3	22K PULLDOWN
HDMI_RSET	STUFF
HDMI_VPROBE	STUFF
DDC_DATA3_R	10K PULLHIGH
HDCPL_ROM_SDATA	10K PULLHIGH
HPLUG_DET2_R	6.2K PULLDOWN

MCP67 Unused UMA Only	
MCP67 Signal Name	Component
RGB_DAC_RSET	STUFF
RGB_DAC_VREF	STUFF
DDC_DATA0	10K PULLHIGH
TV_DAC_RSET	STUFF
TV_DAC_VREF	STUFF
IFPAB_RST	STUFF
IFPAB_VROBE	STUFF
DDC_DATA2	10K PULLHIGH
HPLUG_DET3	22K PULLDOWN
HDMI_RSET	STUFF
HDMI_VPROBE	STUFF
DDC_DATA3_R	10K PULLHIGH
HDCPL_ROM_SDATA	10K PULLHIGH
HPLUG_DET2_R	6.2K PULLDOWN



```

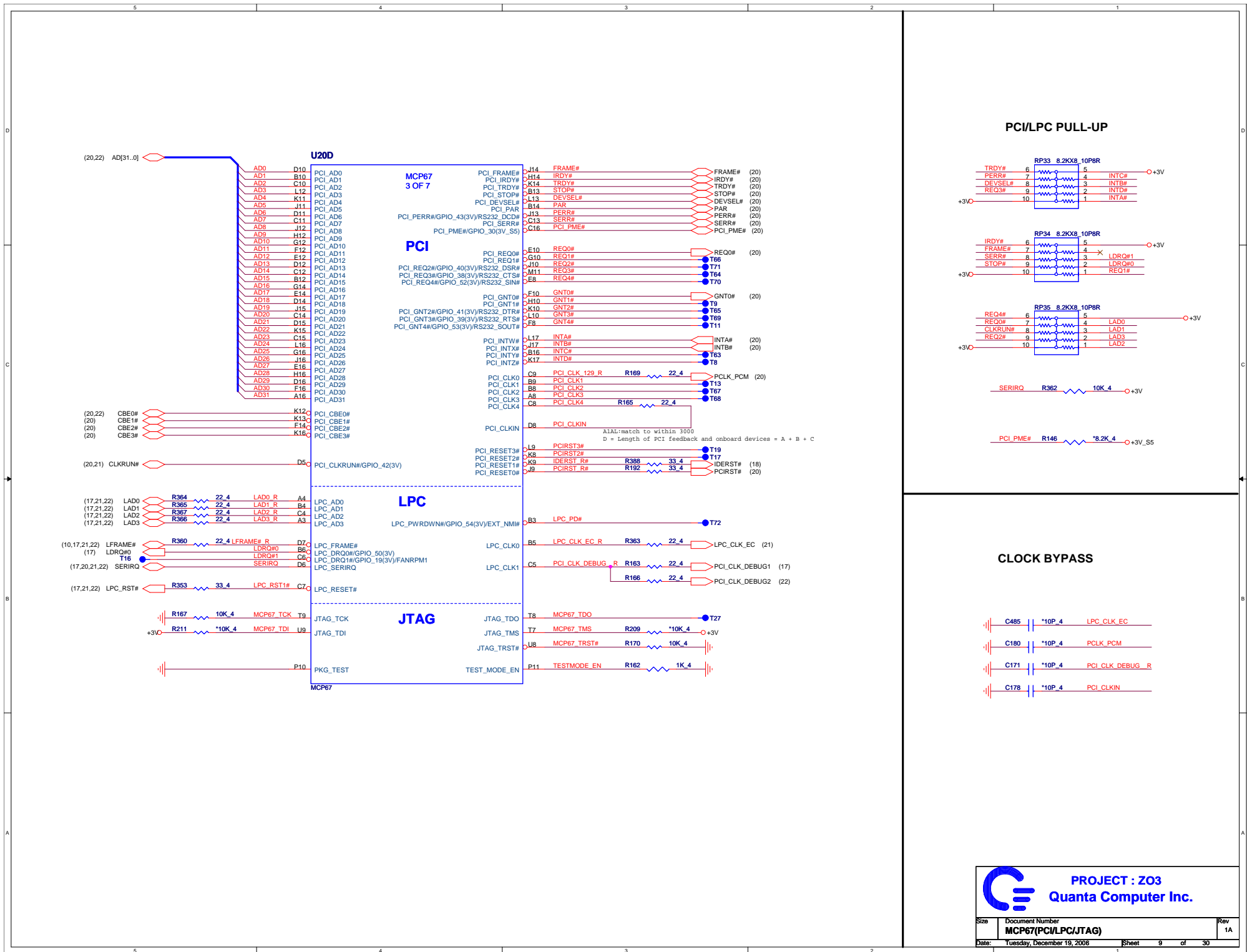
R UMA ONLY
move R168,R139

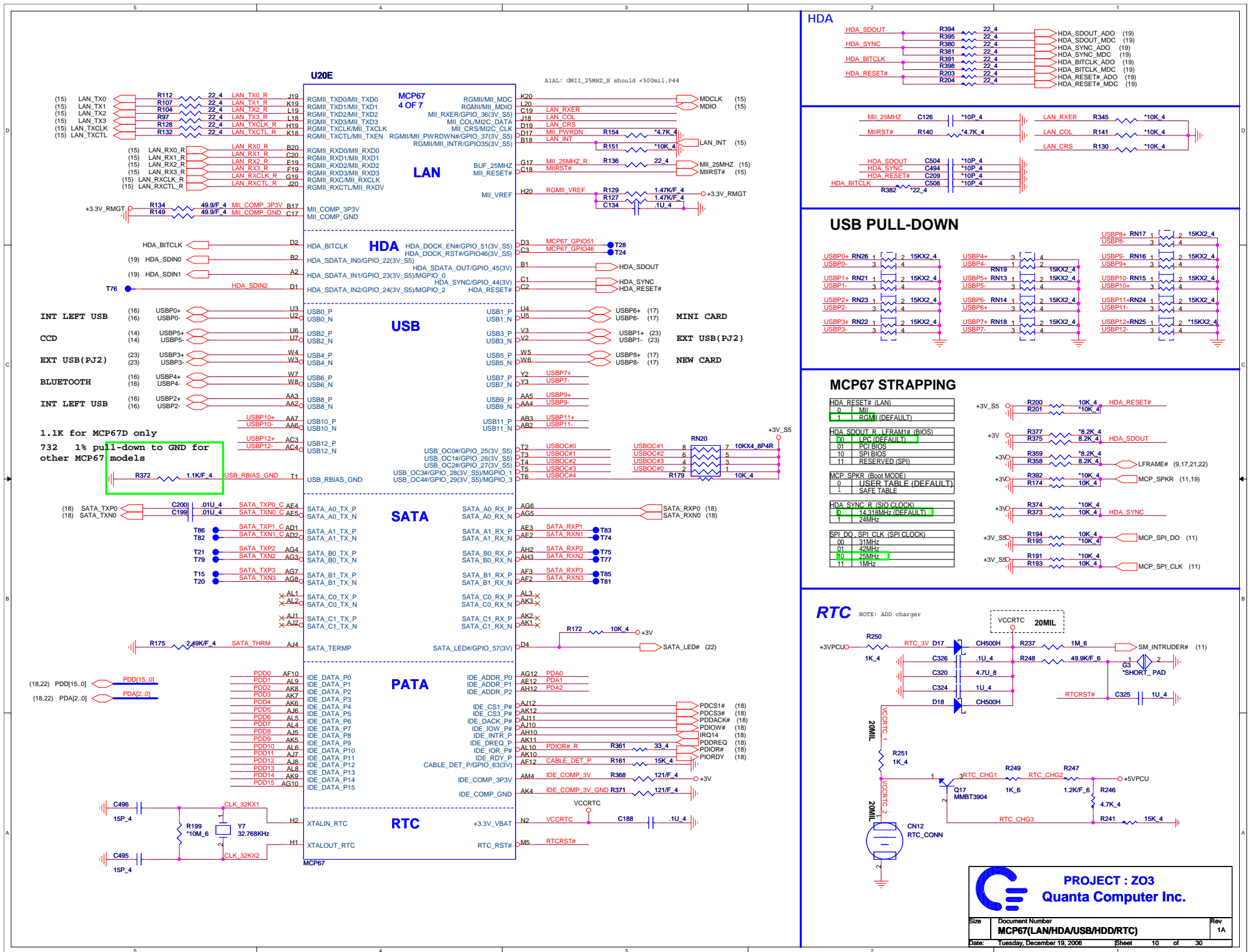
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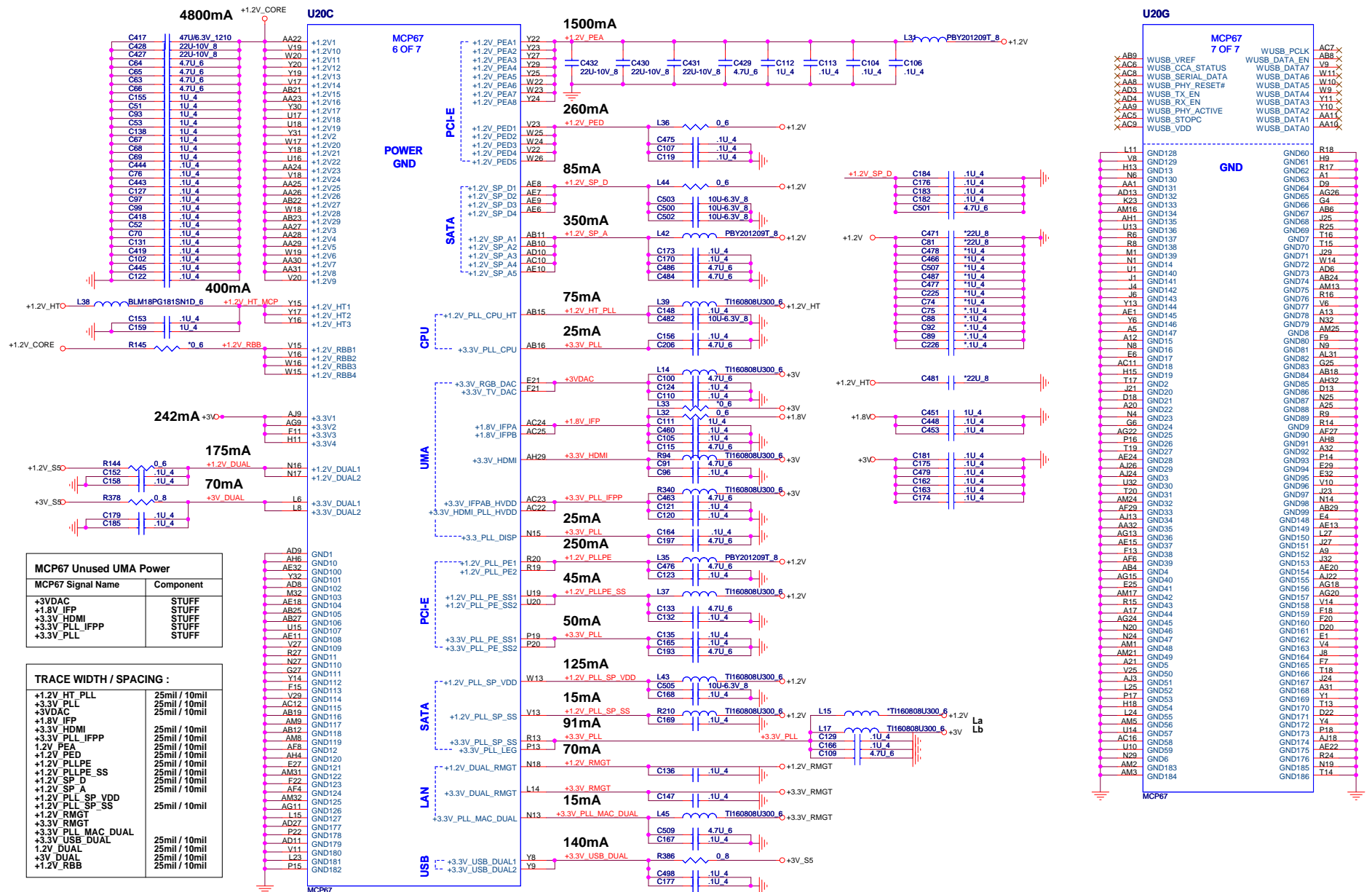
PROJECT : Z03
Quanta Computer Inc.

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	MCP67(HT/VGA/FLAT_PANEL)	1A
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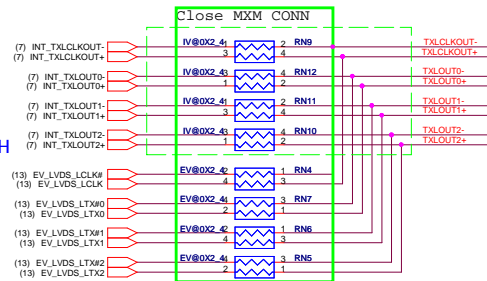


MCP67 POWER PLANE/GND & BYPASS

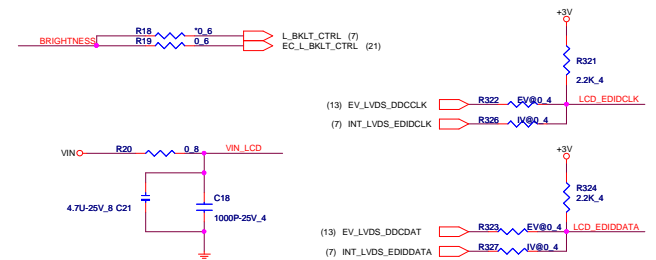
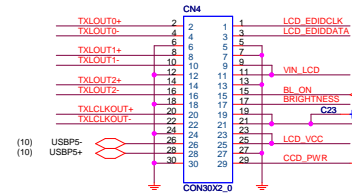


LVDS

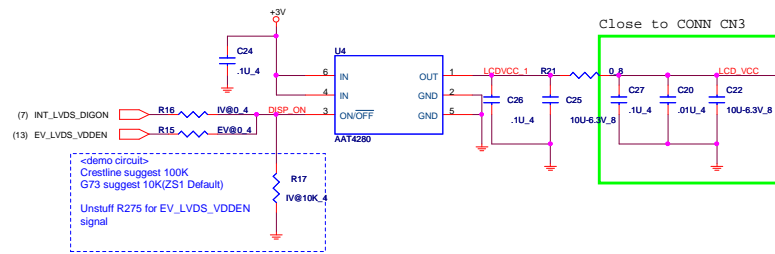
SINGLE_CH



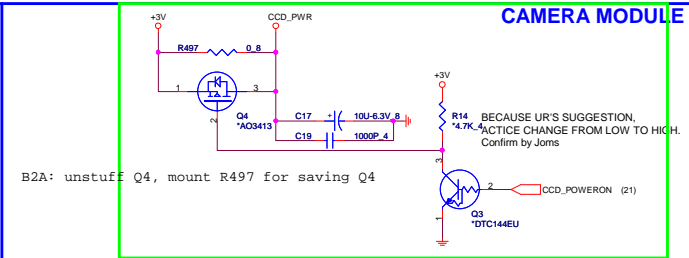
Edison-- 1025 Modify the LVDS pin definition



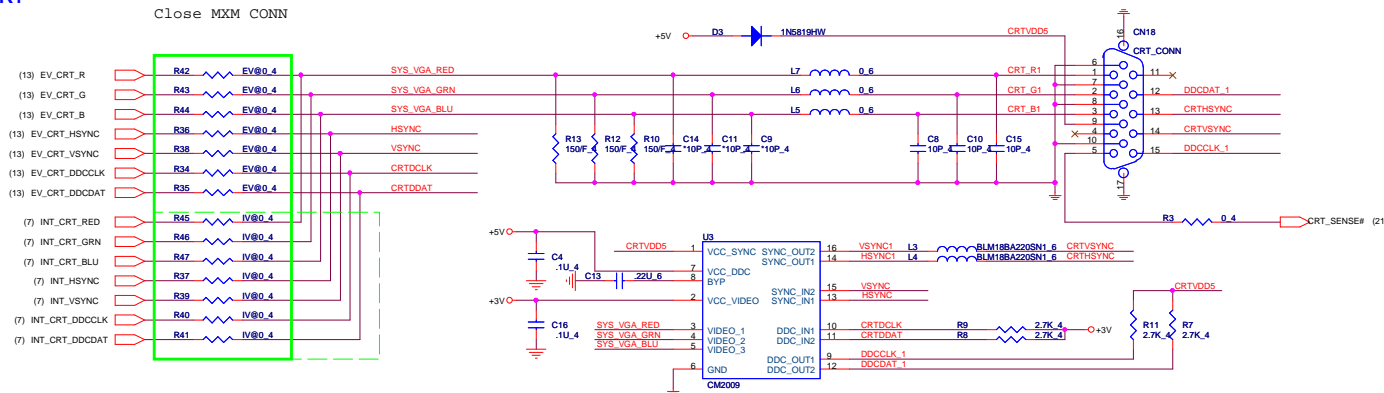
LCD POWER



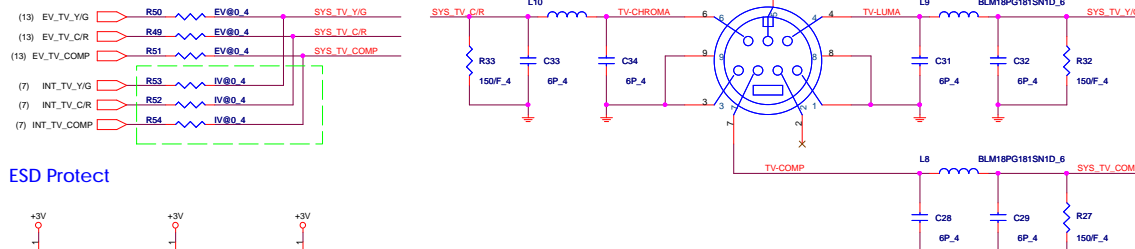
CAMERA MODULE POWER



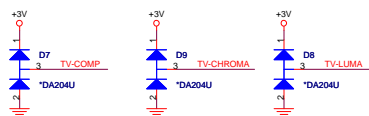
CRT



TV Out (SVHS) MiniDIN 7-pin

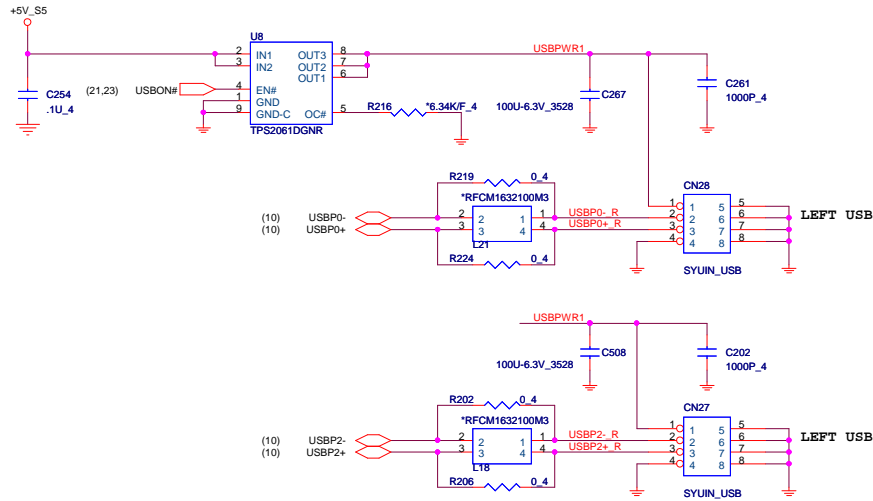


ESD Protect

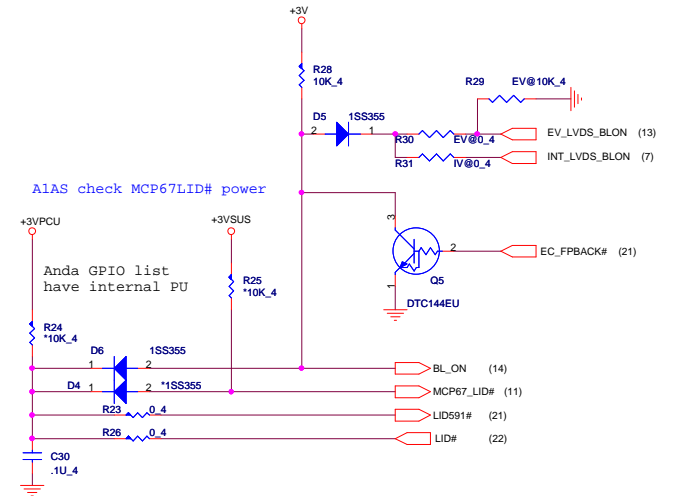


Remove HDMI

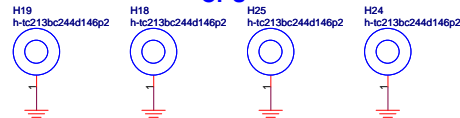
USB MB port



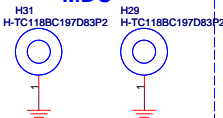
LID SWITCH



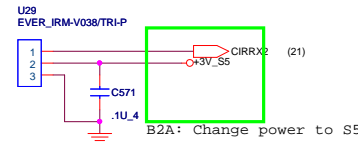
CPU



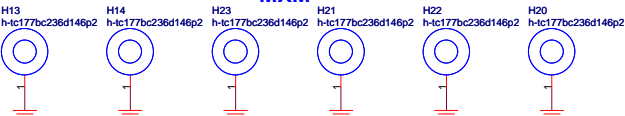
MDC



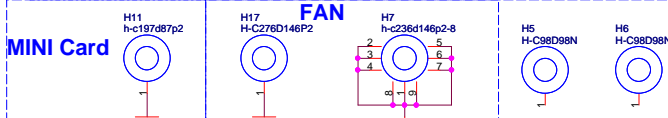
CIR



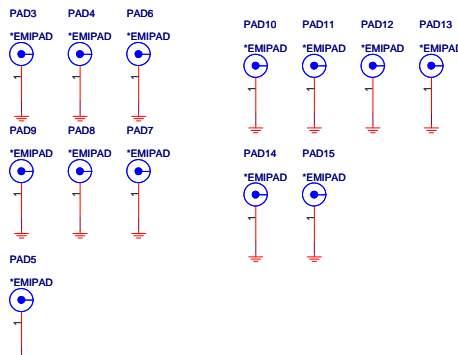
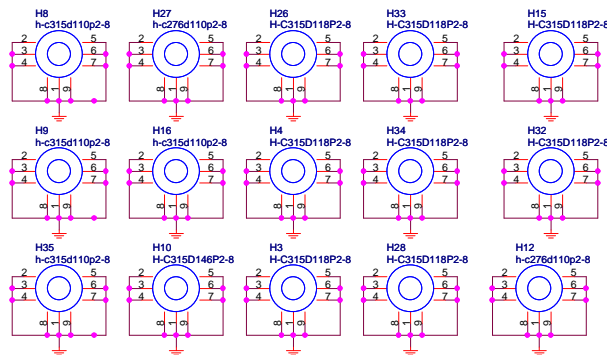
MXM



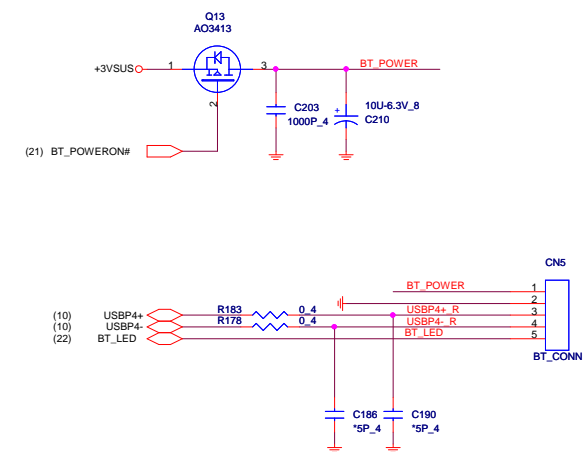
FAN



MINI Card



BLUETOOTH MODULE CONNECTOR



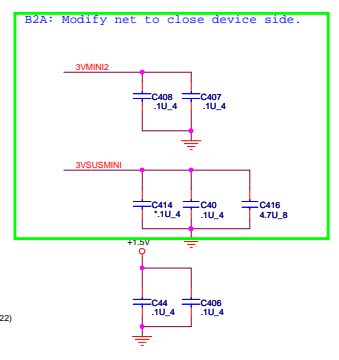
MINI-Card

If M.P must NC all debug R

(9,20,21,22) SERIRQ R316 0.4 SERIRQ RR 51 Reserved 52
 (9) LDRQ0 R317 0.4 LDRQ0 RR 49 Reserved 50
 (9,21,22) LPC_RST# R318 0.4 WCS_DATA 47 Reserved 48
 (9) PCI_CLK_DEBUG1 R319 0.4 WCS_CLKR 45 Reserved 46
 LED_WFPA# 43 Reserved 44
 LED_WLAN# 42 Reserved 43
 GND 40 Reserved 41
 USB_D- 38 Reserved 39
 GND 36 Reserved 37
 USB_D+ 35
 PETp0 33
 SMB_DATA 31
 GND 29
 SMB_CLK 27
 GND 25
 PCI_RXP1 (8) PCI_RXN1 (8) PCI_TXP1 (8) PCI_TXN1 (8)
 (8) CLK_PCIE_MINI1 (8) CLK_PCIE_MINI1# (8)
 (8) MINI_CLKREQ1# (8) MINI_CLKREQ1# (8)
 (11) PCIE_WAKE# (11) PCIE_WAKE# (11)
 Q25 TDC144EU


Need reserve 3G pin define
 Check Footprint

B2A: Modify net to close device side.



New card



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	MINI PCI-E card & NEW CARD	1A	
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[illegible]

Figure 10 shows the pin connections for the MSAKI_SWITCH_4.3 module. The diagram is divided into two main sections: the left side for general control and the right side for specific switch functions.

Left Side Connections:

- LEFT#:** Connected to pin 3 (labeled 1) and pin 4 (labeled 2).
- RIGHT#:** Connected to pin 3 (labeled 1) and pin 4 (labeled 2).
- SCR_UP#:** Connected to pin 3 (labeled 1) and pin 4 (labeled 2).

Right Side Connections:

- SCR_DN#:** Connected to pin 3 (labeled 1) and pin 4 (labeled 2).
- SCR_LEFT#:** Connected to pin 3 (labeled 1) and pin 4 (labeled 2).
- SCR_RIGHT#:** Connected to pin 3 (labeled 1) and pin 4 (labeled 2).

The module is labeled MISAKI_SWITCH_4.3. The internal connections are labeled 1, 2, 3, and 4 for each pin header.

TP CONN

TPDATA (21)
TPCLK (21)

R215 4.7K 4
R214 4.7K 4

+5V

L19 L20 LZA10-2ACB104MT_6_0.1A LZA10-2ACB104MT_6_0.1A

+5V O

L46 BKP160HS181T_6_1.5A

C511 .1U 4

25mil

TP VCC

CN8

1
2
3
4
5
6
7
8
9
10
11
12

RIGHT#
SCR RIGHT#
SCR UP#
SCR LEFT#
SCR DN#
LEFT#

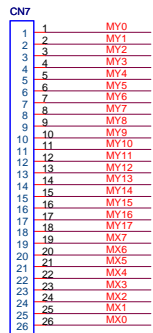
TPDATA C231 *10P 4
TPCLK C224 *10P 4

TOUCH_PAD_TP_12P

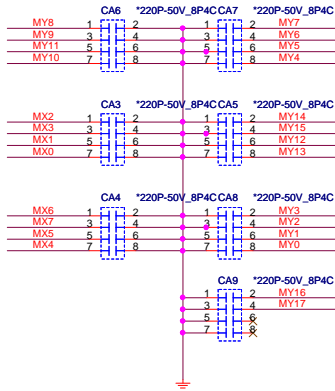
The schematic diagram illustrates the internal components and connections of the PDA module. Key components include a DTC144EU transistor (Q19) connected to a +3V supply and a +5V supply through resistors R284 and R290. The transistor's emitter is connected to ground. The base is connected to the PDD module's PDD8 pin. The collector is connected to the PDD module's PDD9 pin. The PDA module also includes a 10K_4 resistor (R271) connected to the +3V supply and a 100mF capacitor (C330) connected to ground. The PDA module is connected to the PDD module via a 10K_4 resistor (R274) and a 100mF capacitor (C331). The PDA module is also connected to the PDCS module via a 10K_4 resistor (R276) and a 100mF capacitor (C332). The PDA module is connected to the PDCS module via a 10K_4 resistor (R275) and a 100mF capacitor (C333). The PDA module is connected to the PDCS module via a 10K_4 resistor (R276) and a 100mF capacitor (C332). The PDA module is connected to the PDCS module via a 10K_4 resistor (R275) and a 100mF capacitor (C333).

INT K/B

(21,23) MY[17..0]
(21,23) MX[7..0]

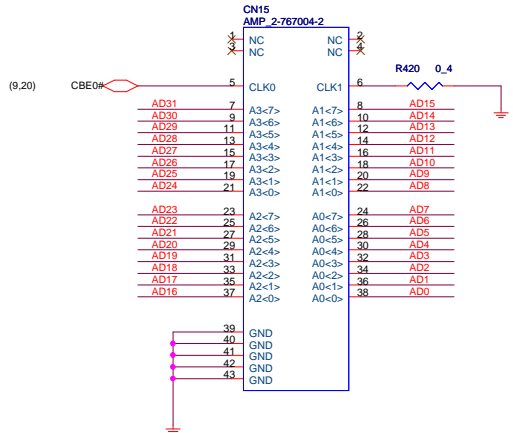


FFC_26P_KB

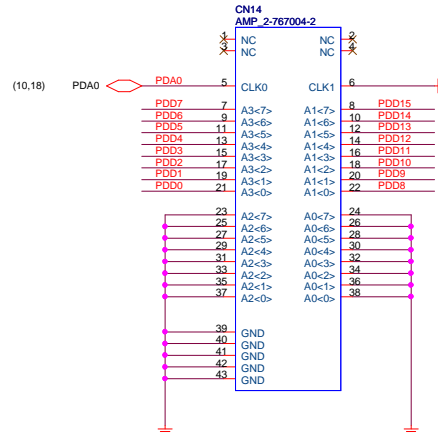


Debug

(9,20) AD[31..0]

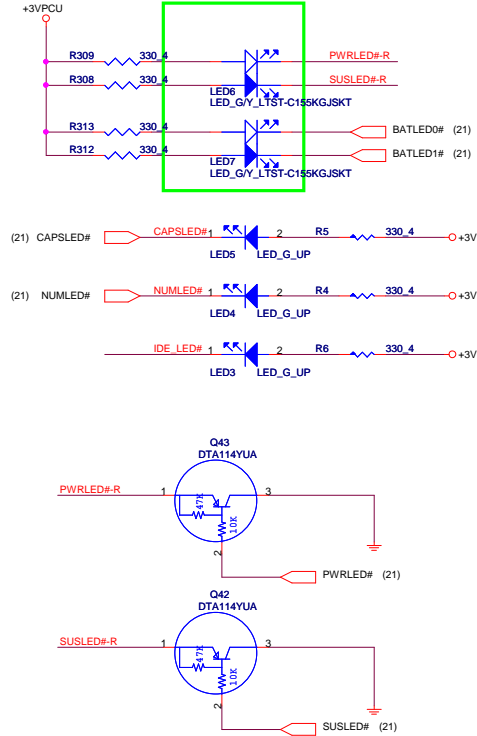


(10,18) PDD[15..0]

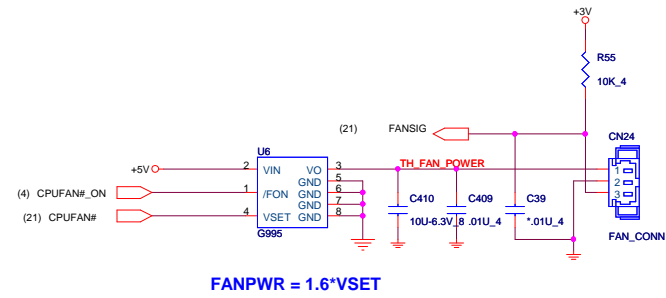


LED

10/16:Changed. Follow BL3 LED

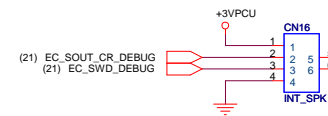


CPU FAN

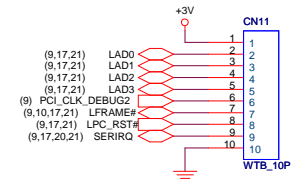


DEBUG PORT

EC Debug Port



Reserved for LPC debug card



Button

BUTTON MATRIX

MY0	
MX1	MAIL
MX2	WWW
MX4	WIRELESS
MX5	BLUETOOTH

