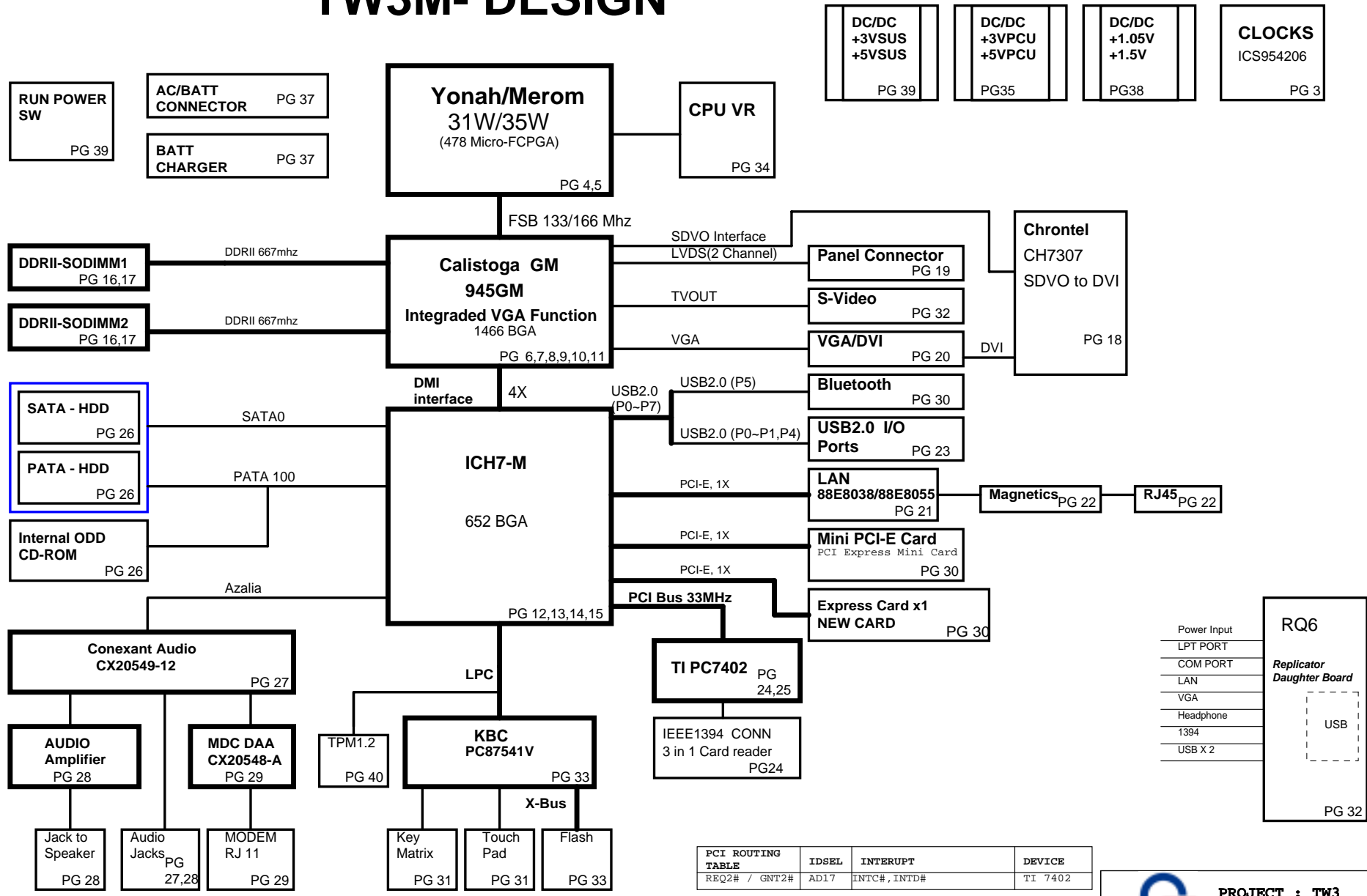


PCB STACK UP

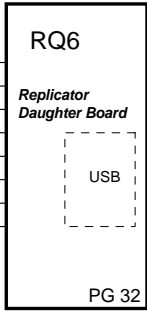
- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT


TW3M- DESIGN



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ2# / GNT2#	AD17	INTC#, INTD#	TI 7402

- Power Input
- LPT PORT
- COM PORT
- LAN
- VGA
- Headphone
- 1394
- USB X 2





PROJECT : TW3
Quanta Computer Inc.

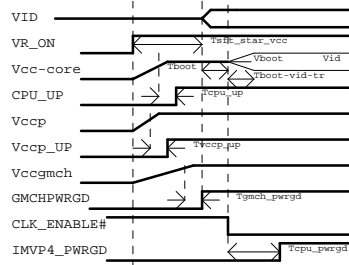
Size	Document Number	Rev
	Block Diagram	B2A
Date:	Tuesday, January 03, 2006	Sheet 1 of 46

Board Stack up Description

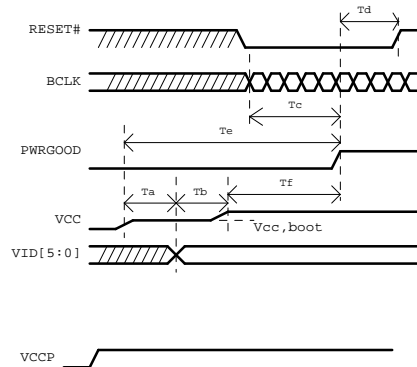
PCB Layers

Layer 1		TOP (Component, Other)
Layer 2		Ground Plane
Layer 3		IN1
Layer 4		IN2
Layer 5		Power Plane
Layer 6		IN3
Layer 7		Ground Plane
Layer 8		BOTTOM

Power On Sequencing Timing Diagram



Dothan Power-up Timing Specifications

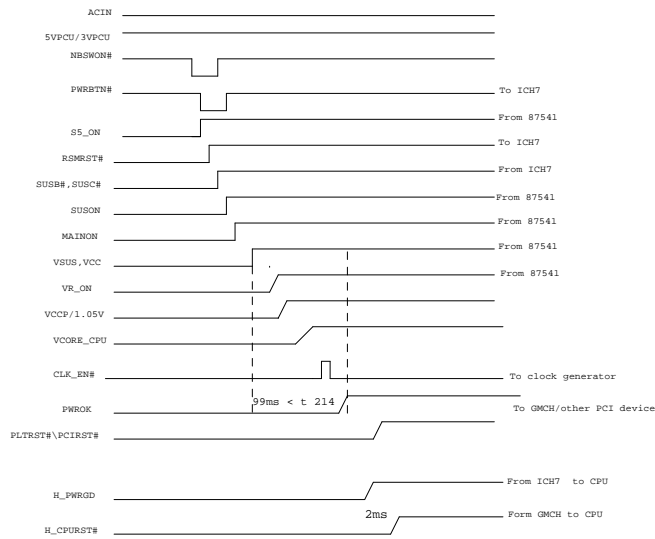


Ta=VCC and VCCP assertion to VID[5:0] valid
 Tb=VID[5:0] stable to VCC valid
 Tc=BCLK stable to PWRGOOD assertion
 Td=PWRGOOD to RESET# de-assertion time
 Te=Vcc,boot valid to PWRGOOD assertion time

Voltage Rails

Voltage Rails	ON S0-S2	ON S3	ON S4	ON S5	Control signal
VCC CORE Core voltage for Processor	X				VR_ON 0.726V~0.94V
VCCP Core voltage for CPU / NB	X				VR_ON
SMDDR_VTERM0.9V for DDR2 Termination voltage	X				MAINON
RVCC1.5	X	X	X		RVCC_ON
RVCC3	X	X	X		RVCCD
VCC1.5	X				MAIND
VCC2.5	X				MAINON
VCC3	X				MAIND
VCC5	X				MAIND
1.8VSUS	X	X			SUSON
3VSUS	X	X			SUSD
5VSUS	X	X			SUSD
3VPCU	X	X	X	X	VL
5VPCU	X	X	X	X	VL
9VPCU	X	X	X	X	5VPCU

ACIN POWER ON TIMING



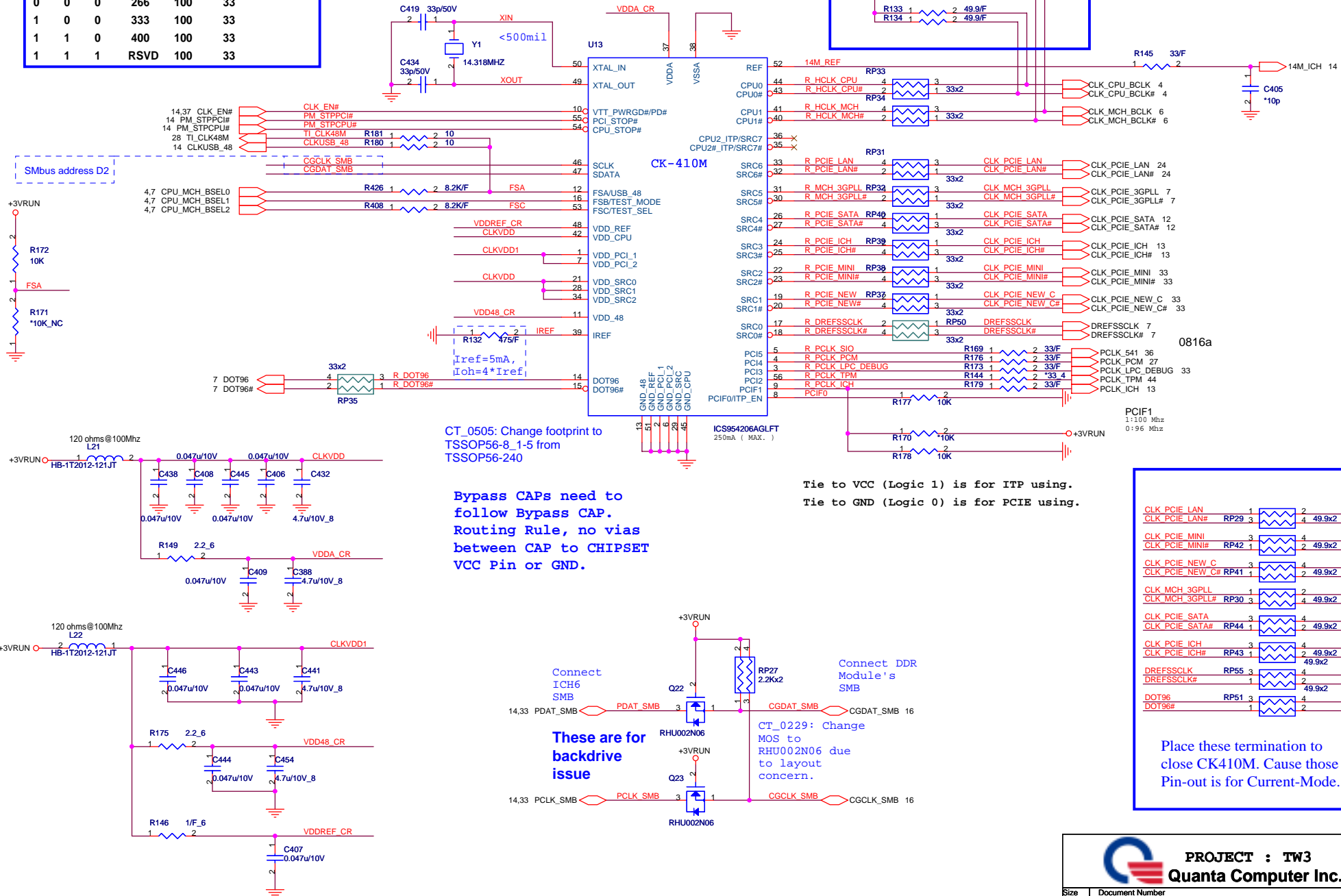
Voltage Rails	ON S0-S1	ON S3	ON S4	ON S5	Control signal
VCC CORE Core voltage for Processor	X				VRON
GMCH VTT Core voltage for GMCH 1.05V	X				MAINON
SMDDR_VTERM 0.9V for DDR II Termination voltage	X				MAINON
SMDDR_VREF 0.9V for DDR II Reference Voltage	X				MAINON
GMCH 1.5V	X				MAINON
1.8VSUS 1.8V for DDR II voltage	X	X			SUSON
2.5V	X				MAINON
3VPCU	X	X	X	X	VL
5VSUS	X	X			SUSON
5V	X				MAINON
4VPCU	X	X	X	X	VL
5VSUS	X	X			SUSON
5V	X				MAINON
VR	X	X	X	X	

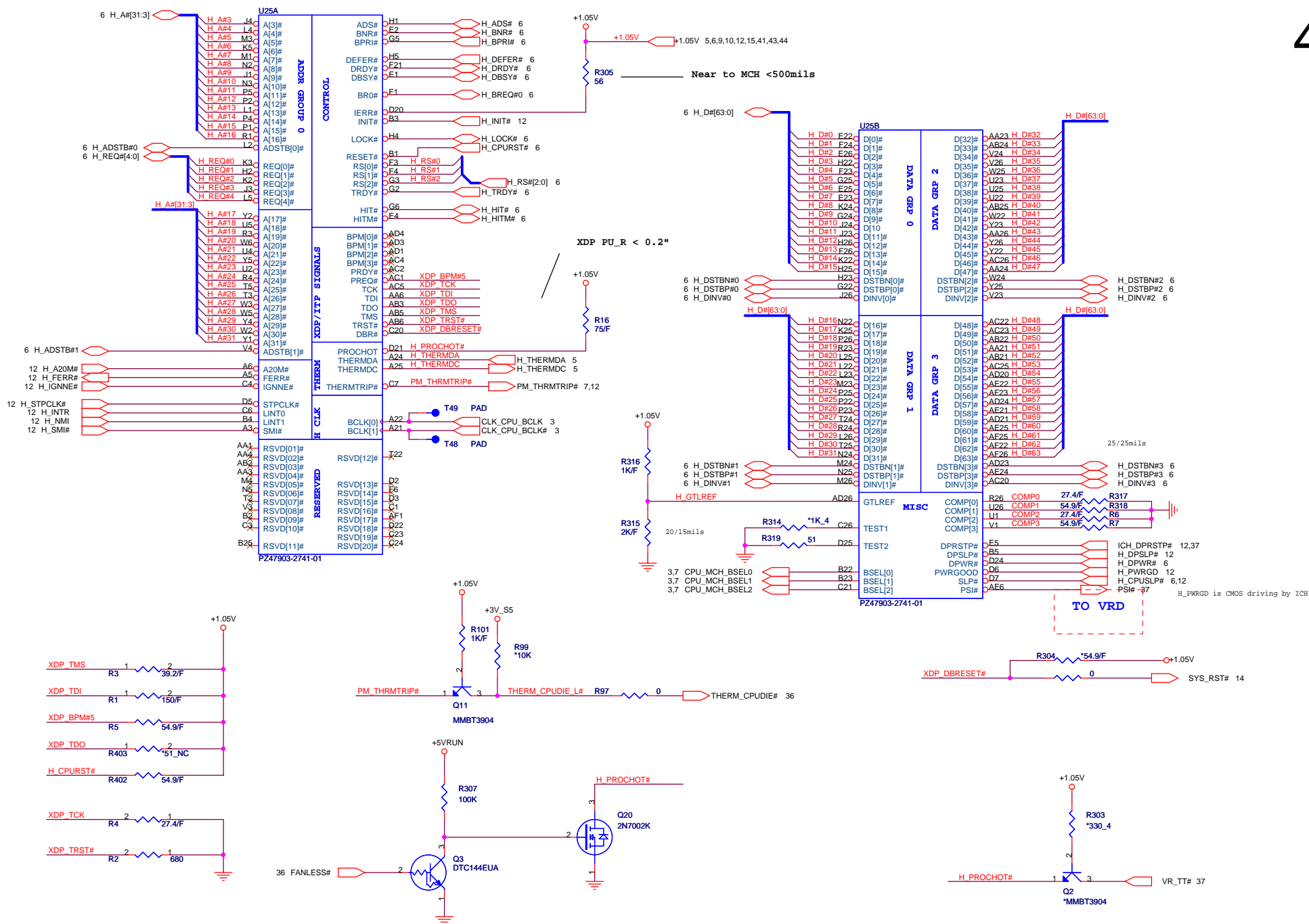
PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI#402	AD17	REQ2# / GNT2#	PIRQ CD

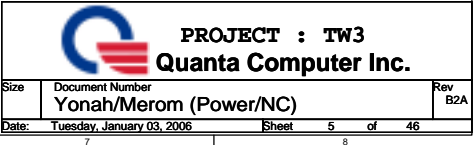
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

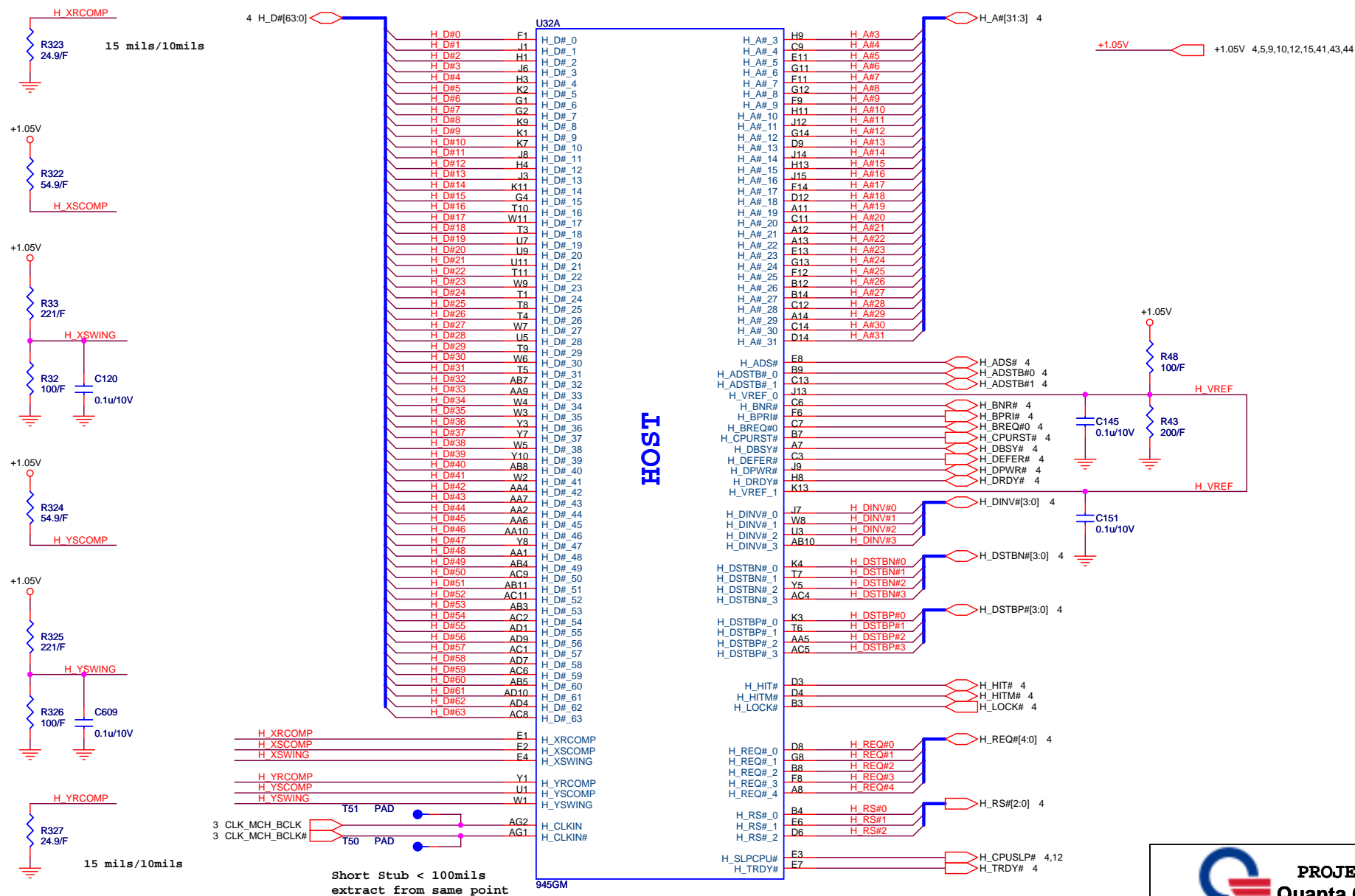
Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.

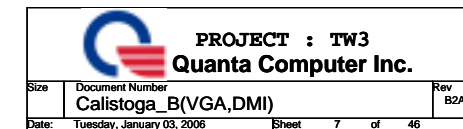
3

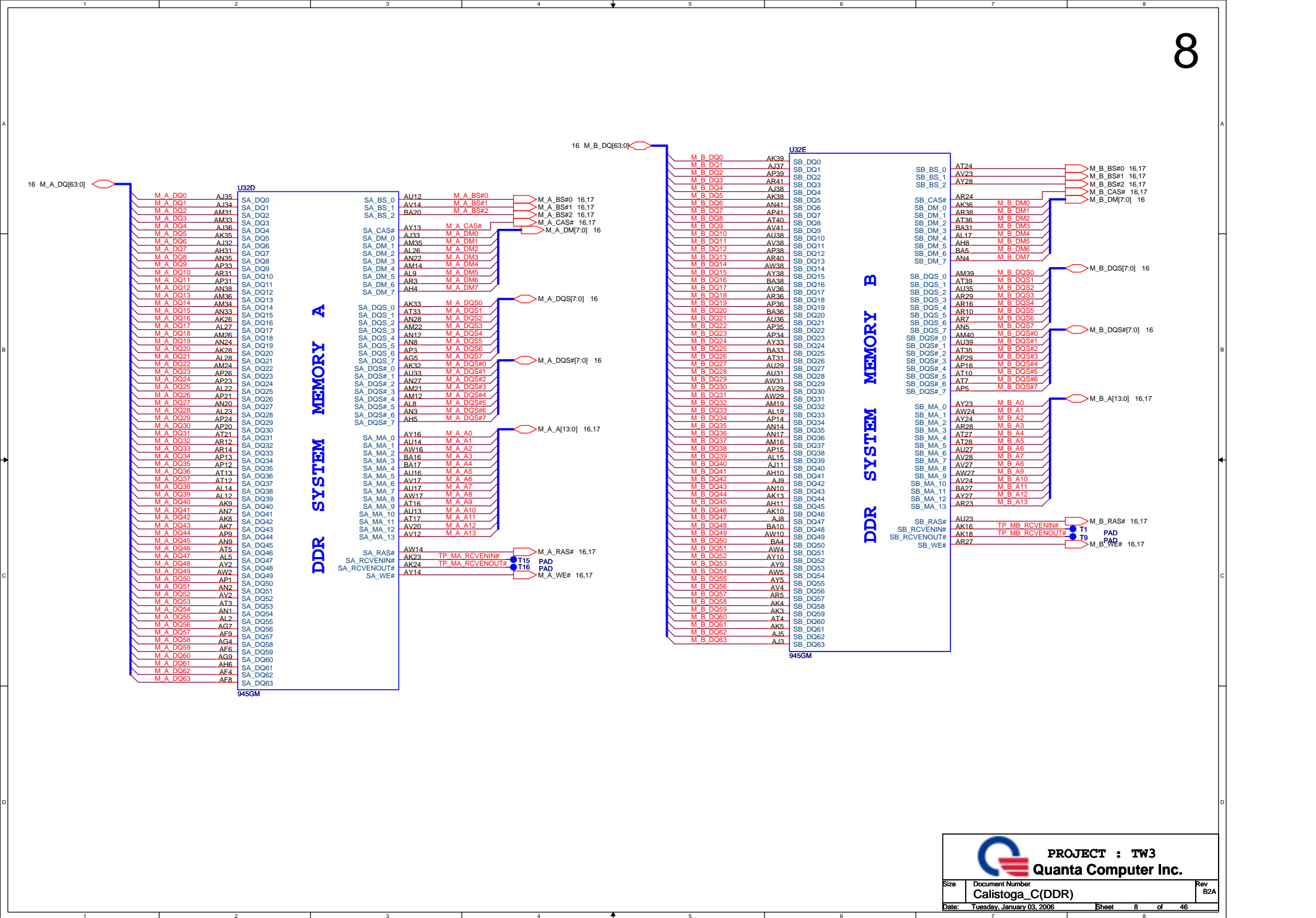


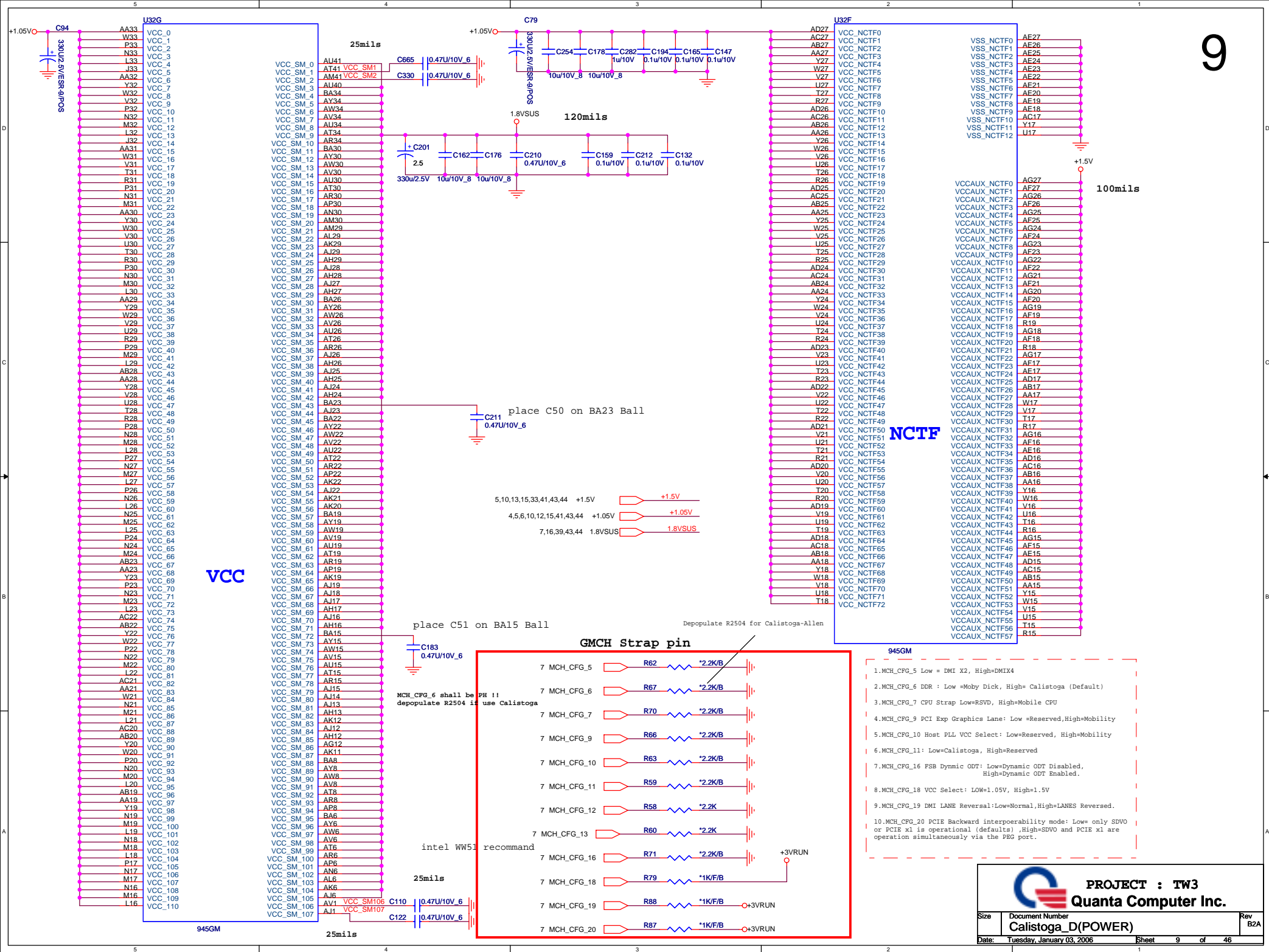


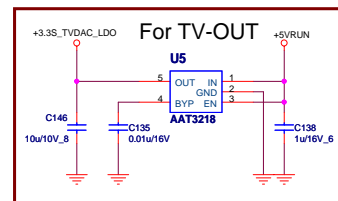
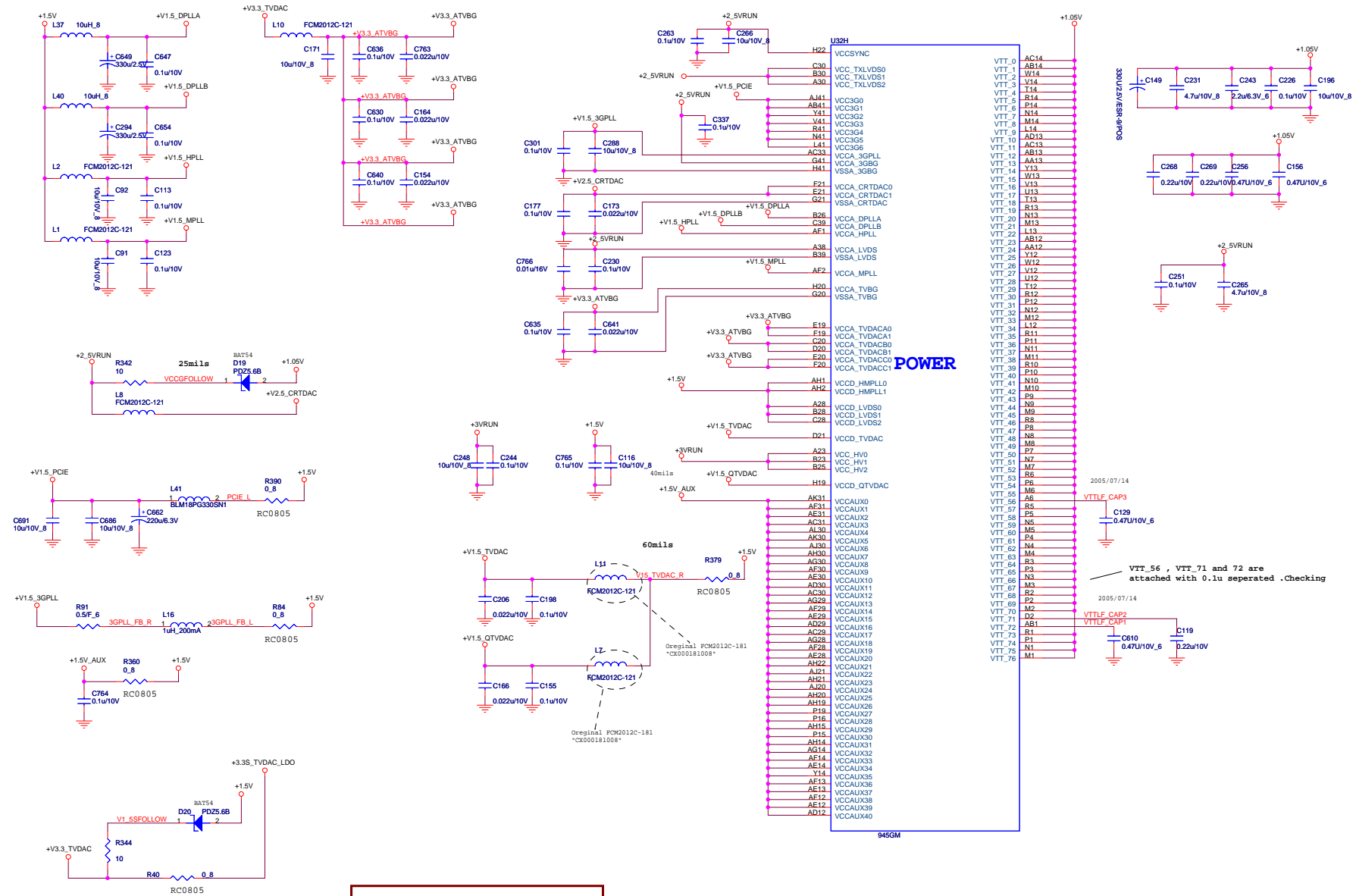


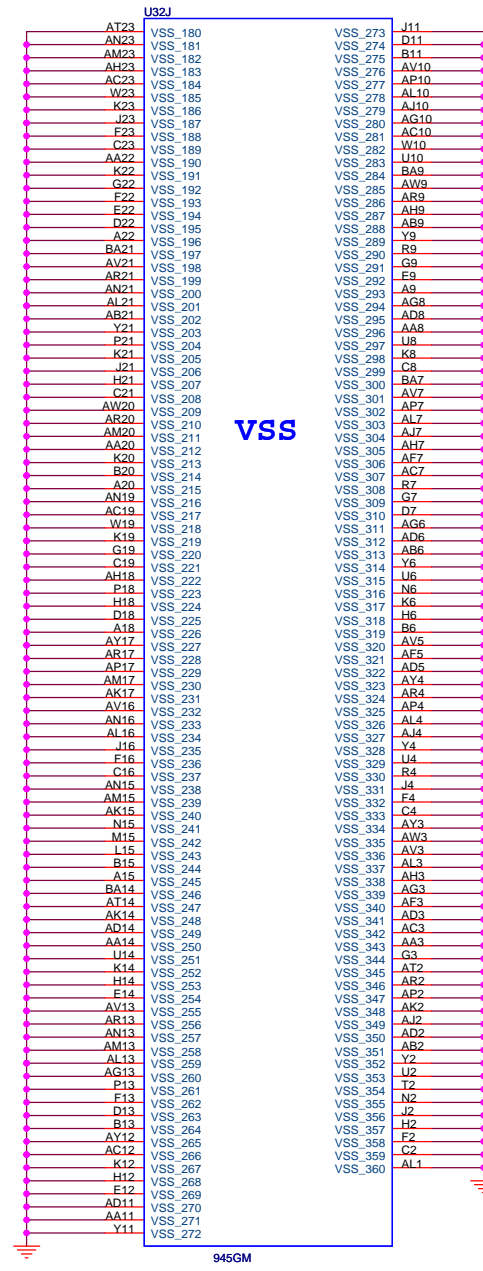
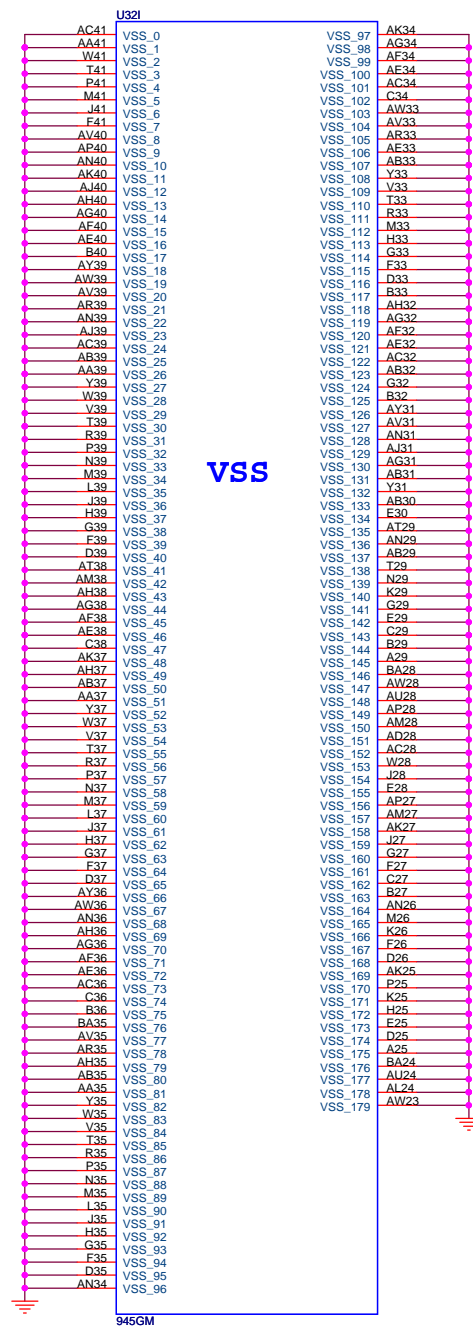


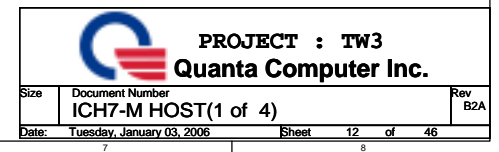






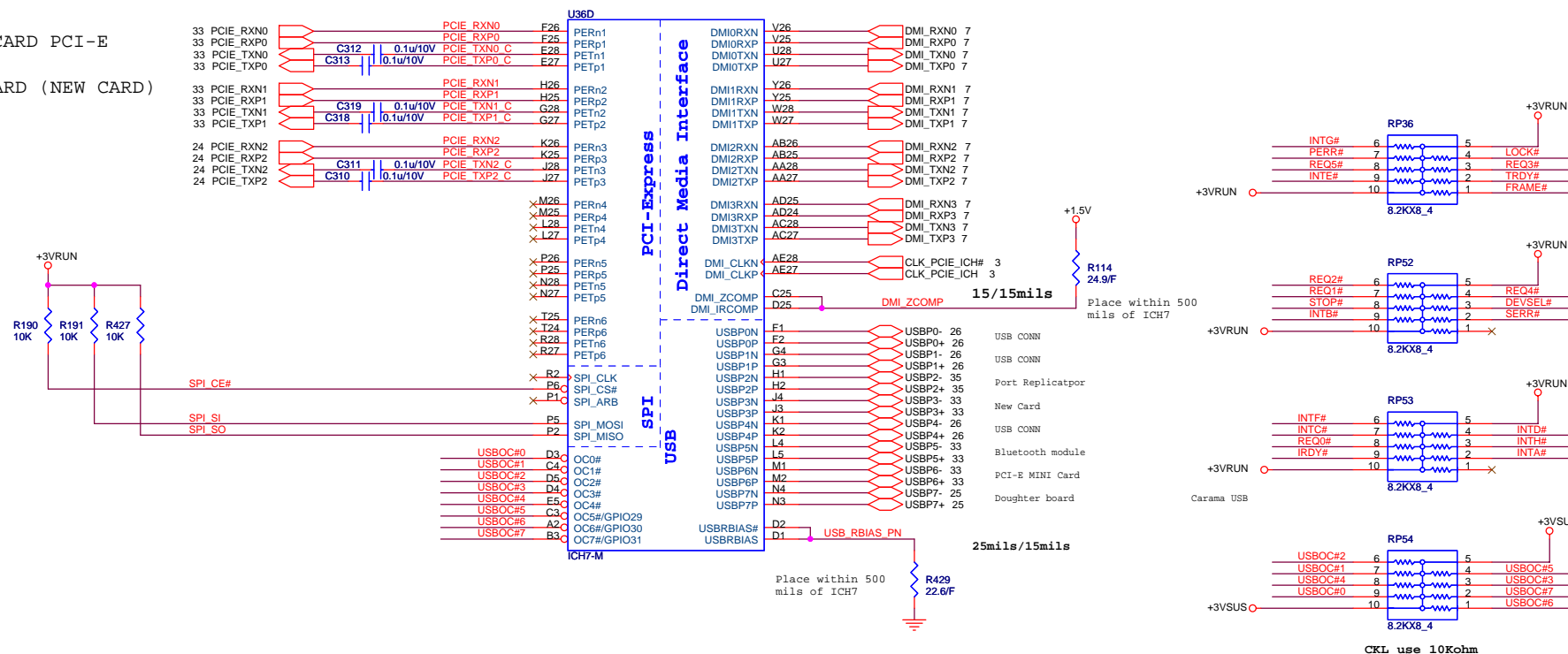






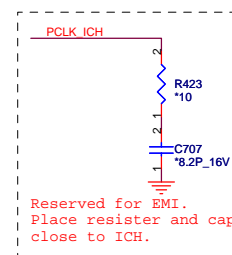
MINI CARD PCI-E

EXPRESS CARD (NEW CARD)



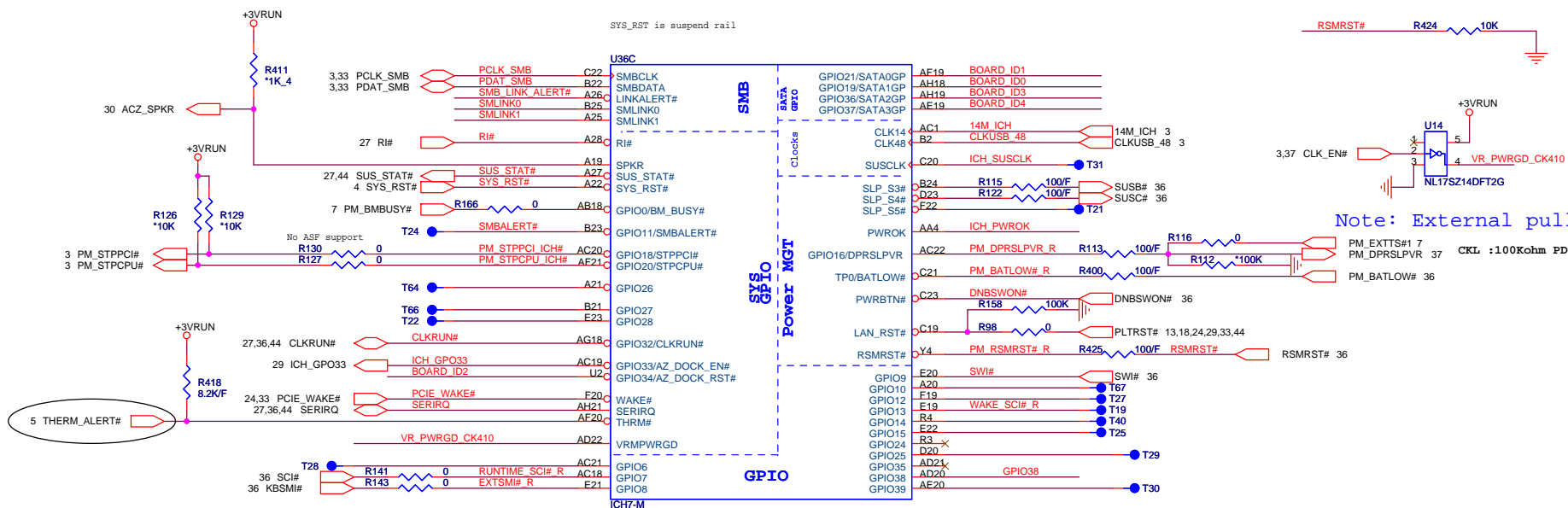
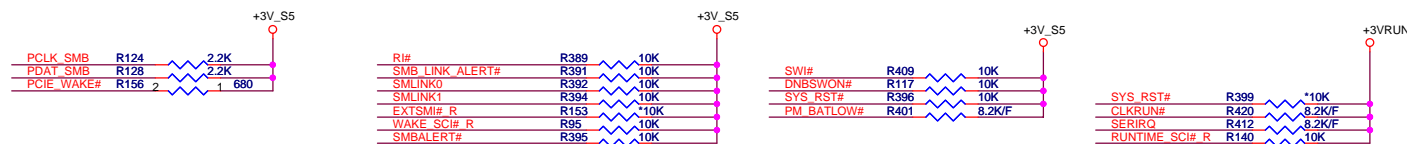
ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF



R376

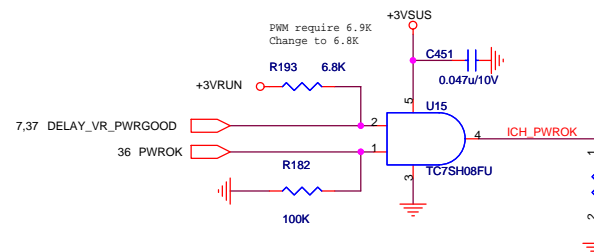
No stuff-->boot
Stuff-->No boot



Note: External pull-up 3V

PM_EXTTS#1 7 CKI :100Kohm PD

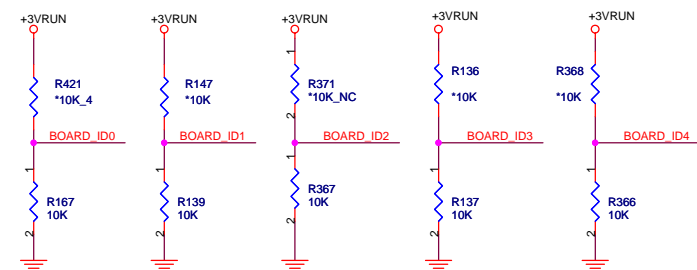
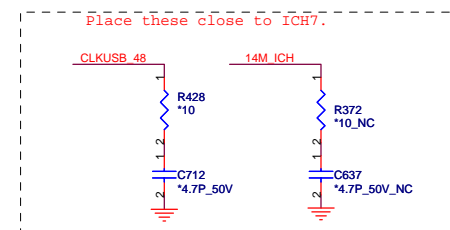
GPI025 /Suspend rail is a HW strap , don't pull down .

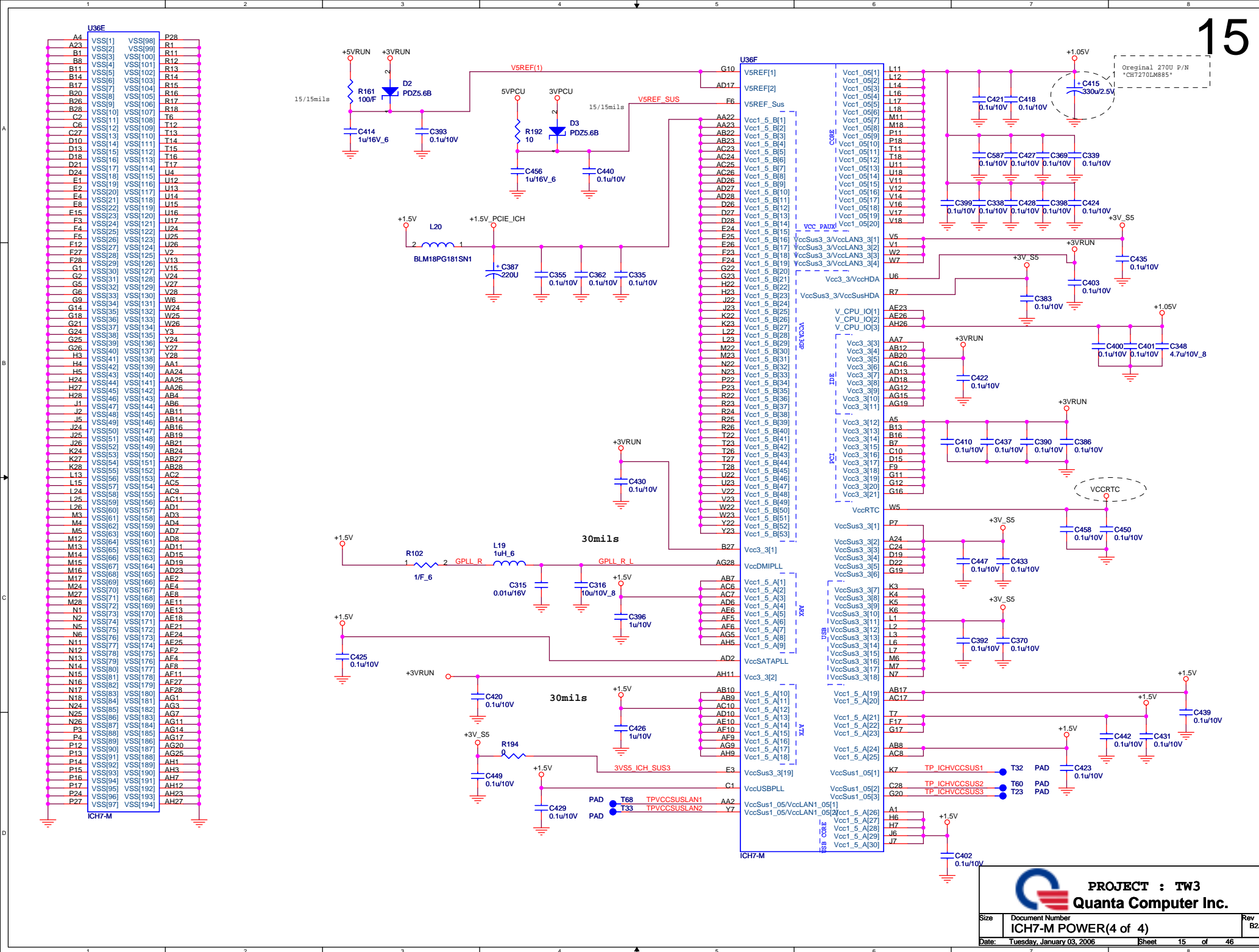


Level is incorrect !!

GPI038	Function
High	CRT
Low	DVI

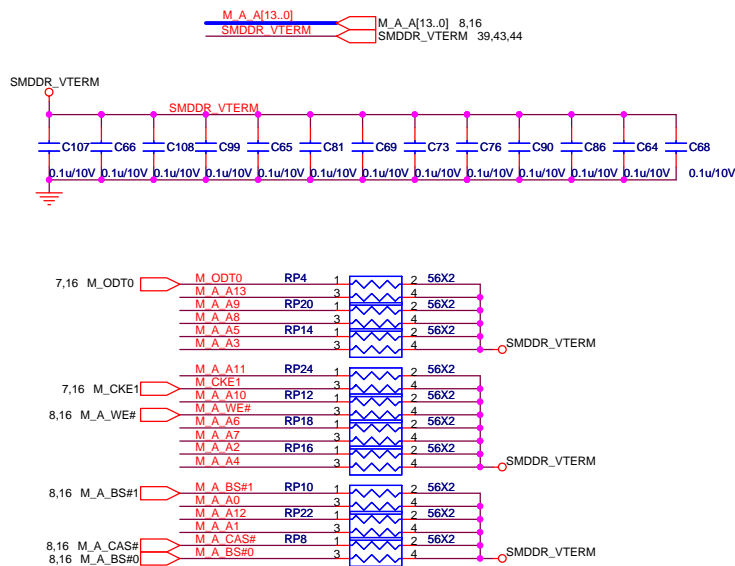
Board ID	Function
ID [1:0]	00: TW3 01: DW1
ID2	0: SATA HDD 1: PATA HDD
ID [4:3]	Reserve



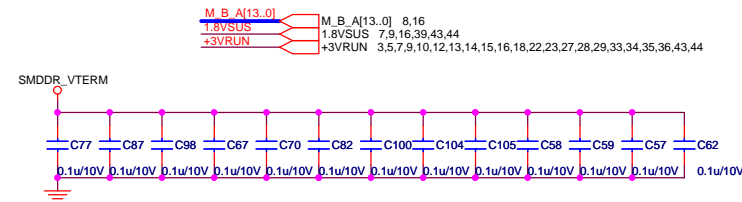


DDRII DUAL CHANNEL A,B.

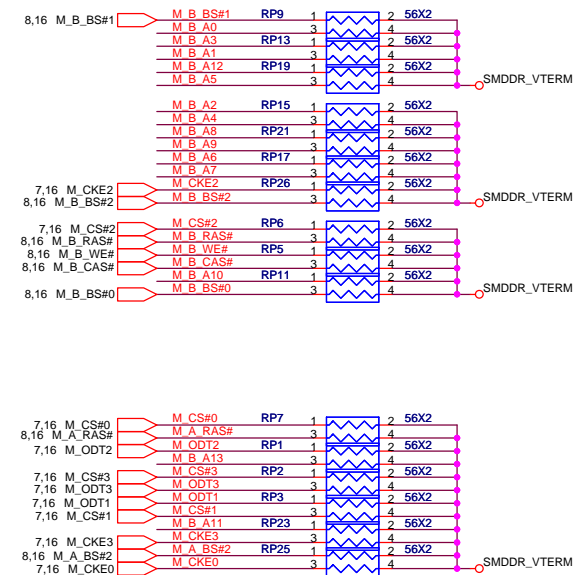
DDR II A CHANNEL



DDR II B CHANNEL

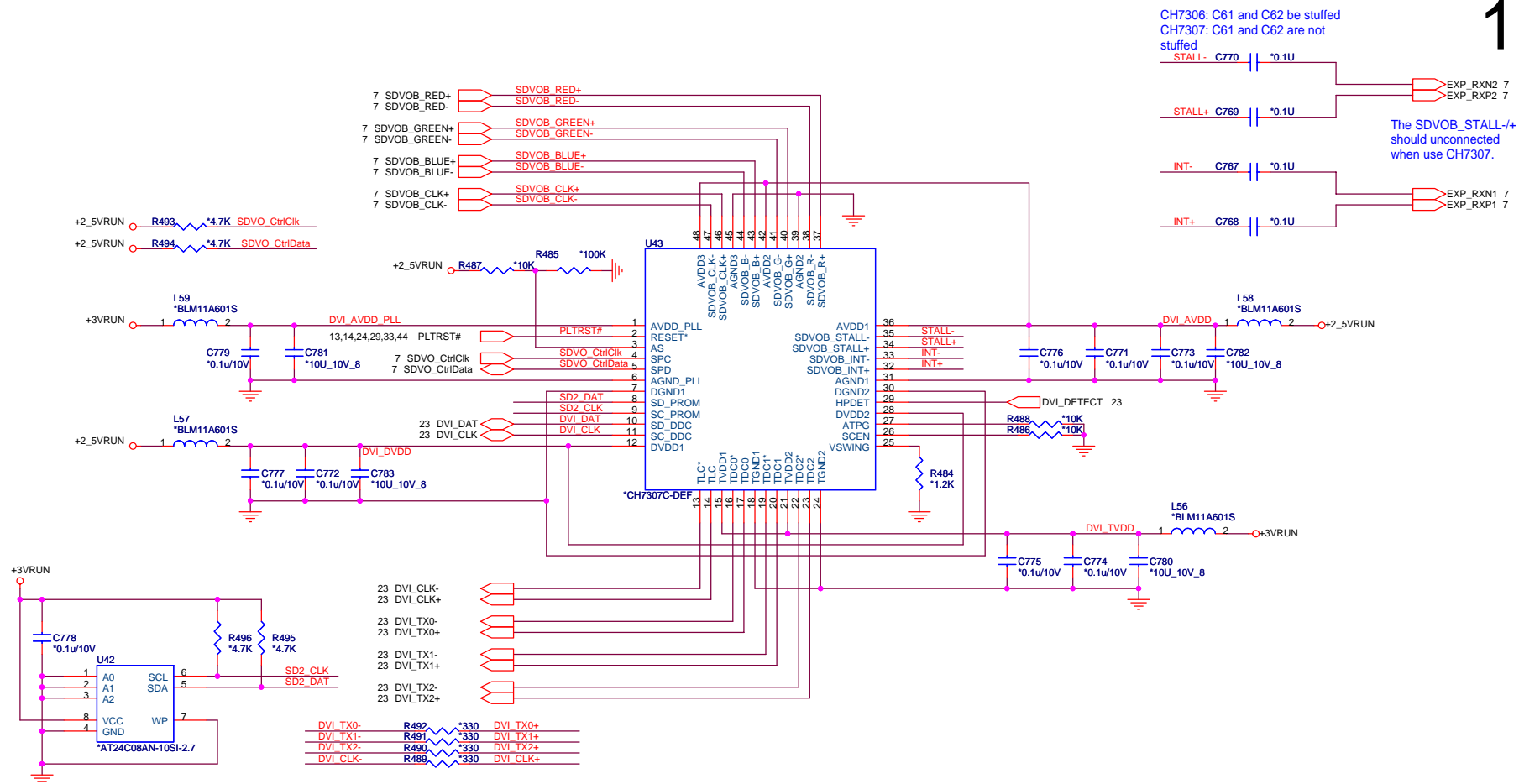


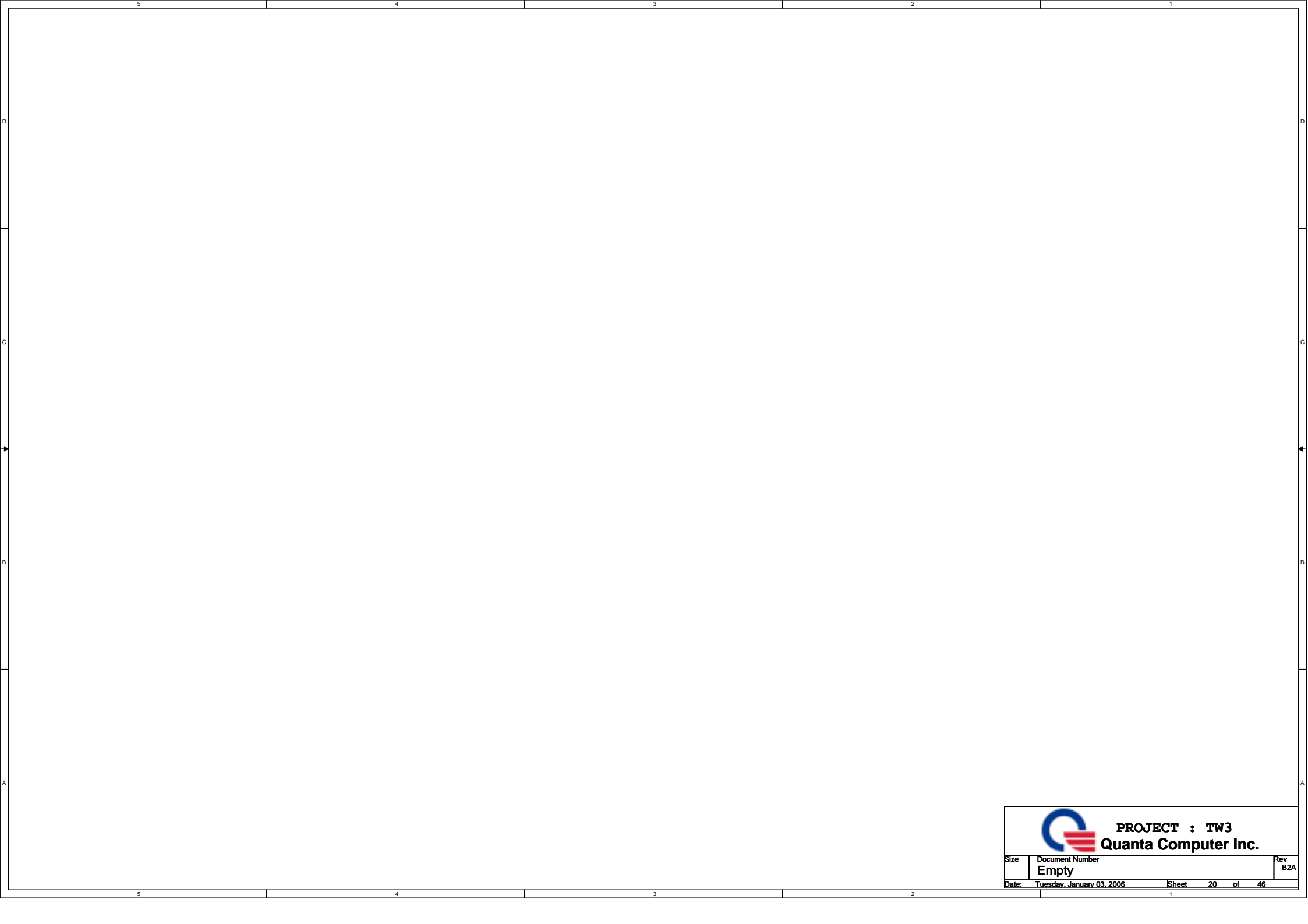
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM




GMCH SDVO Signal to DVI Signal Bridge

18







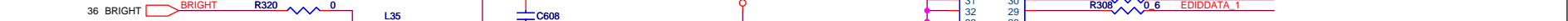
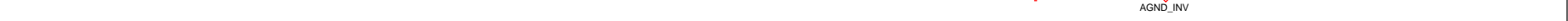
PROJECT : TW3
Quanta Computer Inc.

Size	Document Number			Rev
	Empty			B2A
Date:	Tuesday, January 03, 2006		Sheet	20 of 46
				1



PROJECT : TW3
Quanta Computer Inc.

Size	Document Number Empty	Rev B2A
Date:	Tuesday, January 03, 2006	Sheet 21 of 46

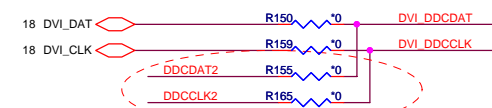
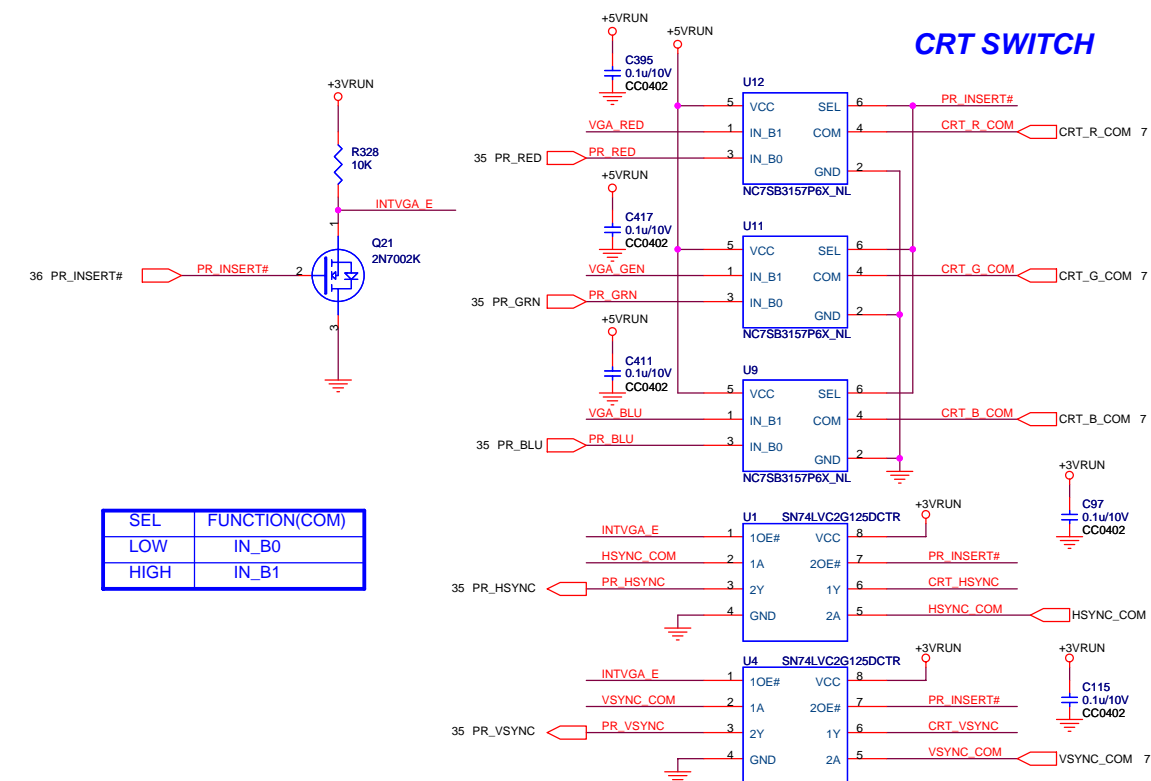
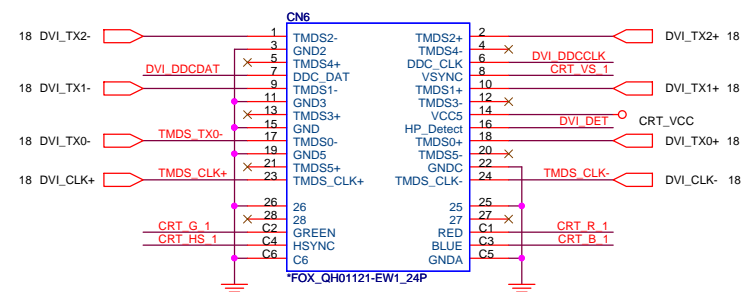
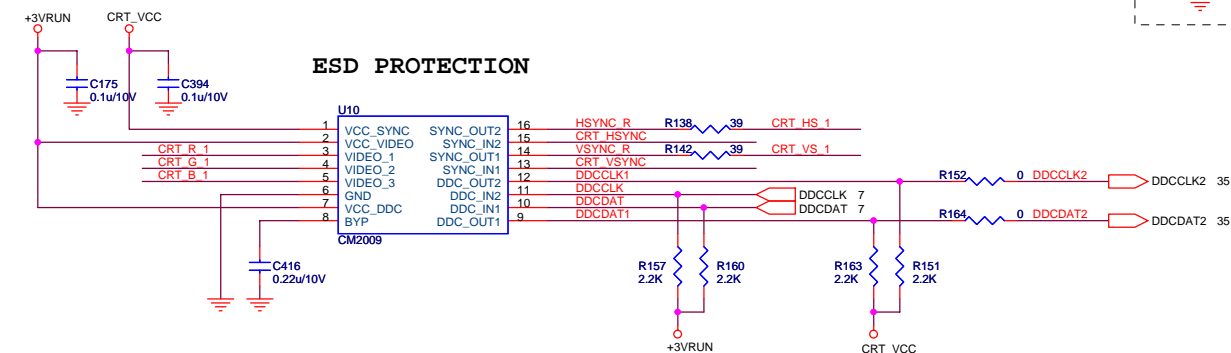
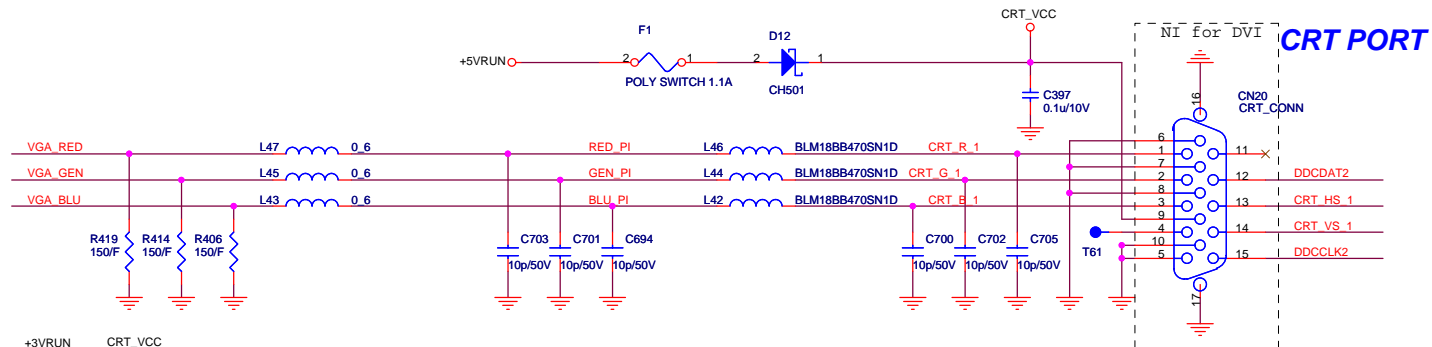


Inverter Interface

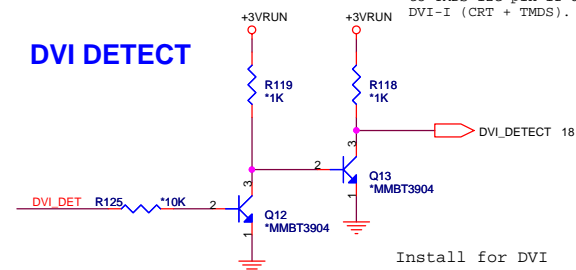


AA14280_3

Size Document Number Rev



DVI DETECT



Install for DVI

C: 88E8053 LF PN: AJ080530010 (20050414)

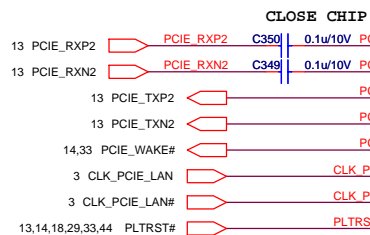
1Mbps

C: Add 9 x GND Pad for LAN controller.
(20050411)

C: Add these GND pin for via hole to GND Plane.

C: Add RC (R37 change to 200K, Add C101) delay to
control LOM_DISABLE#. (20050411)C: Reserve R36. Change
LANRST# to PCIRST# source
from MB option
modify. (2005/04/11)

DELAY PIN10 AT LEAST 150ms



88E8038/88E8055

T58 PAD LAN_SMB_CLK
T59 PAD LAN_SMB_DATALANVCC L38 HI0805R800R-10
120 ohms@100Mhz

C253 22u/10V_8

C646 4.7u/10V_8

C221 0.1u/10V

R77 4.7K

C: Widen to 20 mils. AVDD25 to
20 mils. (20050411)

Q9 2SA1797T100Q

C642 4.7u/10V_8

C215 0.1u/10V

C: Widen to 20 mils. VDD to 20
mils. (20050411)

Q10 2SA1797T100Q

C645 10u/10V_8

C220 0.1u/10V

C: Widen to 20 mils. VDD to 20
mils. (20050411)

C344 0.1u/10V

C292 0.1u/10V

C346 0.1u/10V

C289 0.1u/10V

C340 0.1u/10V

C343 1000p/50V

C345 1000p/50V

C290 1000p/50V

C291 1000p/50V

C293 1000p/50V

LANVCC

PLACEMENT CLOSE TO EACH OTHER

LANVCC L39 HI0805R800R-10
120 ohms@100Mhz

C644 4.7u/10V_8

C222 0.1u/10V

R78 4.7K

C: Widen to 20 mils. VDD to 20
mils. (20050411)

Q9 2SA1797T100Q

C642 4.7u/10V_8

C215 0.1u/10V

C: Widen to 20 mils. VDD to 20
mils. (20050411)

Q10 2SA1797T100Q

C645 10u/10V_8

C220 0.1u/10V

C: Widen to 20 mils. VDD to 20
mils. (20050411)

C344 0.1u/10V

C292 0.1u/10V

C346 0.1u/10V

C289 0.1u/10V

C340 0.1u/10V

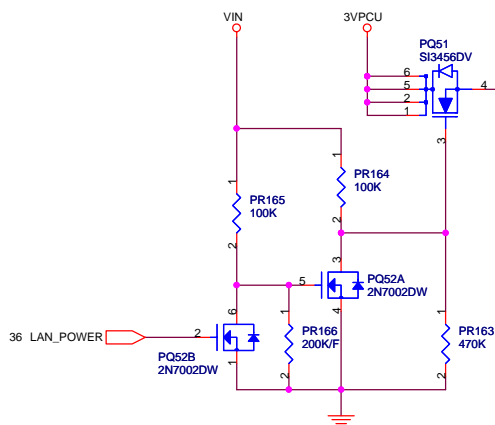
C343 1000p/50V

C345 1000p/50V

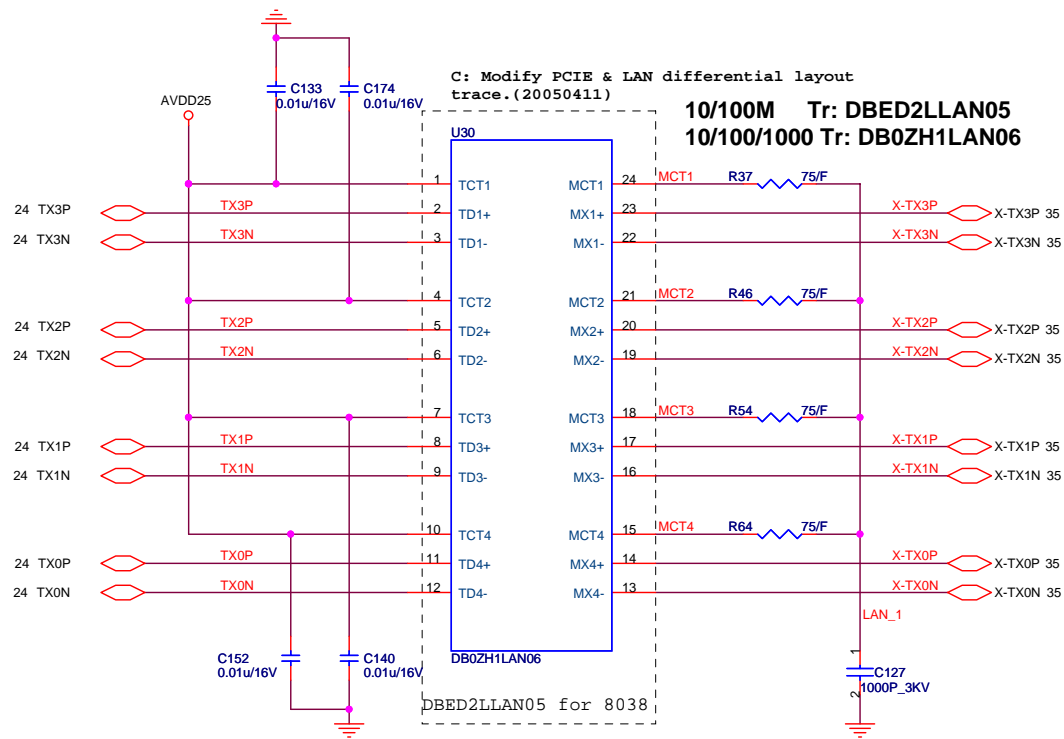
C290 1000p/50V

C291 1000p/50V

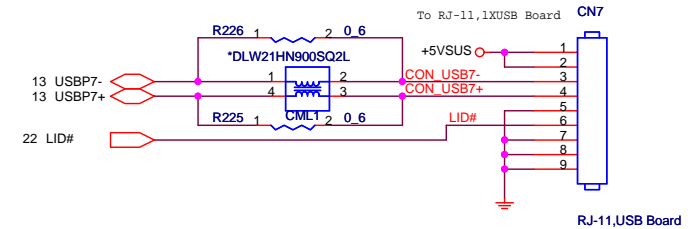
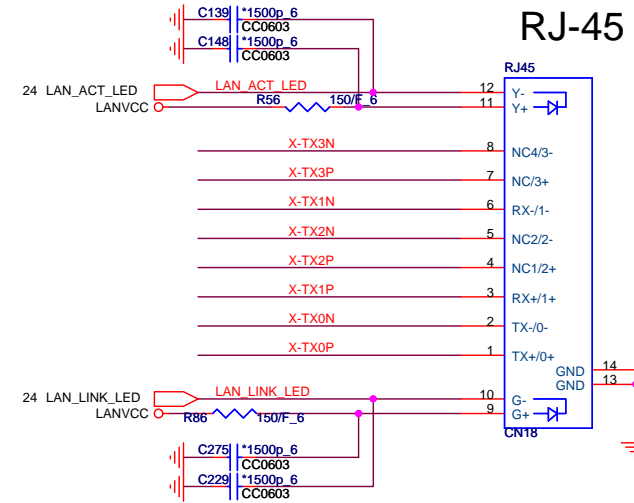
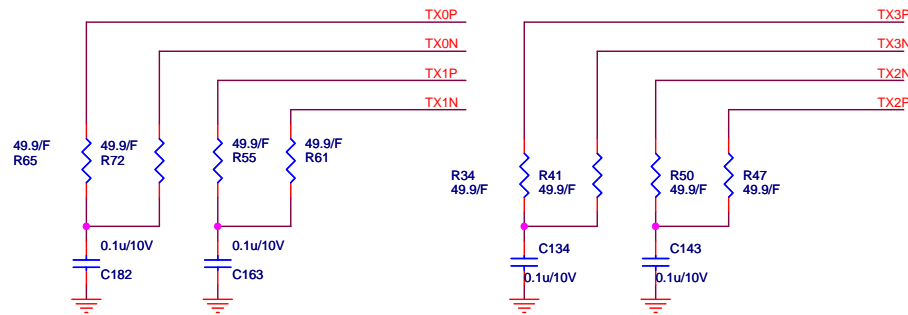
C293 1000p/50V

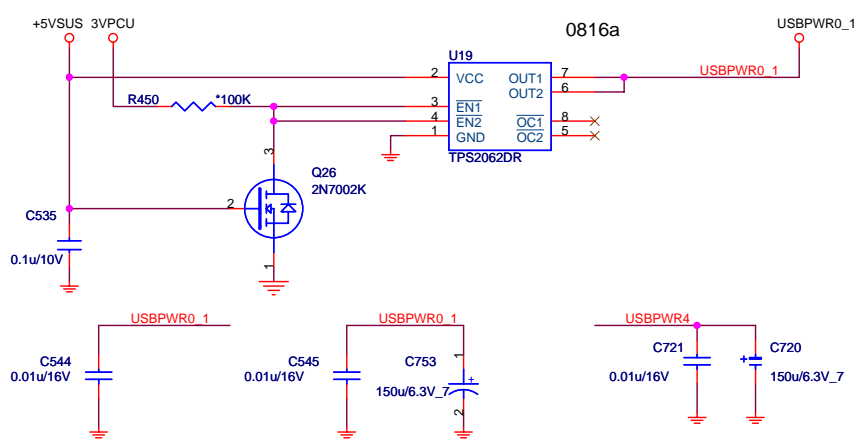


0804 REDUCING THE LANVCC NOISE

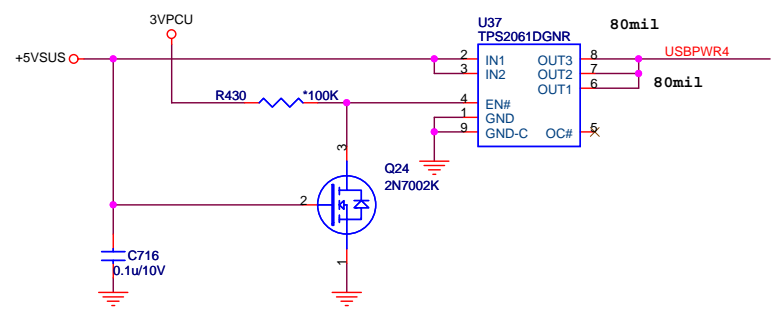


GigaLAN transformer

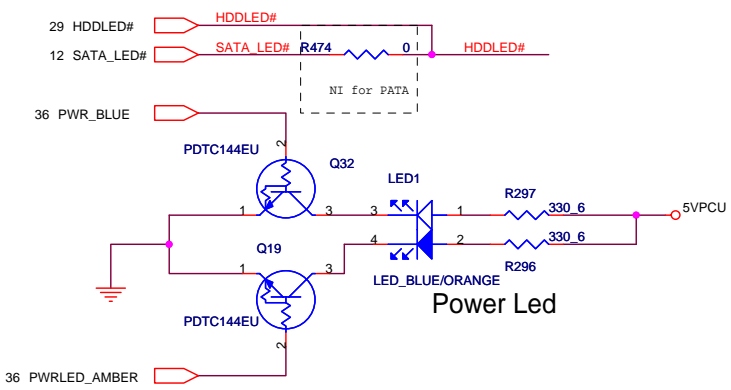




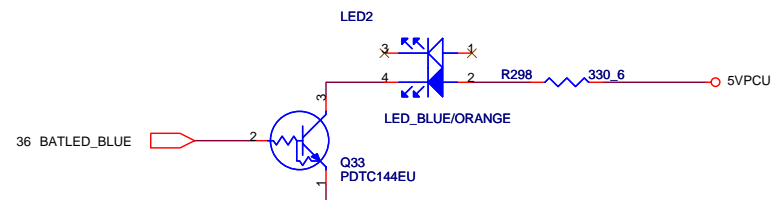
C:Change U1 from G528 to TPS2061



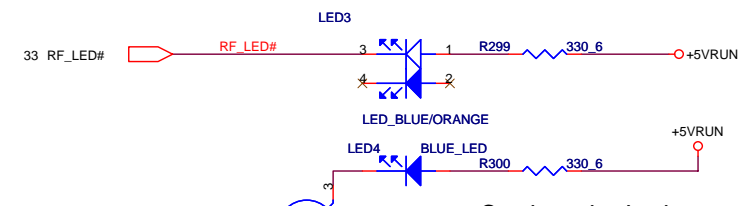
HDD,SATA Led



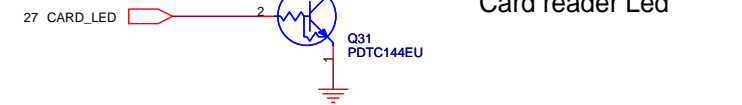
Battery Led



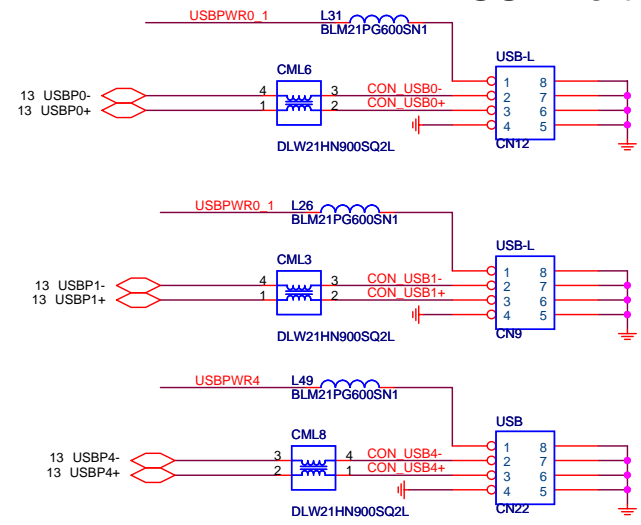
Wireless Led



Card reader Led



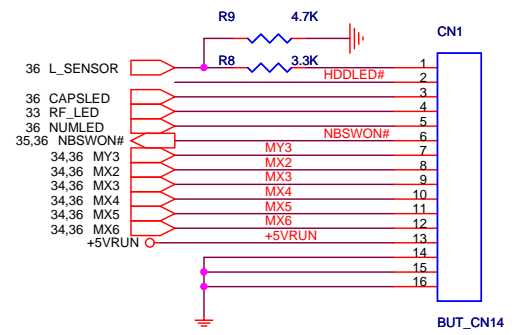
USB Port

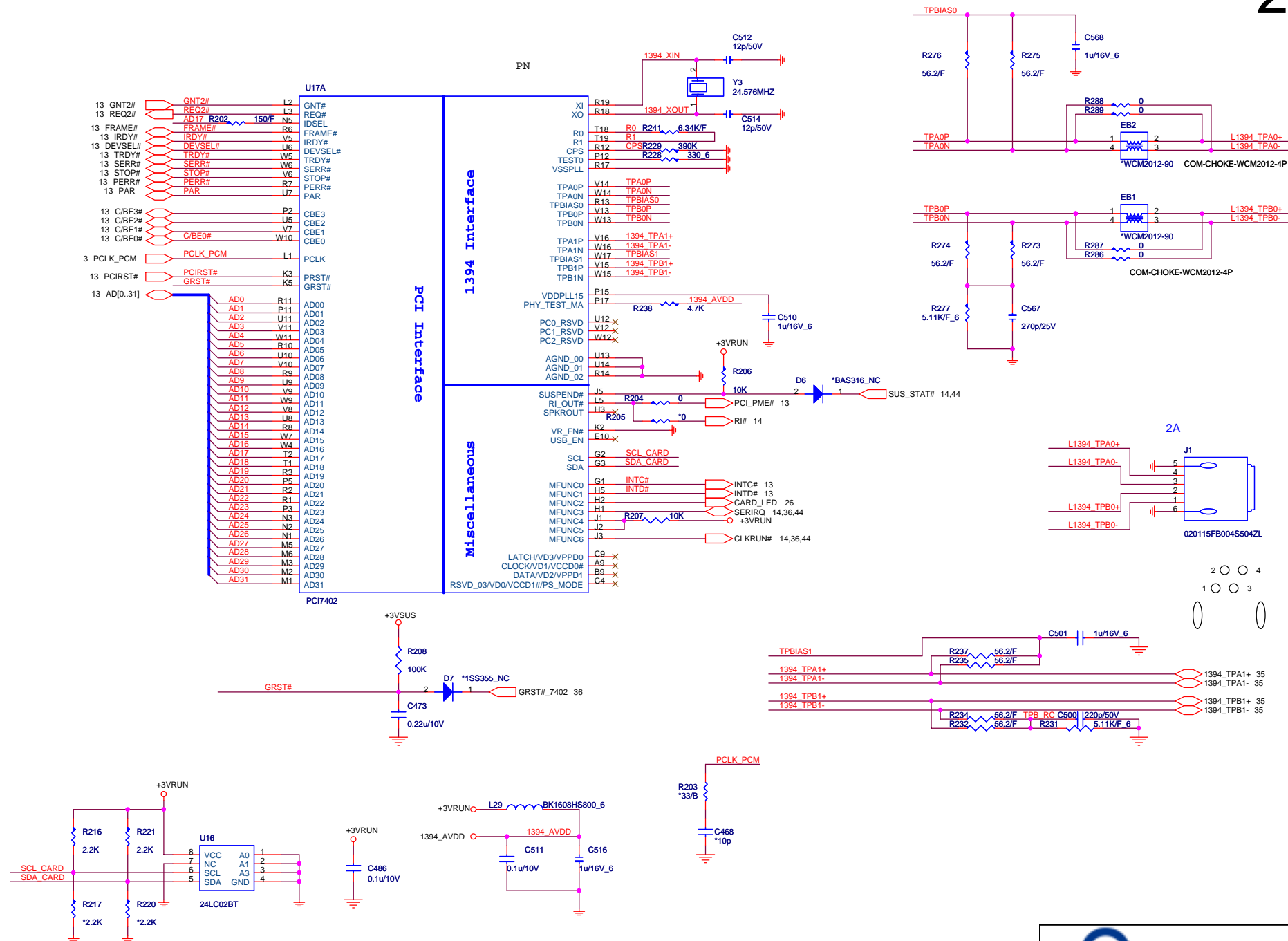


Left

Right

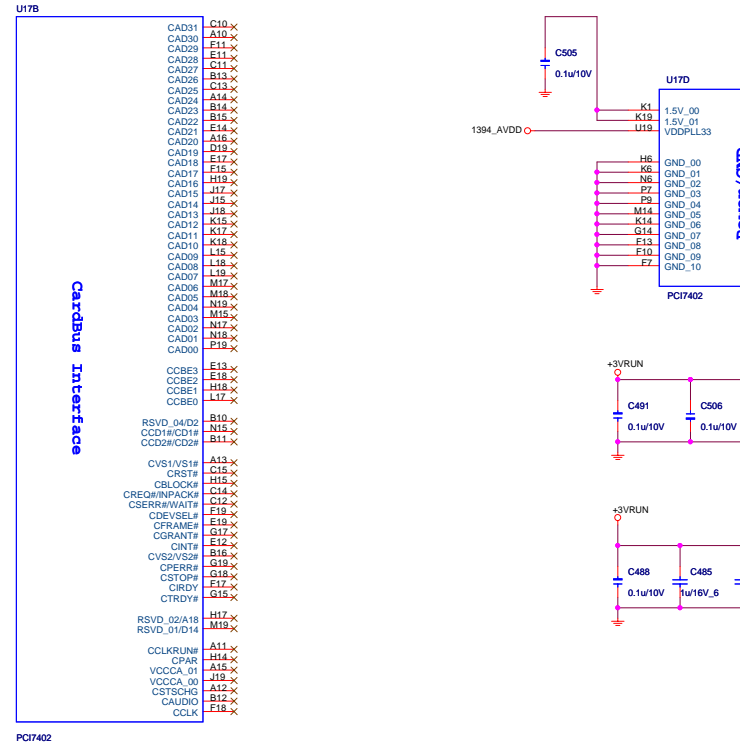
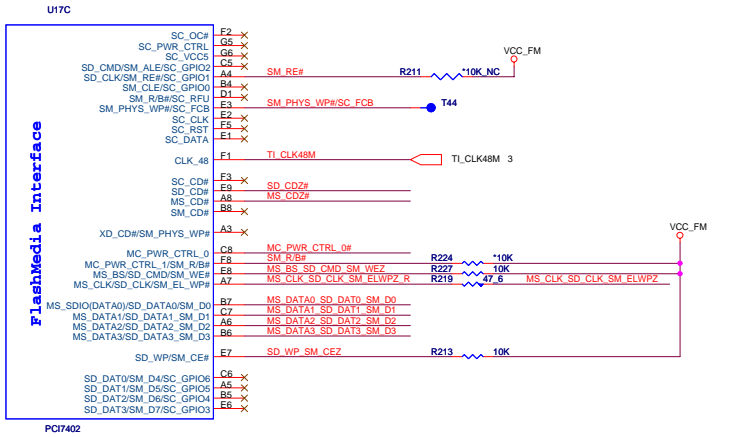
For Bottom Board



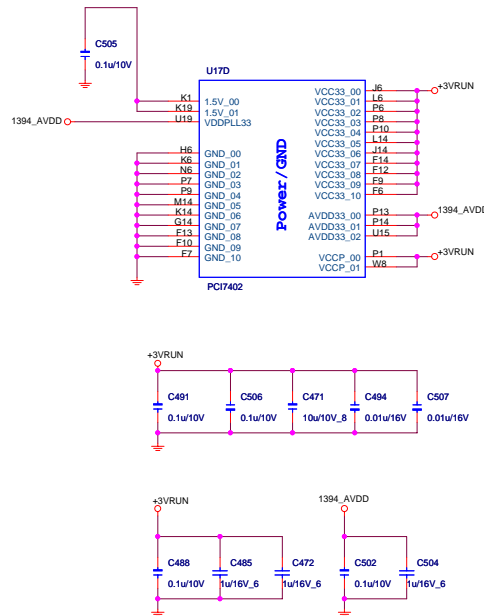
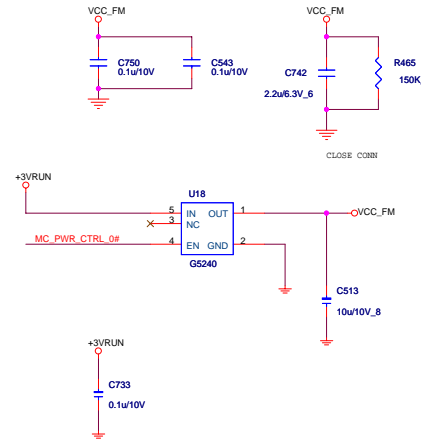
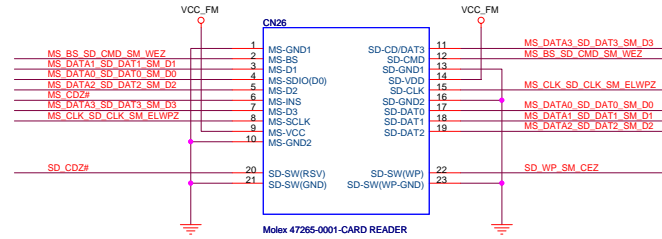


DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.

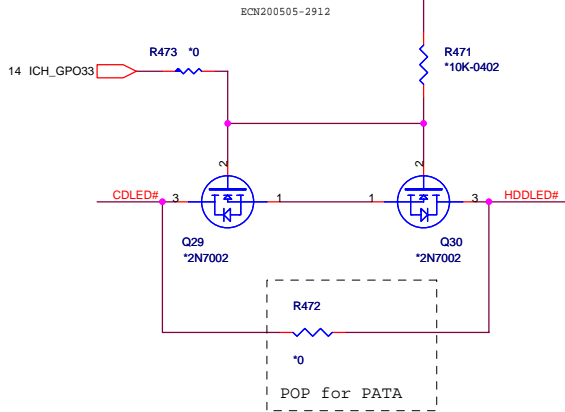
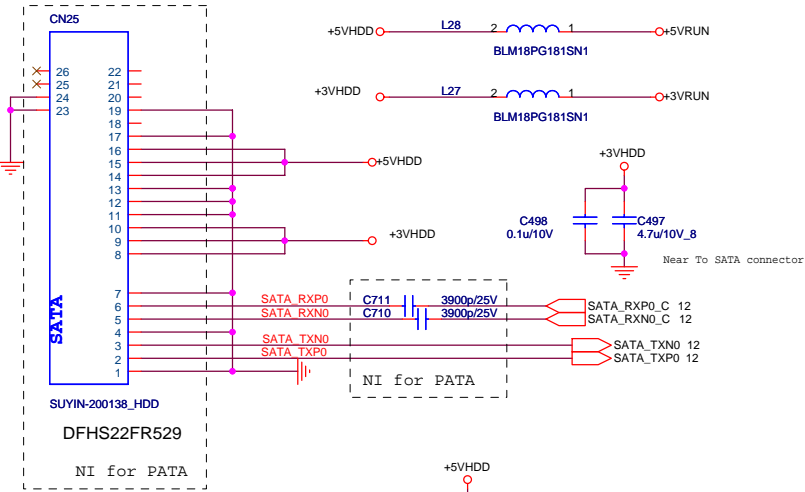
28



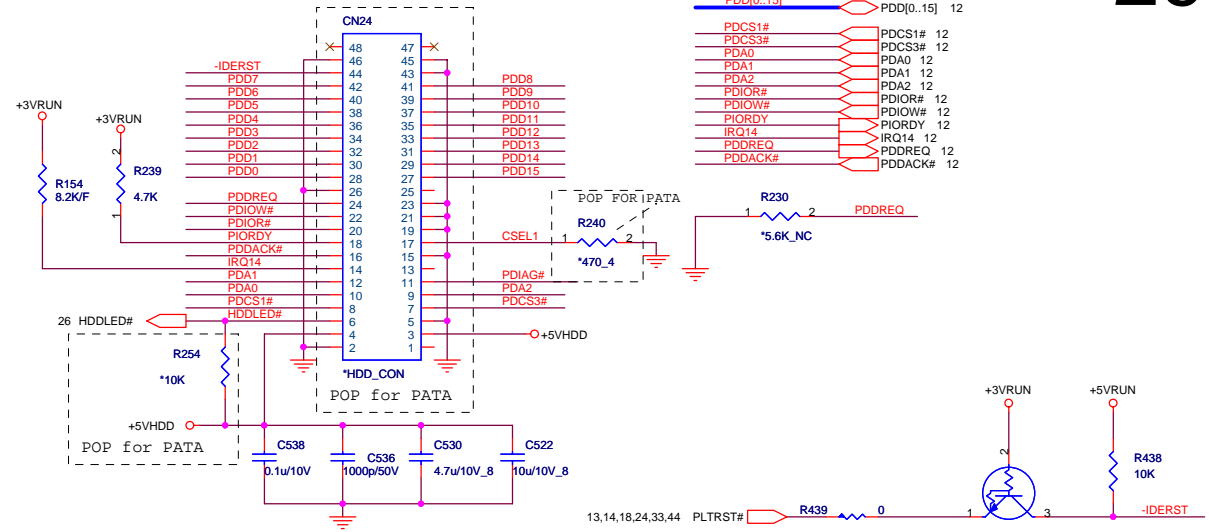
3 IN1 CARD READER (push-push)



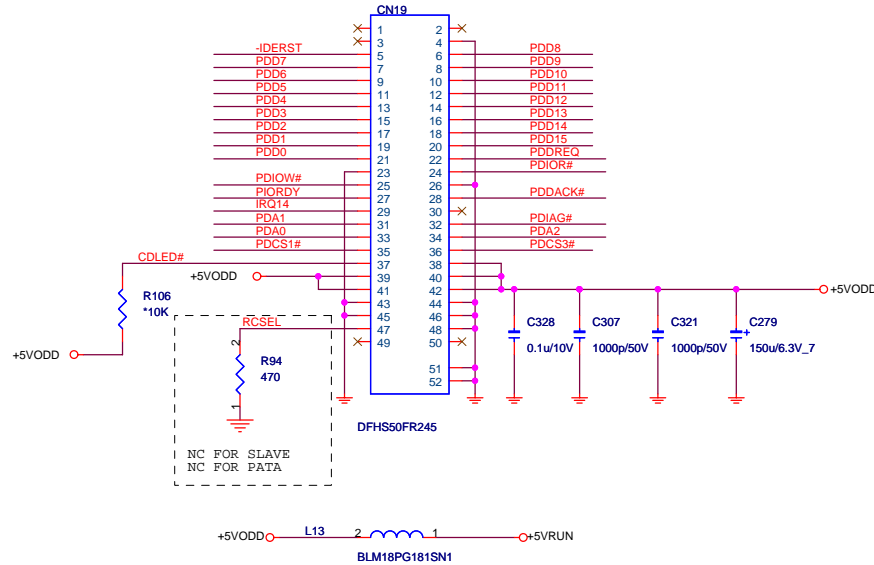
SATA HDD



PATA HDD

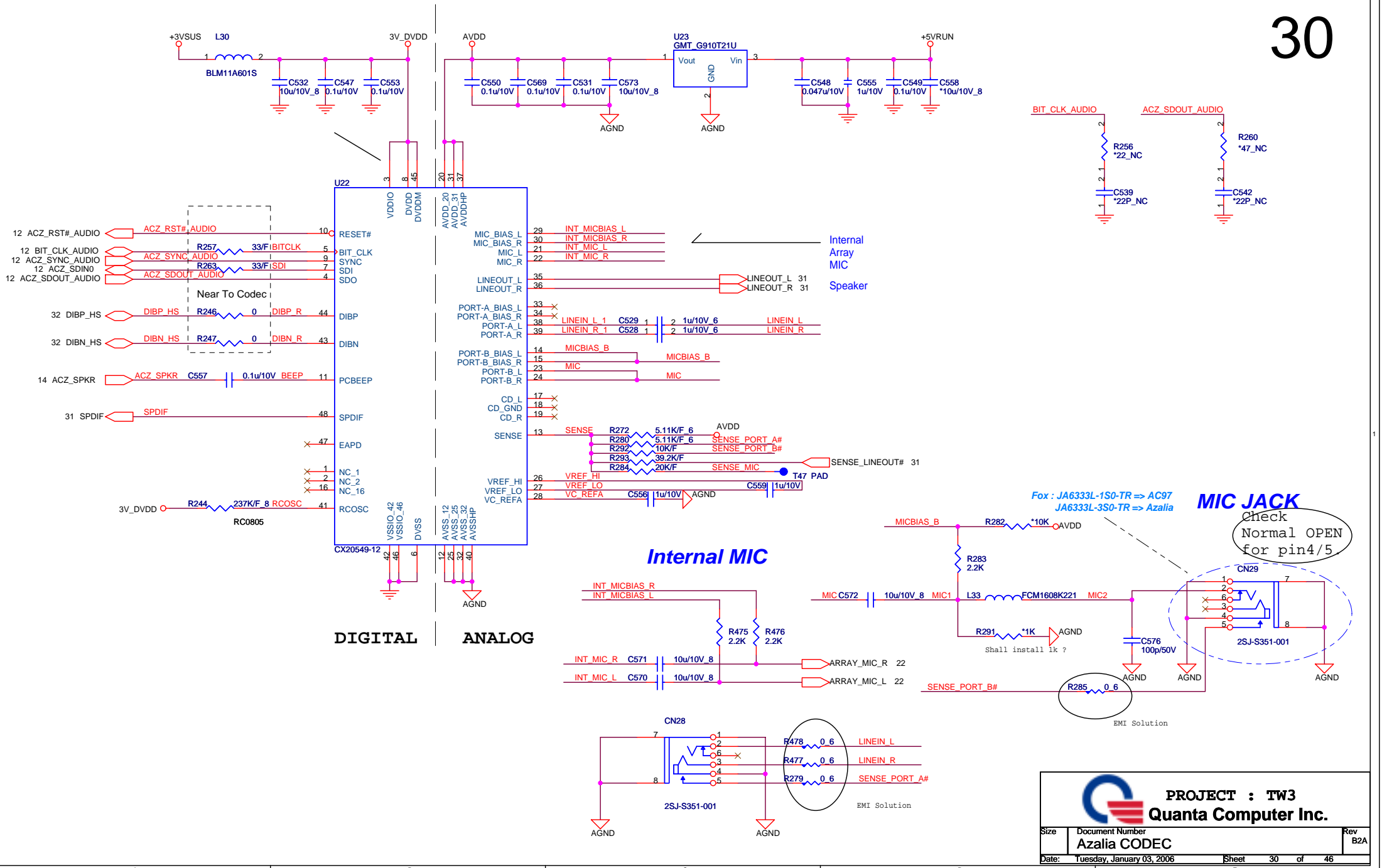


ODD

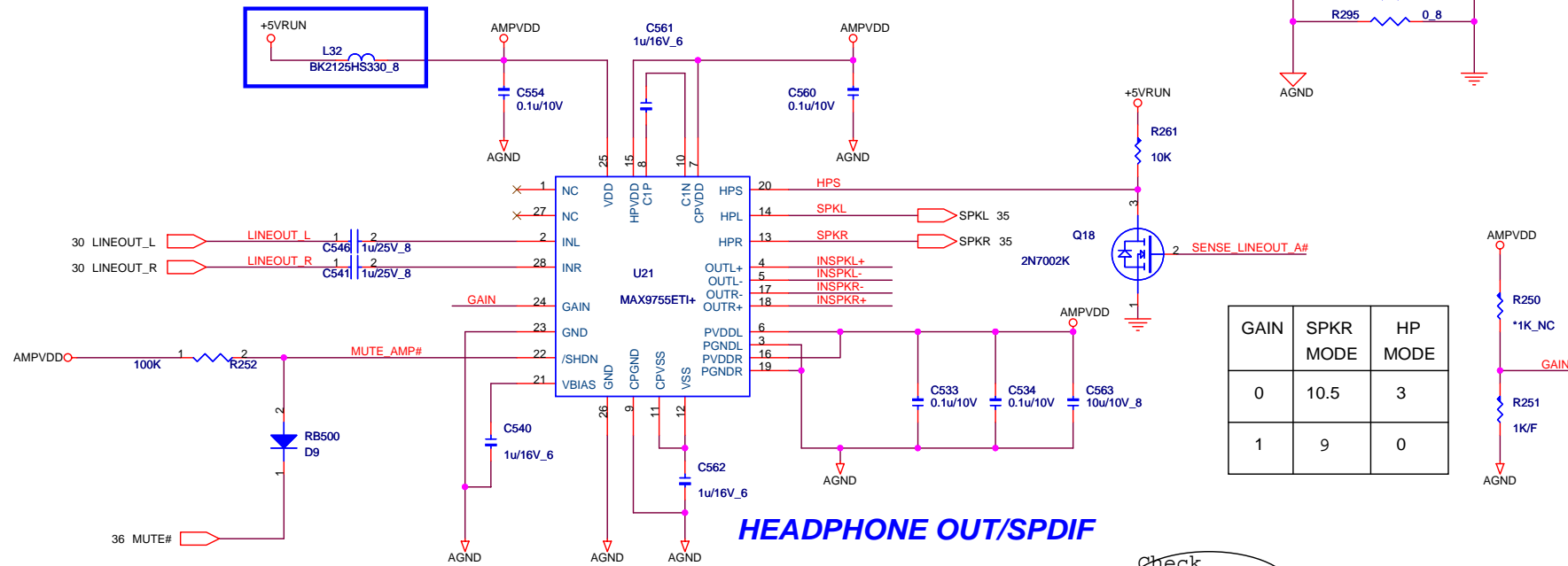


FOR PATA HDD

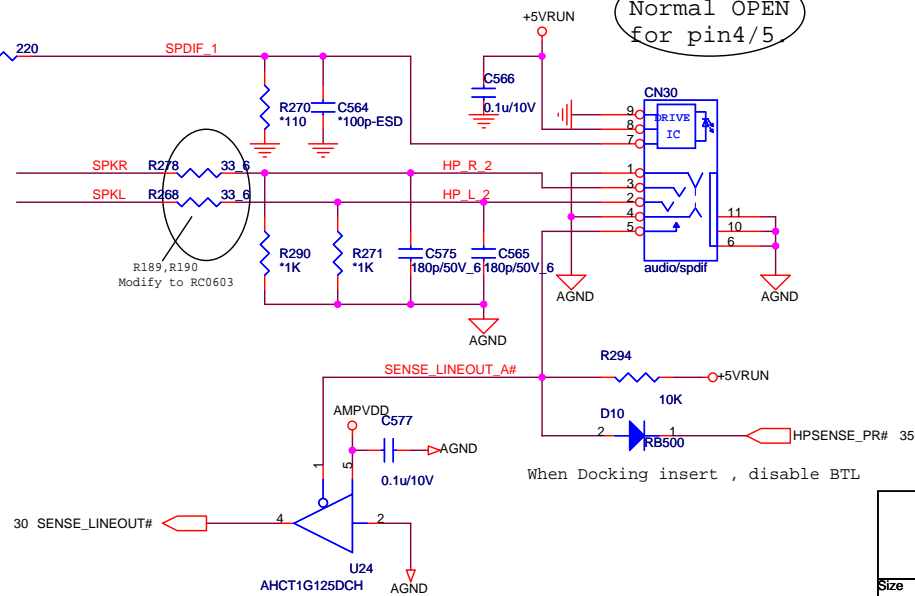
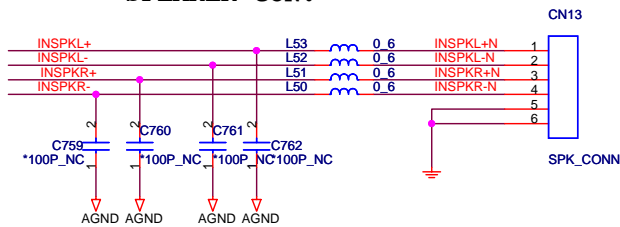
CN19	NI
C730	NI
C729	NI
CN18	HDD CON
R517	NI
Q25	2N7002
Q26	2N7002
R513	10K
R512	0
R168	470



0816a

**HEADPHONE OUT/SPDIF**

Check
Normal OPEN
for pin4/5.

SPEAKER CON.

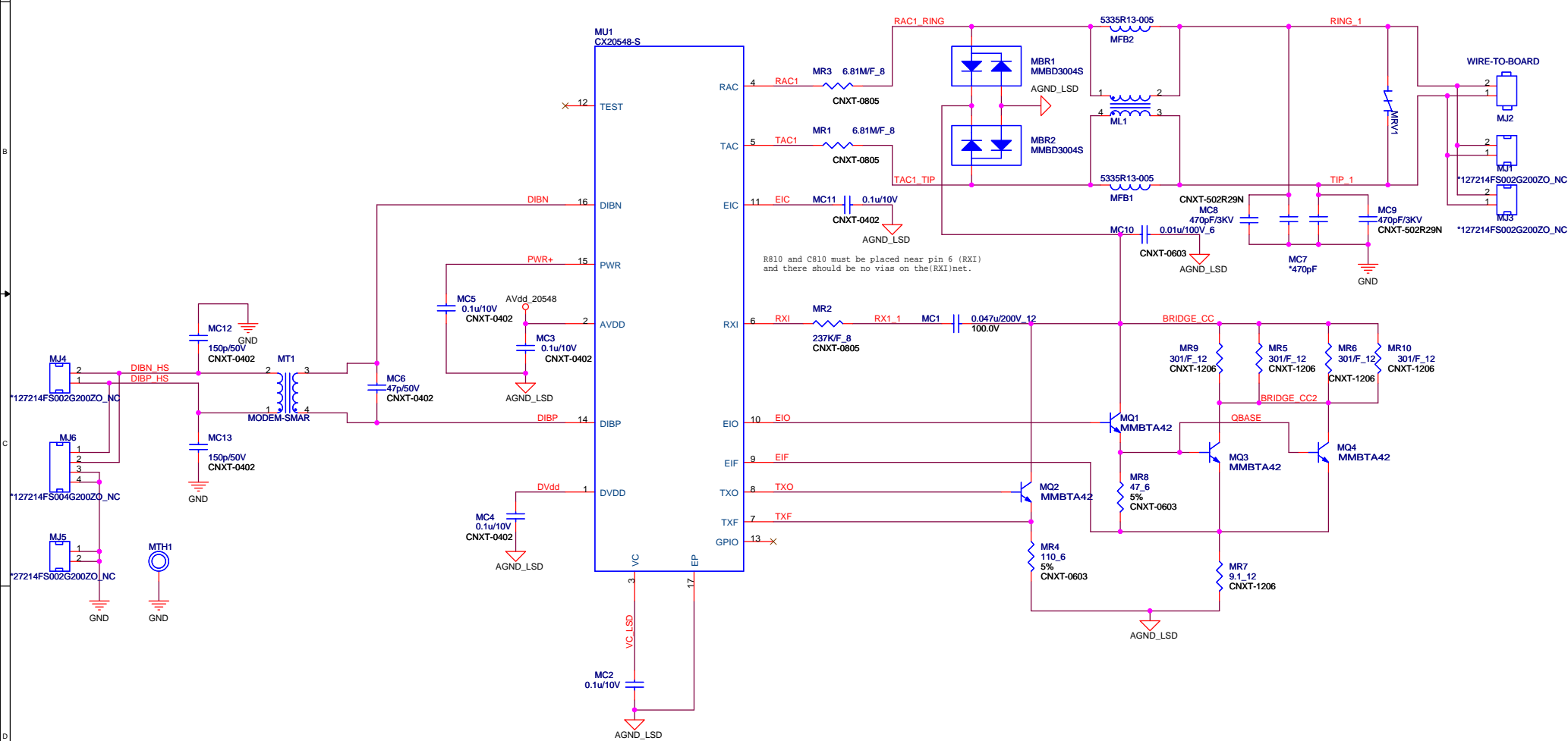
Revision History		
REV	Description	Date
0	Initial Release	April 26, 2005

30 DIBN_HS

30 DIBP_HS

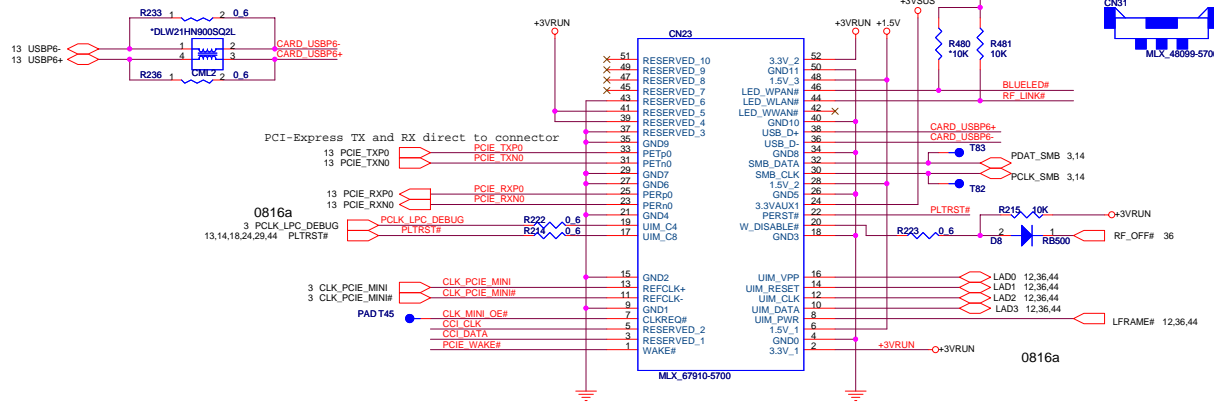
DIBN_HS

DIBP_HS

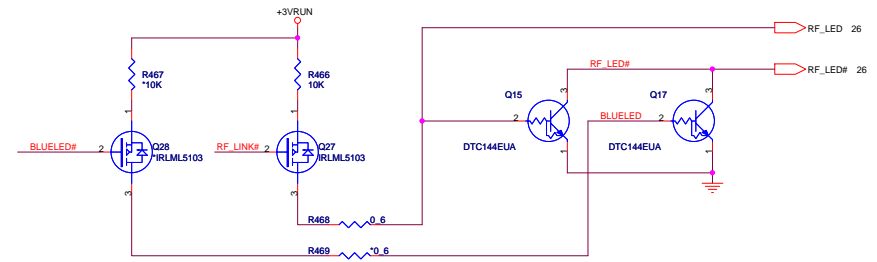
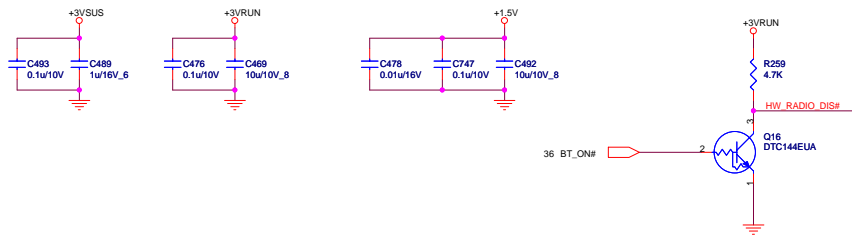
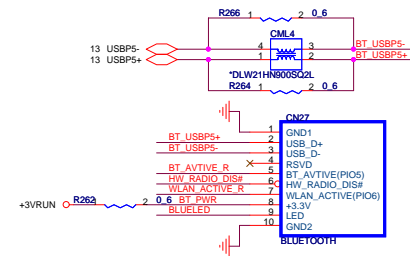
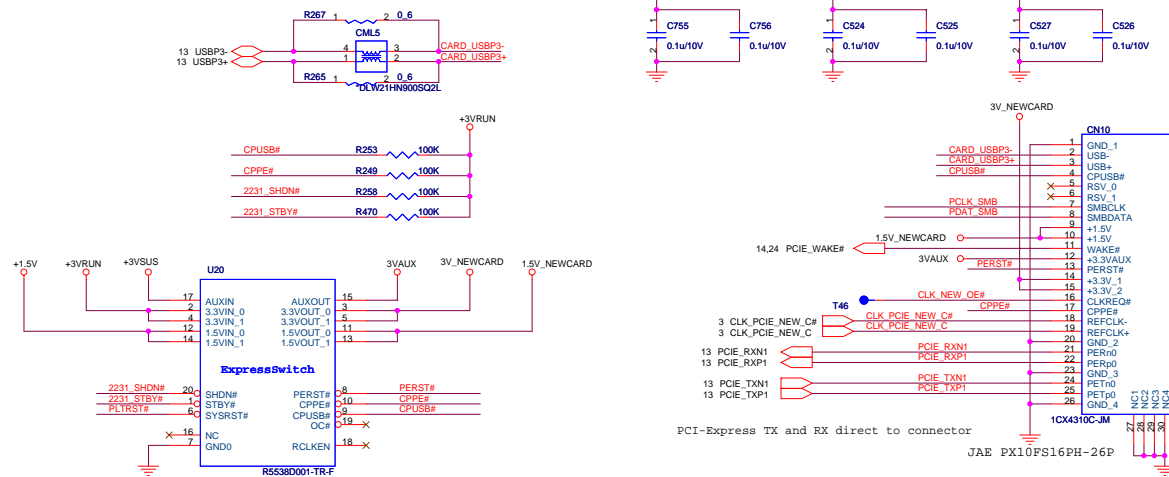


PCI-E Mini Card

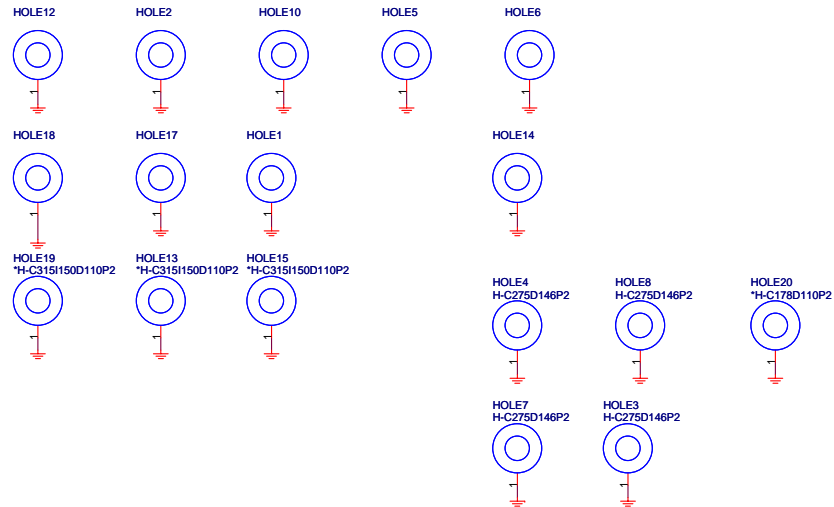
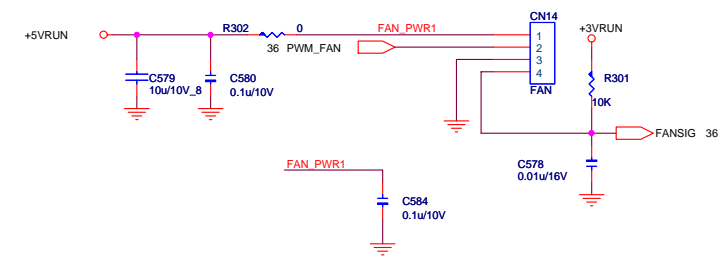
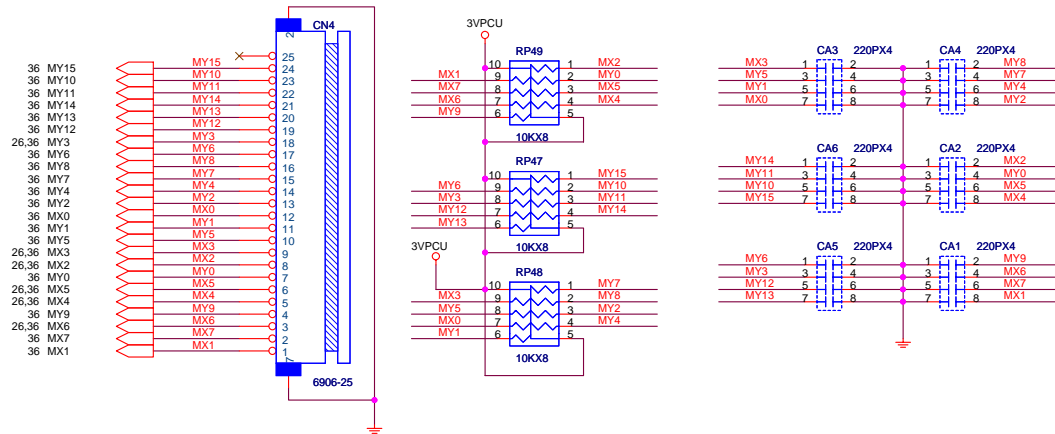
Need one more wireless LED /mini card on MB ?
currently , No LED here



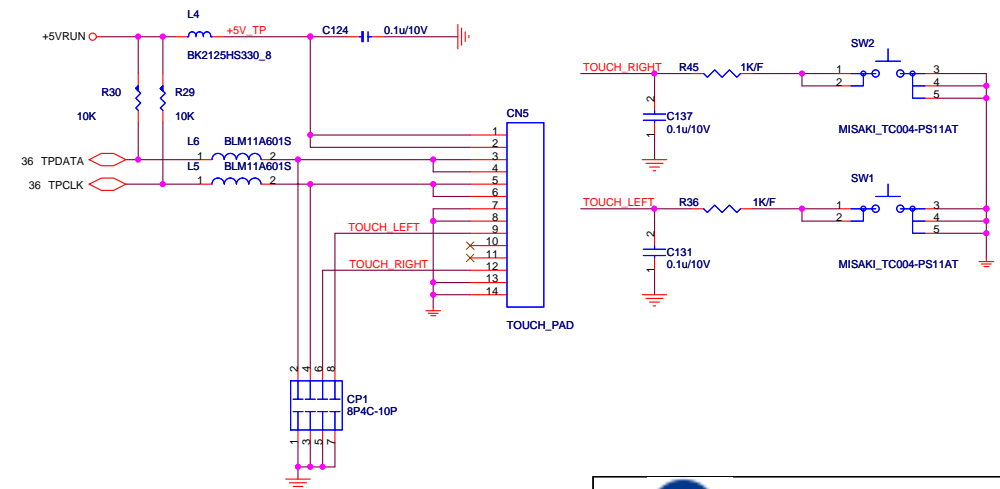
BLUETOOTH CONNECTOR

**NEWCARD (PCIEXPRESS*1 + USB*1)**

KeyBoard Interface

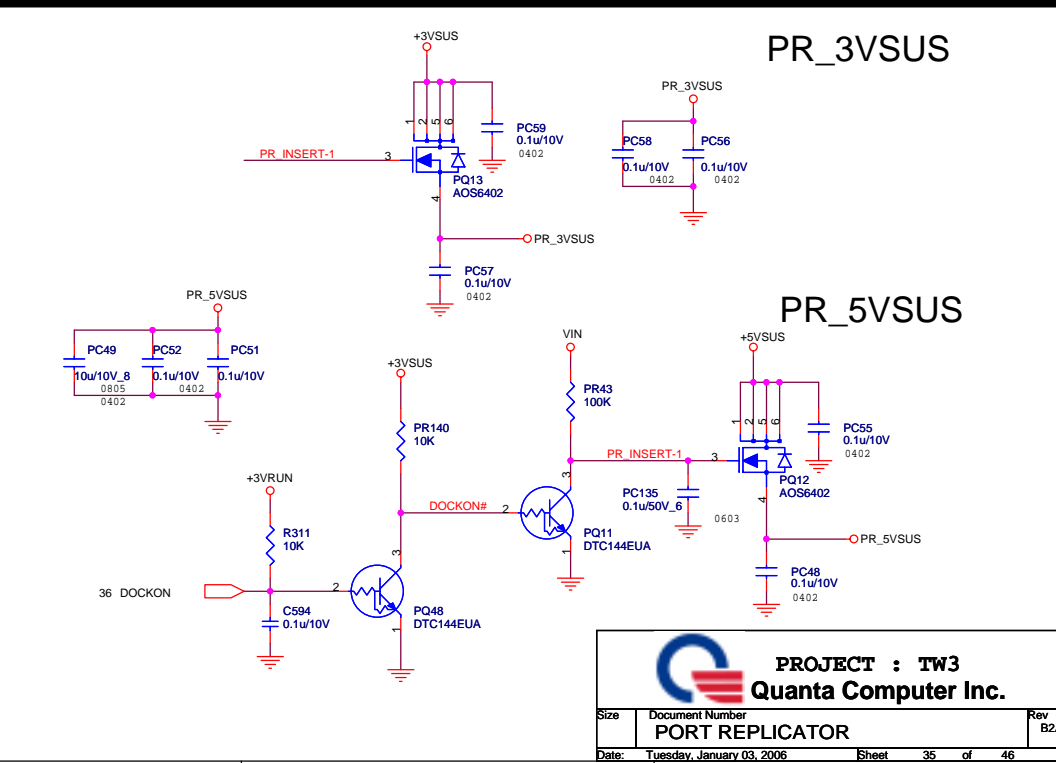
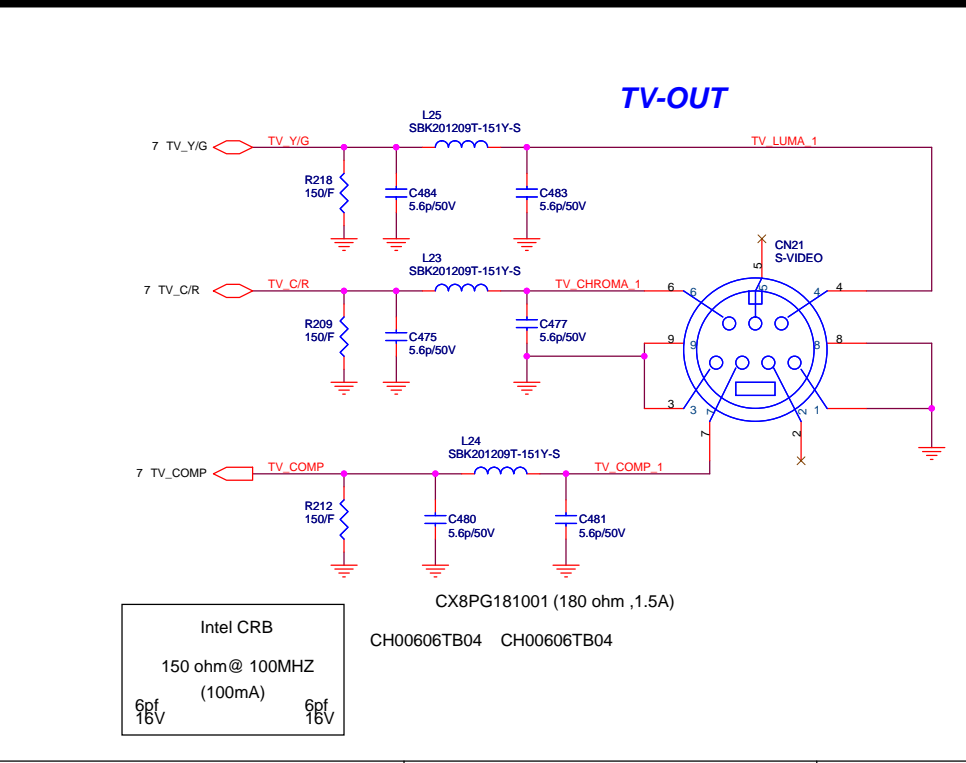
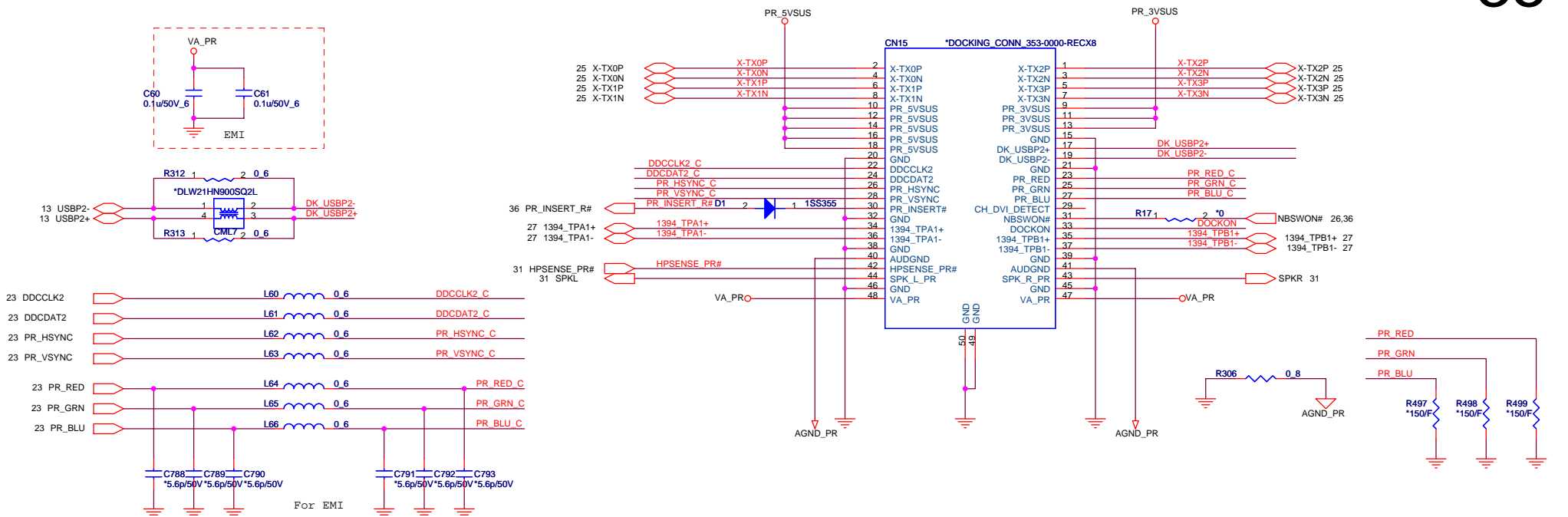


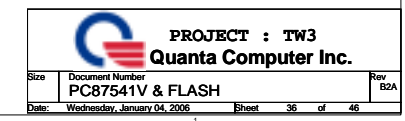
TOUCH PAD

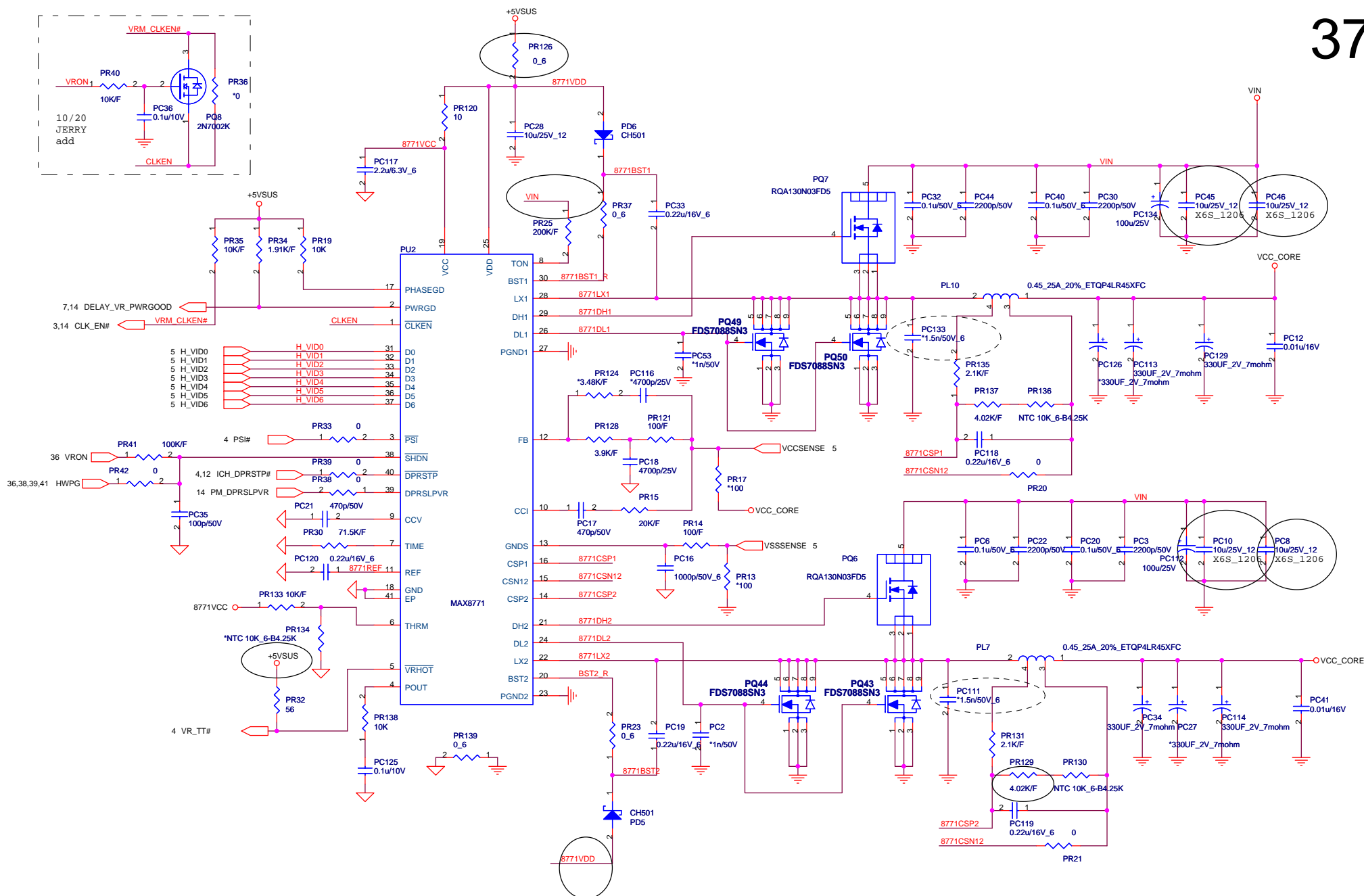


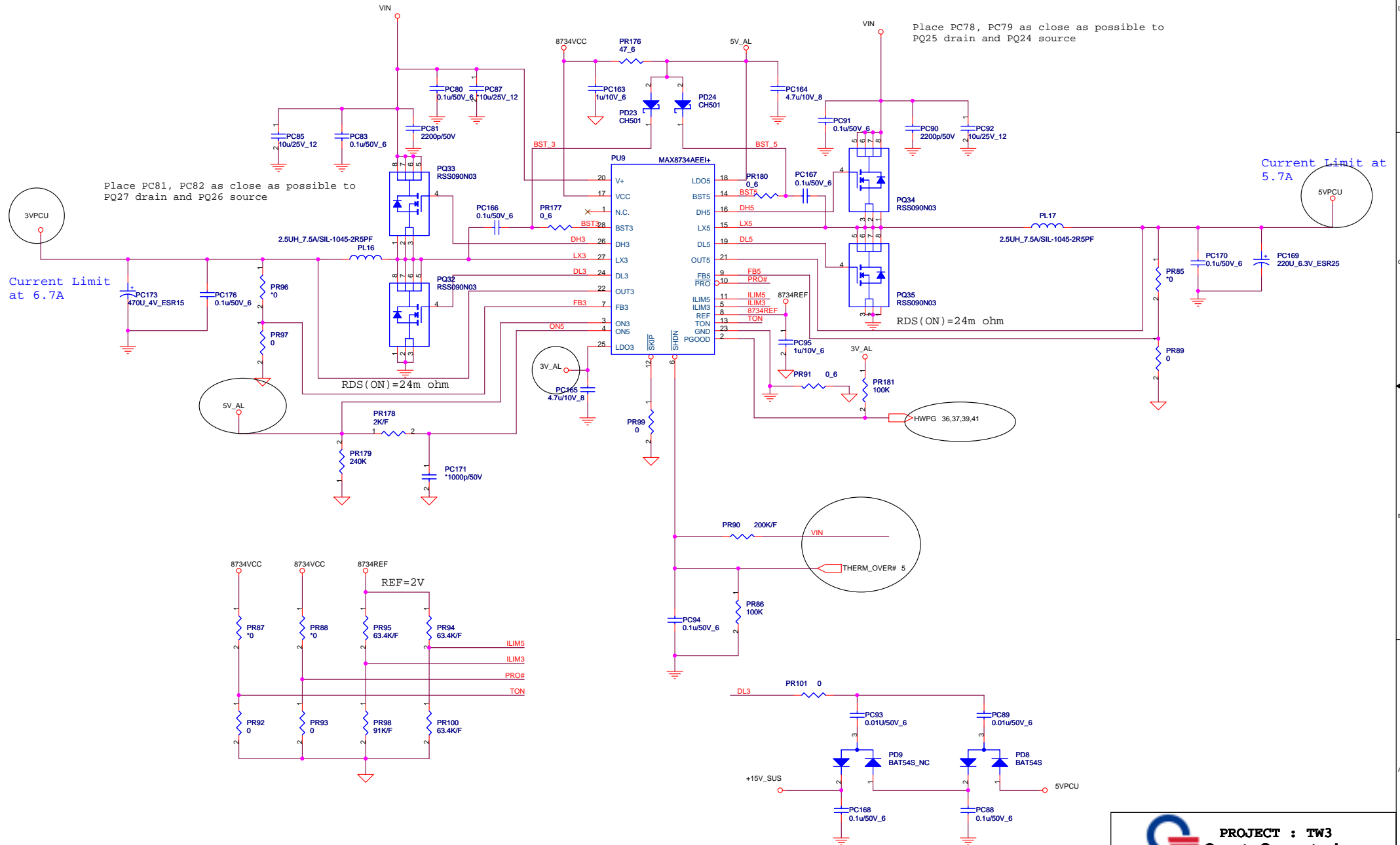
PROJECT : TW3
Quanta Computer Inc.

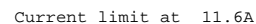
Size	Document Number	Rev
T/P,FAN,KB		B2A
Date:	Tuesday, January 03, 2006	Sheet 34 of 46



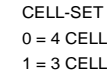






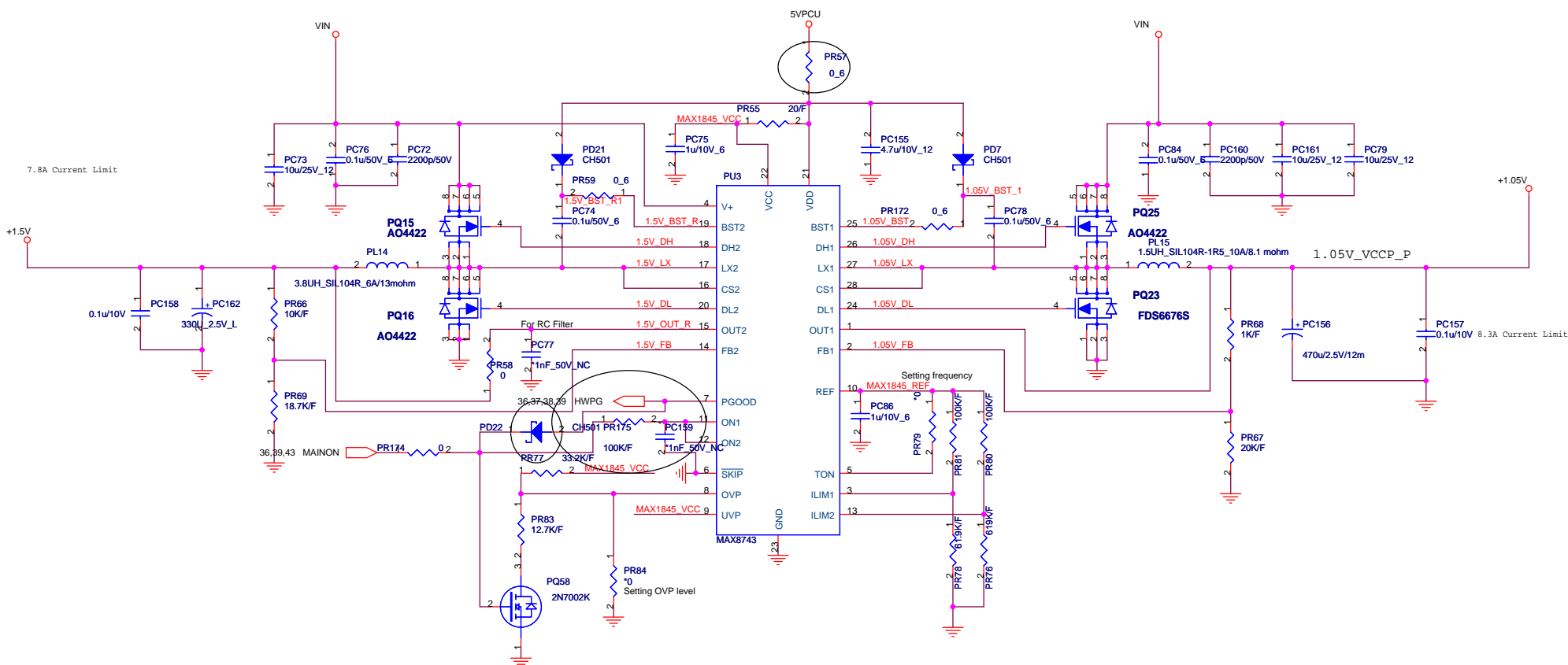


0.9 Volt +/-5%
Design current 1.05A
Peak current 1.5A

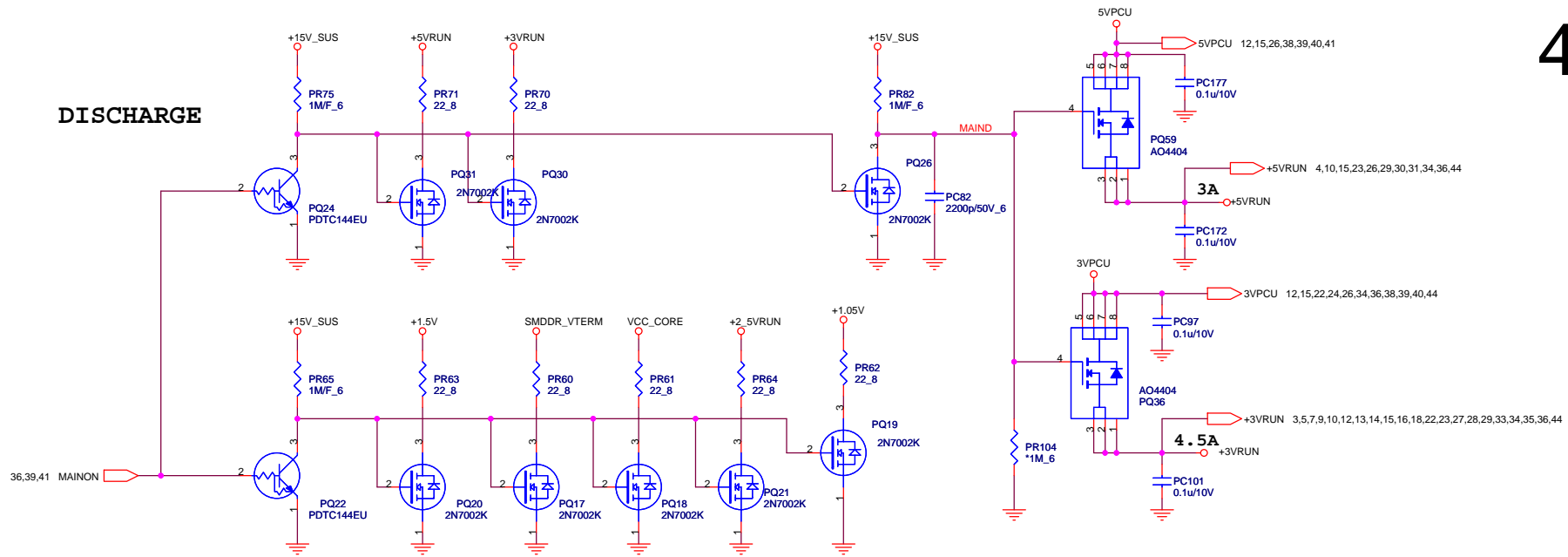


$$\text{ICHG} = (\text{V ICTL} / \text{V REFIN}) * (0.075 / \text{RS2})$$

AO4422: $I_d = 11A$, $R_{ds(on)} = 24m\ \Omega$, $Q_g = 19.8nC$
 FDS6676S: $I_d = 14.5A$, $R_{ds(on)} = 7.25m\ \Omega$, $Q_g = 43\ nC$

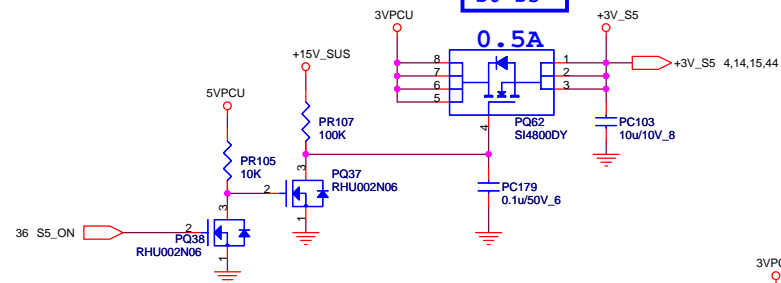


DISCHARGE



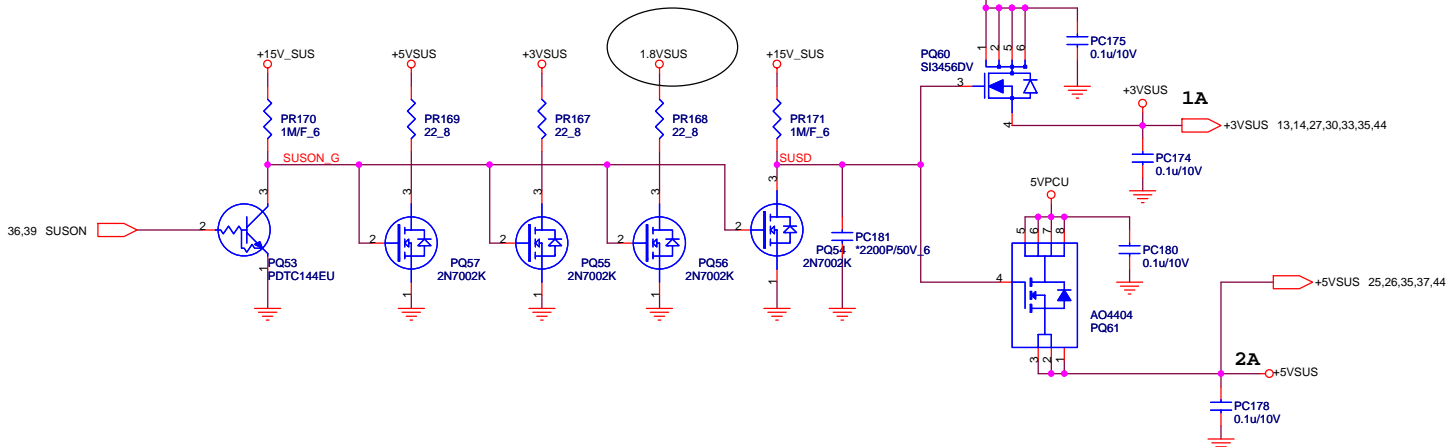
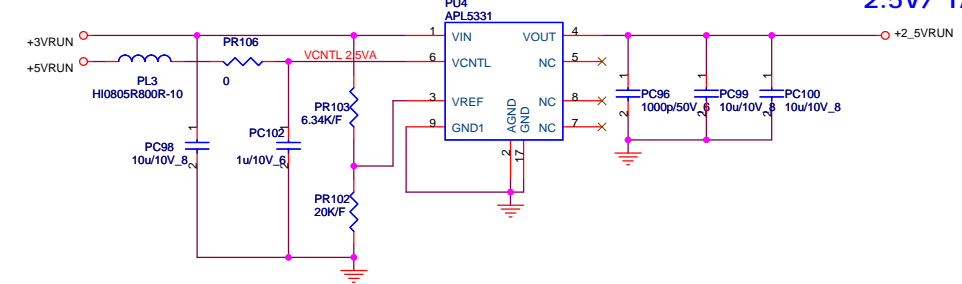
200mils

S0-S5



+2_5VRUN

2.5V/ 1A





[illegible]

A. G72M to G72MV

1. change P/N to G72MV (AJ073000T14)
2. Set VGA core to 1.0V fix.
3. Change PCI_DEVID.

B. VRAM 128MB to 64MB


- 1.follow config table to set RAM_CFG.
- 2.Change VRAM P/N to HYNIX.
- 3.VRAMx2

C. LAN GIGA to 10/100.

- 1.Change LAN chip to 8038(AJ080380000).
- 2.Change Rset resistor.
- 3.Change transformer.

D. SATA to PATA

- 1.Set ODD to slave.
- 2.Set HDD to master.
3. Remove SATA conn.
4. Add PATA conn.
5. Change board ID to PATA.
6. Install resistor to connect ODD and HDD LED.
7. NI resistor of SATA LED.

MODEL	REV	CHANGE LIST		Model	TW3 M/B		
				Page	From	To	
TW3M	1230 to 0102	Page 38	PC173 change to 470uF.	1	1A		
		Page 39	PC66 change to install.	2	1A		
		Page 41	PD7,PD21,PD22 change to CH501.	3	1A		
		Page 37	PD6,PD5 change to CH501.	4	1A		
		Page 26	CN12,CN9 USB connector change to DIP type.	5	1A		
		Page 29	CN25 pin25,26 and CN24 pin47,48 disconnect to GND.	6	1A		
		Page 23	CN6 pin27,28 disconnect to GND.	7	1A		
		Page 32	SW1,SW2 P/N change to DHP00FC1G16.	8	1A		
		Page 36	Change R454 to 100K,R508,R509 to 10K.	9	1A		
		0102 to 0103	Page 4	R101,R97,Q11 change to install.	10	1A	
			Page 6,7,8,9,10,11	Change U32 P/N to AJSL8Z20T17.(945GM)	11	1A	
			Page 12,13,14,15	Change U36 P/N to AJSL8YB0T12.(ICH7M)	12	1A	
			Page 44	Add C785 for EMI.	13	1A	
			Page 37	PR128 change to 3.9K.	14	1A	
					15	1A	
					16	1A	
					17	1A	
					18	1A	
					19	1A	
				20	1A		
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			45	1A			
				<div><div></div><div>PROJECT : TW3 Quanta Computer Inc.</div></div> <div><div>Size</div><div>Document Number</div><div>Rev</div></div> <div><div>Change List (B2A)</div><div>B1A</div></div> <div><div>Date: Wednesday, January 04, 2006</div><div>Sheet 46 of 46</div></div>			
PROJECT: TW3		PCBA NO.	REV: 2B	DOC. NO :			
APPROVED BY : Johnson Hsu		CHECK BY : Titan Chiang	DRAWING BY : Tony Huang	DATE :05/05/2005	SHEET 1		