

01



SMT

O2Micro OZ8681

P2806

Ricktek RT8205

NCP6132/NCP5911/RT8209/G9334

Richtek RT8207

Richtek RT8209/RT9025

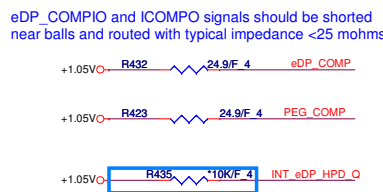
O2Micro OZ8122

Size
A3

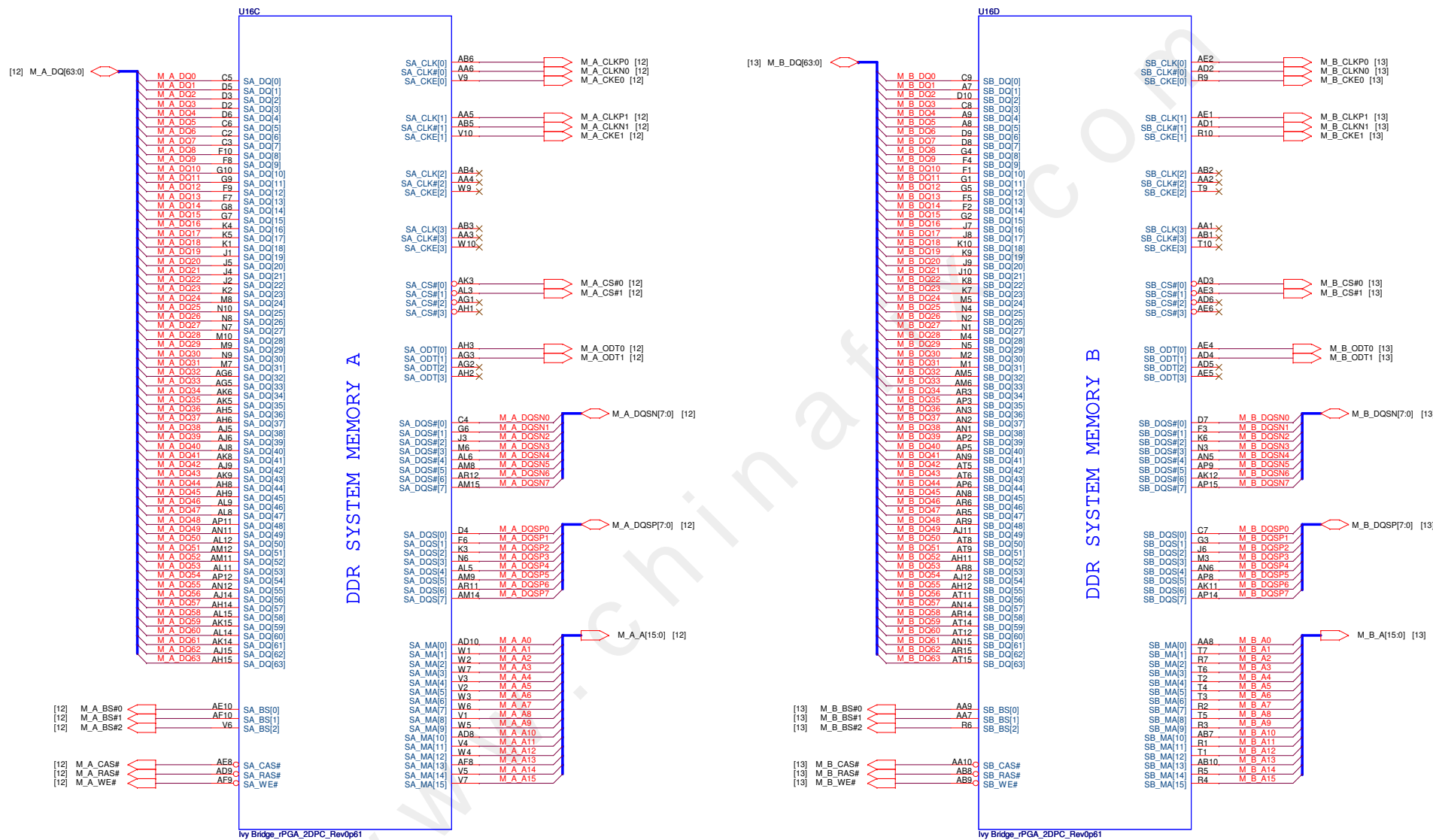
Document Number
Block Diagram

Rev
A

Date: Tuesday, March 27, 2012 Sheet 1 of 42

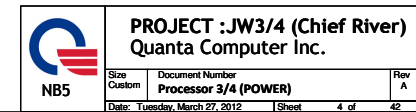


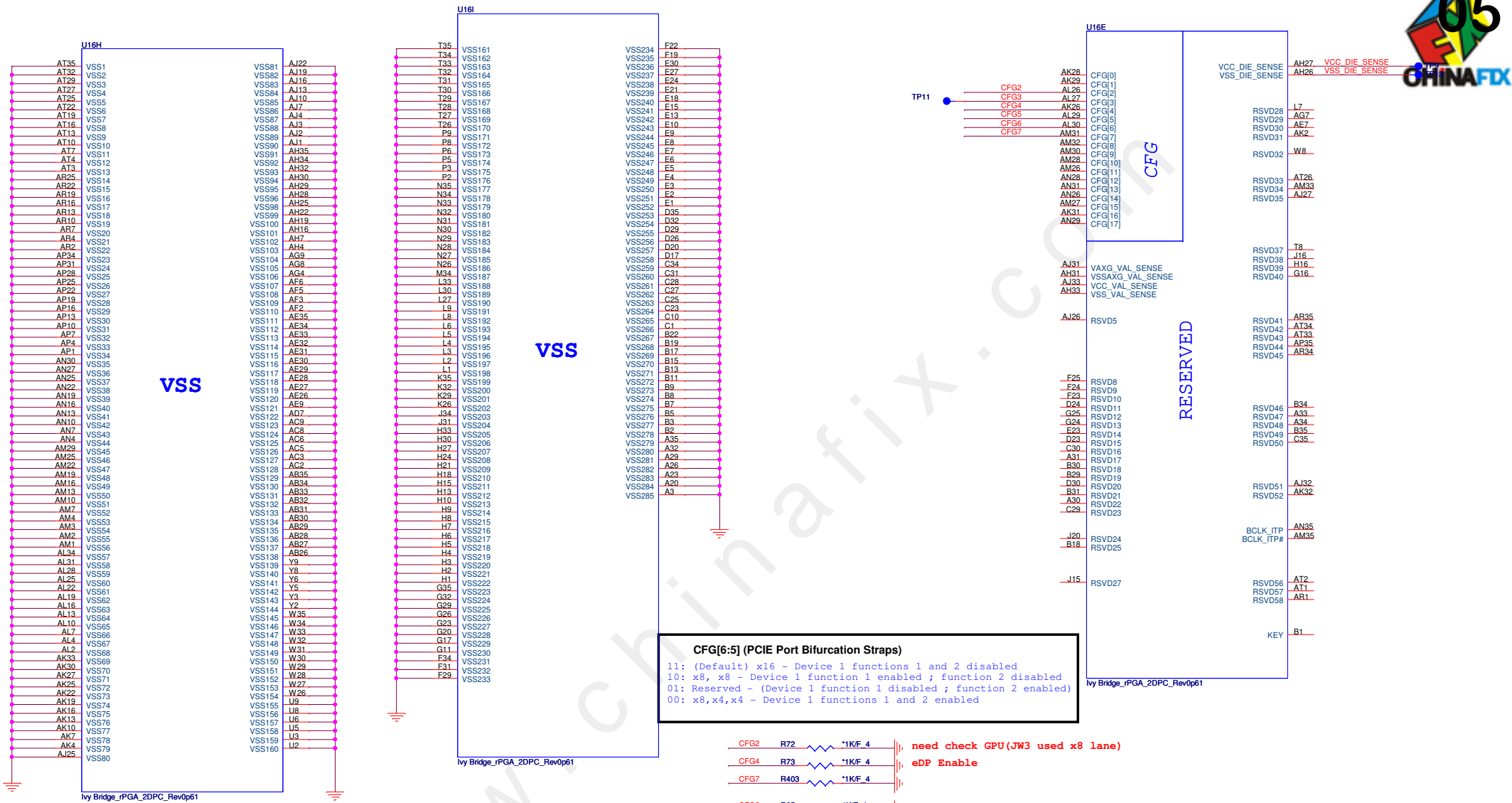
Ivy Bridge Processor (DDR3)



Ivy Bridge_rPGA_2DPC_Rev0p61

Ivy Bridge_rPGA_2DPC_Rev0p61



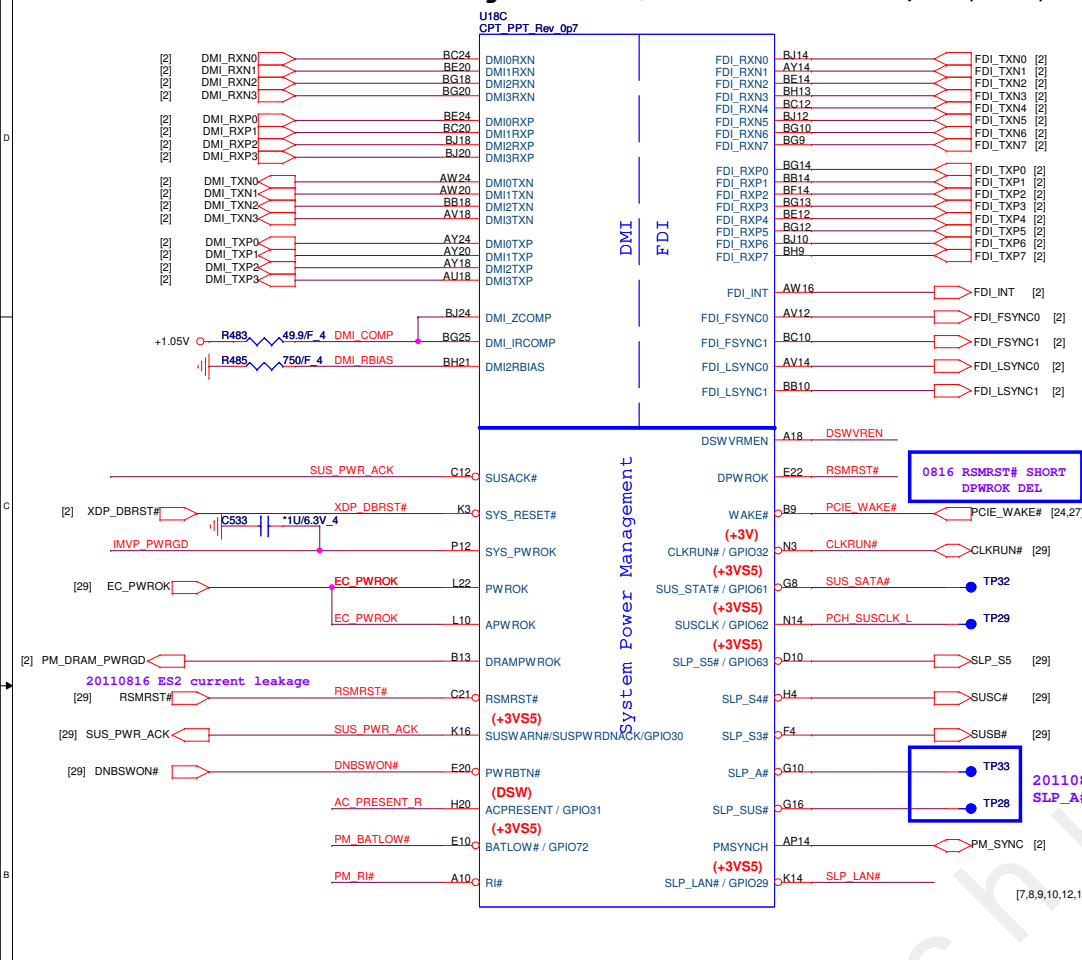


Processor Strapping

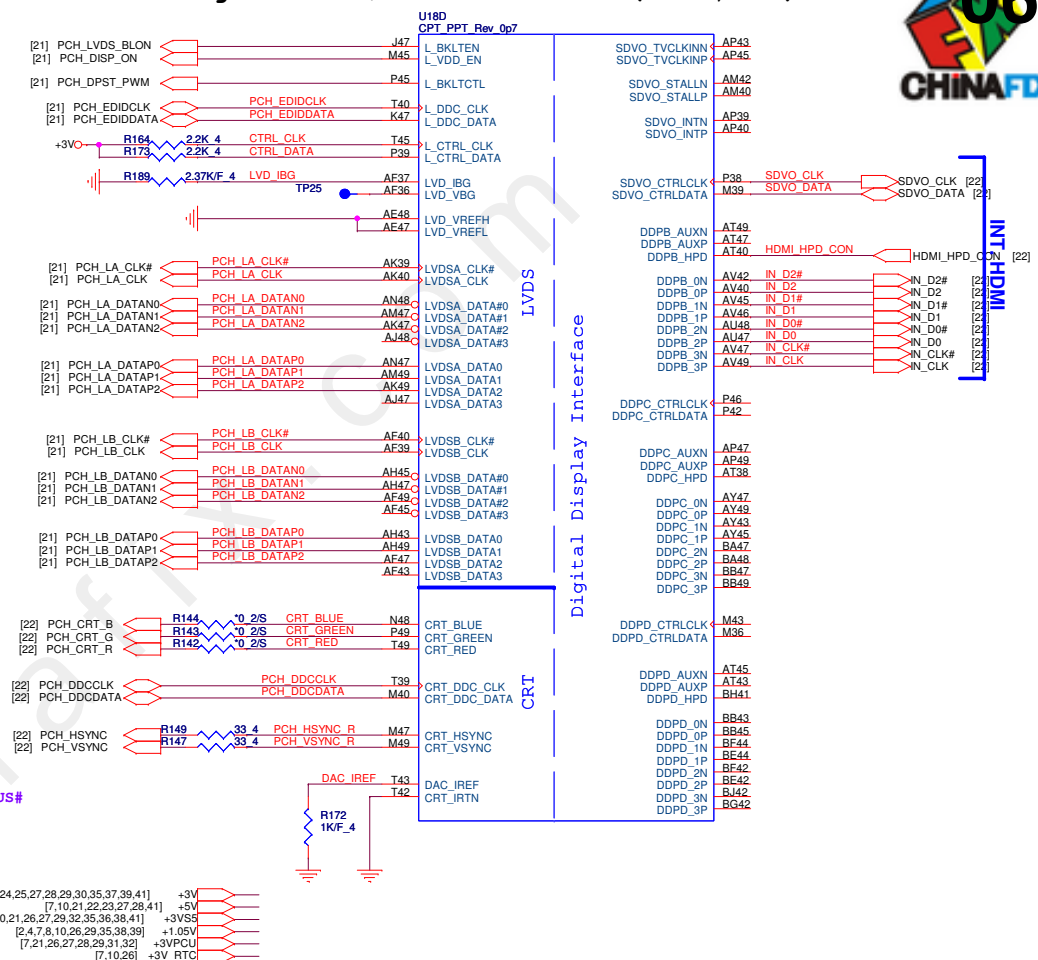
The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCIe Static x16 Lane Numbering Reversal.)	Normal Operation(Default)	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

Cougar Point/Panther Point (DMI, FDI, PM)

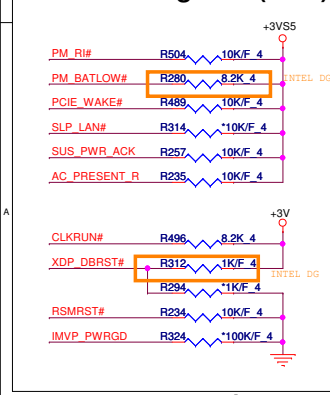


Cougar Point/Panther Point (LVDS, DDI)

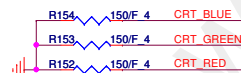


PCH Nut: QCI P/N: MBUL1001010 (Location:H13,H14)

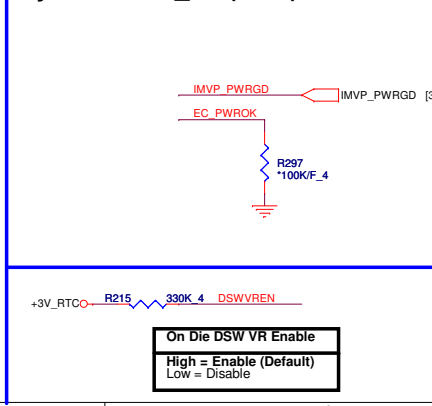
PCH Pull-high/low(CLG)



PD Res place close to PCH
PCH to Res routing 50 ohm Impedance.
Res to connector filter routing 37.5ohm Impedance.



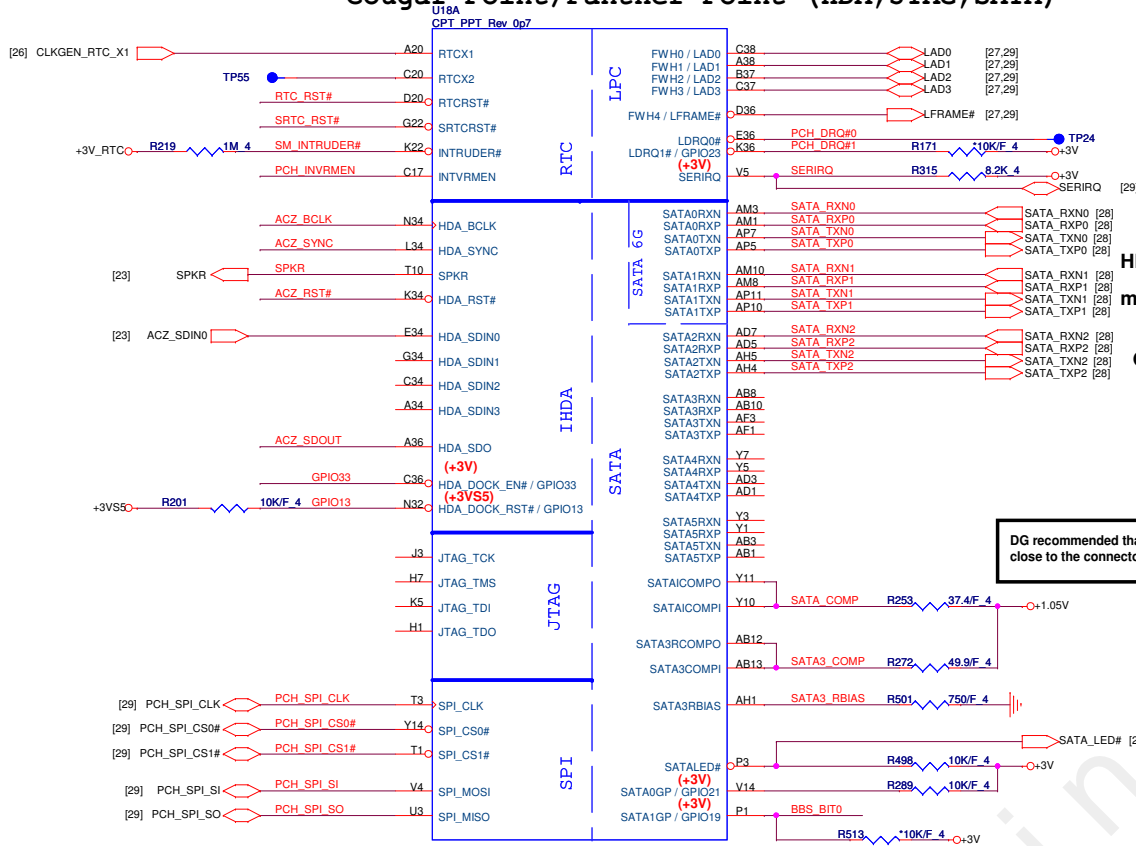
System PWR_OK(CLG)



PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size Custom	Document Number PCH 1/6 (Host/Display)	Re A
Date: Tuesday, March 27, 2012	Sheet	6 of 42

Cougar Point/Panther Point (HDA, JTAG, SATA)



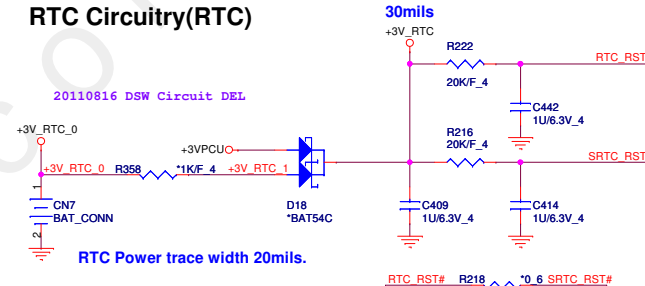
HDD0 (SATA3 6.0Gb/s)

mSATA (SATA4 3Gb/s)

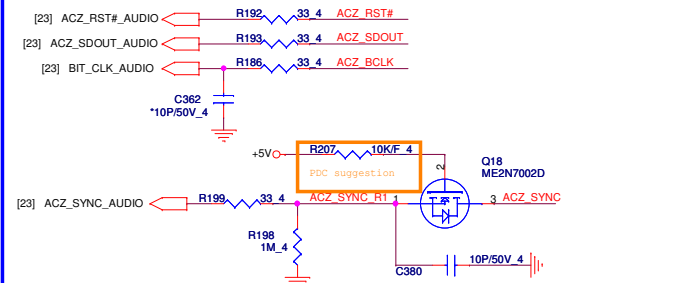
ODD (SATA2 3Gb/s)

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

RTC Circuitry(RTC)

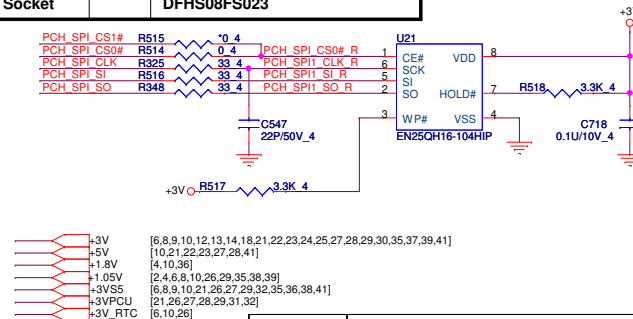


HDA Bus(CLG)



Vender	Size	P/N
EON	2MB	AKE38ZN0Q00 (EN25QH16-104HIP)
AMIC	2MB	AKE38ZN0802 (A25LQ16M-F/Q)
Socket		DFHS08FS023

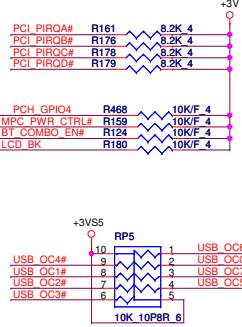
PCH SPI ROM(CLG)



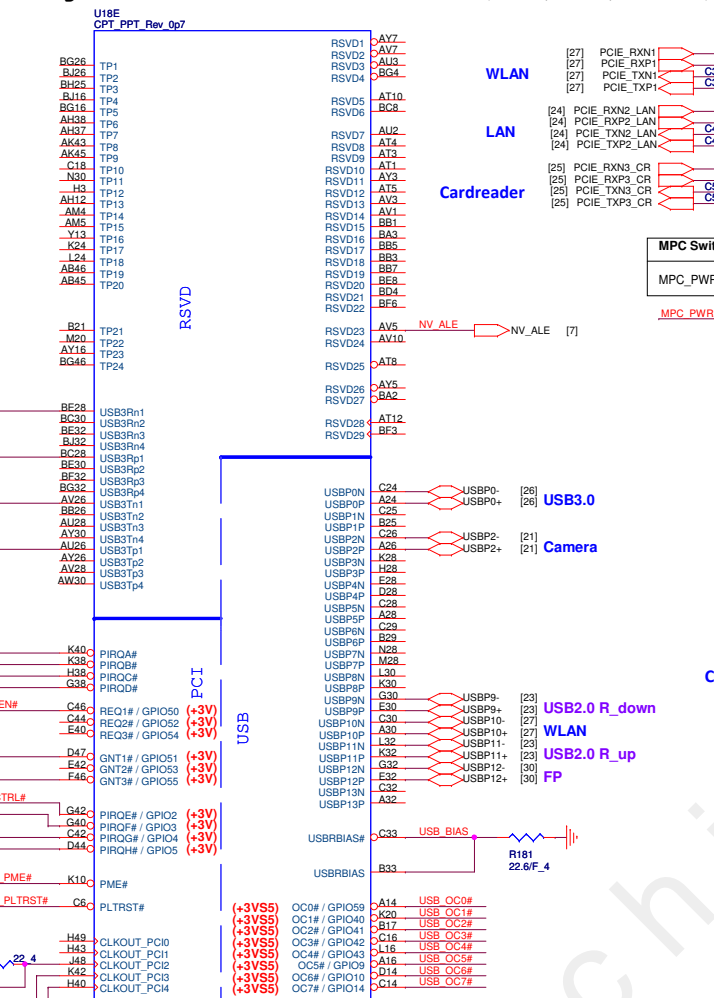
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V - R292 - 1K/F 4 - SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V - R127 - 1K/F 4 - PCH_GNT3# [8] +3V - R125 - 10K/F 4
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V - R228 - 330K 4 - PCH_INVRMEN
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 - R182 - 1K/F 4 - ACZ_SDOOUT [29]
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	+3V - R497 - 1K/F 4 - BBS_BIT0 +3V - R132 - 1K/F 4 - BBS_BIT1 [8]
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V - R267 - 1K/F 4 - INV_ALE [8]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V - R484 - 2.2K 4 - R482 - 1K/F 4 - INV_CLE [9] +1.8V - R484 - 2.2K 4 - H_SNB_IVB# [2]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VSS - R191 - 1K/F 4 - ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3VSS - R187 - 1K/F 4 - ACZ_SDOOUT
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	
SPI_MOSI	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	

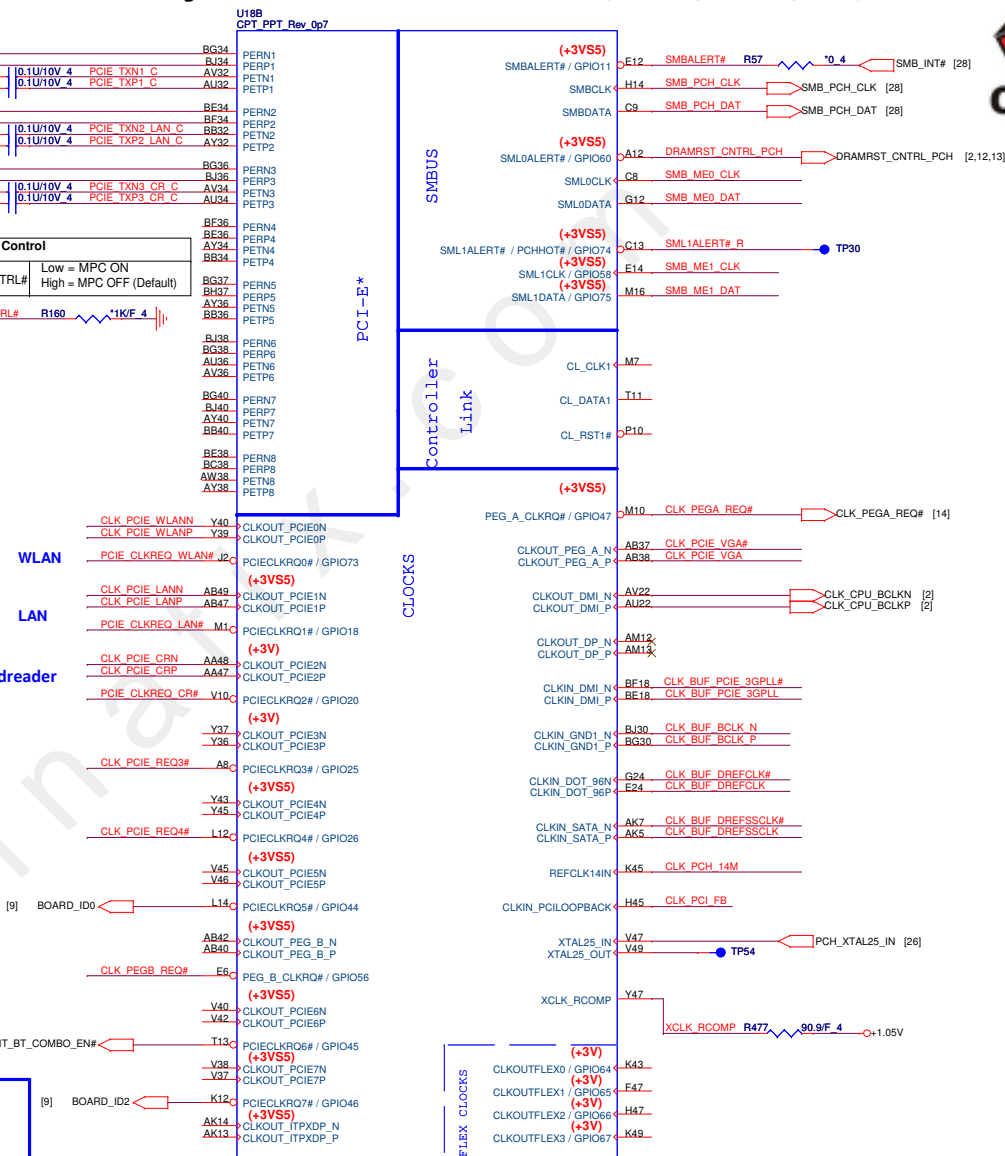
PCI/USB OC# Pull-up (CLG)



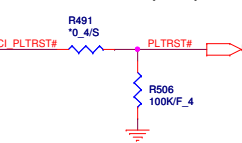
Cougar Point-M/Panther Point (PCI,USB,NVRAM)



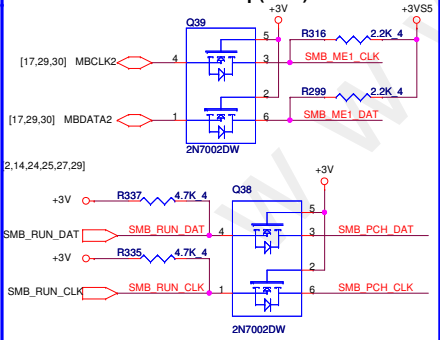
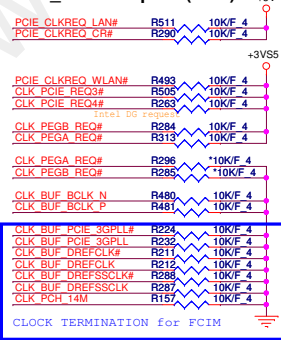
Cougar Point-M/Panther Point (PCI-E, SMBUS, CLK)



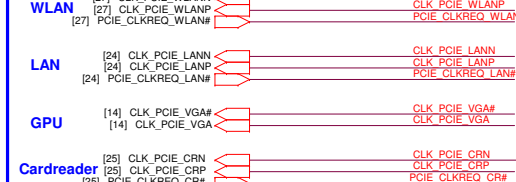
PLTRST#(CLG)



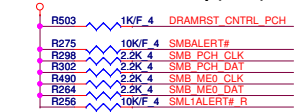
SMBus/Pull-up(CLG)

**CLK REQ/Strap Pin(CLG)**

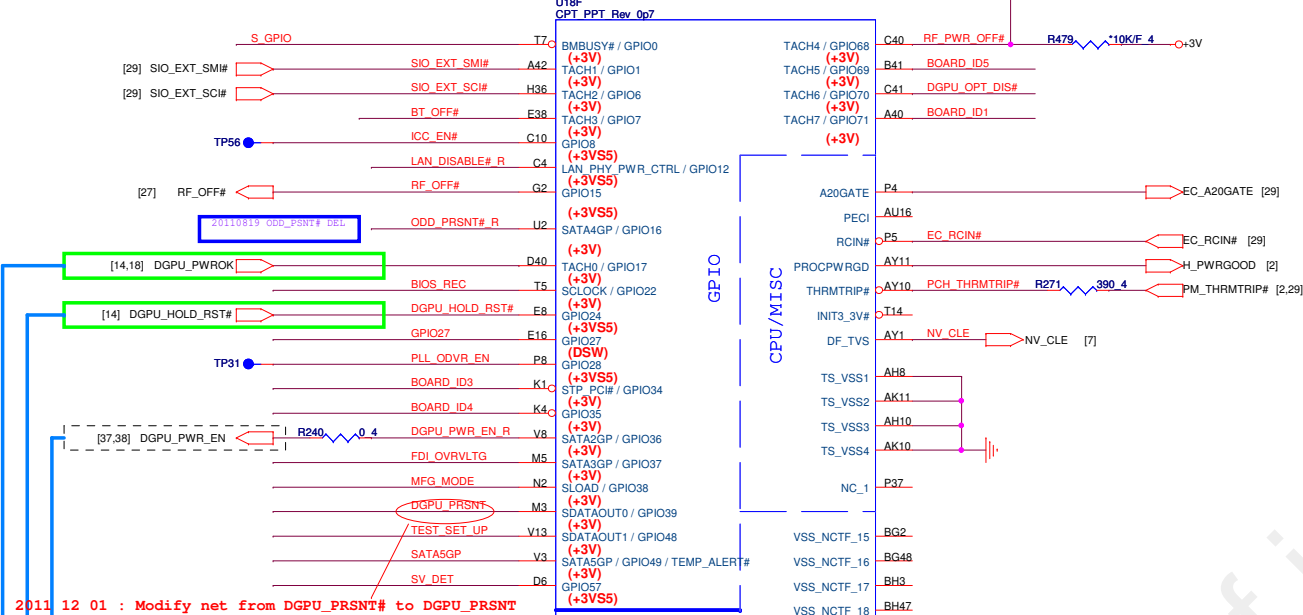
PCIE Clock [2]



SMBus/Pull-up(CLG)



Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



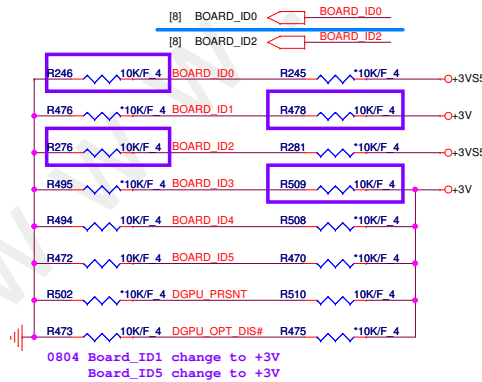
OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

BOARD_ID[3:0]	Model Name
0000	QLGA
0001	TWC
0010	JW2
0011	TBD
0100	LG3
0101	LG5
0110	LG2C
0111	LG4C
1000	TBD
1001	JW6/JW7
1010	JW3

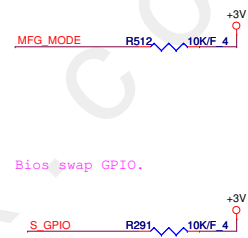
Chief River BOARD ID SETTING

BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO71	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
BOARD_ID3	GPIO34	MODEL BIT3
BOARD_ID4	GPIO35	No Dolby=0, Dolby=1
BOARD_ID5	GPIO69	HM76=0,HM70=1
DGPU_PRST	GPIO39	Optimus=1, UMA=0
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1

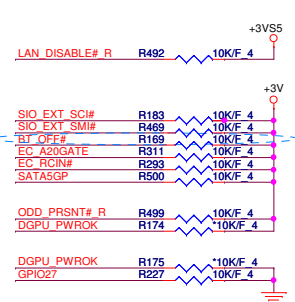
20110816 Define BRD_ID[3:0]



MFG-TEST



GPIO Pull-up/Pull-down(CLG)



Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

BIOS RECOVERY High = Disable (Default)
Low = Enable

TEST_SET_UP
High = Strong (Default)

TEST DETECT
Low = Default

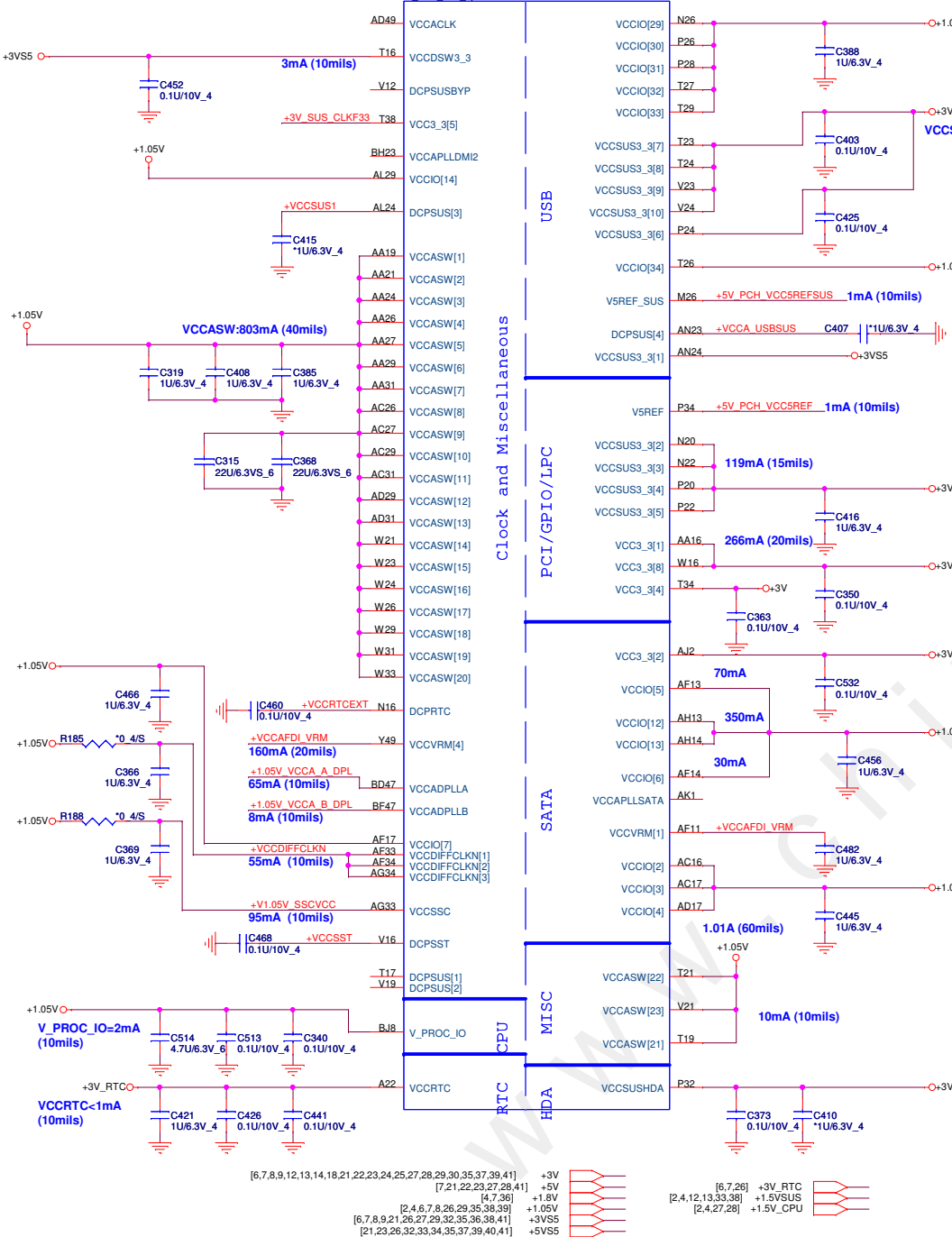
SATA2GP/GPIO36 Reserved only

FDI TERMINATION VOLTAGE OVERRIDE Reserved only

[6,7,8,10,12,13,14,18,21,22,23,24,25,27,28,29,30,35,37,39,41] +3V
[6,7,8,10,21,26,27,29,32,35,36,38,41] +3VSS

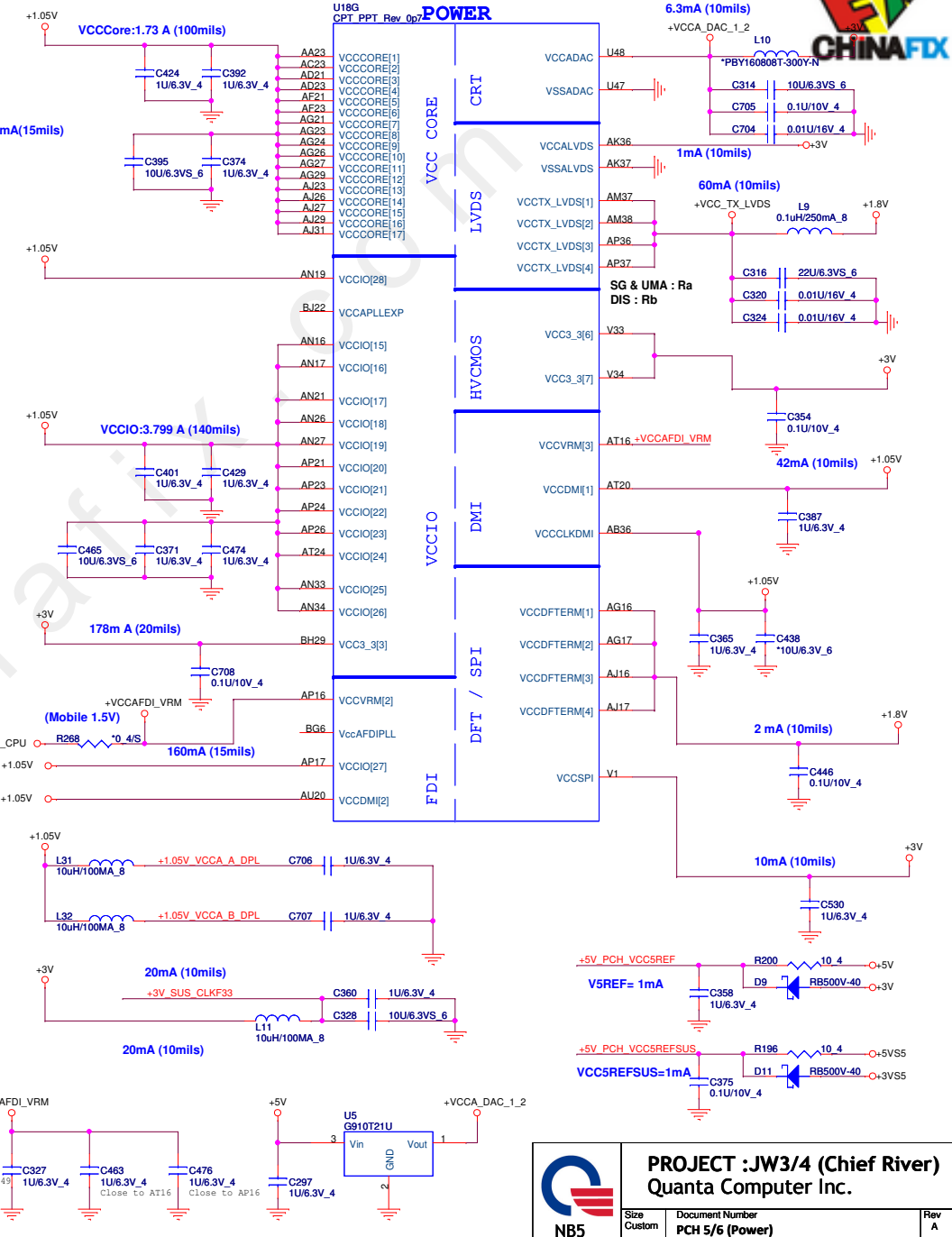
Cougar Point/Panther Point (POWER)

U18J
CPT_PPT_Rev_0p7
POWER



Cougar Point/Panther Point (POWER)

U18G
CPT_PPT_Rev_0p7
POWER



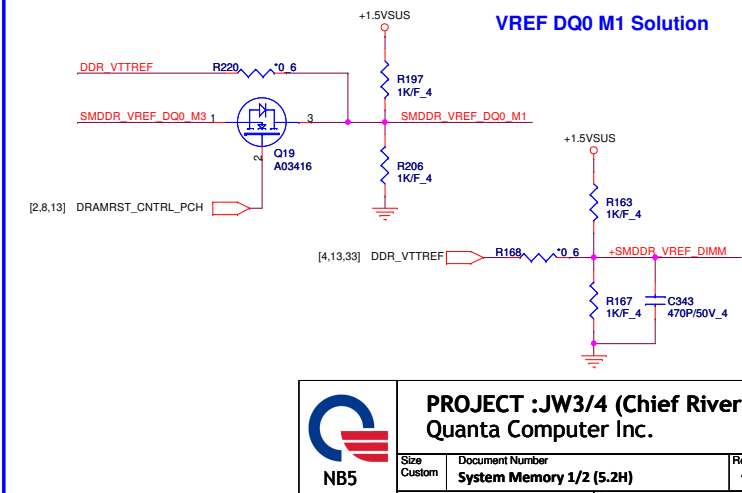
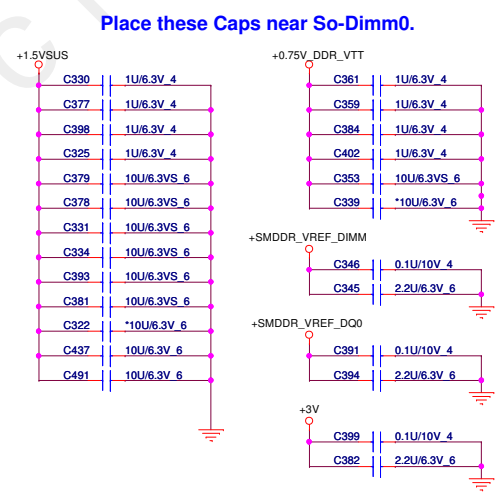
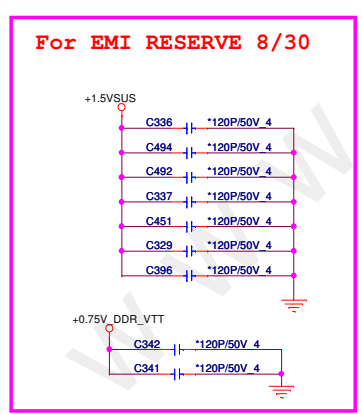
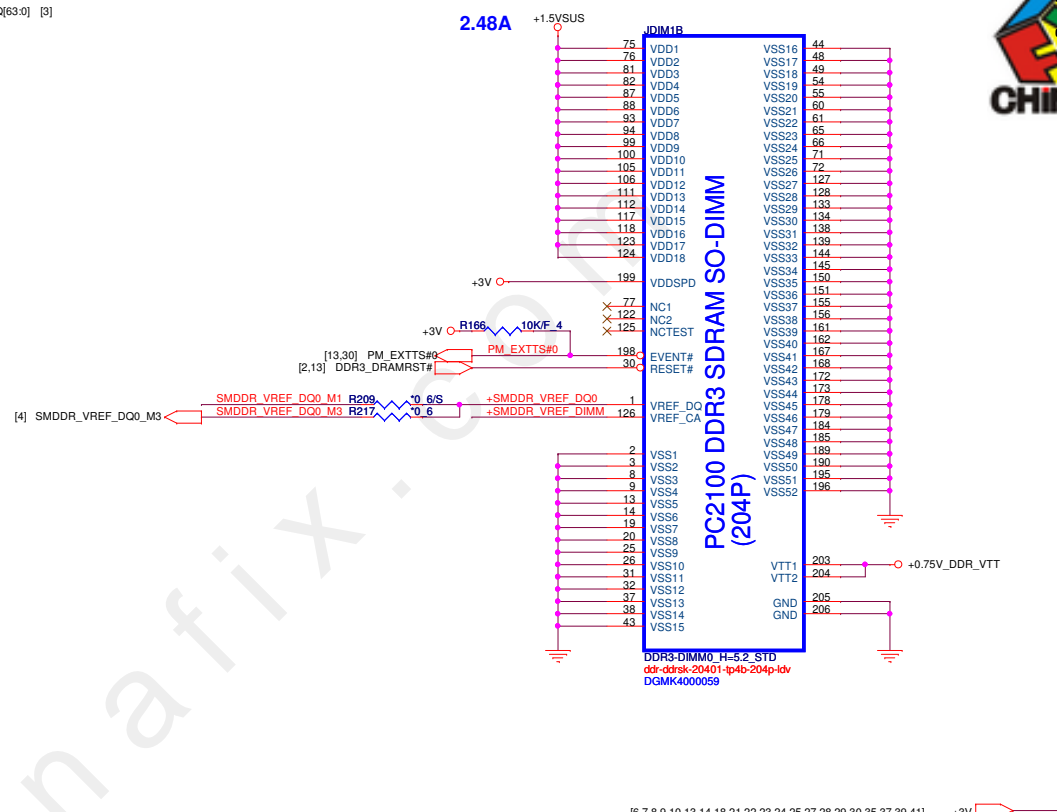
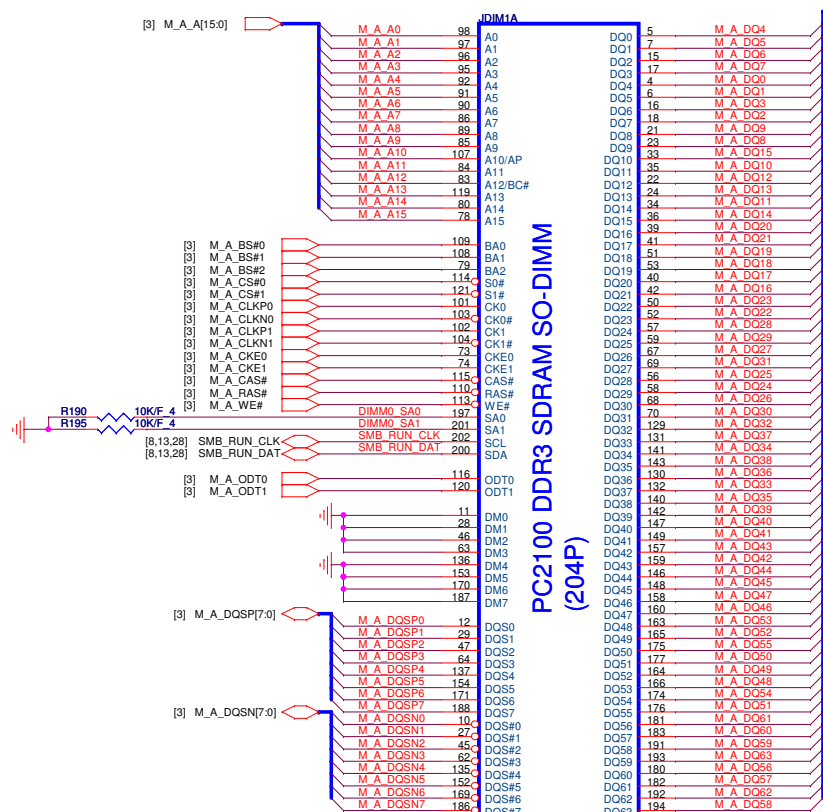
Cougar Point/Panther Point (GND)

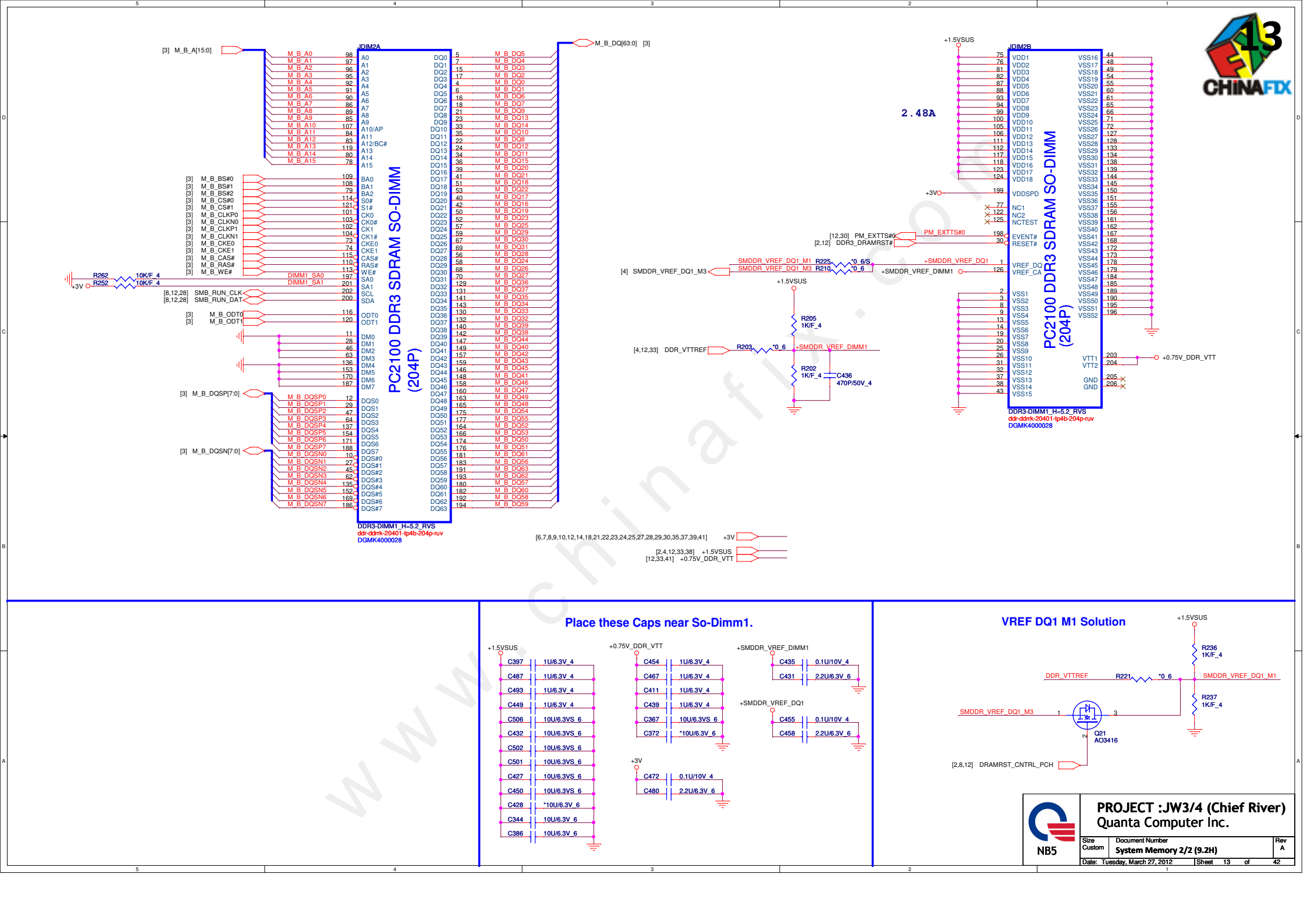
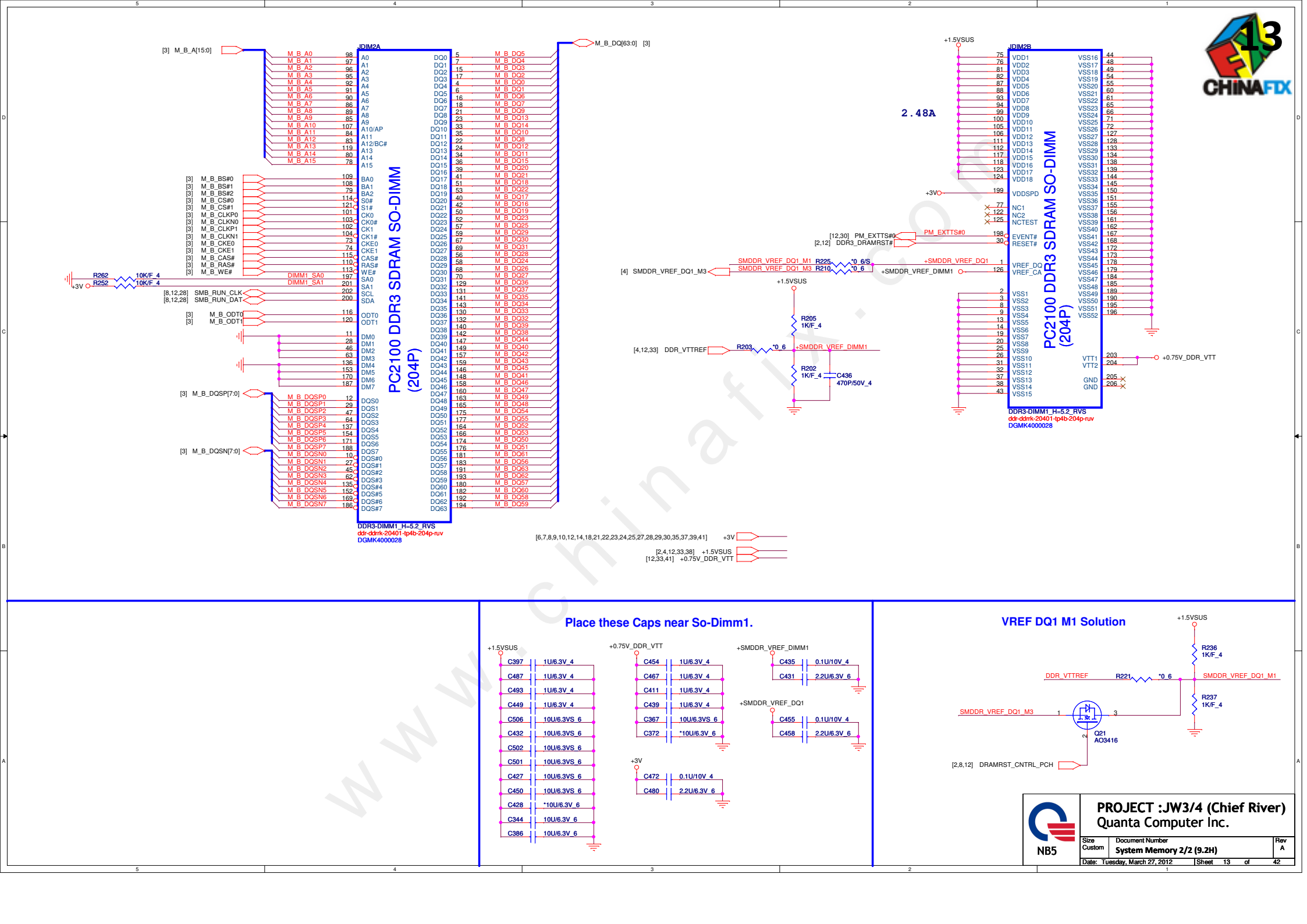
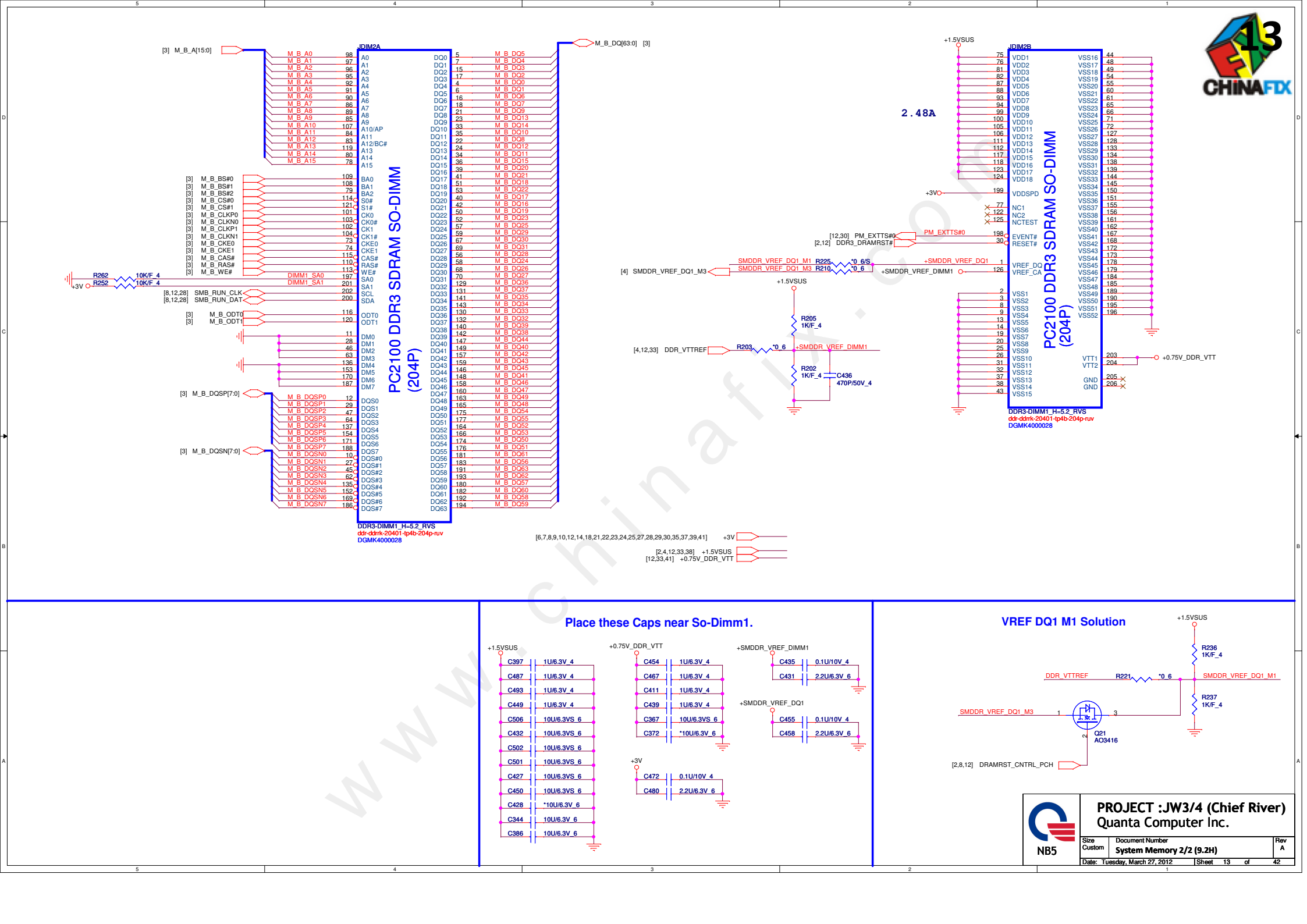
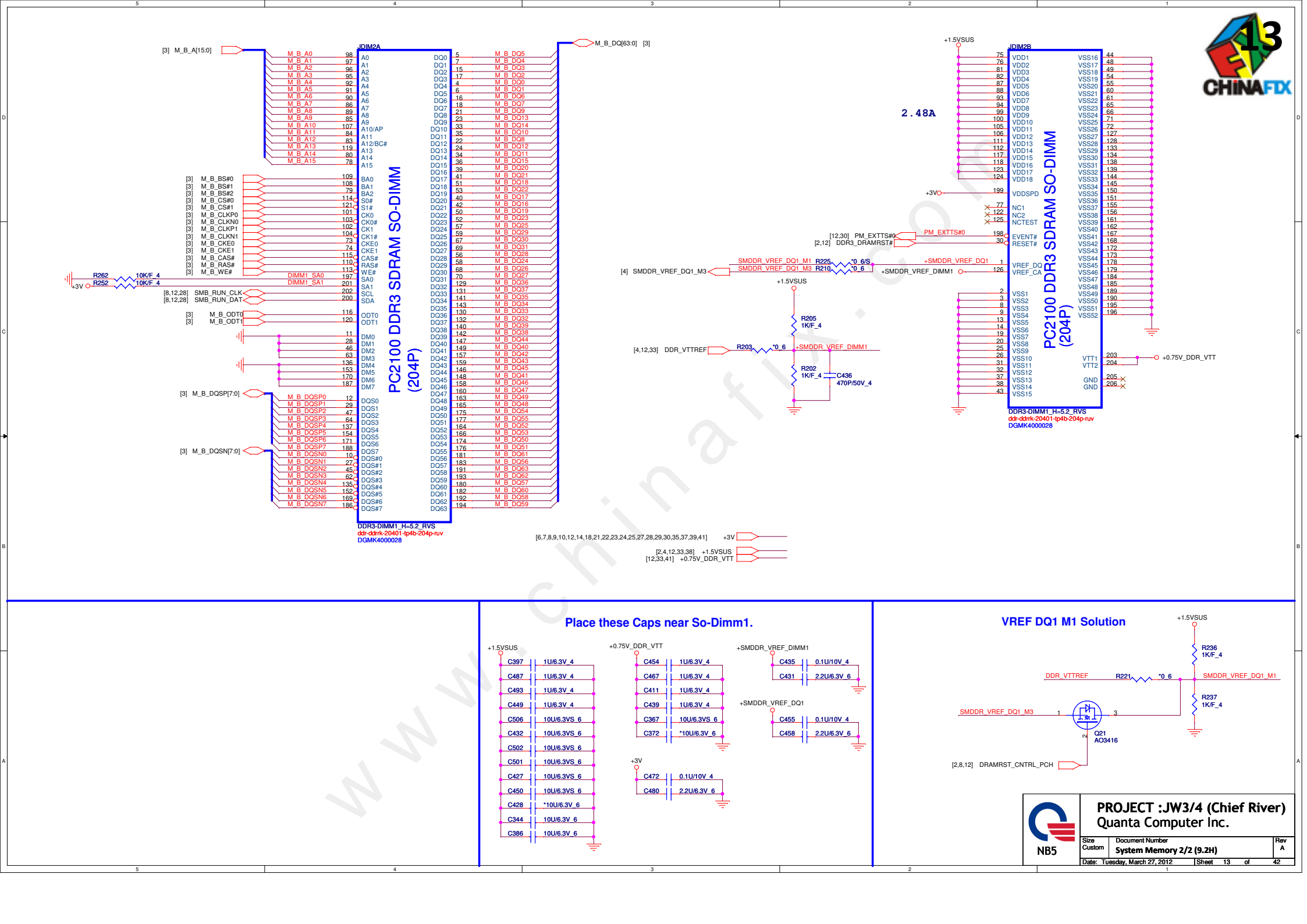
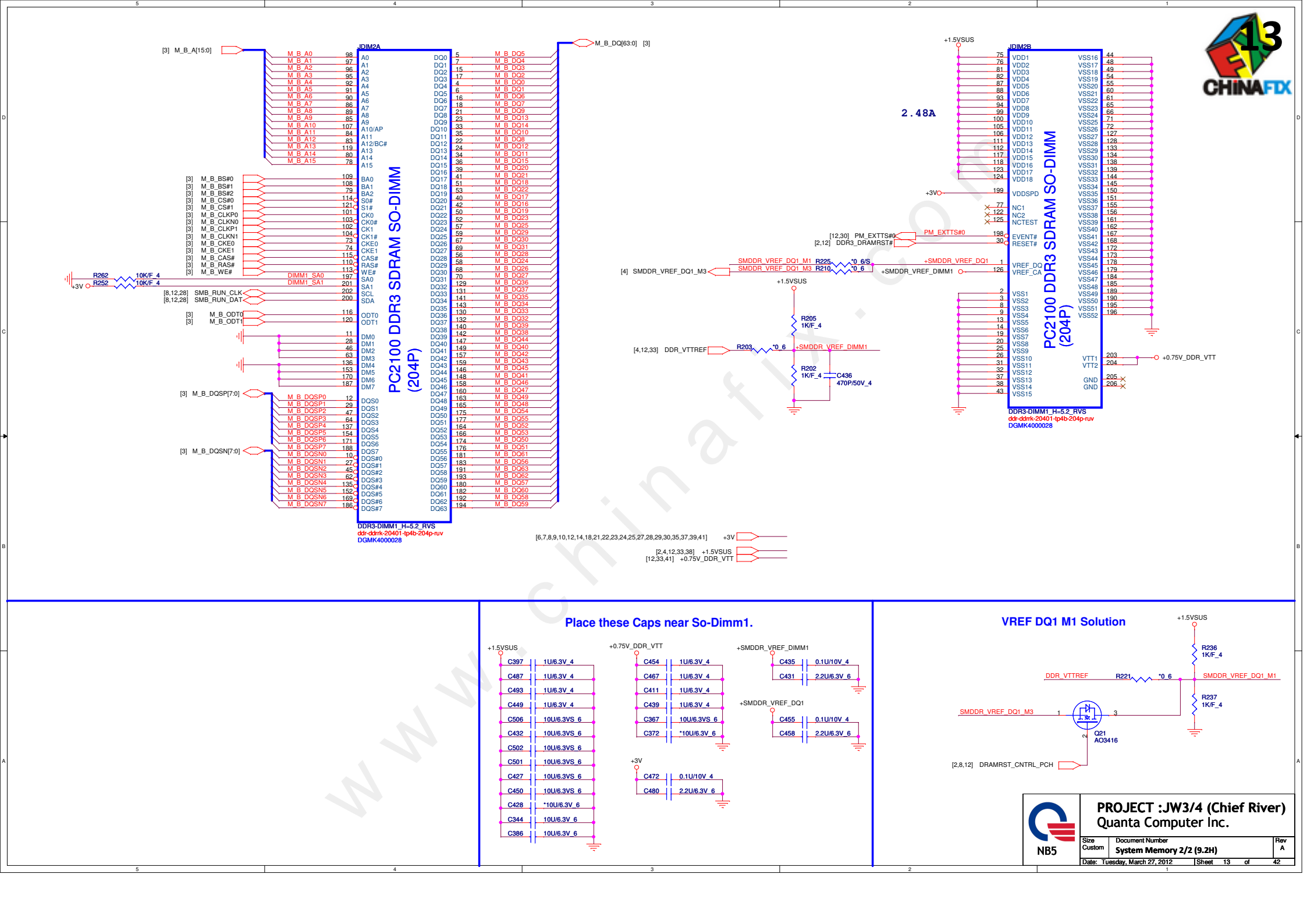
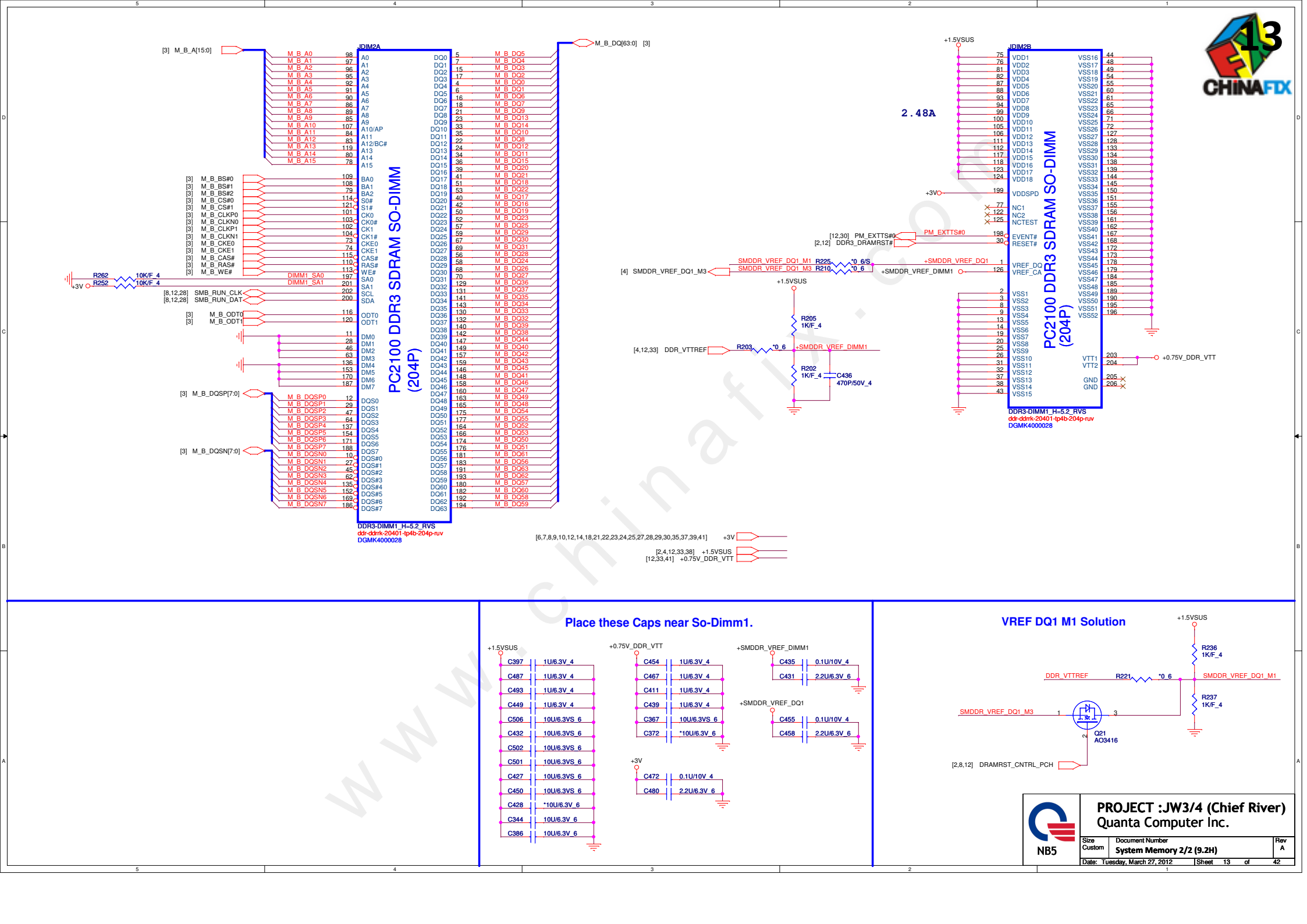
U18I		
CPT PPT Rev Op7		
AY4	VSS[159]	VSS[259] H46
AY42	VSS[160]	K18
AY46	VSS[161]	VSS[260] K26
AY8	VSS[162]	VSS[261] K39
B11	VSS[163]	VSS[262] K46
B12	VSS[164]	VSS[263] K7
B19	VSS[165]	VSS[264] L18
B23	VSS[166]	VSS[265] L2
B27	VSS[167]	VSS[266] L20
B31	VSS[168]	VSS[267] L26
B35	VSS[169]	VSS[268] L28
B39	VSS[170]	VSS[269] L36
B7	VSS[171]	VSS[270] L48
F45	VSS[172]	VSS[271] M12
BB12	VSS[173]	VSS[272] P16
BB16	VSS[174]	VSS[273] M18
BB20	VSS[175]	VSS[274] M22
BB22	VSS[176]	VSS[275] M24
BB24	VSS[177]	VSS[276] M30
BB28	VSS[178]	VSS[277] M32
BB30	VSS[179]	VSS[278] M34
BB38	VSS[180]	VSS[279] M38
BB4	VSS[181]	VSS[280] M4
BB46	VSS[182]	VSS[281] M42
BC14	VSS[183]	VSS[282] M46
BC18	VSS[184]	VSS[283] M8
BC2	VSS[185]	VSS[284] N18
BC22	VSS[186]	VSS[285] P30
BC26	VSS[187]	VSS[286] N47
BC32	VSS[188]	VSS[287] P11
BC34	VSS[189]	VSS[288] P18
BC36	VSS[190]	VSS[289] T33
BC40	VSS[191]	VSS[290] P40
BC42	VSS[192]	VSS[291] P43
BC48	VSS[193]	VSS[292] P47
BD46	VSS[194]	VSS[293] P7
BD5	VSS[195]	VSS[294] R2
BE22	VSS[196]	VSS[295] R48
BE26	VSS[197]	VSS[296] T12
BE40	VSS[198]	VSS[297] T31
BE10	VSS[199]	VSS[298] T37
BE12	VSS[200]	VSS[299] T4
BF16	VSS[201]	VSS[300] W34
BF20	VSS[202]	VSS[301] T46
BF22	VSS[203]	VSS[302] T47
BF24	VSS[204]	VSS[303] T8
BF26	VSS[205]	VSS[304] V11
BF28	VSS[206]	VSS[305] V17
BD3	VSS[207]	VSS[306] V26
BF40	VSS[208]	VSS[307] V27
BF38	VSS[209]	VSS[308] V29
BF40	VSS[210]	VSS[309] V31
BF8	VSS[211]	VSS[310] V36
RG17	VSS[212]	VSS[311] V39
RG21	VSS[213]	VSS[312] V43
RG33	VSS[214]	VSS[313] V7
RG44	VSS[215]	VSS[314] W17
BG8	VSS[216]	VSS[315] W19
BH11	VSS[217]	VSS[316] W2
BH15	VSS[218]	VSS[317] W27
BH17	VSS[219]	VSS[318] W48
BH19	VSS[220]	VSS[319] Y12
H10	VSS[221]	VSS[320] Y38
BH27	VSS[222]	VSS[321] Y4
BH31	VSS[223]	VSS[322] Y42
BH33	VSS[224]	VSS[323] Y46
BH35	VSS[225]	VSS[324] Y8
BH39	VSS[226]	VSS[325] BG29
BH43	VSS[227]	VSS[326] N24
BH7	VSS[228]	VSS[327] A3
D3	VSS[229]	VSS[328] AD47
D12	VSS[230]	VSS[329] B43
D16	VSS[231]	VSS[330] AH40
D18	VSS[232]	VSS[331] BG41
D22	VSS[233]	VSS[332] G14
D24	VSS[234]	VSS[333] H16
D26	VSS[235]	VSS[334] T36
D30	VSS[236]	VSS[335] BG22
D32	VSS[237]	VSS[336] CG24
D34	VSS[238]	VSS[337] AP13
D38	VSS[239]	VSS[338] M14
D42	VSS[240]	VSS[339] AP3
D8	VSS[241]	VSS[340] AP1
E18	VSS[242]	VSS[341] BE16
E26	VSS[243]	VSS[342] BC16
G18	VSS[244]	VSS[343] BG28
G20	VSS[245]	VSS[344] BJ28
G26	VSS[246]	VSS[345]
G28	VSS[247]	VSS[346]
G36	VSS[248]	VSS[347]
G46	VSS[249]	VSS[348]
H12	VSS[250]	VSS[349]
H18	VSS[251]	VSS[350]
H22	VSS[252]	VSS[351]
H24	VSS[253]	VSS[352]
H26	VSS[254]	
H30	VSS[255]	
H32	VSS[256]	
H34	VSS[257]	
F3	VSS[258]	

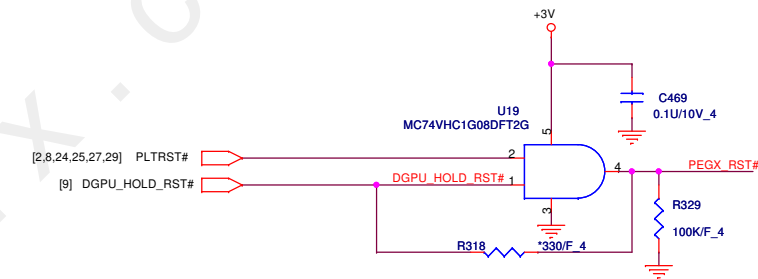
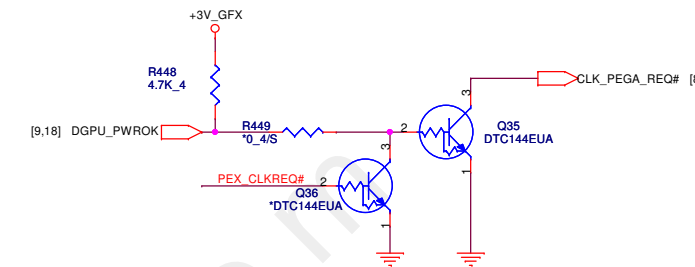
Cougar Point/Panther Point (GND)

U18H		
CPT PPT Rev Op7		
H5	VSS[0]	
AA17	VSS[1]	VSS[80] AK38
AA2	VSS[2]	VSS[81] AK4
AA3	VSS[3]	VSS[82] AK42
AA33	VSS[4]	VSS[83] AK46
AA34	VSS[5]	VSS[84] AK8
AB11	VSS[6]	VSS[85] AL16
AB14	VSS[7]	VSS[86] AL17
AB39	VSS[8]	VSS[87] AL19
AB4	VSS[9]	VSS[88] AL2
AB43	VSS[10]	VSS[89] AL21
P16	VSS[11]	VSS[90] AL23
AB7	VSS[12]	VSS[91] AL26
AC19	VSS[13]	VSS[92] AL27
AC2	VSS[14]	VSS[93] AL31
AC21	VSS[15]	VSS[94] AL33
AC24	VSS[16]	VSS[95] AL34
AC33	VSS[17]	VSS[96] AL48
AC34	VSS[18]	VSS[97] AM11
AC48	VSS[19]	VSS[98] AM14
AD10	VSS[20]	VSS[99] AM36
AD11	VSS[21]	VSS[100] AM39
AD12	VSS[22]	VSS[101] AM43
AD13	VSS[23]	VSS[102] AM45
AD19	VSS[24]	VSS[103] AM46
AD24	VSS[25]	VSS[104] AM7
AD26	VSS[26]	VSS[105] AN2
AD27	VSS[27]	VSS[106] AN29
AD33	VSS[28]	VSS[107] AN3
AD34	VSS[29]	VSS[108] AN31
AD36	VSS[30]	VSS[109] AP12
AD37	VSS[31]	VSS[110] AP19
AD38	VSS[32]	VSS[111] AP28
AD39	VSS[33]	VSS[112] AP30
AD4	VSS[34]	VSS[113] AP32
AD40	VSS[35]	VSS[114] AP38
AD42	VSS[36]	VSS[115] AP4
AD43	VSS[37]	VSS[116] AP42
AD45	VSS[38]	VSS[117] AP46
AD46	VSS[39]	VSS[118] AP8
AD8	VSS[40]	VSS[119] AR2
AE2	VSS[41]	VSS[120] AR48
AE3	VSS[42]	VSS[121] AT11
AF10	VSS[43]	VSS[122] AT13
AF12	VSS[44]	VSS[123] AT18
AD14	VSS[45]	VSS[124] AT22
AD16	VSS[46]	VSS[125] AT26
AF18	VSS[47]	VSS[126] AT28
AF19	VSS[48]	VSS[127] AT30
AF24	VSS[49]	VSS[128] AT32
AF26	VSS[50]	VSS[129] AT34
AF27	VSS[51]	VSS[130] AT39
AF29	VSS[52]	VSS[131] AT42
AF31	VSS[53]	VSS[132] AT46
AF38	VSS[54]	VSS[133] AT7
AF4	VSS[55]	VSS[134] AU24
AF42	VSS[56]	VSS[135] AU30
AF46	VSS[57]	VSS[136] AV16
AF5	VSS[58]	VSS[137] AV20
AF7	VSS[59]	VSS[138] AV24
AF8	VSS[60]	VSS[139] AV30
AG19	VSS[61]	VSS[140] AV38
AG2	VSS[62]	VSS[141] AV4
AG31	VSS[63]	VSS[142] AV43
AG48	VSS[64]	VSS[143] AV8
AH11	VSS[65]	VSS[144] AW14
AH3	VSS[66]	VSS[145] AW18
AH36	VSS[67]	VSS[146] AW2
AH39	VSS[68]	VSS[147] AW22
BE10	VSS[69]	VSS[148] AW26
AH42	VSS[70]	VSS[149] AW28
AH46	VSS[71]	VSS[150] AW32
AH7	VSS[72]	VSS[151] AW34
AJ19	VSS[73]	VSS[152] AW36
AJ21	VSS[74]	VSS[153] AW40
AJ24	VSS[75]	VSS[154] AW48
AJ33	VSS[76]	VSS[155] AY11
AJ34	VSS[77]	VSS[156] AY12
AK12	VSS[78]	VSS[157] AY22
AK3	VSS[79]	VSS[158] AY28









Power up sequence

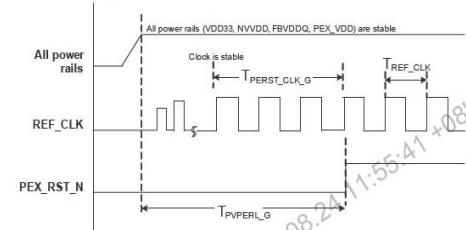
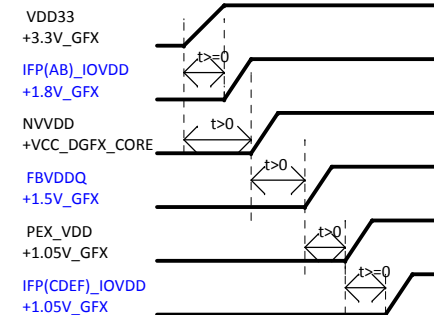
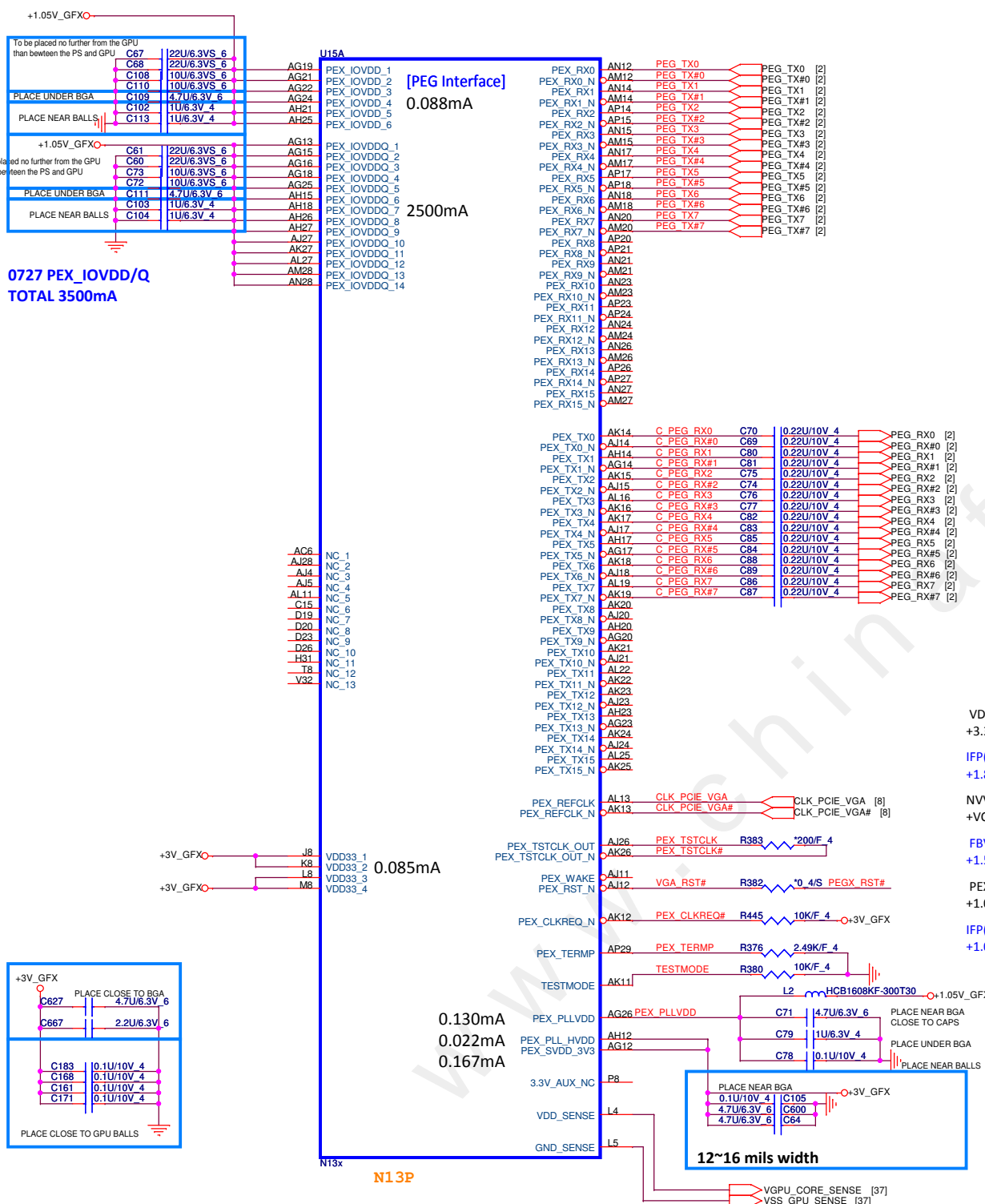
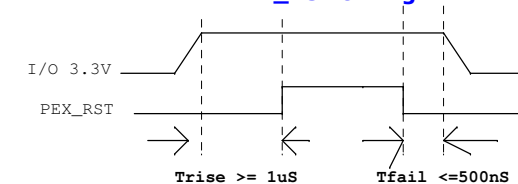


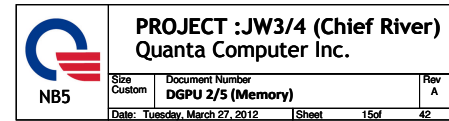
Figure 3-18. PEX_RST_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T_{PVPERL_G}	$T_{PVPERL_G} \geq 1\mu s$	
$T_{PEST_CLK_G}$	$T_{PEST_CLK_G} \geq 1T_{REF_CLK}$	

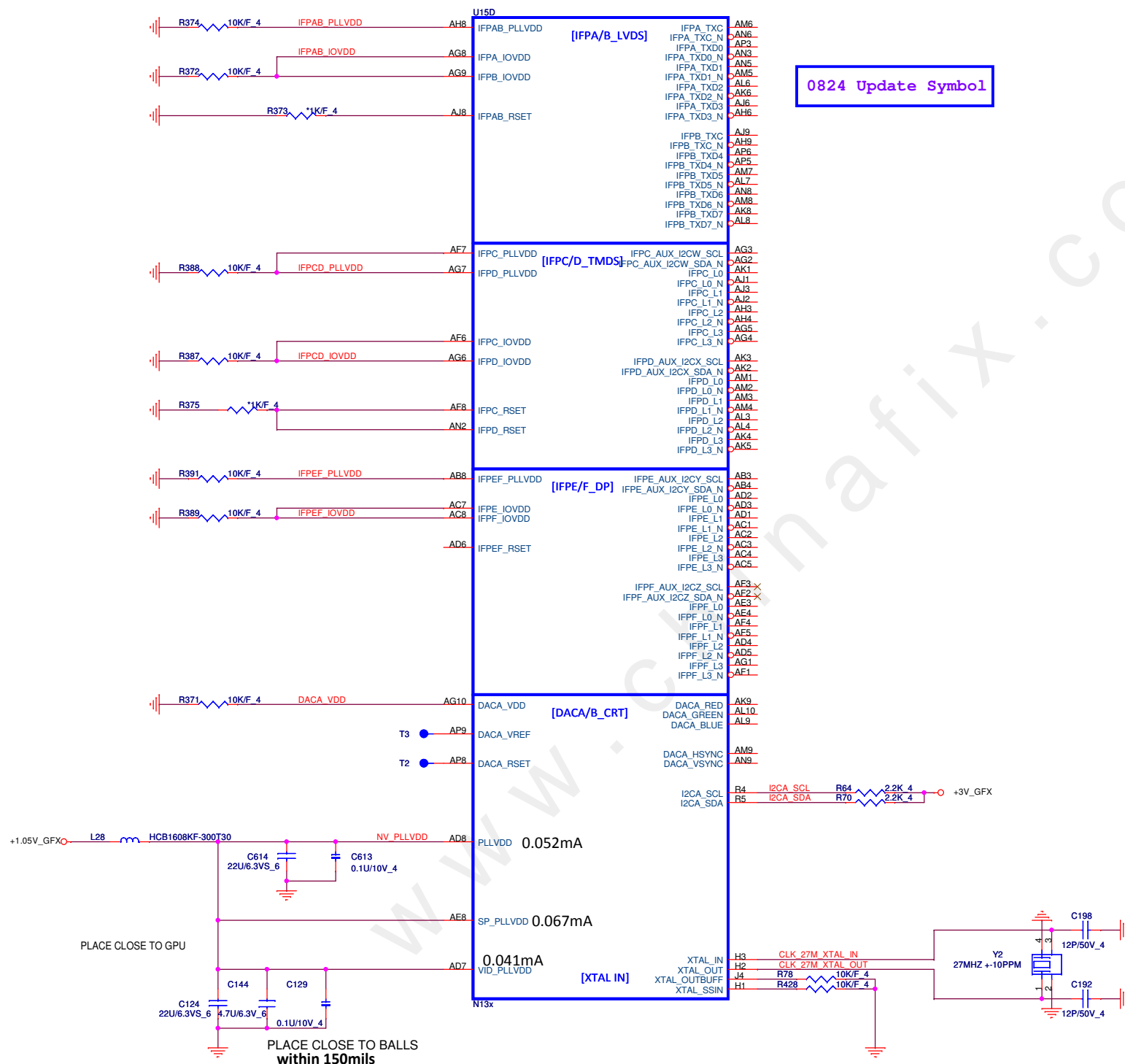
PEX_RST timing





[14,15,18,38] +1.05V_GFX
[14,17,18,37,38] +3V_GFX

0824 Update Symbol

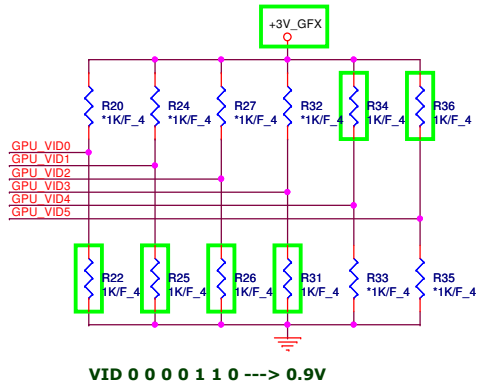
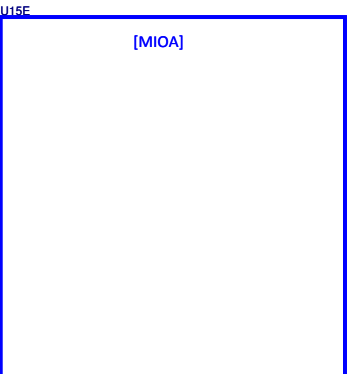




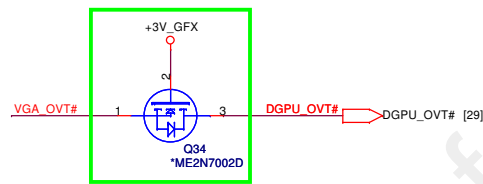
For N13M-GE2
ROM_SO PD 10K
ROM_SCLK PD 15K

N13M-GE2-A1 ID:0X0DEA
N13P-GS ID:0X0FD2

Net name	N13M-GE2	N13P-GS (QS)
ROM_SI		
ROM_SO	PD 10K	PU 10K
ROM_SCLK	PD 15K	PU 5K
STRAP0	PU 45K	PU 45K
STRAP1	PD 45K	PD 5K
STRAP2	PU 15K	PD 15K
STRAP3	UN-STUFF	PD 5K
STRAP4	UN-STUFF	PD 45K

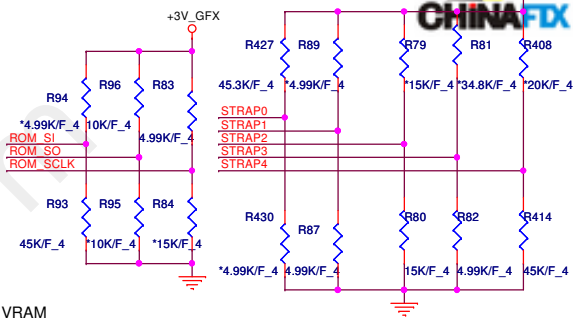


VID 0 0 0 0 1 1 0 ---> 0.9V



Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



Default: Hynix VRAM

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	1001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0011
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0111
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	XXXX
STRAP4	RESERVED	PCI SPEED CHANGE GEN3	PCI_MAX SPEED	DP_PLL_VDD33	XXXX

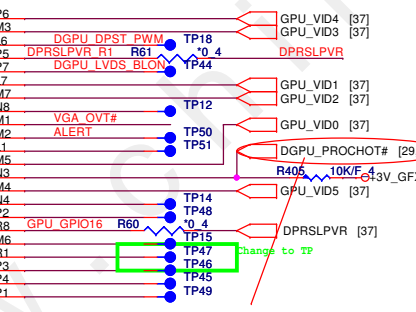
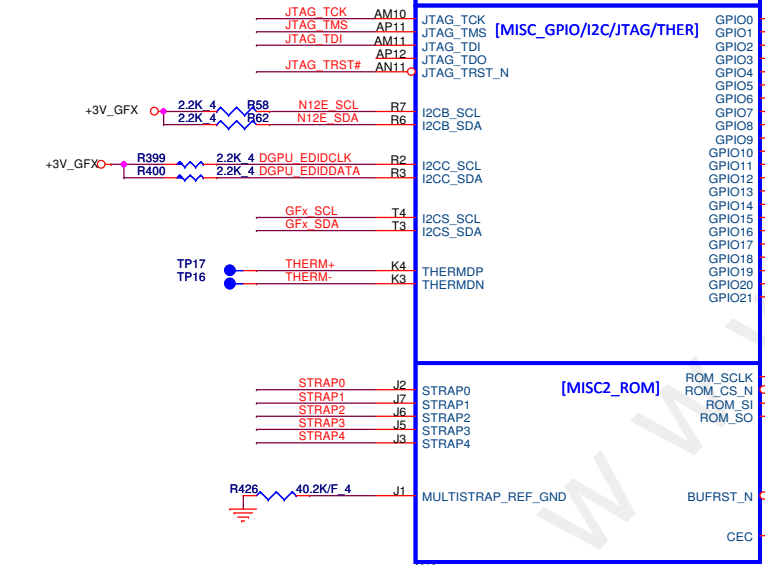
	N13M-GE2	N13P-GS
Ra	Un-Stuff	Stuff
Qa	Stuff	Un-Stuff

For N13M-GE2, N13M-GS (QS)
Default : 2G Samsung

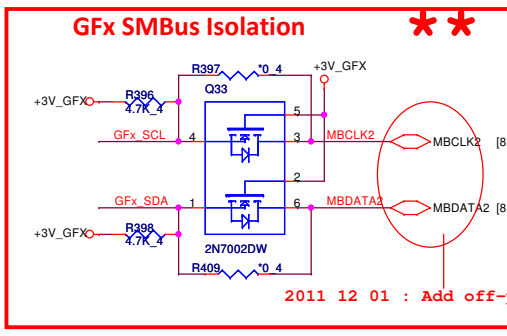
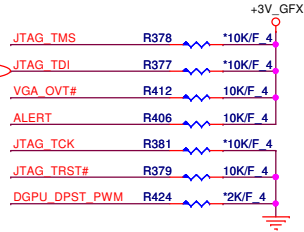
VRAM Configuration Table	
ROM_SI	
1G Hynix 64Mx16	-->15K PD
1G Samsung 64Mx16	-->20K PD
2G Hynix 128Mx16	-->35K PD
2G Samsung 128Mx16	-->45K PD

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	OUT	GPU_VID4	GPU CORE_VDD VID4
1	OUT	GPU_VID3	GPU CORE_VDD VID3
2	OUT	LCD_BL_PWM	LCD BACKLIGHT PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	GPU_VID1	GPU CORE_VDD VID1
6	OUT	GPU_VID2	GPU CORE_VDD VID2
7	OUT	3D VISION	3D VISION LEFT/RIGHT VISION
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF	MEMORY VREF CONTROL
11	OUT	GPU_VID0	GPU CORE_VDD VID0
12	IN	PWR_LEVEL	Power Detect ,HIGH=AC, LOW=DC
13	OUT	GPU_VID5	GPU CORE_VDD VID5
14	IN	HPD_AB	HOT PLUG DETECT FOR IFPAB
15	IN	HPD_C	HOT PLUG DETECT FOR IFPC
16	OUT	MEM VDD	MEMMORY VDD CONTROL
17	IN	HPD_D	HOT PLUG DETECT FOR IFPD
18	IN	HPD_E	HOT PLUG DETECT FOR IFPE
19	IN	HPD_F	HOT PLUG DETECT FOR IFPF
20/21		RESERVE	



2011 12 01 : Add net DGPU_PROCHOT#



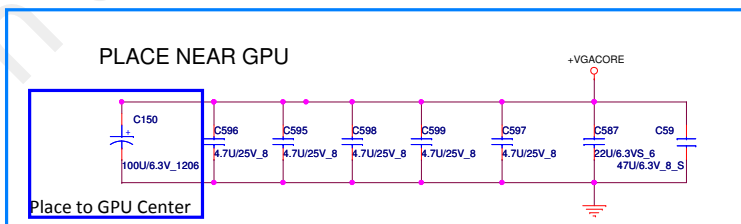
2011 12 01 : Add off-page connector

	N13M-GE2	N13P-GS
Stuff Rc		Un-stuff Rc



PROJECT :JW3/4 (Chief River)
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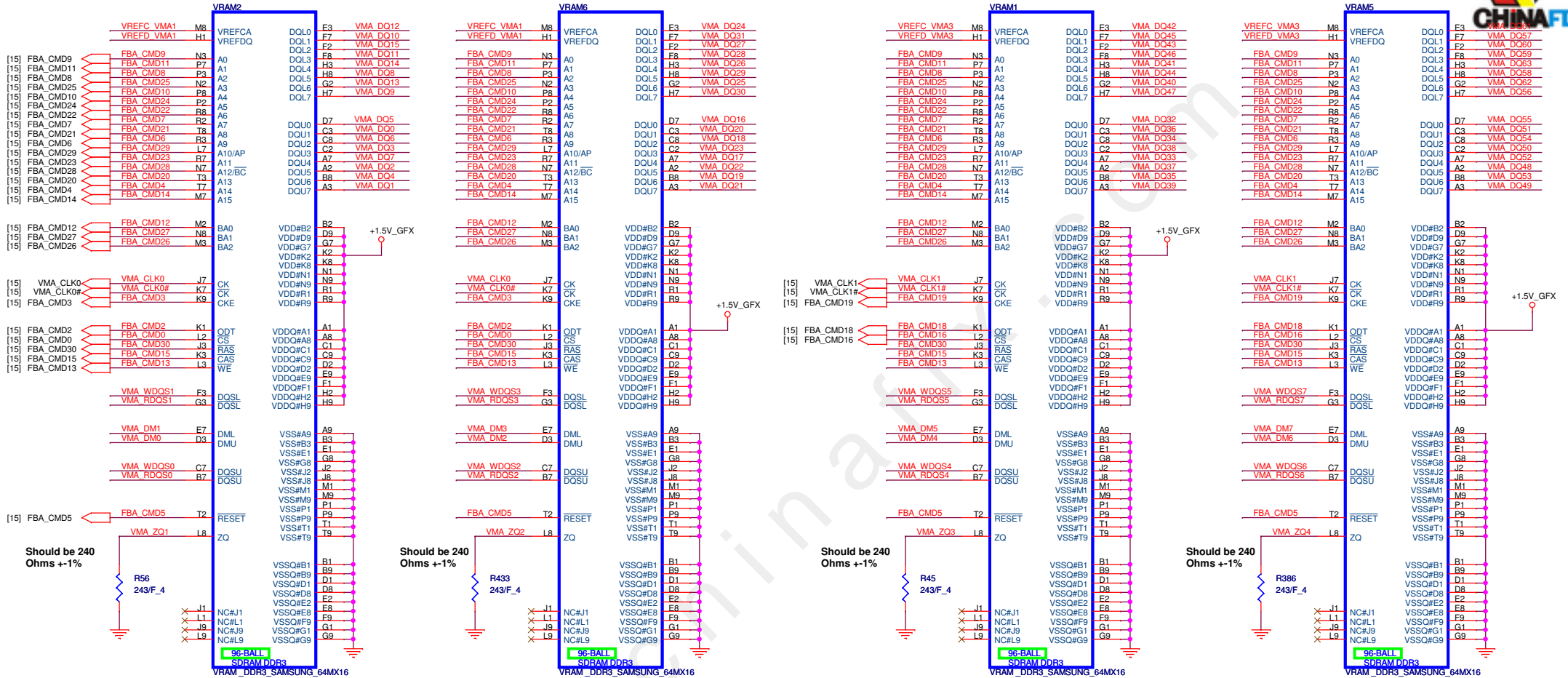
Size	Document Number	Rev
Custom	DGPU 4/5 (MIO/GPIO)	A
Date:	Tuesday, March 27, 2012	Sheet 17of 42



[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

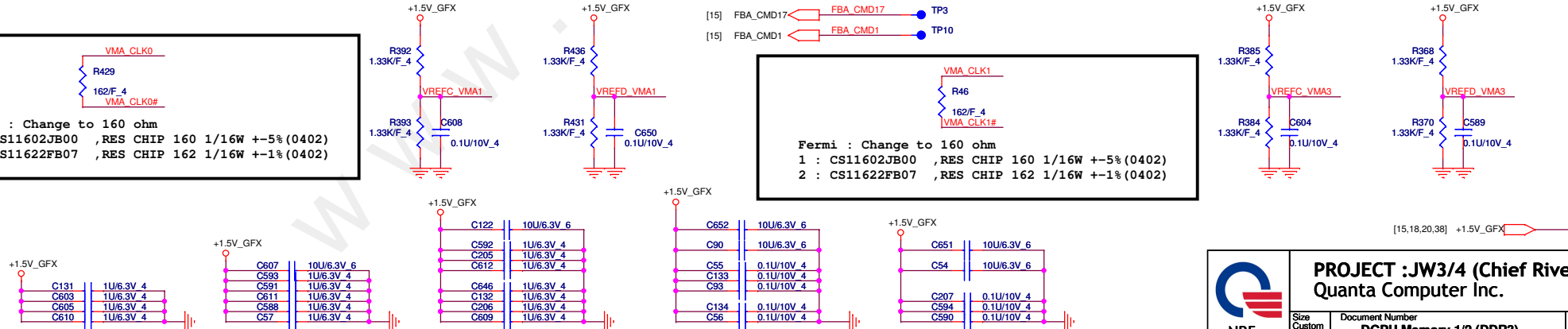
CHANNEL A: 256MB/512MB DDR3

900MHz VRAM size:
Samsung 64Mx16, P/N = AKD5EGGT500
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 64Mx16, P/N = AKD5LZWTW02
Hynix 128Mx16, P/N = AKD5MGWTW00



Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1% (0402)

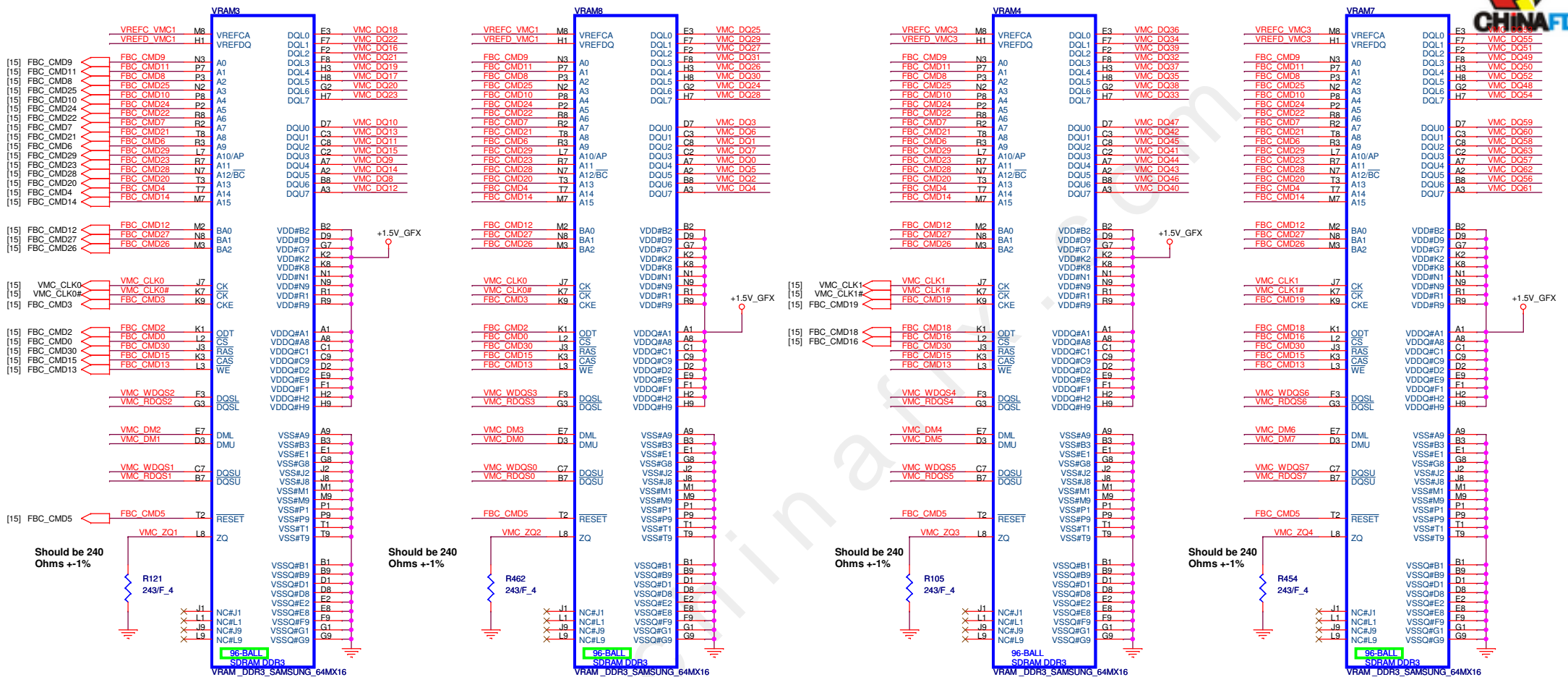
Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1% (0402)





[15] VMC_DQ[63..0]
[15] VMC_DM[7..0]
[15] VMC_WDQS[7..0]
[15] VMC_RDQS[7..0]

CHANNEL B: 256MB/512MB DDR3



Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1% (0402)

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1% (0402)

[15,18,19,38] 1.5V_GFX

900MHz VRAM size:
Samsung 64Mx16, P/N = AKD5EGGT500
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 64Mx16, P/N = AKD5LZWTW02
Hynix 128Mx16, P/N = AKD5MGWTW00

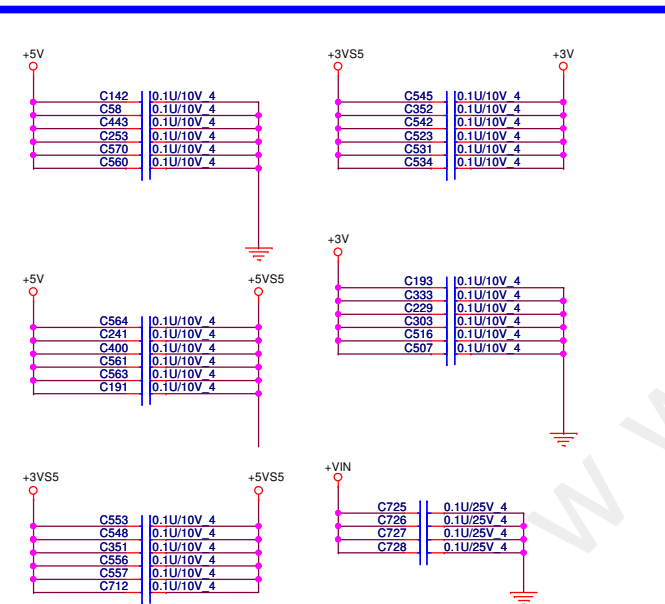
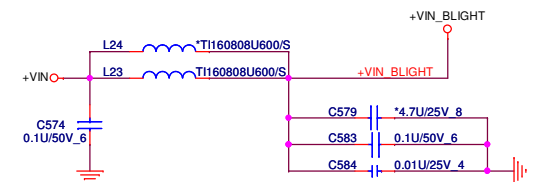
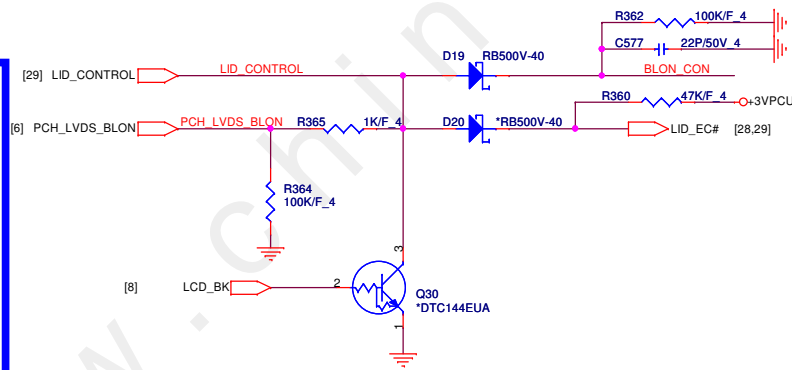
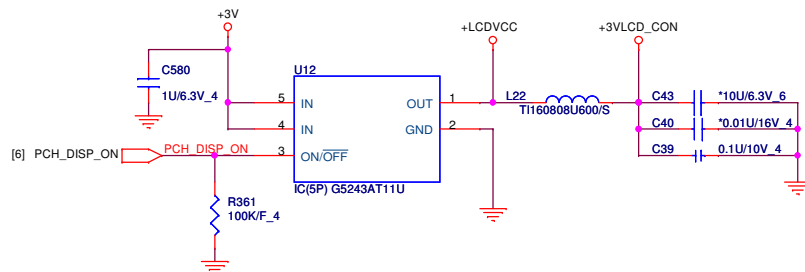
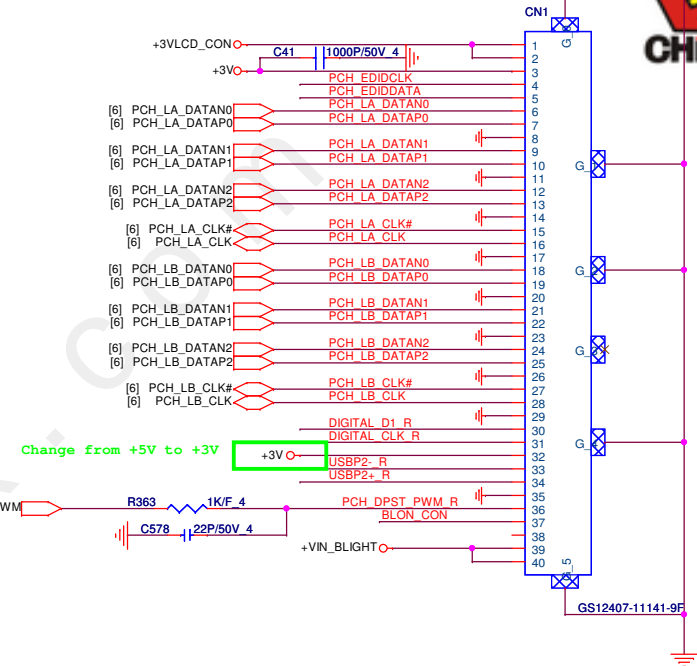
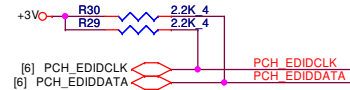
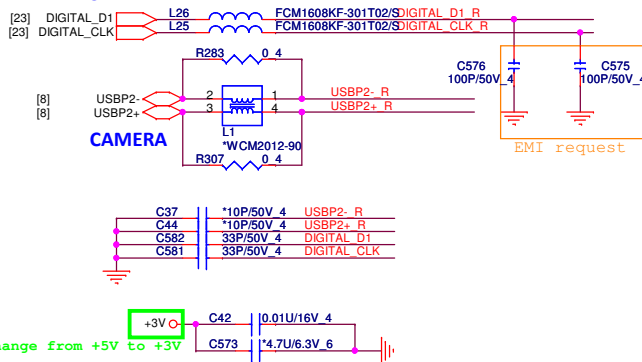


PROJECT : JW3/4 (Chief River)
Quanta Computer Inc.

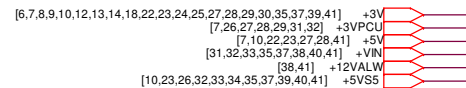
Size Custom	Document Number DGPU Memory 2/2 (DDR3)	Rev 1A
Date: Tuesday, March 27, 2012	Sheet 20 of 42	


USB Camera Connector

MIC

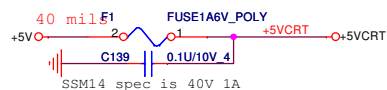


EMI/ESD
Stitching Cap(each 1" place one cap)

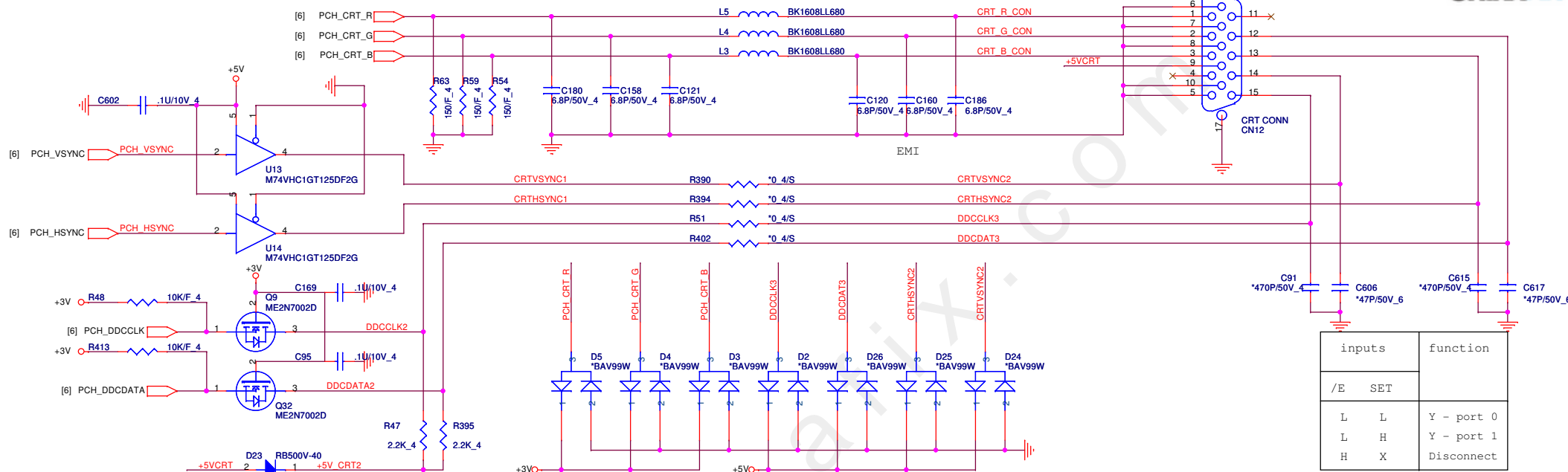


		PROJECT :JW3/4 (Chief River)	
		Quanta Computer Inc.	
Size	Custom	Document Number	LCD Connector (LVDS)
Date:	Tuesday, March 27, 2012	Sheet	21of 42

40 MIL

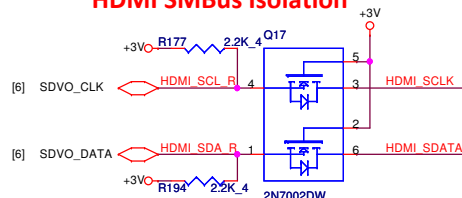


CRT PORT

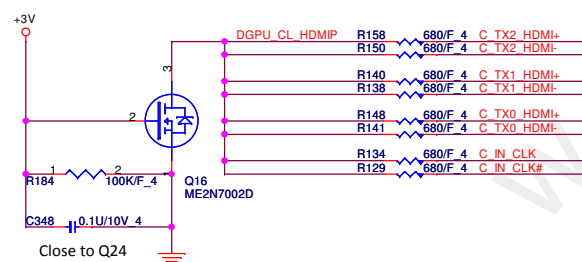


inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

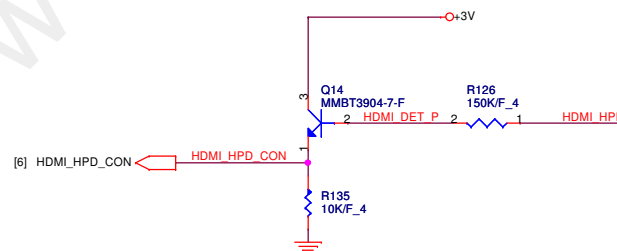
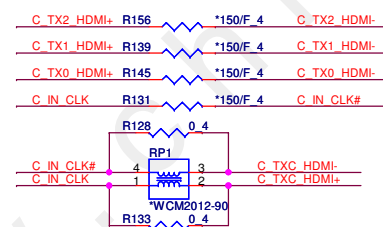
HDMI SMBus Isolation



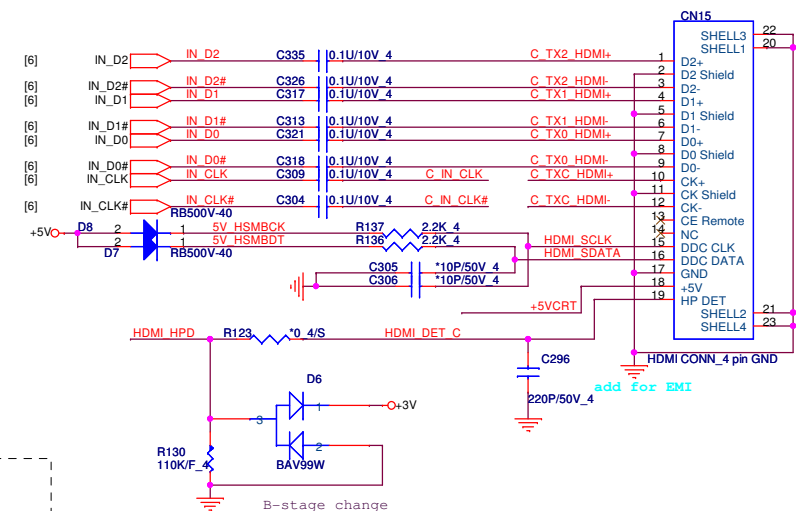
Close to HDMI connector



EMI Solution

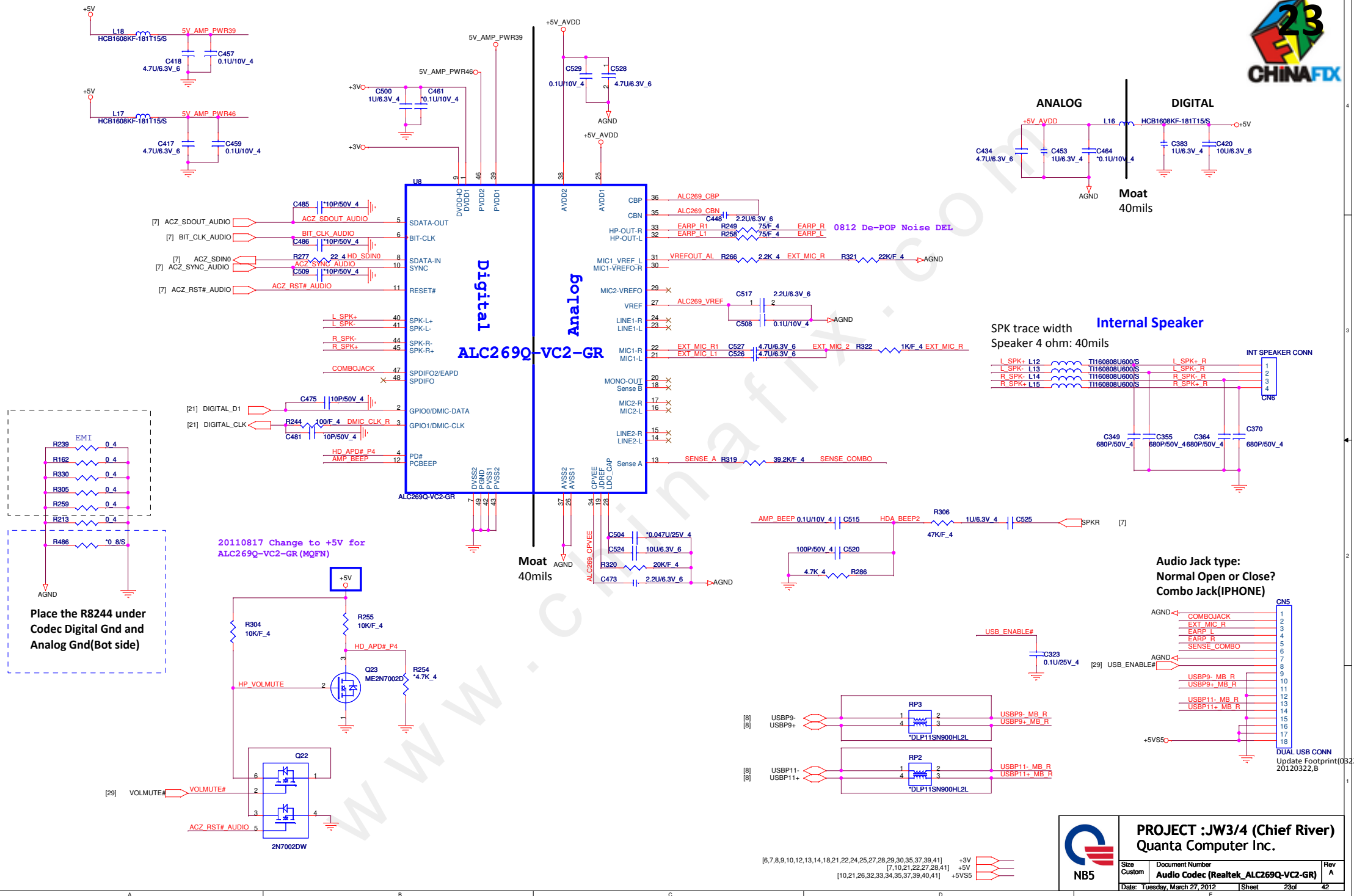


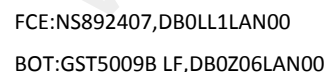
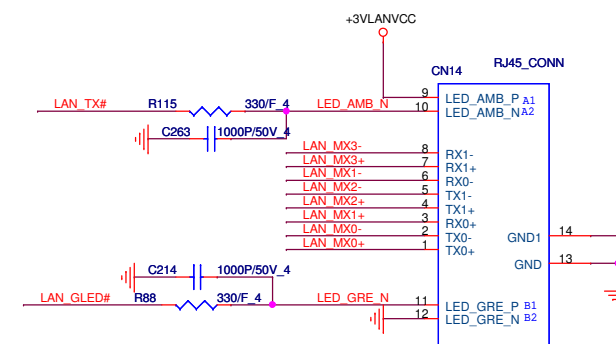
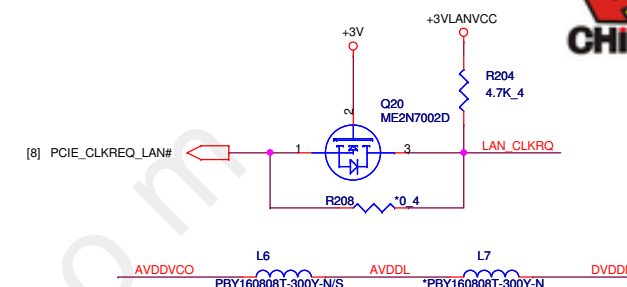
HDMI PORT

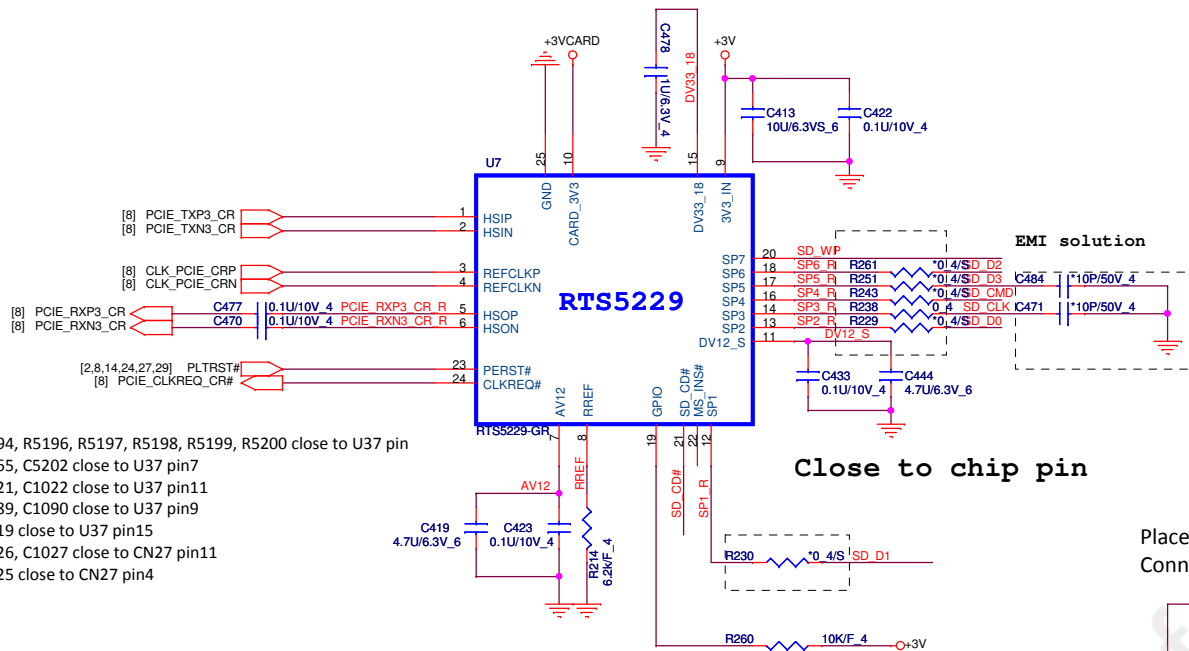


PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size Custom	Document Number CRT/HDMI Connector	Rev A
Date: Tuesday, March 27, 2012	Sheet 22 of	42

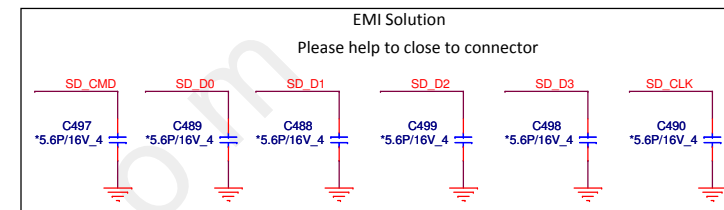






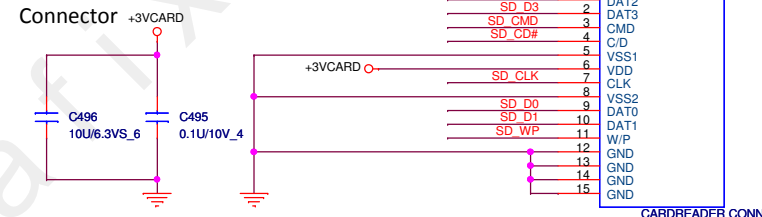
- Note:
1. R5194, R5196, R5197, R5198, R5199, R5200 close to U37 pin
 2. C5265, C5202 close to U37 pin7
 3. C1021, C1022 close to U37 pin11
 4. C1089, C1090 close to U37 pin9
 5. C1019 close to U37 pin15
 6. C1026, C1027 close to CN27 pin11
 7. C1025 close to CN27 pin4

Share Pin

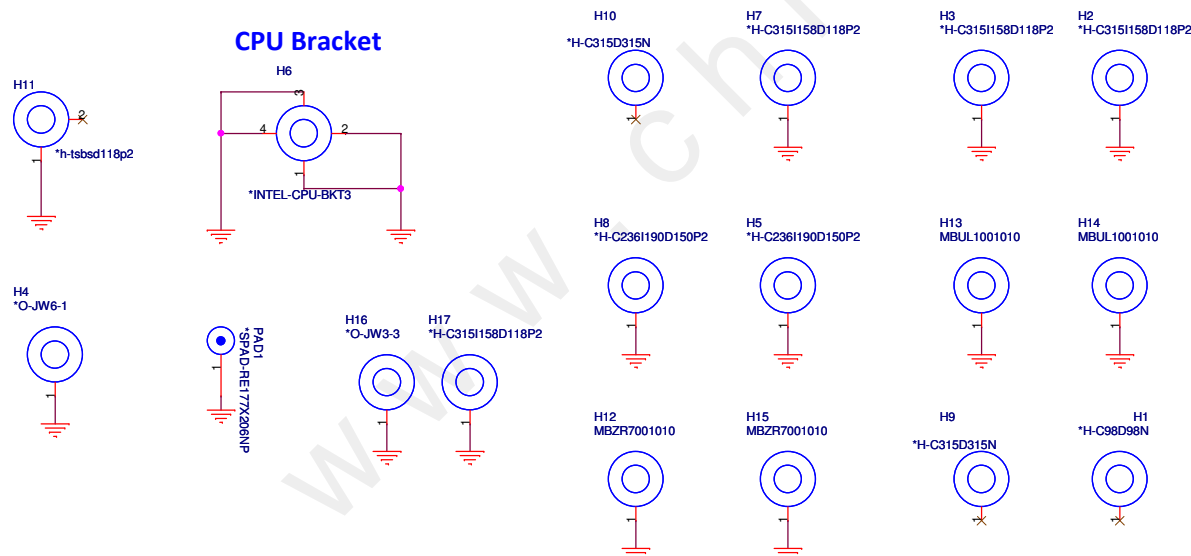


SD / MMC CARD READER

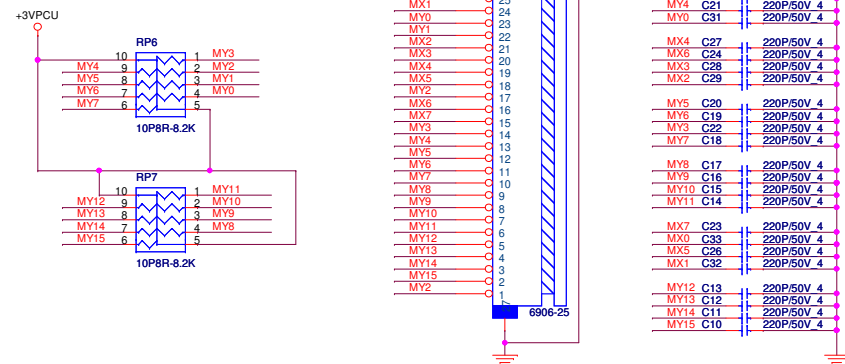
Place close to
Connector



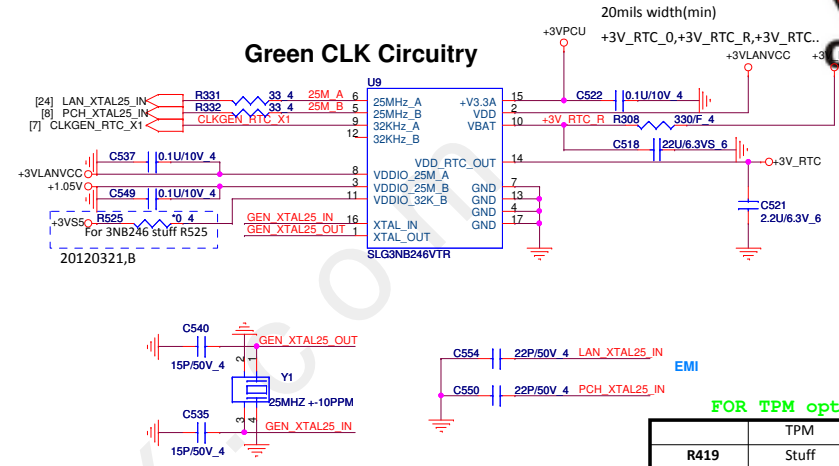
CPU Bracket



Keyboard Connector

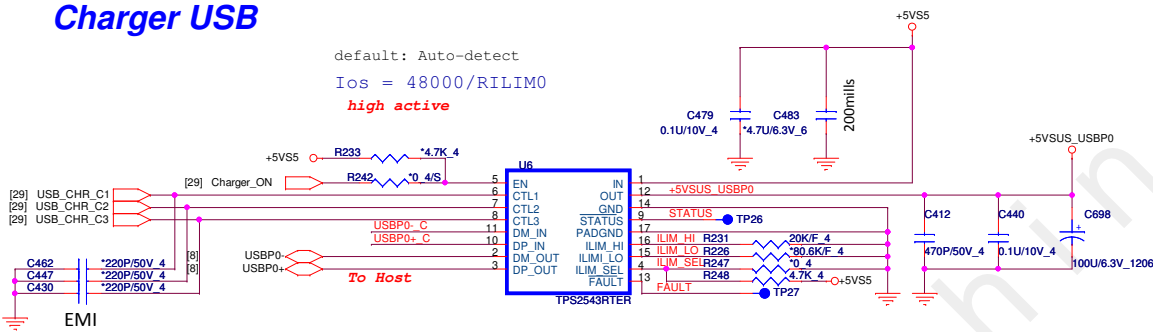


Green CLK Circuitry



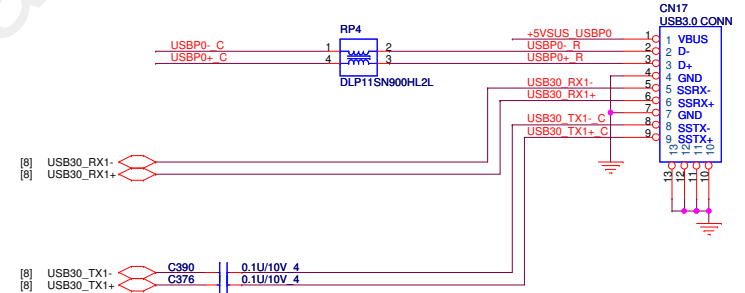
Charger USB

default: Auto-detect
Ios = 48000/RILIMO
high active



USB3.0 X 1/USB2.0 COMBO

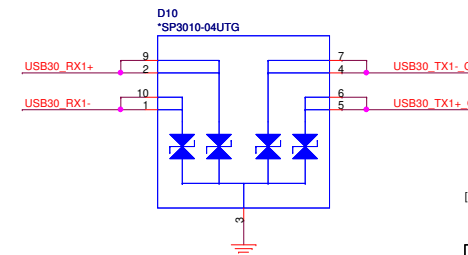
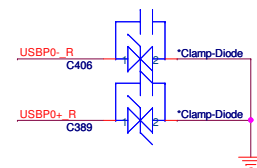
USB 3.0



TPS2543/45 Control Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	Charging Mode	Current Limit Setting	TPS2543 STATUS Output (active low)
0	0	0	1	Discharge	NA	off
0	0	1	1	DCP/auto	IOS_PW & ILIM_HI (1)	DCP load present
0	1	0	1	SDP	ILIM_HI	off
0	1	1	1	DCP/auto	ILIM_HI	DCP load present
1	1	0	1	SDP	ILIM_HI	off
1	1	1	1	CDP	ILIM_HI	CDP load present

(1) ILIM_HI: 20K(R5233), 2.4A

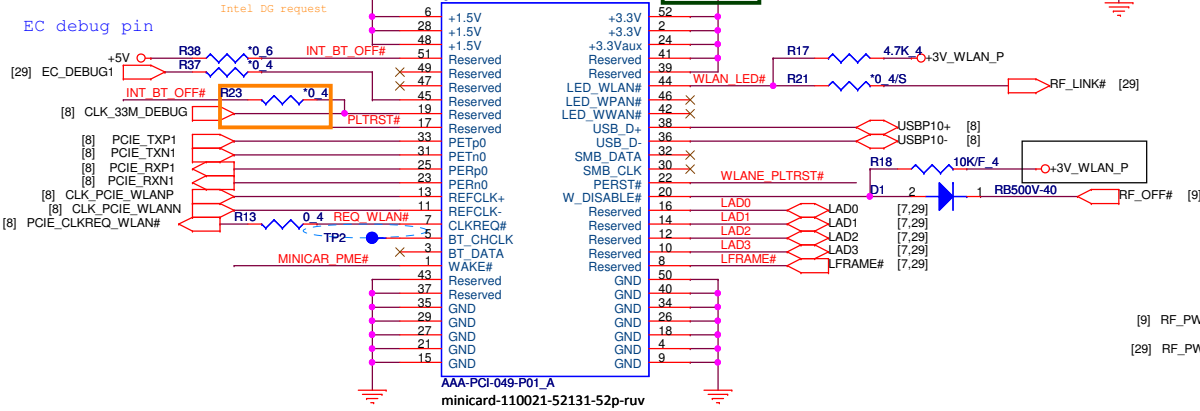


[10,21,23,32,33,34,35,37,39,40,41] +5VSS

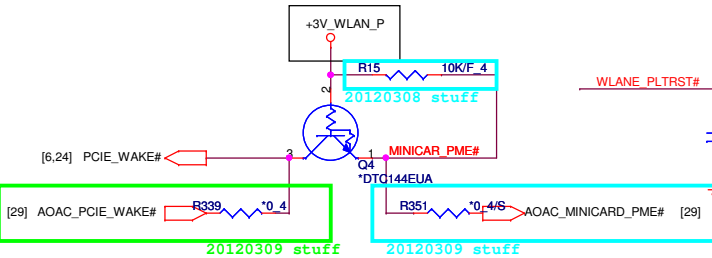
[7,21,27,28,29,31,32] +3VPCU

Mini Card WLAN/BT(Optional)

EC debug pin

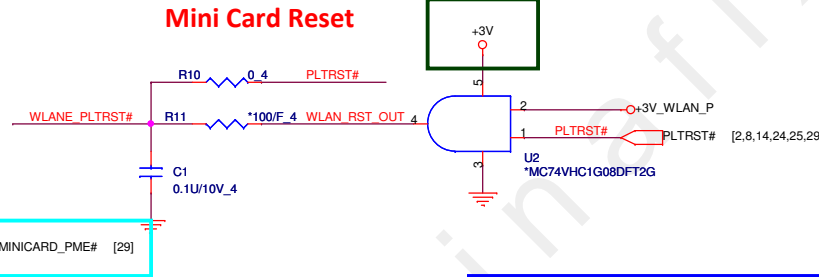


Support Wake Function(Reserve)

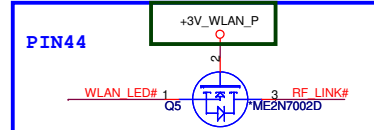


Add for AOAC

Mini Card Reset



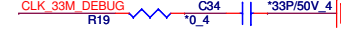
Avoid leakage issue



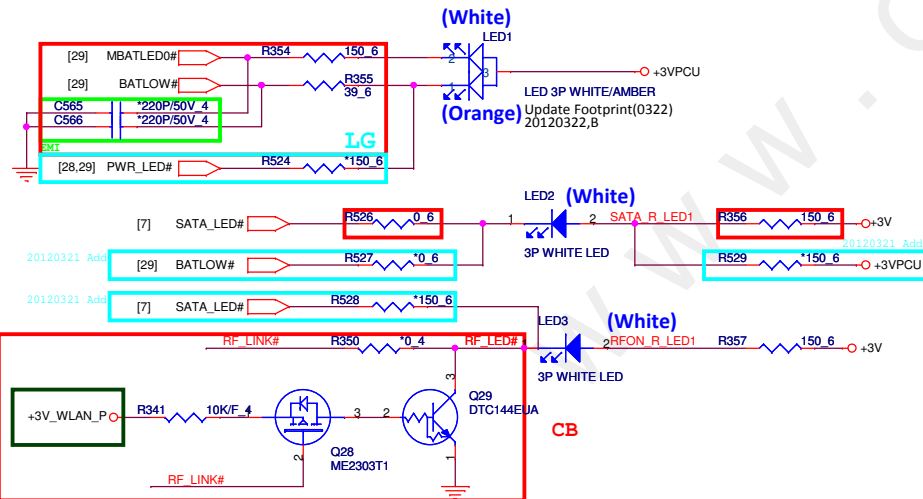
LGE mini-pcie power status

WLAN	Bluetooth	+3V_WLAN_P
Radio-ON	Radio-ON	Power-ON
Radio-ON	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF

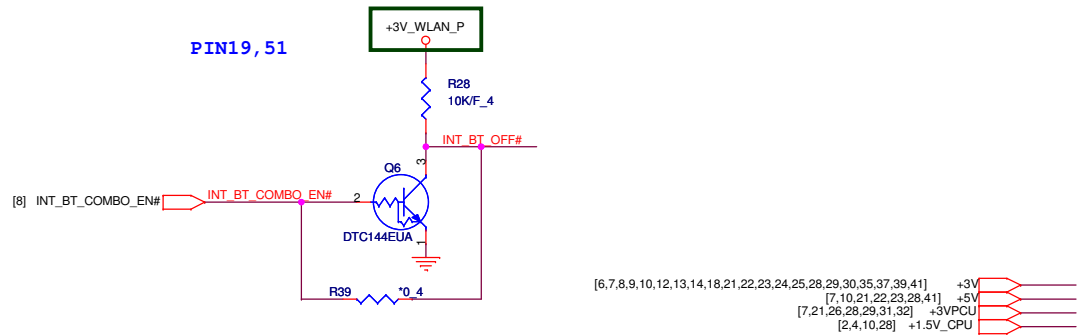
For EMI Suggestion



LED Status



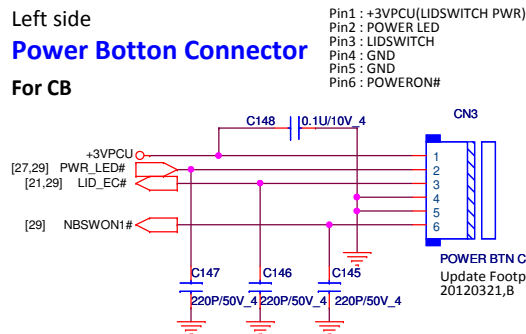
PIN19, 51



9/4 Intel COMBO card control circuit
1.add R1001,R1002,Q1001
2.add net name"INT_BT_COMBO_EN#" -> "INT_BT_OFF#"

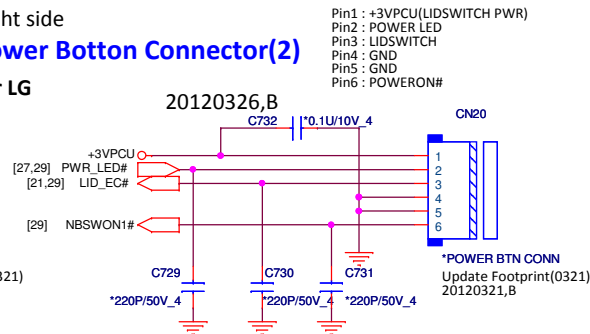
Left side Power Botton Connector

For CB

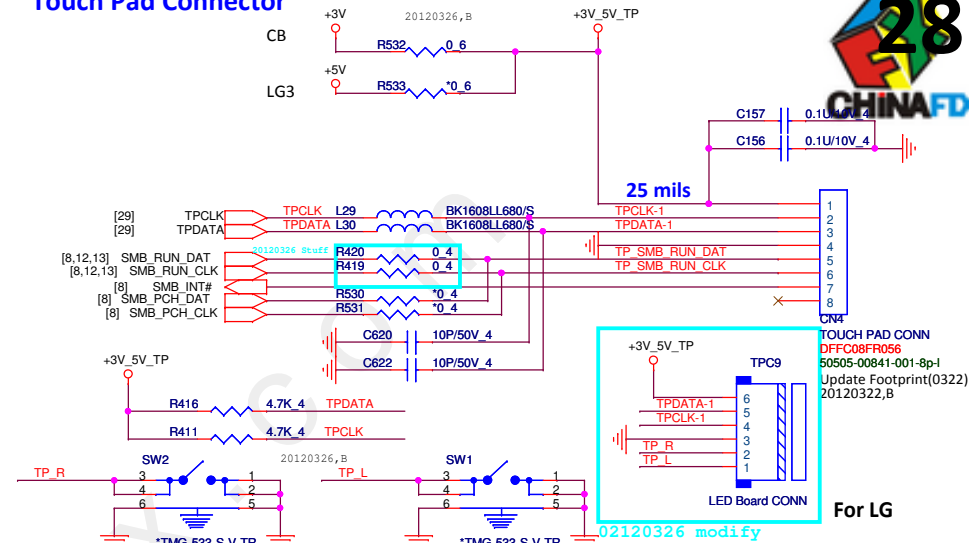


Right side Power Botton Connector(2)

For LG

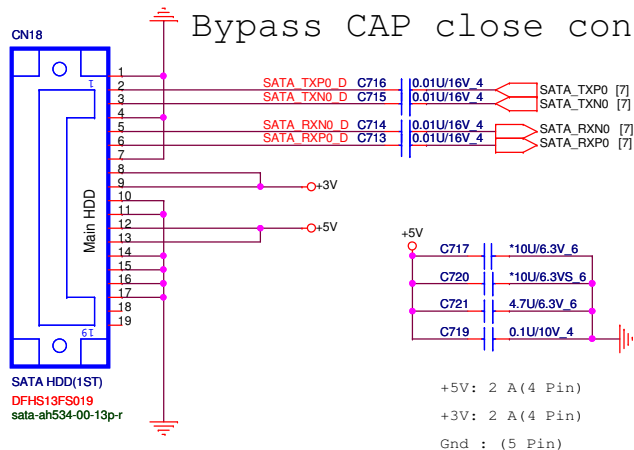


Touch Pad Connector

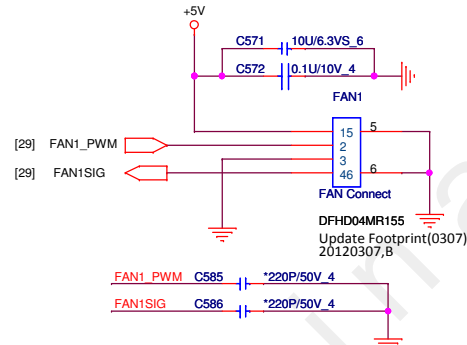


SATA HDD Connector(Cable type)

Bypass CAP close conn

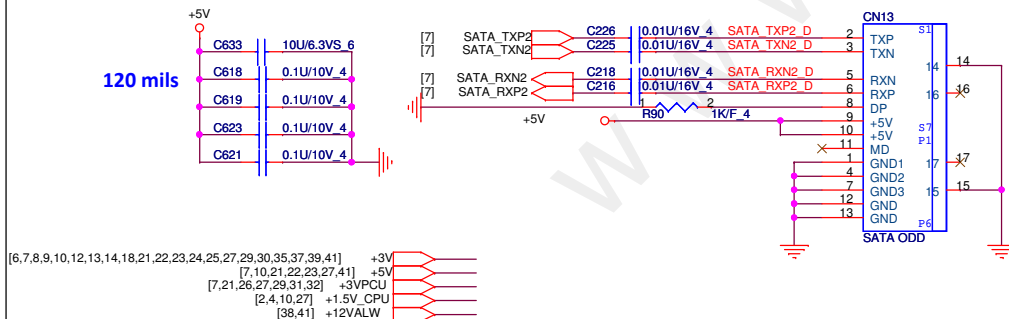


CPU FAN

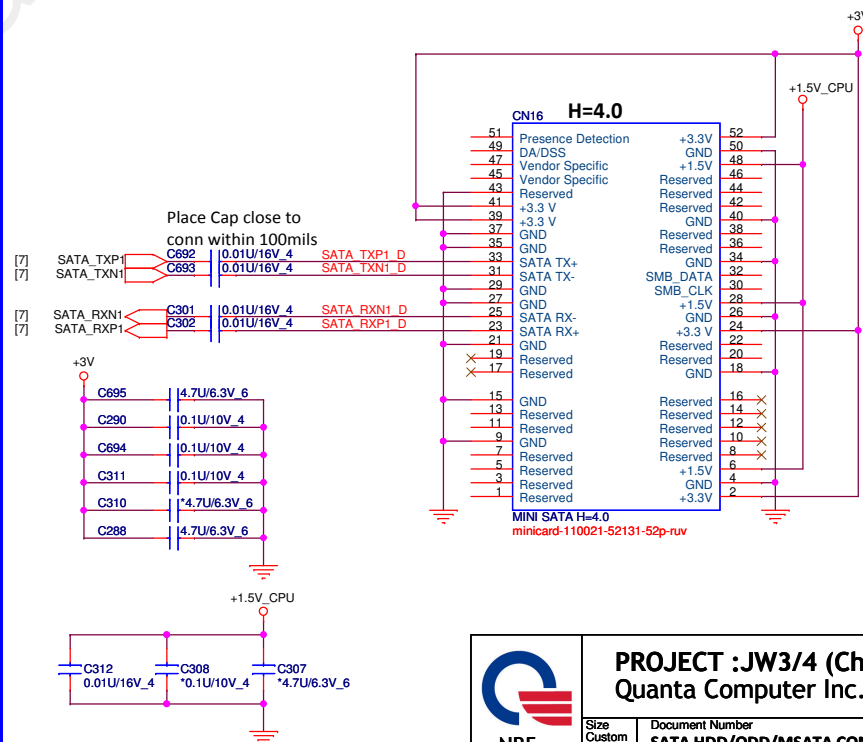


SATA ODD Connector

120 mils



Mini PCI-E Card 2- Full size MINISATA

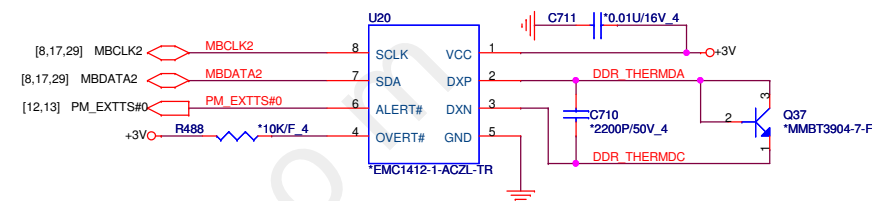


PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD/ODD/MSATA CONN	A
Date: Tuesday, March 27, 2012	Sheet	28of 42



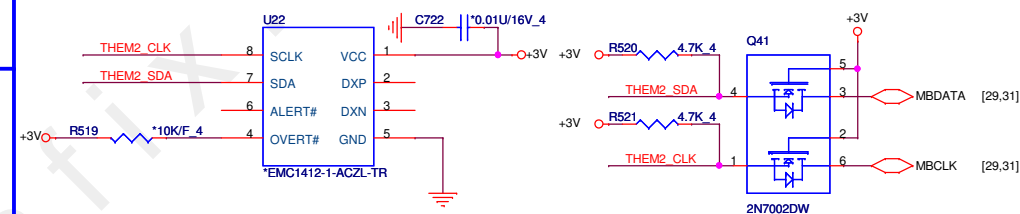
DDR3 Thermal Sensor



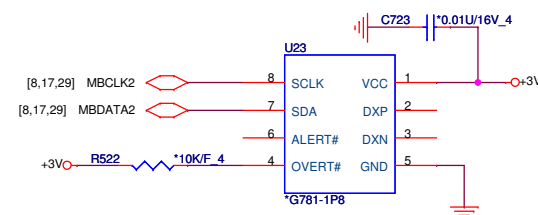
Main:AL001412003 EMC1412-1-ACZL-TR(98h)

2nd:AL000431014 TMP431ADGKR(98h)

Thermal Solution(Close to CRT)



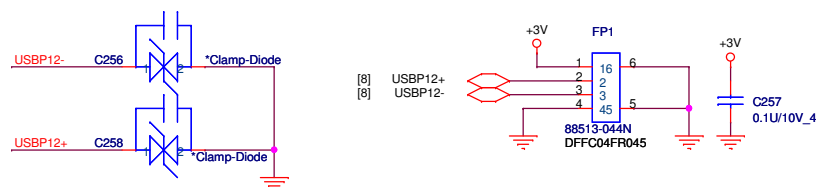
Thermal Solution(Close to GPU)



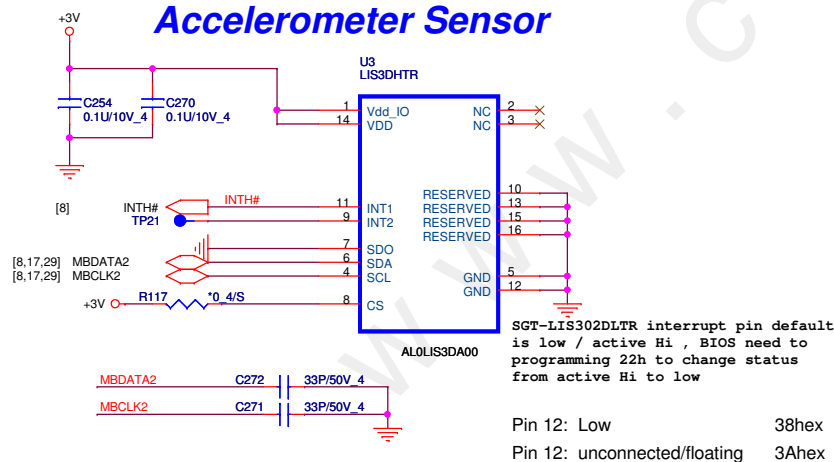
Main:AL000781039 G781-1P8(9Ah)

2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

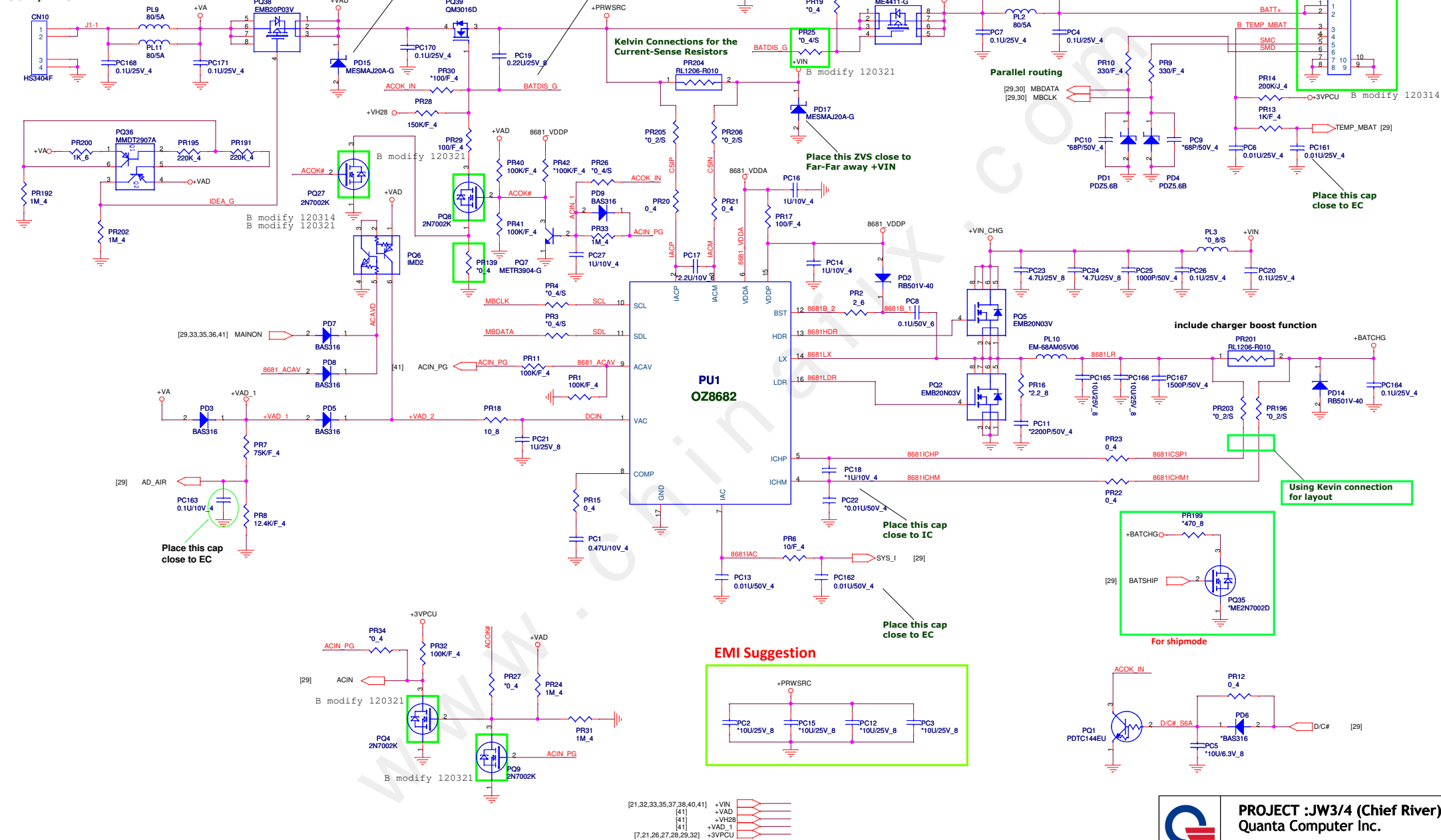
Finger Printer



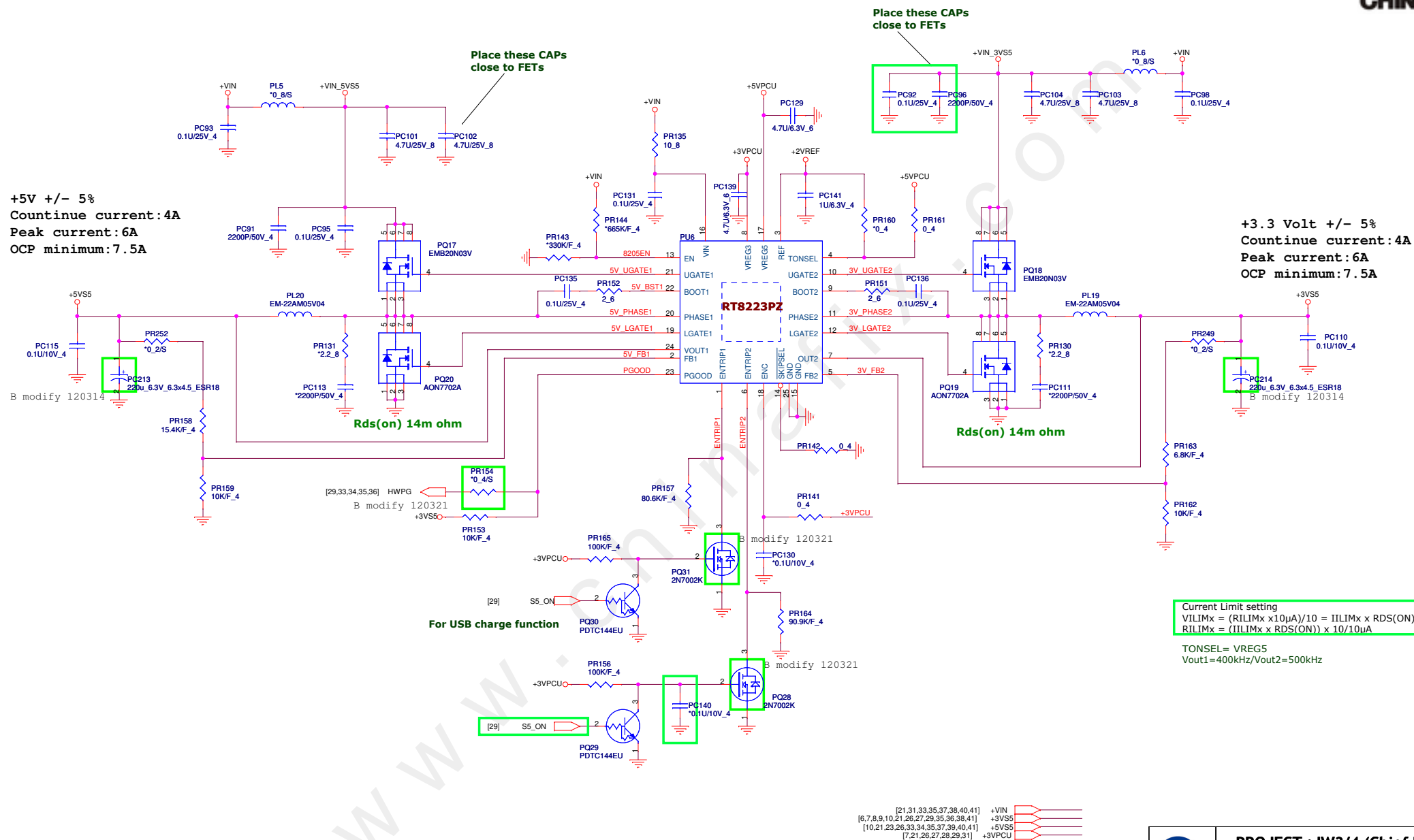
Accelerometer Sensor



TOP DC_JACK
90W/4.75A



[21,32,33,35,37,38,40,41] +VIN
[41] +VAD
[41] +VH28
[41] +VH_1
[7,21,26,27,28,29,32] +3VPCU



Current Limit setting

$$VILIMx = (RILIMx \times 10\mu A) / 10 = IILIMx \times RDS(ON)$$
$$RILIMx = (IILIMx \times RDS(ON)) \times 10 / 10\mu A$$

TONSEL= VREG5
Vout1=400kHz/Vout2=500kHz

(VTT/2A)

+0.75V_DDR_VTT

+VIN_DDR

PL25
*0.8/S

+VIN

(3mA)

[4,12,13] DDR_VTTREF

+1.5VSUS +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

RILIM = ILIM x RDS(ON) / 10uA

RDSon= 5m ohm

Place this short pad
close to output CAP

Place this FB parts close to IC

[21,31,32,35,37,38,40,41] +VIN
[10,21,23,26,32,34,35,37,39,40,41] +5VS5
[2,4,12,13,38] +1.5VSUS
[12,13,41] +0.75V_DDR_VTT



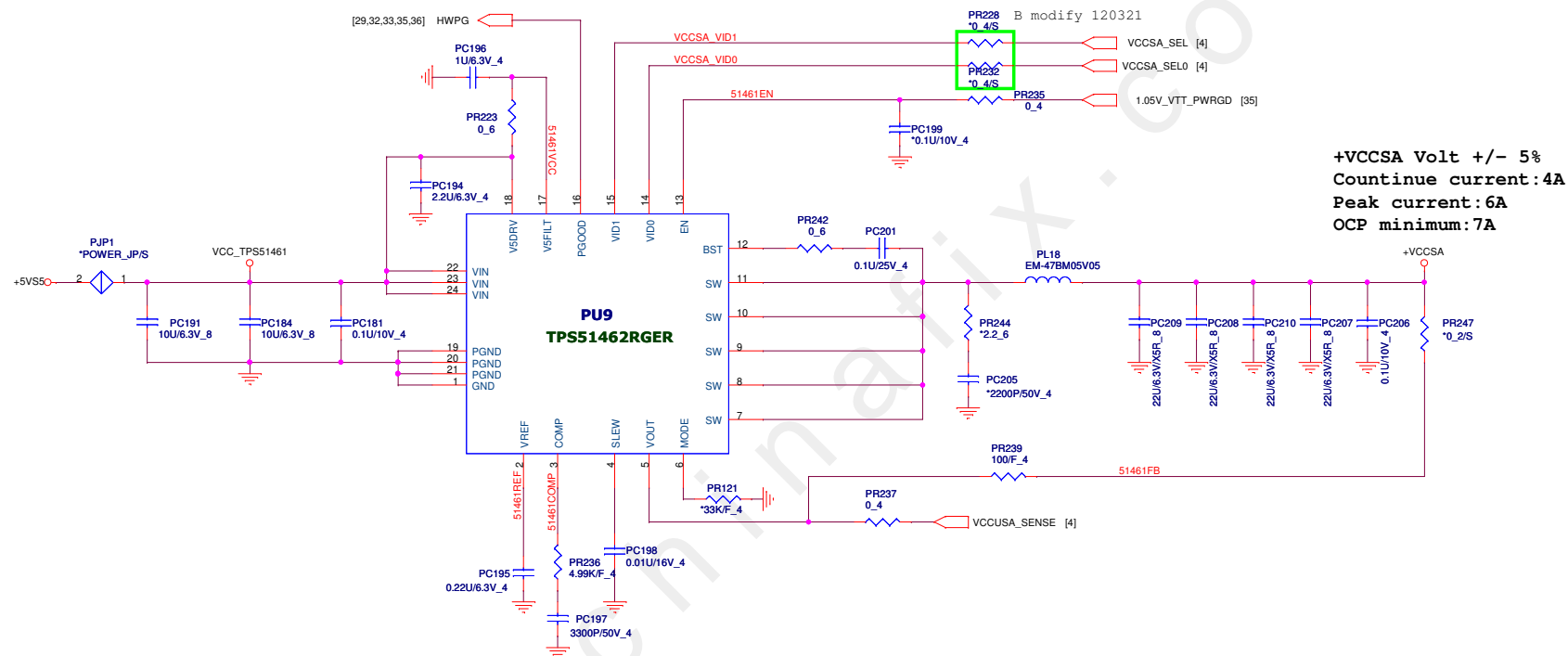
PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

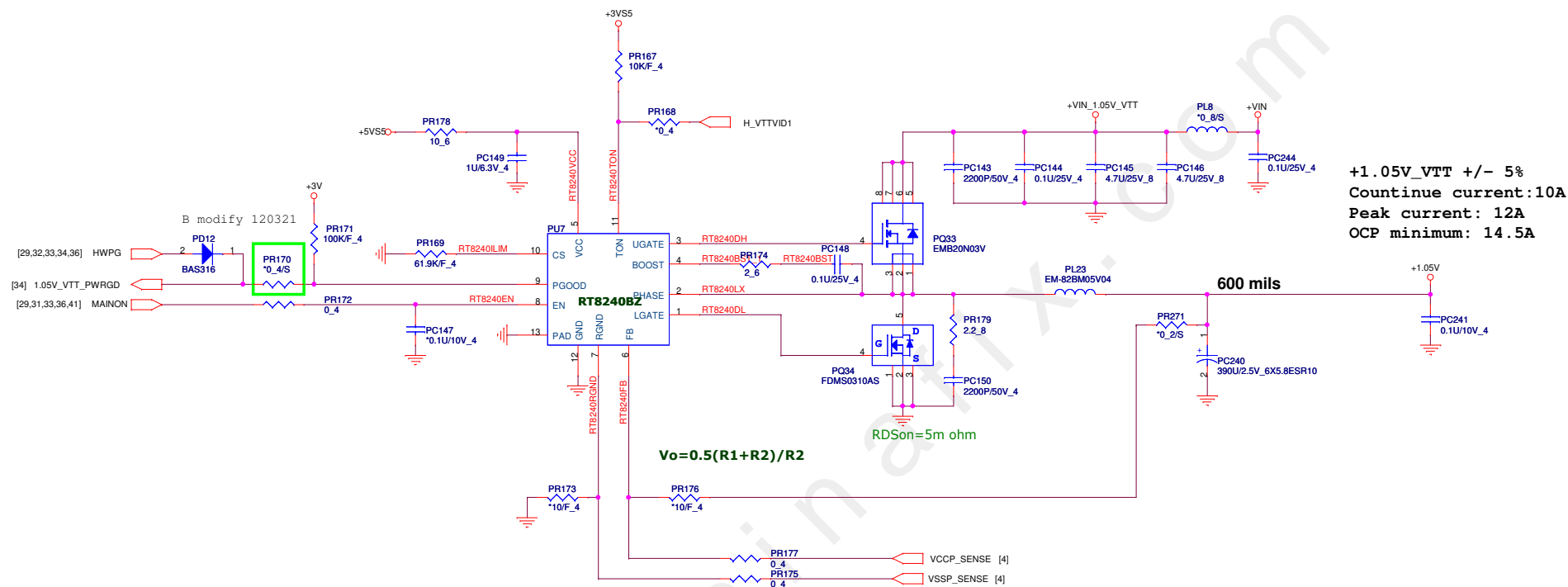
Size	Document Number	Rev
Custom	DDR3 (RT8207)	A
Date: Tuesday, March 27, 2012	Sheet 33of	42

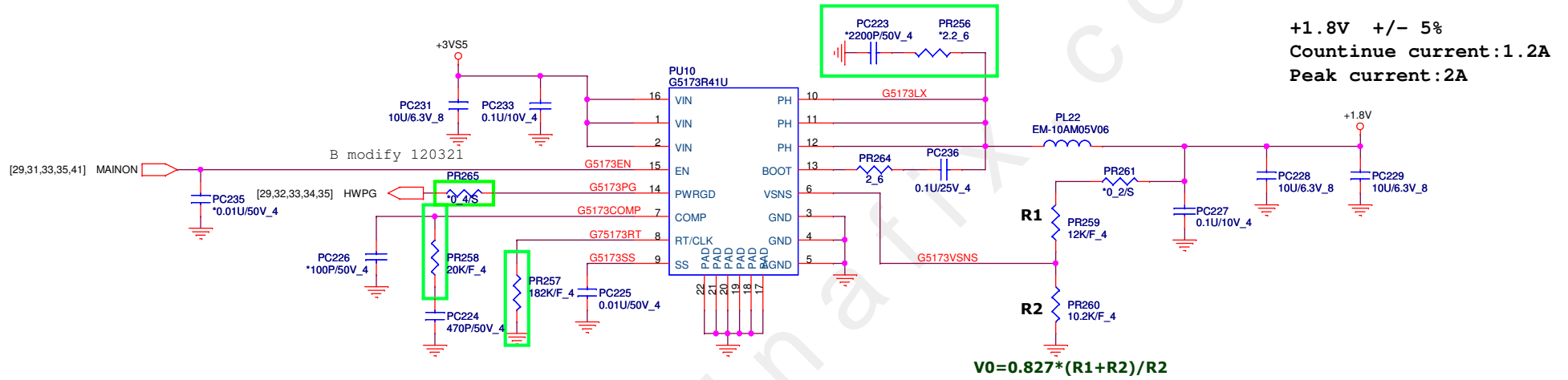
CPU system agent
voltage slew rate of 0.5 -10 mV/ μ s

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

TPS51462RGER for SV CPU

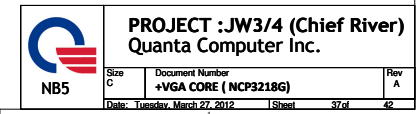






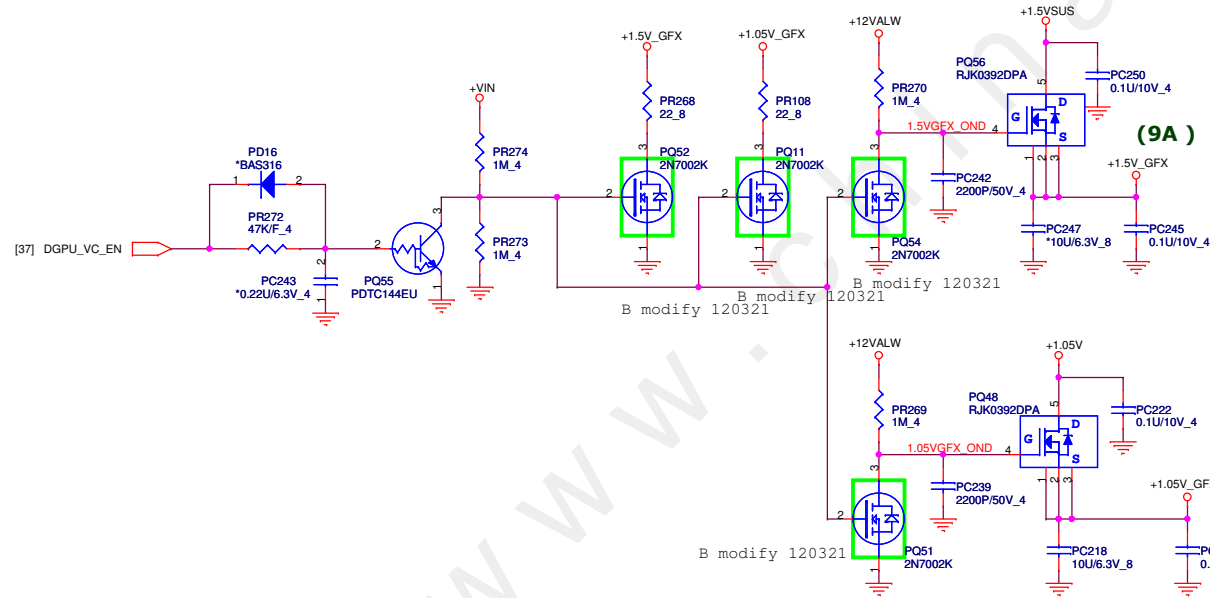
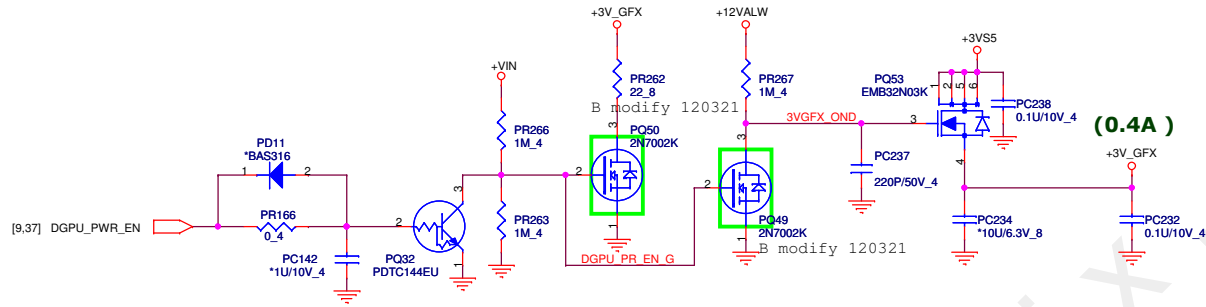
PROJECT :JW3/4 (Chief River)
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Size B	Document Number +1.8V (G9661)	Rev A
Date: Tuesday, March 27, 2012	Sheet	36of 42



VGA

[2,4,12,13,33] +1.5VSUS
[7,8,9,10,21,26,27,29,32,35,36,41] +3VSS
[14,16,17,18,37] +3V_GFX
[15,18,19,20] +1.5V_GFX
[14,15,16,18] +1.05V_GFX
[41] +12VALW
[2,4,6,7,8,10,26,29,35,39] +1.05V

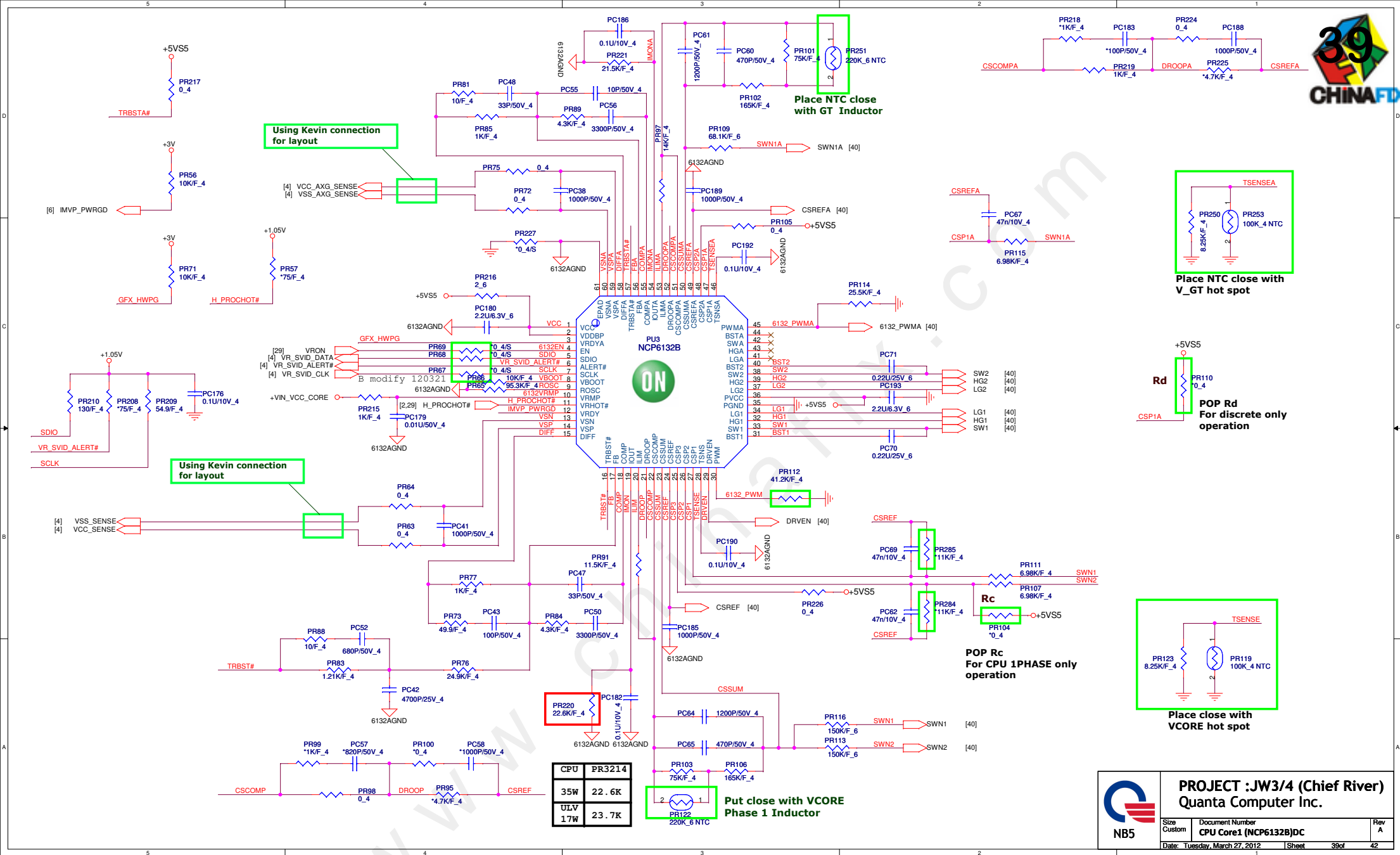


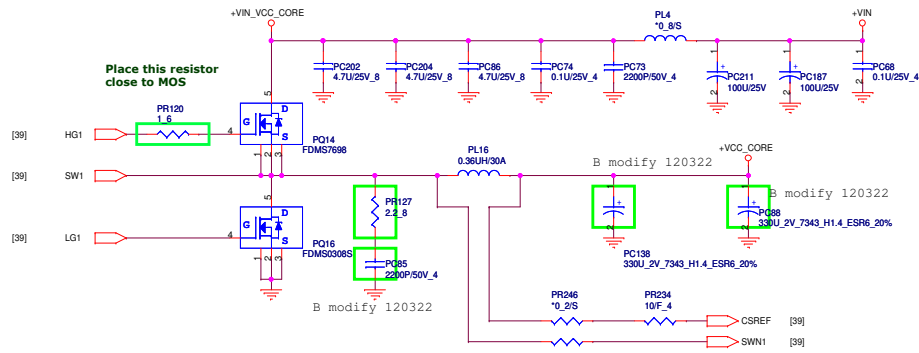
+1.05V +/- 3%
Countinue current:2.1A
Peak current:3A



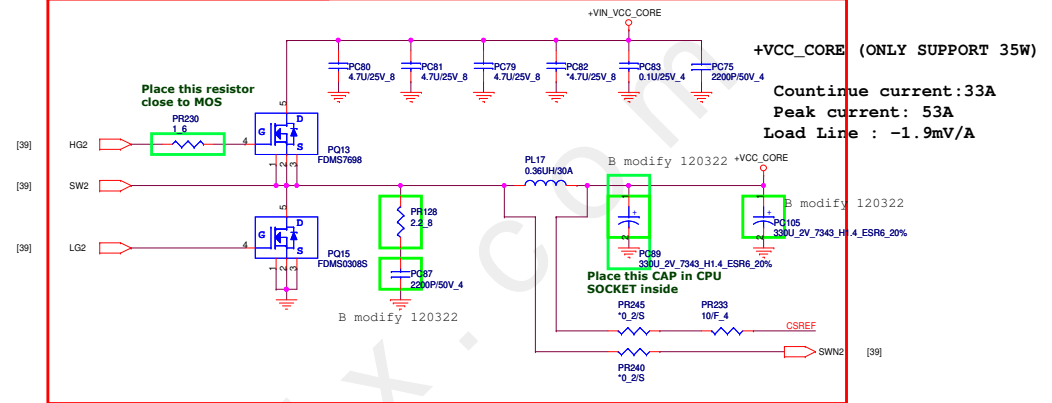
PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size Custom	Document Number +VGA POWER	Rev A
Date: Tuesday, March 27, 2012	Sheet 38 of 42	





Dummy This Schematic
For CPU 1-Phase operation

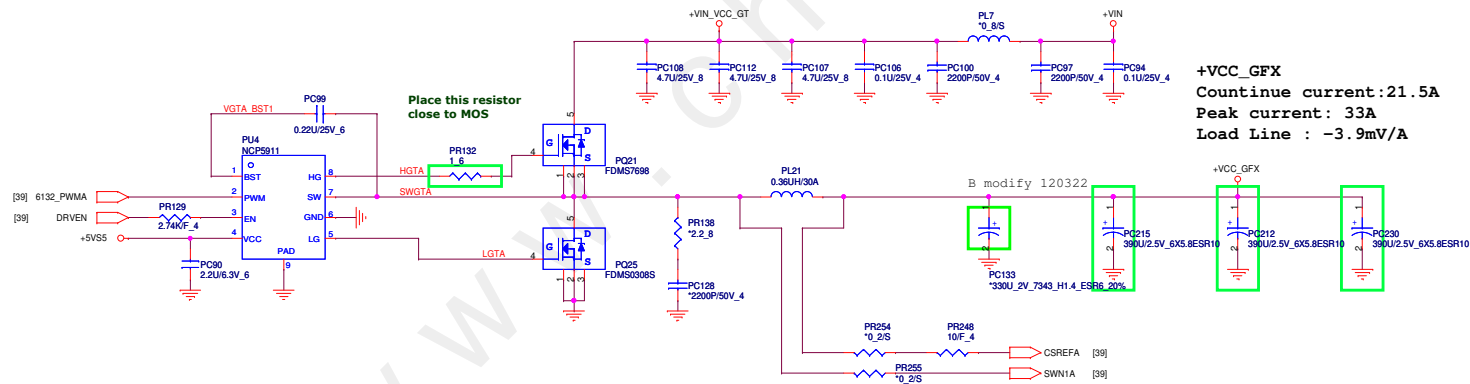


+VCC_CORE (ONLY SUPPORT 35W)

Countinue current:33A
Peak current: 53A
Load Line : -1.9mV/A

+VCC_CORE (ULV 17W)

TDC : 25A
Peak current: 33A
Load Line : -2.9mV/A



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