JE40 HR
DIS/UMA/Muxless Schematics Document
Sandy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

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JE40 HR Block Diagram (Discrete/UMA/co-lay)

Project code : 91.4IQ01.001
PCB P/N : 48.4IQ01.0SA
Revision : 10267-1

##OnMainBoard

VRAM
2GB/1GB/512MB
88,89,90,91

DDR3
800MHz

Nvidia N12P
83,84,85,86,87

PCIe x 16
(Discrete only)

Intel CPU
Sandy Bridge
FSB: 1066 MHz
4,5,6,7,8,9,10,11,12,13

DDRIII 1066/1333 Channel A
DDRIII 1066/1333 Channel B

DDRIII Slot 0 1066/1333 14
DDRIII Slot 1 1066/1333 15

Discreet/UMA/PX Co-lay

FDIx4x2
(UMA only)

DMIx4

HDMI 51
LCD 49
HDMI
LVDS(Dual Channel)
RGB CRT
Level shifter 57
CRT 50

Intel
PCH
Cougar Point

14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1

17,18,19,20,21,22,23,24,25,26

PCIE x 1
USB x 2
USB3.0
uPD720200
75

PCIE x 1
USB x 1
Mini-Card
802.11a/b/g
65

PCIE x 1
1000 NIC
BCM57780A1
31

RJ45 CONN 59

SD/MMC+/MS/
MS Pro/xD

PCIE x 1,USB x 1
Mini-Card
WWAN 66

SIM 66

USB 2.0 x 1
Right Side:
USB x 1

Left Side:
USB x 1

Bluetooth 63

CAMERA 49

64

USB2.0 x 4

AZALIA

Azalia
CODEC
ALC271X
29

Internal Analog MIC
HP1
MIC IN
2CH SPEAKER

SPI

Flash ROM
4MB 60

LPC Bus

LPC debug port 71

SATA x 2

HDD 56

ODD 56

KBC
NUVOTON
NPCE795P 27

SMBus

Touch PAD 69

Int. KB 69

Thermal
ENE P2800
ENE P2793 28

Fan 28

SYSTEM DC/DC APL5916KAI 48	
INPUTS	OUTPUTS
1D05V_PWR	0D85V_S0

CPU DC/DC NCP6131S52MNR 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6128PQDD 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183PQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6165BQKF 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC NCP5911MNTBG 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208BGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC RT9025-25PSP 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0
3D3V_S5	1D8V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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SSID = CPU

CPU1A
SANDY
62.10055.421
Change:62.10053.611
2nd = 62.10055.321
3rd = 62.10040.821

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

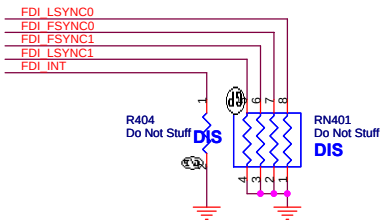
PEG Static Lane Reversal

JE40 delete eDP function

20100614 V1.1

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

Stuff to disable internal graphics function for power saving.



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Title: CPU (PCIE/DMI/FDI)

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SSID = CPU

CPU1B
SANDY

2 OF 9

SANDY

MISC
- 18 H_SNB_IVB# — C26 — SNB_IVB#
- JE40 modify — AN34 — SKTOCC#

THERMAL
- JE40 modify — AL33 — CATERR#
- 22,27 H_PECI — AN33 — PECI
- 27,42 H_PROCHOT# — R513 56R2J-4-GP — H_PROCHOT# R — AL32 — PROCHOT#
- 22,36 H_THERMTRIP# — AN32 — THERMTRIP#

PWR MANAGEMENT
- 19 H_PM_SYNC — AM34 — PM_SYNC
- 22,36,97 H_CPUPWRGD — R503 10KR2J-3-GP — AP33 — UNCOREPWRGOOD
- 19,37 PM_DRAM_PWRGD — R505 DX Do Not Stuff — V8 — SM_DRAMPWROK
- 37 VDDPWRGOOD
- BUF_CPU_RST# — AR33 — RESET#

CLOCKS
- BCLK — A28 — CLK_EXP_P — 20
- BCLK# — A27 — CLK_EXP_N — 20
- DPLL_REF_SSCLK — A16 — CLK_DP_P_R — RN502 Do Not Stuff DIS — JE40 modify — 1D05V_VTT
- DPLL_REF_SSCLK# — A15 — CLK_DP_N_R

DDR3 MISC
- SM_DRAMRST# — R8 — R502 4K99R2F-L-GP — SM_DRAMRST# 37
- SM_RCOMP0 — AK1 — SM_RCOMP_0 R506 140R2F-GP
- SM_RCOMP1 — A5 — SM_RCOMP_1 R507 25D5R2F-GP
- SM_RCOMP2 — A4 — SM_RCOMP_2 R508 200R2F-L-GP

JTAG & BPM
- PRDY# — AP29
- PREQ# — AP27
- JE40 modify
- TCK — AR26
- TMS — AR27
- TRST# — AP30 — XDP_TRST#
- TDI — AR28
- TDO — AP26 — XDP_TDO
- DBR# — AL35 — XDP_DBRESET#
- BPM#0 — AT28
- BPM#1 — AR29
- BPM#2 — AR30
- BPM#3 — AT30
- BPM#4 — AP32
- BPM#5 — AR31
- BPM#6 — AT31
- BPM#7 — AR32
- JE40 modify

1D05V_VTT
- R501 62R2J-GP — H_PROCHOT#
- C502 SC47P50V2JN-3GP

CRB : 47pf
CEKLT:43pf

Connect EC to PROCHOT# through inverting OD buffer.

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

1D05V_VTT
- RN501 SRN51J-GP — XDP_TDO — XDP_TRST#

3D3V_S0
- RN503 SRN1K5J-1-GP — XDP_DBRESET# — 18,27,31,36,65,66,71,82,97 PLT_RST# — BUF_CPU_RST#

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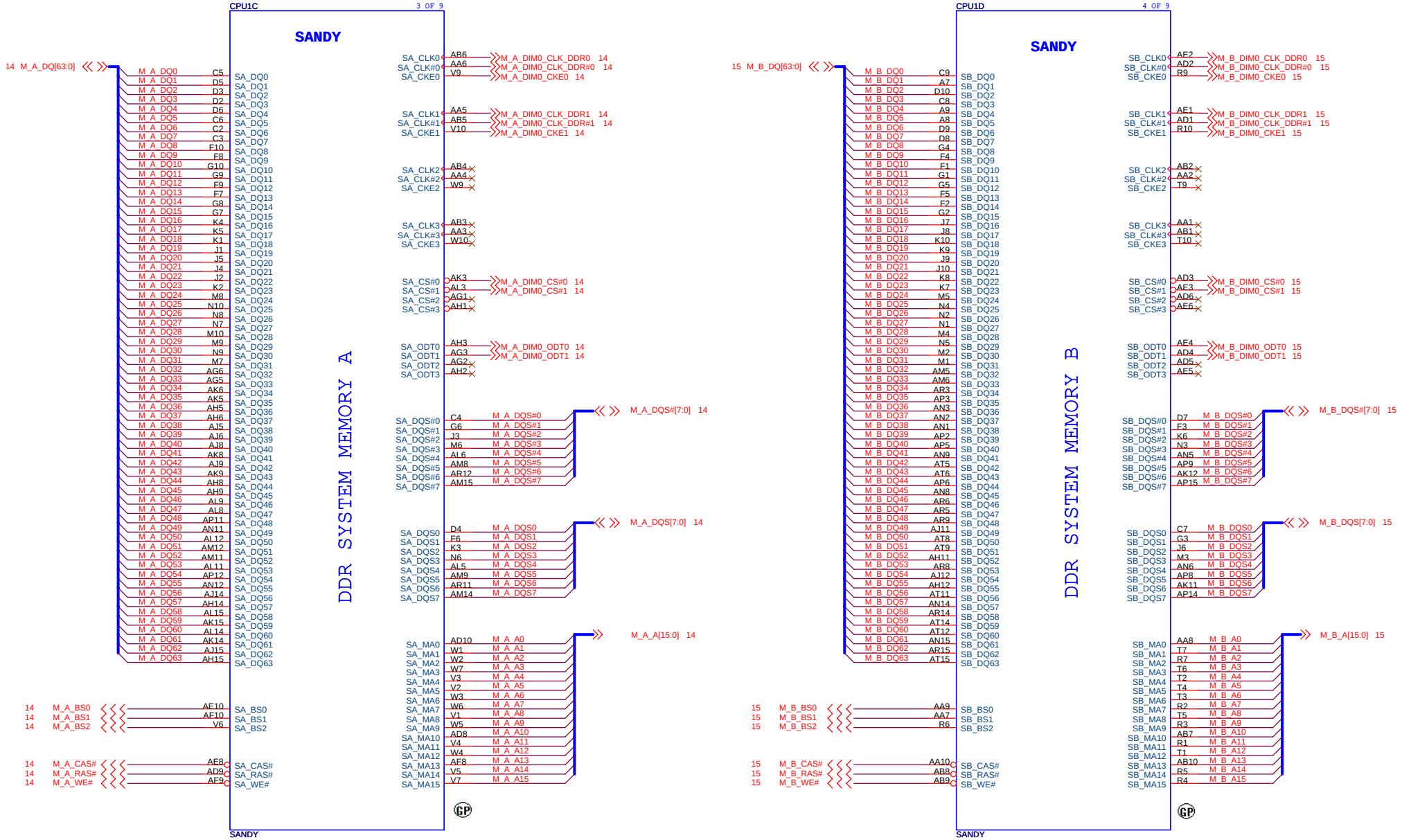
SSID = CPU



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Title: CPU (DDR)

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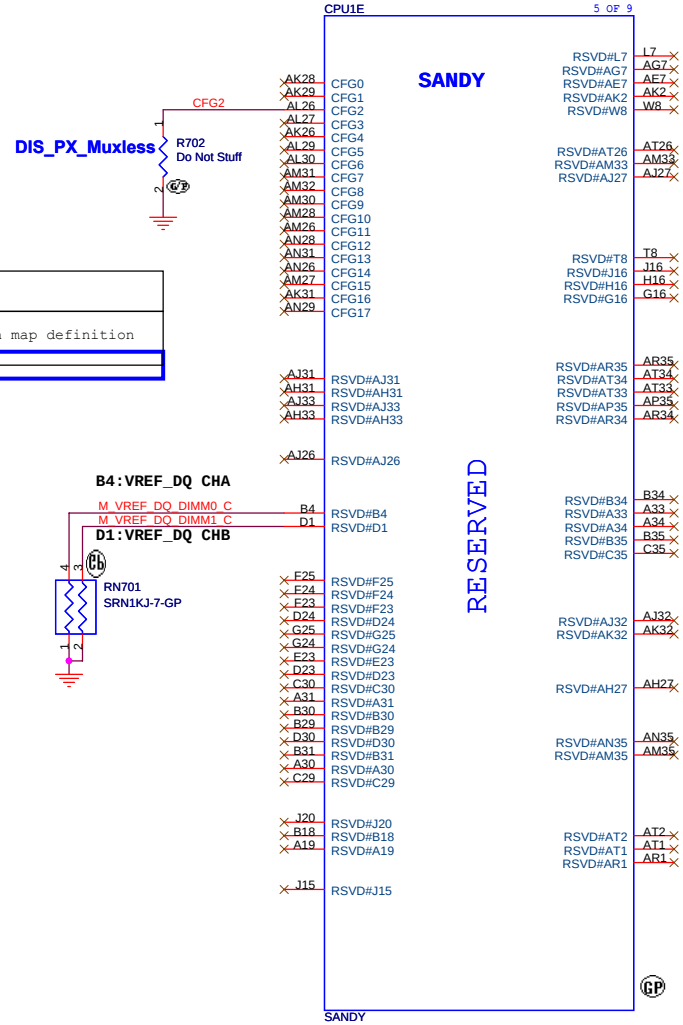
SSID = CPU



PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed

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Title: *CPU (RESERVED)*		
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SSID = CPU

PROCESSOR CORE POWER

53A

VCC_CORE

C801 Do Not Stuff, C802 Do Not Stuff, C803 Do Not Stuff, C804 Do Not Stuff, C811 Do Not Stuff

C820 Do Not Stuff, C819 Do Not Stuff, C818 Do Not Stuff, C817 Do Not Stuff, C815 Do Not Stuff

C816 SC10U6D3V5KX-1GP, C821 Do Not Stuff, C822 SC10U6D3V5KX-1GP, C823 SC10U6D3V5KX-1GP, C824 SC10U6D3V5KX-1GP, C825 SC10U6D3V5KX-1GP, C826 SC10U6D3V5KX-1GP, C827 SC10U6D3V5KX-1GP

C837 SC10U6D3V5KX-1GP, C836 SC10U6D3V5KX-1GP, C835 SC10U6D3V5KX-1GP, C834 SC10U6D3V5KX-1GP, C833 SC10U6D3V5KX-1GP, C832 Do Not Stuff, C831 Do Not Stuff, C828 SC10U6D3V5KX-1GP

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

POWER

CPU1F — 6 OF 9 — SANDY

CORE SUPPLY | PEG AND DDR | SVID | SENSE LINES

VCC_CORE

VCC: AG35, AG34, AG33, AG32, AG31, AG30, AG29, AG28, AG27, AG26, AE35, AE34, AE33, AE32, AE31, AE30, AE29, AE28, AE27, AE26, AD35, AD34, AD33, AD32, AD31, AD30, AD29, AD28, AD27, AD26, AC35, AC34, AC33, AC32, AC31, AC30, AC29, AC28, AC27, AC26, AA35, AA34, AA33, AA32, AA31, AA30, AA29, AA28, AA27, AA26, Y35, Y34, Y33, Y32, Y31, Y30, Y29, Y28, Y27, Y26, V35, V34, V33, V32, V31, V30, V29, V28, V27, V26, U35, U34, U33, U32, U31, U30, U29, U28, U27, U26, R35, R34, R33, R32, R31, R30, R29, R28, R27, R26, P35, P34, P33, P32, P31, P30, P29, P28, P27, P26

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

1D05V_VTT

VCCIO: AH13, AH10, AG10, AC10, Y10, U10, P10, L10, J14, J13, J12, J11, H14, H12, H11, G14, G13, G12, F14, F13, F12, F11, E14, E12

C805 SC10U6D3V5KX-1GP, C806 SC10U6D3V5KX-1GP, C807 SC10U6D3V5KX-1GP, C809 SC10U6D3V5KX-1GP, C810 SC10U6D3V5KX-1GP, C838 SC10U6D3V5KX-1GP, C839 SC10U6D3V5KX-1GP, C840 SC10U6D3V5KX-1GP, C841 SC10U6D3V5KX-1GP

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

1D05V_VTT

VCCIO: F11, E11, D14, D13, D12, D11, C14, C13, C12, C11, B14, B12, A14, A13, A12, A11, J23

C812 SC10U6D3V5KX-1GP, C813 SC10U6D3V5KX-1GP, C814 SC10U6D3V5KX-1GP, C829 SC10U6D3V5KX-1GP, C830 SC10U6D3V5KX-1GP, C842 Do Not Stuff, C843 Do Not Stuff, C844 SC10U6D3V5KX-1GP, C845 SC10U6D3V5KX-1GP

VIDALERT# AJ29 — H_CPU_SVIDALRT# — R803 43R2J-GP — VR_SVID_ALERT# 42
VIDSCLK AJ30 — H_CPU_SVIDCLK 42
VIDSOUT A28 — H_CPU_SVIDDAT 42

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

1D05V_VTT

H_CPU_SVIDDAT — R804 130R2F-1-GP

VCC_CORE

R801,R802 close to CPU

R801 100R2F-L1-GP-U

VCC_SENSE AJ35 — VCCSENSE 42
VSS_SENSE AJ34 — VSSSENSE 42

R802 100R2F-L1-GP-U

VCCIO_SENSE B10 — VCCIO_SENSE 45
VSSIO_SENSE A10 — VSSIO_SENSE 45

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SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

R906,R907 close to CPU

POWER

CPU1G — 7 OF 9 — SANDY

GRAPHICS | DDR3 -1.5V RAILS | SA RAIL | 1.8V RAIL | MISC | VREF | SENSE LINES

VCC_GFXCORE

PROCESSOR VAXG: 24A

C901 Do Not Stuff (DY) — C902 SC10U6D3V5KX-1GP — C903 SC10U6D3V5KX-1GP — C904 SC10U6D3V5KX-1GP — C905 SC10U6D3V5KX-1GP — C906 Do Not Stuff (DY)

C907 Do Not Stuff (DY) — C908 SC10U6D3V5KX-1GP — C918 Do Not Stuff (DY) — C919 SC10U6D3V5KX-1GP — C920 SC10U6D3V5KX-1GP — C921 SC10U6D3V5KX-1GP

UMA_PX_Muxless

AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17 — VAXG

VAXG_SENSE — AK35
VSSAXG_SENSE — AK34

VCC_AXG_SENSE 42
VSS_AXG_SENSE 42

VCC_AXG_SENSE
VSS_AXG_SENSE

R906 100R2F-L1-GP-U
R907 100R2F-L1-GP-U

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

SM_VREF — AL1 — +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

1D5V_S0

PROCESSOR VDDQ: 10A

VDDQ — AF7 AF4 AF1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1

C909 Do Not Stuff (DY) — C910 SC10U6D3V5KX-1GP — C911 SC10U6D3V5KX-1GP — C912 SC10U6D3V5KX-1GP — C913 SC10U6D3V5KX-1GP — C914 Do Not Stuff (DY)

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

0D85V_S0

PROCESSOR VCCSA: 6A

C916 Do Not Stuff (DY) — C915 SC10U6D3V5KX-1GP

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

VCCSA — M27 M26 L26 J26 J25 J24 H26 H25

0D85V_S0

R902 need be close to pin H23.

R902 10R2J-2-GP

VCCSA_SENSE — H23 — VCCUSA_SENSE — TP901 Do Not Stuff

FC_C22 — C22 — H_FC_C22
VCCSA_VID1 — C24 — VCCSA_SEL 48

RN901 SRN1KJ-7-GP

VCC_GFXCORE

R903 Do Not Stuff DIS — R904 Do Not Stuff DIS — R905 Do Not Stuff DIS — R901 Do Not Stuff DIS

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

1D8V_S0

PROCESSOR VCCPLL: 1.2A

C922 SC1U10V2KX-1GP

VCCPLL — B6 A6 A2

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

HR UMA

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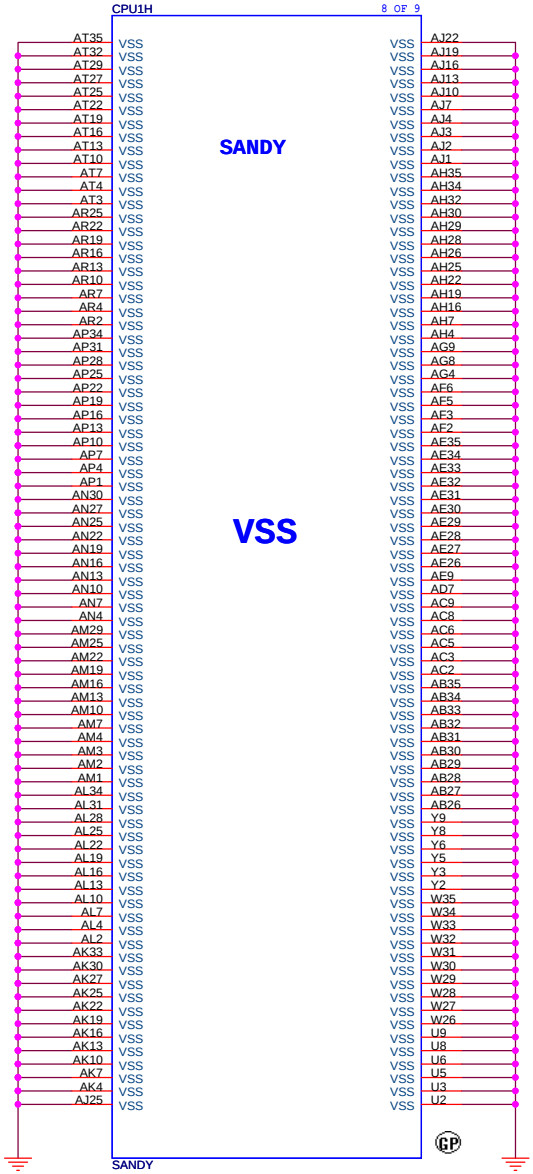
Taipei Hsien 221, Taiwan, R.O.C.

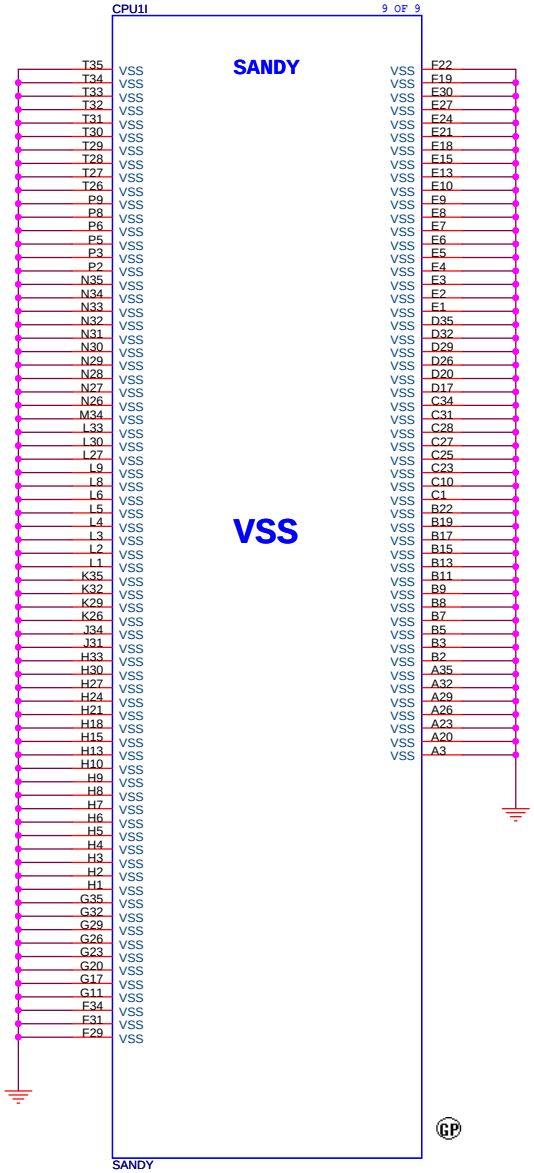
Title: *CPU (VCC_GFXCORE)*

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 — Sheet 9 of 102

SSID = CPU





HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *CPU (VSS)*		
Size: A3	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 10 of 102	

JE40 delete XDP function

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *XDP*		
Size: A3	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 11 of 102	

(Blanking)

HR UMA

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Reserved***		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 12 of 102	

(Blanking)

HR UMA

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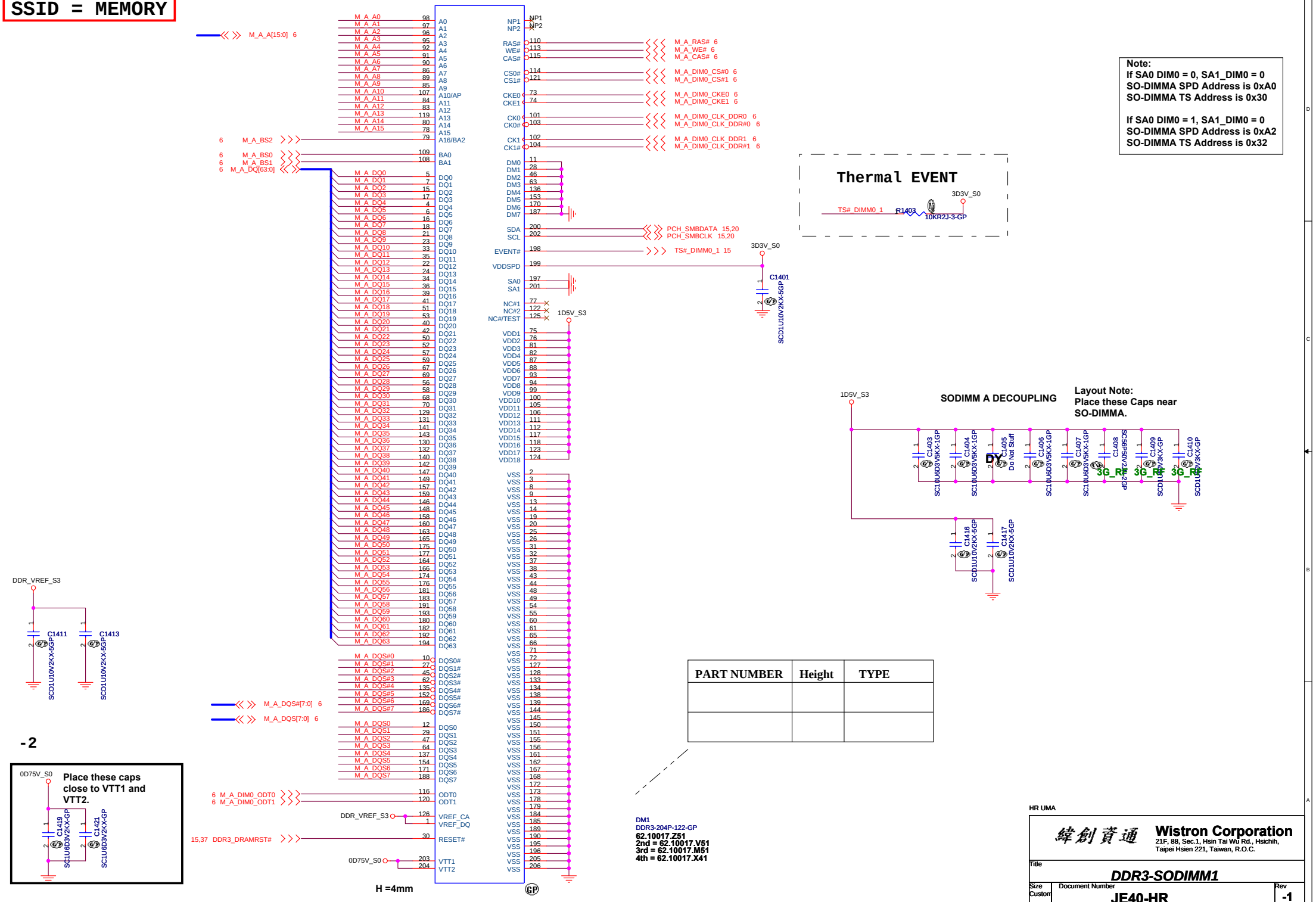
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 13 of 102

SSID = MEMORY



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

SODIMM A DECOUPLING

Layout Note:
Place these Caps near SO-DIMMA.

-2

PART NUMBER	Height	TYPE

DM1
DDR3-204P-122-GP
62.10017.Z51
2nd = 62.10017.V51
3rd = 62.10017.M51
4th = 62.10017.X41

HR UMA

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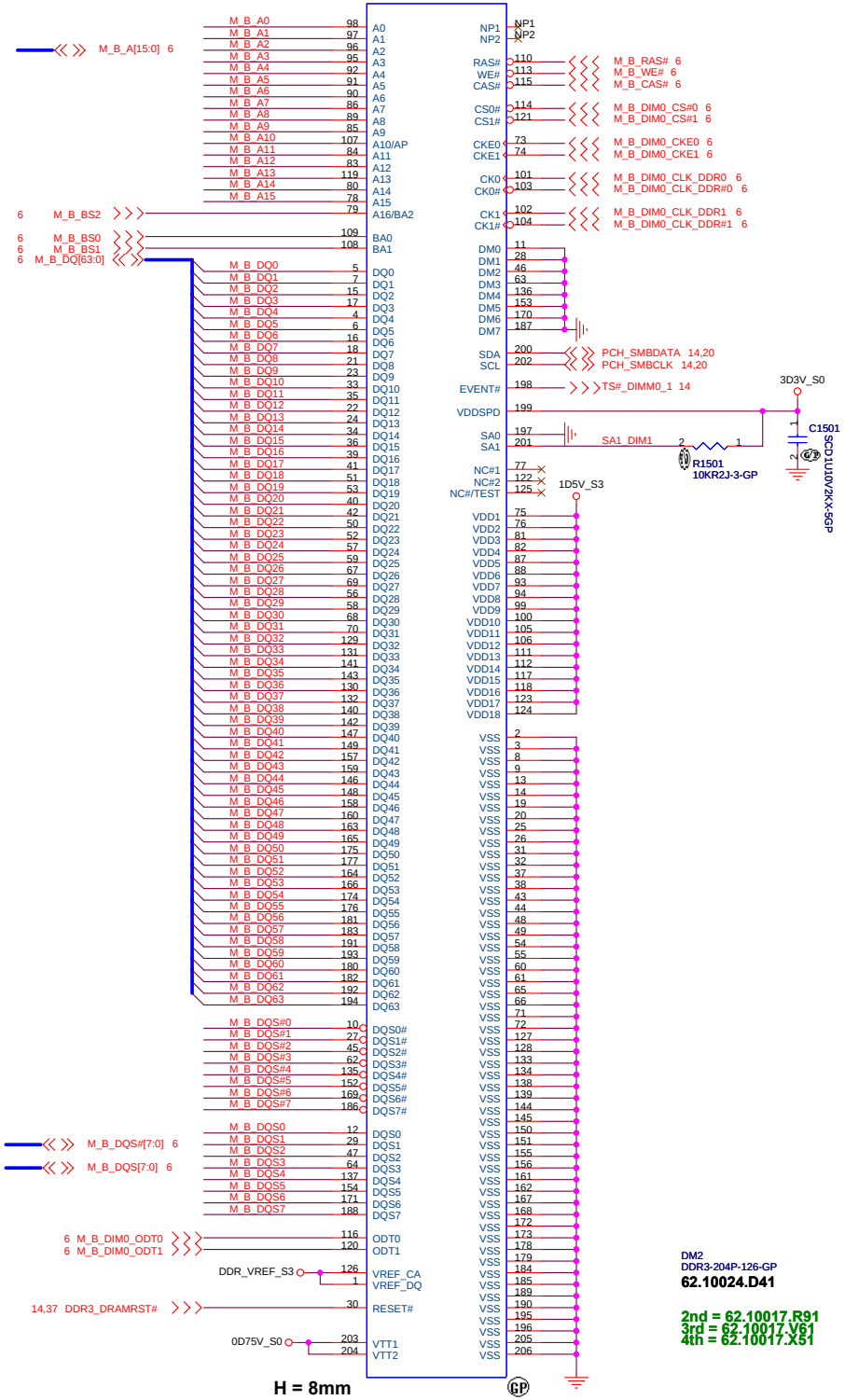
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 14 of 102

SSID = MEMORY



DDR_VREF_S3

C1515 SCD1U10V2KX-5GP

C1517 SCD1U10V2KX-5GP

-2

Place these caps close to VTT1 and VTT2.

0D75V_S0

C1519 SC1U6D3V2KX-GP

C1521 SC1U6D3V2KX-GP

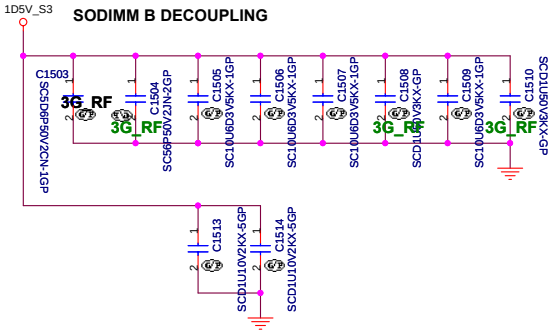
H = 8mm

DM2
DDR3-204P-126-GP
62.10024.D41

2nd = 62.10017.R91
3rd = 62.10017.V61
4th = 62.10017.X51

Layout Note:
Place these Caps near SO-DIMMB.

SODIMM B DECOUPLING



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

HR UMA

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Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
Custom	**JE40-HR**	-1

Date: Thursday, December 02, 2010 Sheet 15 of 102

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HR UMA

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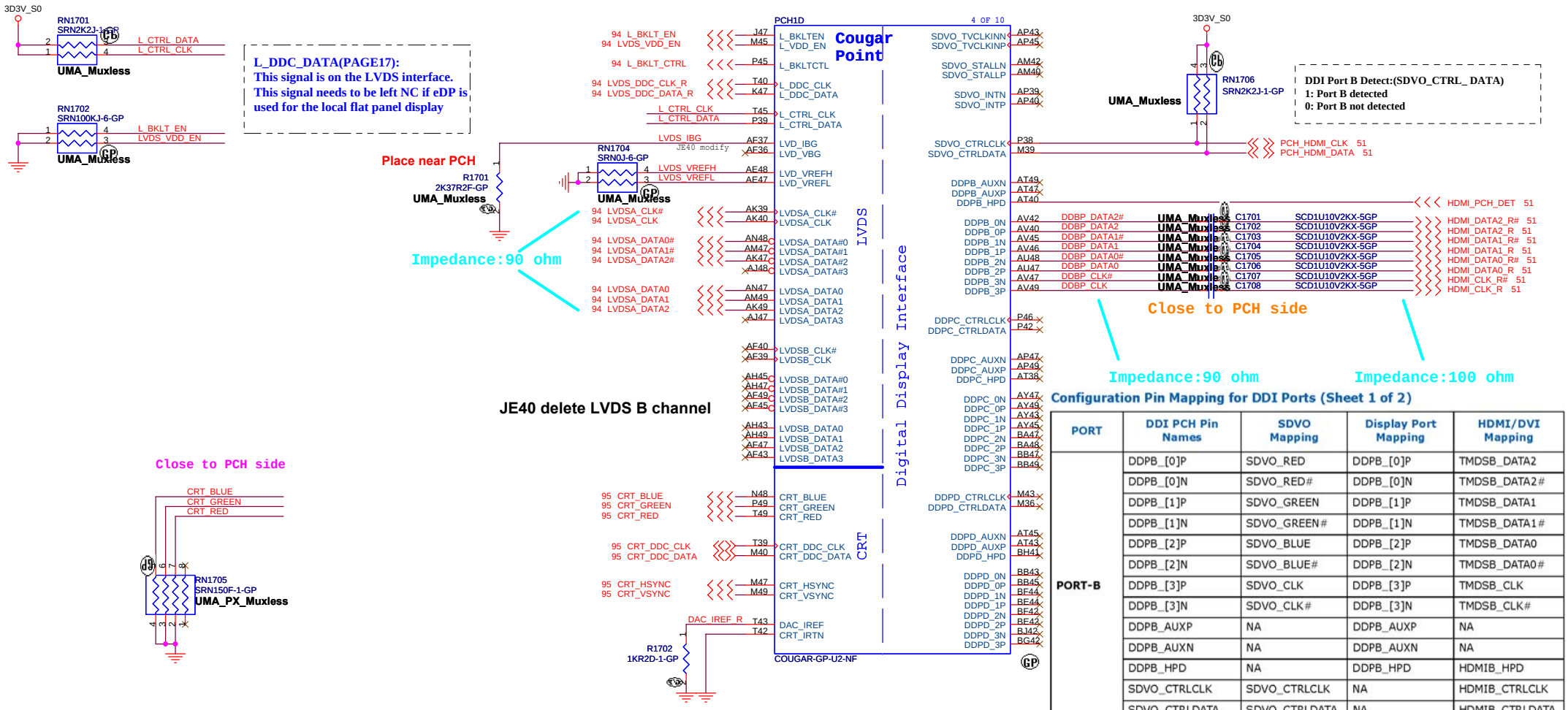
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A4	**JE40-HR**	**-1**

Date: Thursday, December 02, 2010 Sheet 16 of 102



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

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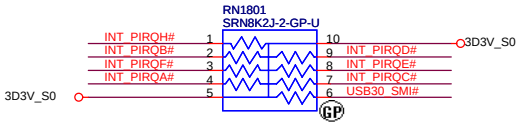
Title: PCH (LVDS/CRT/DDI)

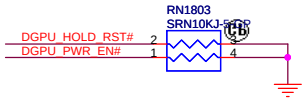
Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 17 of 102

SSID = PCH



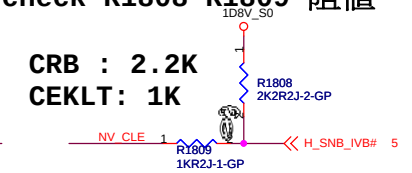
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

check R1808 R1809 阻值

CRB : 2.2K
CEKLT: 1K



USB Ext. port 1 (HS)
External debug port use on Huron river platform

SB add USB port 5

JE40 co-lay USB2.0

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER(DY)
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

HR UMA

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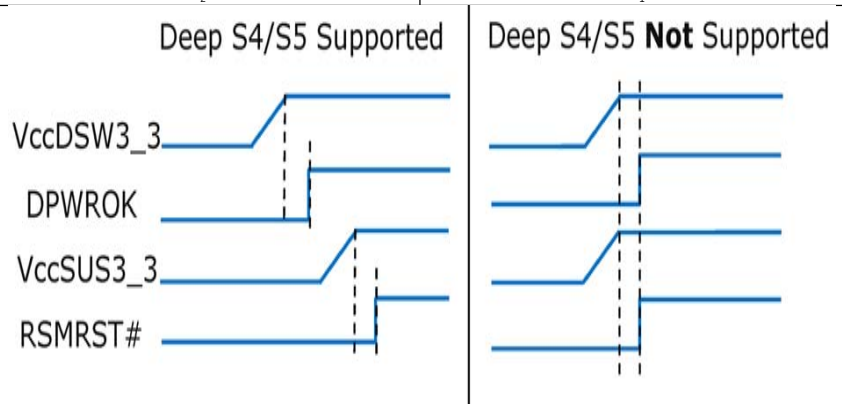
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)
Size: A3 | Document Number: JE40-HR | Rev: -1
Date: Thursday, December 02, 2010 | Sheet 18 of 102

SSID = PCH



Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

JE40 modify 07/16

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

SB modify

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

PWRBTN#
This signal has an internal pull-up resistor

PM_RSMRST#
CRB : PL 10K
ANNIE : PL 100K

HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PCH (DM I/FDI/PM)		
Size: A3	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 19 of 102	

SSID = PCH

PCH1B — Cougar Point — 2 OF 10

W-WAN · WLAN · Card Reader · LAN · USB3.0 · Intel GBE LAN · Dock · NEW CARD

PCI-E* · SMBUS · Controller Link · CLOCKS · FLEX CLOCKS

COUGAR-GP-U2-NF

JE40 delete New Card function

JE40 delete XDP function

SB

CRB : 1K
CEKLT: 10K

For DIS_PX mode or MXM mode.

R2008 and C2008 CO-LAY

UMA_DISCRETE#
UMA: 1 1
DIS :0 1
SG(PX) : 0 0
Optimus(Muxless) : 1 0

WWAN CLK · WLAN CLK · LAN CLK · USB3.0 CLK

PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

RTS

need very close to PCH

- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

HR UMA

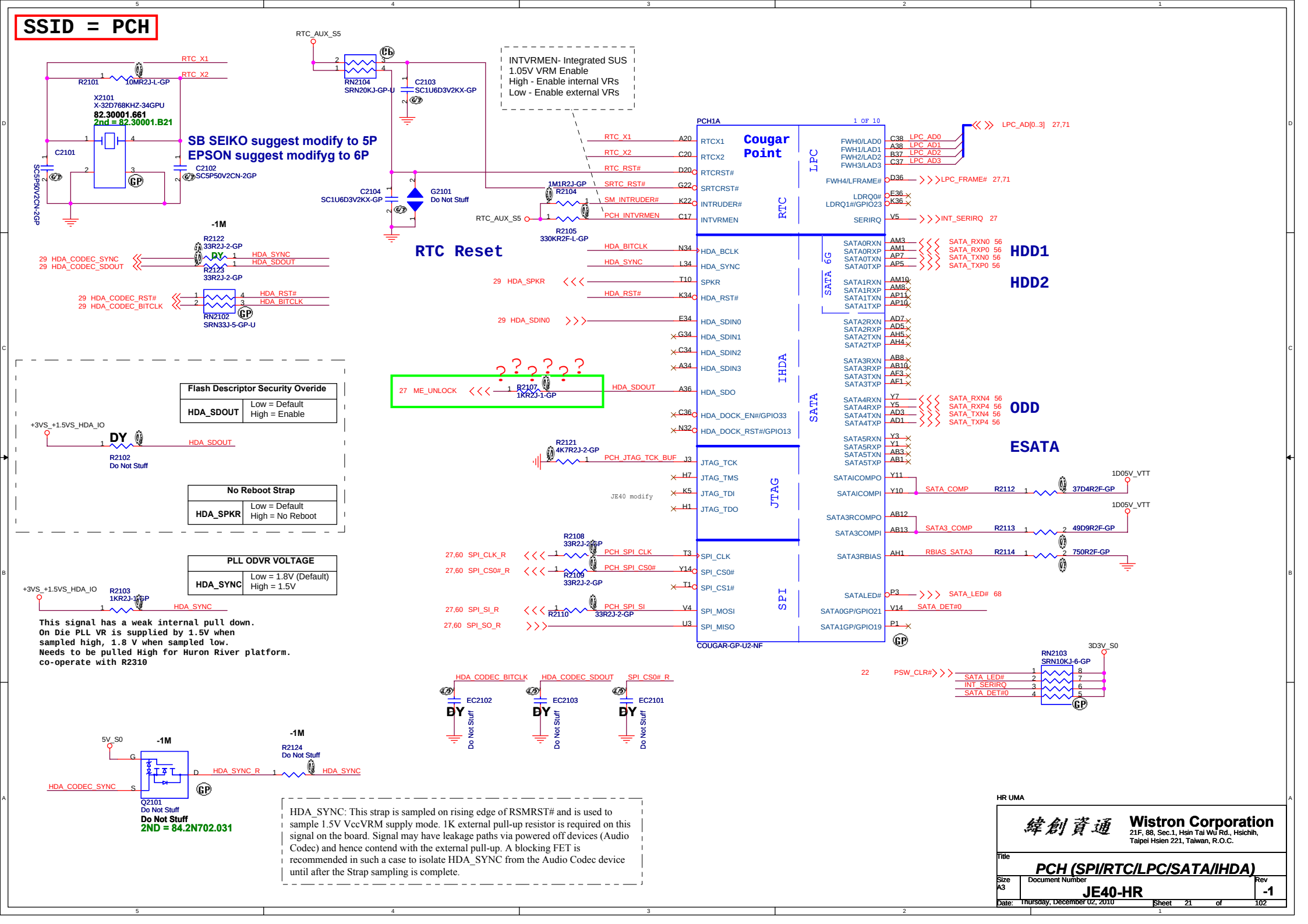
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 20 of 102

SSID = PCH



HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 21 of 102

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

Pass Word Clear

JE40 delete G Sensor

SB add Zero ODD function

SB 公板 check different , check need modify or not check intel , R2204

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT]
	LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

SB VRAM Frequency
Pull high: 800MHZ
Pull low :900MHZ

VRAM Size

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 22 of 102

SSID = PCH 6A

POWER

PCH1G — Cougar Point — 7 OF 10

COUGAR-GP-U2-NF

VCC CORE

1D05V_VTT — 1.3A — (1uFx3) (10uFx1_0603)

C2301 SC10U6D3V5KX-1GP, C2302 SC1U6D3V2KX-GP, C2303 SC1U6D3V2KX-GP, C2304 SC1U6D3V2KX-GP

AA23 AC23 AD21 AD23 AE21 AE23 AG21 AG23 AG24 AG26 AG27 AG29 AJ23 AJ26 AJ27 AJ29 AJ31 — VCCCORE

CRT

VCCADAC — U48 +VCCA_DAC_1_2

(0.1uF/0.01uF x1) (10uF x1_0603)

R2301 Do Not Stuff — 3D3V_S0

R2315 Do Not Stuff — 3D3V_DAC_S0

C2313 SCD01U50V2KX-3GP, C2314 SCD01U50V2KX-5GP, C2315 Do Not Stuff

UMA_PX_Muxless UMA_PX_Muxless

VSSADAC — U47

LVDS

VCCALVDS — AK36 +3VS_VCCA_LVDS — 0.001A — R2304 0R3J-0-U-GP — 3D3V_S0

UMA_PX_Muxless

VSSALVDS — AK37 — DIS — R2303 Do Not Stuff

VCCTX_LVDS — AM37
VCCTX_LVDS — AM38
VCCTX_LVDS — AP36
VCCTX_LVDS — AP37

0.06A — +1.8VS_VCCTX_LVDS — R2305 0R5J-5-U-GP — 1D8V_S0

UMA_PX_Muxless

R2309 Do Not Stuff — DIS

C2316 SCD01U16V2KX-3GP, C2317 SCD01U16V2KX-3GP, C2318 Do Not Stuff — DY

UMA_PX_Muxless UMA_PX_Muxless

(0.01uF x2) (22uF x1)

HVCMOS

VCC3_3 — V33 — 3D3V_S0

VCC3_3 — V34

C2319 SCD01U10V2KX-5GP

-2 modify power net name

VCCVRM — AT16 — VCCVRM_S0

DMI

VCCDMI — AT20 — JE40 modify — 1D05V_VTT — (1uF x1)

C2320 SC1U6D3V2KX-GP

VCCCLKDMI — AB36

0.02A — +1.05VS_VCC_DMI_CCI — L2303 IND-10UH-218-GP — 1D05V_VTT

68.10050.10Y

2nd = 68.10090.10B

C2321 SC1U6D3V2KX-GP, C2325 Do Not Stuff — DY

(1uFx1) (10uFx1)

NAND / SPI

VccDFTERM — AG16
VccDFTERM — AG17
VccDFTERM — AJ16
VccDFTERM — AJ17

0.19A — 1D8V_S0 — JE40 modify

C2326 SCD01U10V2KX-5GP, C2322 SCD01U10V2KX-5GP

VCCSPI — V1

0.02A — 3D3V_S5 — (1uFx1)

C2323 SC1U6D3V2KX-GP

FDI

1D05V_VTT — AN19 — VCCIO

JE40 modify 07/16

JE40 modify — BJ22 — VCCAPLLEXP

1D05V_VTT — 2.925A(Total current of VCCIO) — (1uF x4)

C2306 Do Not Stuff — DY, C2307 SC1U6D3V2KX-GP, C2308 SC1U6D3V2KX-GP, C2309 SC1U6D3V2KX-GP

AN16 AN17 AN21 AN26 AN27 AP21 AP23 AP24 AP26 AT24 AN33 AN34 — VCCIO

0.266A (Totally VCC3_3 current) — 3D3V_S0 — (0.1uF x1)

C2310 SCD1U10V2KX-5GP

BH29 — VCC3_3

0.159A(Totally current of VCCVRM) — -2 modify power net name

VCCVRM_S0 — AP16 — VCCVRM

0806 check VCCAFDIPLL — BG6 — VCCAFDIPLL

1D05V_VTT — AP17 — VCCIO

0.042A (Totally current of VCCDMI) — 1D05V_VTT — AU20 — VCCDMI — JE40 modify

U2301 for ANNIE flicker issue
R2312 for don't flicker solution

3.3V CRT LDO

U2301 G9091-330T11U-GP
74.09091.J3F
2nd = 74.09198.G7F

5V_S0 — VIN GND EN — VOUT NC#4 — 3D3V_DAC_S0

C2311 SC1U6D3V2KX-1GP

UMA_PX_Muxless UMA_PX_Muxless

C2312 SC1U6D3V2KX-GP, C2327 SC1U6D3V3MX-GP

UMA_PX_Muxless UMA_PX_Muxless

SB add C2327

-1M add LDO for VCCVRM_S0

3D3V_S0 — 1D5V_S0 — VCCVRM_S0

U2302 G913CF-GP
74.00913.A3F

SHDN# GND IN — SET OUT

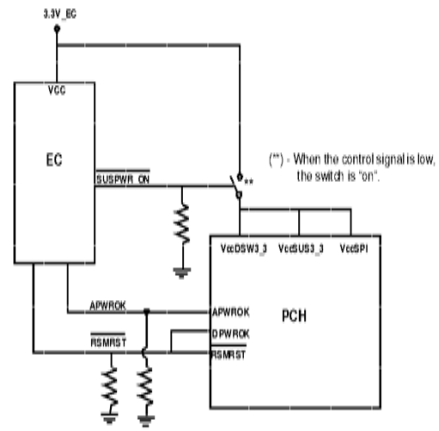
C2328 SC1U10V3KX-3GP DY, C2329 SC4D7U6D3V3KX-GP DY

C2330 SC22P50V2JN-4GP DY, R2316 2K8R2F-GP DY

C2331 SCD01U10V2KX-5GP DY, R2317 10KR2J-3-GP DY

Vout=1.25*(1+R1/R2)

Refer to NPCE795 shared SPI flash architecture



SB 公板suggest delete 3D3V_S0, R2313
SPI only support 3D3V_S5

The same BIOS SPI ROM power

HR UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (POWER1)	
Size A3	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010	Sheet 23 of 102	

JE40 modify 07/16

SSID = PCH

PCH1J

POWER

Cougar Point

10 OF 10

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

MISC

CPU

RTC

HDA

COUGAR-GP-U2-NF

VCCACLK
VCCDSW3_3
DCPSUSBYP
VCC3_3
VCCAPLLDMI2
VCCIO
DCPSUS
VCCASW
VCCRTC
V_PROC_IO
VCCADPLLA
VCCADPLLB
VCCVRM
DCPRTC
VCCSSC
DCPSST
VCCIO
VCCDIFFCLKN
VCCSUS3_3
V5REF_SUS
V5REF
DCPSUS
VCCAPLLSATA
VCCSUSHDA

0.002A
0.097A (Totally current of VCCSUS3_3)
0.001A
1.01A (Total current of VCCASW)
0.16A (Totally current of VCCVRM)
0.08A
0.055A
0.095A
0.001A
6uA
0.01A

-1M modify power net name

(1uFx1)
(0.1uFx1)
(10uFx1)
(220uFx1)
(22uFx2_0603)
(1uFx3)
(0.1uFx2)
(4.7uFx1_0603)
(0.1uFx1)

L2402 IND-10UH-218GP 68.10050.10Y 2nd = 68.10090.10B
L2403 IND-10UH-218GP 68.10050.10Y 2nd = 68.10090.10B

+1.05VS_VCCA_A_DPL
+1.05VS_VCCA_B_DPL
+VCCRTCEXT
+VCCSST
+5VA_PCH_VCC5REFSUS
+5VS_PCH_VCC5REF
+3VS_+1.5VS_HDA_IO
RTC_AUX_S5

JE40 modify 07/16

D2401 Do Not Stuff DY 2nd = 83.R2004.B8F
D2402 Do Not Stuff DY 2nd = 83.R2004.B8F
R2408 10R2J-2-GP
R2407 10R2J-2-GP
R2414 Do Not Stuff
R2402 Do Not Stuff
U2401 Do Not Stuff
R2409 Do Not Stuff
R2415 Do Not Stuff
R2413 Do Not Stuff

HR UMA

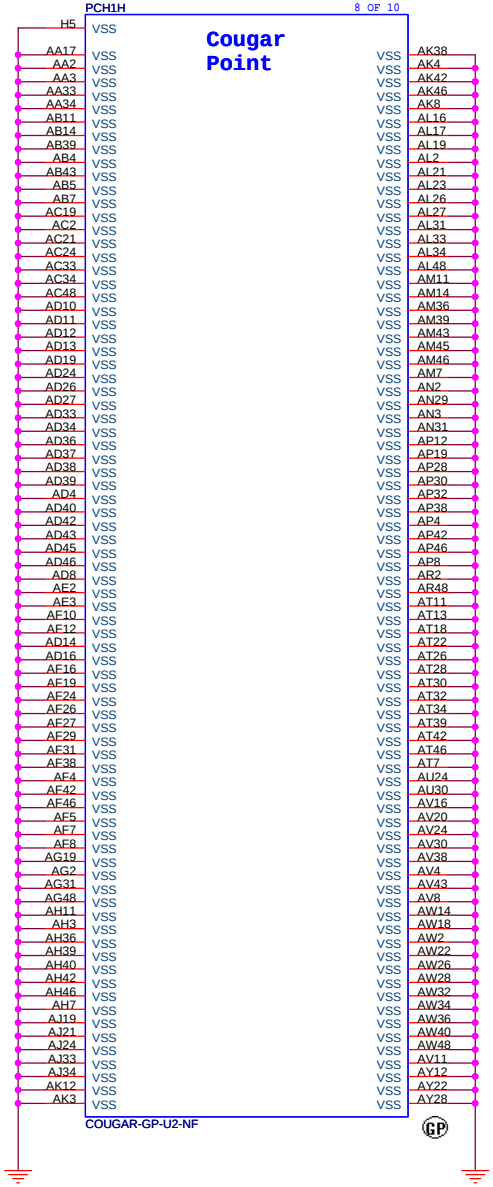
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

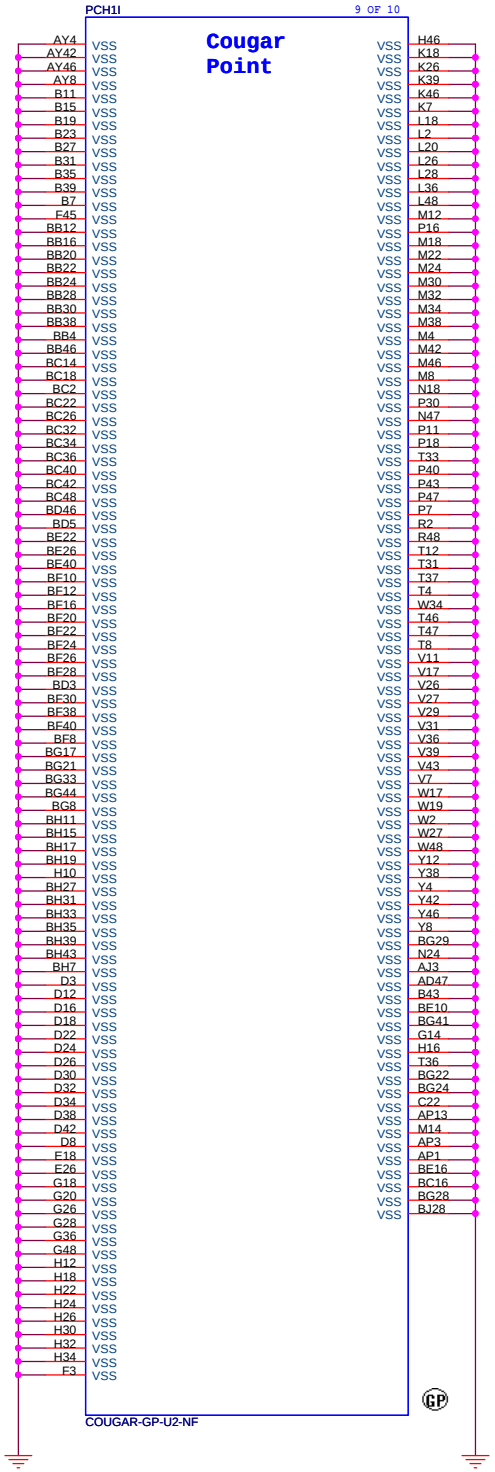
Title: PCH (POWER2)

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 24 of 102

SSID = PCH





HR UMA

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Title: ***PCH (VSS)***

Size	Document Number	Rev
A3	**JE40-HR**	-1

Date: Thursday, December 02, 2010 Sheet 25 of 102

HR UMA

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Title: ***Clock(colay)***

Size	Document Number	Rev
A4	**JE40-HR**	**-1**

Date: Thursday, December 02, 2010 Sheet 26 of 102

SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
-1M	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V

PSL SOLUTION
(Power Switch Control Logic)

NO PSL SOLUTION

SB modify R2756 stuff, R2760 change DY

SB to -1 default active Low

JE40 delete USB Charger function

JE40 VGA_THRM

0628 Modify:
Move R2771 to closed 3D3V_AUX_KBC power rail base on layout placement.

0604 Modify:
RN2704 pull-Low 10K Resistor to DY on BLUETOOTH_EN.

NOTE:
Locate resistors R2719 and R2722 close to the NPCE791L.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

<------ TP

<------ BATTERY / CHARGER

<------PCH / EDP

SB to -1

JE40 delete AMP function

C2716 need very close to EC

如果移除PLS function 要改成pull high 3D3V_AUX_S5

EC GPIO standard PH/PL

SB to -1

SB LID_CLOSE# can not pull high, because push pull suggest RN2708 Pin5 change FAN_TACH1

0604 Modify:
Add Pull down 100k ohm at F_SDI for Power consumption concern.

Prevent BIOS data loss

EC_GPIO47 High Active

ADT_TYPE A/D(PIN99)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

JE40 modify

65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete

SB EC_AGND , change GND

HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

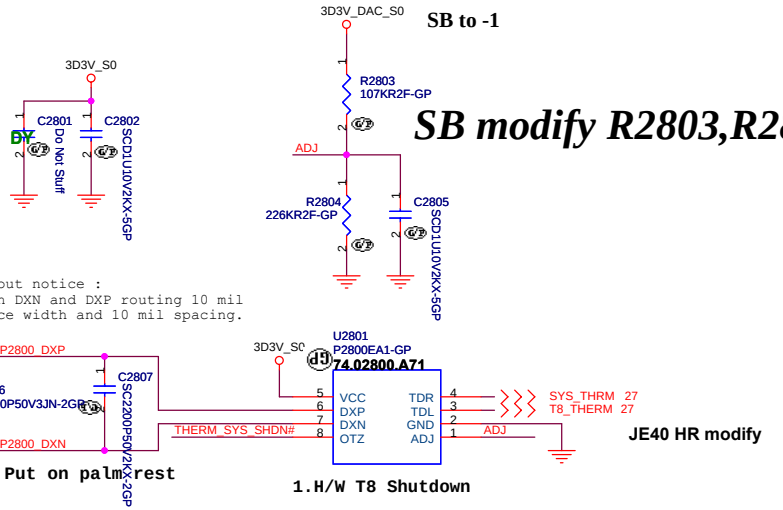
Title: KBC Nuvoton NPCE795

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 27 of 102

SSID = Thermal

Thermal sensor P2800



SB modify R2803,R2804 setting

ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

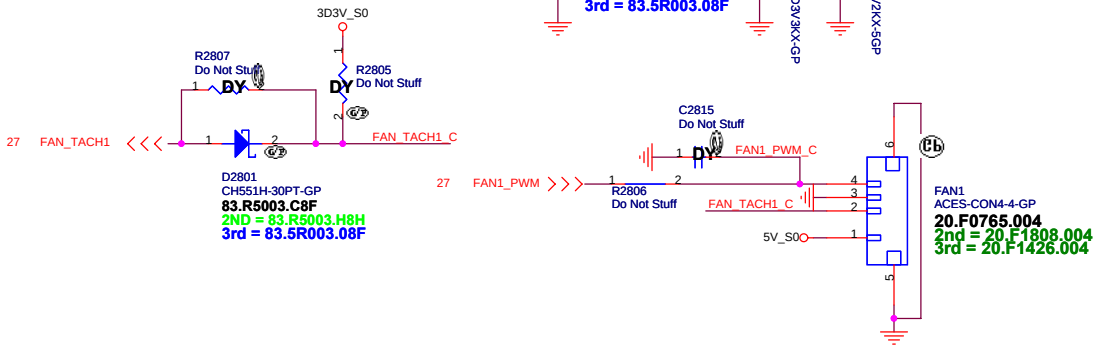
RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (v)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

VGA Thermal sensor P2800

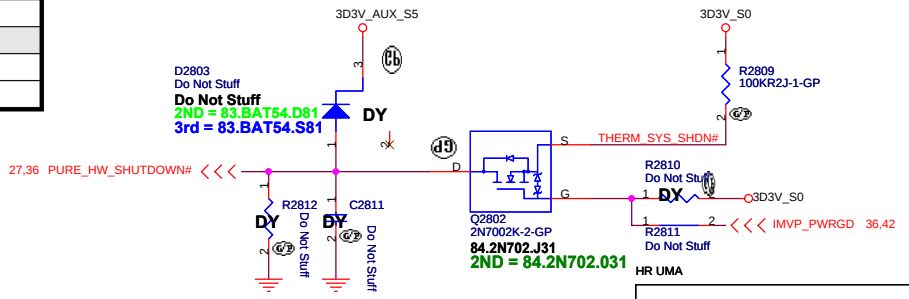
SMBUS modify to Page 84

Fan controller P2793

Layout 15 mil



For PWM FAN

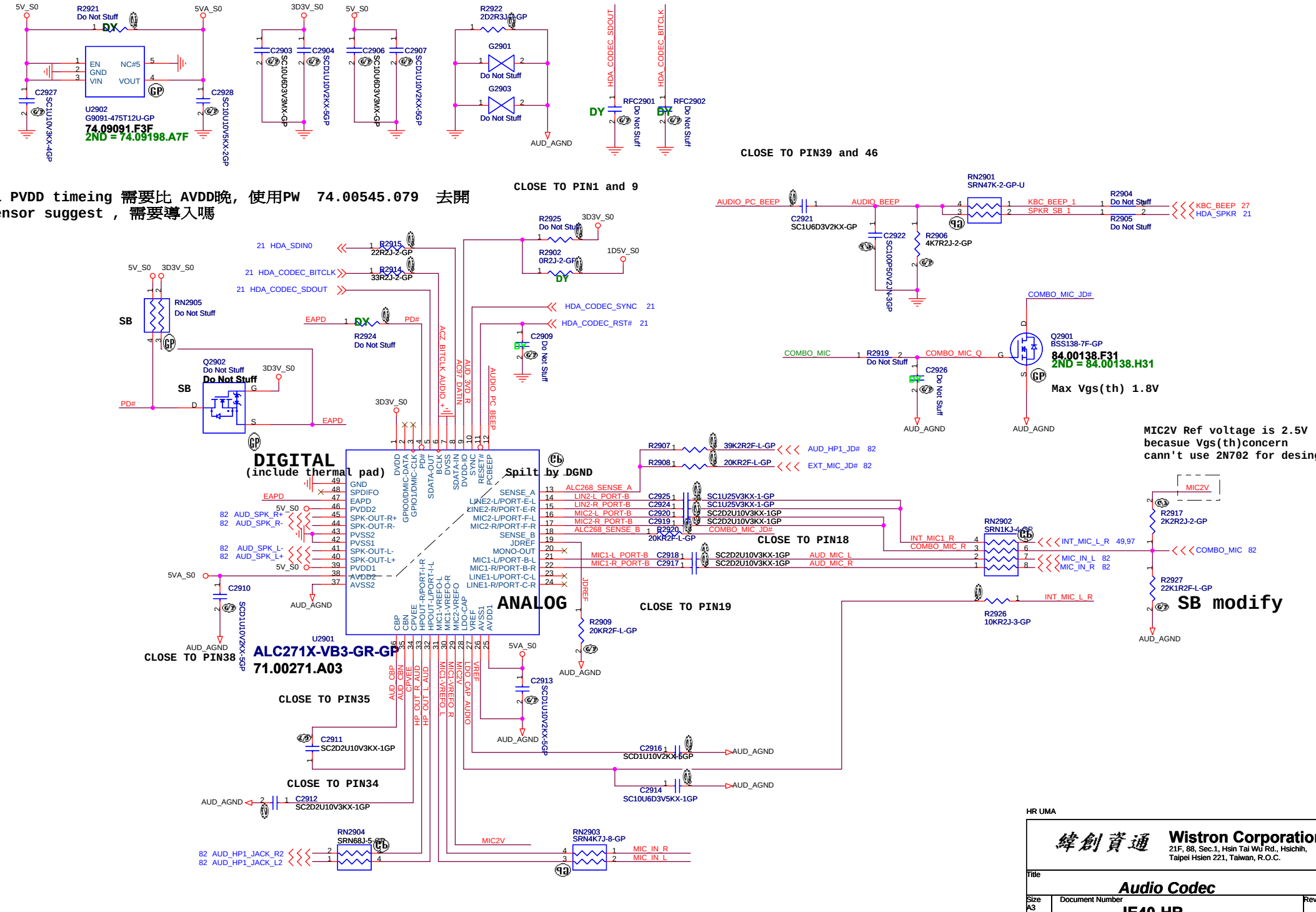


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal P2800/Fan Controllor P2793**

Size	Document Number	Rev
Custom	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 28 of 102


-1 PVDD timeing 需要比 AVDD晚, 使用PW 74.00545.079 去開
vensor suggest , 需要導入嗎
CLOSE TO PIN1 and 9
CLOSE TO PIN39 and 46
MIC2V Ref voltage is 2.5V becasue Vgs(th)concern cann't use 2N702 for desing
Max Vgs(th) 1.8V
DIGITAL
(include thermal pad)
Spilt by DGND
ANALOG
ALC271X-VB3-GR-GP
71.00271.A03
U2901
CLOSE TO PIN18
CLOSE TO PIN19
CLOSE TO PIN35
CLOSE TO PIN34
CLOSE TO PIN38
SB modify
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Audio Codec
JE40-HR
-1
Thursday, December 02, 2010

AUDIO OP AMPLIFIER

JE40 delete AMP function

HR UMA

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Title: *Audio AMP*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 30 of 102	

SB modify L3101,2,4,5,6 to 0 ohm

SB modify R3102 DY, R3104 to pull low

SB mmodify vendor suggest

SB delete EEPROM

128K byte

SB delete R3112

SB delete R3117

SB delete R3129 for LDO power

Card-reader Off-Page

Check VDDO_CR power plan

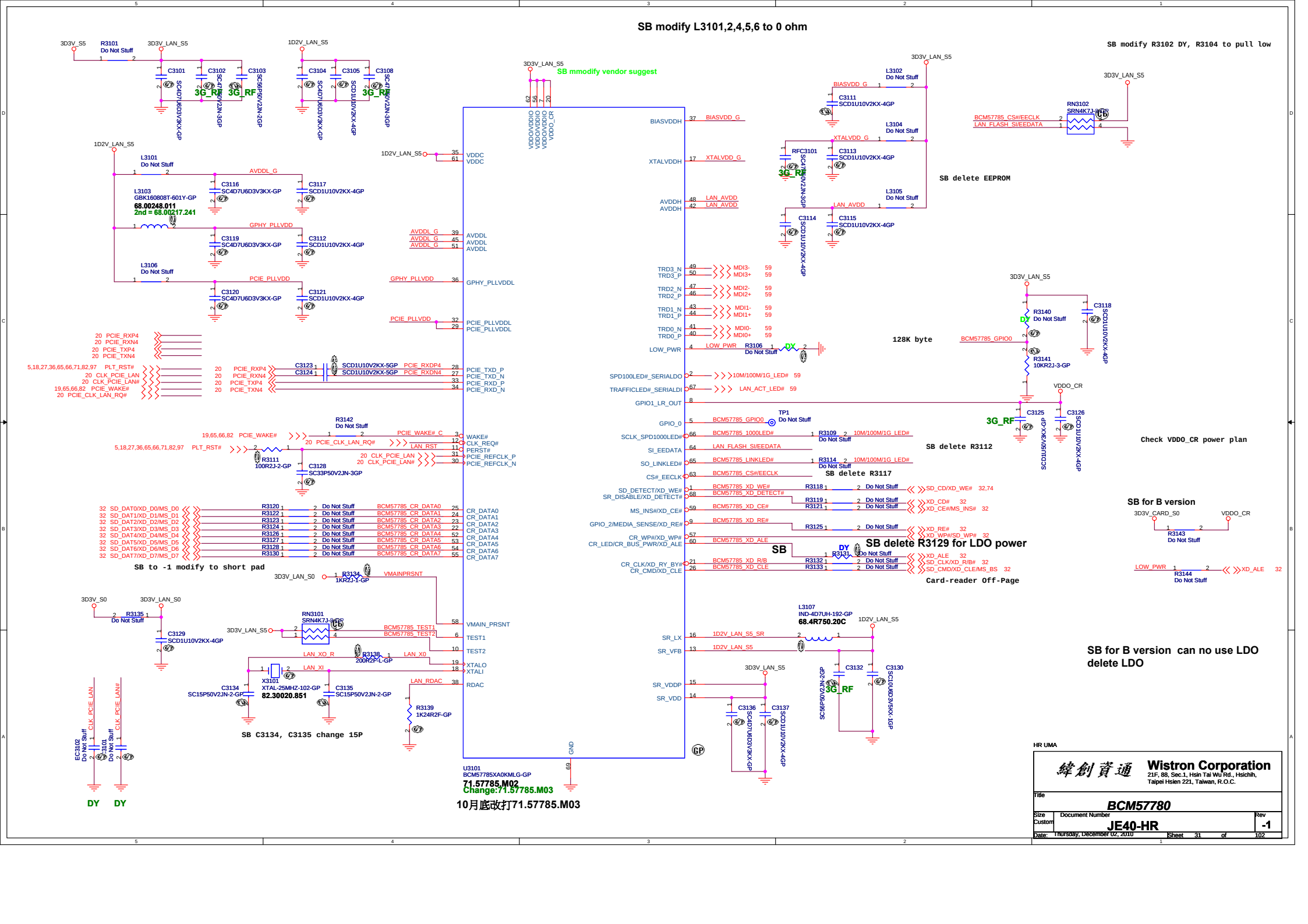
SB for B version

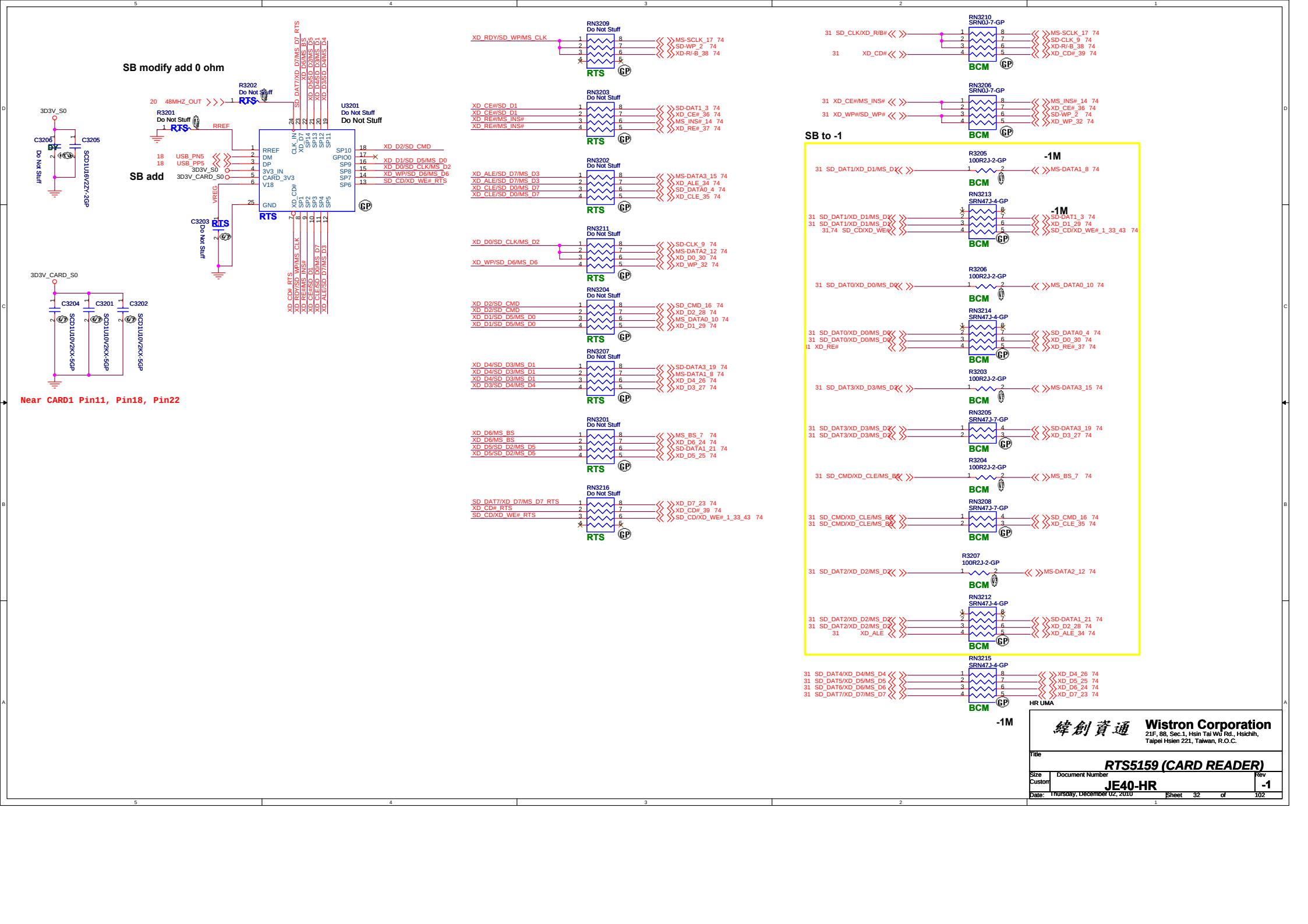
SB for B version can no use LDO delete LDO

SB to -1 modify to short pad

SB C3134, C3135 change 15P

10月底改打71.57785.M03




SB modify add 0 ohm
SB add
SB to -1
-1M
3D3V_S0
3D3V_CARD_S0
C3206
C3205
C3204
C3201
C3202
C3203
SCD1U16V2ZY-2GP
SCD1U10V2KX-5GP
R3202
R3201
U3201
Do Not Stuff
RTS
GP
BCM
HR UMA
Near CARD1 Pin11, Pin18, Pin22
RN3209
RN3210
RN3211
RN3202
RN3203
RN3204
RN3207
RN3201
RN3216
RN3206
RN3213
RN3214
RN3205
RN3208
RN3212
RN3215
R3205
R3206
R3203
R3204
R3207
SRN0J-7-GP
SRN47J-4-GP
SRN47J-7-GP
100R2J-2-GP
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RTS5159 (CARD READER)
JE40-HR
-1
Thursday, December 02, 2010
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102

(Blanking)

HR UMA

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

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(Blanking)

HR UMA

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Reserved***		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 34 of 102	

HR UMA

緯創資通 **Wistron Corporation**
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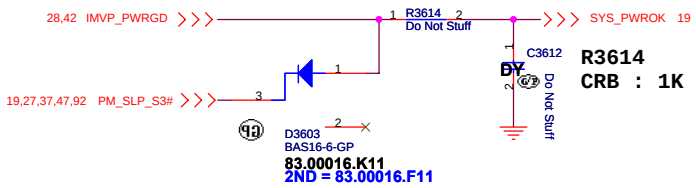
Title: ***USB 3.0 Controller***

Size	Document Number	Rev
A3	**JE40-HR**	-1

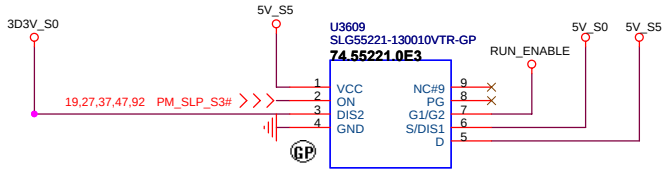
Date: Thursday, December 02, 2010 Sheet 35 of 102

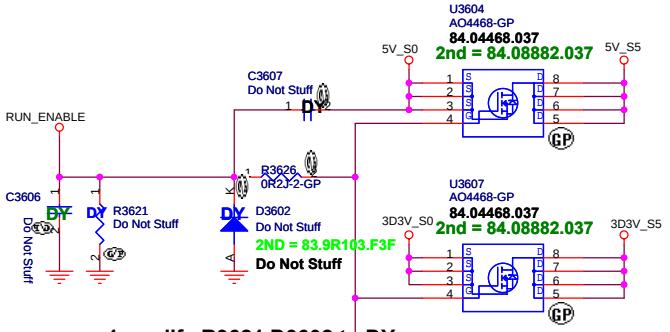
Power Sequence



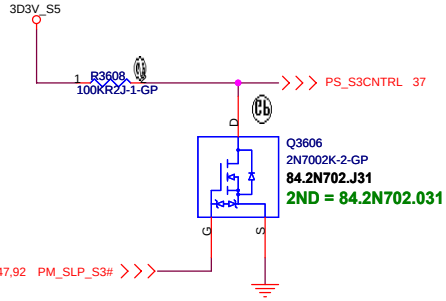
R3614
CRB : 1K

ANNIE Run Power



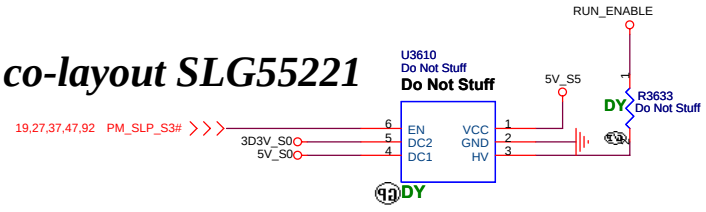


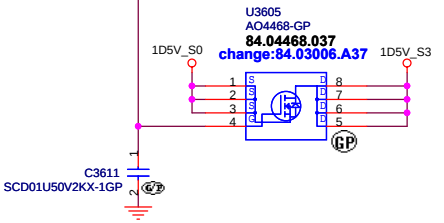
-1 modify R3621,D3602 to DY



SB modify part number

-1 co-layout SLG55221

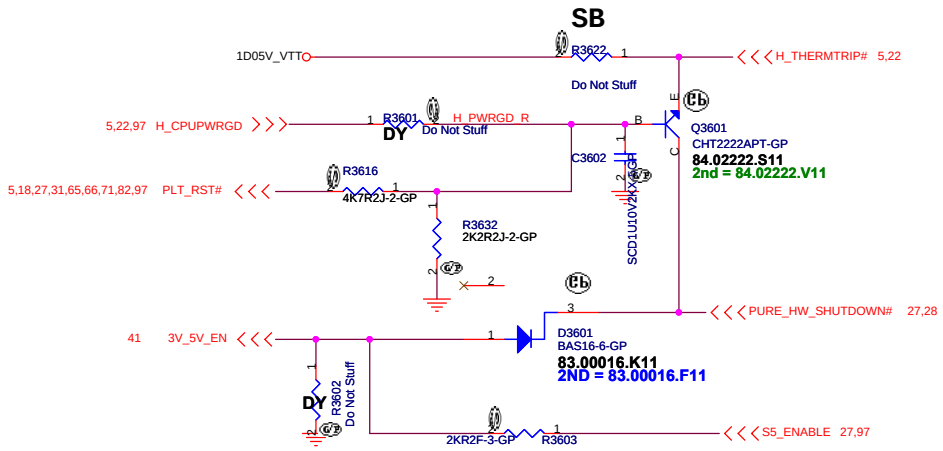




1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A

SB



HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **Power Plane Enable**		
Size: A3	Document Number: **JE40-HR**	Rev: **-1**
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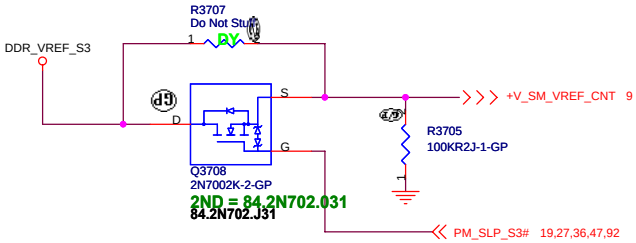
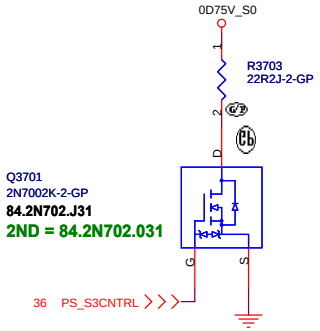
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

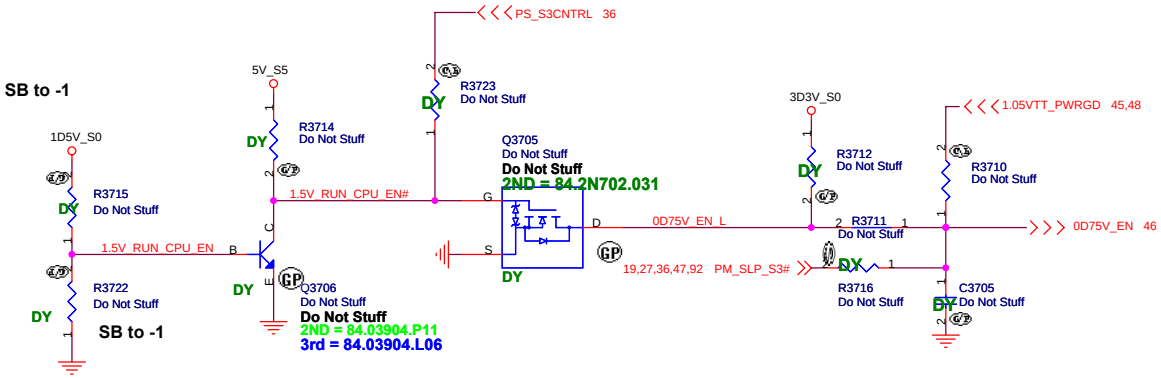


Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

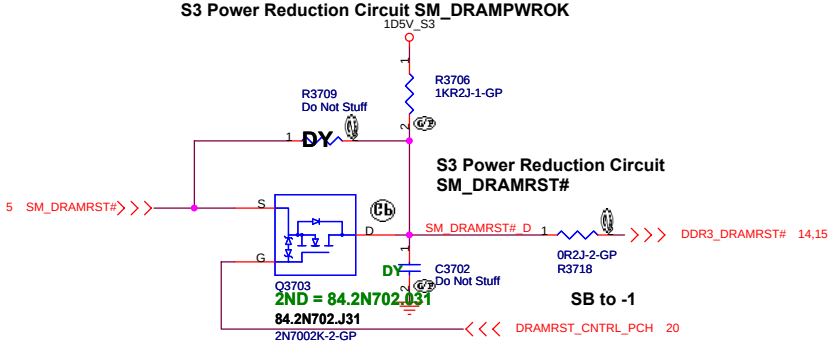


5 S3 Power Reduction X01 20091111 JE40 HR modify 驗證R3710上件

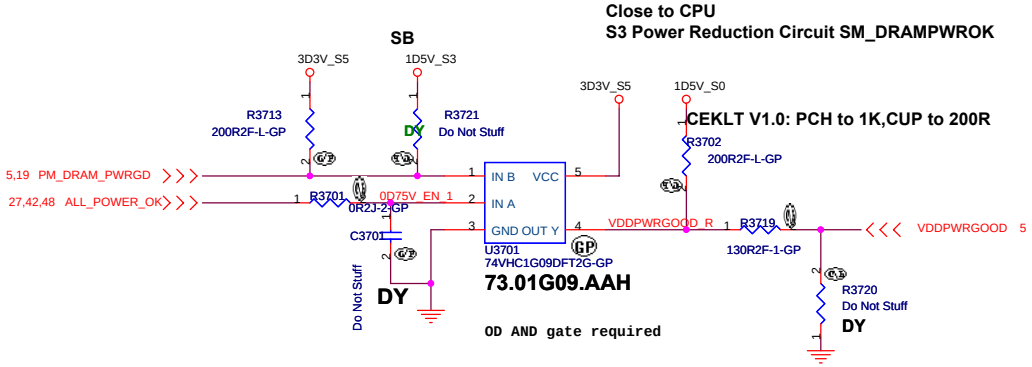
SB to -1 reserve R3723



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY

SM_DRAMPWROK must have a maximum of 15ns rise or fall time
over VDDQ * 0.55± 200mV and the edge must be monotonic

HR UMA

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Title: ADAPTER

Size	Document Number	Rev
A3	JE40-HR	-1

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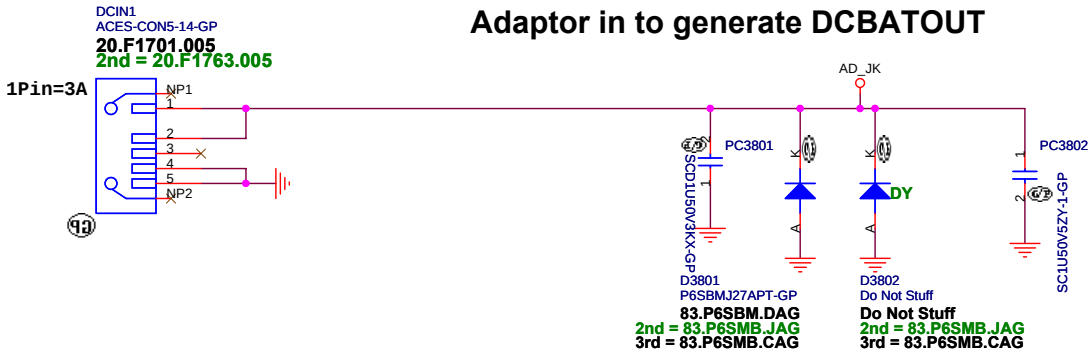
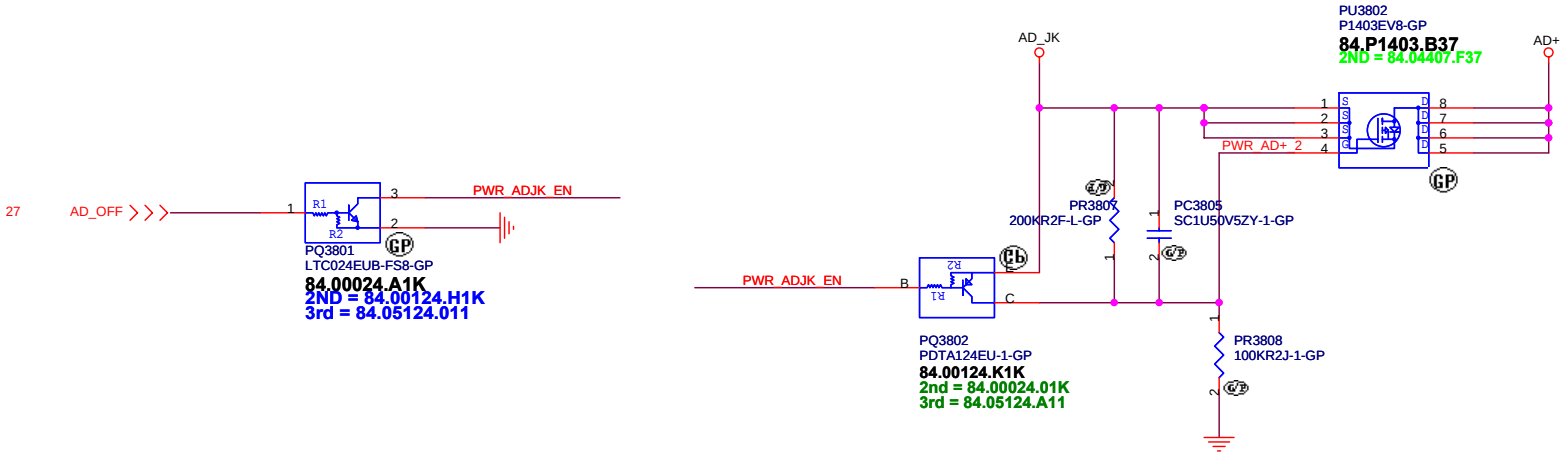
ANNIE solution

Adaptor in to generate DCBATOUT



JE40 change DCIN1 part number



HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *DCIN JACK*		
Size: Custom	Document Number: JE40-HR	Rev: -1
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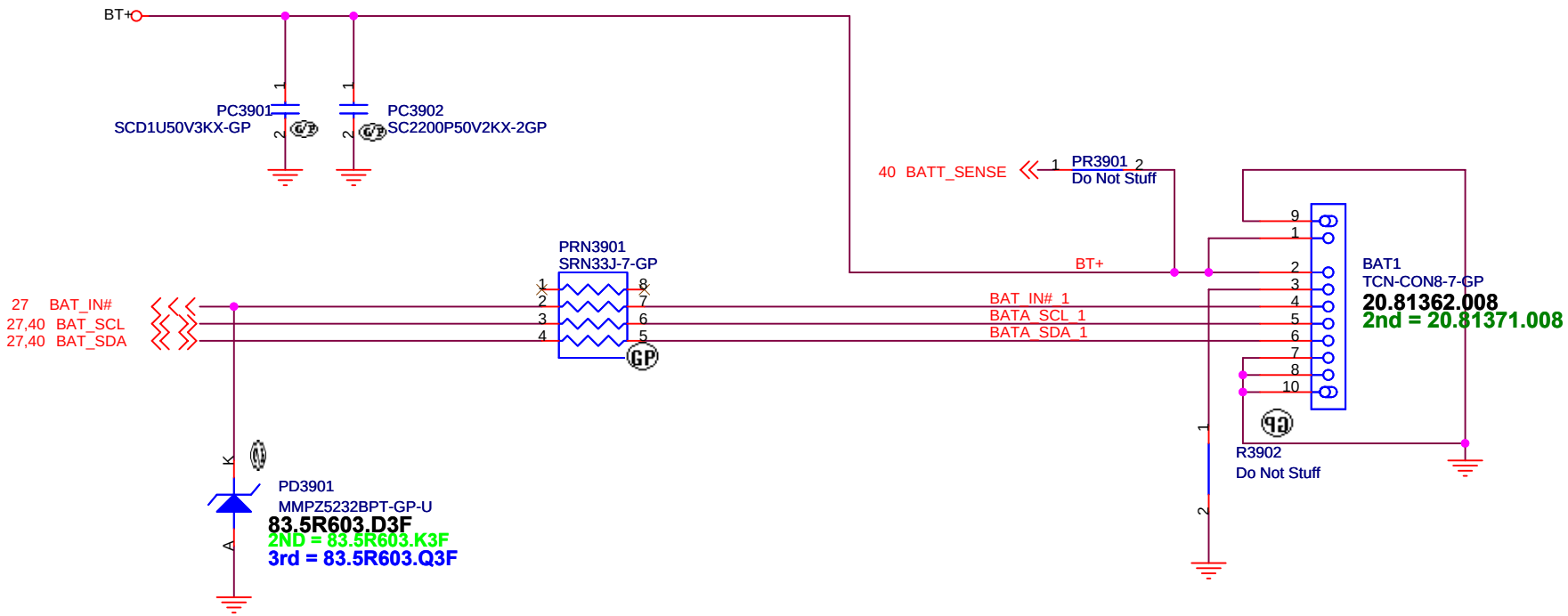
BATTERY CONNECTOR



EC Protect

HR UMA

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Title: *BATT CONN*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 39 of 102	

AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			

NEAR

ADD A 24V ZENAR

20100706 Wayne

20100721

20101018

JE40 HR RF

-1M

AC_OK to KBC

HR UMA

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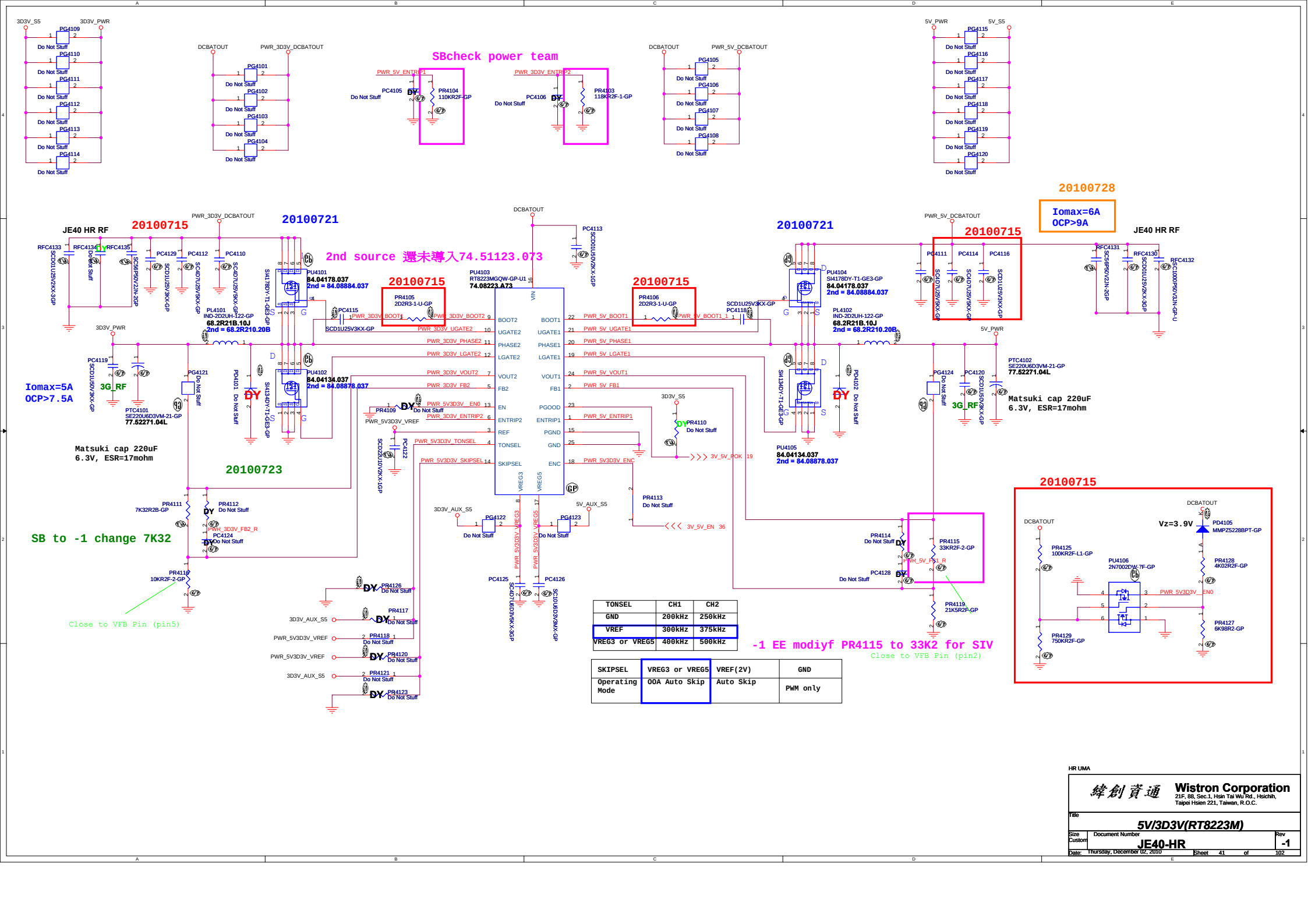
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24745

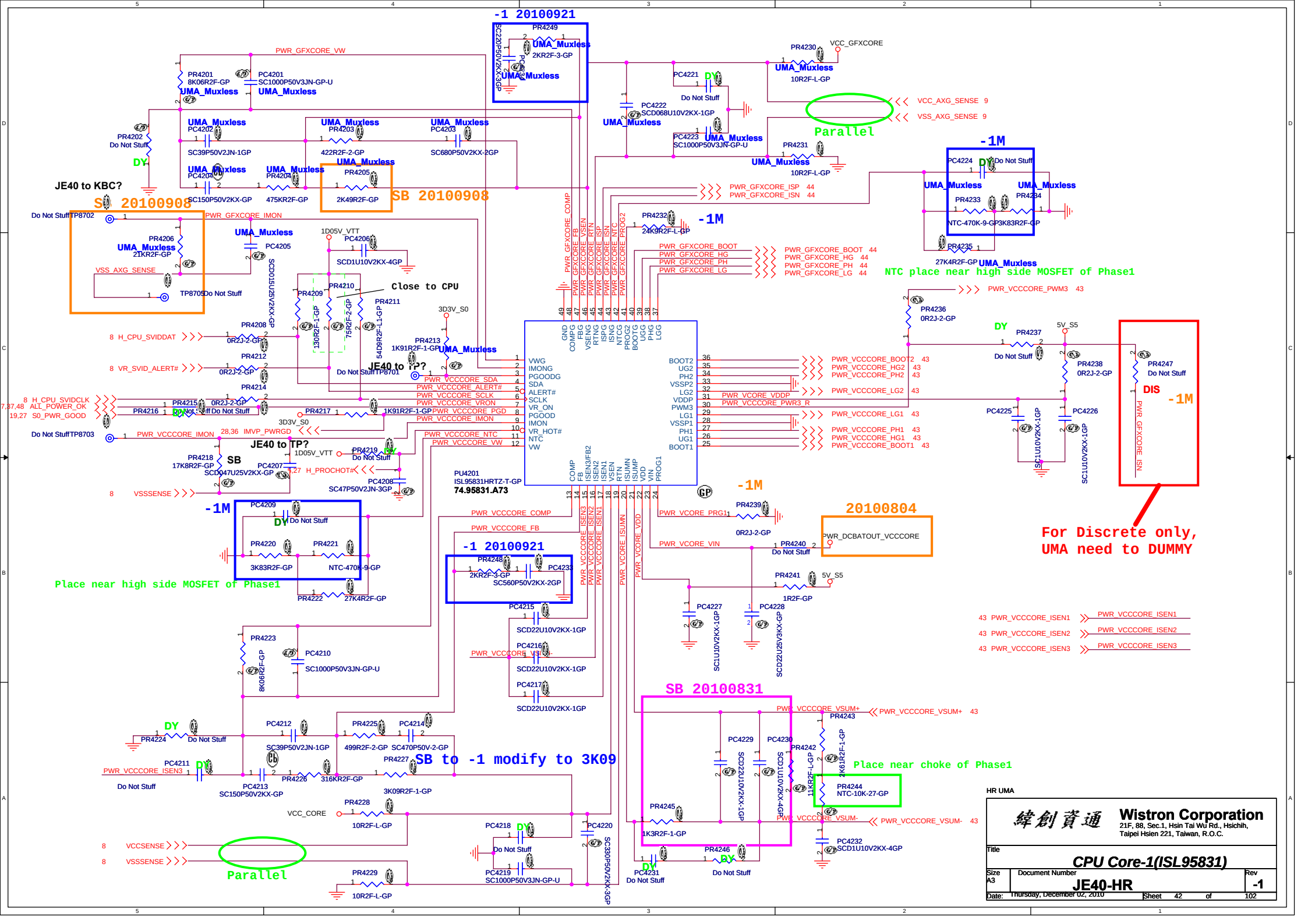
Size: A3 | Document Number: JE40-HR | Rev: -1

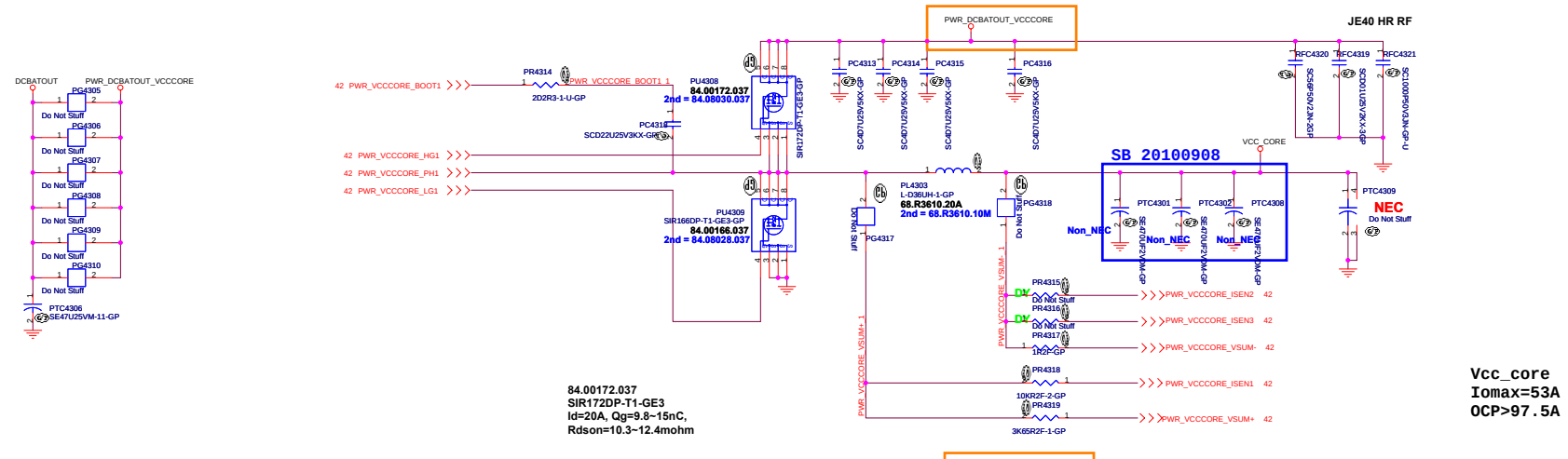
Date: Thursday, December 02, 2010 | Sheet 40 of 102

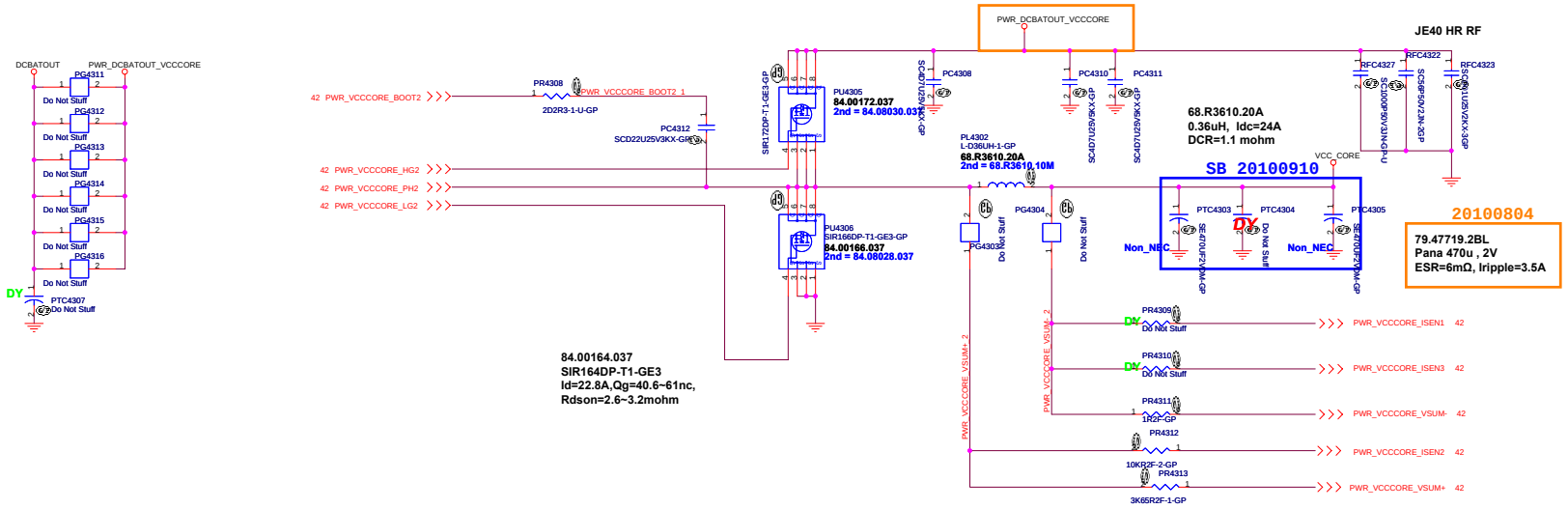


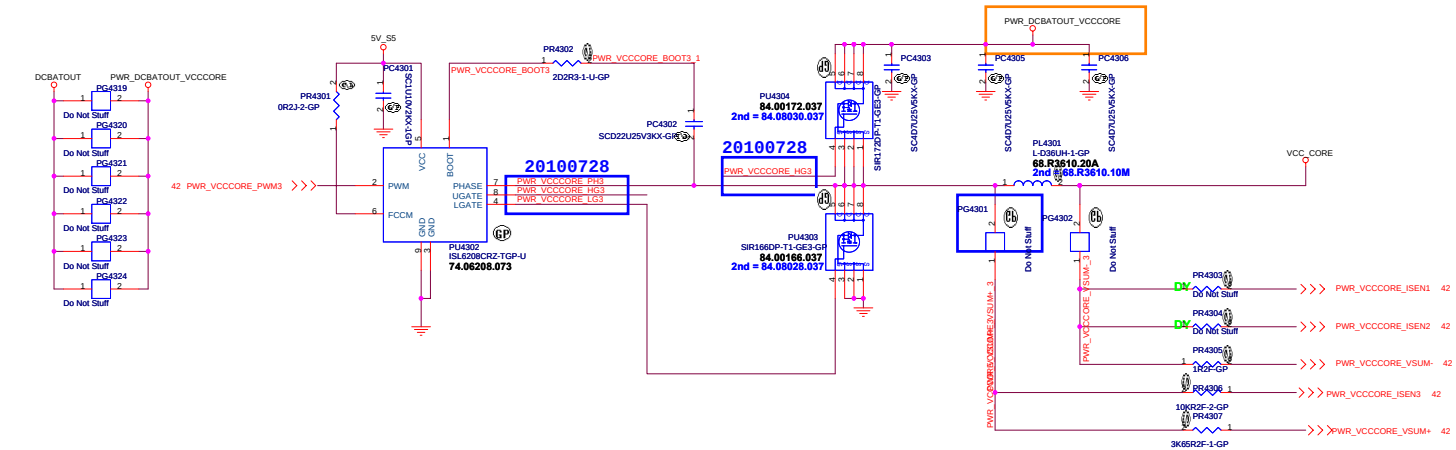
TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only


-1 20100921
SB 20100908
JE40 to KBC?
Close to CPU
JE40 to TP?
SB
-1M
Parallel
NTC place near high side MOSFET of Phase1
20100804
For Discrete only,
UMA need to DUMMY
SB 20100831
SB to -1 modify to 3K09
Place near choke of Phase1
PU4201
ISL95831HRTZ-T-GP
74.95831.A73
PWR_DCBATOUT_VCCCORE
VCC_GFXCORE
VCC_CORE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Core-1(ISL95831)
JE40-HR
Thursday, December 02, 2010







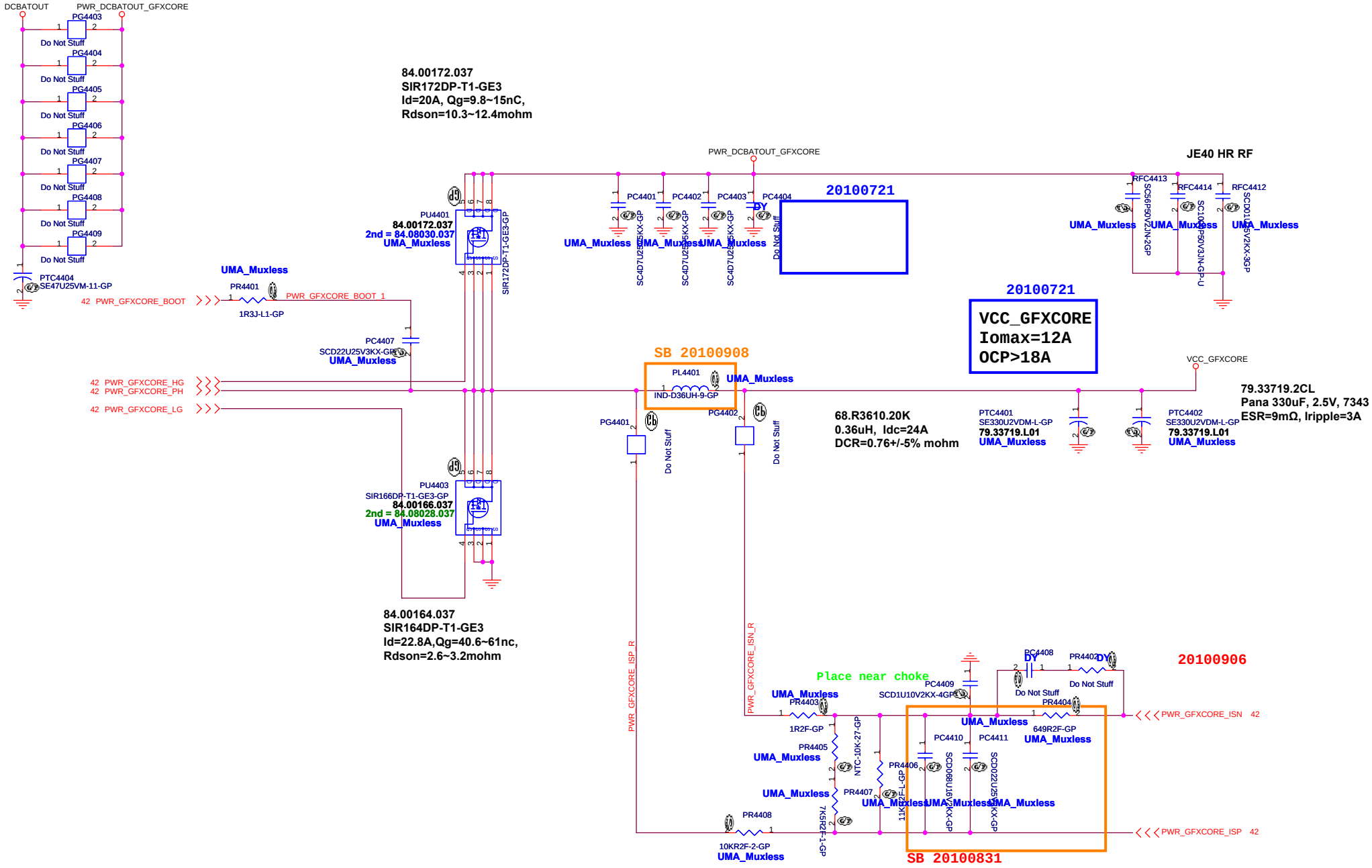
HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Core-2(ISL95831)

Size: A2 | Document Number: JE40-HR | Rev: -1

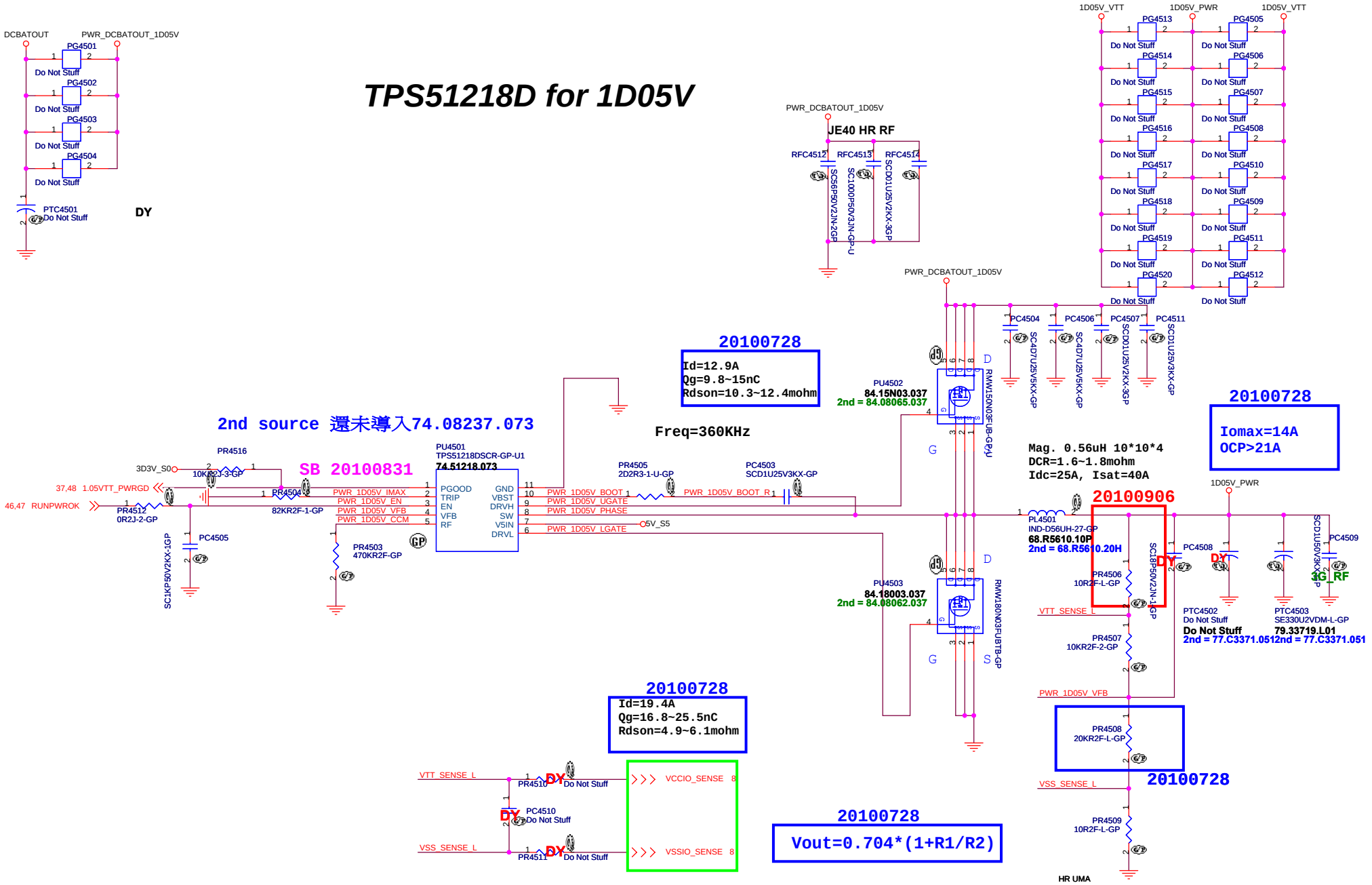
Date: Thursday, December 02, 2010 | Sheet 43 of 102



HR UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU Core-3(ISL95831)***	
Size: A3	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 44 of 102	

TPS51218D for 1D05V



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	DC to DC 1D05V(TPS51218D)		
Size: A3	Document Number: JE40-HR	Rev: -1	
Date: Thursday, December 02, 2010	Sheet 45 of 102		

SSID = PWR.Plane.Regulator_1p5v0p75v

20100805

RT8207L for 1D5V

DCBATOUT PWR_DCBATOUT_1D5V
PG4601 PG4602 PG4603 PG4604 Do Not Stuff
PTC4601 Do Not Stuff
DY

19,27 PM_SLP_S4# PR4612 Do Not Stuff PWR_1D5V_EN
PC4612 Do Not Stuff
DY

SB 20100831

PWR_1D5V_VCC5 PR4604 5D1R2F-GP 5V_S5
PC4606 SC1U10V2KX-1GP
PC4602 SC1K50V2KX-1GP
PR4603 12K4R2F-GP
PWR_1D5V_VDDP PR4605 Do Not Stuff 5V_S5
C694 SC1U10V2KX-1GP
PWR_1D5V_CS

3D3V_S5 PR4602 10KR2F-2-GP

Close to pin23

45,47 RUNPWROK
PWR_DCBATOUT_1D5V PR4610 620KR2F-GP PWR_1D5V_TON
20100728
PWR_1D5V_EN
PWR_0D75V_EN
PWR_1D5V_VTTIN
PC4603 SC10U6D3V5MX-3GP

1D5V_S3 PG4605 Do Not Stuff PG4606 Do Not Stuff
1D5V_S3 PG4607 Do Not Stuff PWR_1D5V_VDDQ
DDR_VREF_PWR

Close to pin23

20100728
Iomax=1A
OCP>1.5A

Close to output cap pin1, not inside of the output cap

PU4601 RT8207LGQW-GP-U1 74.08207.B73

Pin	Name
13	PGOOD
12	TON
11	S5
10	S3
23	VLDOIN
7	NC#7
1	VTTGND
4	MODE
24	VTT
2	VTTSNS
25	GND
3	GND
16	CS
14	VDD
15	VDDP
22	BOOT
21	UGATE
20	PHASE
19	LGATE
18	PGND
17	NC#17
8	VDDQ
9	FB
6	DEM
5	VTTREF

PWR_1D5V_BOOT PR4606 2D2R3-1-U-GP PWR_1D5V_PHASE_L PC4609 SCD1U25V3KX-GP
PWR_1D5V_UGATE
PWR_1D5V_PHASE
PWR_1D5V_LGATE
PWR_1D5V_VDDQ
PWR_1D5V_FB
5V_S5

-1 PR4608 需要將來都改32K4R

R1 PR4608 33KR2F-GP DY PC4610 Do Not Stuff
R2 PR4609 30KR2F-GP

PWR_1D5V_VTTREF PR4607 Do Not Stuff DDR_VREF_S3
PC4608 SCD033U16V2KX-GP

Close to PIN9

37 0D75V_EN PR4615 Do Not Stuff PWR_0D75V_EN

+0.75VS
Iomax: 1.2A

0D75V_S0 PG4608 Do Not Stuff PG4609 Do Not Stuff DDR_VREF_PWR
PC4604 SC10U6D3V5MX-3GP PC4605 Do Not Stuff DY

PWR_DCBATOUT_1D5V
JE40 HR RF
RFC4617 SC10U25V2KX-3GP RFC4618 SC1000P50V3JN-GP-U RFC4616 SC56P50V2JN-2GP

20100728
Id=12.9A
Qg=9.8~15nC
Rdson=10.3~12.4mohm

PU4602 84.15N03.037 2nd = 84.08065.037 RMW150N03FUB-GP-U1

20100906
PC4611 PC4614 PC4616 PC4617 SC4D7U25V5KX-GP PC4615 SCD1U25V3KX-GP

Mag. 1.0uH 10*10*4
DCR=2.9~3.3mohm
Idc=18A, Isat=36A

Iomax=12A
OCP>20A

1D5V_S3
PL4601 IND-1UH-93-GP 68.1R01B.10J 2nd = 68.1R01C.10Q
PC4613 DY
PTC4602 SE390U2D5VM-7GP 79.3971V.30L 2nd = 79.3971V.6AL
Matsuki cap 390uF 2.5V, ESR=10mohm

PU4603 84.18003.037 2nd = 84.18002.037 RMW180N03FUBTB-GP

Vout=0.75*(1+R1/R2)

20100728
Id=19.4A
Qg=16.8~25.5nC
Rdson=4.9~6.1mohm

SB R4608 chekc 修改31K6R
Vout 需再1.55V 以上

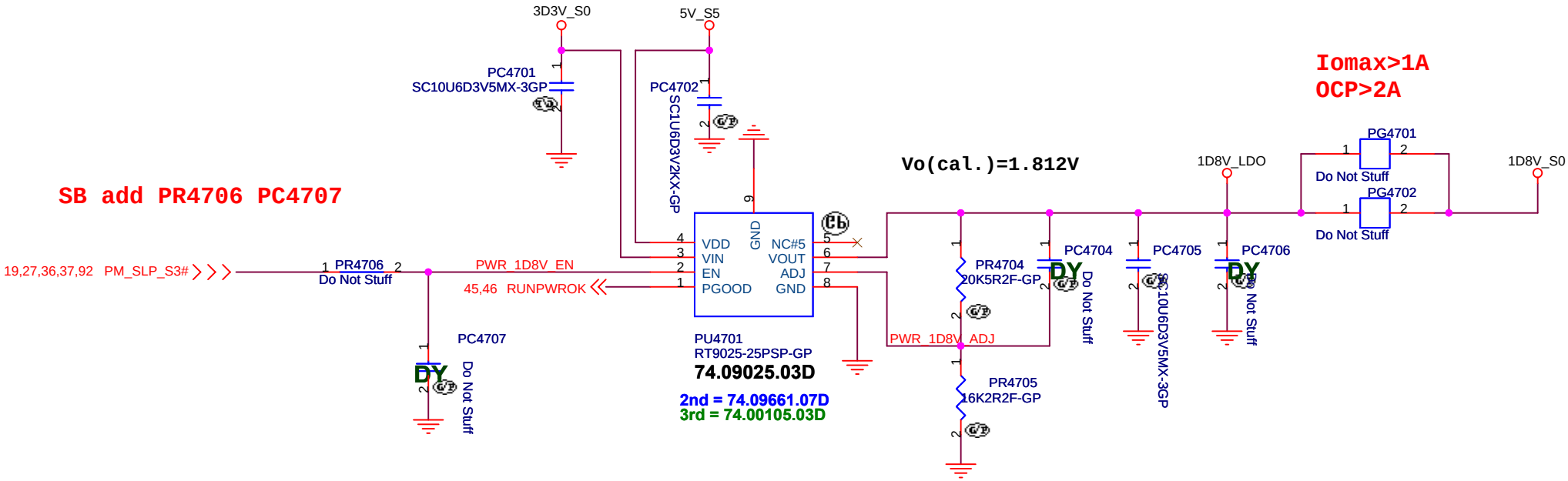
HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS5111
Size: Custom
Document Number: JE40-HR
Rev: -1
Date: Thursday, December 02, 2010
Sheet 46 of 102

SSID = PWR.Plane.Regulator_1p8v

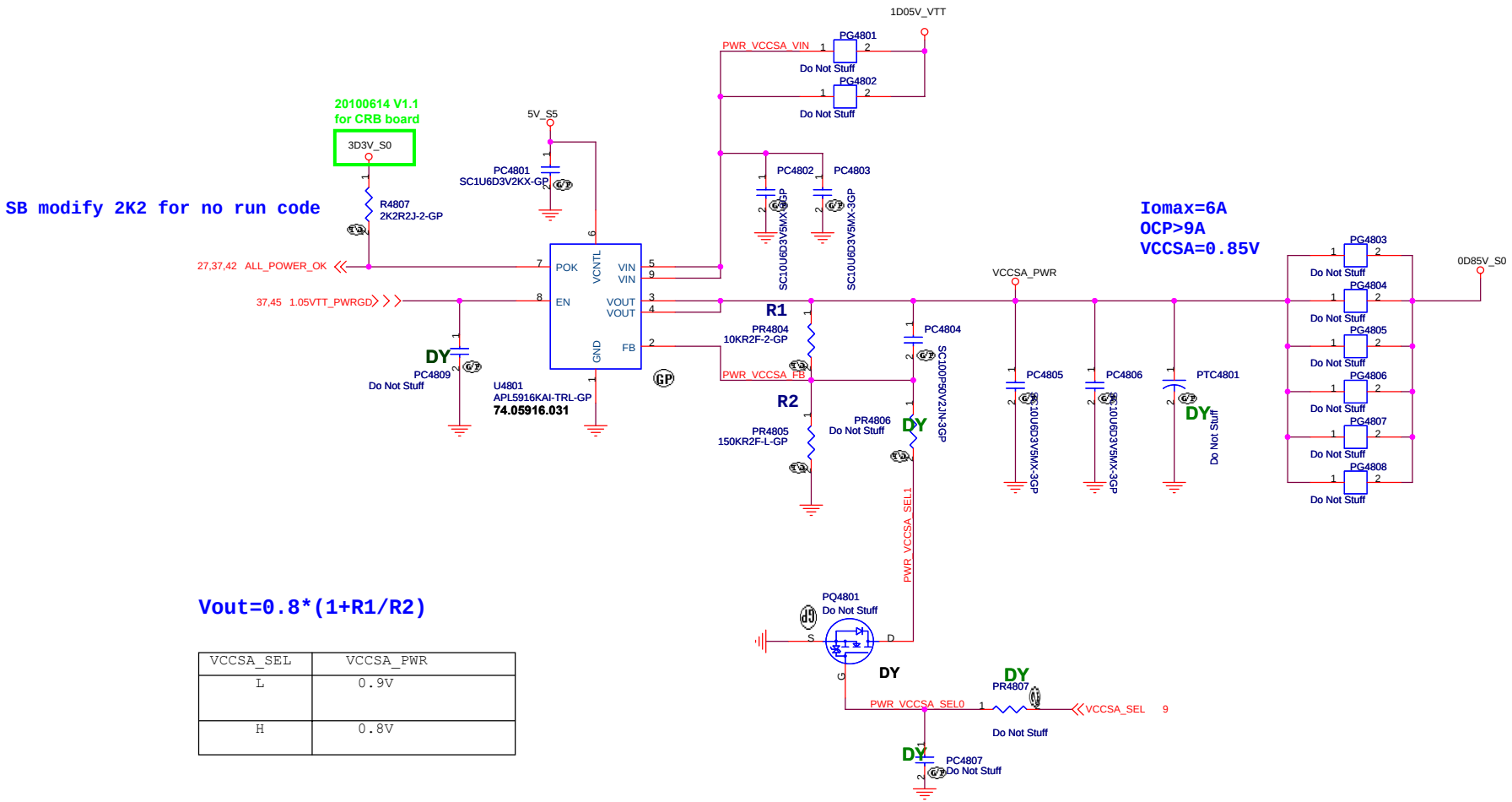
RT9025 for 1D8V_S0



HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *LDO_1D8V(RT9025)*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 47 of 102	

APL5916 for VCCSA



Vout=0.8*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

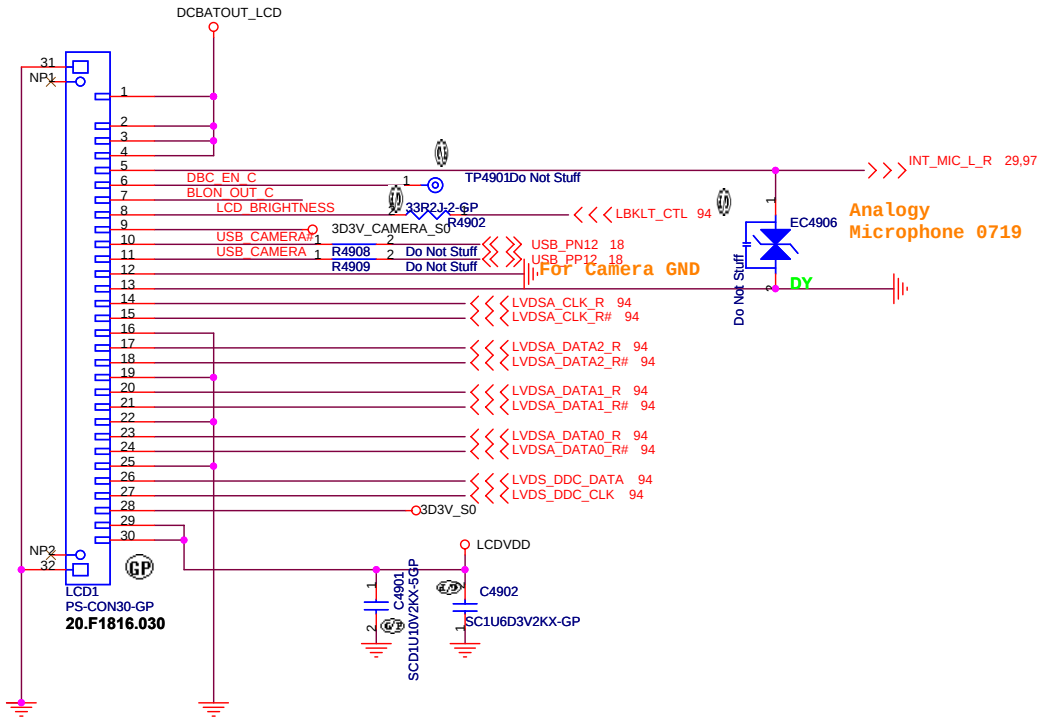
Title: LDO VCCSA(APL5916)

Size: A3 | Document Number: JE40-HR | Rev: -1

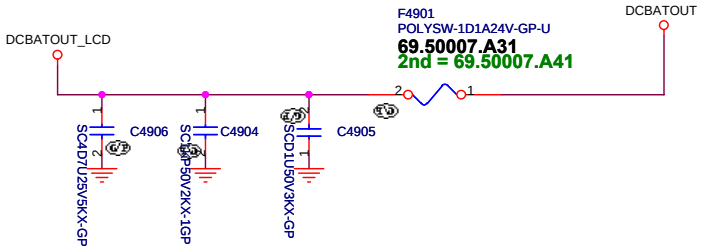
Date: Thursday, December 02, 2010 | Sheet 48 of 102

SSID = VIDEO

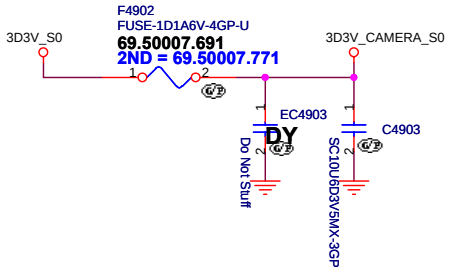
LVDS CONNECTOR



INVERTER POWER

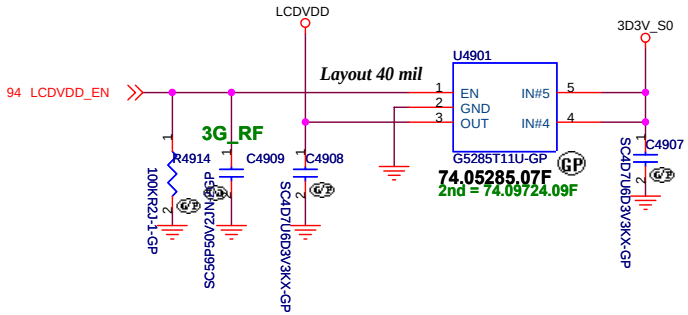


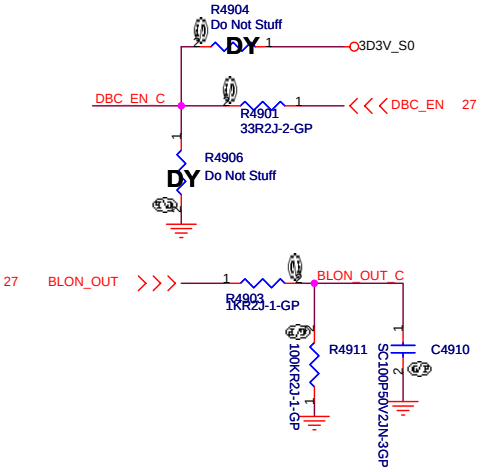
Camera Power



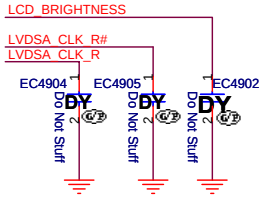
SSID = VIDEO

LCD POWER for ANNIE





For EMI request
Close to LVDS connector

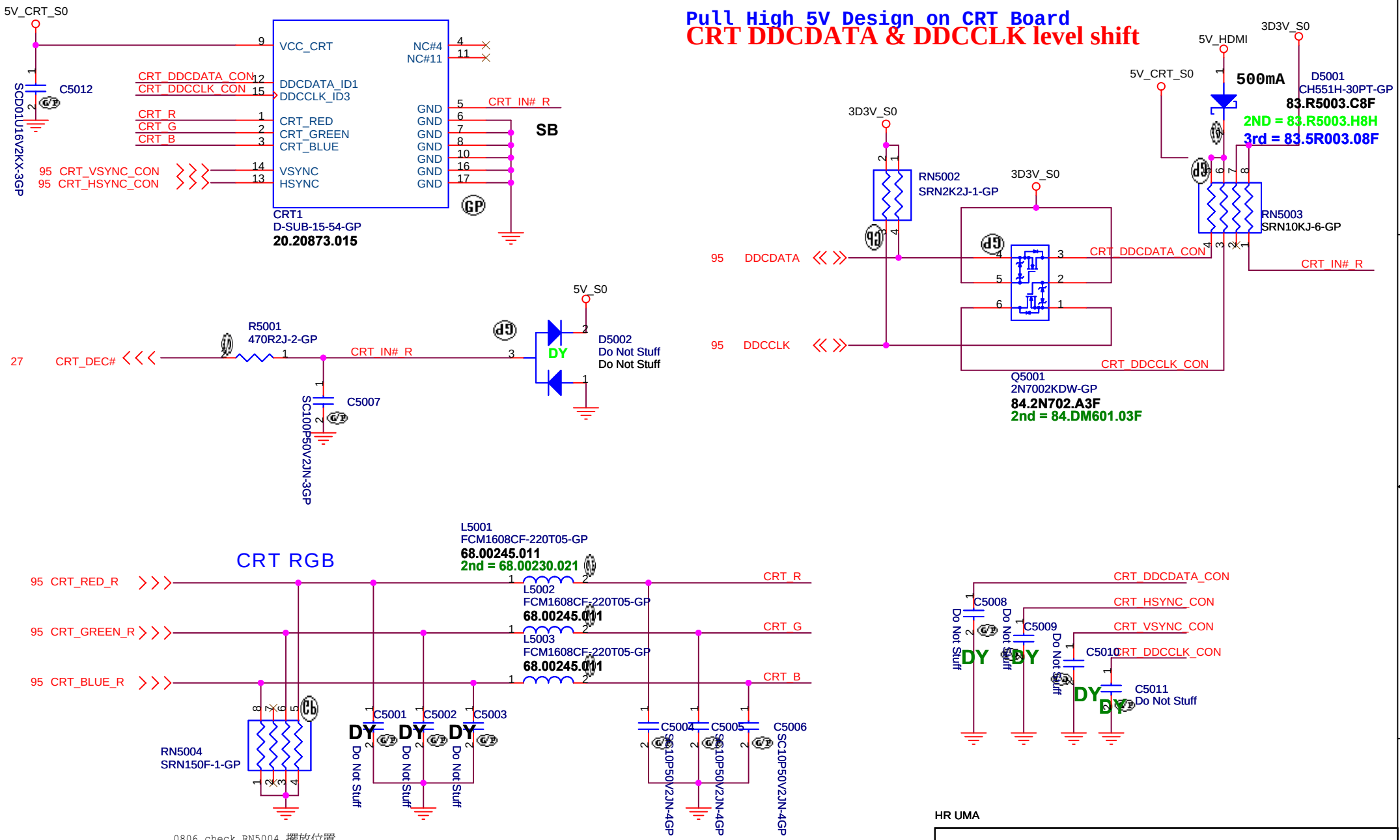


HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD Connector	
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 49 of 102	

Pull High 5V Design on CRT Board
CRT DDCDATA & DDCCLK level shift



0806 check RN5004 擺放位置

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size	Document Number	Rev
A4	JE40-HR	-1

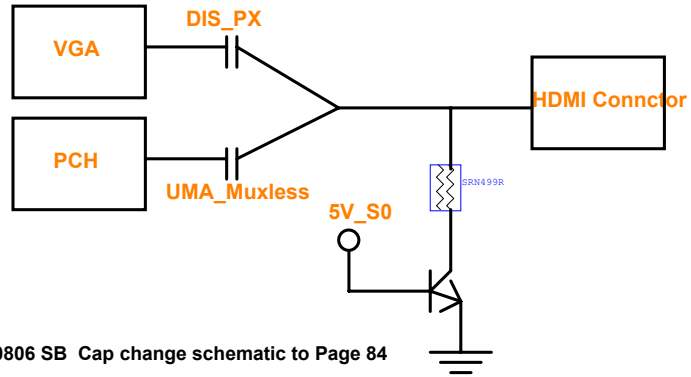
Date: Thursday, December 02, 2010 Sheet 50 of 102

SSID = VIDEO

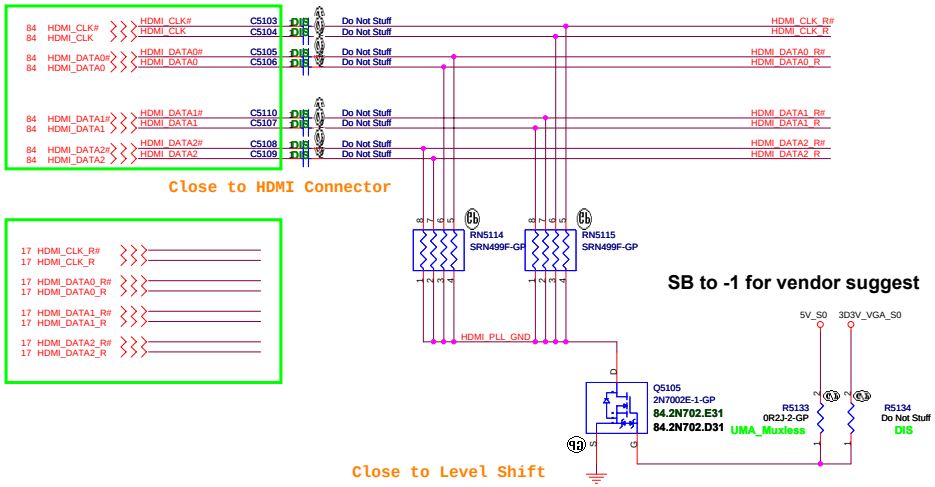
HDMI Level Shifter & CONNECTOR

UMA_Muxless : default setting used PS8101. if don't used PS8101
please change C5103~C5110 to 0 ohm resister

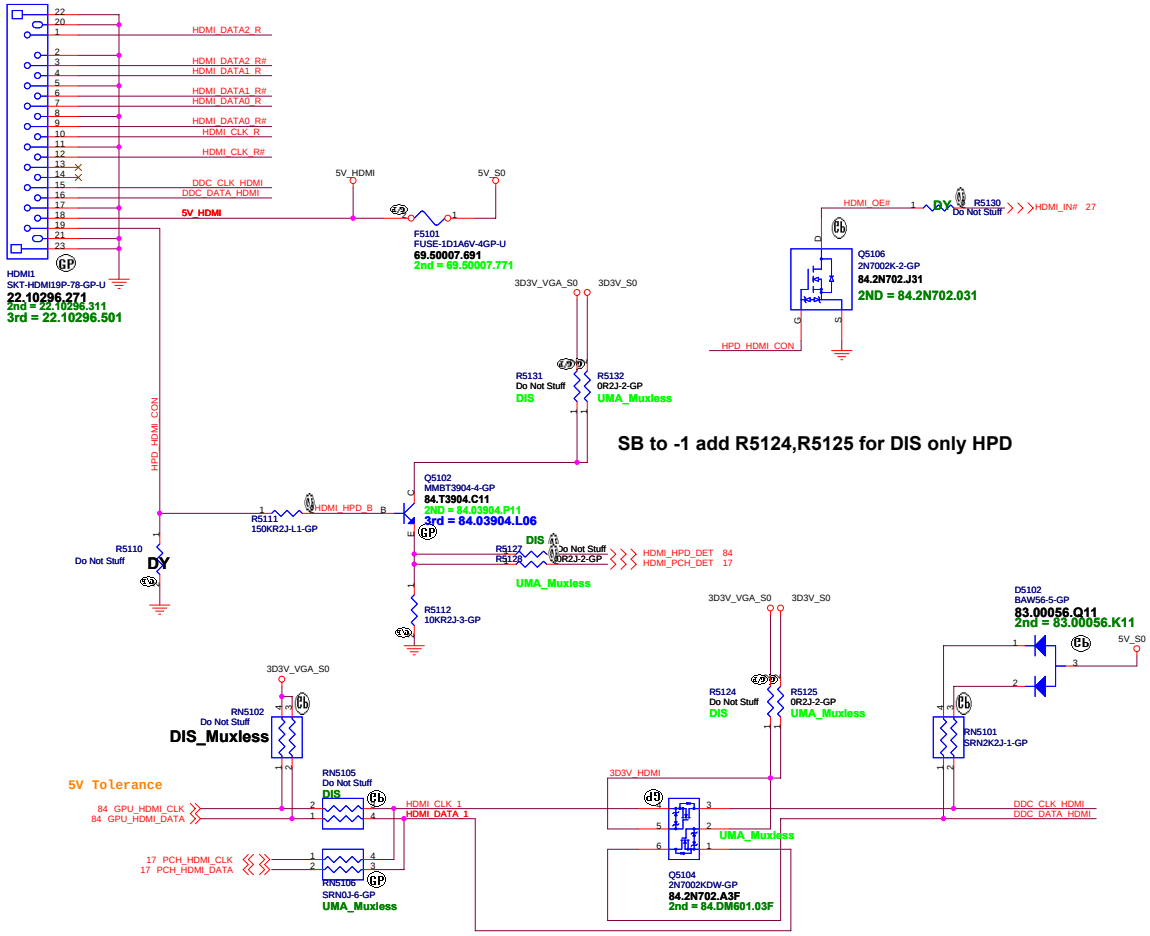
HDMI DISCRETE/ UMA Co-lay



0806 SB Cap change schematic to Page 84



HDMI CONN



HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
Custom	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 51 of 102

LED BACKLIGHT CONVERTER POWER

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *eDP*		
Size: A3	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 52 of 102	

(Blanking)

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	**JE40-HR**	**-1**

Date: Thursday, December 02, 2010 Sheet 53 of 102

(Blanking)

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

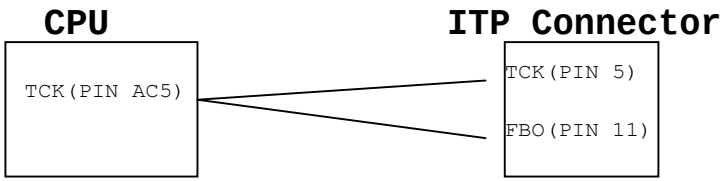
Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 54 of 102

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close ITP connector 500 mil (max), others place near CPU side.



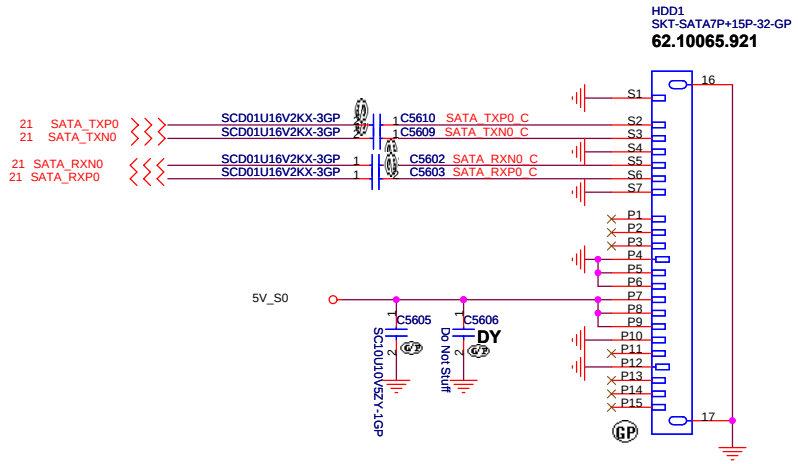
HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

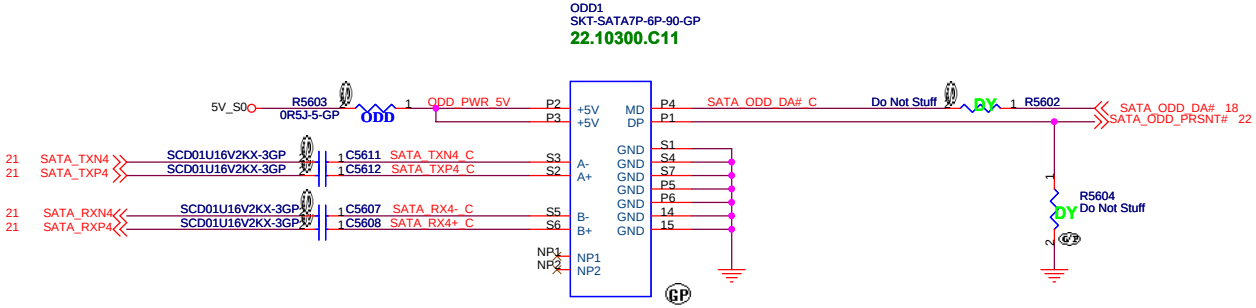
Title: ITP		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 55 of 102	

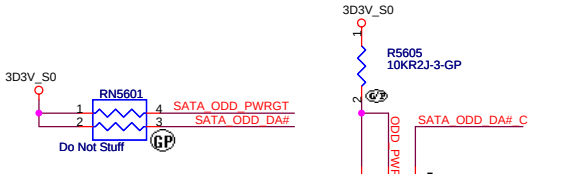
SSID = SATA

SATA HDD Connector



ODD Connector



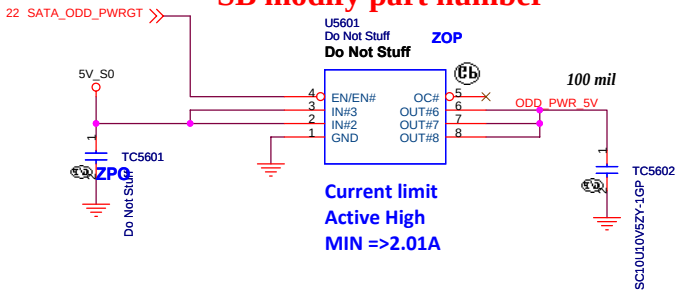


0707 Modify:
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD.

SB

SATA Zero Power ODD

SB modify part number



HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD/ODD		
Size: A3	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 56 of 102	

ESATA Power

USB CHARGER

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *E-SATA/USB CHARGER*

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 57 of 102

SSID = AUDIO

Speaker Connector

LINE1 OUT
SPDIF

JE40 Modify LINE OUT

Audio at small board

MIC IN

Internal
Microphone

JE40 delete Line in function

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Audio Jack*

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 58 of 102

GIGA Lan Transformer

SSID = LOM

LAN MDI Off-Page

XF5901
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B

XF5902
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B

C5901 SCD1U10V2KX-5GP
C5902 SCD1U10V2KX-5GP
C5903 SCD1U10V2KX-5GP
C5904 SCD1U10V2KX-5GP

XRF_TDC1
XRF_TDC2
XRF_TDC3
XRF_TDC4

MDI3+ MDI3- MDI2- MDI2+ MDI1+ MDI1- MDI0- MDI0+

RJ45_7 MCT2 RJ45_8 RJ45_5 MCT1 RJ45_4 RJ45_3 MCT4 RJ45_6 RJ45_2 MCT3 RJ45_1

1CT:1CT
Tx Side
Rx Side

C5916 C5917 C5918 C5919 DY Do Not Stuff

EC5910 EC5909 EC5903 EC5904 EC5905 EC5906 EC5908 EC5907 SCD28P50V2CN-GP

C5907 C5906 DY Do Not Stuff

LAN_ACT_LED#
10M/100M/1G_LED#

SB modiyf Pin9 Pin10 SWAP

RJ45
RJ45-12P-16-GP
22.10321.Y21
2nd = 22.10321.Y91

LED COLOR
10(+) 9(-)::GREEN
12(+) 13(-)::ORANGE

31 10M/100M/1G_LED#
31 LAN_ACT_LED#

RN5901 SRN470J-4-GP-U
3D3V_S5
CONN_PWR2
CONN_PWR

EC5901 EC5902 DY Do Not Stuff

SB modify For EMI

U5901 U5902 U5903 U5904
TVLST2304AD0-GP
SURGE

5V_S5

31 MDI1+
31 MDI1-
31 MDI0+
31 MDI0-
31 MDI3+
31 MDI3-
31 MDI2+
31 MDI2-

GDT1 GDT2 GDT3 GDT4
BSB063X2X2312T23-GP
SURGE

MCT1 MCT2 MCT3 MCT4

R5903 R5901 R5902 R5904 75R3J-L-GP
MCT_R
C5905 SC1KP2KV6KX-GP

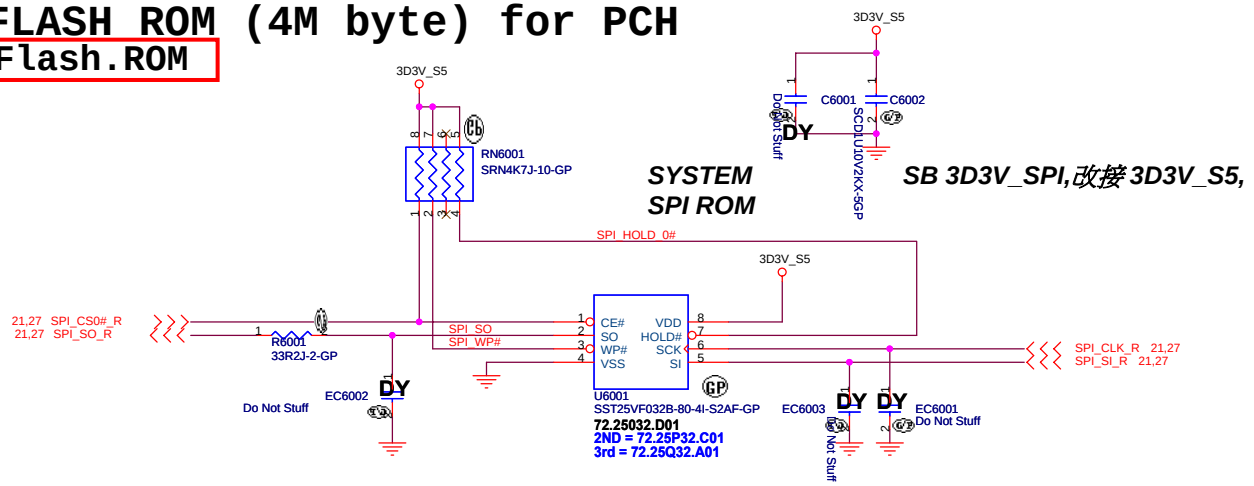
HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONNECTOR
Size: Custom
Document Number: JE40-HR
Rev: -1
Date: Thursday, December 02, 2010
Sheet 59 of 102

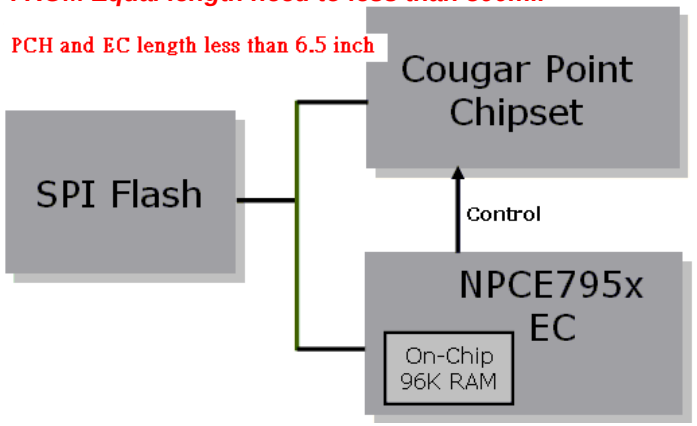
SPI FLASH ROM (4M byte) for PCH

SSID = Flash.ROM

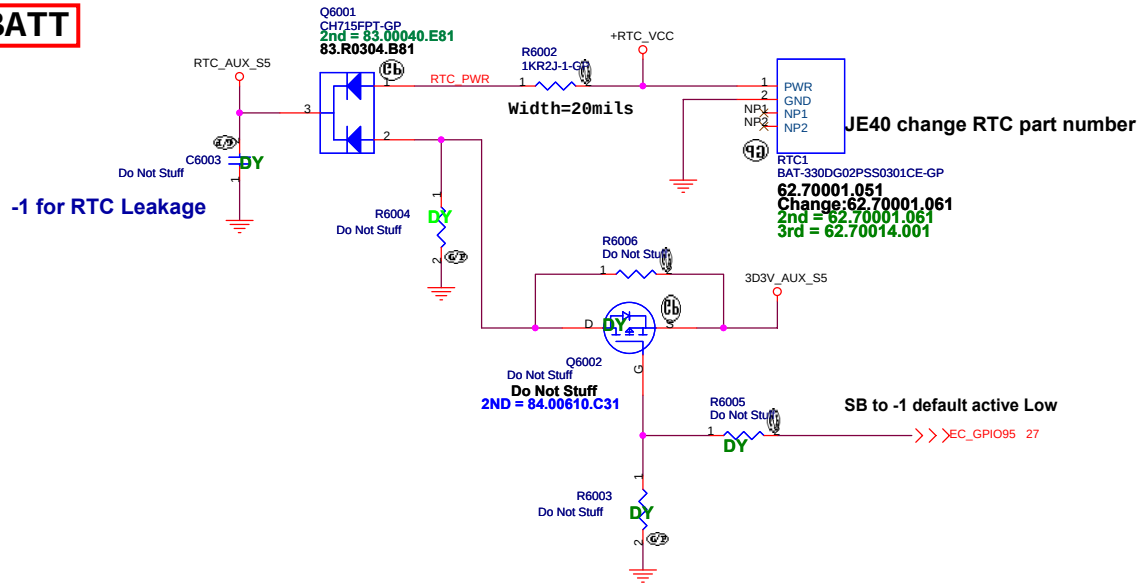


SPI ROM Equal length need to less than 500mil

PCH and EC length less than 6.5 inch



SSID = RBATT

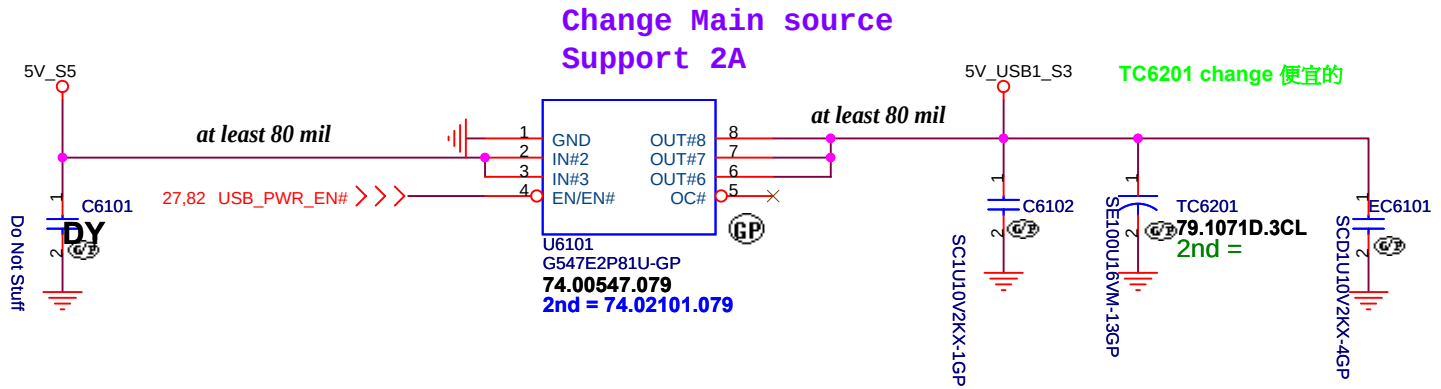


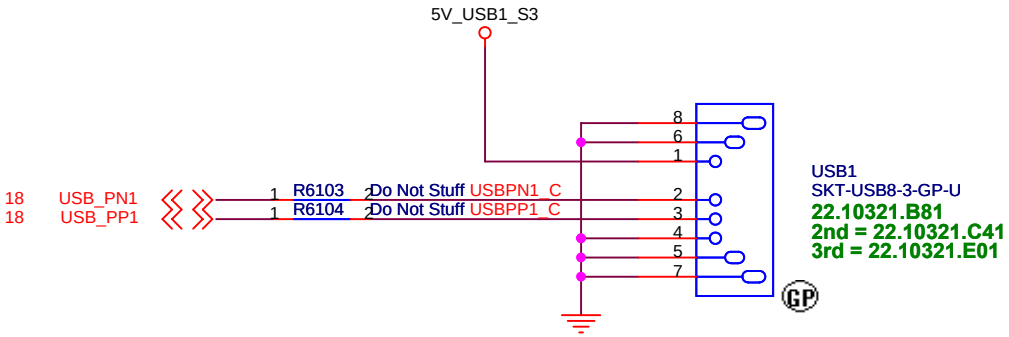
HR UMA

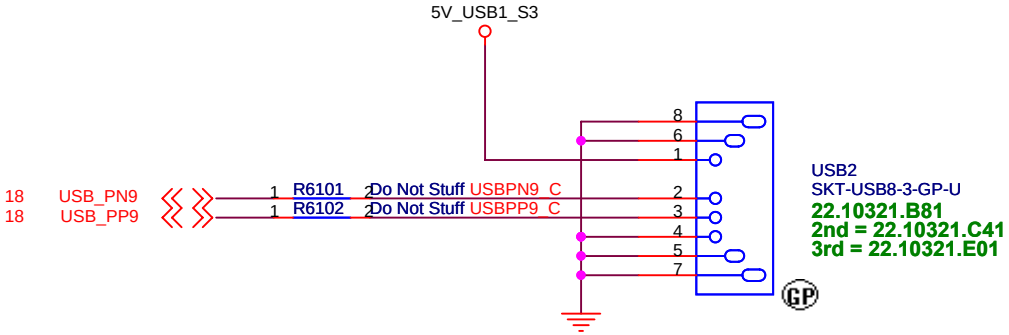
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Flash/RTC*		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 60 of 102	

SSID = USB

IO Board USB Power







HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 61 of 102

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0 Port***

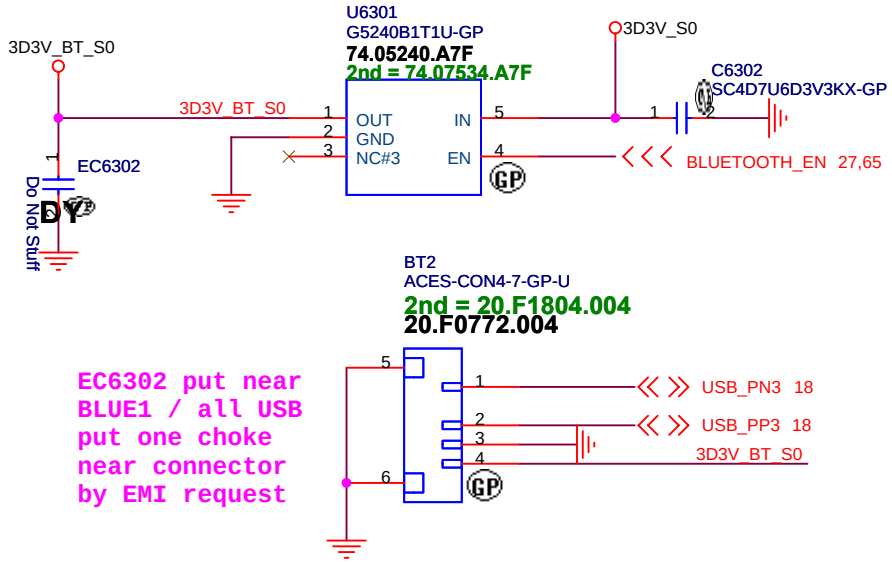
Size	Document Number	Rev
A3	**JE40-HR**	-1

Date: Thursday, December 02, 2010 Sheet 62 of 102

SSID = User.Interface

Bluetooth Module conn.

ANNIE Bluetooth Module

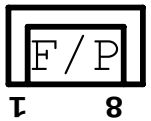


HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Bluetooth***		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 63 of 102	

Finger printer

JE40 delete FP function

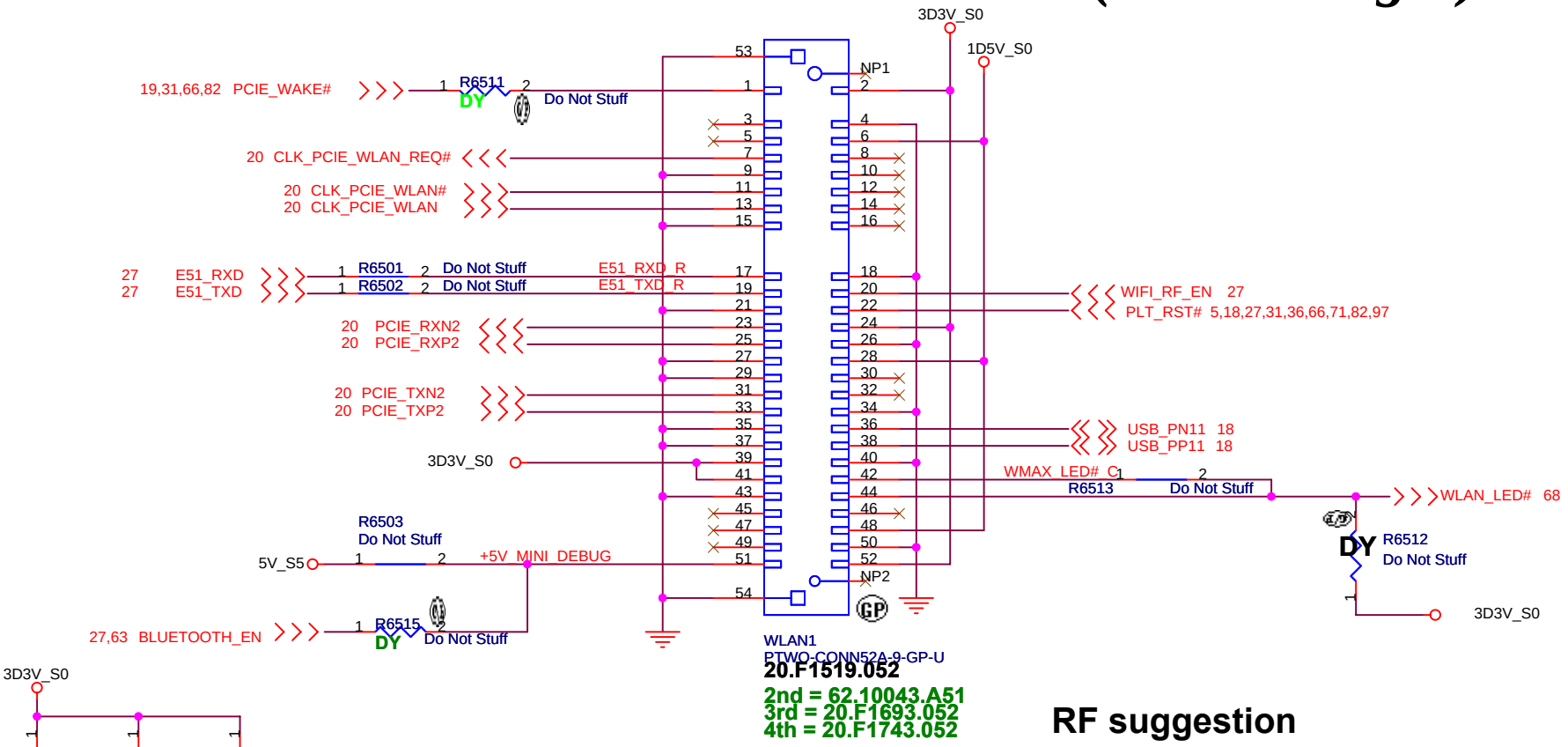


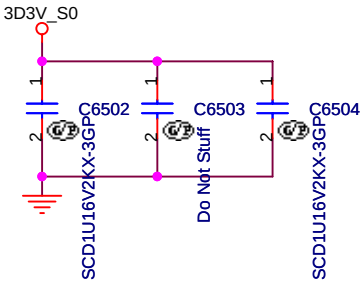
HR UMA

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 64 of 102	

SSID = Wireless

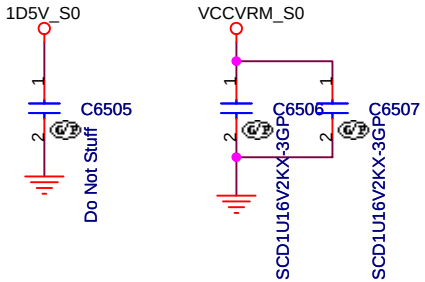
Mini Card Connector(802.11a/b/g/n)

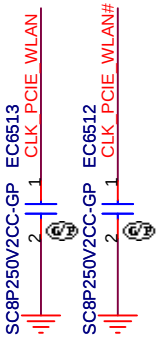




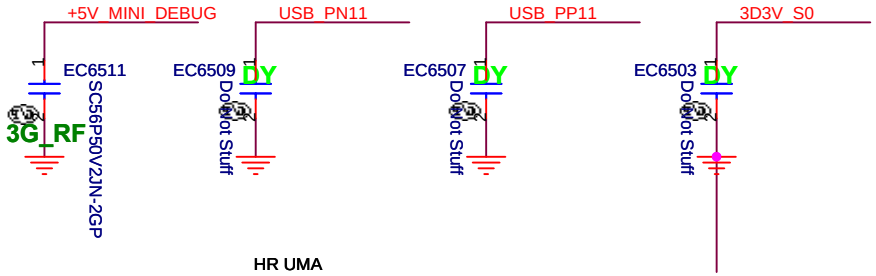
SB modify for SIV

-2





RF suggestion



HR UMA

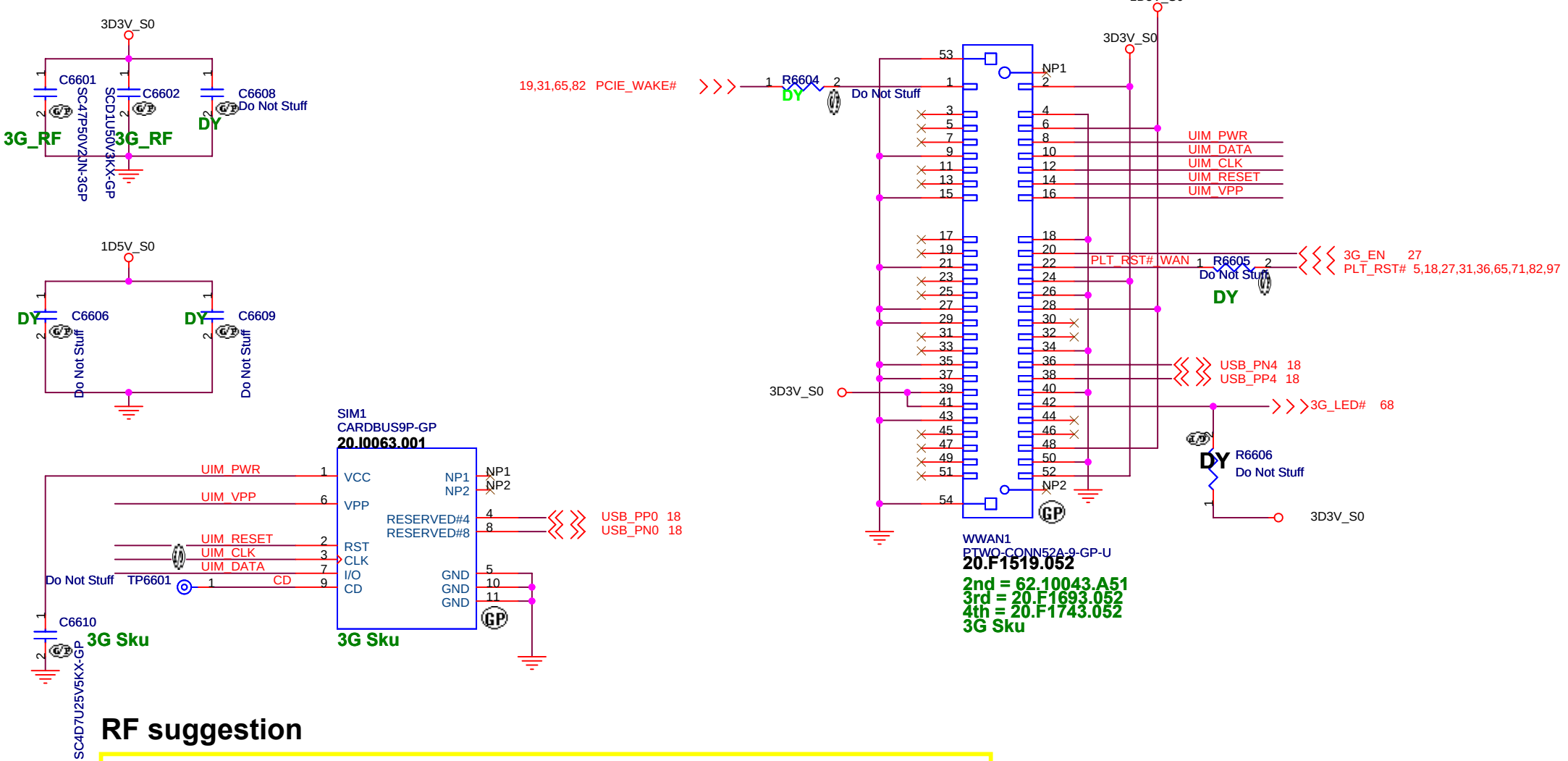
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINICARD(WLAN)/ITP CONN		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 65 of 102	

SSID = Wireless

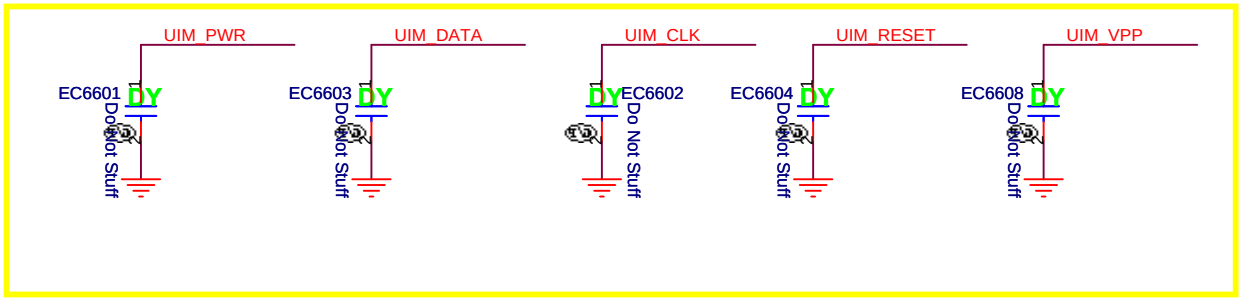
Mini Card Connector(WWAN)

20100712 V1.5

Place near MINI Card CONN



RF suggestion



HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **WWAN Connector**		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 66 of 102	

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HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

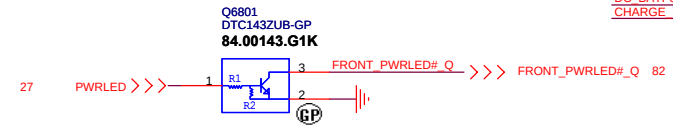
Title: ***Reserved***

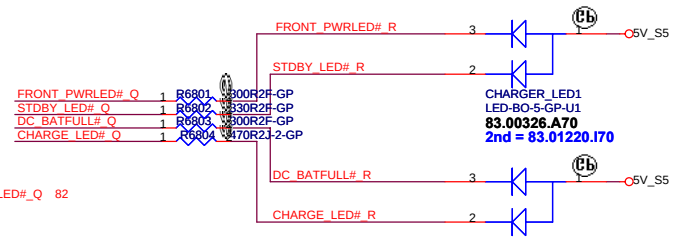
Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 67 of 102

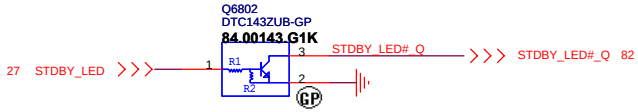
SSID = User.Interface

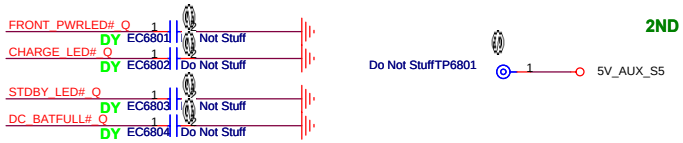
Power button LED





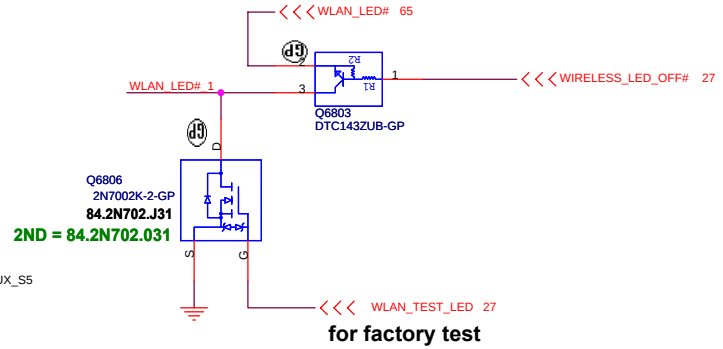
Power STDBY_LED





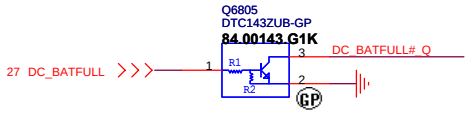
WLAN_LED

From module

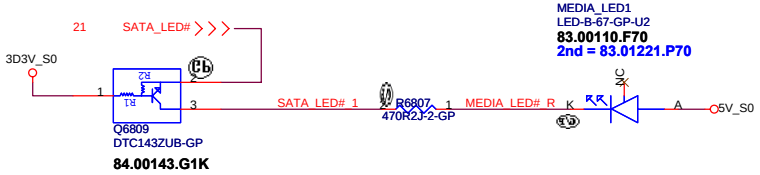


for factory test

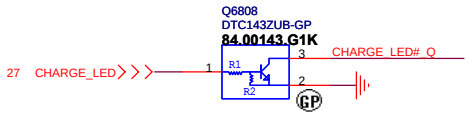
Battery LED2(DC_BATFULL)

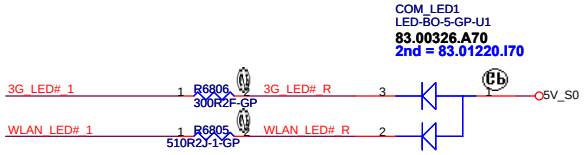


SATA HDD LED



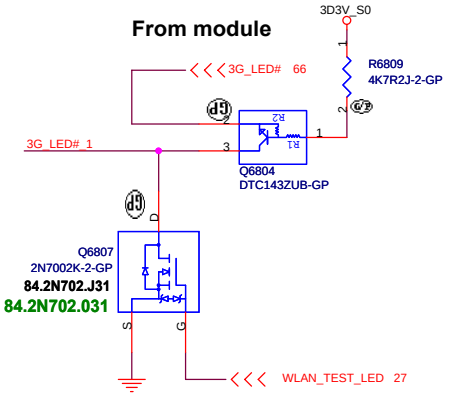
Battery LED1(CHARGE)





3G LED

From module



for factory test

HR UMA

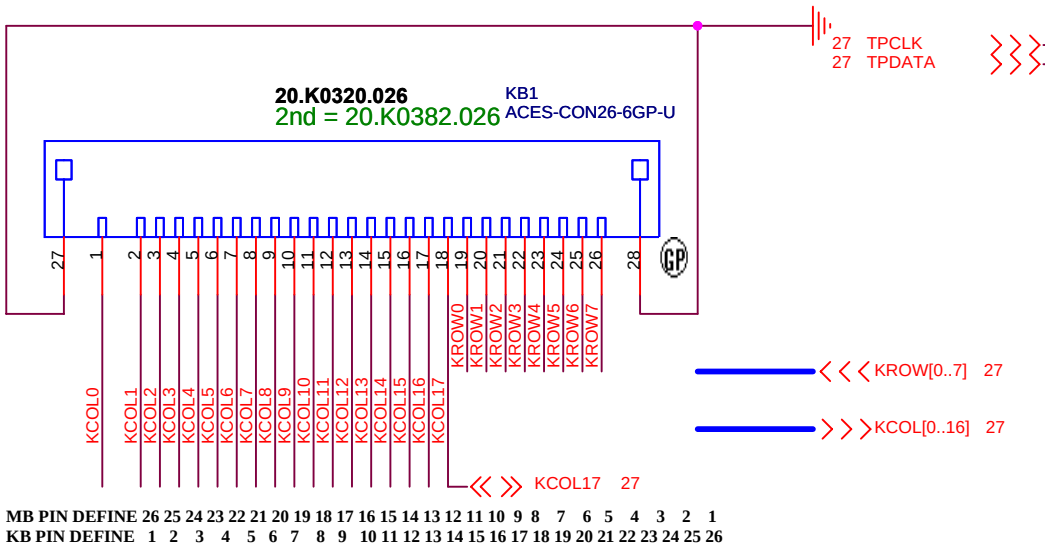
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LED Bard/Power Button		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 68 of 102	

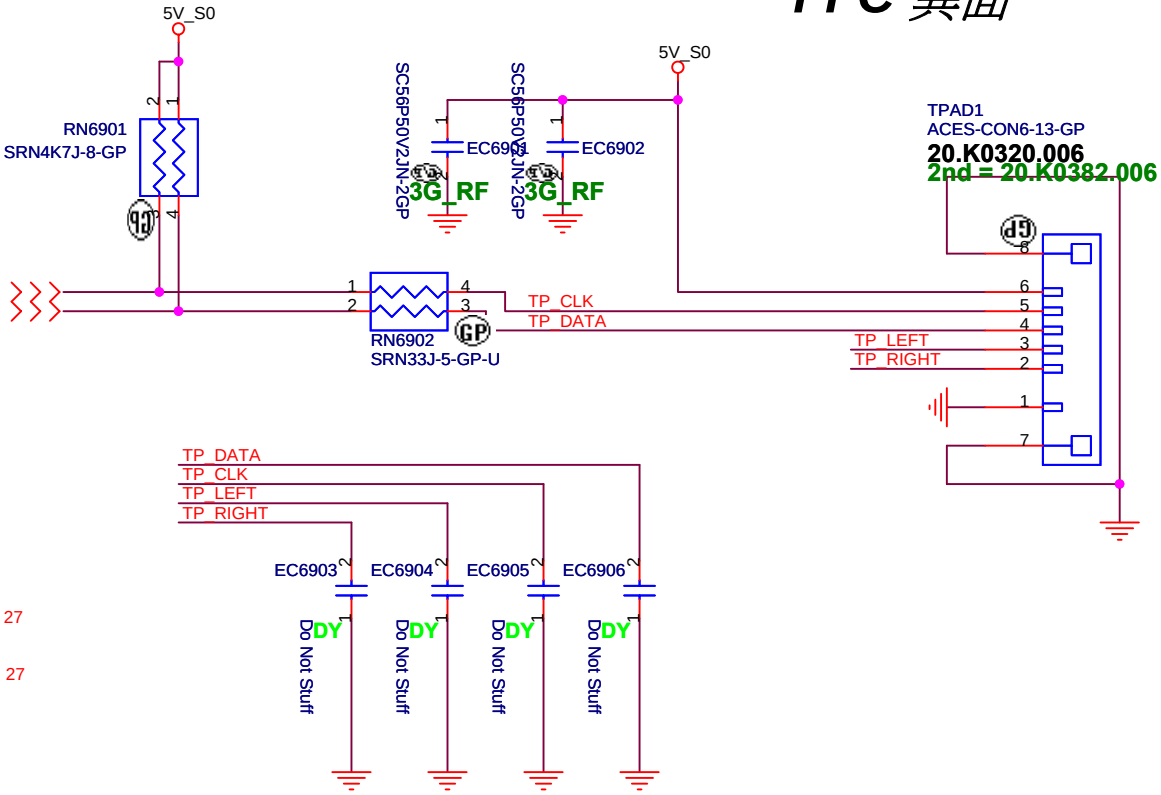
SSID = KBC

TOUCH PAD

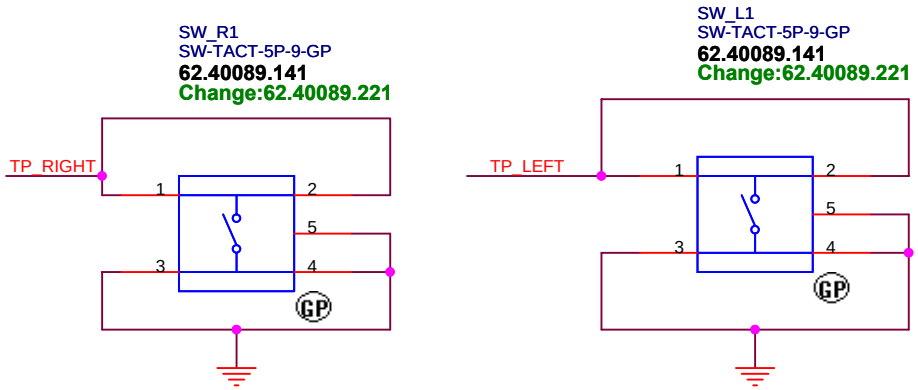
FFC 異面

Internal KeyBoard Connector





26 K/B 1 **SB to -1 modify Part number**



HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Key Board/Touch Pad***

Size	Document Number	Rev
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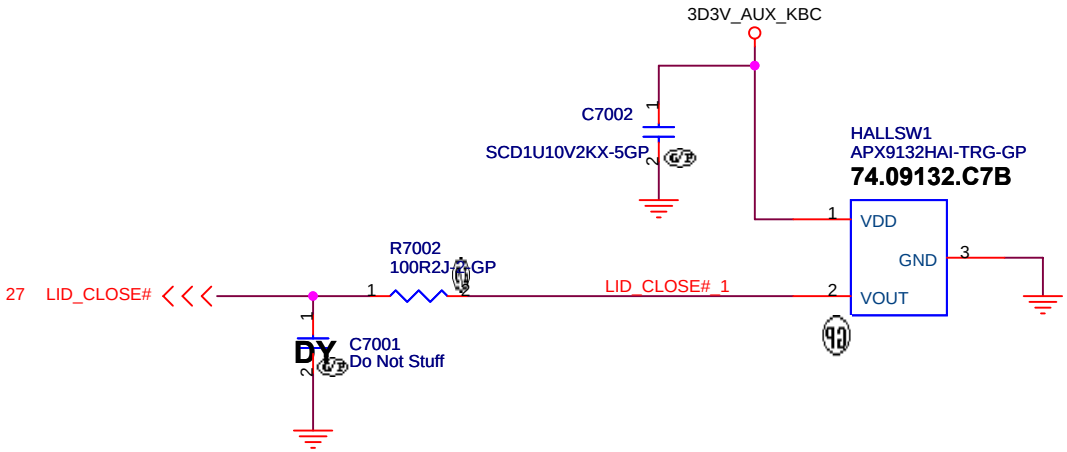
Date: Thursday, December 02, 2010 Sheet 69 of 102



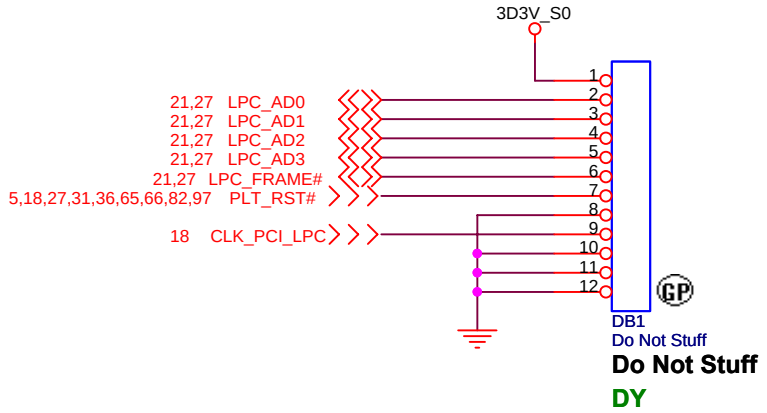
HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	**JE40-HR**	**-1**

Date: Thursday, December 02, 2010 Sheet 70 of 102



HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	**JE40-HR**	**-1**

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HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	JE40-HR	-1

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HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

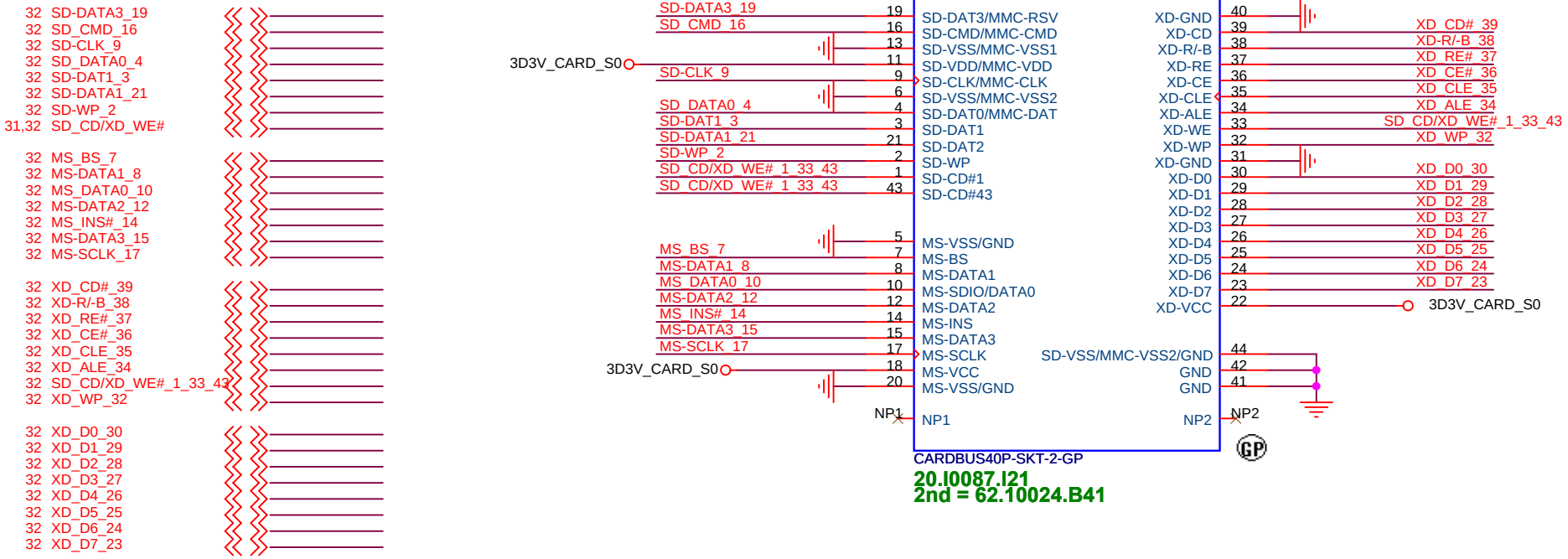
Title: ***Reserved***

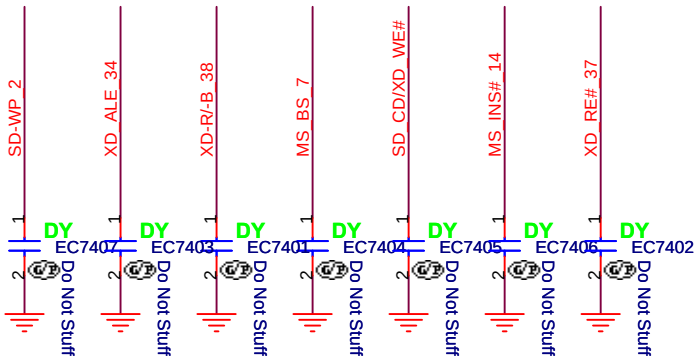
Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 73 of 102

SD/XD/MS Card Reader

SSID = SDIO





HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD Reader CONN**

Size	Document Number	Rev
A4	JE40-HR	-1

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SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *New Card*

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 75 of 102

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HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

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HR UMA

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Reserved***		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 77 of 102	

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HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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Date: Thursday, December 02, 2010 Sheet 78 of 102

SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

JE40 delete G Sensor Function

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Free Fall Sensor*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 79 of 102	

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HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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Date: Thursday, December 02, 2010 Sheet 80 of 102

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HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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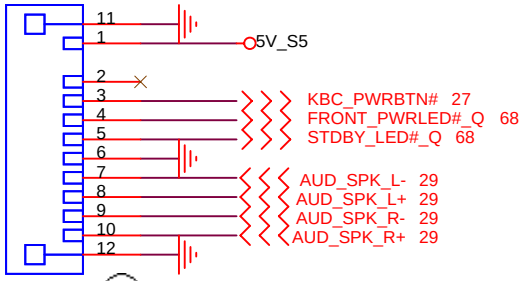
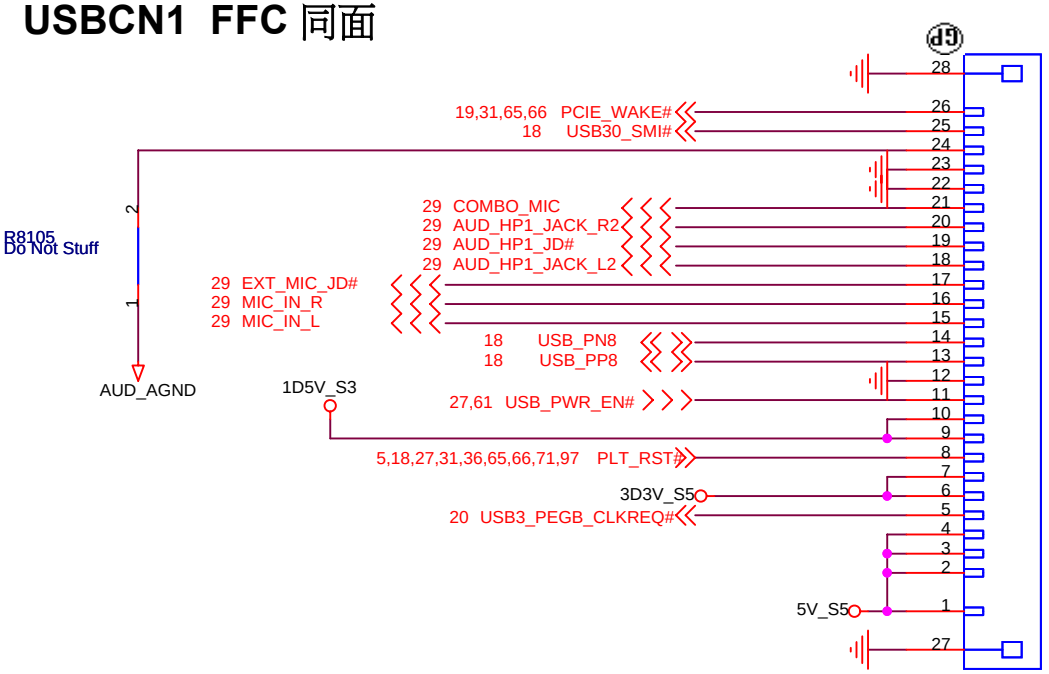
PWRCN1 FFC 異面



PWRCN1
ACES-CON10-20-GP
20.K0422.010
2nd = 20.K0382.010

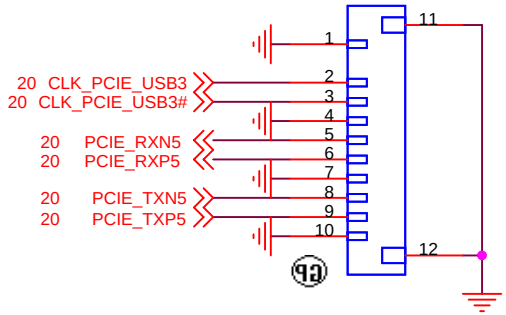
USBCN1 FFC 同面



USBCN1
ACES-CON26-11-GP
20.K0315.026
2nd = 20.K0370.026

0806 change 10Pin

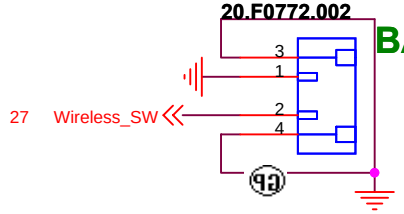
USBCN2
ACES-CON10-18-GP
20.K0315.010
2nd = 20.K0392.010



USBCN2 FFC 同面

-1 add RF connector
BAE40 Only

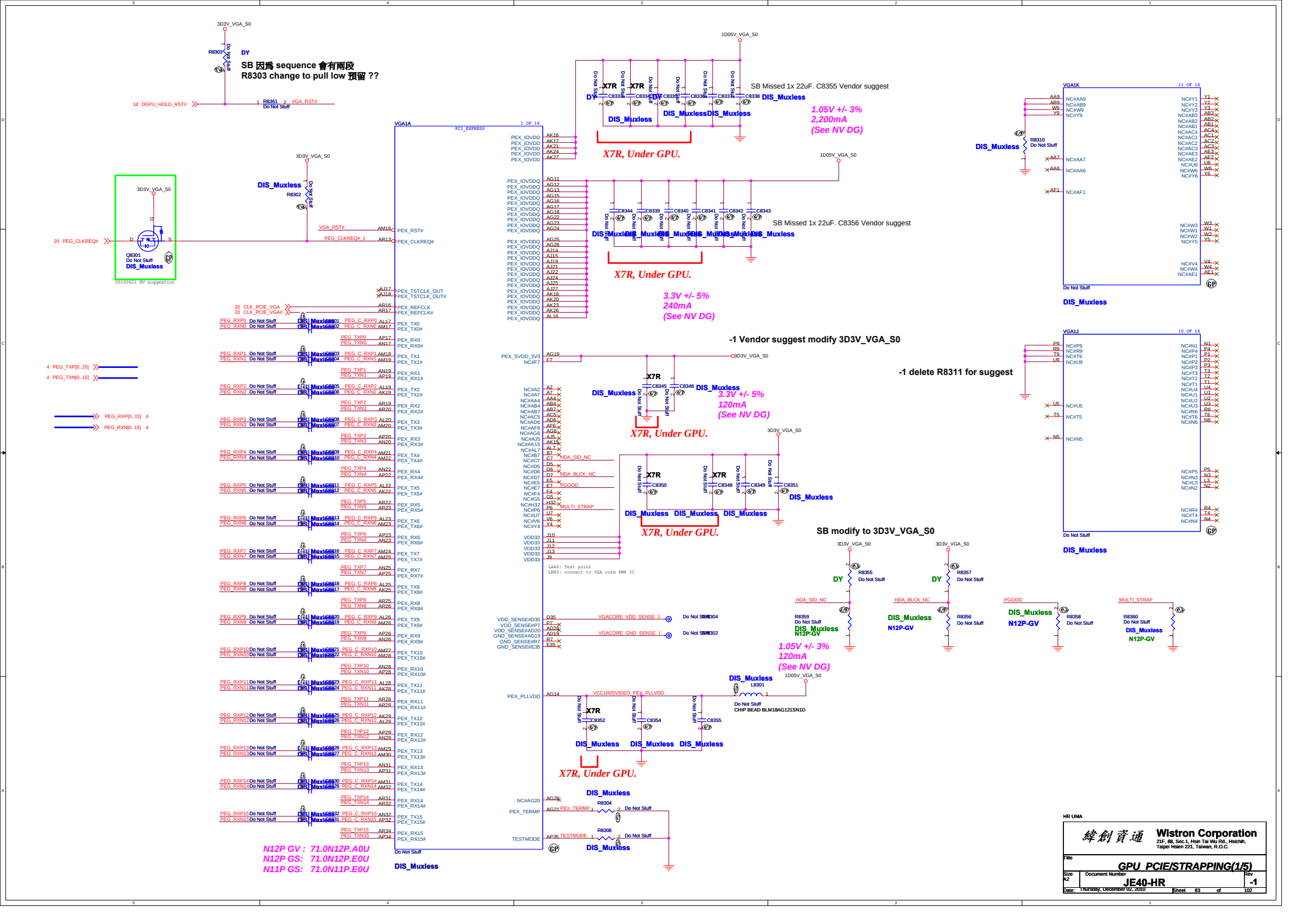
RF_CN1
ACES-CON2-11-GP
20.F0772.002



Cabele Wire to BD

HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***IO Board Connector***		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 82 of 102	


SB 因爲 sequence 會有兩段
R8303 change to pull low 預留 ??
SB Missed 1x 22uF. C8355 Vendor suggest
1.05V +/- 3%
2,200mA
(See NV DG)
X7R, Under GPU.
SB Missed 1x 22uF. C8356 Vendor suggest
3.3V +/- 5%
240mA
(See NV DG)
-1 Vendor suggest modify 3D3V_VGA_S0
3.3V +/- 5%
120mA
(See NV DG)
-1 delete R8311 for suggest
SB modify to 3D3V_VGA_S0
1.05V +/- 3%
120mA
(See NV DG)
N12P GV : 71.0N12P.A0U
N12P GS: 71.0N12P.E0U
N11P GS: 71.0N11P.E0U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
GPU_PCIE/STRAPPING(1/5)
JE40-HR
-1
Thursday, December 02, 2010
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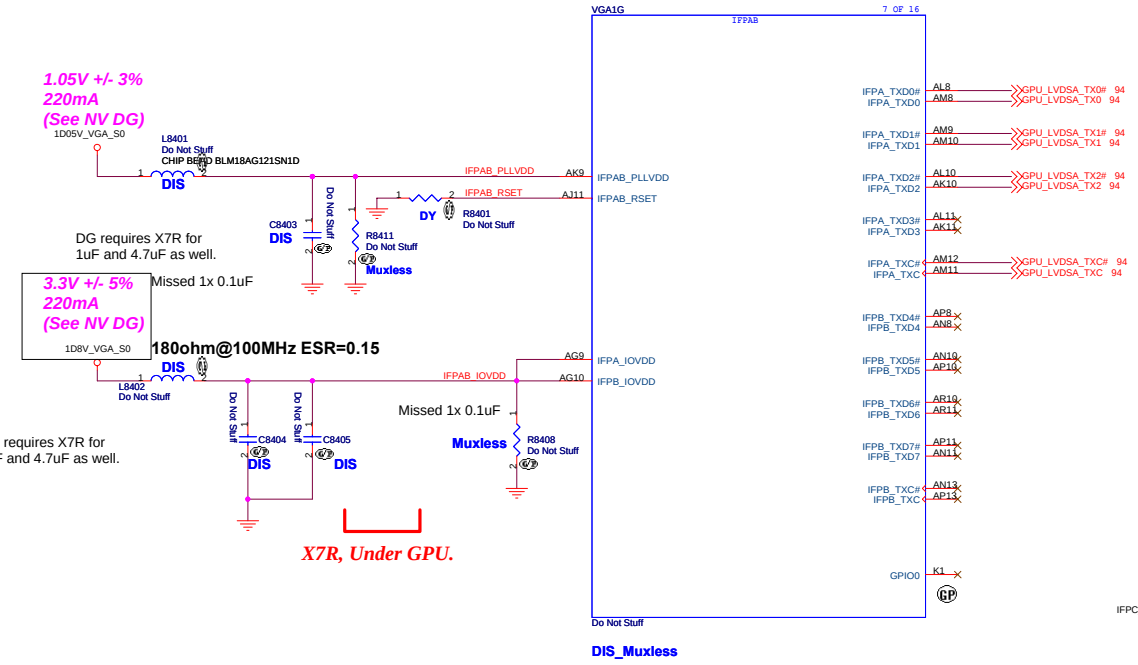
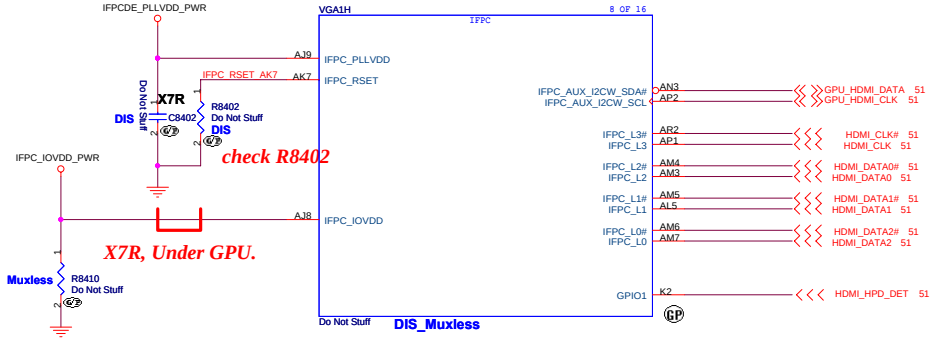
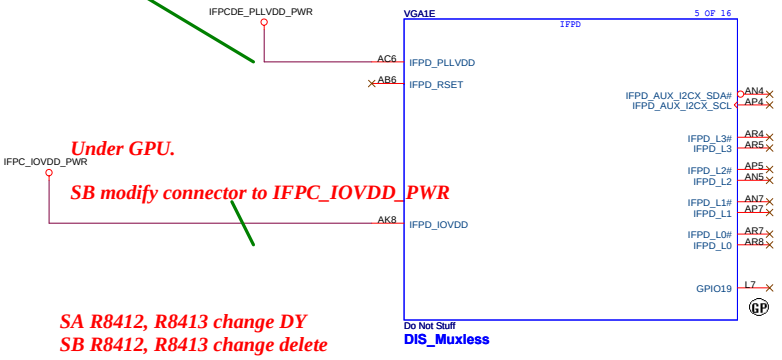
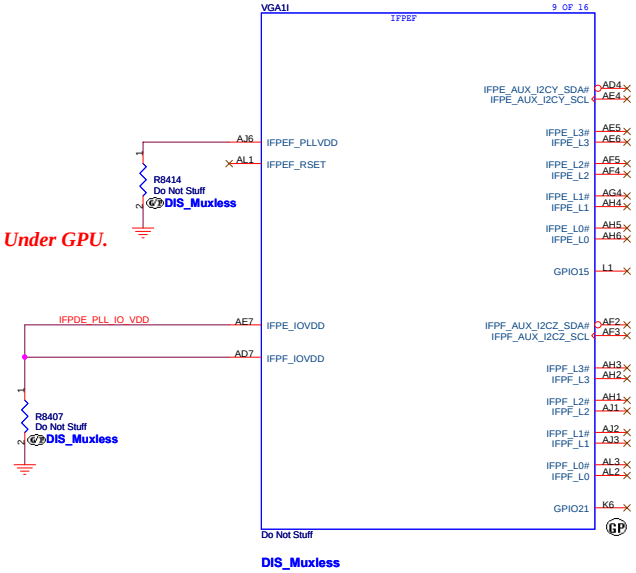
LVDS Interface

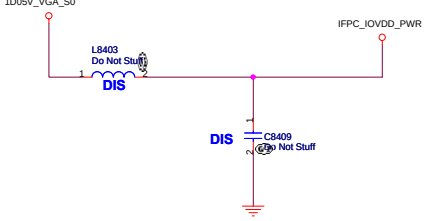


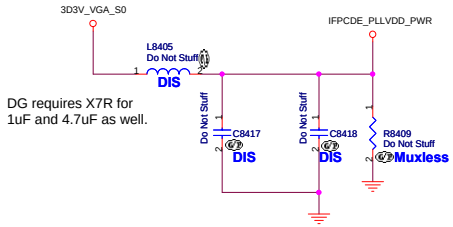






HDMI Interface





HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 84 of 102

EDP 10A

DC tolerance +/- 75mV
AC tolerance +/- 50mV < 100MHz

X7R, Under GPU.

X7R, Near GPU.

1.05V +/- 3%
200mA
(See NV DG)

X7R, Under GPU.

FBCLK Termination place on VRAM side

FBCLK Termination place on VRAM side

Group A

Group B

HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

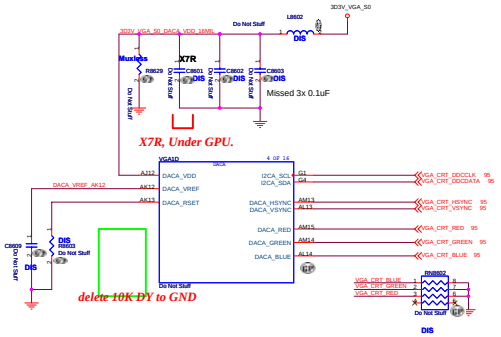
Title: **GPU_DP/LVDS/CRT/GPIO(3/5)**

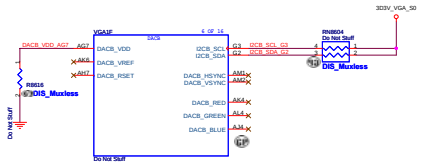
Size: Custom | Document Number: **JE40-HR** | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 85 of 102

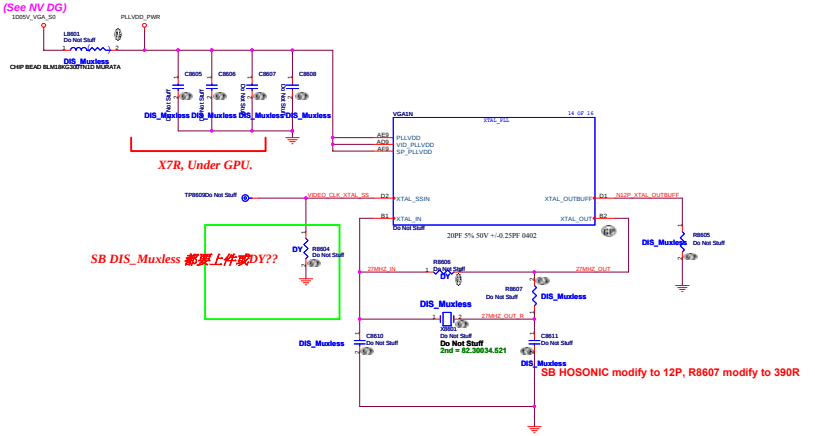
300ohm@100MHz ESR=0.25ohm

3.3V +/- 5%
120mA
(See NV DG)

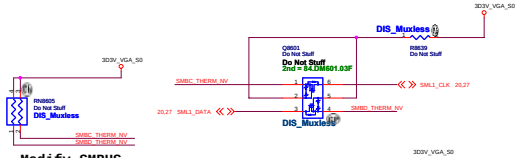


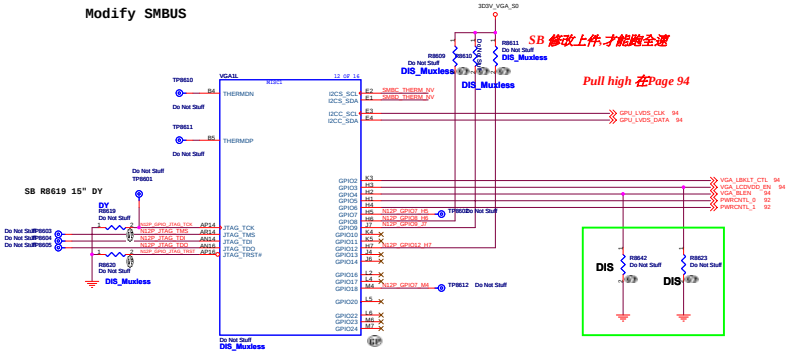


1.05V +/- 3%
150mA
(See NV DG)



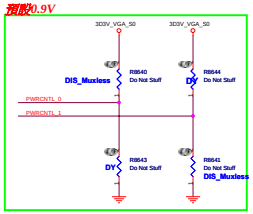
VGA Thermal sensor P2800





SJM50-CP SUPPORT							
P-STATE	NVVDD_ALT_V1	NVVDD_ALT_V0	N11M-GE1	N11M-GE2	N11M-OP1	N11P-GE1	N11P-GE Fermi
P12	0	0	0.85V	0.85V	0.85V	0.85V	0.85V
P8	0	1	0.85V	0.85V	0.85V	0.85V	0.9V
P0	1	0	1.03V	1.03V	1.03V	0.95V	0.95V

預設0.9V



NVIDIA TABLE

	Hynix 2G 0110 128*16*8 800MHZ	Hynix 1G 0000 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 512 64*16*4 800MHZ	Samsung 2G 0111 128*16*8 800MHZ
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	5Kohm 64.49915.6DL	20Kohm 64.20025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL

GPU_ROM_SI

for 1Gbit Hynix VRAM	for 2Gbit Hynix VRAM	for 1Gbit Samsung VRAM	for 2Gbit Samsung VRAM
RAM_CFG[0]=0	RAM_CFG[0]=0	RAM_CFG[0]=1	RAM_CFG[0]=1
RAM_CFG[1]=1	RAM_CFG[1]=1	RAM_CFG[1]=1	RAM_CFG[1]=1
RAM_CFG[2]=0	RAM_CFG[2]=1	RAM_CFG[2]=0	RAM_CFG[2]=1
RAM_CFG[3]=0	RAM_CFG[3]=0	RAM_CFG[3]=0	RAM_CFG[3]=0

GPU_ROM_SO

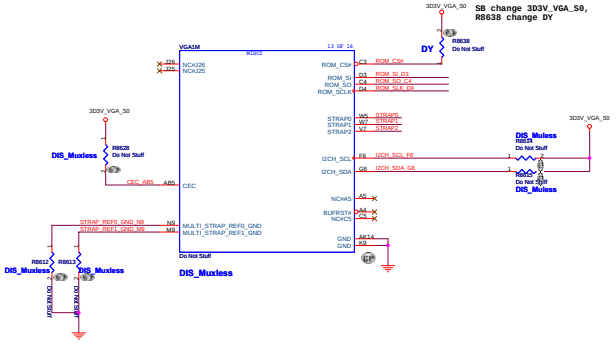
VGA_DEVICE =1 (low bit)
SMB_ALT_ADDR =0
FB_0_BAR_SIZE =0
XCLK_417 =0 (High bit)

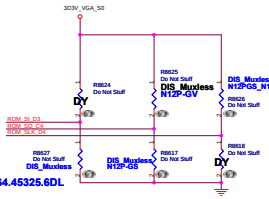
GPU_ROM_SCLK

PEX_PLL_EN_TERM =0
SLOT_CLK_CFG =1
SUB_VENDOR =0
PCI_DEVID[4] =1 N11P Fermi QS 1

Logical Strap Bit Mapping

Resistor	Pull-up	Pull-down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111





Hy2G_64.34825.6DL,Hy1G_64.15025.6DL,Sam1G512M_64.20025.6DL,Sam2G_64.45325.6DL

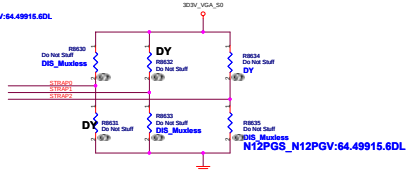


TABLE NVIDIA 71.0N12P.E0U

-1 modify N12P GV setting
71.0N12P.A0U

	N12P-GS DEV ID: 0x0DF4	N12P-GV DEV ID: 0x1050	N11P-GE Fermi DEV ID: 0x0DF1 (0001)	N11P-GS Fermi DEV ID: 0x0DF0 (0000)	N12P-GE DEV ID: 0x0DF5 (0101)
STRAP2 PU	25Kohm 64.24925.6DL	45Kohm ES 45K QS 5K 64.49915.6DL	10Kohm 63.10334.1DL	5Kohm 64.49915.6DL	30Kohm 64.30025.6DL

STRAP0 USER[0]=1 USER[1]=1 USER[2]=1 USER[3]=1 — N12P-GS — N12P-GV — N11P-GE Pull Low — N11P-GS Pull Low — N12P-GE

USE 1111 (45K)

STRAP1 3GIO_PADCFG[0]=0 3GIO_PADCFG[1]=1 3GIO_PADCFG[2]=1 3GIO_PADCFG[3]=1 — 0 1 1 0

USE 0110 (35K)

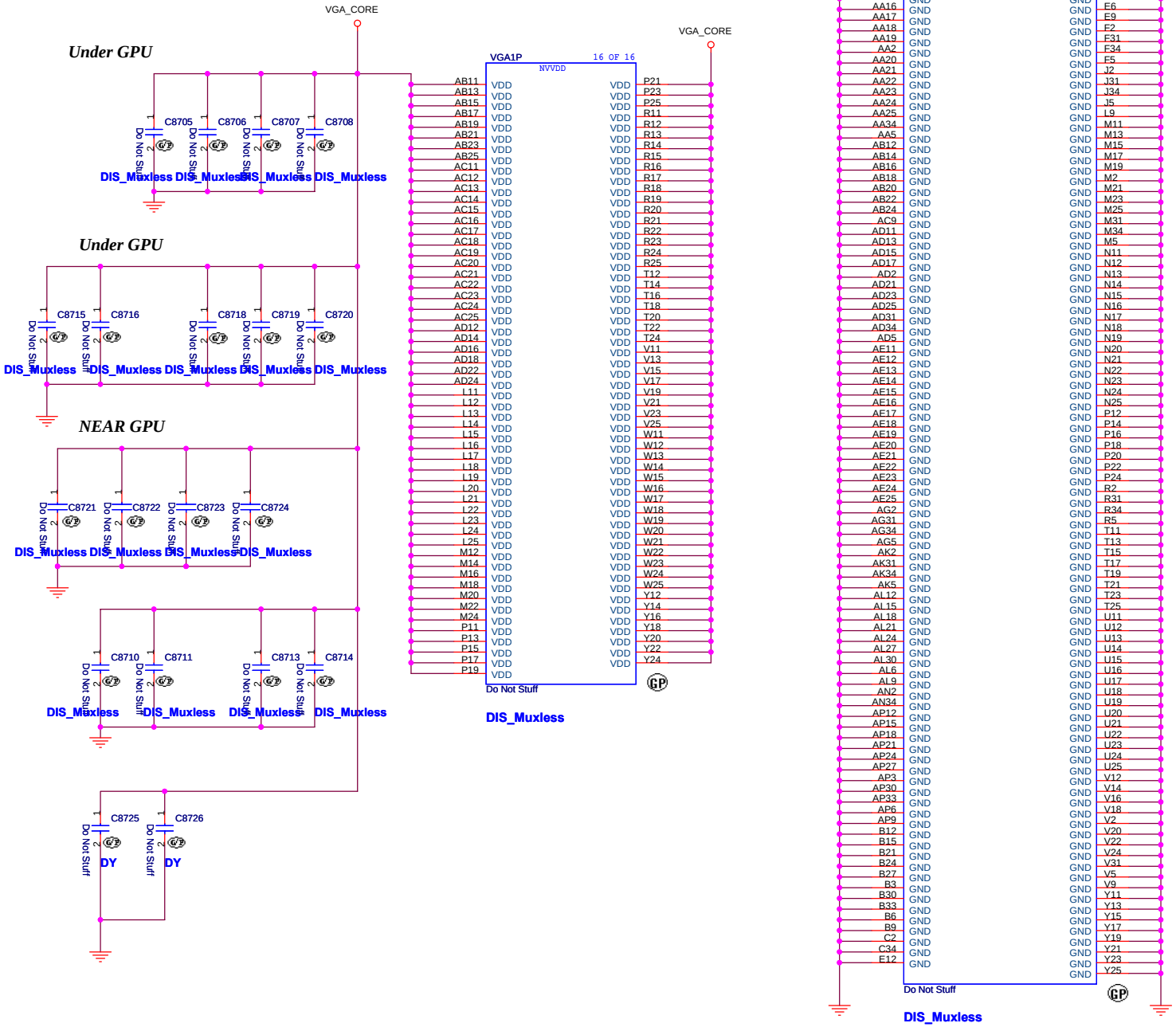
STRAP2
PCI_DEVID[0]=1 N12P-GS GF108-730-A1 0x0DF4 (0X4) (0100)
PCI_DEVID[1]=0 N12P-GV1 GF108-705-A1 0x0DF7 (0X7) (0111)
PCI_DEVID[2]=0 N11P-GS Fermi 0x0DF0 (0000)
PCI_DEVID[3]=0 N11P-GE Fermi 0x0DF1 (0001)

HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

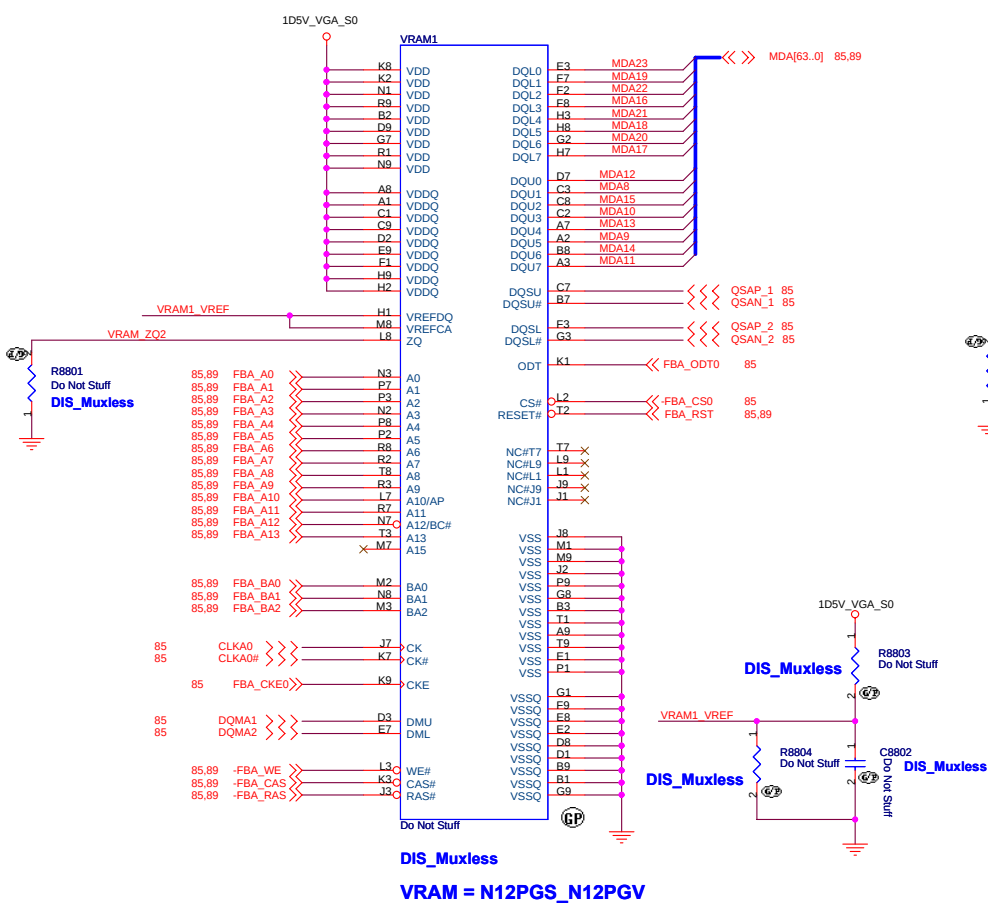
Title: GPU_POWER(4/5)
Size: A1 | Document Number: JE40-HR | Rev: -1
Date: Thursday, December 02, 2010 | Sheet 85 of 102

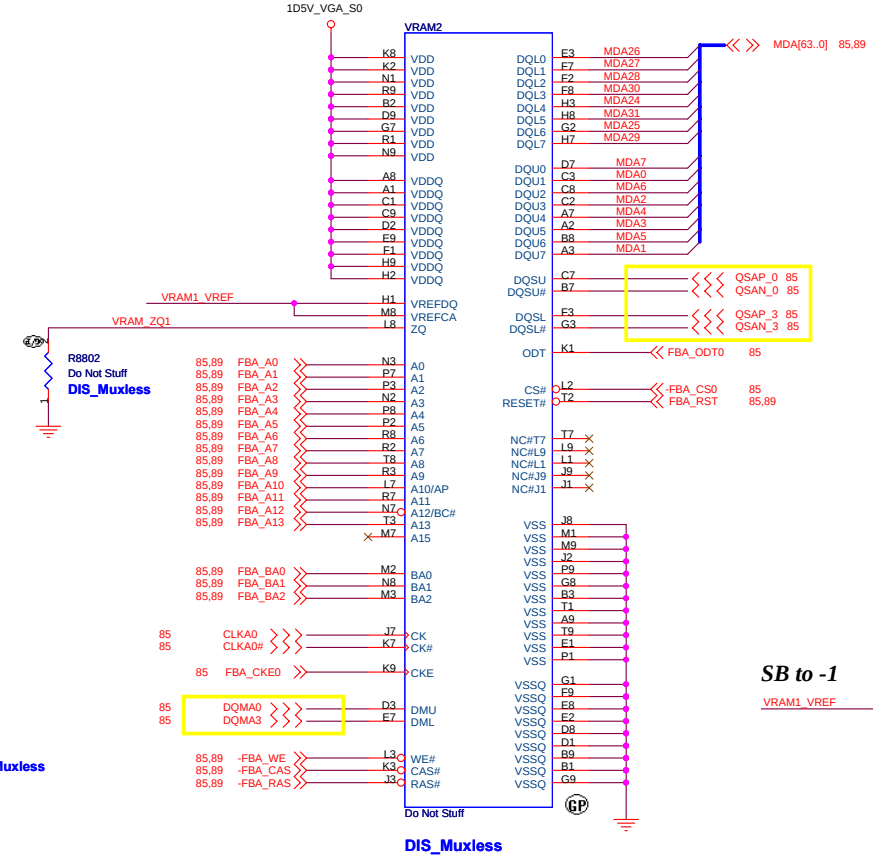
EDP 50A
(TDP 37W)

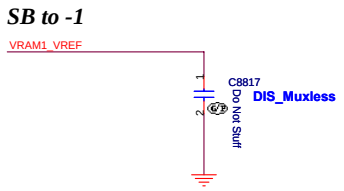


HR UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GPU_DPPWR/GND(5/5)***	
Size A3	Document Number **JE40-HR**	Rev **-1**
Date: Thursday, December 02, 2010	Sheet 87 of 102	

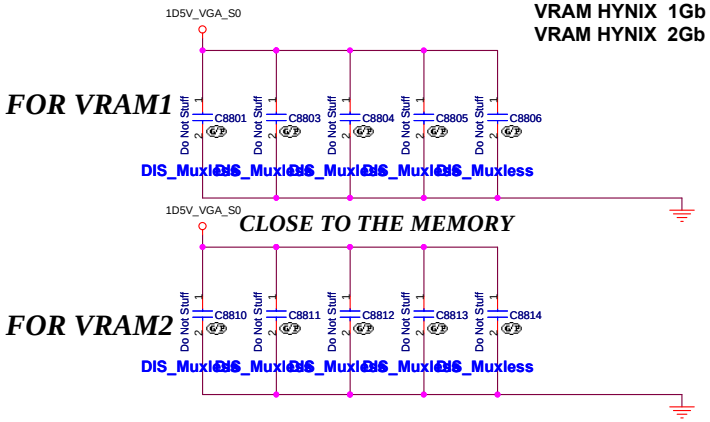


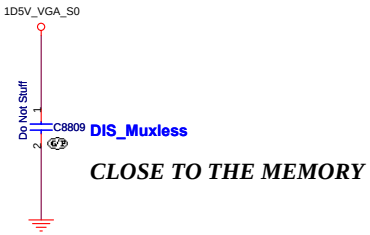




VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001

DG requires 4x0.1uF and 8x1.0uF per VRAM chip





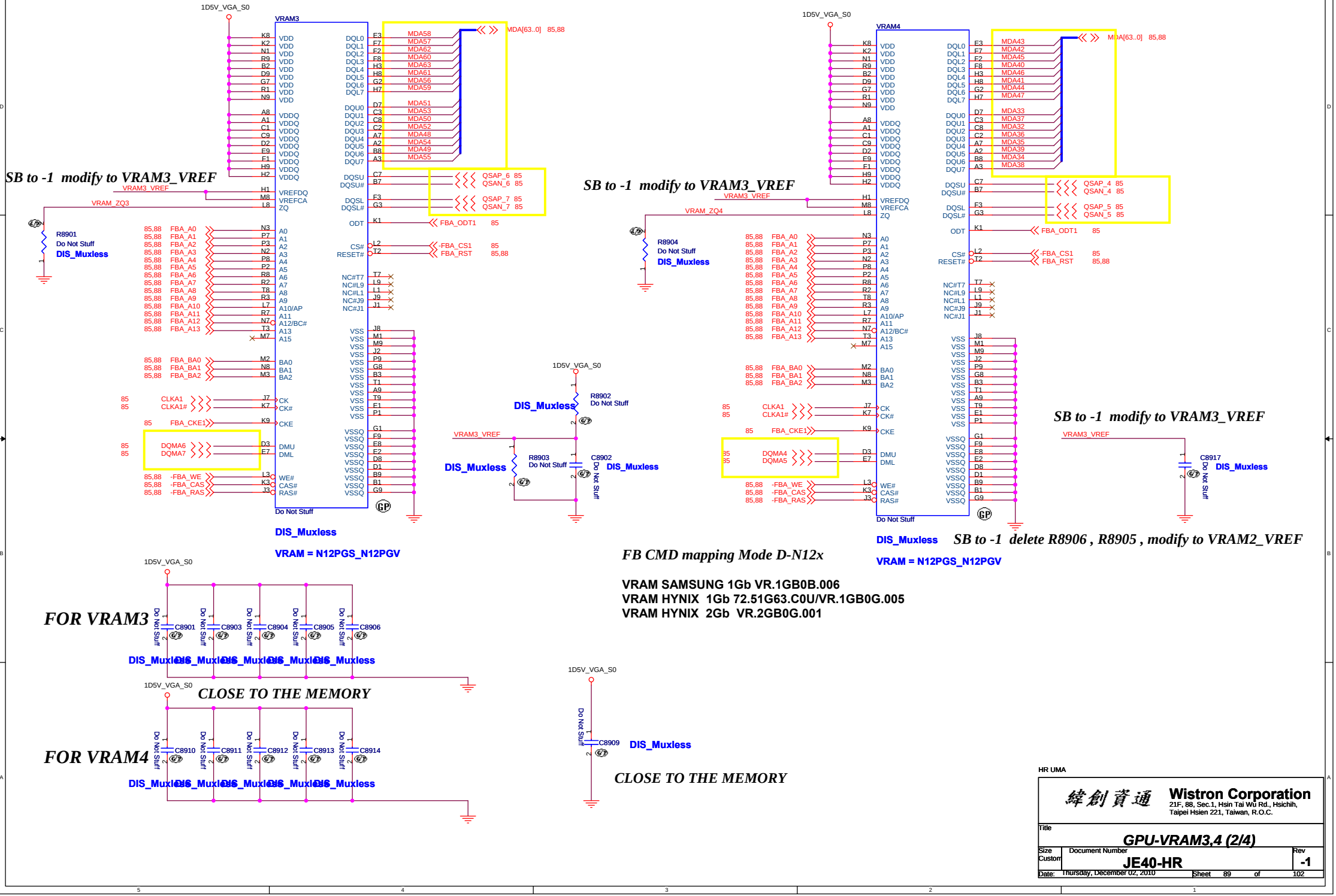
HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

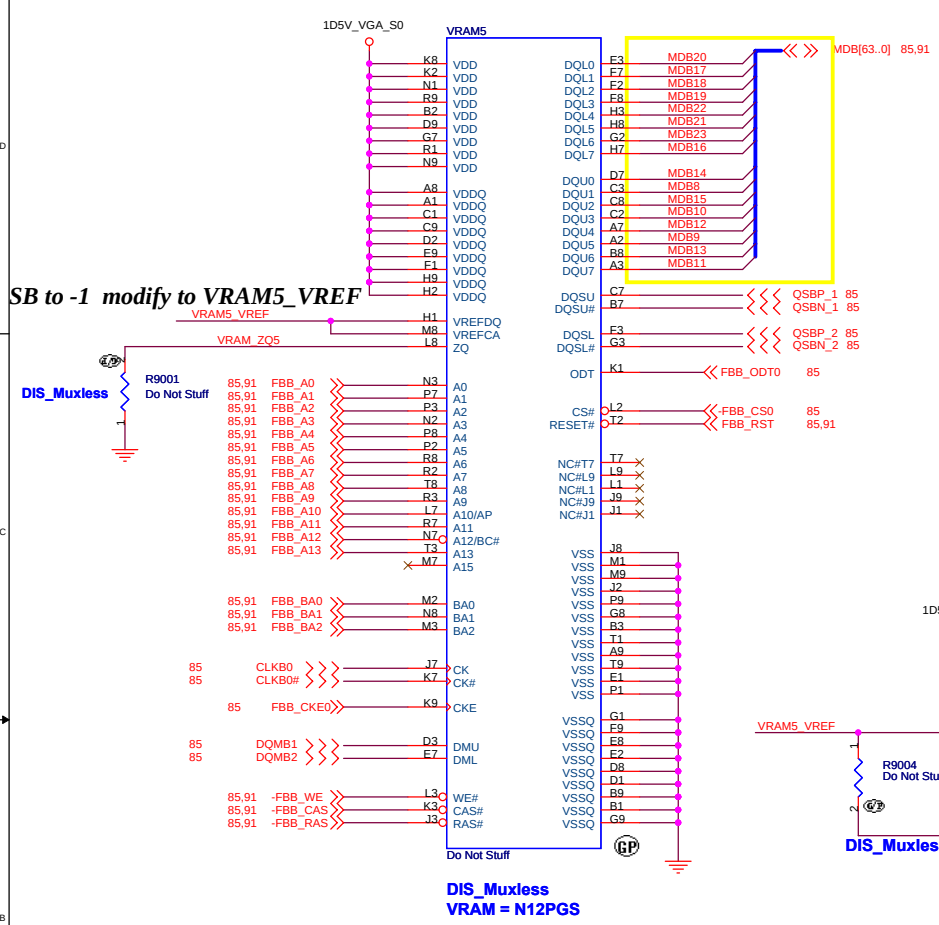
Size	Document Number	Rev
Custom	JE40-HR	-1

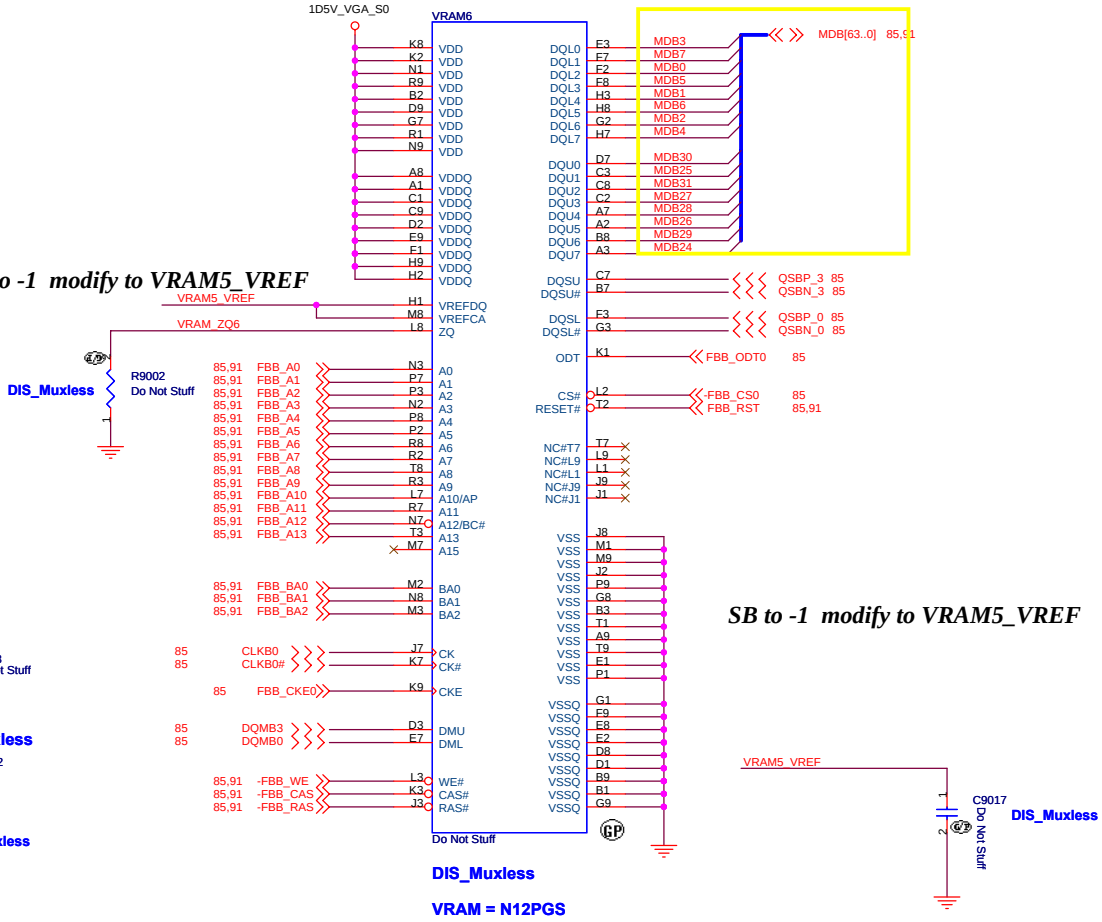
Date: Thursday, December 02, 2010 Sheet 88 of 102



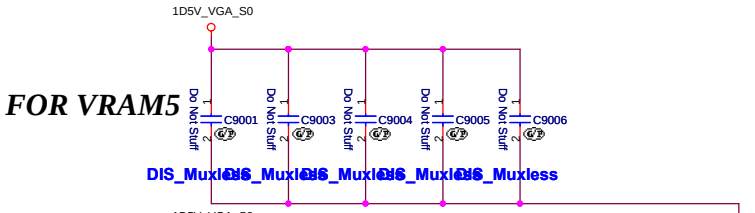
HR UMA

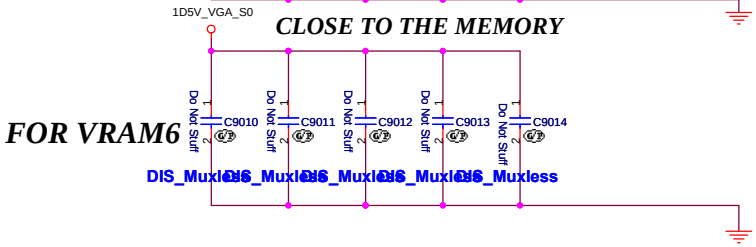
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	GPU-VRAM3,4 (2/4)	
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 89 of 102	



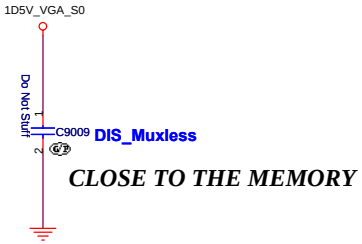


VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001





DG requires 4x0.1uF and 8x1.0uF per VRAM chip



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
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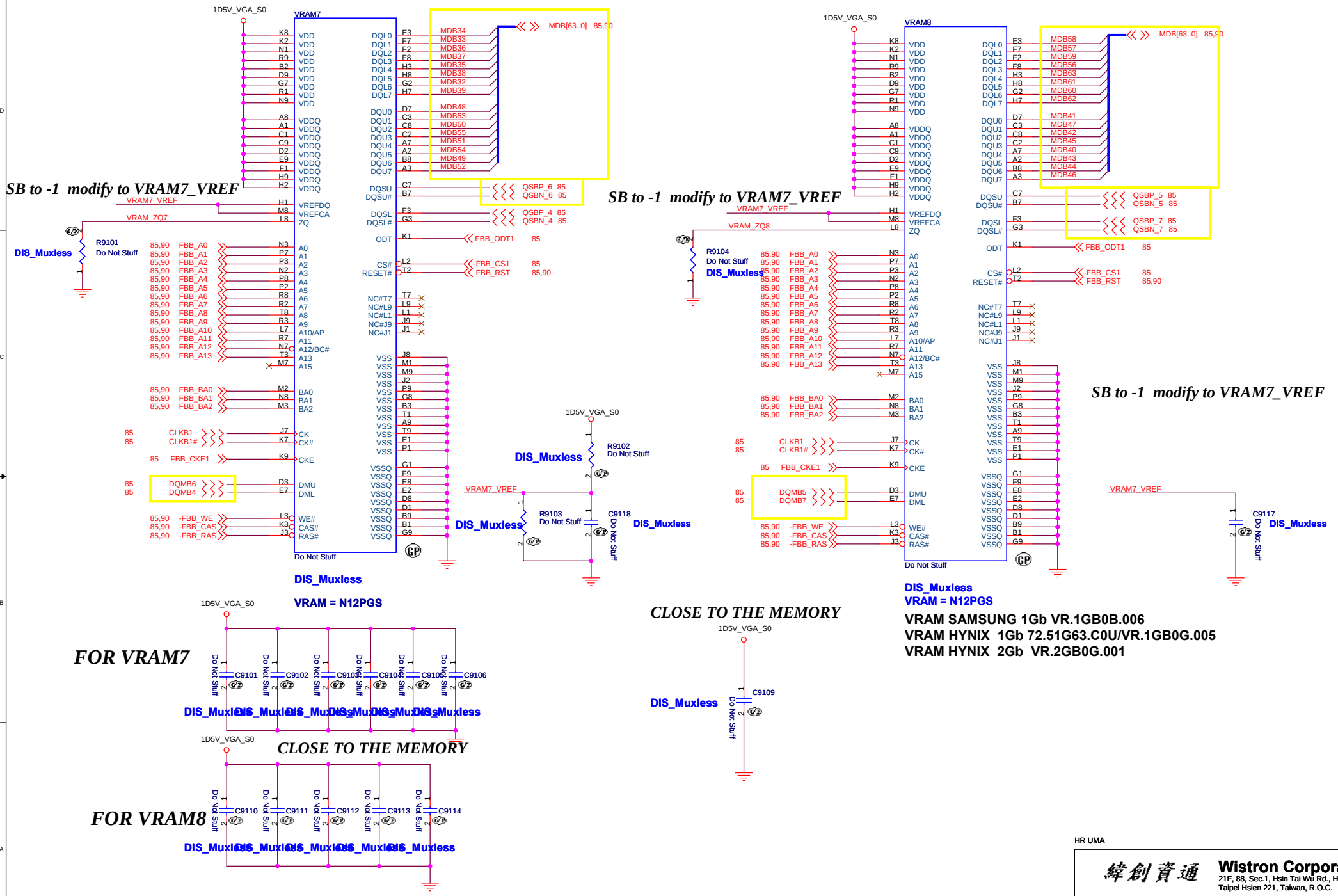

HR UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**GPU-VRAM7,8 (4/4)**	
Size: Custom	Document Number: **JE40-HR**	Rev: **-1**
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20100715

SSID = PWR.Plane.Regulator_GFX

20100719

SB 20100831

20100715

SB 20100831

Vout=0.75V*(R1+R2)/R2

Design Current = 21.94A
24.14A<OCP< 28.53A

RT8208A

N12P GS

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.825V
P0 - HOT	L	H	0.975V
P0 - COLD	H	L	1.00V
	H	H	

SB to -1 modify PR9213 VGA_Core to 1.05V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

Switching freq-->350KHz

Frequency setting
470K -->165KHz
200K -->323KHz
100K -->500KHz

Vout=0.75V*(R1+R2)/R2

N12P GV

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.85V
P0 - HOT	L	H	1.00V
P0 - COLD	H	L	1.025V
	H	H	

HR UMA

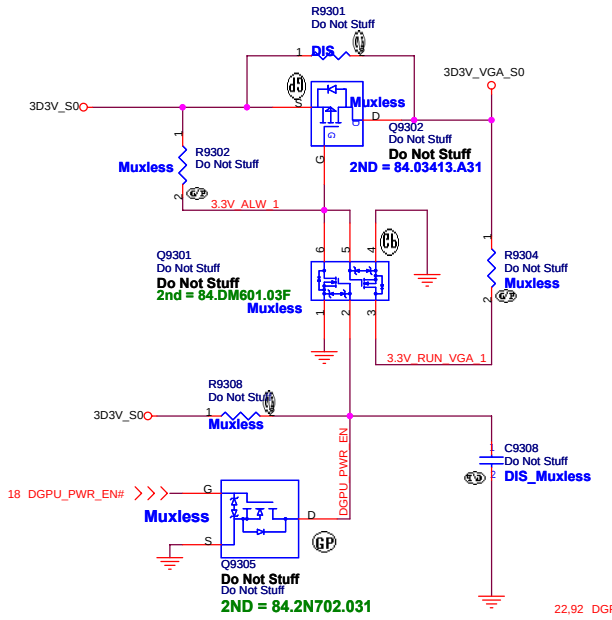
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208B +VGA_CORE

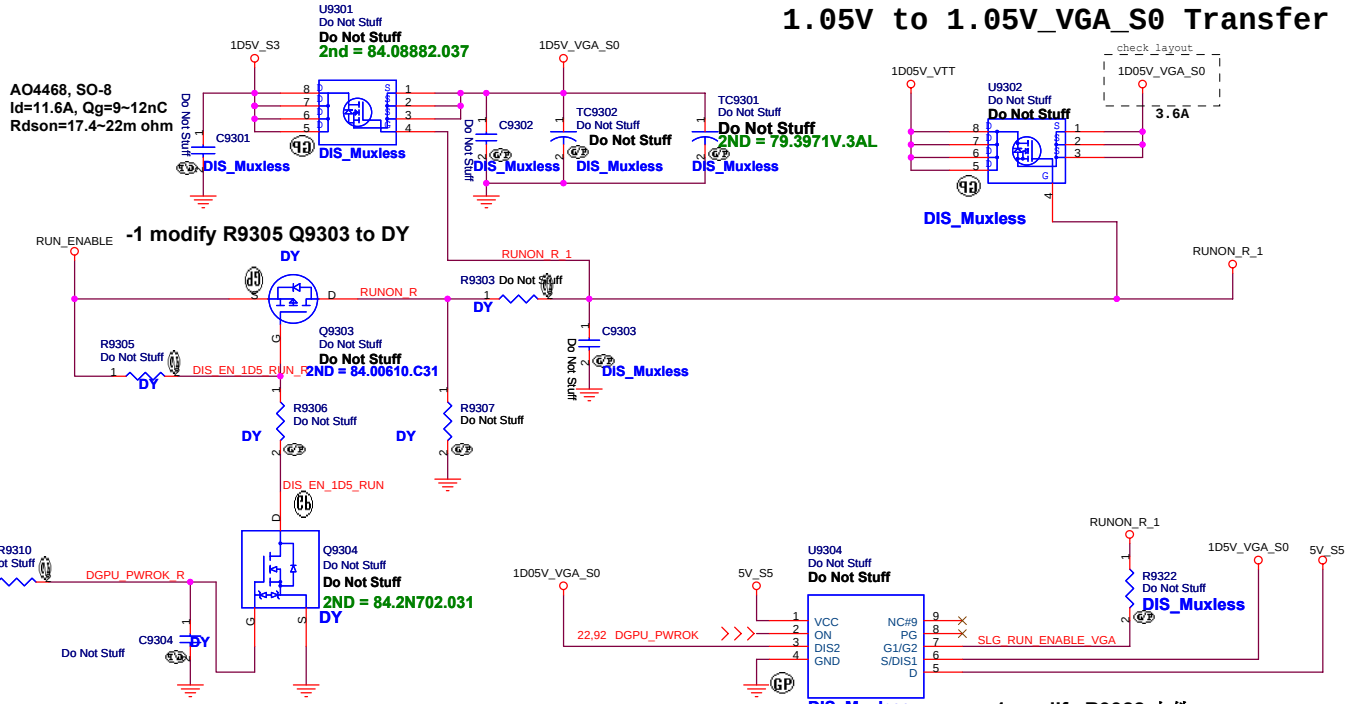
Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 92 of 102

+3VS to 3.3V_DELAY Transfer



1D5V_VGA_S0

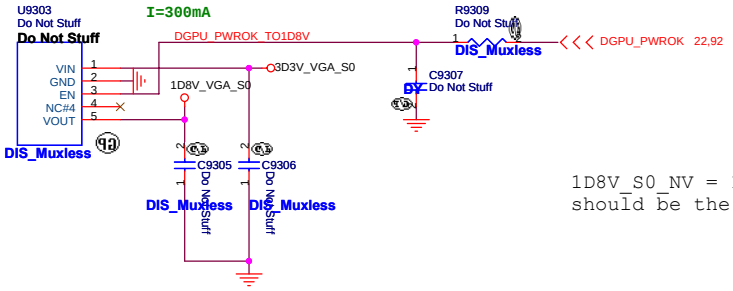


SB modify to 84.03006.A37

1.05V to 1.05V_VGA_S0 Transfer

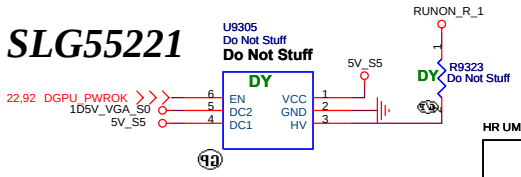
RT9025 for 1D8V_VGA

+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

-1 co-layout SLG55221



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size: Custom | Document Number: JE40-HR | Rev: -1

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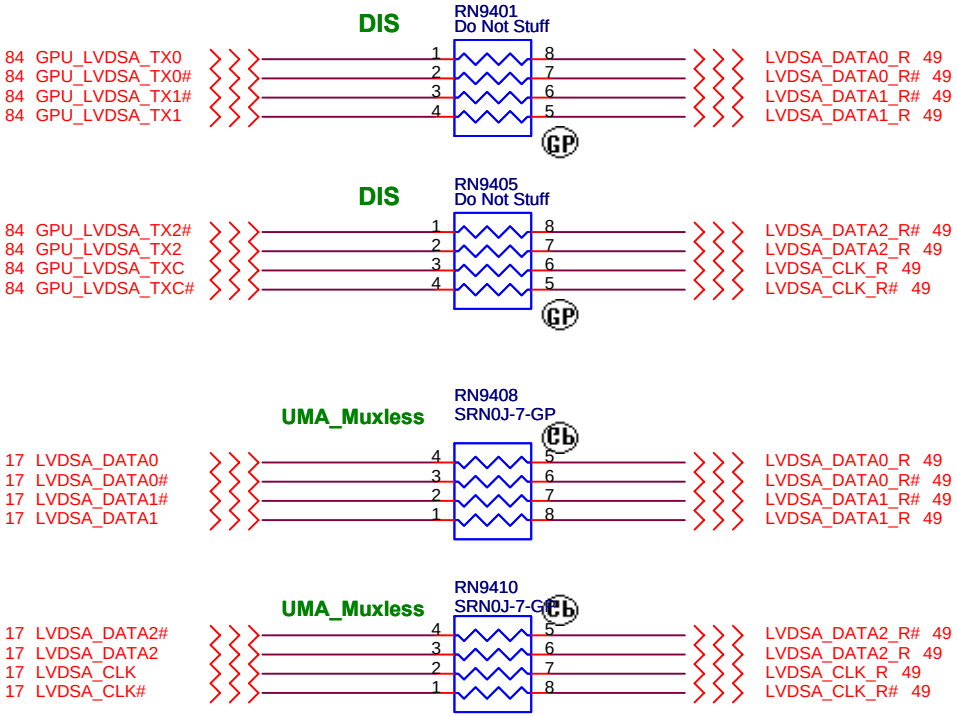
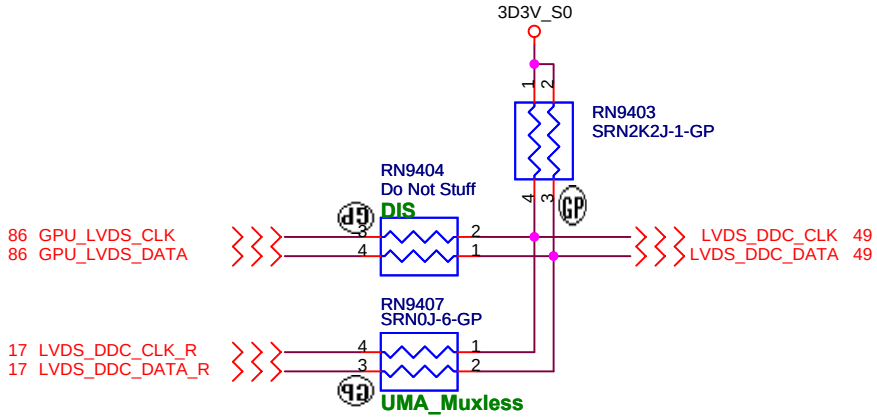
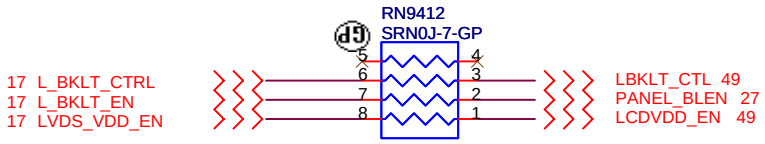
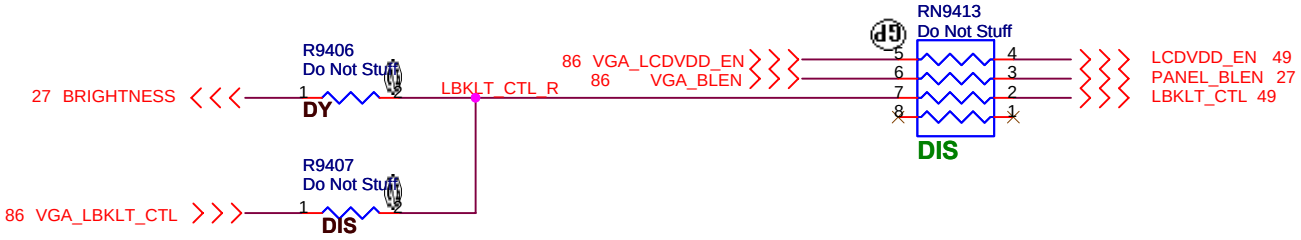
LVDS Channel A





Panel BL brightness/Power En/BL En





HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LVDS_Switch*

Size	Document Number	Rev
A4	JE40-HR	-1

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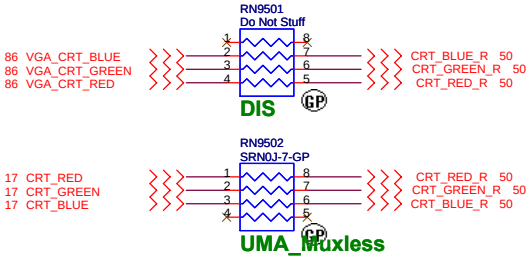
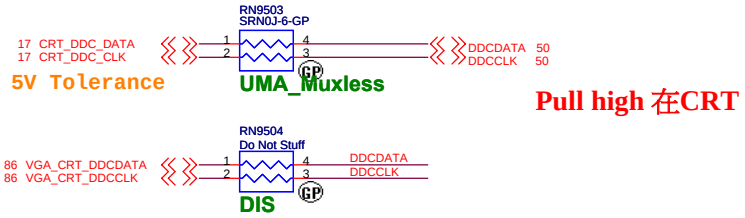
Close to CRT Board CONN

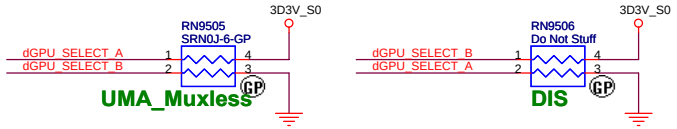


CRT DDCDATA & DDCCLK



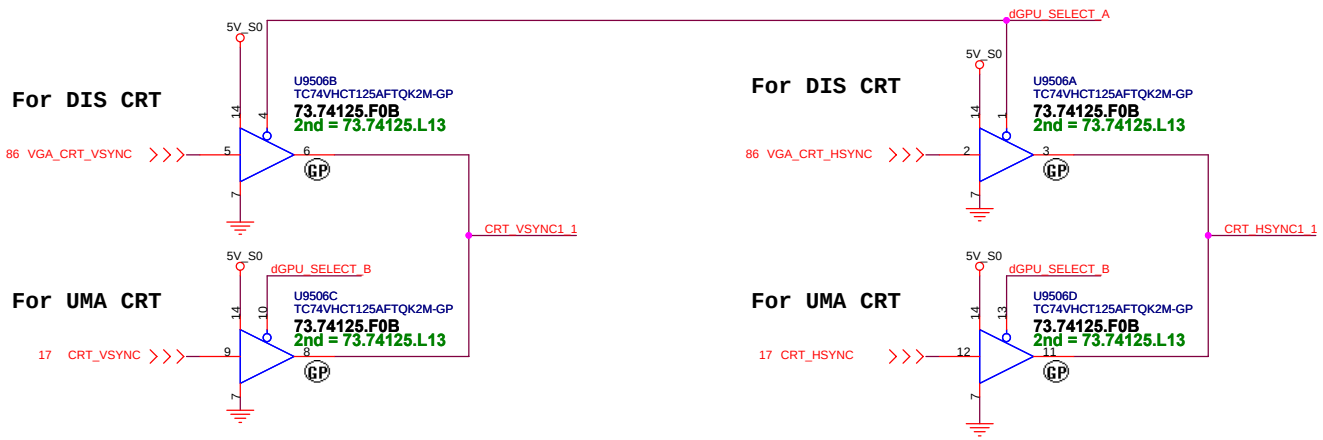
Pull high 在CRT

SB to -1 modify 4 port Logic



CRT Hsync & Vsync level shift

L=>B0 -DIS
H=>B1 -UMA



SB to -1 modify R9503,R9504 to 10 ohm

HR UMA

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Title: CRT Switch

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SSID = SDIO

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Title: ***TOUCH PANEL***

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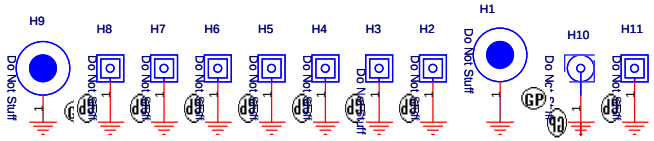
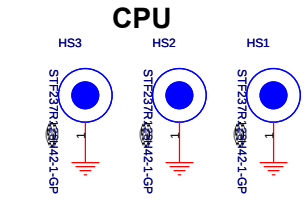
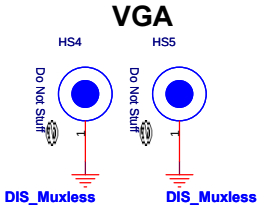
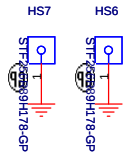
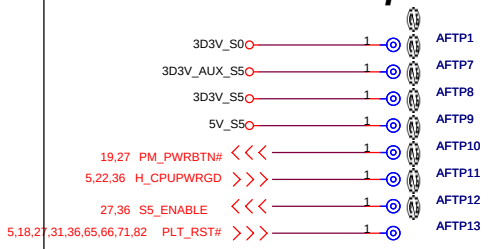








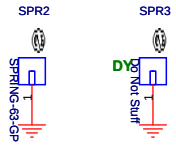
Check test point



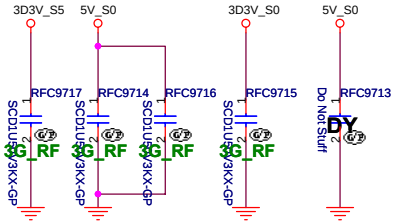
Test Point放在Dimm Door打開可量測處

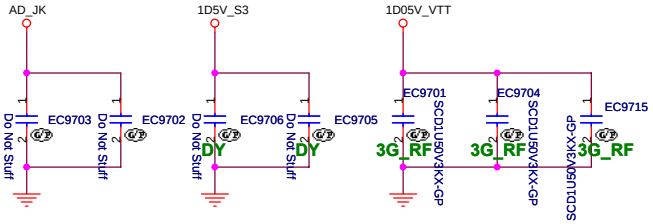
SB to -1 BOM add SPR2

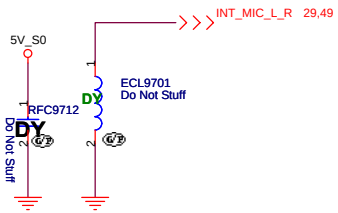
-2 delete SPR5

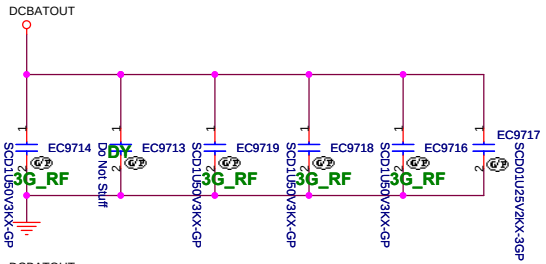


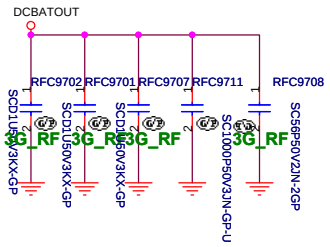
Change:34.40V16.001

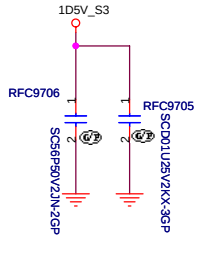


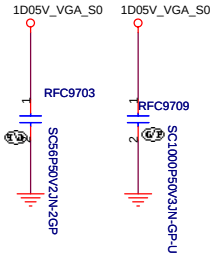


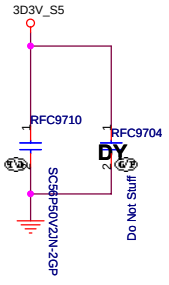


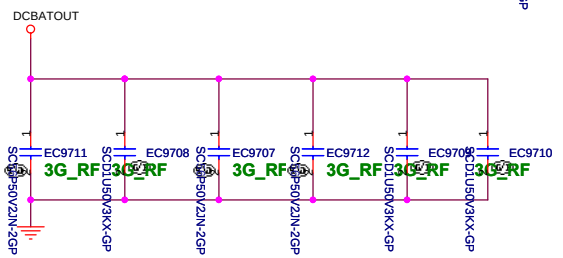












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Title: **UNUSED PARTS/EMI Capacitors**

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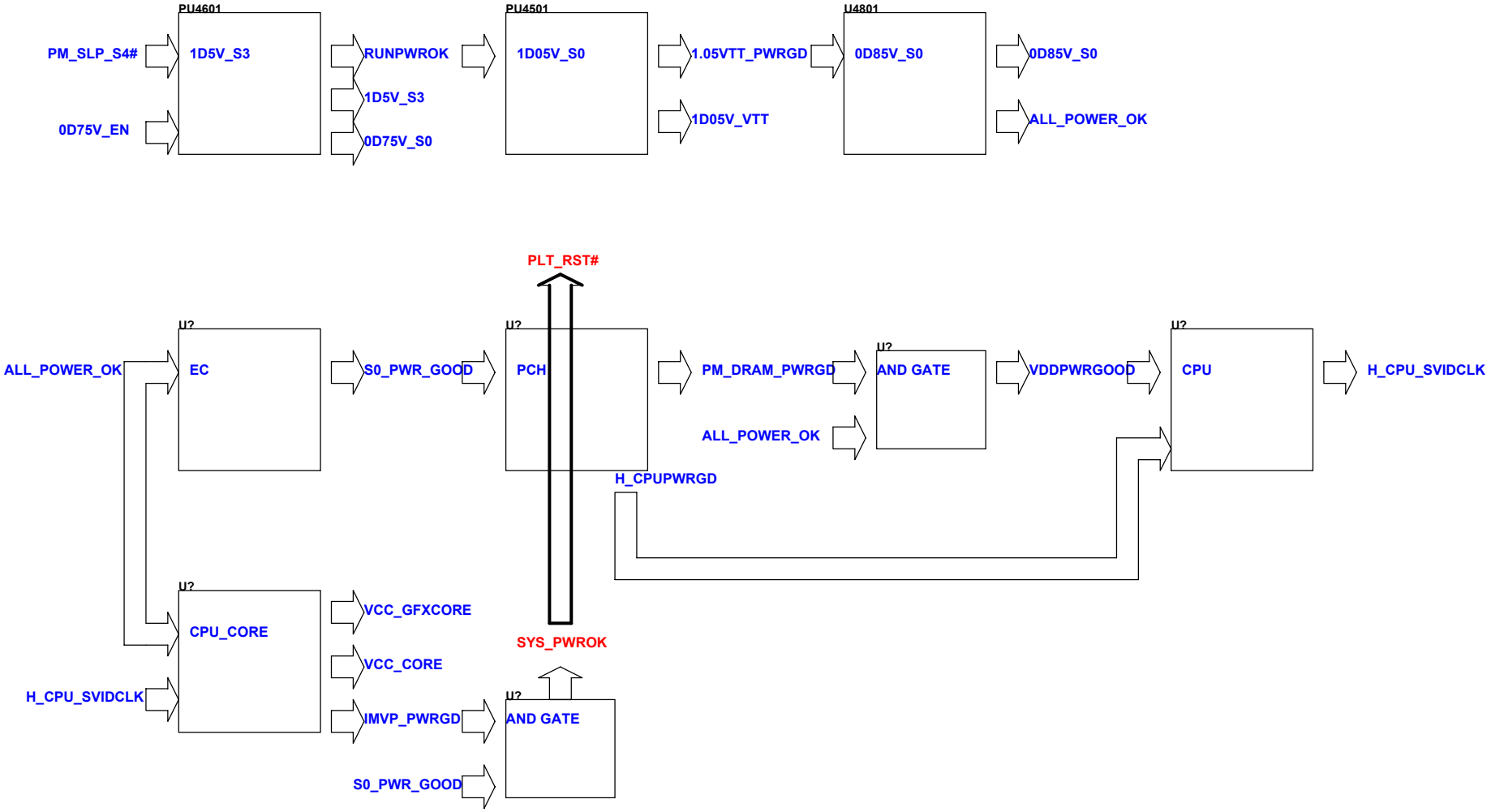
Power Sequence



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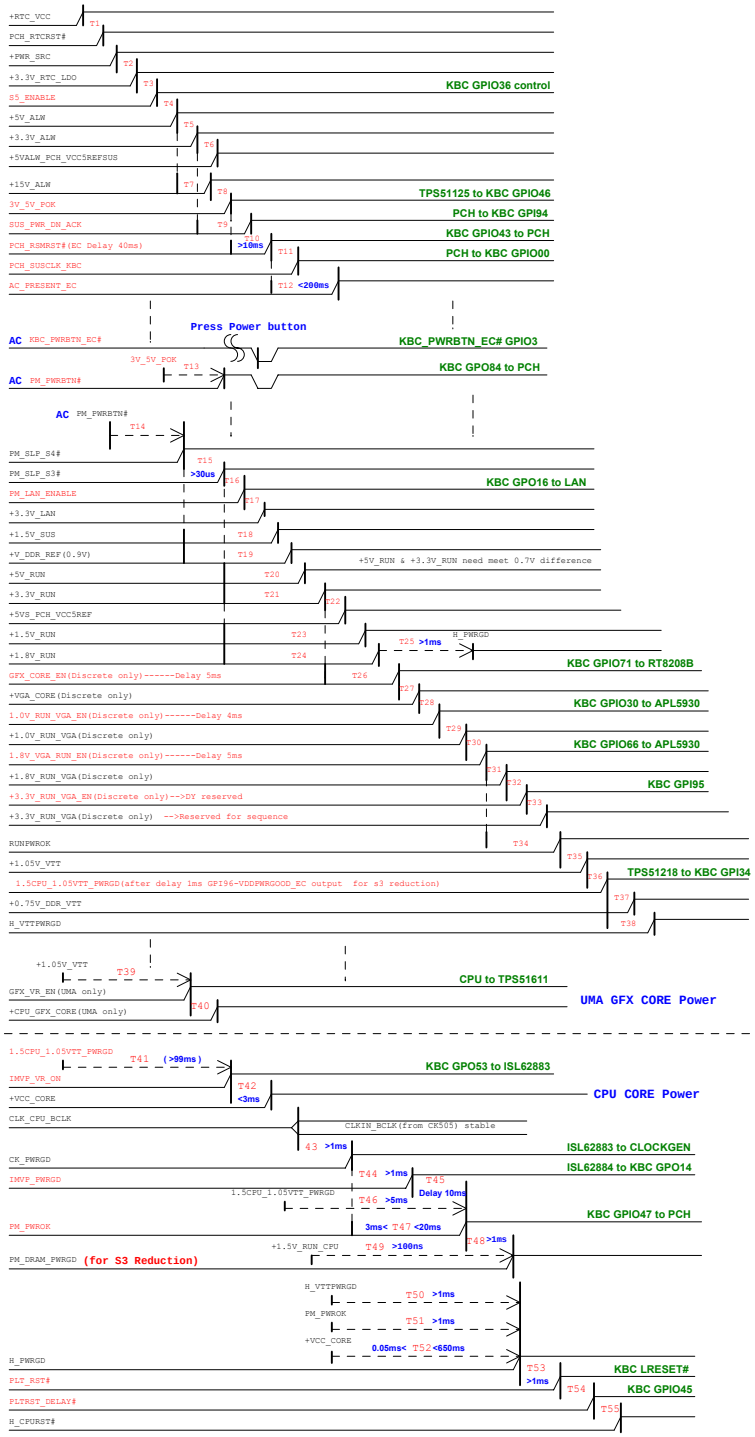
Intel-Power Up Sequence

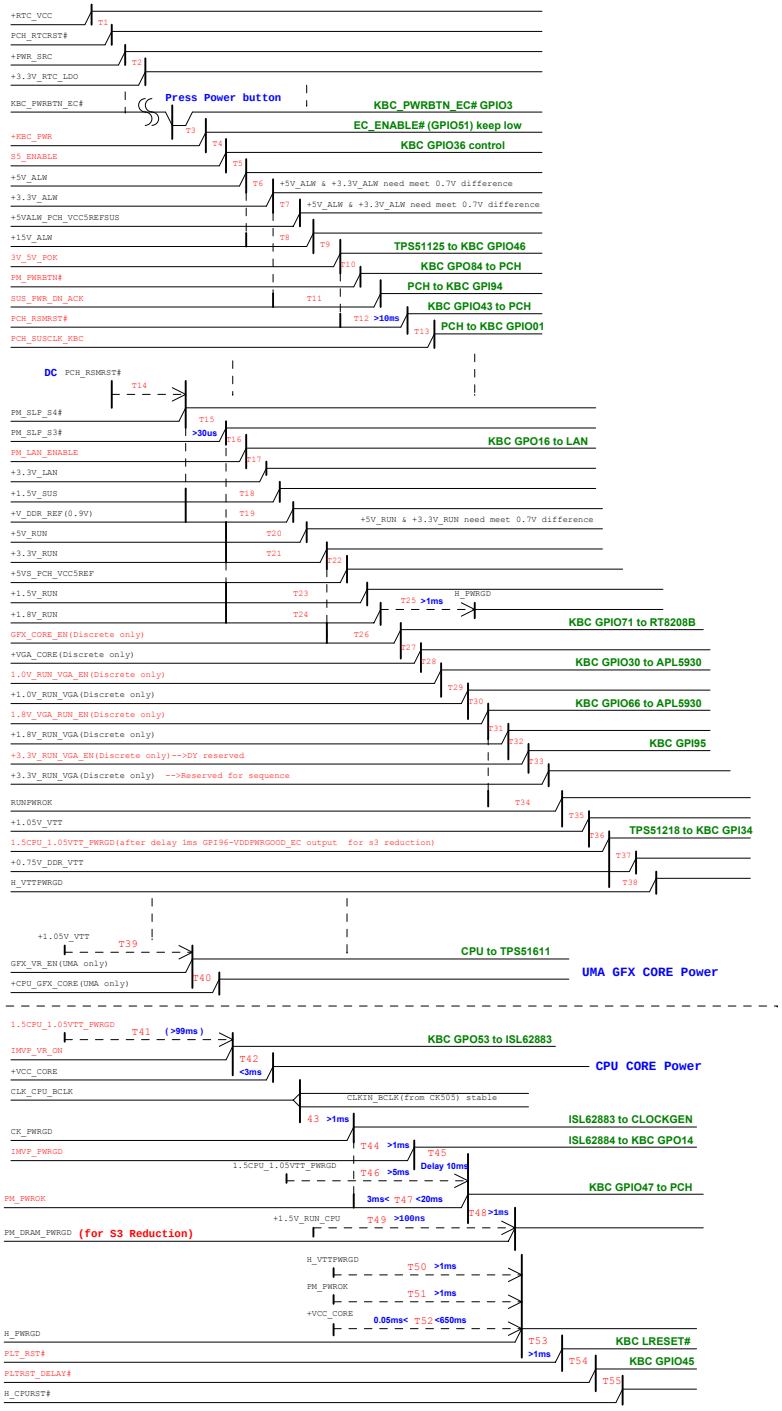
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



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Title: Power Sequence

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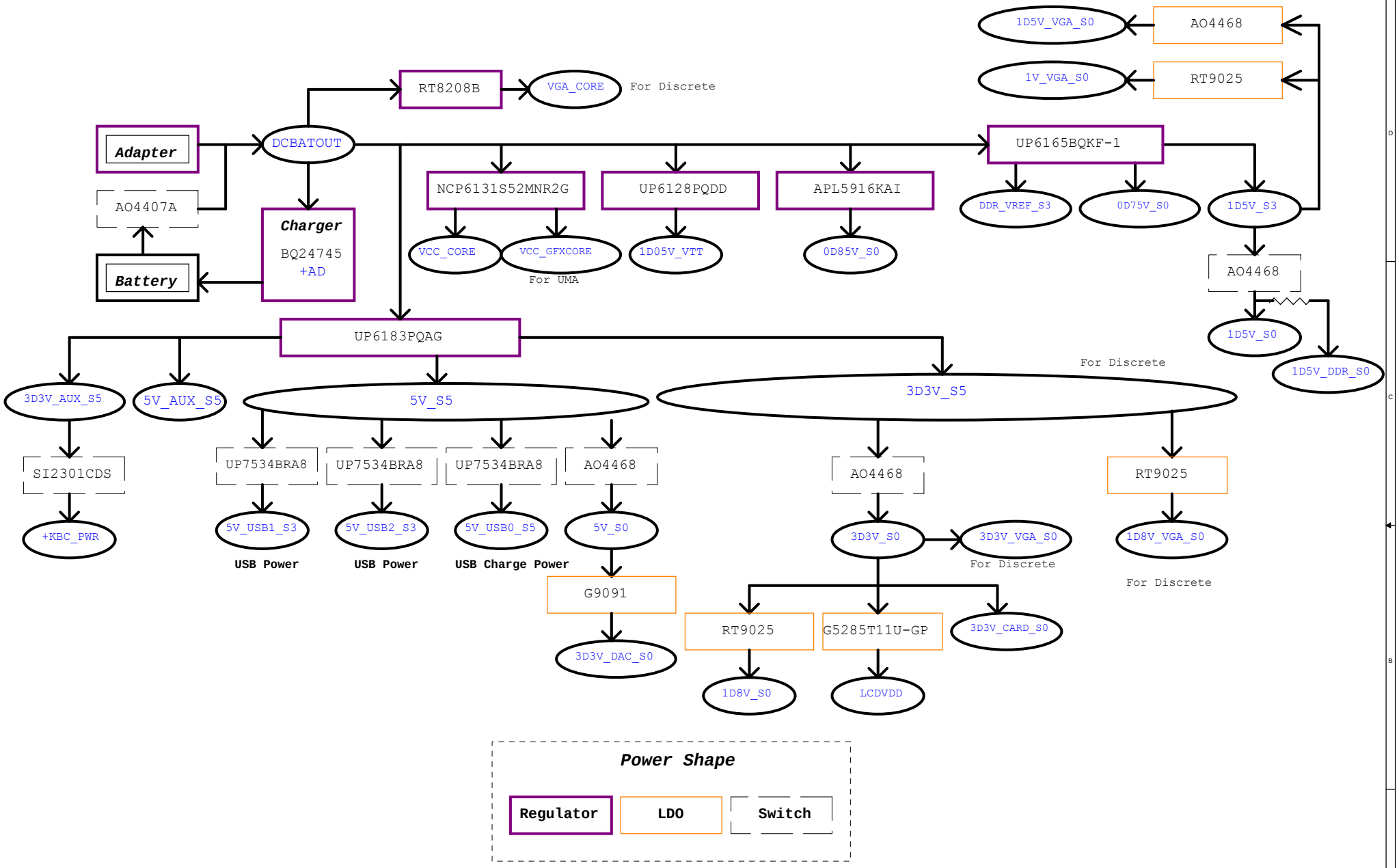

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Title: **Power Block Diagram**

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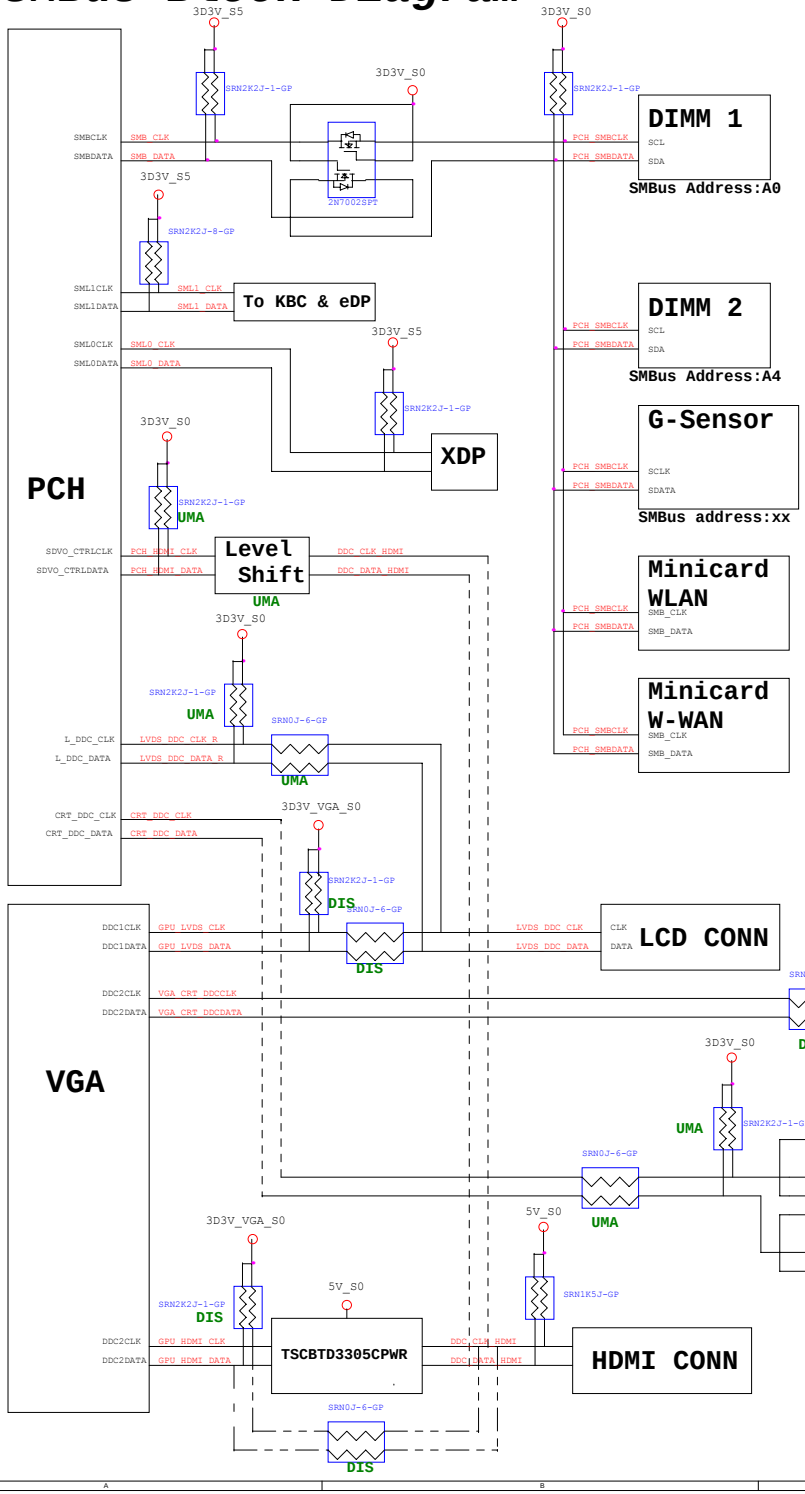
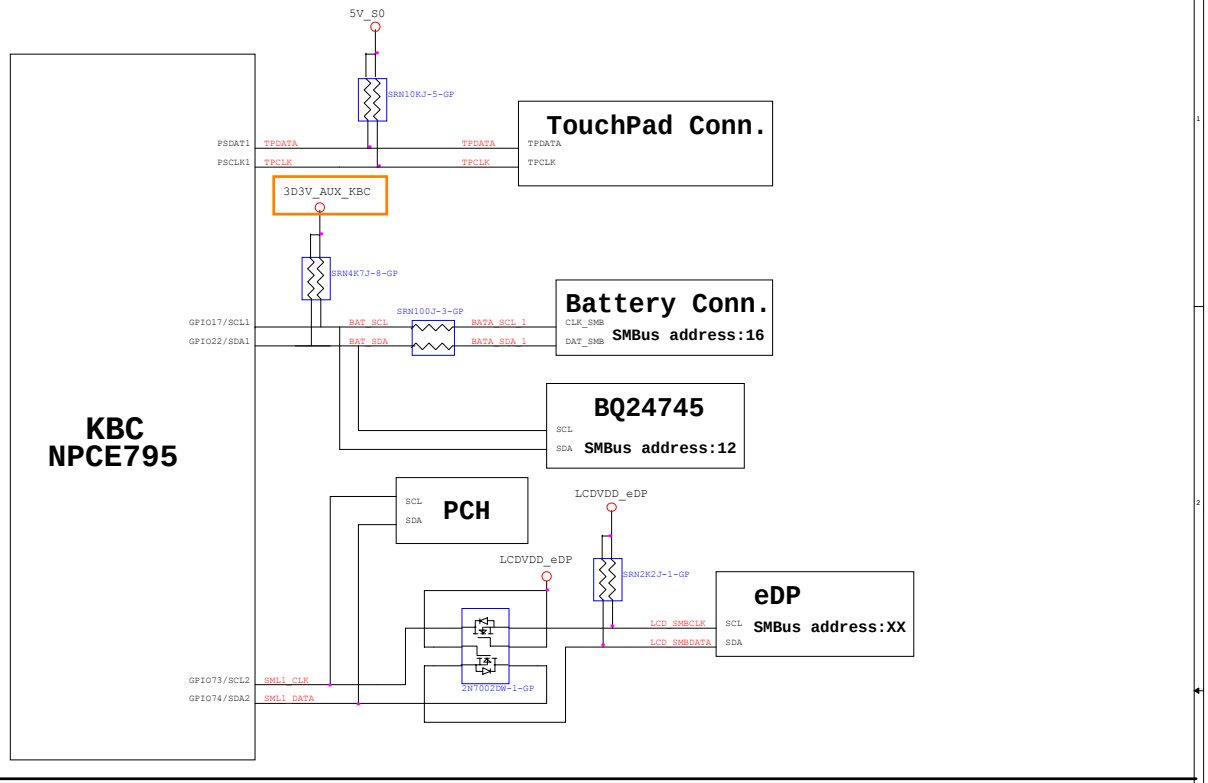
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram		
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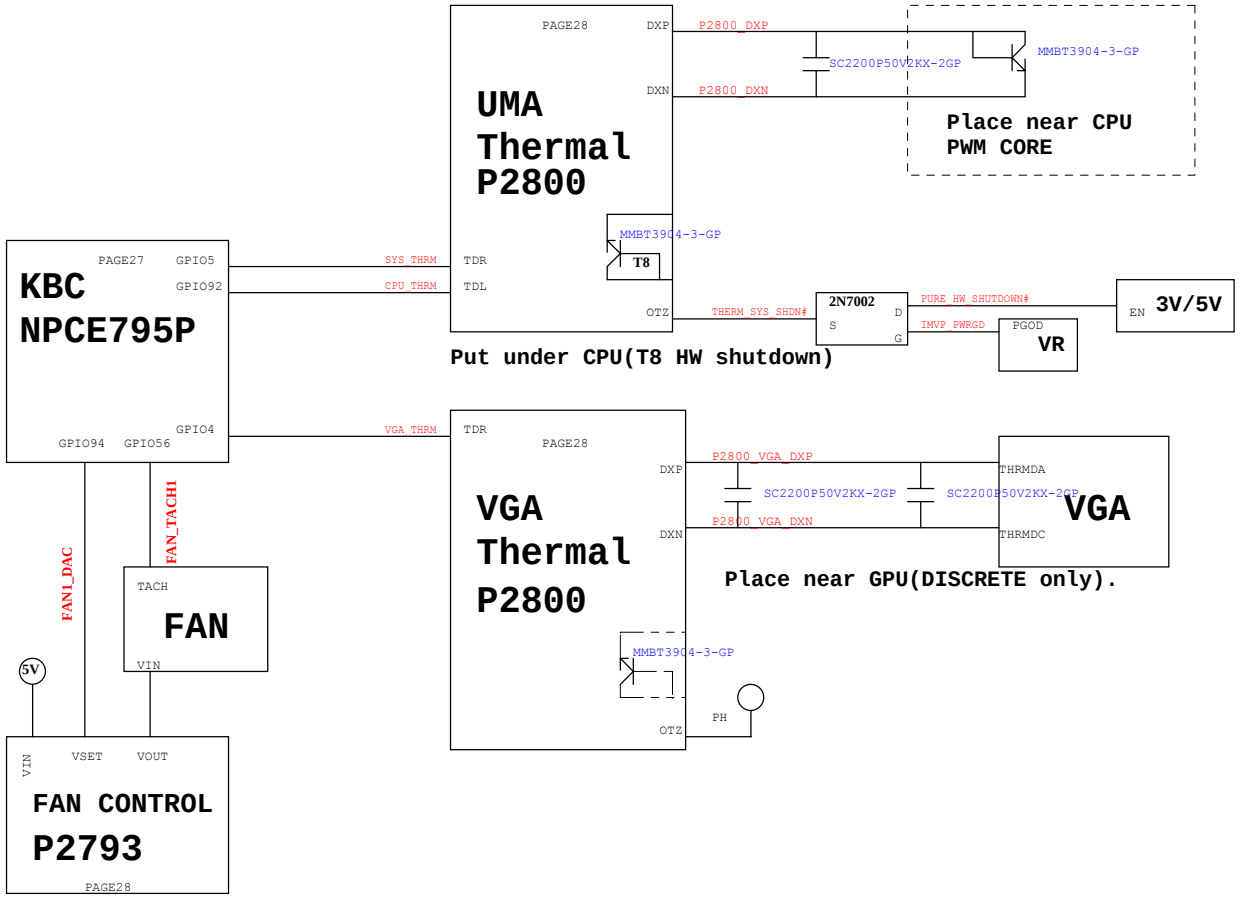
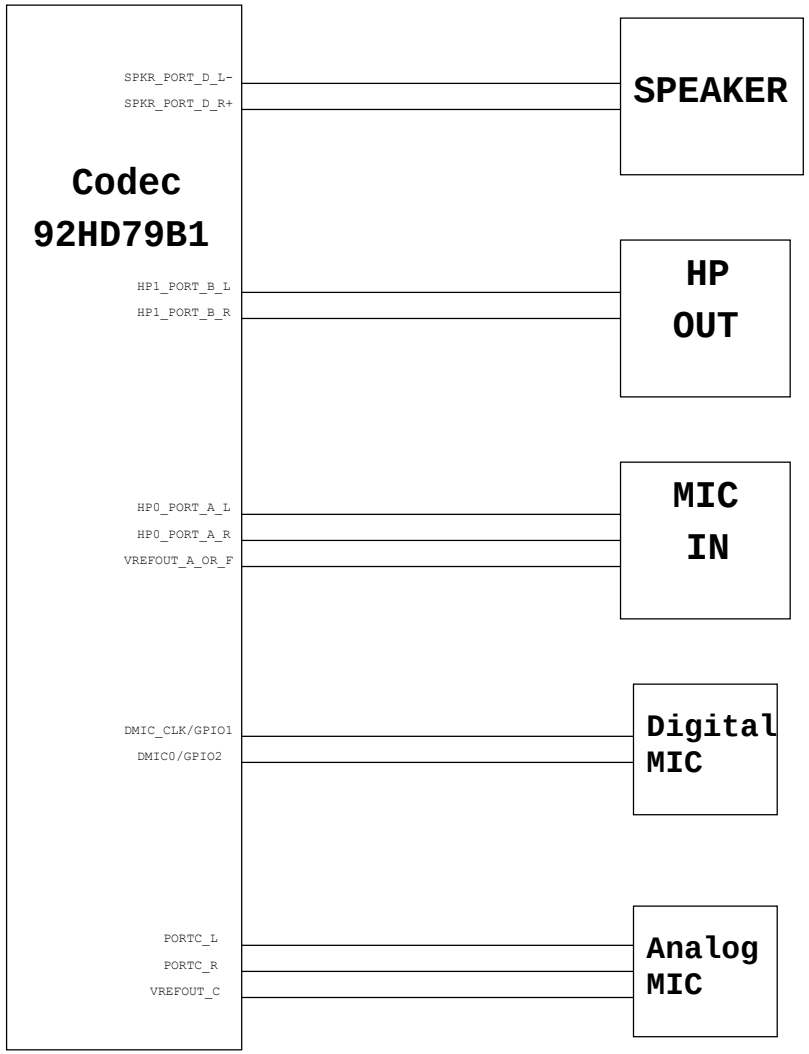
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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